IIT Bhubaneswar

School of Electrical Sciences

COA Lab (0-0-3)

Autumn 2022

Lab Schedule: Monday (2:30PM-5:30 PM)

Instructor: Debi Prosad Dogra (dpdogra@iitbbs.ac.in)

Teaching Assistant: Soumya/Manish

Submission Deadline: 09-10-2022 (midnight)

Assignment 4 (Mini Project)

Points: 200

Problem Statement: Designing of a 32-bit RISC processor that will support the following assembly instructions:

MOVE R i , R j \\The content of R j is transferred to R i .

MOVE R i , Immediate (16-bit) \\The immediate value (32-bit unsigned extended) will be transferred to Ri .

LOAD R i , X (R j) \\ The content of memory location [[R j] + X] is loaded into R i , where X is a 16-bit unsigned immediate value.

STORE R i , X (R j) \\ The content of register R i is stored in memory [[R j] + X], where X is a 16-bit unsigned immediate value.

ADD R i , R j , R k \\ R i = R j + R k .

ADI R i , R j , Immediate (16-bit) \\ R i = R j + Immediate Value (32-bit unsigned extended)

SUB R i , R j , R k \\ R i = R j - R k

SUI R i , R j , Immediate (16-bit) \\ R i = R j - Immediate Value (32-bit unsigned extended)

AND R i , R j , R k \\ R i = R j AND R k .

ANI R i , R j , Immediate (16-bit) \\ R i = R j AND Immediate Value (32-bit unsigned extended)

OR R i , R j , R k \\ R i = R j OR R k .

ORI R i , R j , Immediate (16-bit) \\ R i = R j OR Immediate Value (32-bit unsigned extended)

HLT (Stops the execution).

Additional Information: The instructions will be executed sequentially. So, the next instruction will be fetched from the memory only after the current instruction completes it execution. Each instruction will go through all 5 stages of the pipeline. All registers are 32-bit. The intermediate registers needed can be decided as per your design. There is no need to exactly follow the pipeline discussed in the class. You can use any built-in components (including memory) available in the Logisim for designing the circuit. There will be at least 4 GPRs (32-bit) in the system. Other special purpose registers may be included as needed. The control unit should be designed using hardwired control mechanism. The design will be tested against a few sample assembly codes. Ensure the memory has sufficient space to store at least 32 instructions and 32 data. Provide a reset signal that will set the value of PC to 0. The programs should be written from the memory location 0.

Submission Documents:

1) A PDF/DOC file containing the complete encoding scheme of the instructions as per your design. This should clearly identify various fields of the instructions. Also, provide an assembler table that will be used convert an assembly code into machine code as per your design.

2) A PDF/DOC file with the block-level diagram of the implementation. Also, provide an overall 5-stage architecture similar to the diagram discussed in the class with all necessary stages, intermediate registers, and other components.

3) The Logisim circuit design file.

4) A readme file on how to use your design for execution. Mention any other information in this file.

N.B. Your design will be tested against 2-3 benchmark test programs that will be shared with you on a later date. Avoid copying from others as each design will be evaluated separately.