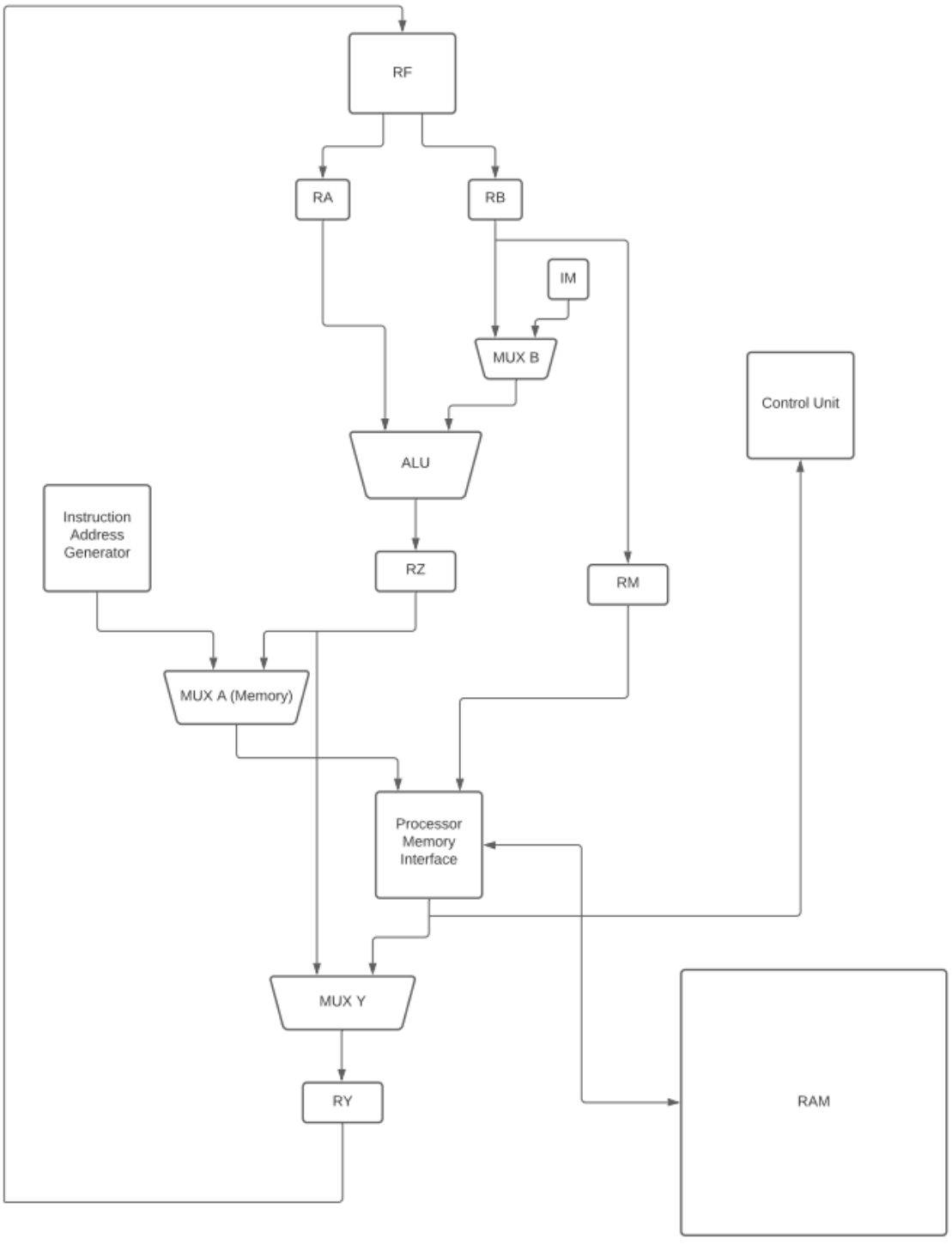
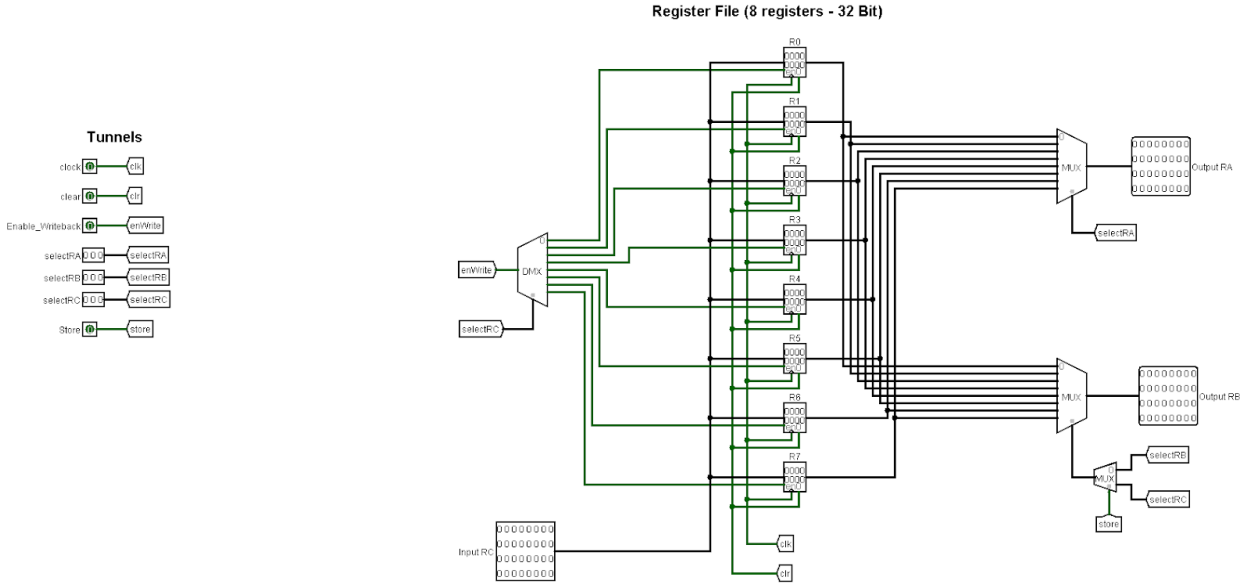
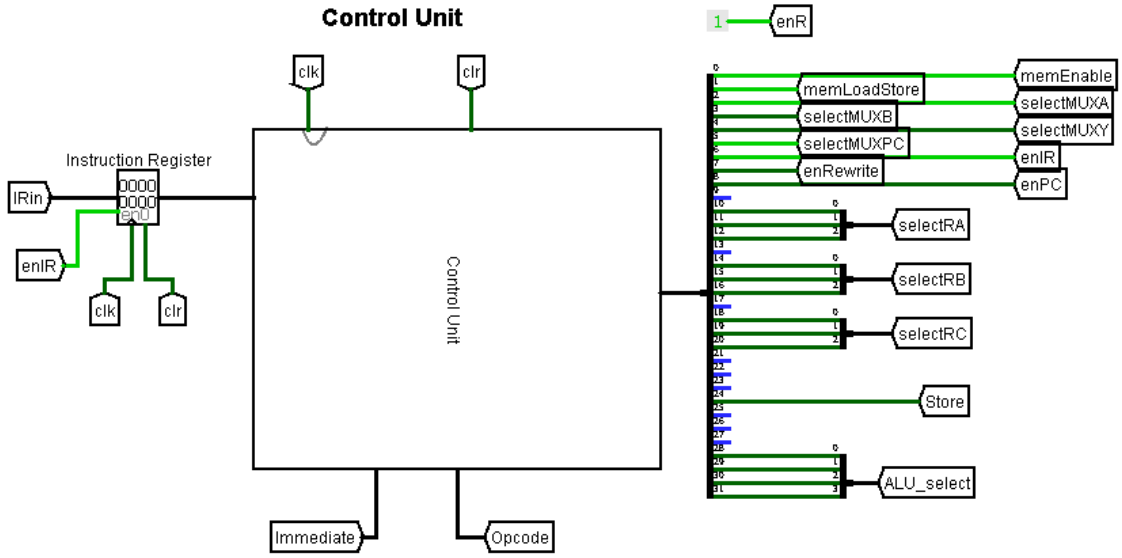
Block Diagram



Register File (RF)



Control Unit (CU)

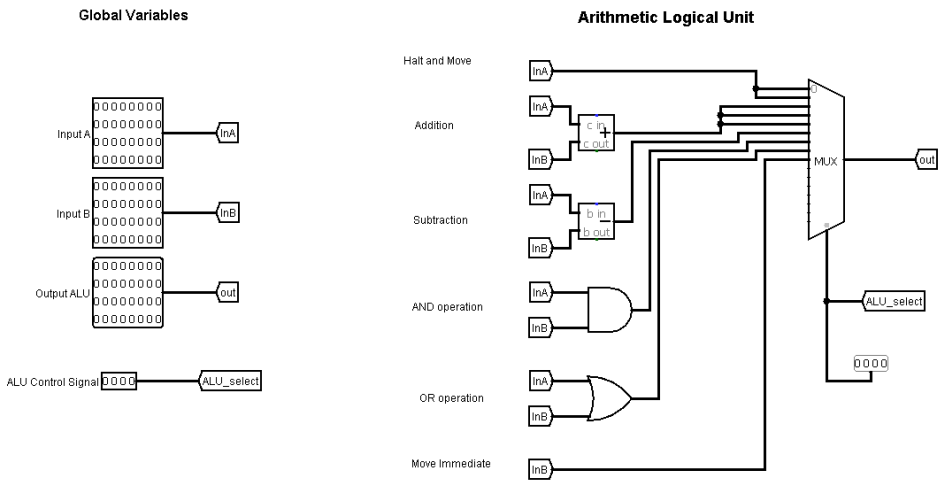


Instruction Encoding

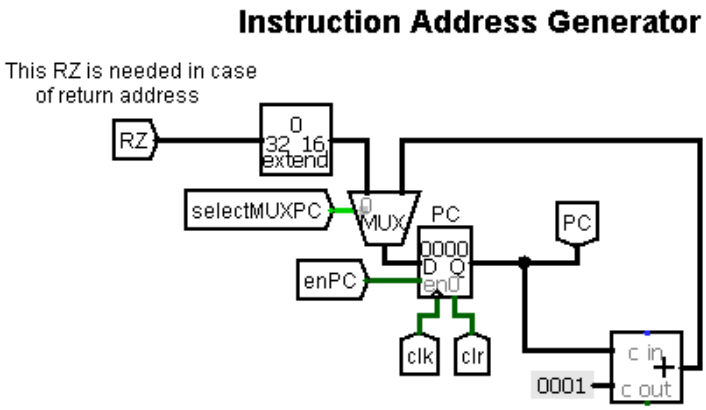
Opcode (5 bits)	Destination Register(Rc) - 5 bits	Source Register 1 (Ra) - 5 bits	Source Register 2 (Rb) - 5 bits	Immediate Value or Offset (11 bits)	Enable Immediate or Offset (1 bit)

Fig 1: Instruction Encoding Format

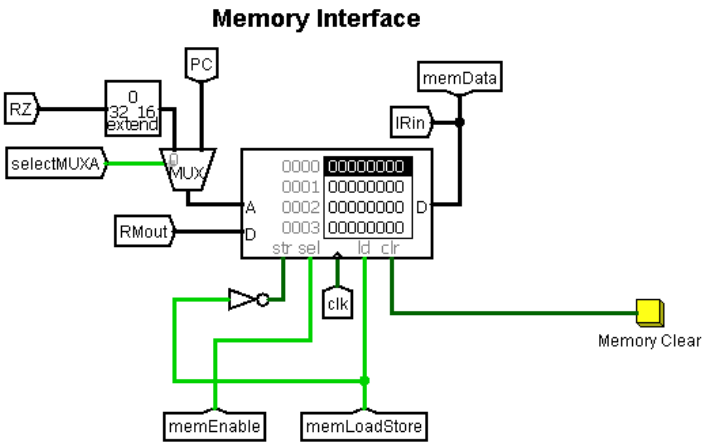
Arithmetic Logic Unit (ALU)



Instruction Address Generator (IAG)



Processor Memory Interface



Five Stage Complete Pipeline