Computer Organization and Architecture Lab

Project: Design a 32 - bit RISC Processor

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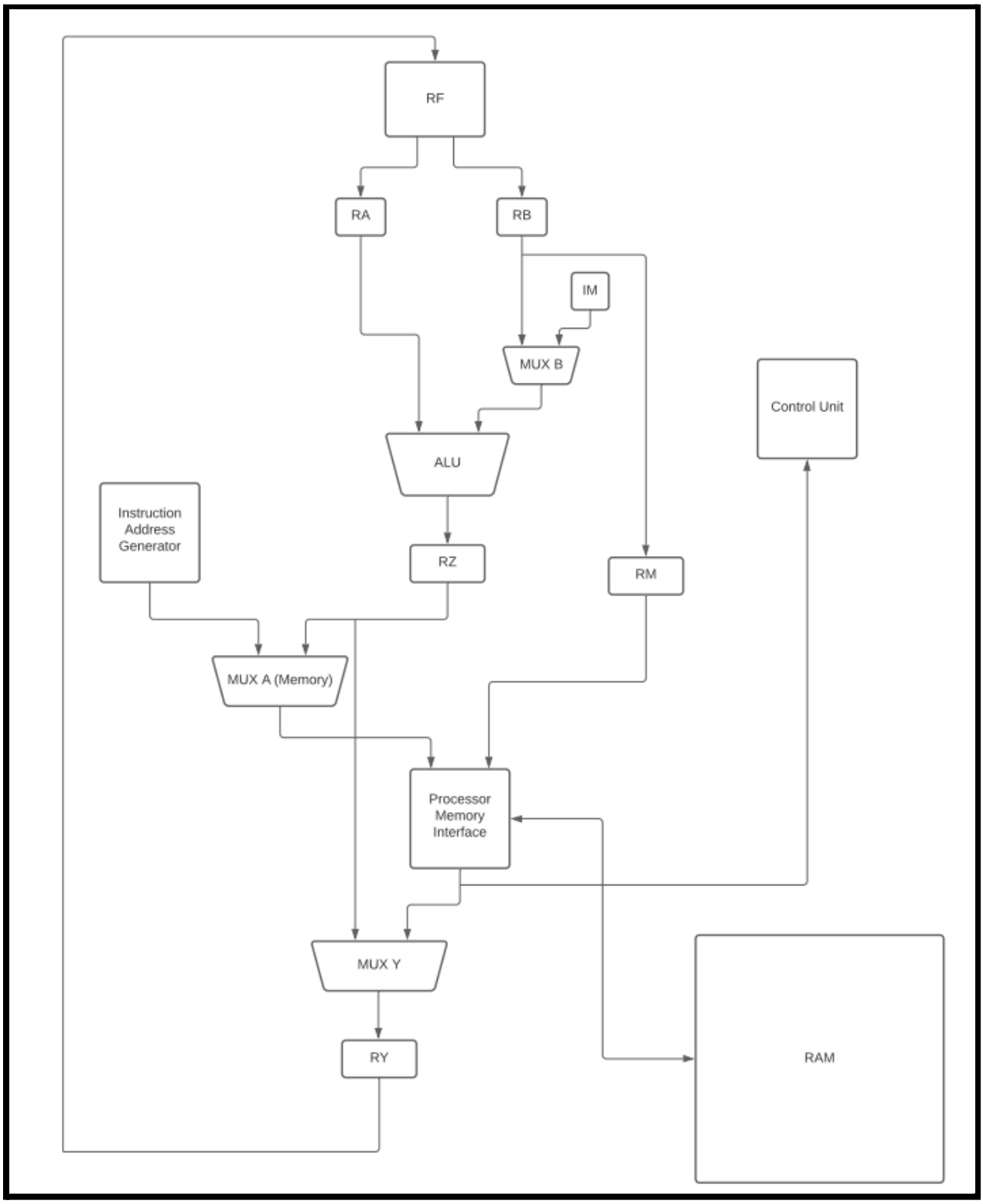
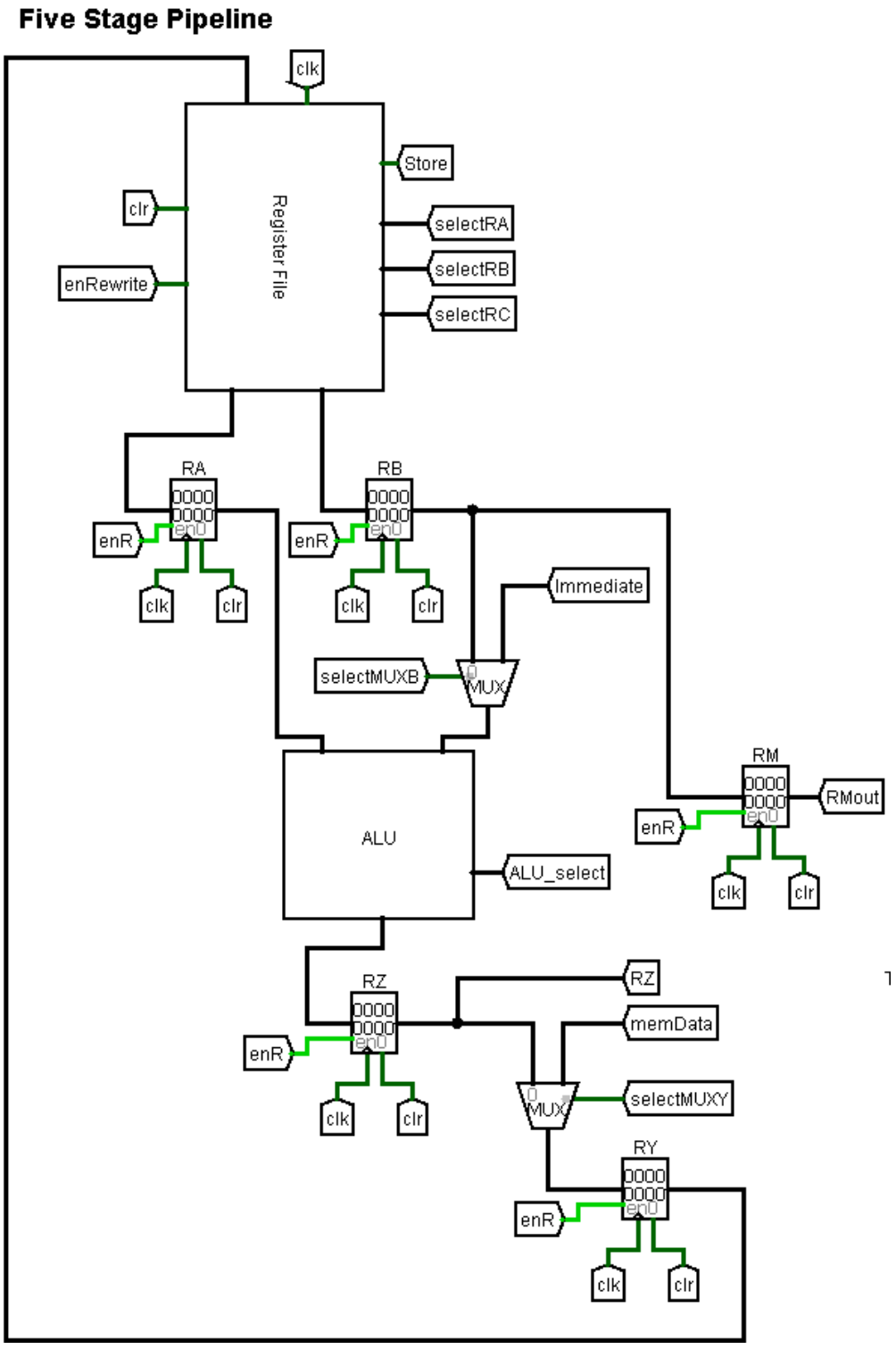
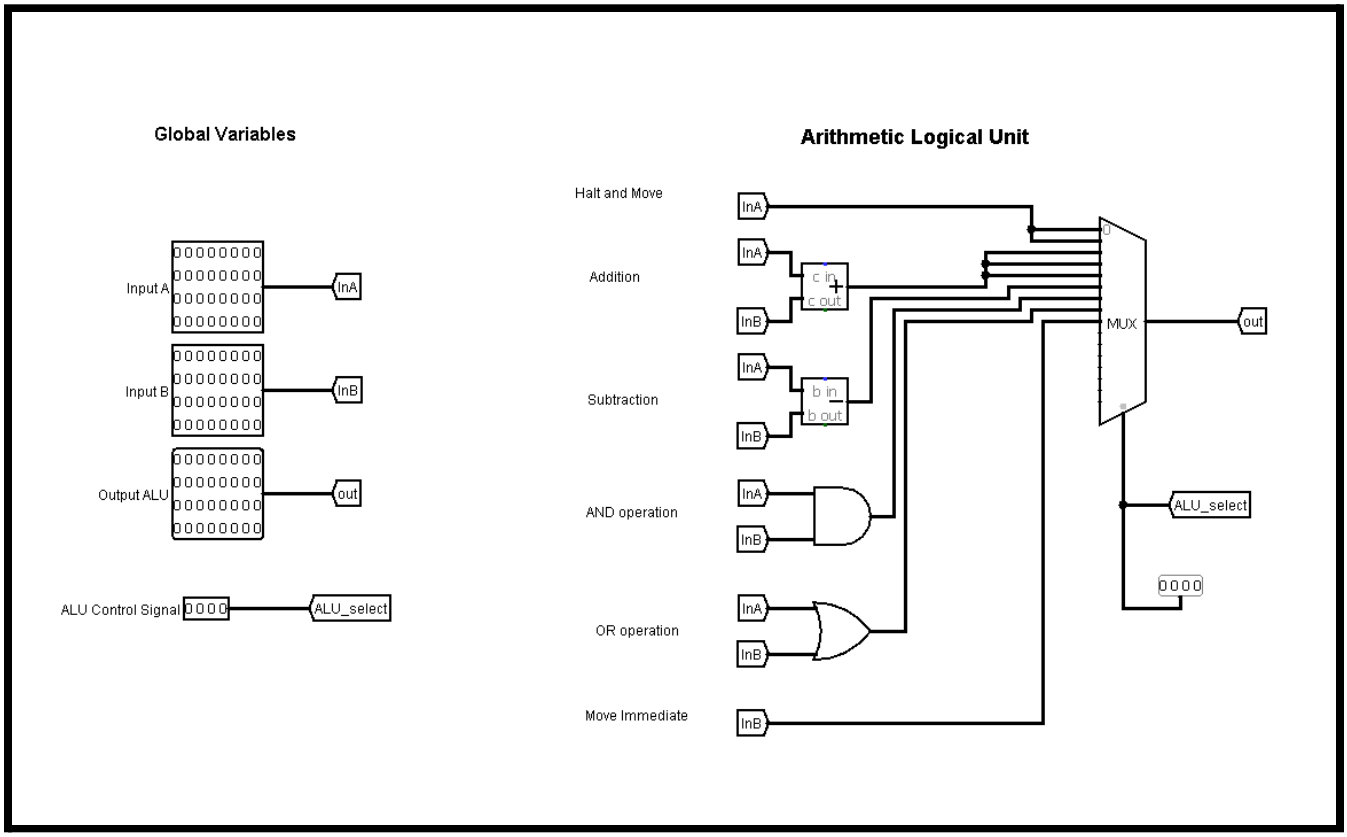
1. Block Diagram of the Five-Stage Architecture



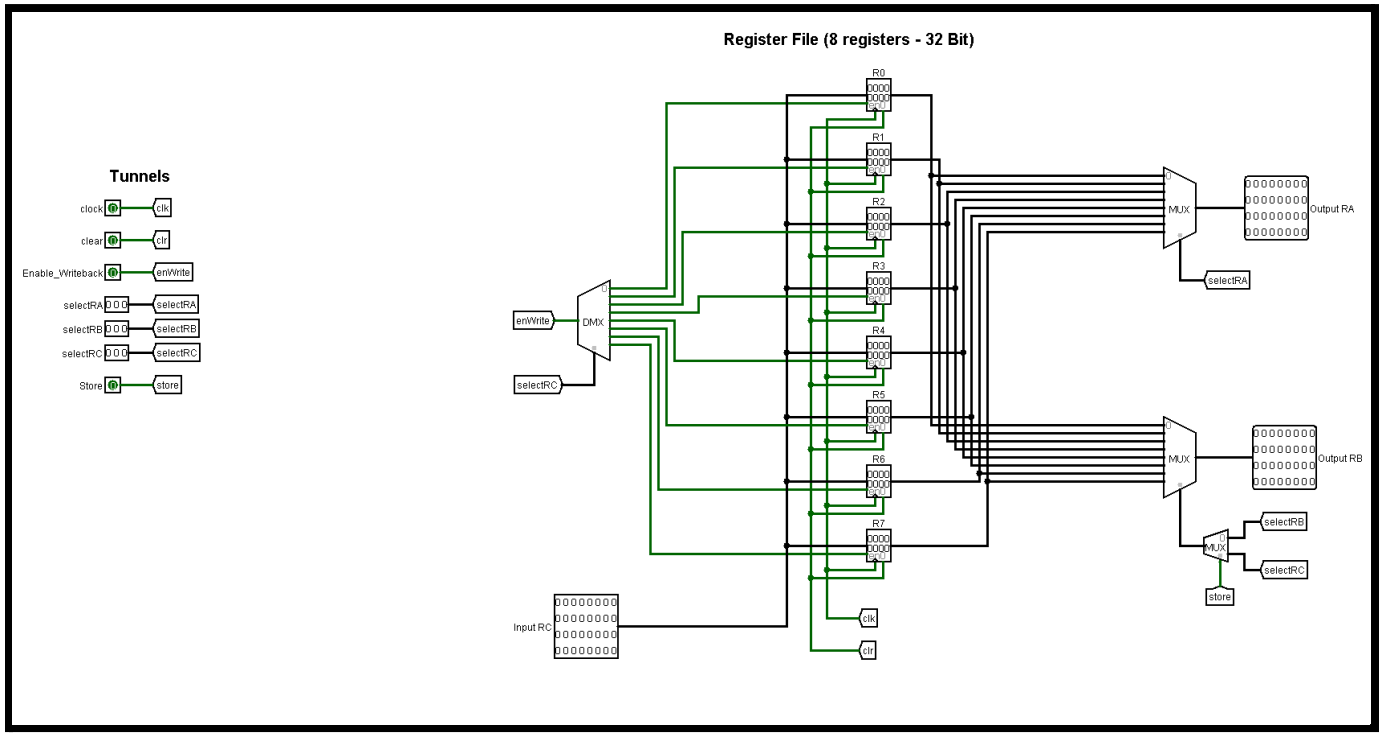
2. Five Stage Pipeline



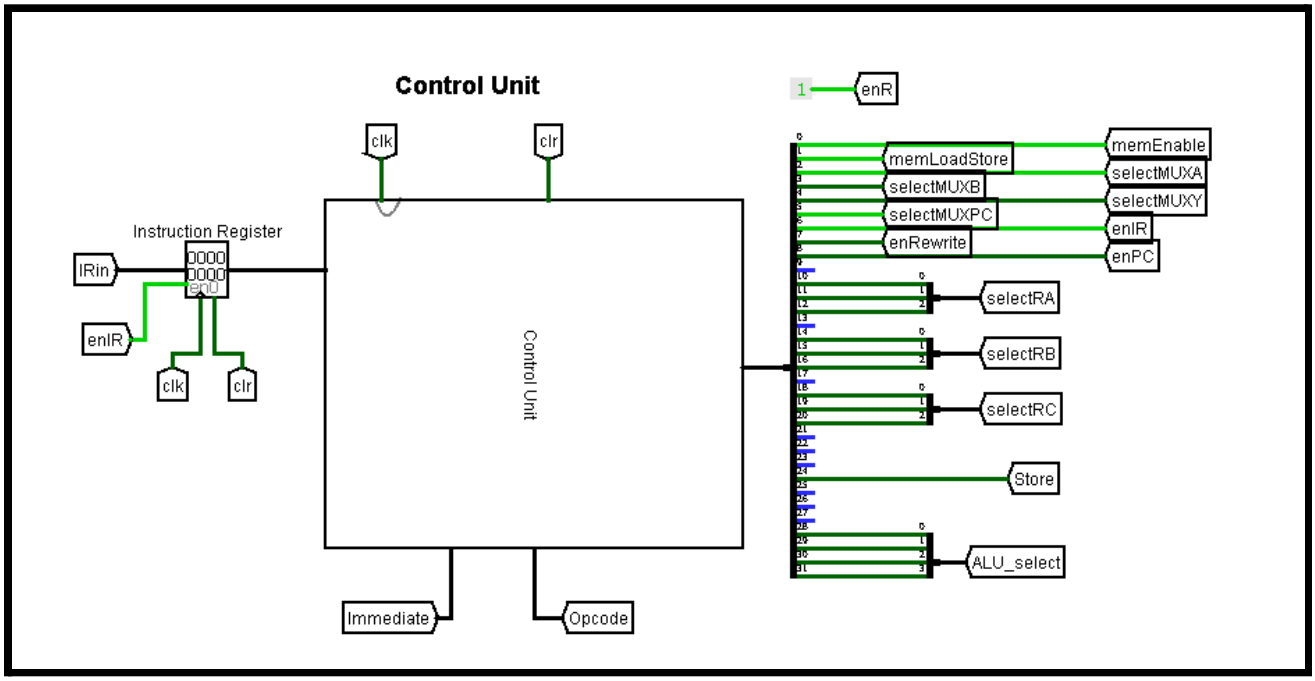
3. Arithmetic Logical Unit



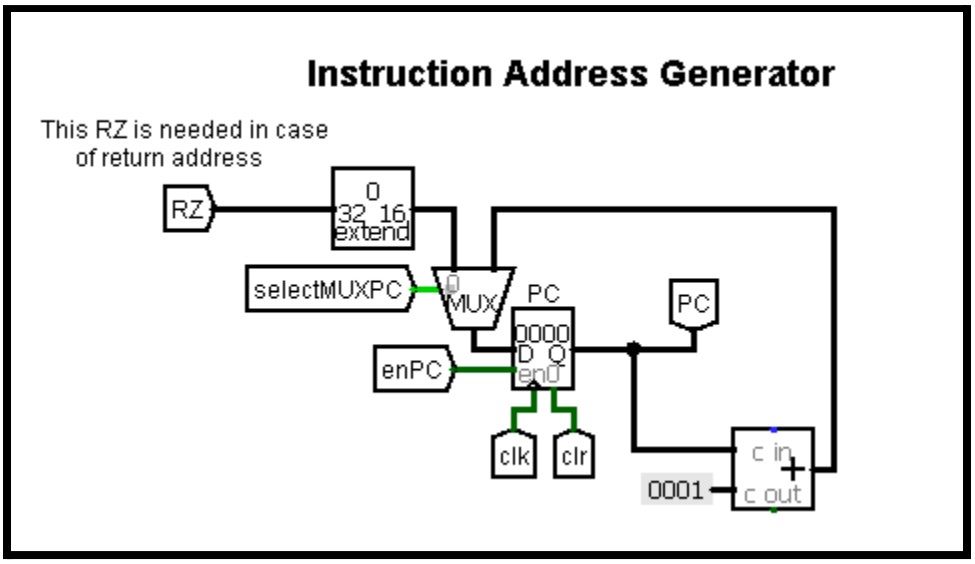
4. Register File Block



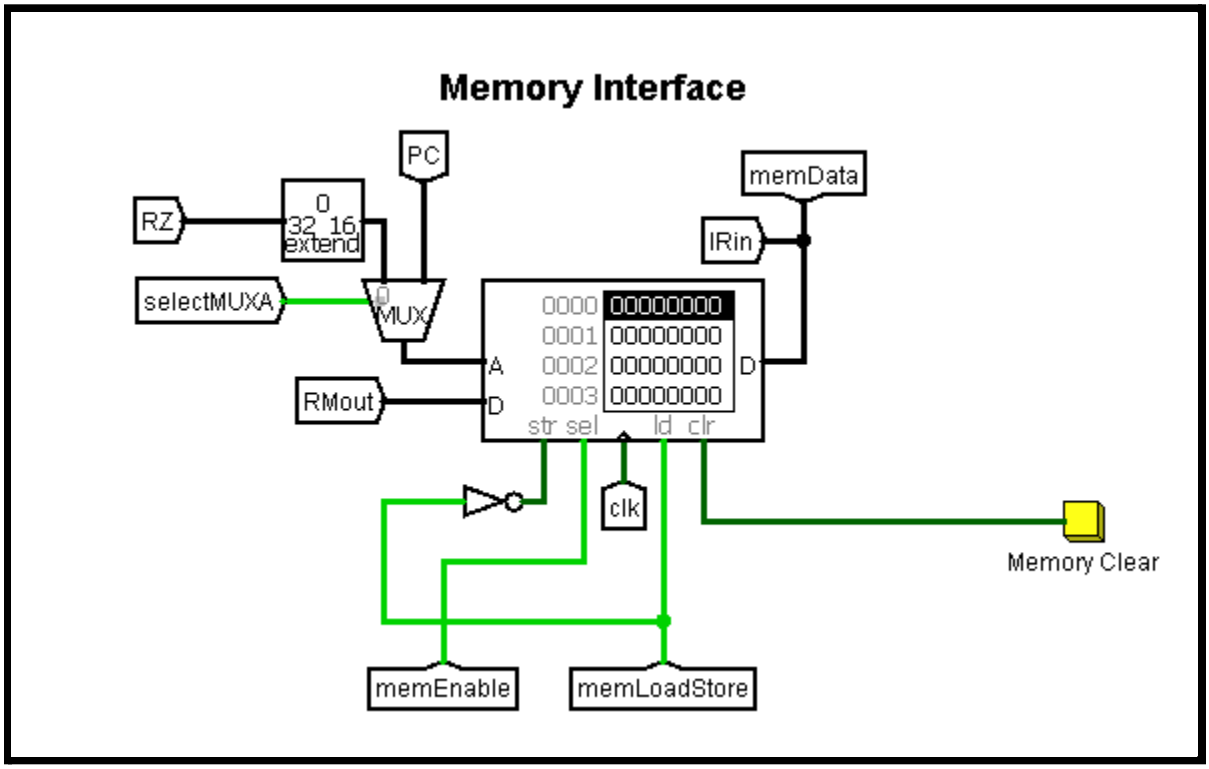
5. Control Unit



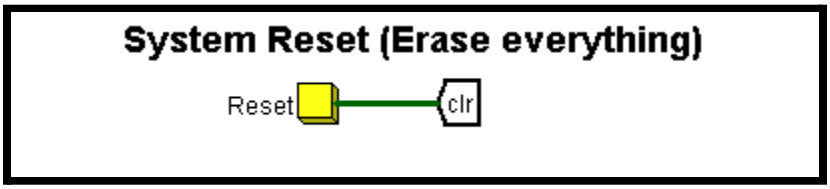
6. Instruction Address Generator



7. **Processor Memory Interface**



8. **Reset Block**



9. Five Stage Architecture Explanation

a. Fetch: The instruction pointed by Program Counter is fetched from Random Access Memory and transmitted to the Instruction Register (IR).
b. Decode: Instruction Register transfers the value of instruction for decode inside the control unit, which further generates the control signals needed for handling the operation. In my circuit, I am making use of 14 control signals, each one required to handle different blocks and components mentioned above.
    i. Register File is controlled by the following signals: select_RA, select_RB, select_RC, enRewrite, and store.
    ii. The arithmetic and Logical Unit is controlled by ALU_select.
    iii. Processor Memory Interface is controlled by - select_MUXA, and memEnable, memLoadStore
    iv. Instruction Address Generator is controlled by - select_MUXPC and enPC
    v. Other Signals: select_MUXB, select_MUXY and Immediate
c. Execute: According to the control signals generated by the control unit, the instructions are executed by the ALU (OR, AND, ADD and SUB).
d. Memory: If Load/Store is to be performed, then the result produced by ALU interacts with memory for the operation, else it is transferred to Register RY.
e. Writeback: If write mode is enabled in Register File, then the values present in register RY, are written to the RF. This is needed in the case of ADD, ADI, SUB, SUI, AND, ANI, OR, ORI, MOV, MVI and LOAD.