Name: _____ PS ID: _____

Part 3: Assignment 2
Cache

BB Due Date: Wednesday, April 22nd Midnight
Hard Copy Submission: Next Lab after BB due date

1. Imagine an empty direct mapped cache with 2 byte blocks and total size of 8 bytes. For the address references listed below, do the following:
    a. Fill in the requested information in the table.
    b. Show the final content of the cache.
    c. Calculate the miss rate.

    Note:The first one has been done for you. To show the content of the cache use M(address). For example M(18) means data in memory address 18. We are using a byte addressable machine and memory address is 8 bits. The cache size in this homework is assigned only to data portion (blocks) so do not include validity bit and tag in the calculation.

Address reference	Binary address	Hit/Miss	Assigned cache block (index)
0	0000 0000	Miss	00
1			
2			
3			
7			
8			
9			
2			
18			
10			
11			

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20			
21			
11			

Miss rate:

Final Content of Cache:

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Now Imagine a cache with four blocks where each block has one byte. After the same address references what is the final content of the new cache and what is the miss rate?

Address reference	Binary address	Hit/Miss	Assigned cache block (index)
0	0000 0000	Miss	00
1			
2			
3			
7			
8			
9			
2			
18			
10			
11			
20			
21			
11			

Miss rate:

Name: _____ PS ID: _____

Final Content of Cache:

2. Imagine a 2-way set associative cache of data size of 16 bytes and each memory block has one byte. Show the hits and misses for these series of references and the final content of cache. Assuming LRU replacement. Show the final content of the cache.

Address reference	Binary address	Hit/Miss	Assigned cache set
16			
11			
30			
4			
9			
19			
24			
12			
6			
4			
16			
8			
12			
19			
27			
14			
6			

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Miss Rate:

Final Cache:

Name: _____ PS ID: _____

3. Consider a fully associative cache with 4 byte blocks and total size of 16 bytes. Find the hits and misses and final content of the cache for these address references. Use LRU replacement.

Address reference	Binary address	Hit/miss	Cache Line Used (Optional) for reference when showing final cache
3			
14			
17			
12			
26			
9			
21			
24			
5			
11			

Miss Rate:

Final Cache: