1. Realize a 4-bit carry lookahead adder comprising the following two submodules:

(i) the sum module having A[i.3 : i.0], B[i.3 : i.0], C[i.3 : i.0] as inputs and
S[i.3 : i.0] as outputs;
the input C[i.0] is the carry-in from the previous nibble fed as an external input when i = 0 and from the inter-nibble CL unit for i > 0;
thus, the inputs C[i.3:i.1] are from the intra-nibble CL unit described below,

(ii) the intra-nibble CL module having A[i.3:i.0], B[i.3:i.0, C[i.0] as inputs and as outputs
(a) C[i.3:i.1] for consumption in the sum-module as indicated above,
(b) P[i] -- inter-nibble carry-propagate for consumption by the inter-nibble CL unit (to be realized in experiment 2A given below,
(c) G[i] -- inter-nibble carry-generate for consumption by the inter-nibble CL unit.

2A. Realize a 16-bit adder with an inter-nibble carry lookahead comprising the following submodules:

(i) 4 modules of carry lookahead adder, realized in experiment 1, and

(ii) an inter-nibble CL unit for the four nibbles with inputs
(a) carry-in c0 from previous 4 nibble block (for cascading),
(b) inter-nibble carry propagate inputs p[3:0] to be driven by the outputs P[i], 0 <= i <= 3, from the 4 modules of (i) and
(c) inter-nibble carry generate inputs g[3:0] to be driven by G[i], 0 <= i <= 3, from the 4 modules of (i).

and outputs:
(a) inter-nibble carry outputs C[i+1], 0 <= i <= 3, of which the first three (for 0 <= i <= 2) are fed as C[i+1.0] inputs to the higher significant three modules of 2A(i); the input C[0.0] to the module for the 0th nibble is carry-in input. The final carry out from the 16 bit adder is provided by C[4] output of the inter-nibble CL unit.

2B. Realize a 32-bit adder using two 16-bit adder modules of experiment 4.

Reference: Patterson and Hennessy, Computer Organization and Design.

Do the following for each of the above experiments:

(i) A Verilog behavioral description;
(ii) A test bench generator module and test the circuit;
(iii) A Verilog structural description;
(iv) Test it using the same module as in (ii);
(v) Synthesize the behavioural code of (i) using the FPGA kit;
(vi) Measure some performance metircs like area, delay, number of LUTs;
(vii) Synthesize the structural description of (iii) using the FPGA kit;
(viii) Measure the performance using the same metrics as in (vi) and compare the performance of the two synthesized units.