The specific operation performed by the desired subunit is determined by a "select" control line S as shown. The ALU's logical operations are performed bitwise; that is, the same operation f is applied to every pair of data lines x_i and y_i. The maximum number of distinct logical operations of the form $f(x_i,y_i)$ is 16, because there are only 16 distinct truth tables of two Boolean variables. Hence the select input needs to be of size 4 at most, as in Figure 4.28. S can also be used to select 16 different arithmetic operations such as $X + Y$, $X - Y$, $Y - X$, $X + 1$ (increment), $X - 1$ (decrement), and so on, as needed.

The four logical operations in Figure 4.28 can be obtained by generating all four minterms of $f(x_i,y_i)$, namely,

$$m_3 = x_i y_i \quad m_2 = x_i \bar{y}_i \quad m_1 = \bar{x}_i y_i \quad m_0 = \bar{y}_i \bar{y}_i$$

for the pair $x_i y_i$ of data bits and by using the control lines $S = S_3S_2S_1S_0$ to select the subsets of the minterms to be ORed together. In particular, if we construct the sum-of-products expression

$$\begin{aligned} f(x_i,y_i) &= m_3S_3 + m_2S_2 + m_1S_1 + m_0S_0 \\ &= x_i y_i S_3 + x_i \bar{y}_i S_2 + \bar{x}_i y_i S_1 + \bar{x}_i \bar{y}_i S_0 \end{aligned} \tag{4.32}$$

we see that every combination of $S_3S_2S_1S_0$ produces a different function. For example, $S = 0110$ makes $f(x_i,y_i) = x_i\bar{y}_i + \bar{x}_i y_i$, which is EXCLUSIVE-OR. Because of the bitwise nature of the logic operations, we can replace x_i and y_i in (4.32) with the words X and Y.

$$f(X,Y) = XYS_3 + X\bar{Y}S_2 + \bar{X}YS_1 + \bar{X}\bar{Y}S_0 \tag{4.33}$$

We now implement the logic unit directly from Equation (4.33), using several three-input gates as in Figure 4.29. The adder-subtracter can be designed by any of the techniques presented earlier, with appropriate additional connections to X, Y, and S.

Despite its conceptual simplicity, the ALU of Figure 4.28 is more expensive and slower than necessary. For $n = 4$, the logic subunit employs about 25 gates and 4 levels. If the arithmetic subunit is designed with carry lookahead in the style of Figure 4.6, around 60 gates are needed, depending on the variants of add and subtract that are implemented. The multiplexer in Figure 4.28 also requires additional

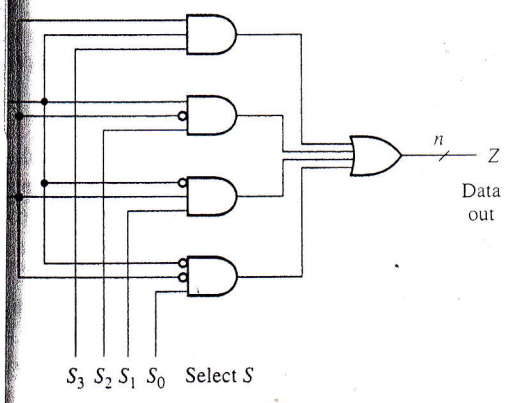

Figure 4.29
An n-bit logic unit that realizes all 16 two-variable functions.