

How you make the UCF file & download program on the kit?

1. From Sources for : select **Implementation / Behavioral Simulation**

Select **XXXX.v** file from “+ xc3s400-4pq208” clicking on ‘+’ symbol → Right Click in Mouse on the **XXXX.v** → **New Source**

The screenshot shows the Xilinx ISE 10.1 Design Summary window for a project named FA1. The window is divided into several sections:

- FA1 Project Status:** A table showing project details and current status.
- FA1 Partition Summary:** A section indicating that no partition information was found.
- Device Utilization Summary:** A table showing logic utilization and distribution.
- Performance Summary:** A table showing final timing score, routing results, and timing constraints.
- Detailed Reports:** A section for generating detailed reports.

The **FA1 Project Status** table is as follows:

| Project File: | FA1.isc | Current State: | Programming File Not Generated |
|------------------|---------------------------------|---------------------|---|
| Module Name: | FA1 | Errors: | No Errors |
| Target Device: | xc3s400-4pq208 | Warnings: | No Warnings |
| Product Version: | ISE 10.1 - Foundation Simulator | Routing Results: | All Signals Completely Routed |
| Design Goal: | Balanced | Timing Constraints: | 0 Timing Report |
| Design Strategy: | Xilinx Default (unlocked) | Final Timing Score: | 0 Timing Report |

The **Device Utilization Summary** table is as follows:

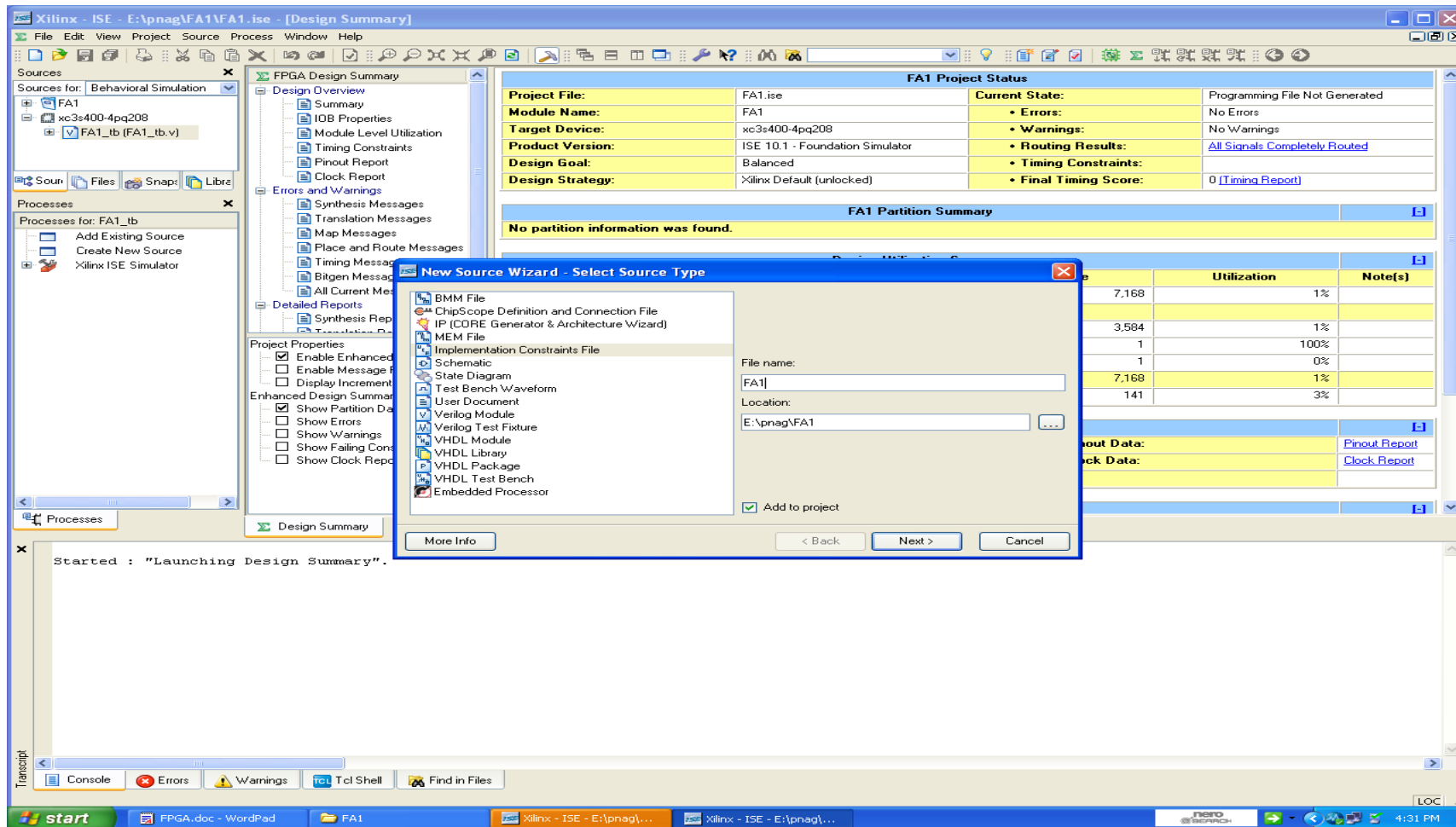
| Logic Utilization | Used | Available | Utilization | Note(s) |
|--|----------|--------------|-------------|---------|
| Number of 4 input LUTs | 2 | 7,168 | 1% | |
| Logic Distribution | | | | |
| Number of occupied Slices | 1 | 3,584 | 1% | |
| Number of Slices containing only related logic | 1 | 1 | 100% | |
| Number of Slices containing unrelated logic | 0 | 1 | 0% | |
| Total Number of 4 input LUTs | 2 | 7,168 | 1% | |
| Number of bonded I/Os | 5 | 141 | 3% | |

The **Performance Summary** table is as follows:

| Final Timing Score: | 0 | Pinout Data: | Pinout Report |
|---------------------|---|--------------|-------------------------------|
| Routing Results: | All Signals Completely Routed | Clock Data: | Clock Report |
| Timing Constraints: | | | |

The **Detailed Reports** section is currently empty.

Select **Implementation Constraints File (ucf)** from New Source Wizard → Give File Name as in New Project **XXXX** → **Next**



→ Finish.

The screenshot shows the Xilinx ISE Design Summary window for project FA1. The Design Summary is partially visible, showing project details and a table of utilization. A 'New Source Wizard - Summary' dialog box is open in the foreground, displaying configuration options for a new source file.

FA1 Project Status

| | | | |
|-------------------------|---------------------------------|----------------------------|---|
| Project File: | FA1.isc | Current State: | Programming File Not Generated |
| Module Name: | FA1 | Errors: | No Errors |
| Target Device: | xc3s400-4pq208 | Warnings: | No Warnings |
| Product Version: | ISE 10.1 - Foundation Simulator | Routing Results: | All Signals Completely Routed |
| Design Goal: | Balanced | Timing Constraints: | |
| Design Strategy: | Xilinx Default (unlocked) | Final Timing Score: | 0 (Timing Report) |

FA1 Partition Summary

No partition information was found.

New Source Wizard - Summary

Project Navigator will create a new skeleton source with the following specifications:

- Add to Project: Yes
- Source Directory: E:\pnag\FA1
- Source Type: Implementation Constraints File
- Source Name: FA1.ucf
- Association: FA1

Utilization Table

| | Utilization | Note(s) |
|-------|-------------|---------|
| 7,168 | 1% | |
| 3,584 | 1% | |
| 1 | 100% | |
| 1 | 0% | |
| 7,168 | 1% | |
| 141 | 3% | |

Report Data: [Pinout Report](#)

Check Data: [Clock Report](#)

Started : "Launching Design Summary".

2. From Sources for: select **Implementation**

Now click on '+' symbol of "+XXXX.v" file → select "- XXXX.ucf" → go & click on "+" symbol of "+ **User Constraints**" under

Processes: → double click on **Edit Constraints (Text)**

The screenshot shows the Xilinx ISE Design Suite 10.1 Design Summary window. The window is titled "Xilinx - ISE - E:\pnag\FA1\FA1.ise - [Design Summary]". The left pane shows the "Sources for: Implementation" and "Processes for: FA1.ucf" sections. The "Sources for: Implementation" section shows the project files: FA1, xc3s400-4pq208, FA1 (FA1.v), and FA1.ucf (FA1.ucf). The "Processes for: FA1.ucf" section shows the process steps: Add Existing Source, Create New Source, User Constraints, and Edit Constraints (Text). The "Edit Constraints (Text)" process is selected and highlighted. The main pane displays the "FA1 Project Status" summary, which includes the Project File (FA1.ise), Module Name (FA1), Target Device (xc3s400-4pq208), Product Version (ISE 10.1 - Foundation Simulator), Design Goal (Balanced), and Design Strategy (Xilinx Default (unlocked)). The "FA1 Partition Summary" section indicates that no partition information was found. The "Device Utilization Summary" table shows the logic utilization, including the number of 4 input LUTs, occupied slices, and the total number of 4 input LUTs. The "Performance Summary" section shows the final timing score (0) and routing results (All Signals Completely Routed). The "Detailed Reports" section is also visible at the bottom.

| FA1 Project Status | | | | |
|--------------------|---------------------------------|---------------------|---|--|
| Project File: | FA1.ise | Current State: | Programming File Generated | |
| Module Name: | FA1 | Errors: | No Errors | |
| Target Device: | xc3s400-4pq208 | Warnings: | No Warnings | |
| Product Version: | ISE 10.1 - Foundation Simulator | Routing Results: | All Signals Completely Routed | |
| Design Goal: | Balanced | Timing Constraints: | | |
| Design Strategy: | Xilinx Default (unlocked) | Final Timing Score: | 0 (Timing Report) | |

| FA1 Partition Summary | | | | |
|-------------------------------------|--|--|--|--|
| No partition information was found. | | | | |

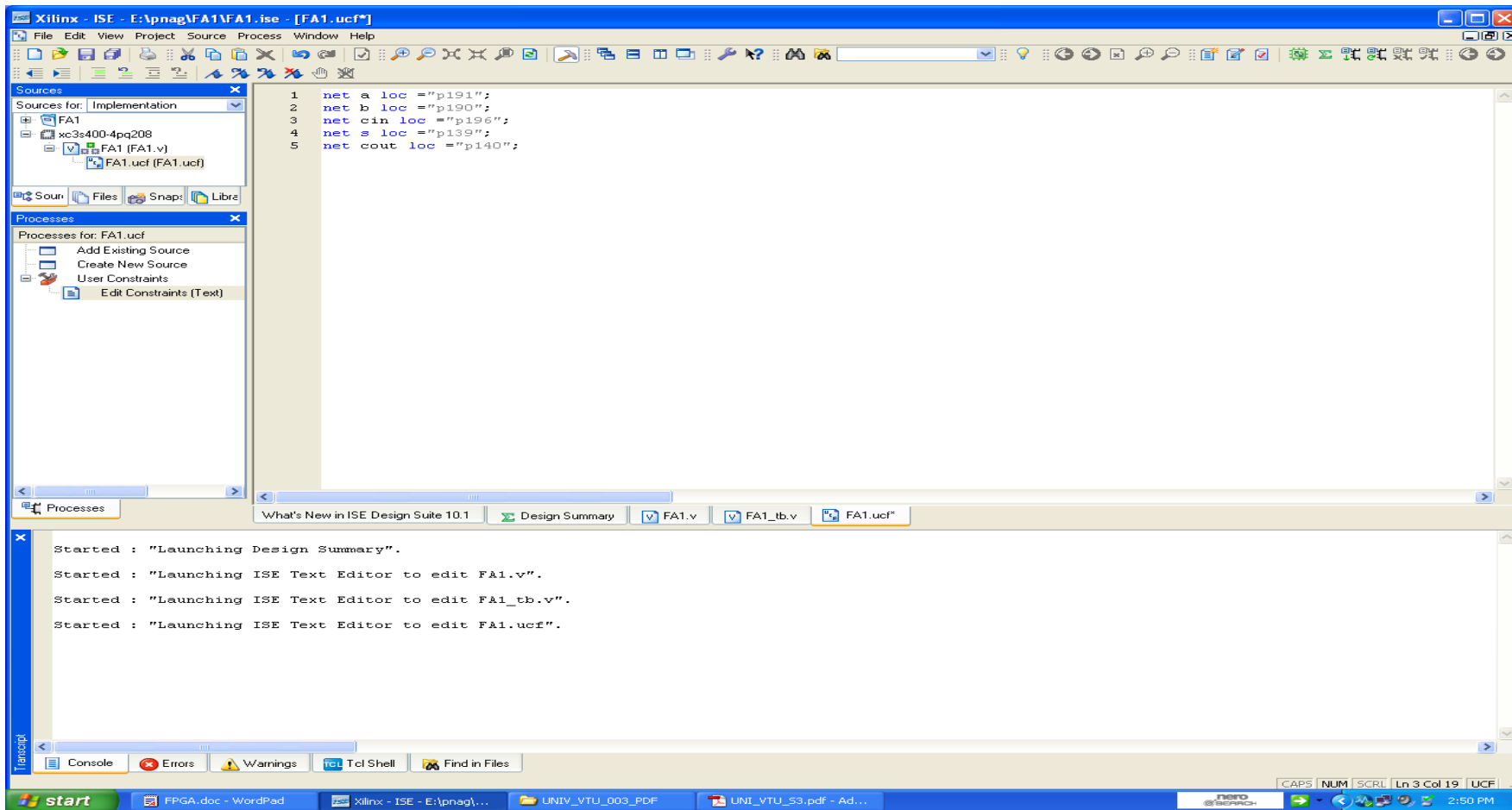
| Device Utilization Summary | | | | |
|--|----------|--------------|-------------|---------|
| Logic Utilization | Used | Available | Utilization | Note(s) |
| Number of 4 input LUTs | 2 | 7,168 | 1% | |
| Logic Distribution | | | | |
| Number of occupied Slices | 1 | 3,584 | 1% | |
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| Total Number of 4 input LUTs | 2 | 7,168 | 1% | |
| Number of bonded I/Os | 5 | 141 | 3% | |

| Performance Summary | | | |
|---------------------|---|--------------|-------------------------------|
| Final Timing Score: | 0 | Pinout Data: | Pinout Report |
| Routing Results: | All Signals Completely Routed | Clock Data: | Clock Report |
| Timing Constraints: | | | |

| Detailed Reports | |
|------------------|--|
| | |

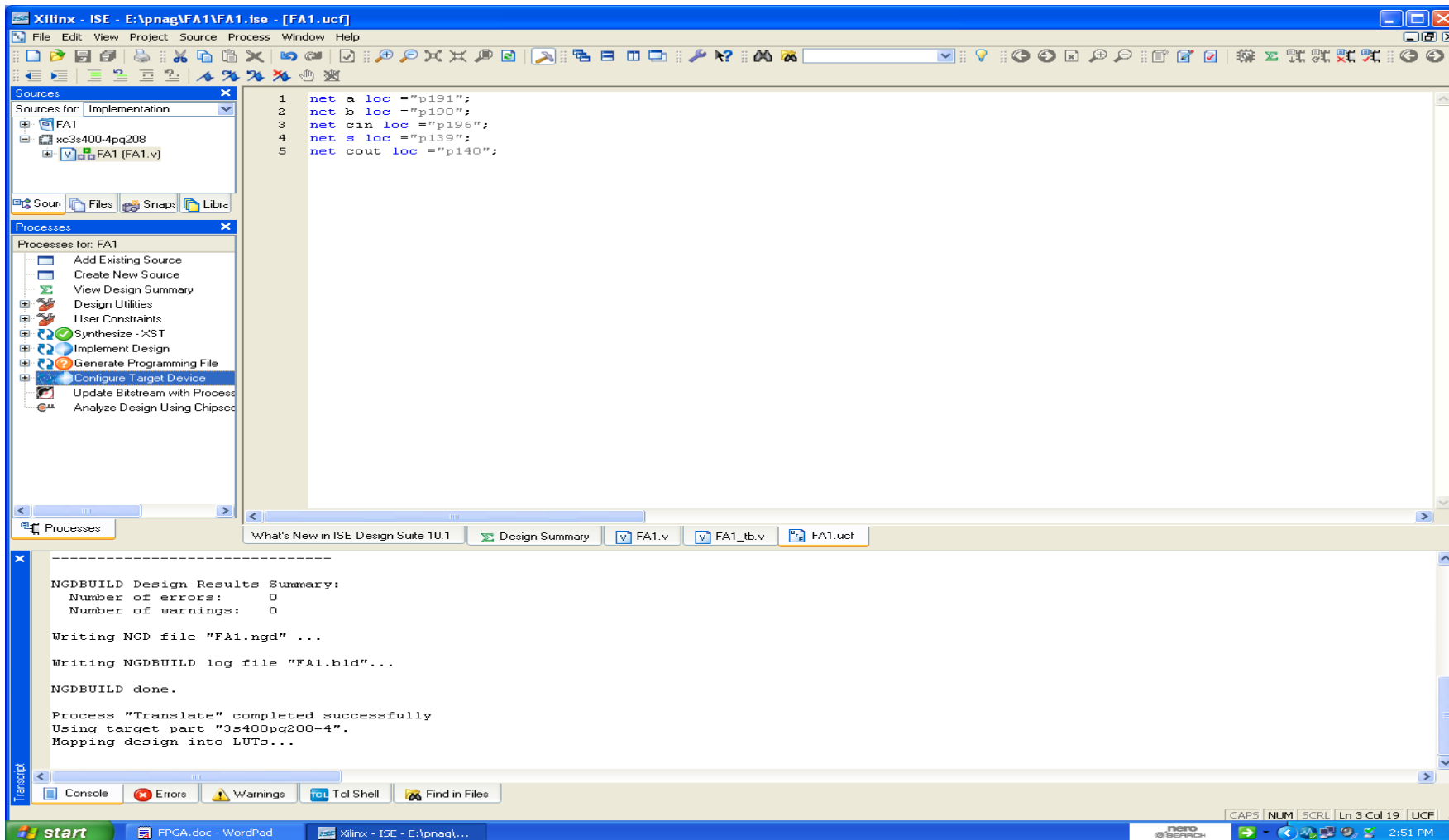
Started : "Launching Design Summary".

Now write the **I/P Pin** & **O/P LED** configuration as given below → **Save**

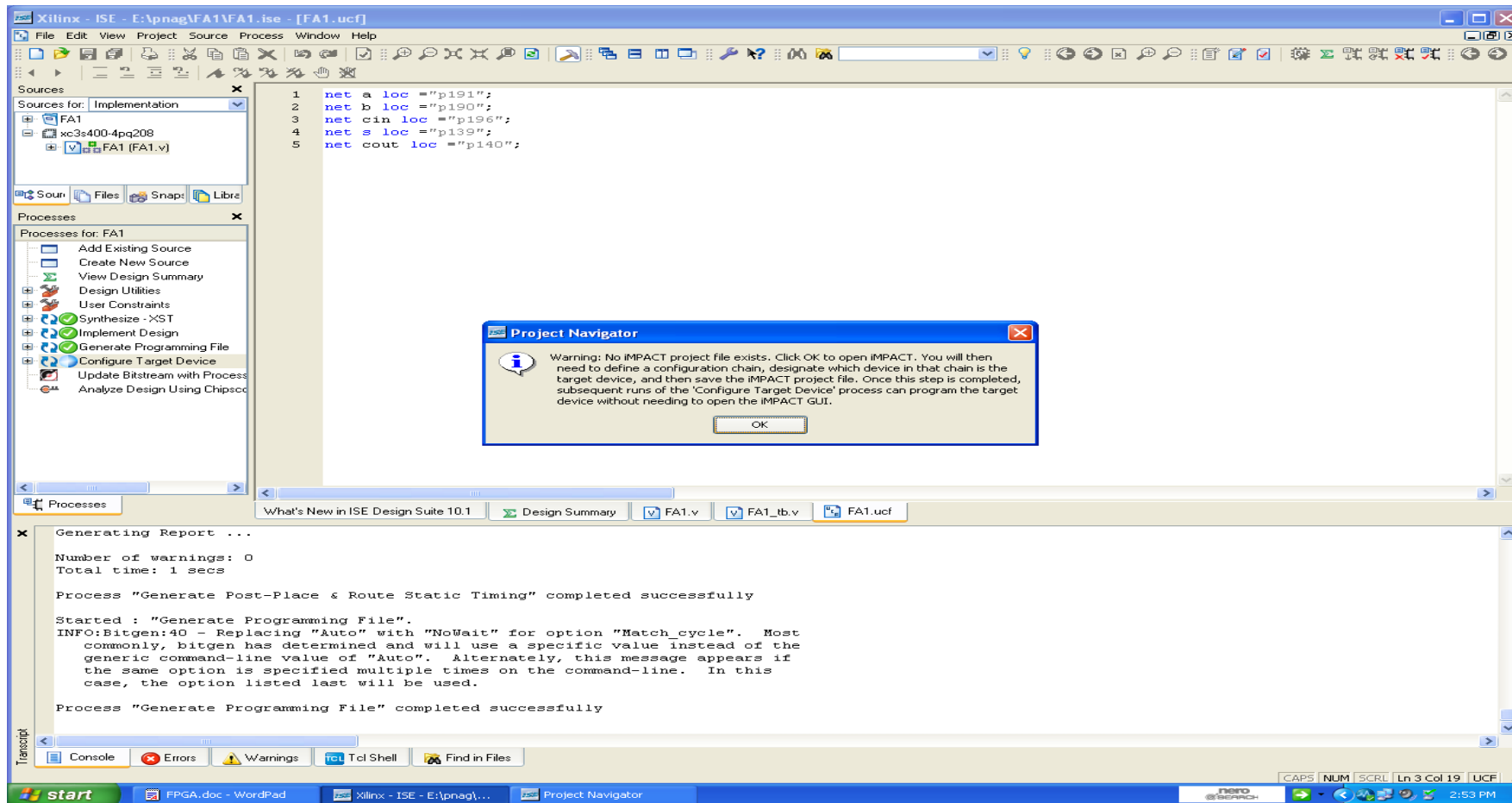


3. From Sources for: select **Implementation** → then select **XXXX.v** file

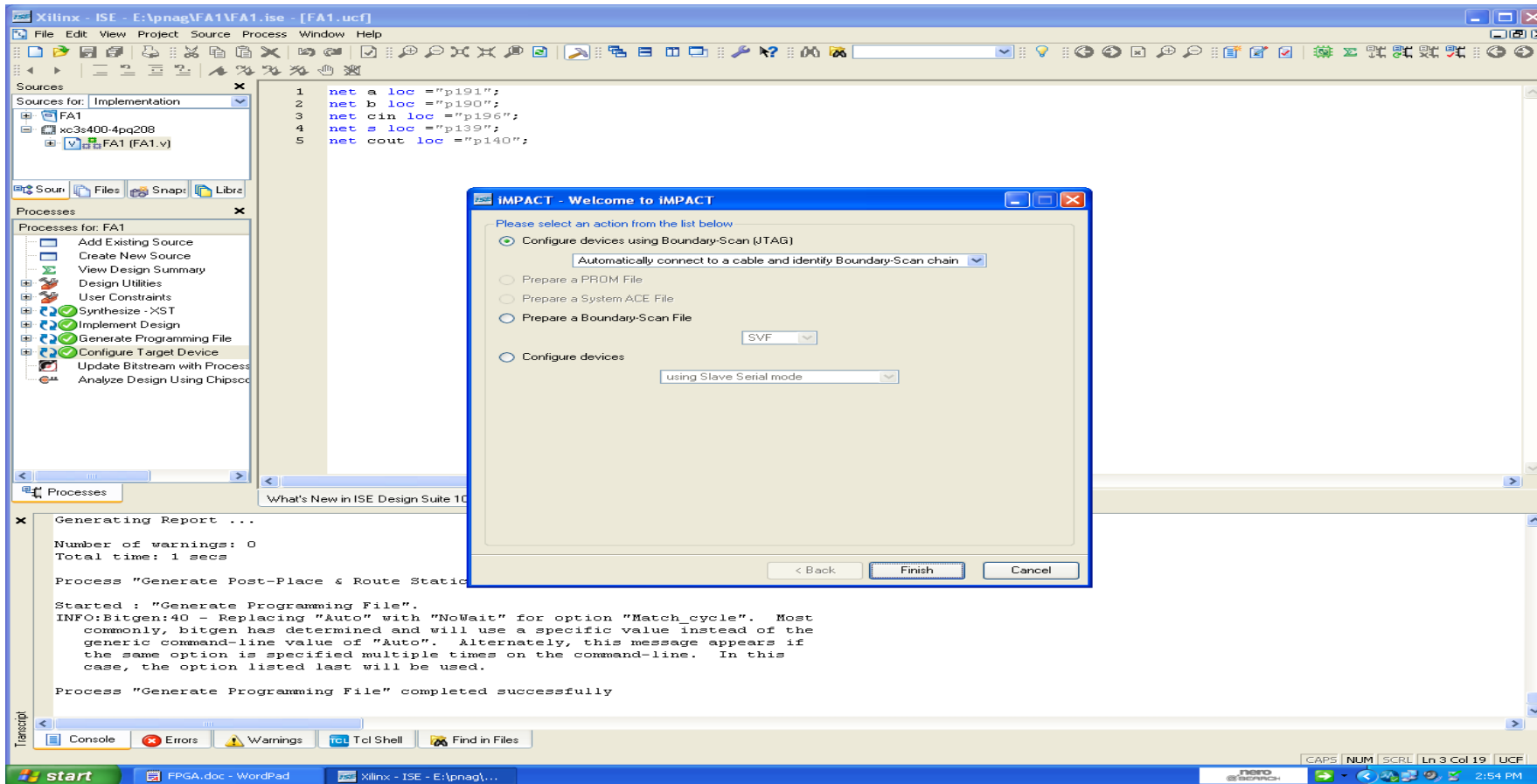
From Processes: select & double click on **+ Configure Target Device** or click on **+** symbol of **+Configure Target Device** and double click on **Manage Configuration Project (iMPACT)**



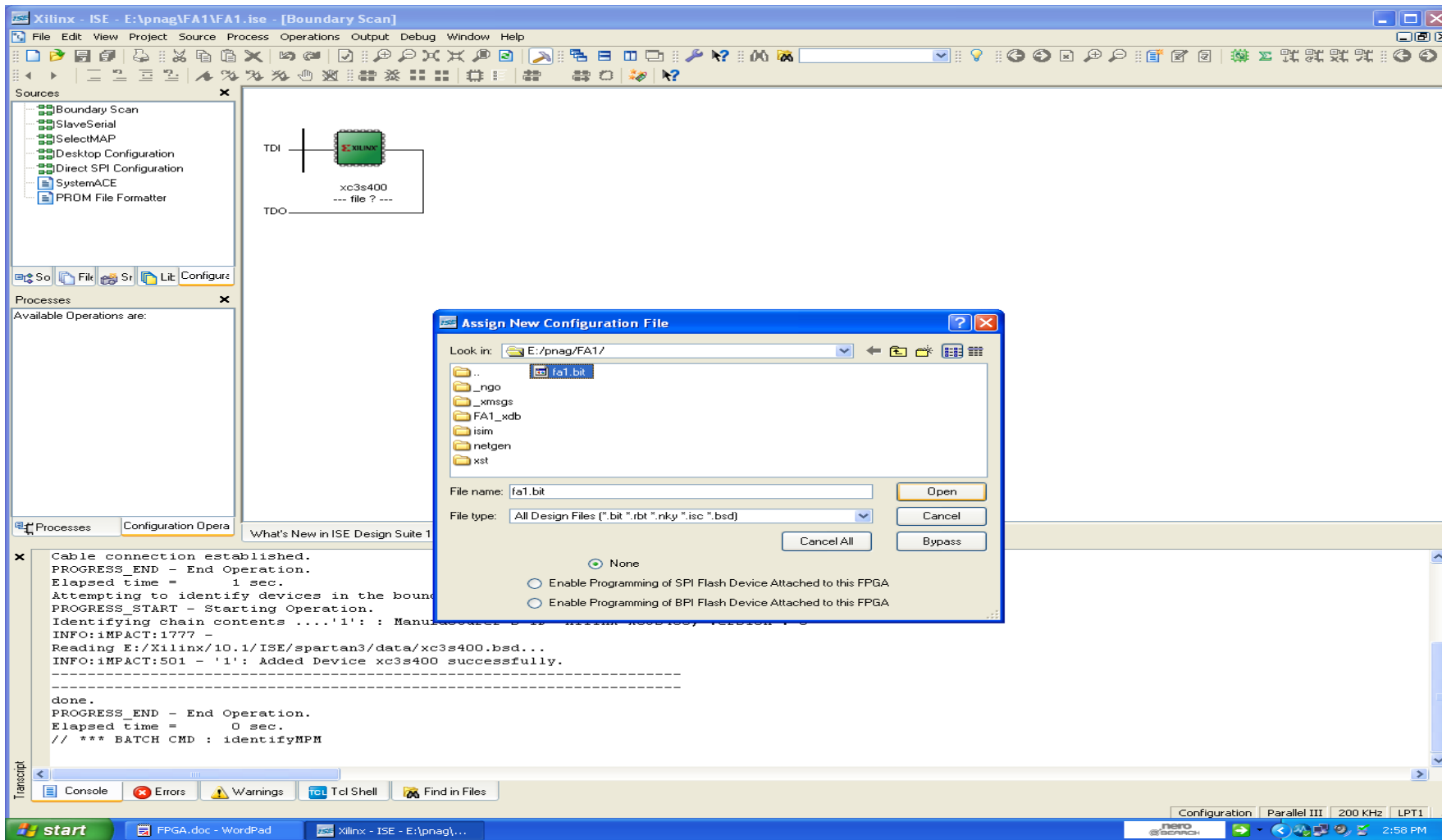
After appearing Project Navigator → click **OK**



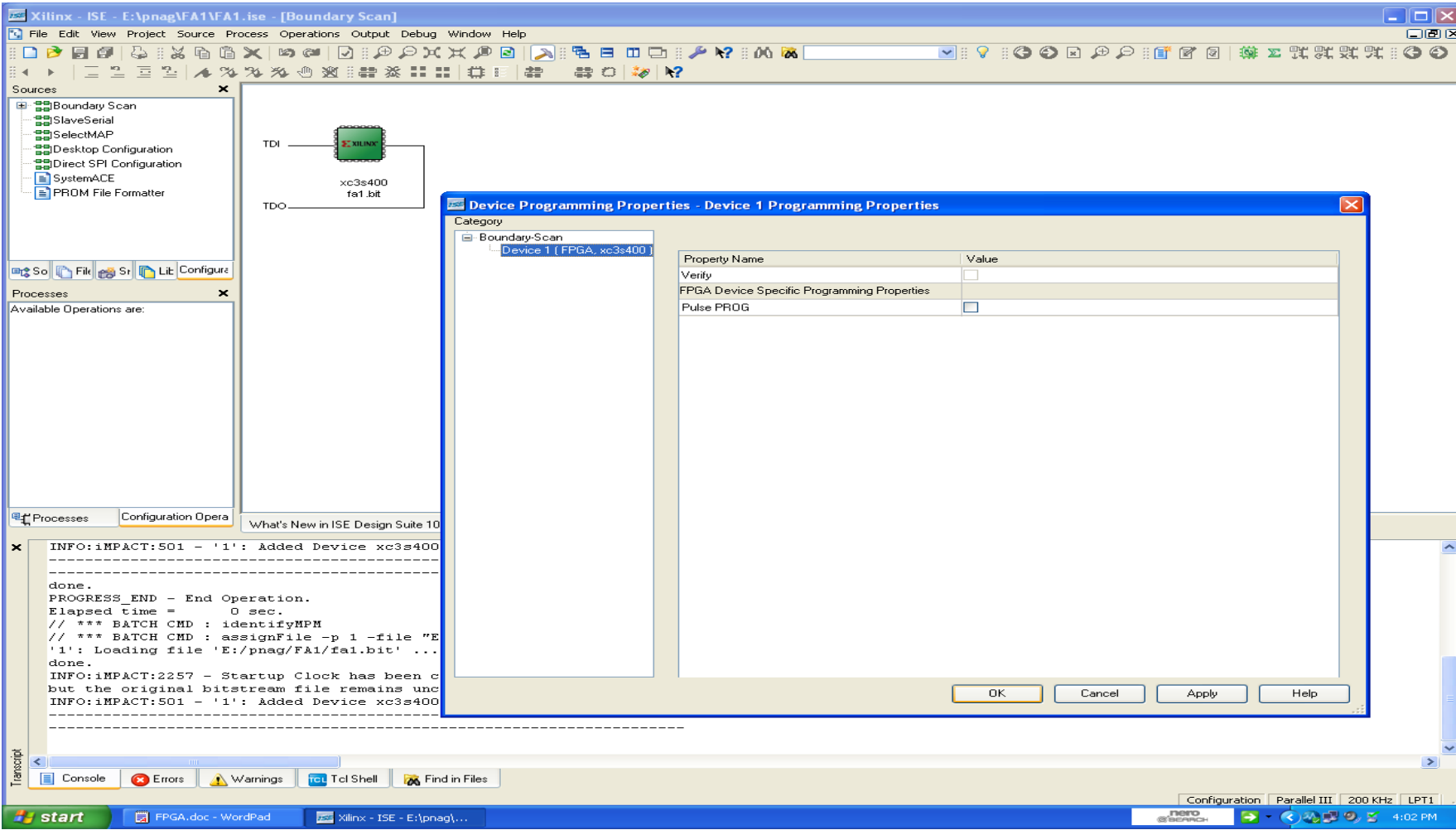
Then click on **Finish**



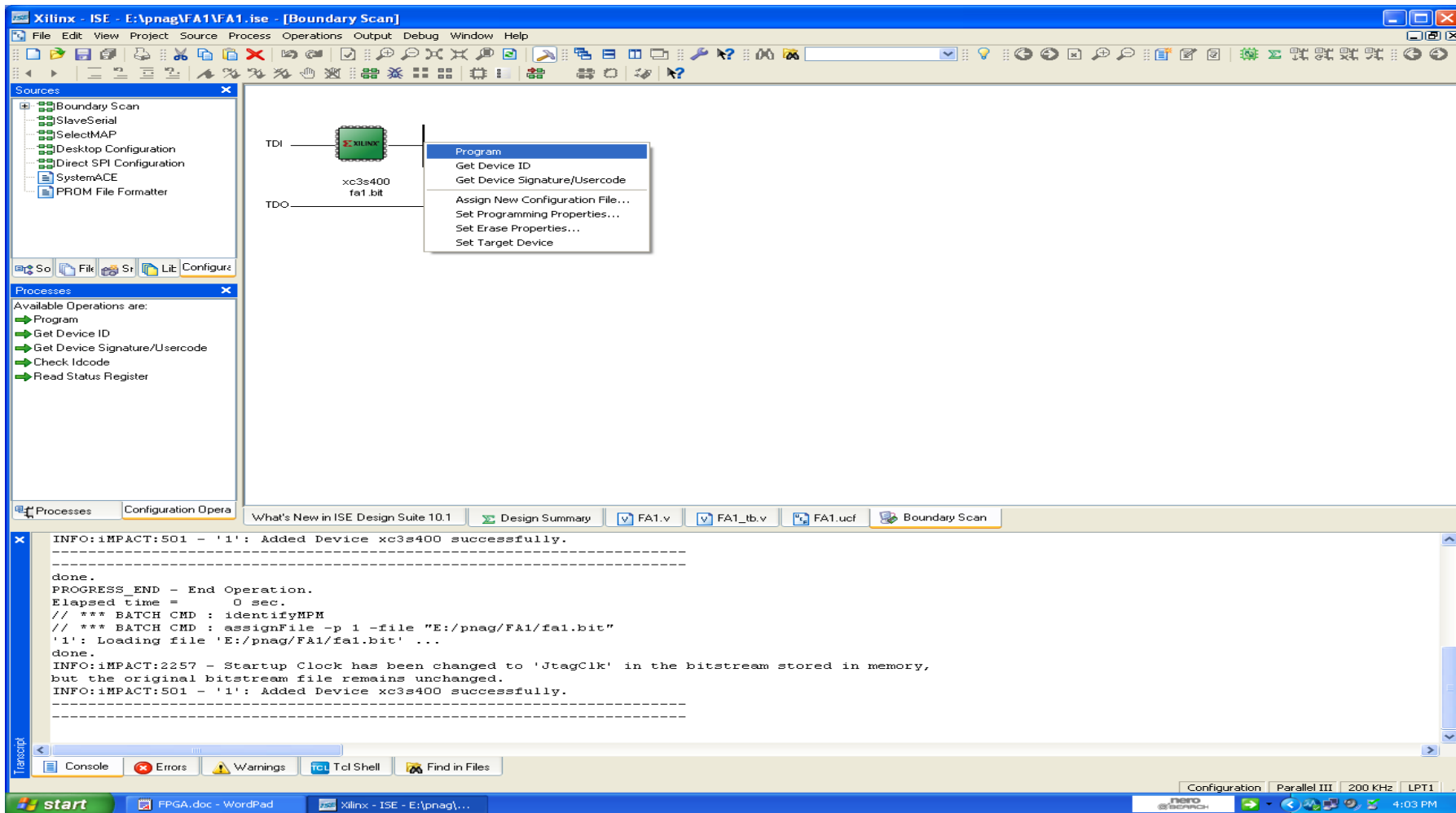
Select **XXXX.bit** file from **Assign New Configuration File** → click on **Open**



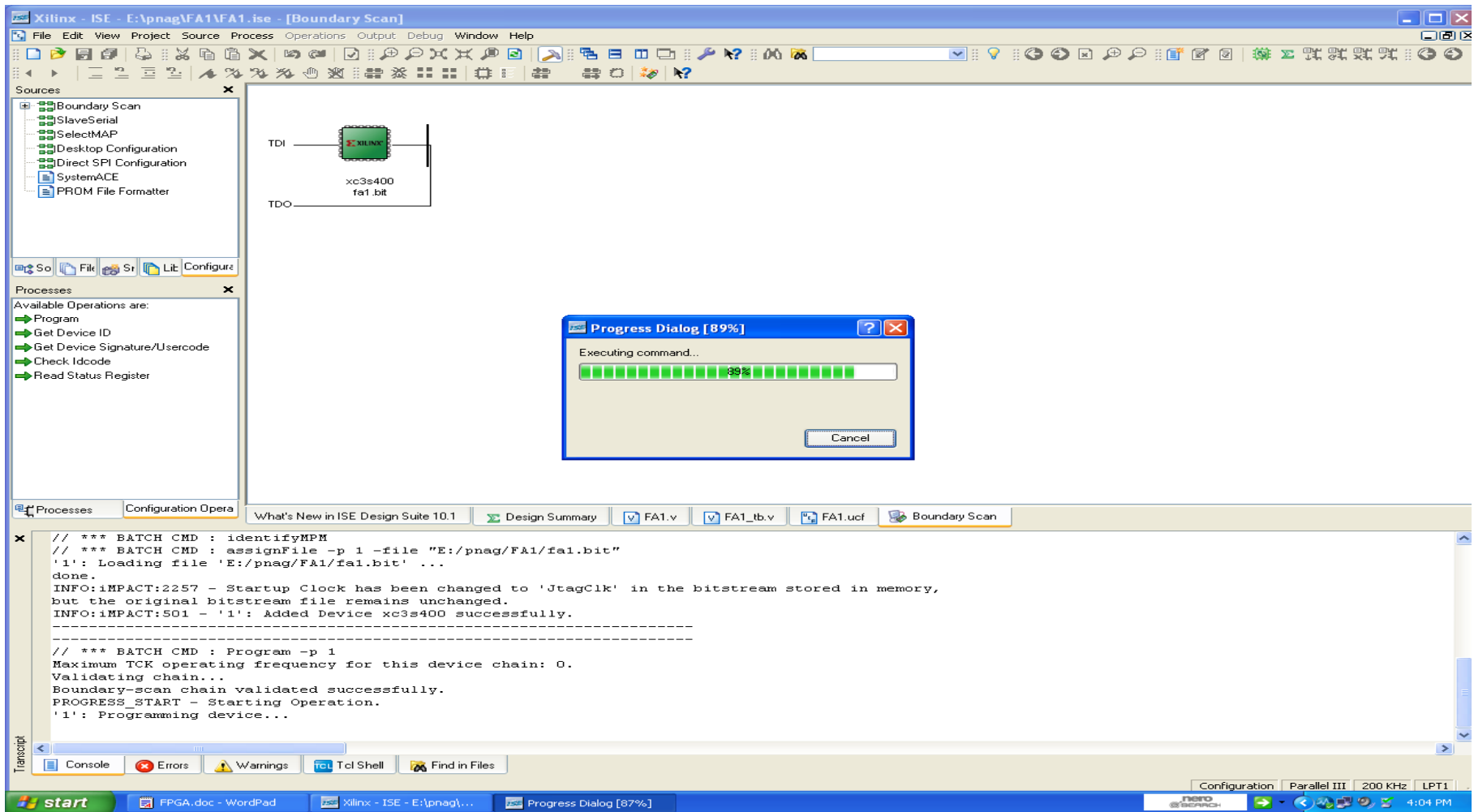
Click **OK** on **Device Programming Properties**



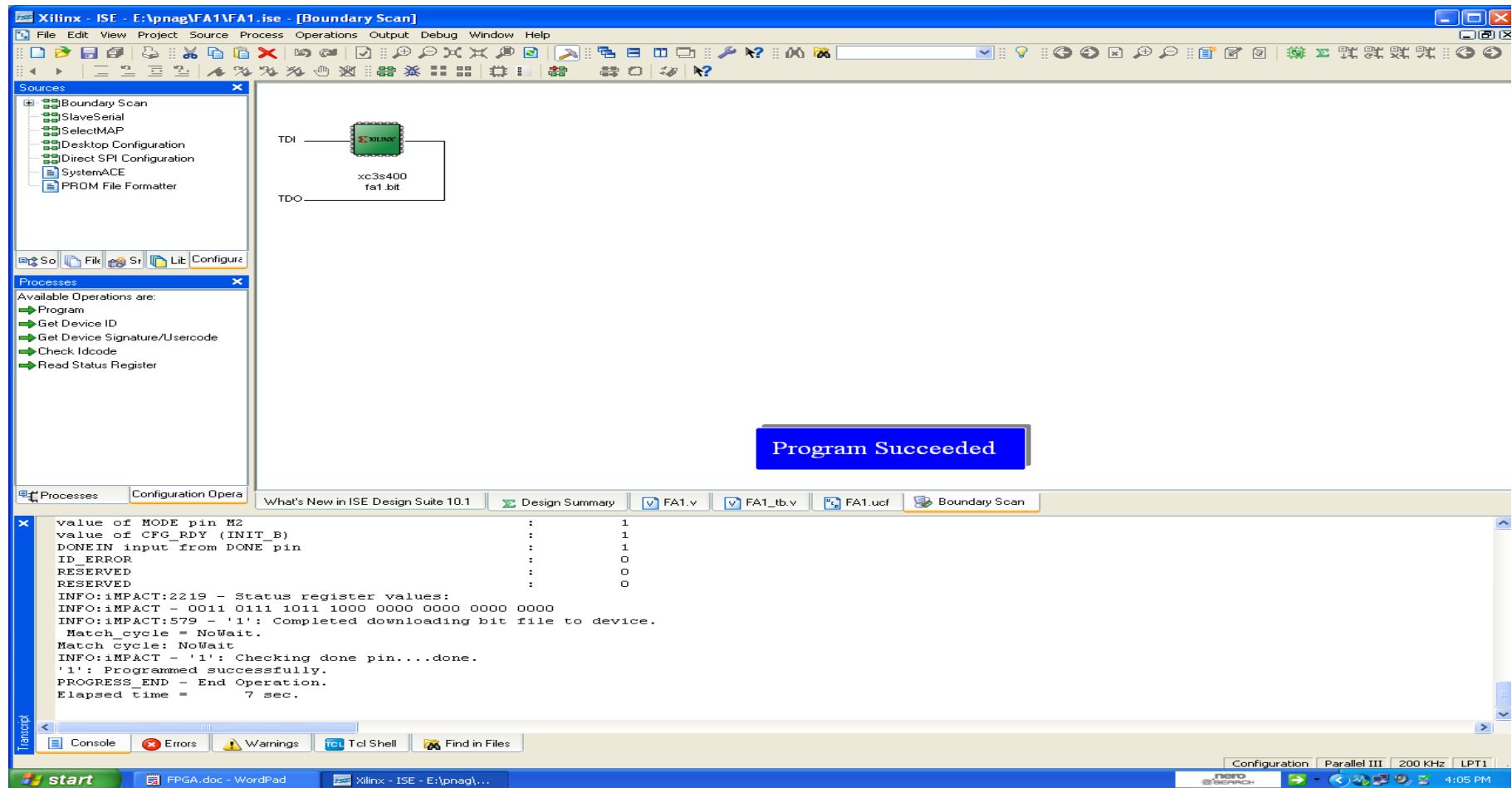
Select **Xilinx** symbol → **Right Click** just on **Xilinx** → click on **Program**



Progress Dialog [89%] starts loading



Now **Programme Succeeded**



Then go to **XILINX Trainer Kit** & the predetermined **Switches** corresponding to **I/P** combinations are adjusted manually and predetermined **LED** glows depending upon the **I/P** combinations. Then **O/P** s are verified with the corresponding **I/P** s combinations according to the truth table of the design.