Starting the ISE Software

To start ISE, double-click the desktop icon,

or start ISE from the Start menu by selecting:

Start All Programs Xilinx ISE 10.1 Project Navigator

Note: Your start-up path is set during the installation process and may differ from the one above.

Create a New Project

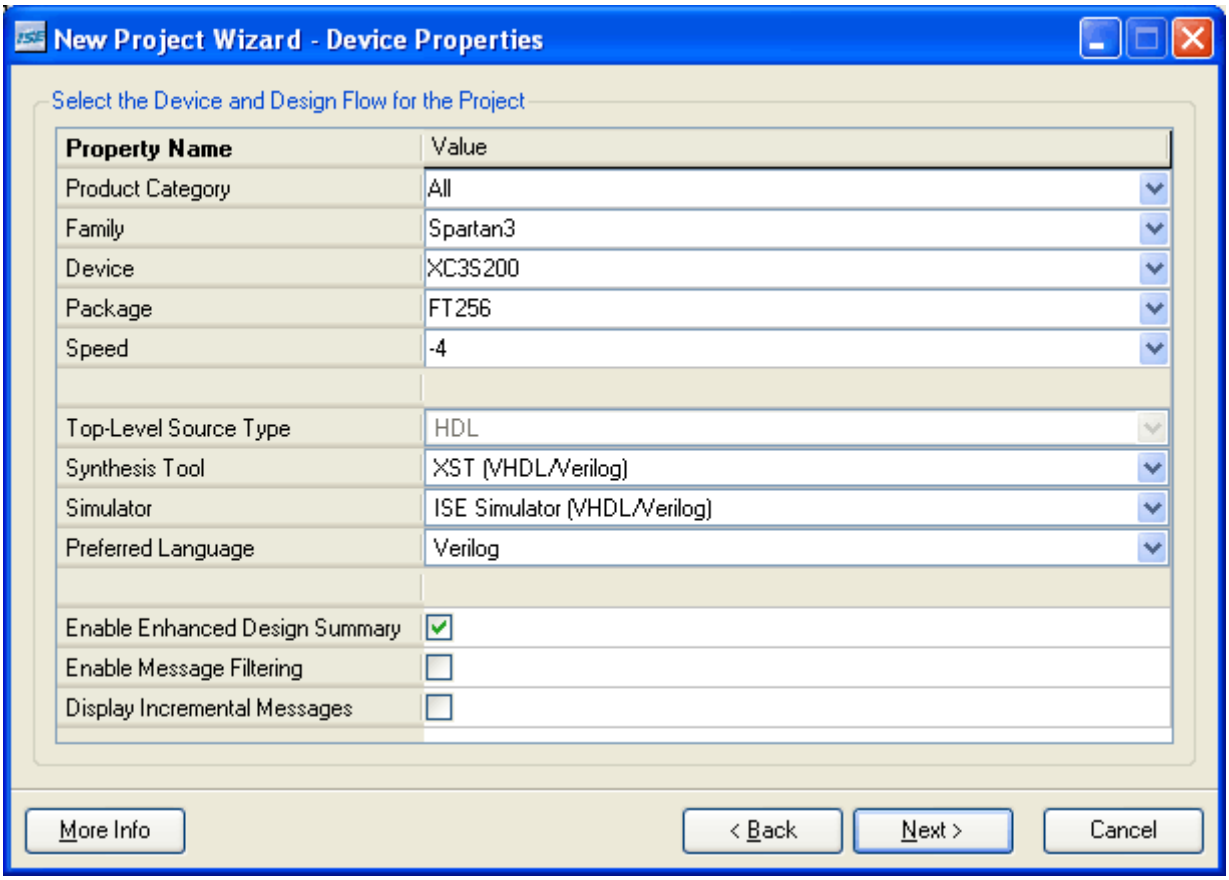
Create a new ISE project which will target the FPGA device on the Spartan-3 Startup Kit demo board.

To create a new project:

1. Select **File** > **New Project...** The New Project Wizard appears.
2. Type **tutorial** in the Project Name field.
3. Enter or browse to a location (directory path) for the new project. A tutorial subdirectory is created automatically.
4. Verify that **HDL** is selected from the Top-Level Source Type list.
5. Click **Next** to move to the device properties page.
6. Fill in the properties in the table as shown below:
   - Product Category: **All**
   - Family: **Spartan3**
   - Device: **XC3S400**
   - Package: **PQ208**
   - Speed Grade: **-4**
   - Top-Level Source Type: **HDL**
   - Synthesis Tool: **XST (VHDL/Verilog)**
   - Simulator: **ISE Simulator (VHDL/Verilog)**
   - Preferred Language: **Verilog** (or **VHDL)**
   - Verify that **Enable Enhanced Design Summary** is selected.

   Leave the default values in the remaining fields.

   When the table is complete, your project properties will look like the following:

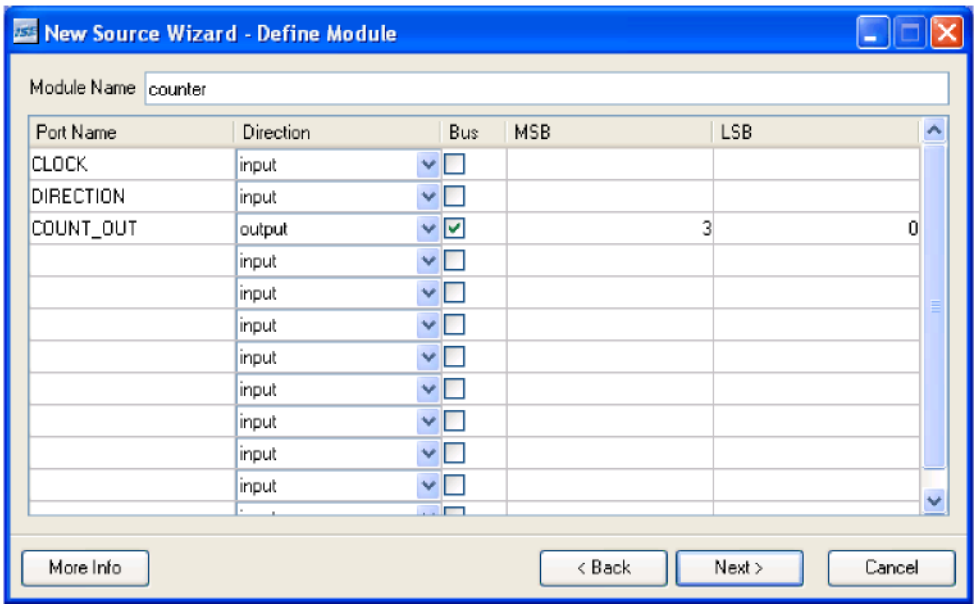


Project Device Properties

Creating a Verilog Source

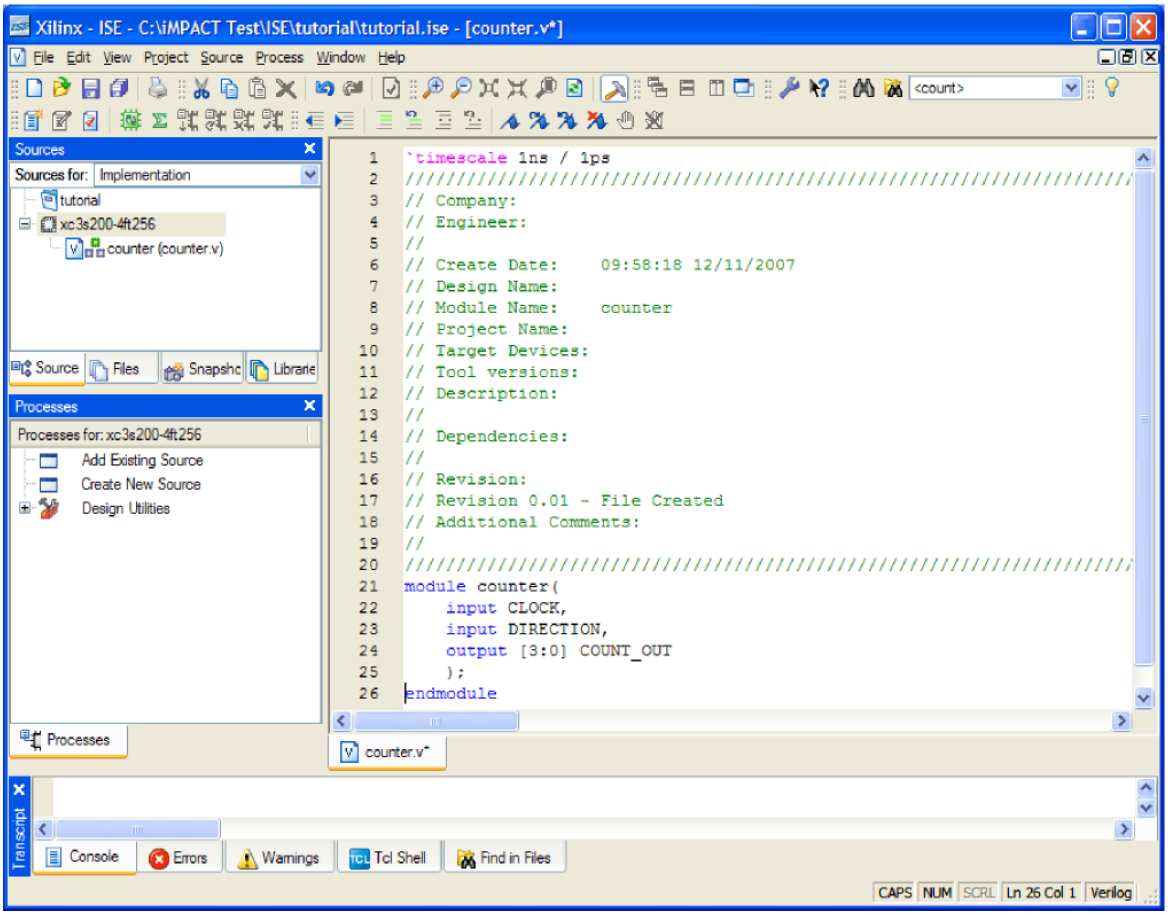
Create the top-level Verilog source file for the project as follows:

1. Click **New Source** in the New Project dialog box.
2. Select **Verilog Module** as the source type in the New Source dialog box.
3. Type in the file name **counter.**
4. Verify that the **Add to Project** checkbox is selected.
5. Click **Next.**
6. Declare the ports for the counter design by filling in the port information as shown below:
7. Click **Next,** then **Finish** in the New Source Information dialog box to complete the new source file template.
8. Click **Next,** then **Next,** then **Finish.**



Define Module

The source file containing the counter module displays in the Workspace, and the counter displays in the Sources tab, as shown below:



New Project in ISE

You have now created the Verilog source for the project.

Checking the Syntax of the New Counter Module

When the source files are complete, check the syntax of the design to find errors and typos.

1. Verify that **Implementation** is selected from the drop-down list in the Sources window.
2. Select the **counter** design source in the Sources window to display the related processes in the Processes window.
3. Click the **"+"** next to the Synthesize-XST process to expand the process group.
4. Double-click the **Check Syntax** process.

   Note: You must correct any errors found in your source files. You can check for errors in the Console tab of the Transcript window. If you continue without valid syntax, you will not be able to simulate or synthesize your design.

5. Close the Verilog file.

Design Simulation

Verifying Functionality using Behavioral Simulation

Create a Verilog Test Fixture (test bench) containing input stimulus to verify the functionality of the counter module. Create the test bench as follows:

1. Click **New Source in** the **counter** verilog file in the Sources window.
2. In the New Source Wizard, select **Verilog Test Fixture** as the source type, and type **counter_tbw** in the File Name

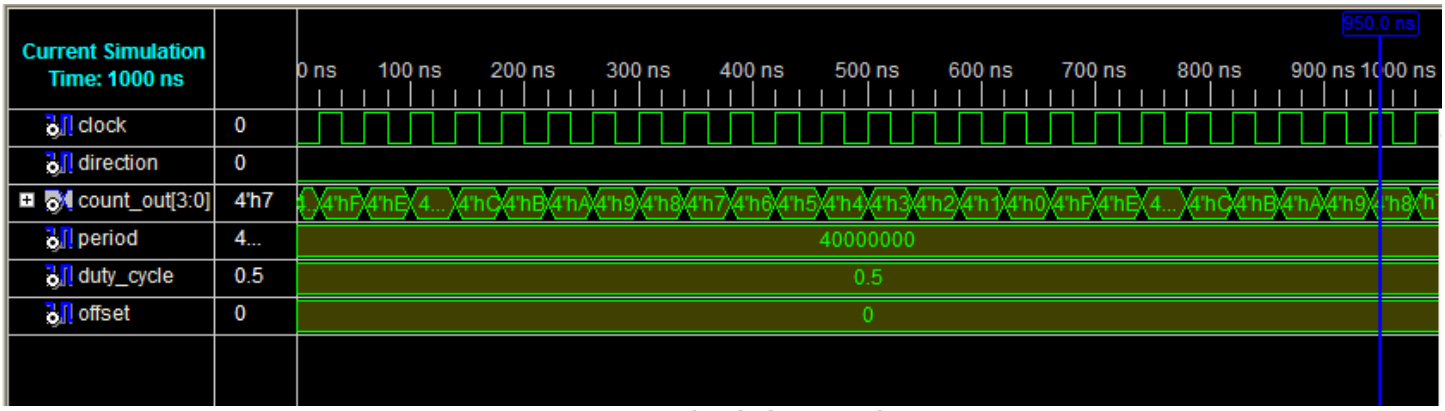
   field.
3. Click **Next.**
4. The Associated Source page shows that you are associating the test bench source file counter. Click **Next.**
5. Then click **finish**. Test Bench editor will open. Write the program and Save it.
6. In the Sources window, select the **Behavioral Simulation** view to see that the test bench file is automatically added to your project.

Simulating Design Functionality

Verify that the counter design functions as you expect by performing behavior simulation as follows:

1. Verify that **Behavioral Simulation** and **counter_tbw** are selected in the Sources window.
2. In the **Processes** tab, click the **"+"** to expand the Xilinx ISE Simulator process and double-click the **Simulate Behavioral Model** process. The ISE Simulator opens and runs the simulation to the end of the test bench.
3. To view your simulation results, select the **Simulation** tab and zoom in on the transitions.

The simulation waveform results will look like the following:



Simulation Results

Note: You can ignore any rows that start with **TX**.

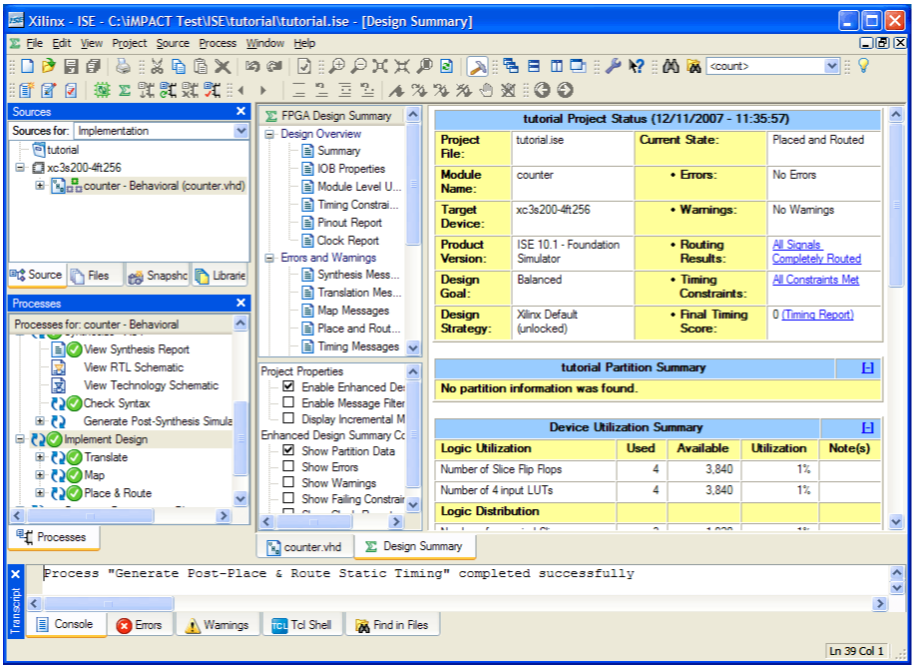
4. Verify that the counter is counting up and down as expected.
5. Close the simulation view. If you are prompted with the following message, "You have an active simulation open. Are you sure you want to close it?", click **Yes** to continue.

You have now completed simulation of your design using the ISE Simulator.

Implement Design and Verify Results

Implement the design and verify that it meets the timing constraints specified in the previous section.

1. Select the **counter** source file in the Sources window.
2. Open the Design Summary by double-clicking the **View Design Summary** process in the Processes tab.
3. Double-click the **Implement Design** process in the Processes tab.
4. Notice that after Implementation is complete, the Implementation processes have a green check mark next to them indicating that they completed successfully without Errors or Warnings.
5. Locate the **Performance Summary** table near the bottom of the Design Summary.
6. For Details report click the Detailed Report section for synthesis, Translation, Map and etc.



Post Implementation Design Summary