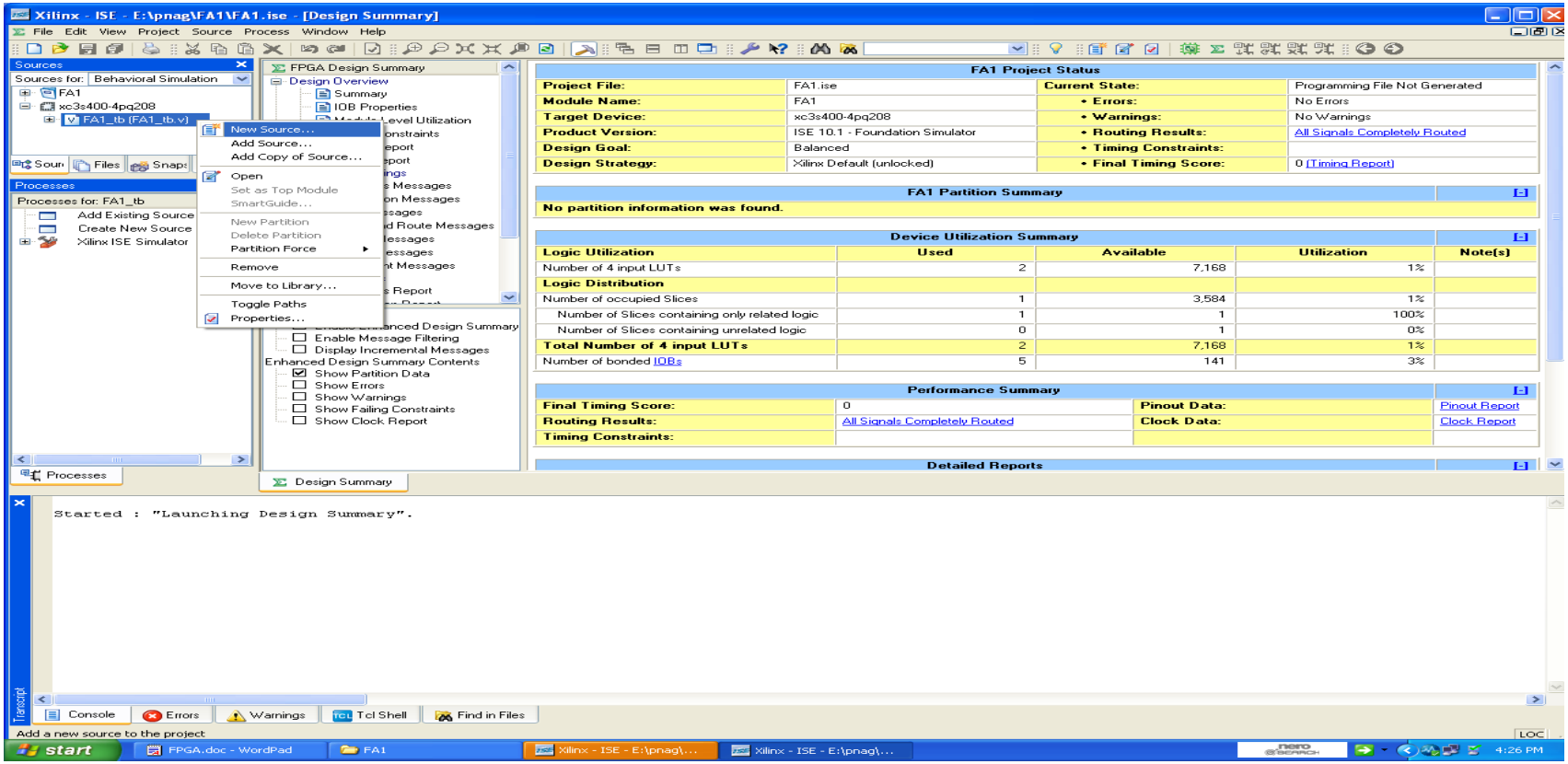
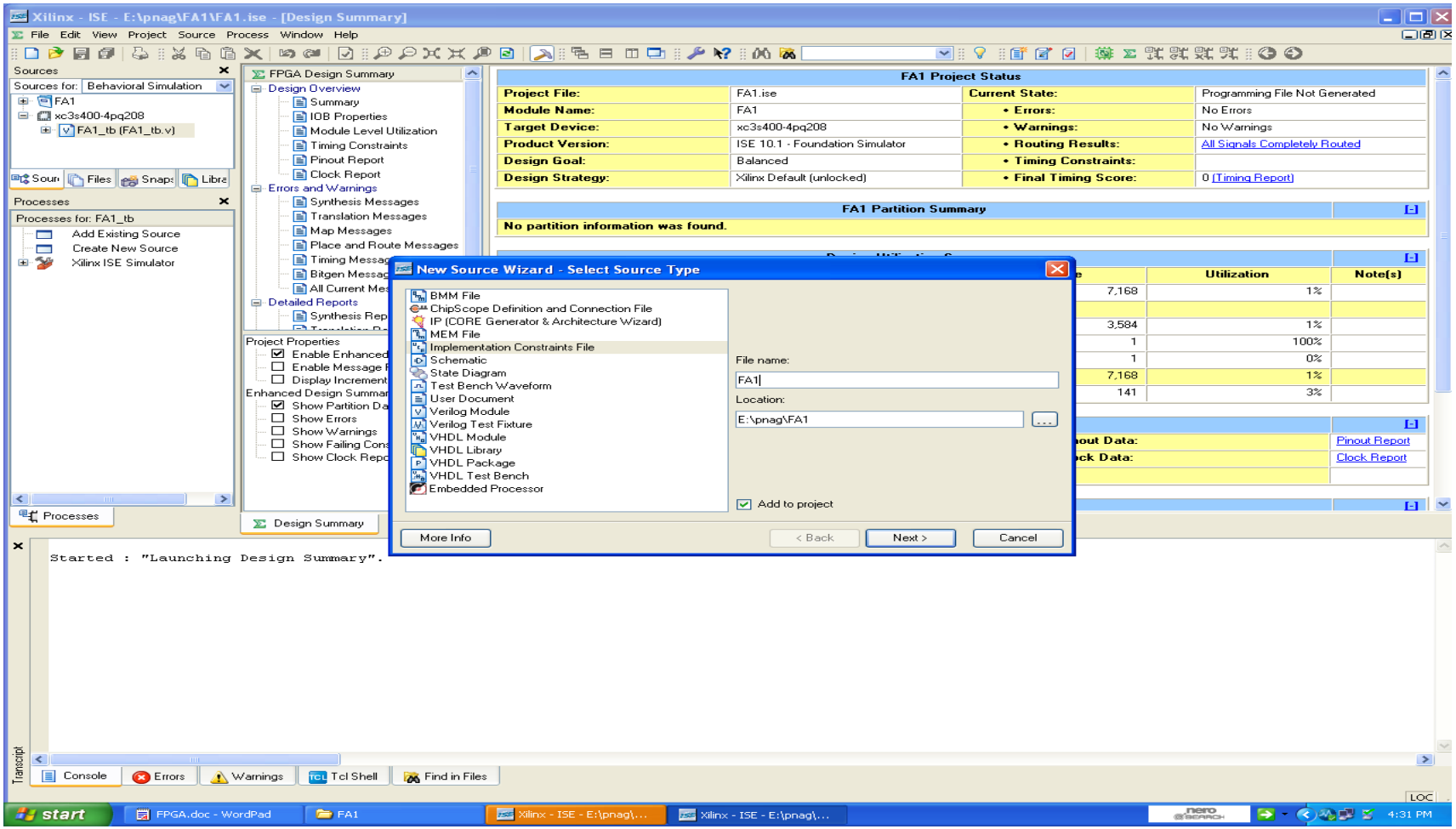
How you make the *UCF* file & download *program* on the kit?

1. **From Sources for :** select **Implementation / Behavioral Simulation**

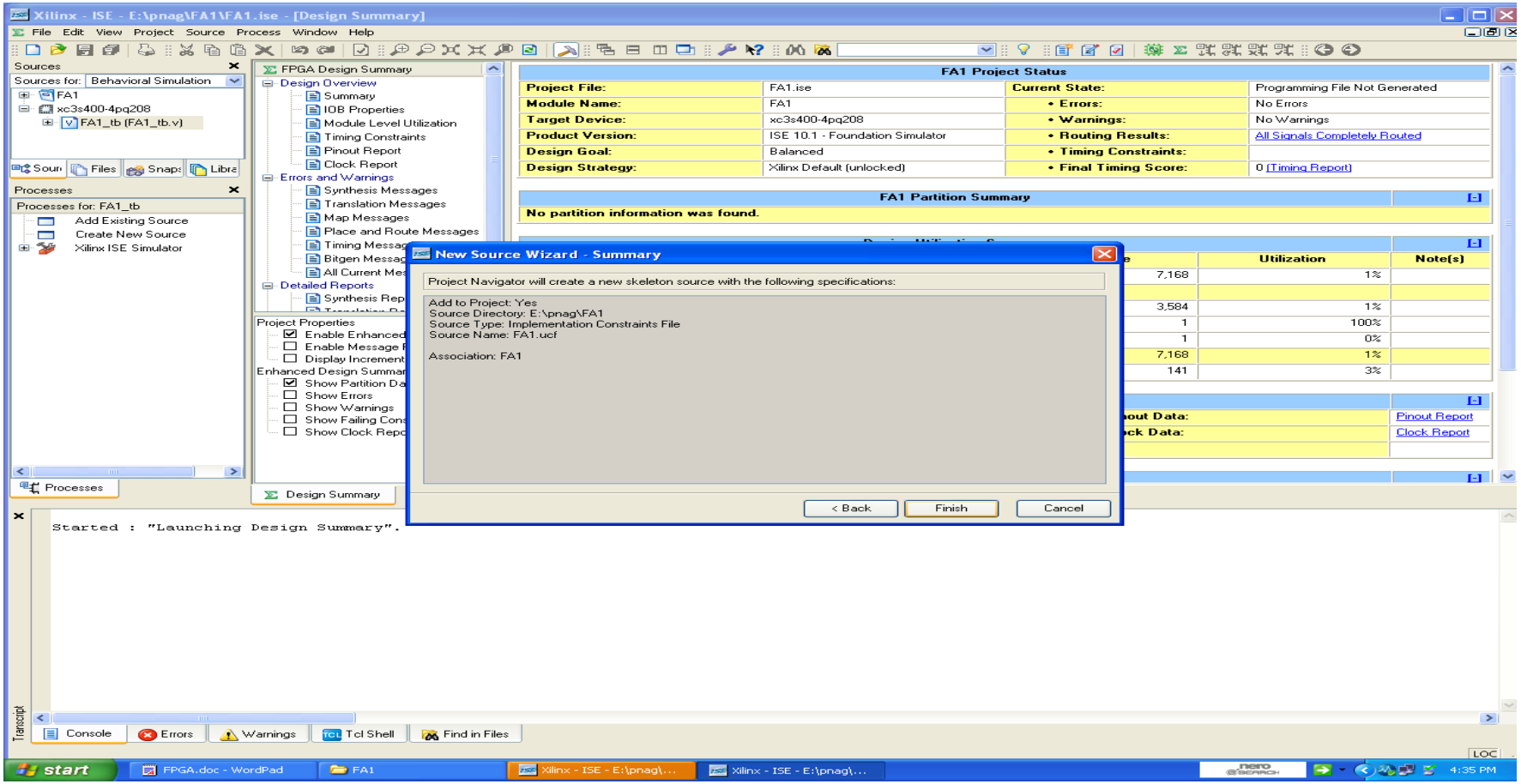
Select **XXXX.v** file from **"+ xc3s400-4pq208"** clicking on **'+'** symbol → Right Click in Mouse on the **XXXX.v** → **New Source**



Select **Implementation Constraints File (ucf)** from New Source Wizard → Give File Name as in New Project **XXXX** → **Next**

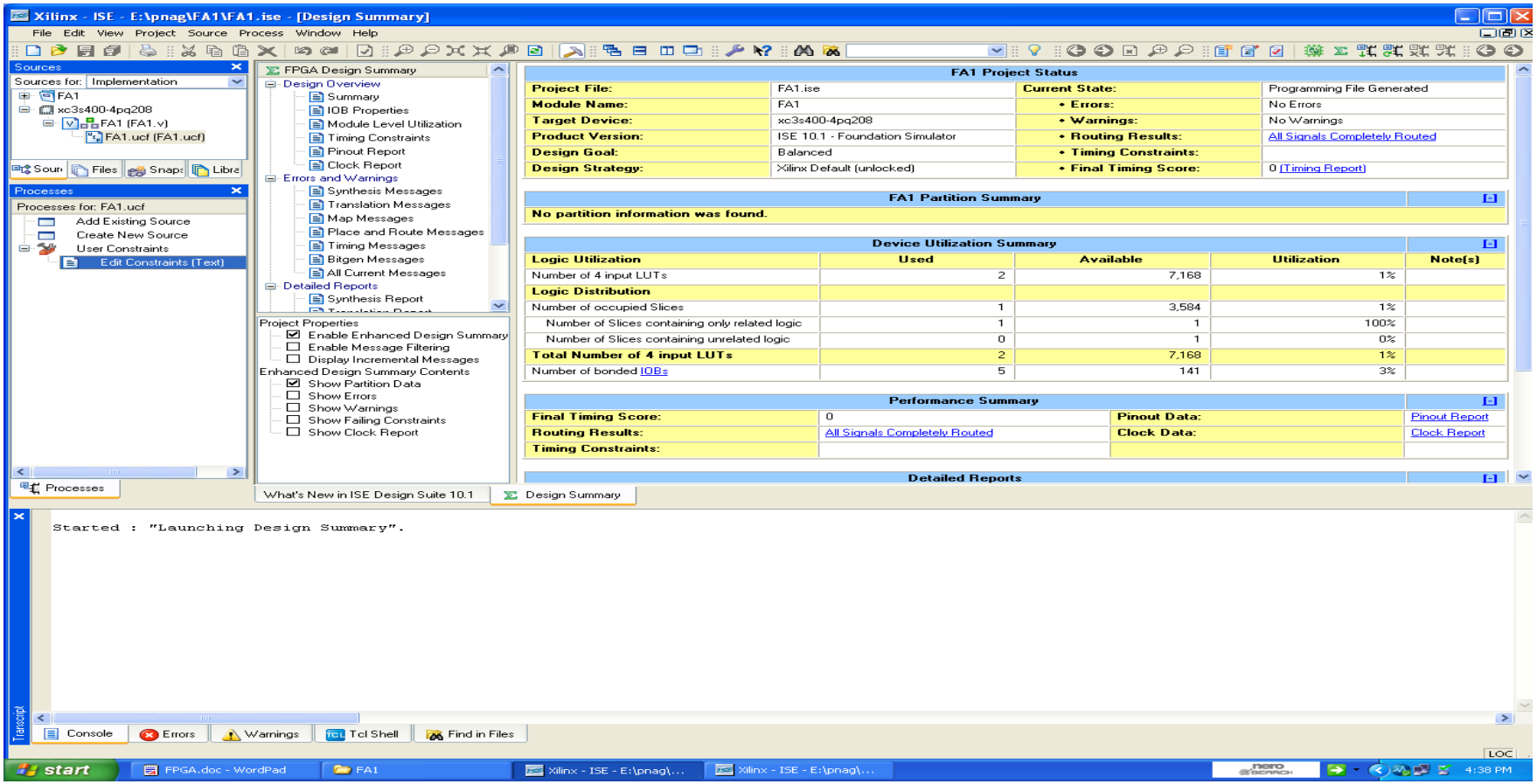


→ **Finish.**

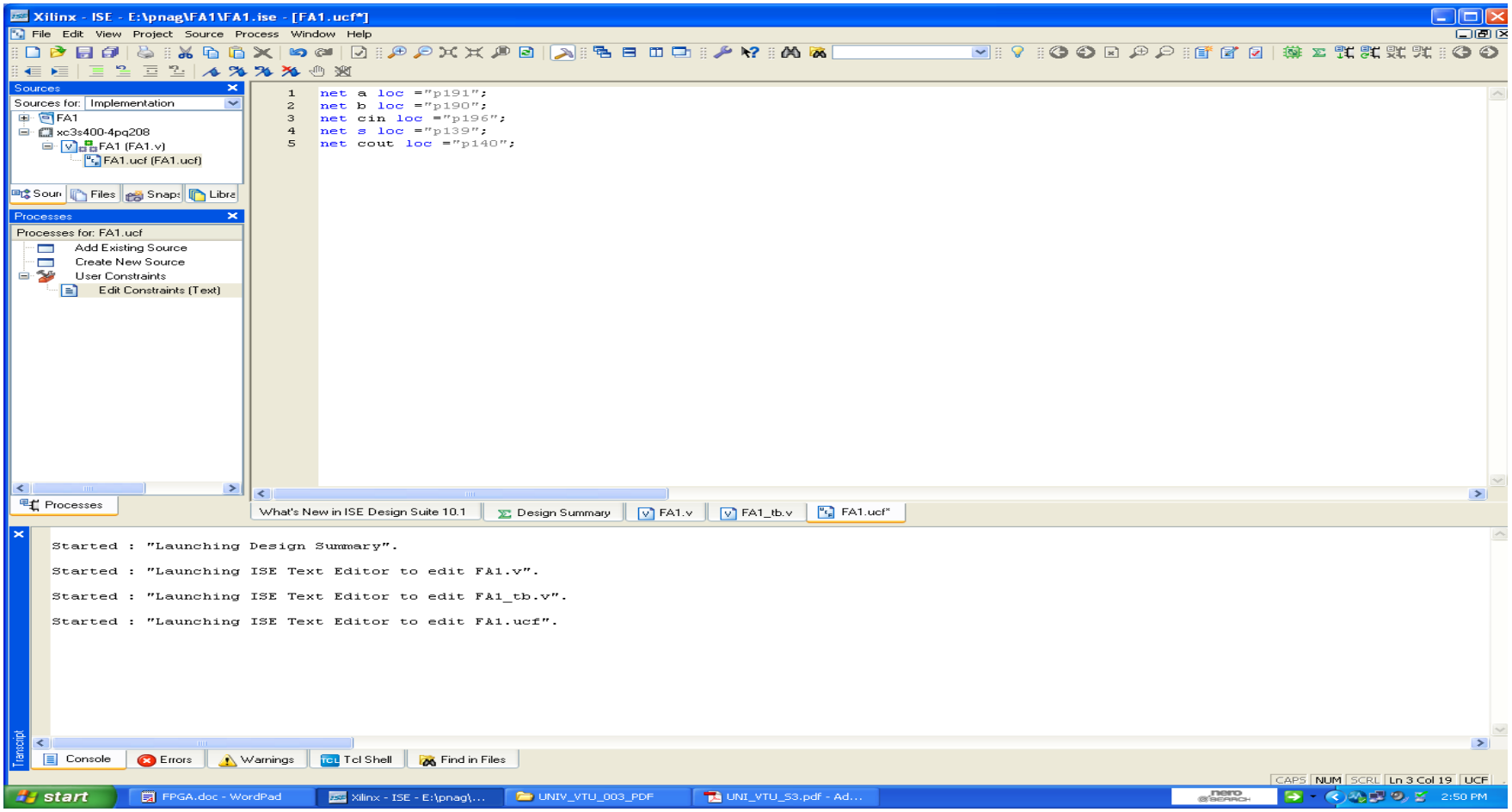

Xilinx - ISE - E:\pnag\FA1\FA1.ise - [Design Summary]
File Edit View Project Source Process Window Help
Sources
Sources for: Behavioral Simulation
FA1
xc3s400-4pq208
FA1_tb (FA1_tb.v)
Processes
Processes for: FA1_tb
Add Existing Source
Create New Source
Xilinx ISE Simulator
FPGA Design Summary
Design Overview
Summary
IOB Properties
Module Level Utilization
Timing Constraints
Pinout Report
Clock Report
Errors and Warnings
Synthesis Messages
Translation Messages
Map Messages
Place and Route Messages
Detailed Reports
Project Properties
Enhanced Design Summar
Show Partition Da
Show Errors
Show Warnings
Show Failing Cons
Show Clock Repo
FA1 Project Status
Project File: FA1.ise
Module Name: FA1
Target Device: xc3s400-4pq208
Product Version: ISE 10.1 - Foundation Simulator
Design Goal: Balanced
Design Strategy: Xilinx Default (unlocked)
Current State: Programming File Not Generated
• Errors: No Errors
• Warnings: No Warnings
• Routing Results: All Signals Completely Routed
• Timing Constraints:
• Final Timing Score: 0 (Timing Report)
FA1 Partition Summary
No partition information was found.
Utilization
Note(s)
7,168 1%
3,584 1%
1 100%
1 0%
7,168 1%
141 3%
Pinout Report
Clock Report
New Source Wizard - Summary
Project Navigator will create a new skeleton source with the following specifications:
Add to Project: Yes
Source Directory: E:\pnag\FA1
Source Type: Implementation Constraints File
Source Name: FA1.ucf
Association: FA1
< Back
Finish
Cancel
Started : "Launching Design Summary".
Console
Errors
Warnings
Tcl Shell
Find in Files
Transcript
start
FPGA.doc - WordPad
FA1
Xilinx - ISE - E:\pnag\...
Xilinx - ISE - E:\pnag\...
4:35 PM

2. **From Sources for:** select **Implementation**

Now click on **‘ +’** symbol of **“+XXXX.v”** file → select **“- XXXX.ucf’’** → go & click on **“+”**symbol of **“+ User Constraints”** under **Processes:** → double click on **Edit Constraints (Text)**

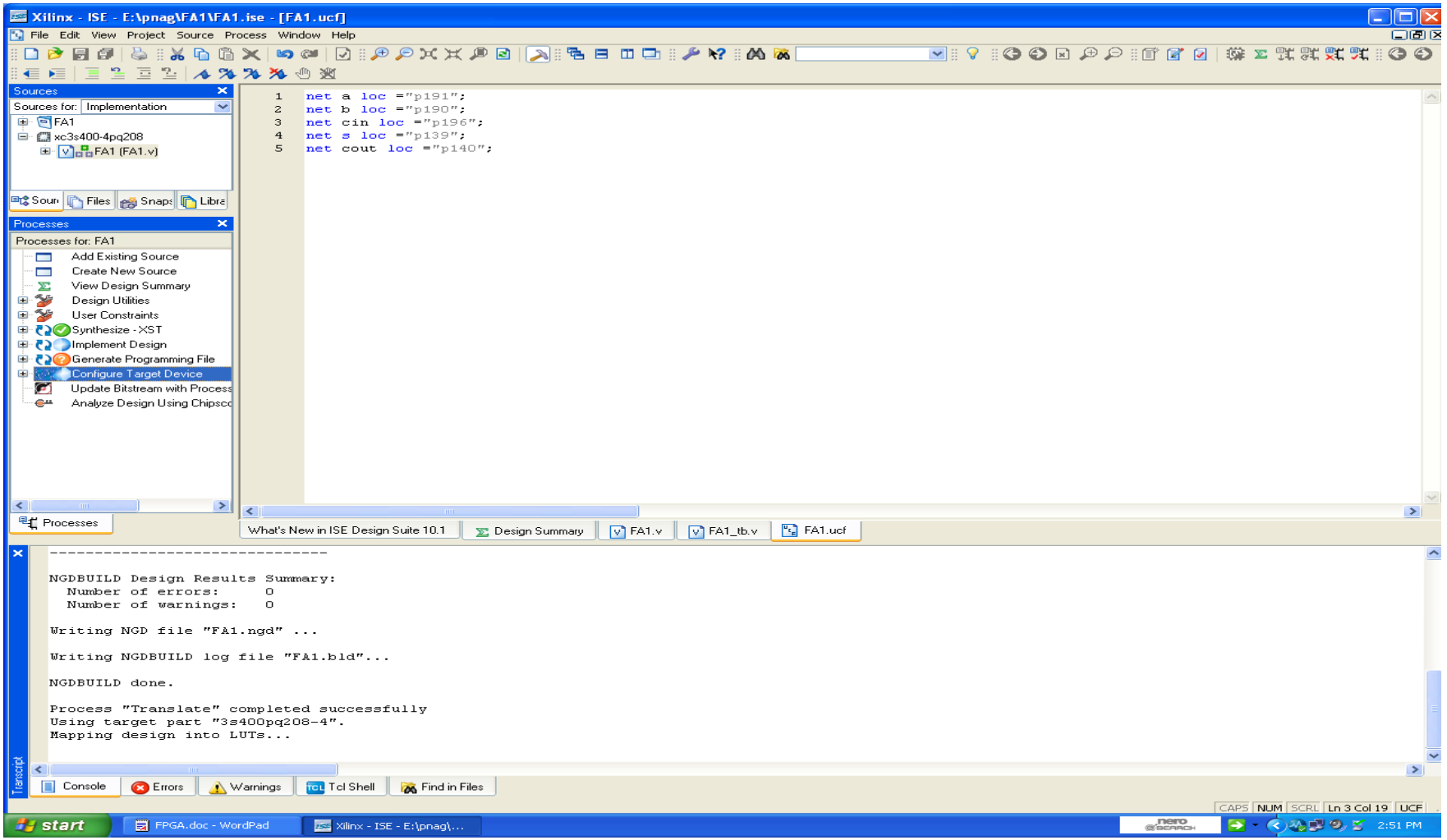


Now write the **I/P Pin** & **O/P LED** configuration as given below → **Save**

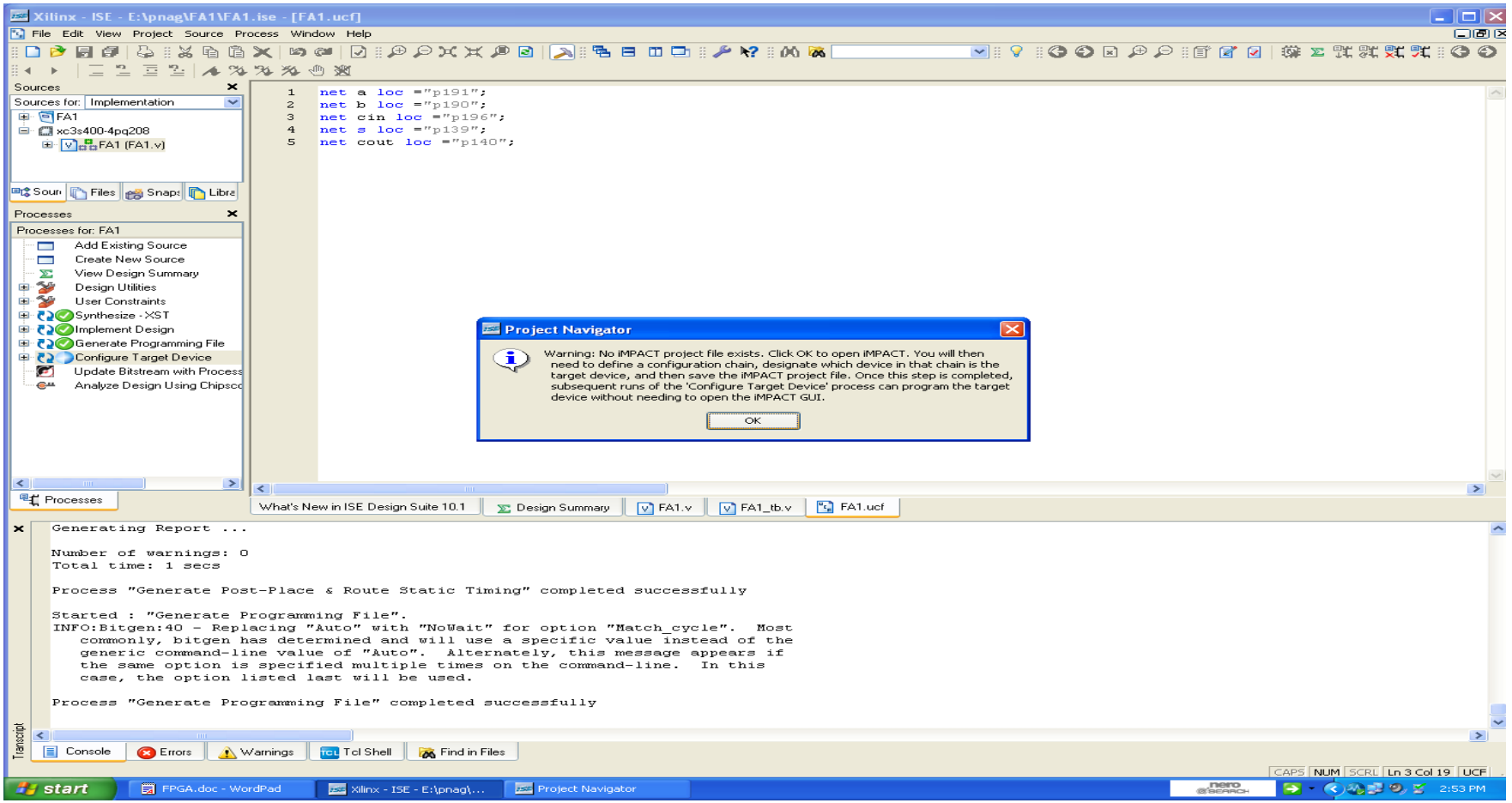


3. **From Sources for:** select **Implementation** → then select **XXXX.v** file

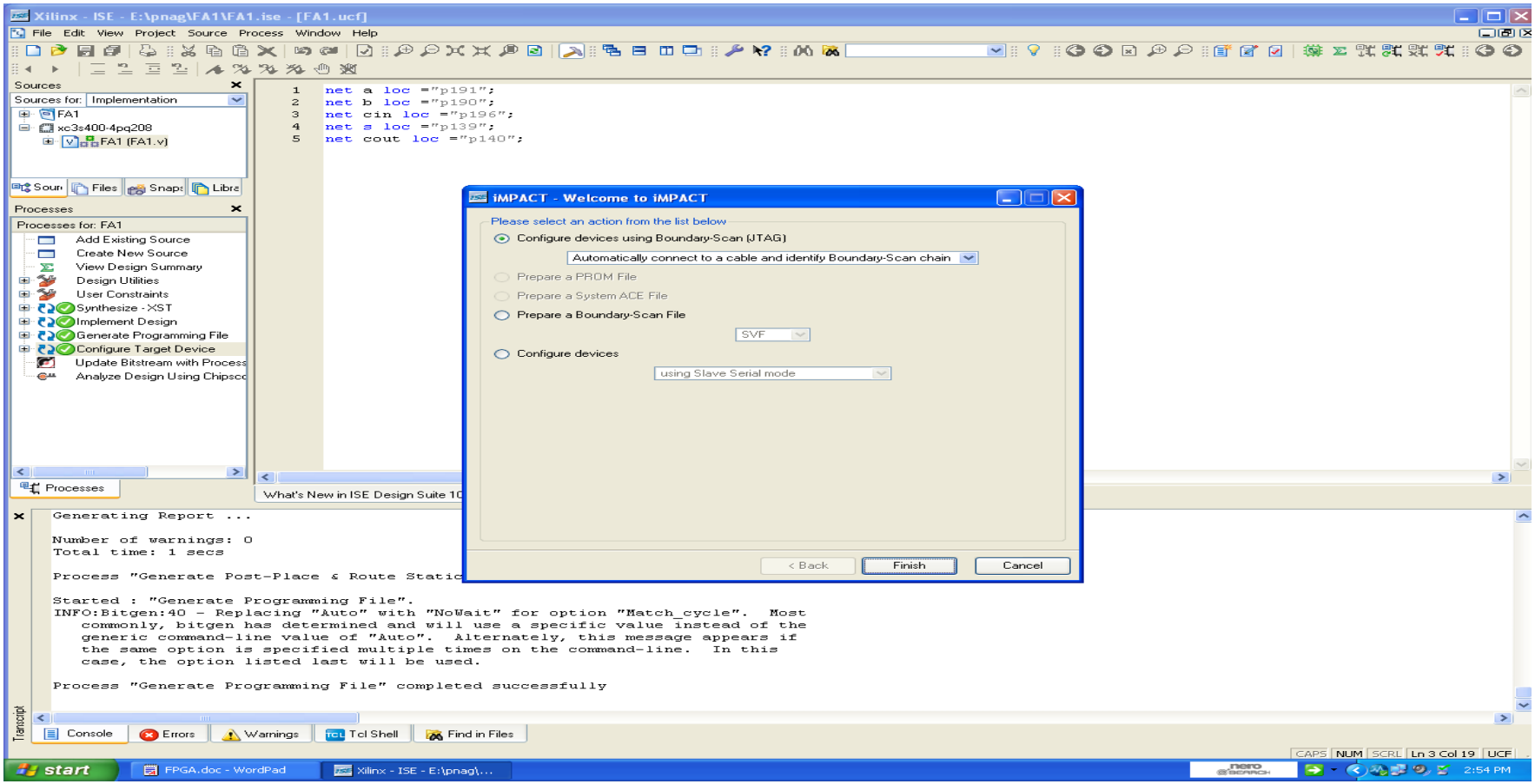
From Processes: select & double click on **"+ Configure Target Device" or** click on **"+"**symbol of **"+Configure Target Device"** and double click on **Manage Configuration Project (iMPACT)**



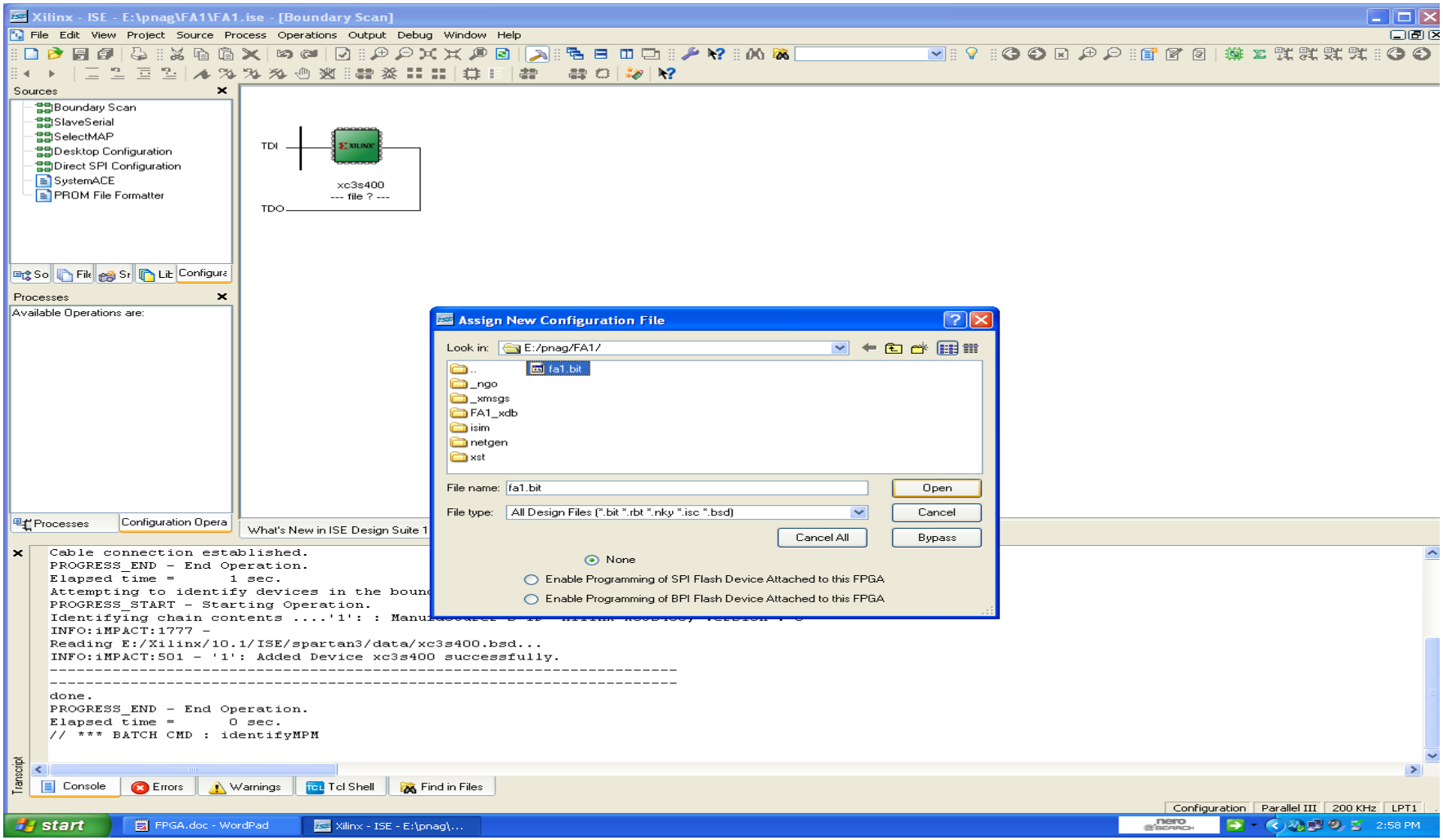
After appearing **Project Navigator → click OK**



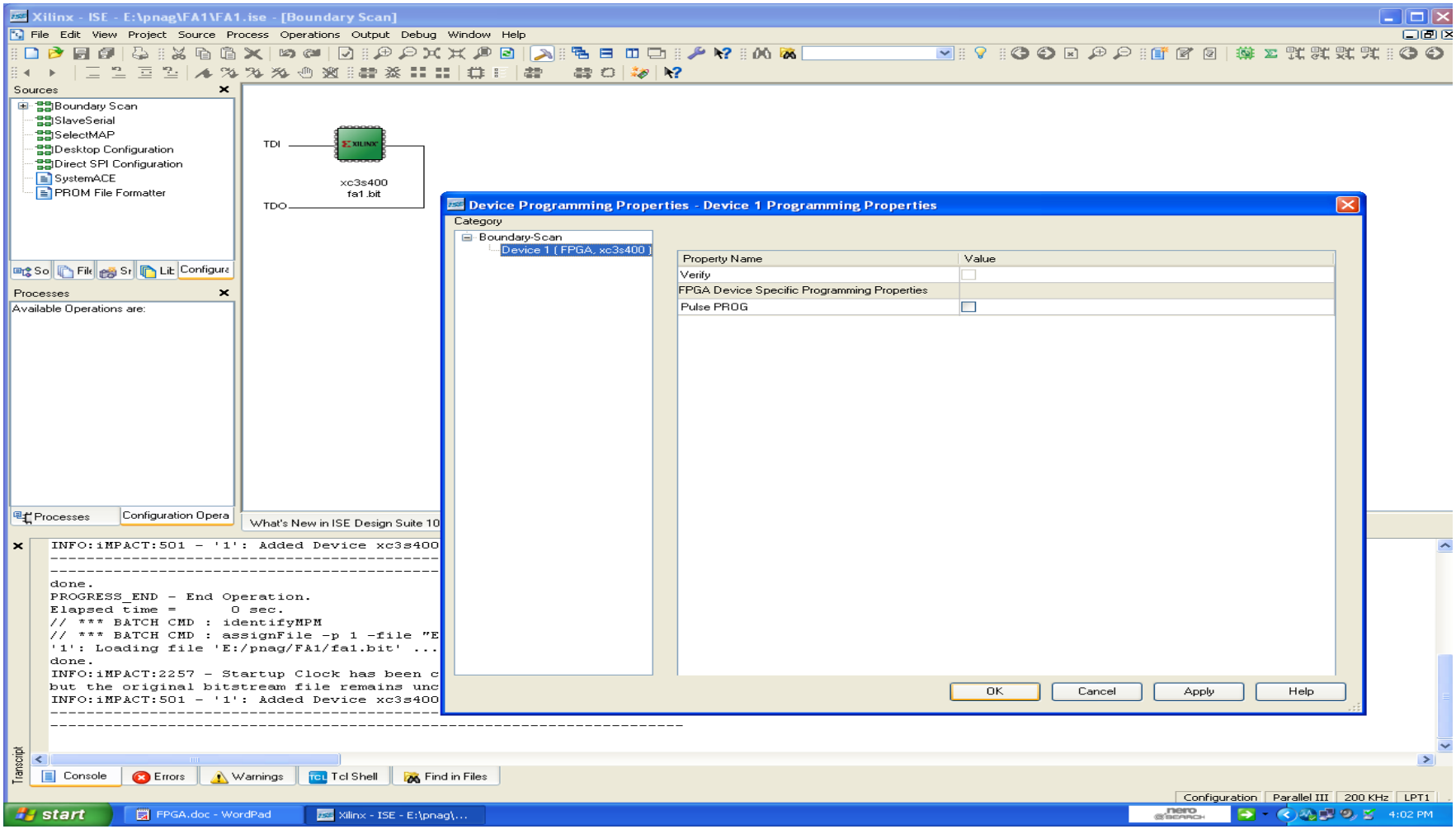
Then click on **Finish**



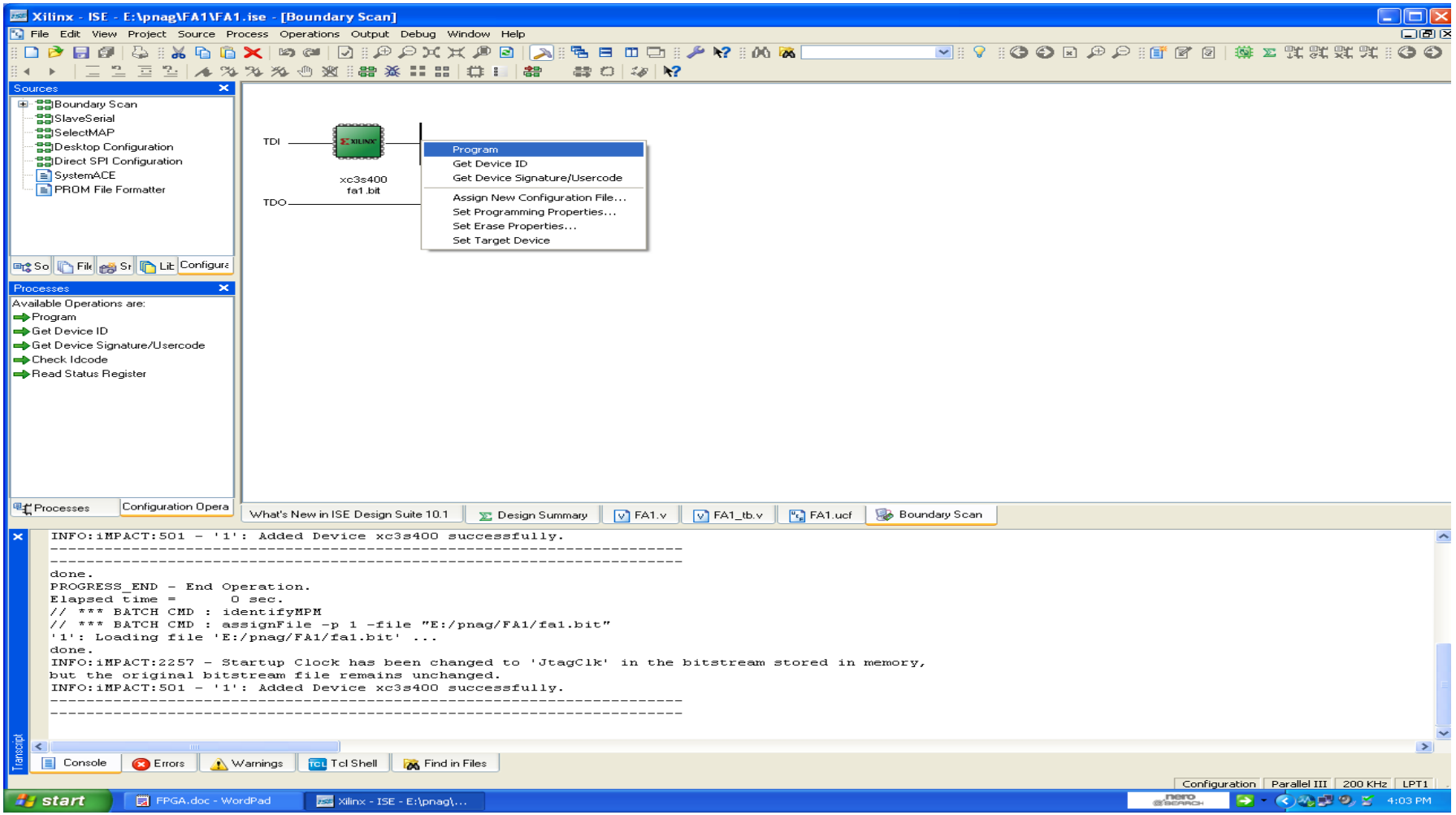
Select **XXXX.bit** file from **Assign New Configuration File** → **click on Open**



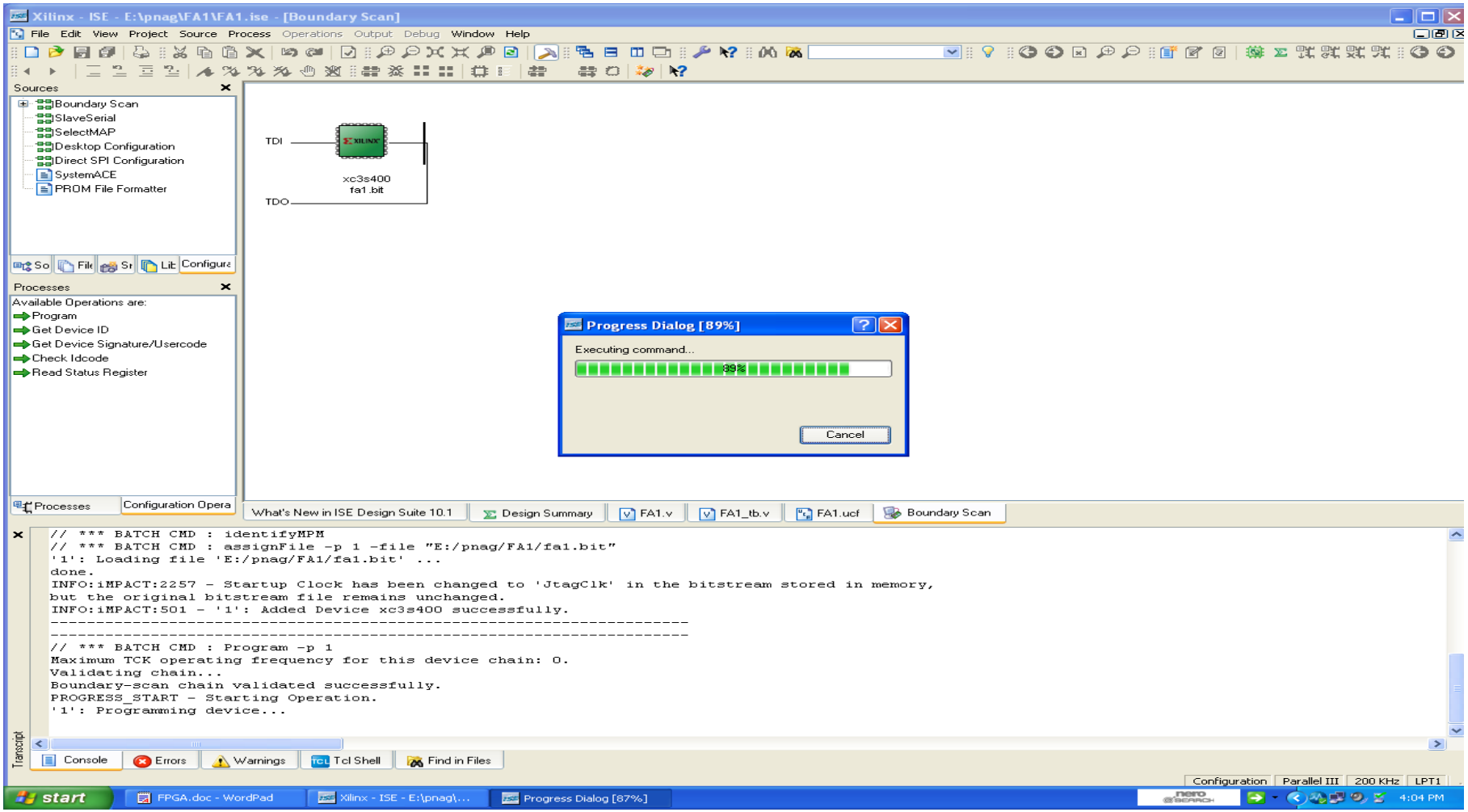
Click **OK** on **Device Programming Properties**



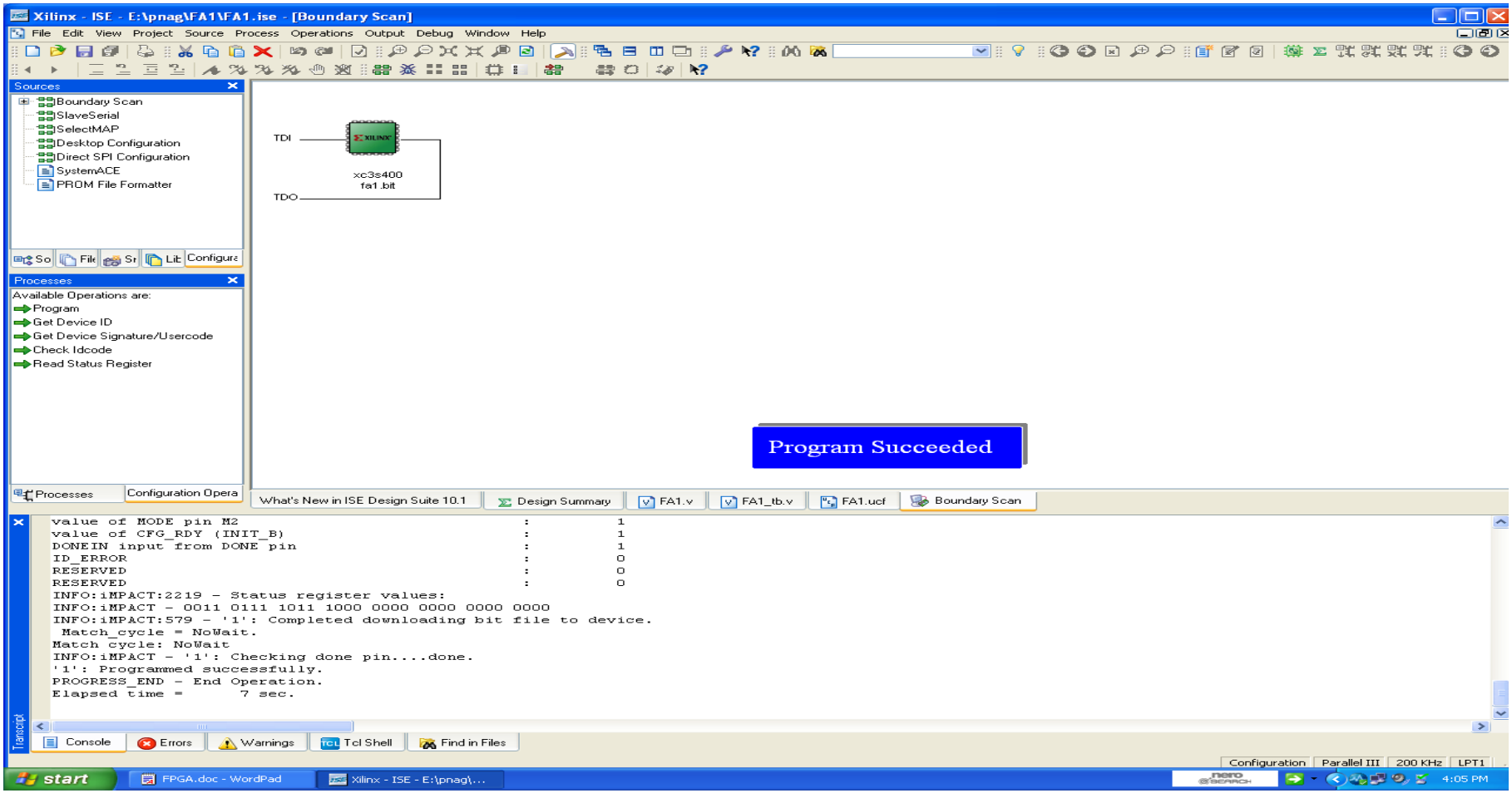
Select Xilinx symbol → **Right Click** just on **Xilinx** → click on **Program**



Progress Dialog [89%] starts loading



Now **Programme Succeeded**



Then go to **XILINX Trainer Kit** & the predetermined **Switches** corresponding to **I/P** combinations are adjusted manually and predetermined **LED**

glows depending upon the **I/P** combinations. Then **O/P** s are verified with the corresponding **I/P** s combinations according to the truth table of the

design.