R type Instruction and Register Bank

- **Instruction Format**

OP-CODE	Rs	Rt	Rd	Reserved Bits
6 bit	4 bit	4 bit	4 bit	14 bit

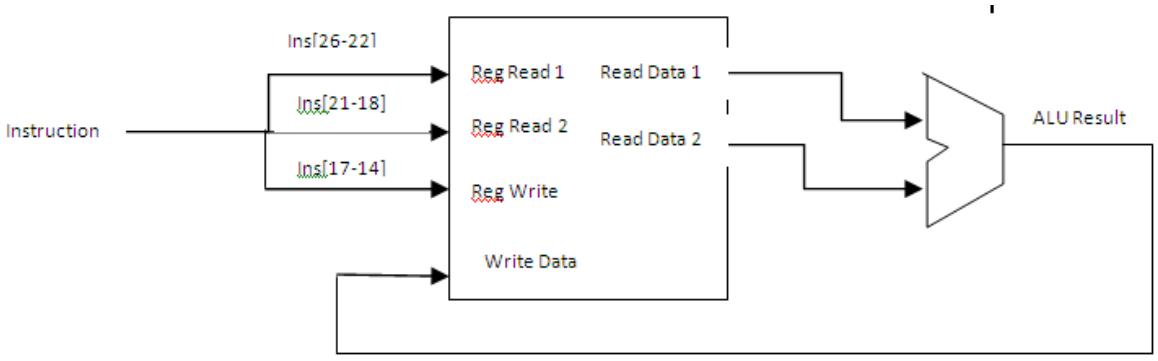
32 bit instruction made up of:

- Ins[31-26] – Op Code
- Ins [26-22] – Read Register 1
- Ins [21-18] – Read Register 2
- Ins [17-14] – Write Register
- Ins[13-0] – Reserved Bits

- **Instructions Supported**

Sr. No.	OP Code	OP No.	Operation Implemented	Instruction Type	Rs	Rt	Rd
1	000000	0	ADD	R-type	Address(OP1)	Address(OP2)	Address(Dest)
2	000100	4	SUB	R-type	Address(OP1)	Address(OP2)	Address(Dest)
3	011000	24	AND	R-type	Address(OP1)	Address(OP2)	Address(Dest)
4	011110	30	OR	R-type	Address(OP1)	Address(OP2)	Address(Dest)
5	010110	22	XOR	R-type	Address(OP1)	Address(OP2)	Address(Dest)
6	010101	21	NOT	R-type	Address(OP1)	----------	Address(Dest)
7	001000	8	SLA	R-type	Address(OP1)	Address(OP2)	Address(Dest)
8	001010	10	SRA	R-type	Address(OP1)	Address(OP2)	Address(Dest)
9	001011	11	SRL	R-type	Address(OP1)	Address(OP2)	Address(Dest)

- **Data Path for R Type Instructions**



- Reg read 1 = Read Address 1
- Reg read 2 = Read Address 2
- Reg Write = Write Address

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- **Control Signals**
  - To ALU : 5 control bits
  - Register Write - 1 bit

Register Bank

The register bank will have 16 registers, 3 16x1 multiplexers for Rs, Rd and Rt. Each register is of 32 bits.

Register 0
Register 1
Register 2
Register 3
Register 4
Register 5
Register 6
Register 7
Register 8
Register 9
Register 10
Register 11
Register 12
Register 13
Register 14
Register 15

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