CSE206 (Digital Logic Design Sessional)

Experiment No. 04

Name of the Experiment

Comparator, adder / subtractor

Group no.	**01**
Group Members	**1805061, 1805062, 1805063, 1805064, 1805065**
Section	**B1**
Department	**CSE**
Date of Submission	**03.04.2021**

Problem No. 01

Problem specification:

Design using basic gates, a 2-bit comparator to compare 2-bit numbers X and Y. The circuit should provide 3 output lines to indicate X>Y, X=Y and X<Y.

Required instruments:

No.	Name of the Instrument	Quantity
1	IC - Hex 1-input Inverter gate (74x04)	1 piece
2	IC- Quad 2-input AND gate (74x08)	2 pieces
3	IC- Quad 2-input OR gate (74x32)	1 piece
4	IC- Quad 2-input XOR gate (74x86)	1 piece
5	Input pin	4 pieces
6	Output pin	3pieces
7	Wires	A lot
8	Software Logisim	

Truth Table:

Here A_1, A_0, B_1, B_0 are the input pins and L, E, G are the output pins. L is on when A<B, E is on when A=B and G is on when A>B. The truth table is shown below:

A_1	A_0	B_1	B_0	L	E	G
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Simplification of the Equation:

From the truth table we can derive the equation of L, E, and G.

Now,

$L = A_1'A_0'B_1'B_0 + A_1'A_0'B_1B_0' + A_1'A_0'B_1B_0 + A_1'A_0B_1B_0' + A_1'A_0B_1B_0 + A_1A_0'B_1B_0$

$= A_1'A_0'B_1B_0' + A_1'A_0'B_1B_0 + A_1'A_0B_1B_0' + A_1'A_0B_1B_0 + A_1'A_0'B_1'B_0 + A_1A_0'B_1B_0$

$= A_1' B_1 (A_0'B_0' + A_0'B_0 + A_0B_0' + A_0B_0) + (A_1'B_1'+ A_1B_1) A_0'B_0$

$= A_1' B_1 (A_0'(B_0' + B_0) + A_0(B_0' + B_0)) + (A_1 \oplus B_1)' A_0'B_0$ [$X'Y' + XY = (X \oplus Y)'$]

$= A_1' B_1 (A_0' + A_0) + (A_1 \oplus B_1)' A_0'B_0$ [$X' + X = 1$ and $X.1 = X$]

$= A_1' B_1 + (A_1 \oplus B_1)' A_0'B_0$

$E = A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0'B_1B_0' + A_1A_0B_1B_0$

$= A_1'B_1'(A_0'B_0' + A_0B_0) + A_1B_1 (A_0'B_0' + A_0B_0)$

$= (A_1'B_1' + A_1B_1) (A_0'B_0' + A_0B_0)$

$= (A_1 \oplus B_1)' (A_0 \oplus B_0)'$ [$X'Y' + XY = (X \oplus Y)'$]

$G = A_1'A_0B_1'B_0' + A_1A_0'B_1'B_0' + A_1A_0'B_1'B_0 + A_1A_0B_1'B_0' + A_1A_0B_1'B_0 + A_1A_0B_1B_0'$

$= A_1A_0'B_1'B_0' + A_1A_0'B_1'B_0 + A_1A_0B_1'B_0' + A_1A_0B_1'B_0 + A_1'A_0B_1'B_0' + A_1A_0B_1B_0'$

$= A_1B_1' (A_0'B_0' + A_0'B_0 + A_0B_0' + A_0B_0) + (A_1'B_1'+ A_1B_1) A_0B_0'$

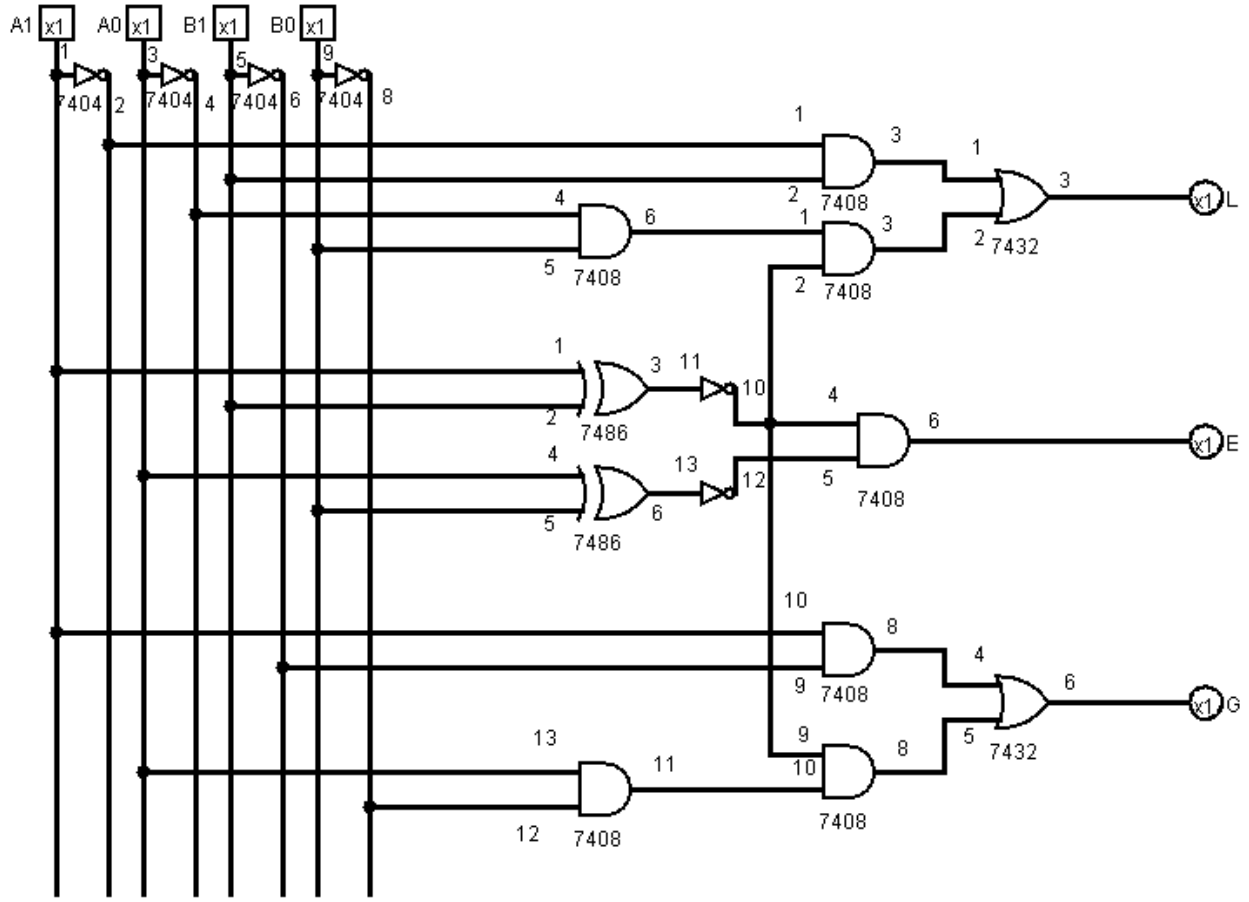
$= A_1 B_1' (A_0'(B_0' + B_0) + A_0(B_0' + B_0)) + (A_1 \oplus B_1)' A_0B_0'$ [$X'Y' + XY = (X \oplus Y)'$]

$= A_1B_1' (A_0' + A_0) + (A_1 \oplus B_1)' A_0B_0'$ [$X' + X = 1$ and $X.1 = X$]

$= A_1B_1' + (A_1 \oplus B_1)' A_0B_0'$

Circuit Diagram:

The circuit diagram is shown below-



Observation:

We can make some observations from the truth table and the simplified equations and can derive equations for a n-bit comparator.

- <u>E Function:</u>

  From the truth table we can see that, output pin E will be on if $A_i = B_i$, where i=0, 1,…, n-1.

  Two bits A_i and B_i are equal if, $x_i = (A_i \odot B_i) = (A_i \oplus B_i)'$ holds.

  So, for n-bit comparator, $E = x_0x_1...x_{n-1,}$ where $x_i = (A_i \oplus B_i)'$.

- L Function:

  From the truth table we can see that, output pin L will be on if

  - $A_{n-1}<B_{n-1}$
  - $A_{n-1}=B_{n-1}$ and $A_{n-2}< B_{n-2}$
  - $A_{n-1}=B_{n-1}$ and $A_{n-2}= B_{n-2}$ and $A_{n-3}< B_{n-3}$ and so on.

  So, for n-bit comparator, $L = A_{n-1}'B_{n-1} + x_{n-1} A_{n-2}'B_{n-2} + \ldots + x_{n-1}x_{n-2}\ldots x_1A_0'B_0$,

  where $x_i = (A_i \oplus B_i)'$.

- G Function:

  From the truth table we can see that, output pin L will be on if

  - $A_{n-1}>B_{n-1}$
  - $A_{n-1}=B_{n-1}$ and $A_{n-2}> B_{n-2}$
  - $A_{n-1}=B_{n-1}$ and $A_{n-2}= B_{n-2}$ and $A_{n-3}> B_{n-3}$ and so on.

  So, for n-bit comparator, $L = A_{n-1}B_{n-1}' + x_{n-1} A_{n-2}B_{n-2}' + \ldots + x_{n-1}x_{n-2}\ldots x_1A_0B_0'$,

  where $x_i = (A_i \oplus B_i)'$.

Problem No. 02

Problem specification:

Design a 1-bit full sub tractor circuit using basic logic gates. Inputs are P, Q and R denoting minuend, subtrahend and previous borrow respectively. The outputs are D and B representing the difference and output borrow.

Required instruments:

No.	Name of the Instrument	Quantity
1	IC - Hex 1-input Inverter gate (74x04)	1 piece
2	IC- Quad 2-input AND gate (74x08)	1 piece
3	IC- Quad 2-input OR gate (74x32)	1 piece
4	IC- Quad 2-input XOR gate (74x86)	1 piece
5	Input pin	3 pieces
6	Output pin	2 pieces
7	Wires	A lot
8	Software Logisim	

Truth Table:

Here P, Q, R are the input pins and D and Bout is the output pin.

The truth table of the equation of F:

Inputs			Outputs	
Minuend(P)	Subtrahend(Q)	Borrow(R)	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Simplification of the Equation:

$D = P'Q'R+P'QR'+ \quad PQ'R'+PQR$

$= R(P'Q'+PQ) + R'(P'Q+PQ')$

$= R(P'Q+PQ')' + R'(P'Q+PQ')$

$= P \oplus Q \oplus R$

So, the simplified equation is for D: P ⊕Q ⊕R

And,

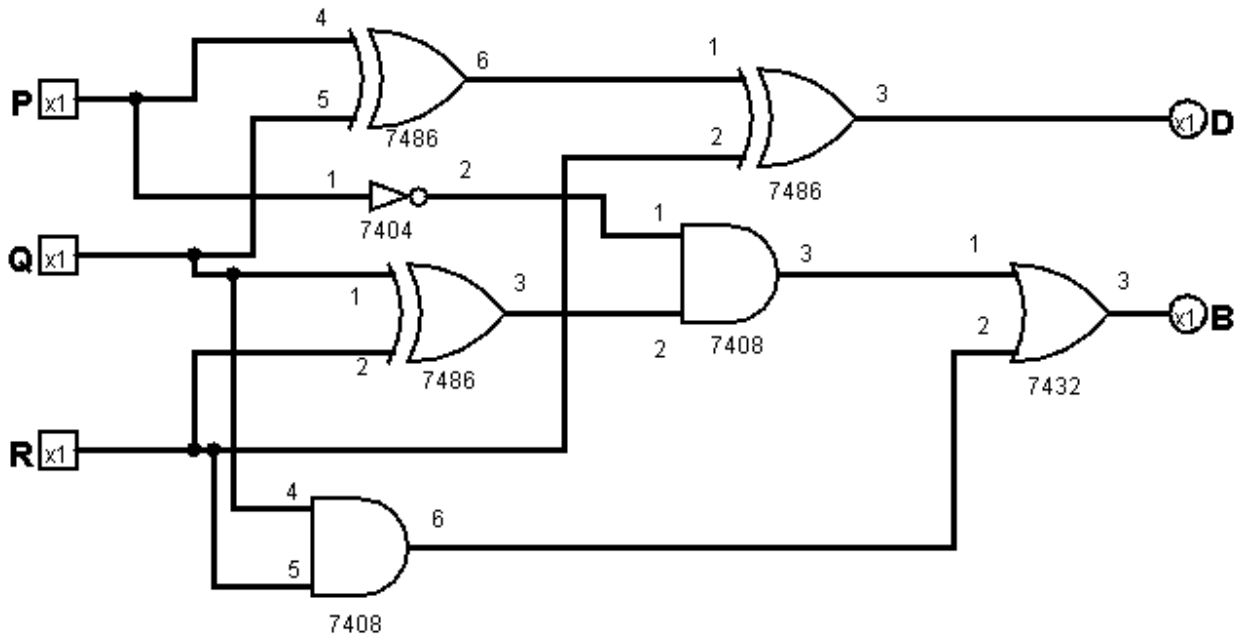
B(out) = P'Q'R+P'QR'+P'QR+PQR

= P'(Q'R+QR') + QR(P+P')

=P'(Q ⊕R) + QR [since P+P' =1]

So, the simplified equation is for B(out): P'(Q ⊕R) + QR

Circuit Diagram:



Observation:

After simplifying the equation, we can see that the function represents P ⊕ Q ⊕ R

And P'(Q ⊕R) + QR. Combination of X-OR and AND gates.