Course Number: CSE206

Digital Logic Design Sessional

Experiment No:	**07**
Topic:	**Flip-Flops and Registers**
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Section	**B1**
Department	**CSE**
Date of Submission	**12.06.2021**

PROBLEM NO: 1

Problem Statement:

Design and implement a **master-slave JK** *flip-flop using only* **NAND** *gates.*

Truth Table:

Clock	Inputs		Present State	Next State
	J	K	Q_n	Q_{n+1}
0	X	X	X	Q_n
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Excitation Table:

Clock	**J**	**K**	**Q_{n+1}**	**Mode**
0	X	X	Q_n	No change
1	0	0	Q_n	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Q_n'	Toggle

Required Equation in Minimized Form (Using K-Map):

- **K-Map for Q_{n+1}:**

Q_n \ JK		00	01	11	10
		J'K'	**J'K**	**JK**	**JK'**
0	Q_n'	0	0	1	1
1	Q_n	1	0	0	1

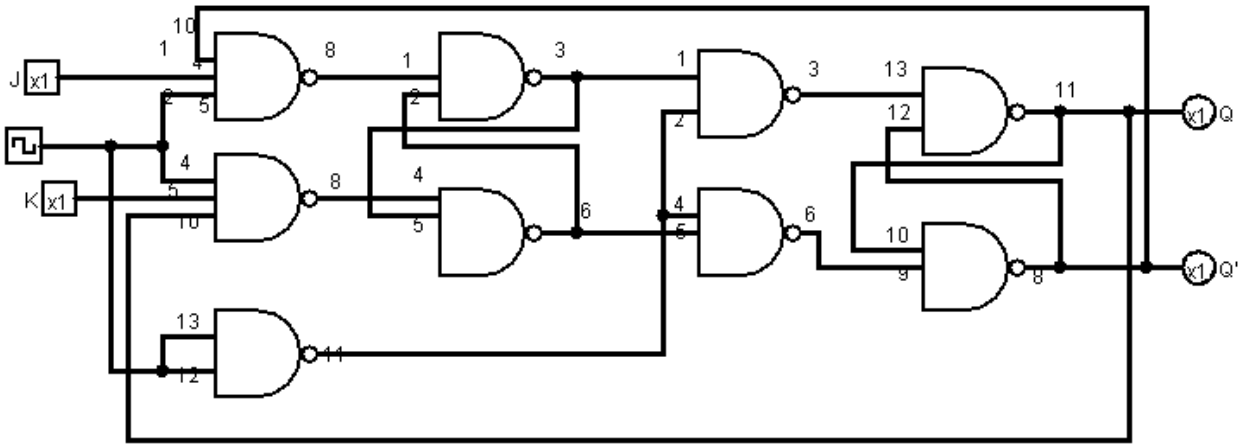
Q_{n+1} = JQ_n' + Q_nK' [Combining K-map results]

= JQ_n' + Q_nK'

Required Instruments:

No.	Name of Instruments	Quantity
1.	IC-7400	4
2.	1 bit Input Pin	2
3.	1 bit output Pin	2
4.	Clock pulse	1
5.	Wires	A lot

Circuit Diagram:



Observation:

Master-Slave JK Flip-Flop is introduced to solve the continuous toggling of output in specific cases, and taking one output as current state in input, it solves the problem.

PROBLEM NO: 2

Problem Statement:

Design and implement a 4-bit universal shift register.

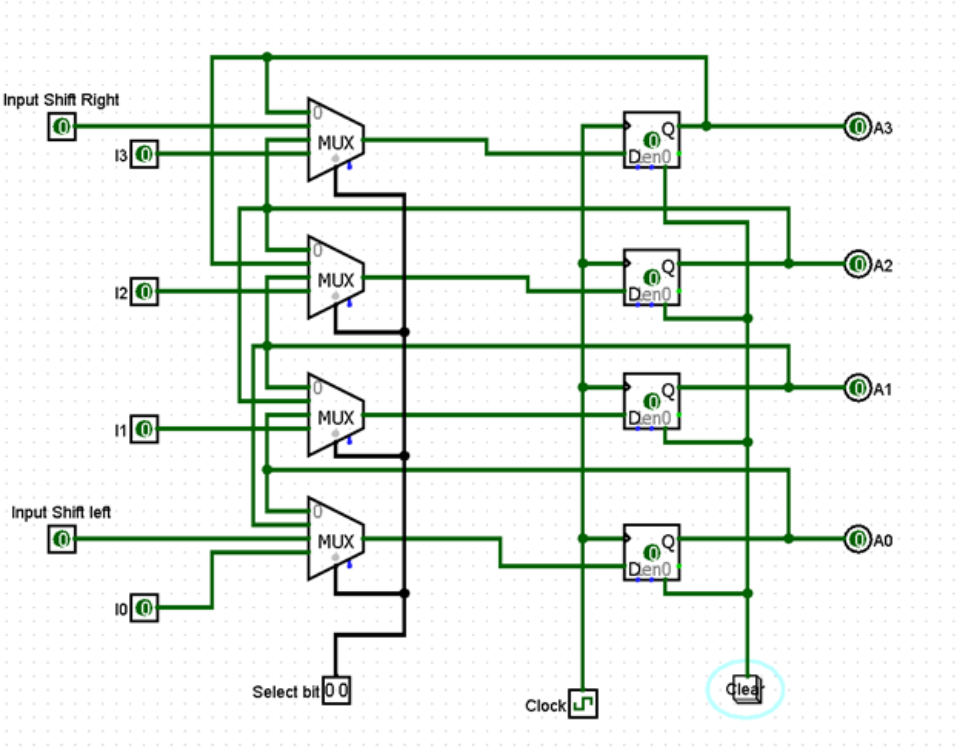
Excitation Table:

Input					Output				
Clear	Clock	S_1	S_0	Internal Signal	A_3	A_2	A_1	A_0	Mode
0	x	x	x	x	0	0	0	0	Async
1	x	0	0	x	A_3	A_2	A_1	A_0	Hold
1	1	0	1	A_{i-1}	Input right	A_3	A_2	A_1	Shift Right
1	1	1	0	A_{i+1}	A_2	A_1	A_0	Input left	Shift Left
1	1	1	1	A_i	I_3	I_2	I_1	I_0	Parallel Load

Required Instruments:

No.	Name of Instruments	Quantity
1.	IC-7474	2
2.	IC-74153	2
3.	1 bit Input Pin	6
4.	2 bit Input Pin	1
5.	1 bit Output Pin	4
6.	Clock Pulse	1
7.	Wires	A lot

Circuit Diagram:



Observation:

We need four 4x1-MUXs, four D-flip flops and a clock in order to make a 4-bit universal shift register. We can build an n-bit universal shift register using the same configuration. For n-bit shift register, we will need, n 4x1-MUXs and n D-flip flops and a clock.

In n-bit shift register, the 0^{th} input of MUX_i will be A_i. The 1^{st} input of MUX_i will be A_{i+1} and the input right shift will be connected with 1^{st} input $(n-1)^{th}$ MUX. The 2^{nd} input of MUX_i will be A_{i-1} and the input left shift will be connected with 2^{nd} input of 0^{th} MUX. I_i input will be connected with 3^{rd} input of MUX_i. The output of MUX_i will be input of D_i. The i^{th} output of register A_i will be output Q_i of i^{th} D-flipflop.