DLPC350 Programmer’s Guide

User's Guide

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About This Manual

This document specifies the command and control interface to the 0.45 WXGA chipset. It also defines all applicable commands, default settings, and control register bit definitions to communicate with the 0.45 WXGA chipset.

Related Documents from Texas Instruments

- DLP 0.45 WXGA Chipset: DLP 0.45 WXGA Chipset Data Manual, DLPU009
- DLPC350 Data Sheet: DLP Digital Controller for DLP4500 DMD, DLPS029
- DLP4500 Data Sheet: DLP 0.45 WXGA DMD, DLPS028

If You Need Assistance

See the DLP and MEMS TI E2E Community support forums.

Interface Protocol

This chapter describes the interface protocol between the DLPC350 and a host processor. The DLPC350 supports two host interface protocols: I²C and USB 1.1 slave interfaces.

1.1 I²C Interface

The DLPC350 controller uses the I²C protocol to exchange commands and data with a host processor. The I²C protocol is a two-wire serial data bus that conforms to the NXP I²C specification, up to 400 kHz. One wire, SCL, serves as a serial clock, while the second wire, SDA, serves as serial data. Several different devices can be connected together in an I²C bus. Each device is software addressable by a unique address. Communication between devices occurs in a simple master-to-slave relationship.

1.1.1 I²C Transaction Structure

All I²C transactions are composed of a number of bytes, combined in the following order:

START Condition, Slave Address Byte + R/W Bit, Sub-Address Byte, N-Data Bytes, STOP Condition

where N in "N-Data Bytes" varies based on the sub-address.

1.1.1.1 I²C START Condition

All I²C transactions begin with a START condition. A START condition is defined by a high to low transition on the SDA line, while the SCL line is high.

1.1.1.2 DLPC350 Slave Address

The DLPC350 offers two different slave addresses. The I2C_ADDR_SEL pin of the DLPC350 provides the ability to select an alternate set of 7-bit I²C slave addresses. If the I2C_ADDR_SEL pin is low, then the DLPC350 slave address is 0x1A. If the I2C_ADDR_SEL pin is high, then the DLPC350 slave address is 0x1C. Because the first 8-bit I²C packet includes the 7-bit slave address followed by a read (high) or write (low) bit, a read command to the DLPC350 concatenates the slave address with a 0. A write command to the DLPC350 concatenates the slave address with a 1. Thus, when I2C_ADDR_SEL is low, the DLPC350 first byte packet of an I²C command is 0x34 for write and 0x35 for read. When I2C_ADDR_SEL is high, the DLPC350 first byte packet of an I²C command is 0x3A for write and 0x3B for read.

1.1.1.3 DLPC350 Sub-Address and Data Bytes

The DLPC350 sub-address corresponds to the byte address of the DLPC350 registers described in Appendix A. Each register address requires a certain number of data bytes, typically four. Thus, a register address is followed by variable length data. These bytes contain the value read or written into this register, with the most significant byte first.

1.1.1.4 I²C STOP Condition

All I²C transactions end with a STOP condition. A STOP condition is defined by a low to high transition on the SDA line while the SCL line is high.

1.1.2 I²C Read Transaction Sequence

To issue a command to read a DLPC350 value, the host must perform the following steps:

1. Host sends a START condition (depicted as S in Figure 1-1) followed by the DLPC350 address with the read/write bit cleared (0x34 or 0x3A).
2. Host sends a sub-address byte that contains the command of the desired DLPC350 function.
3. Host sends a STOP (depicted as P in Figure 1-1) condition.
4. Host sends another I²C START condition followed by the DLPC350 address with the read/write bit set (0x35 or 0x3B).
5. Host reads a status byte and checks that bit zero is set. If bit zero is not set, the read transaction is repeated until bit zero is set. If bit one is also set, an error occurred. Successful command requests will only have bit zero set.
6. Host reads the necessary bytes for each command.
7. Host issues a STOP condition to terminate the command read access.

1.1.2.1 Example Read Transaction Sequence

An example of a host reading DLPC350's register 4h whose contents are 00000000h would follow this sequence:

S 34 04 P

S 35 01 00 00 00 00 P

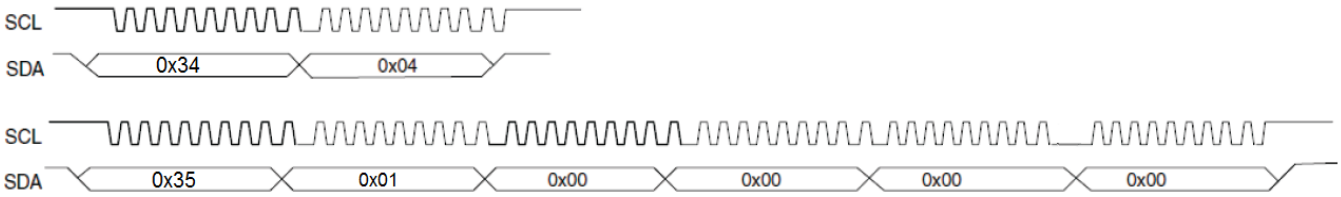

Figure 1-1. I²C Read Register Sequence

1.1.3 I²C Write Transaction Sequence

To issue a command to set a DLPC350 value, the host must perform the following steps:

1. Host sends a START condition (depicted as S in Figure 1-2) followed by the DLPC350 address with the read/write bit cleared (0x34 or 0x3A).
2. Host sends a sub-address byte that contains the command of the desired DLPC350 function.
3. Host sends the necessary bytes for the desired DLPC350 function.
4. Host issues a STOP condition (depicted as P in Figure 1-2) to terminate the command write access.

1.1.3.1 Example Write Transaction Sequence

An example of a host writing DLPC350's register 4h with the content 00000000h would follow this sequence:

S 34 04 00 00 00 00 P

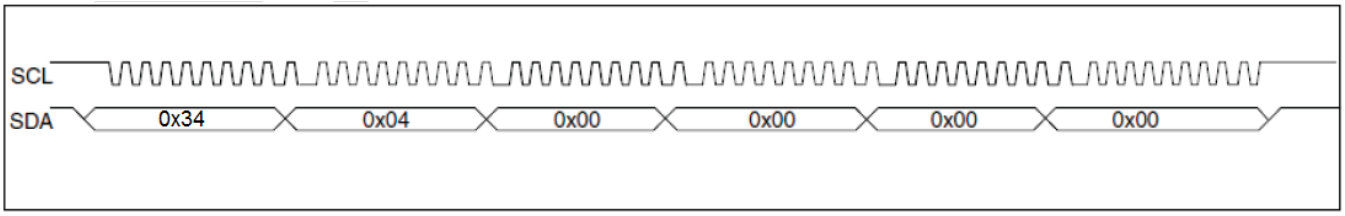

Figure 1-2. I²C Write Register Sequence

1.2 USB Interface

The DLPC350 controller also supports the USB 1.1 Human Interface Device (HID) to exchange commands and data with a host processor. The USB commands are variable length data packets that are sent with the least significant byte first. The DLPC350 offers two different serial numbers for USB enumeration based on whether the I2C_ADDR_SEL pin is high or low.

1.2.1 USB Transaction Sequence

The USB 1.1 HID protocol has the following structure:

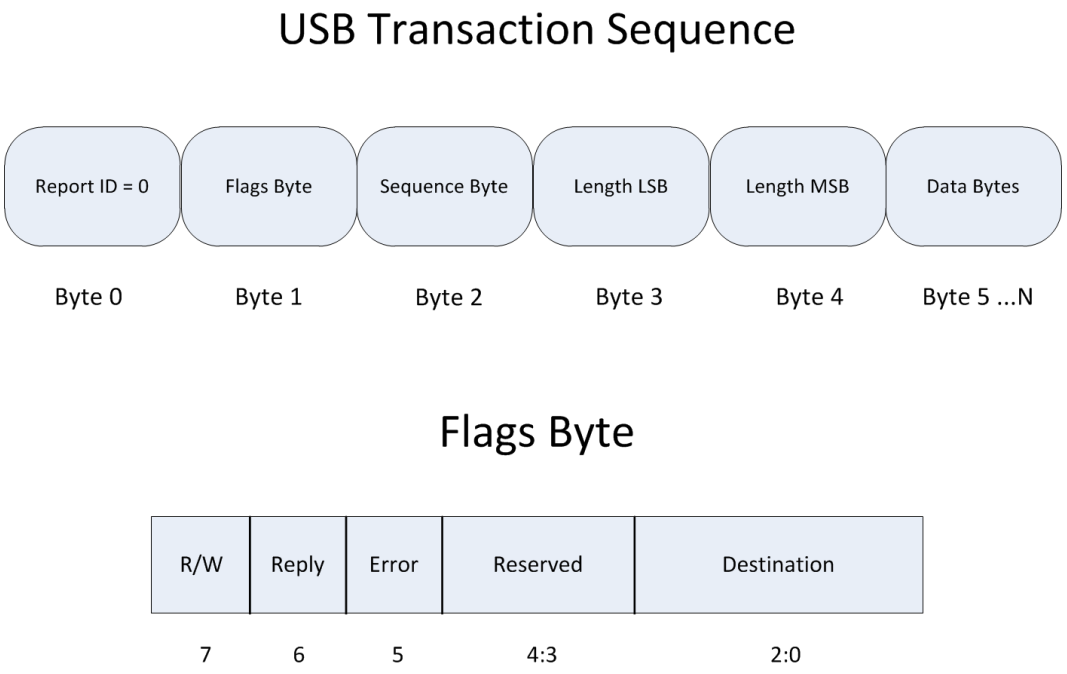

Figure 1-3. USB HID Protocol

1.2.2 USB Read Transaction Sequence

To issue a command to request a DLPC350 value, the host must perform the following steps:

1. Host sends the Report ID byte, which is set to 0.
2. Host sends the Flags byte, where
   - bits 2:0 are set to 0x0 for regular DLPC350 operation, and 0x7 for debugging assistance
   - bit 6 is set to 0x1 to indicate the host wants a reply from the device
   - bit 7 is set to 0x1 to indicate a read transaction
3. Host sends the Sequence byte. When a single command is more than 64 bytes, it is sent as multiple USB packets and the sequence byte is used to number the packets so the device can assemble them in the right sequence. In other cases, this value is irrelevant and generally set to zero.
4. Host sends two bytes with the length of the data packet. This length denotes the number of data bytes in the packet and excludes the number of bytes in steps 1-4. It denotes the total number of bytes sent in steps 5 (command bytes) and 6 (data bytes).
5. Host sends two sub-command bytes: CMD2 and CMD3.
6. Host sends data appropriate to command.
7. After completion of this command, DLPC350 responds with a packet that includes:

   (a) Byte with the command requested by the host (the matching Sequence byte).

   (b) Length of the data packet.

(c) Data requested.

1.2.3 USB Write Transaction Sequence

To issue a command to set a DLPC350 value, the host must perform the following steps:

1. Host sends the Report ID byte, which is set to 0.
2. Host sends the Flags byte, where
   - bits 2:0 are set to 0x0 for regular DLPC350 operation, and 0x7 for debugging assistance
   - bit 6 is set to 0x1 to indicate the host wants a reply from the device. This bit needs to be set for write transactions only if an acknowledgment or reply is needed, which is usually not required.
   - bit 7 is set to 0x1 to indicate a read transaction
3. Host sends the Sequence byte. When a single command is more than 64 bytes, it is sent as multiple USB packets and the sequence byte is used to number the packets so the device can assemble them in the right sequence. In other cases, this value is irrelevant and generally set to zero.
4. Host sends two bytes with the length of the data packet. This length denotes the number of data bytes in the packet and excludes the number of bytes in steps 1-4. It denotes the total number of bytes sent in steps 5 (command bytes) and 6 (data bytes).
5. Host sends two sub-command bytes: CMD2 and CMD3.
6. Host sends data appropriate to command.
7. After completion of this command, DLPC350 responds with a packet that includes a byte with the command requested by the host. This occurs only if bit 6 was set in the Flags byte.

DLPC350 Control Commands

This chapter lists the DLPC350 control commands.

The following sections list the supported control commands of the DLPC350. In the *Type* column, 'wr' type is writeable field through I^2C or USB write transactions. Data can also be read through I^2C or USB read transactions for 'wr' type bits. Type *r* is read-only. Write transactions to read-only fields are ignored.

The Reset column in all of the following command tables is the default value after power up. These values may be overwritten after power up.

NOTE: **Reserved bits and registers.** When writing to valid command bit fields, all bits marked as unused or reserved should be set to zero unless specified otherwise.

NOTE: **Momentary Image Corruption During Command Writes**. Certain commands may cause brief visual artifacts in the display image under some circumstances. Command data values may always be read without impacting displayed image. To avoid momentary corruption of image due to a command, disable the LEDs prior to the command write, then reenable the LEDs after all commands have been issued.

2.1 DLPC350 Status Commands

The DLPC350 has the following set of status commands:

- Hardware Status
- System Status
- Main Status
- Retrieve Firmware Version

2.1.1 Hardware Status

(**I^2C**: 0x20)

(**USB**: CMD2: 0x1A, CMD3: 0x0A)

The Hardware Status command provides status information on the DLPC350's sequencer, DMD controller and initialization.

Table 2-1. Hardware Status Register

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Internal Initialization 0 = Error 1 = Successful	b1	r
	1	Reserved	b0	r
	2	DMD Reset Controller Error 0 = No error has occurred 1 = Multiple overlapping bias/reset operations are accessing the same DMD block.	b0	r
	3	Forced Swap Error 0 = No error has occurred. 1 = Forced Swap Error occurred.	b0	r
	4	Reserved	b0	r
	5	Reserved	b0	r
	6	Sequencer Abort Status Flag 0 = No error has occurred 1 = Sequencer has detected an error condition that caused an abort	b0	r
	7	Sequencer Error 0 = No error has occurred. 1 = Sequencer detected an error.	b0	r

2.1.2 System Status

(**I²C**: 0x21)

(**USB**: CMD2: 0x1A, CMD3: 0x0B)

The System Status command provides DLPC350 status on internal memory tests.

Table 2-2. System Status Register

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Internal Memory Test 0 = Internal Memory Test failed 1 = Internal Memory Test passed	b1	r
	1:7	Reserved	b0	r

2.1.3 Main Status

(**I²C**: 0x22)

(**USB**: CMD2: 0x1A, CMD3: 0x0C)

The Main Status command provides DMD park status and DLPC350 sequencer, frame buffer, and gamma correction status.

Table 2-3. Main Status Register

BIT(S)	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	DMD Park Status 0 = DMD Micromirrors are not parked 1 = DMD Micromirrors are parked	b0	r
	1	Sequencer Run Flag 0 = Sequencer is stopped 1 = Sequencer is running normally	b0	r
	2	Frame Buffer Swap Flag 0 = Frame Buffer is not frozen 1 = Frame Buffer is frozen	b0	r
	3	Gamma Correction Function Enable 0 = Gamma Correction is disabled 1 = Gamma Correction is enabled	b0	r
	4:7	Reserved	b0	r

2.1.4 Retrieve Firmware Version

(**I²C**: 0x11)

(**USB**: CMD2: 0x02, CMD3: 0x05)

This command reads the version information of the DLPC350 firmware.

Table 2-4. Get Version Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
3:0		Application software revision:	Will match firmware version on DLP LightCrafter 4500	r
	15:0	Application software patch number		
	23:16	Application software minor revision		
	31:24	Application software major revision		
7:4		API Software revision:	x0	r
	15:0	API patch number		
	23:16	API minor revision		
	31:24	API major revision		
11:8		SW configuration revision:	x0	r
	15:0	SW configuration patch number		
	23:16	SW configuration minor revision		
	31:24	SW configuration major revision		
15:12		Sequencer configuration revision:	x0	r
	15:0	Sequencer configuration patch number		
	23:16	Sequencer configuration minor revision		
	31:24	Sequencer configuration major revision		

2.2 DLPC350 Programming Commands

The Programming commands manage downloading a new firmware image into flash memory. This can be done with I²C or USB communication.

2.2.1 Read Status

(**I²C**: 0x23)

(**USB**: CMD2: 0x00, CMD3: 0x00)

This command indicates if the flash is ready to be programmed and also if a flash operation is in progress.

Table 2-5. Read Status Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	2:0	Reserved	d0	r
	3	Busy Bit 0 = No flash operation in progress 1 = Flash operation in progress		
	6:4	Reserved		
	7	Programming Mode Bit 0 = Does not allow flash programming operations 1 = Allows flash programming operations		

2.2.2 Enter Program Mode

(**I²C**: 0x30)

(**USB**: CMD2: 0x30, CMD3: 0x01)

This command tells the controller to enter its programming mode and jump to the boot loader. If the boot loader receives this command, then the command has no effect.

Table 2-6. Enter Program Mode Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Program Mode 0 = Enter Program Mode - Jump to boot loader	d0	w
	7:1	Reserved		

2.2.2.1 Exit Program Mode

(**I²C**: 0x30)

(**USB**: CMD2: 0x00, CMD3: 0x30)

This command tells the controller to exit its programming mode. If the application receives the exit command, the command has no effect.

Table 2-7. Exit Program Mode Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Program Mode 1 = Exit Program Mode - Reset controller and run application	d0	w
	7:1	Reserved		

2.2.3 Read Control

(**I²C**: 0x15)

(**USB**: CMD2: 0x00, CMD3: 0x15)

This command reads the Flash Manufacturer and Device IDs, as well as the Checksum, after the Calculate Checksum command has been executed.

Table 2-8. Query Flash IDs Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	3:0	ID 0 = Returns Checksum C = Requests Flash Manufacturer ID D = Requests Flash Device ID	d0	r
	7:4	Reserved		

2.2.4 Start Address

(**I²C**: 0x29)

(**USB**: CMD2: 0x00, CMD3: 0x29)

The Start Address command specifies the start address for the next flash download. It is the responsibility of the user to ensure that the Start Address is on a sector boundary in the current flash device. This command should be followed by a Flash Data Size command and a Flash Erase command to completely describe the programming operation.

The start address is also used in specifying the start of a checksum operation

Table 2-9. Start Address Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
3:0	32:0	Flash address. Byte 0 is LSB, byte 3 is MSB.	x0	w

2.2.5 Erase Sector

(**I²C**: 0x28)

(**USB**: CMD2: 0x00, CMD3: 0x28)

This is a system write command to erase a sector of flash memory. This command should not be executed until valid data has been written to the Flash Start Address. Users are responsible for ensuring that a valid address has been written. The Busy bit will be set in the Boot Loader status byte while the sector erase is in progress.

Note: TI cautions against erasing the boot sector of the device as this contains key initialization parameters and the flash programming functionality. Only the sector that contains the start address will be erased, not all sectors from the start address to the end of the device. Users must either pre-erase all sectors to be programmed, or erase and program each sector individually.

2.2.6 Download Data Size

(**I²C**: 0x2C)

(**USB**: CMD2: 0x00, CMD3: 0x2C)

System write command to specify the size of the following flash download. The data size is sent to tell the Boot Loader how many bytes to expect to program into the flash device during the current operation. It is also used for specifying the checksum range when requesting that operation.

Table 2-10. Download Data Size Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
3:0	32:0	Flash address. Byte 0 is LSB, byte 3 is MSB.	x0	w

2.2.7 Download Data

(**I²C**: 0x25)

(**USB**: CMD2: 0x00, CMD3: 0x25)

This command contains the flash data to be programmed. The maximum data size which can be sent in each command is 512 bytes, which corresponds to a data length of 514. The number of bytes downloaded by consecutive download data commands must match the predefined Flash Data Size for the operation to be successful.

Table 2-11. Download Data Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Length LSB	x0	w
1	7:0	Length MSB		
513:2	4095:0	Up to 512 Data Bytes		
514	7:0	Checksum		

2.2.8 Calculate Checksum

(**I²C**: 0x26)

(**USB**: CMD2: 0x00, CMD3: 0x26)

This command calculates the checksum. Executing this command causes the Boot Loader to read the data in the flash memory and calculate a 4-byte 8-bit checksum. The Busy bit will be set in the Boot Loader status byte while the checksum computation is in progress. After completion, the 4-byte checksum can be read back via the Return Checksum command. The data range to be summed is specified by writing appropriate data with the Flash Start Address and Flash Data Size commands.

2.3 Chipset Control Commands

The DLPC350 has the following set of control commands:

- Chipset configuration and control
- Parallel interface configuration and control
- Input source control
- Image rotation and flip control
- Image processing control
- LED driver control
- Sleep mode control
- GPIO control
- DLP display sequence control

I²C control commands are accepted in any order, except when special sequencing is required (for example, setting up the flash). Each control command is validated for sub-address and parameter errors as it is received. Commands failing validation are ignored. On power up, it is necessary to wait for DLPC350 to complete its initialization before sending it any I²C or USB transactions. The INIT_DONE pin signals when initialization is complete (see the DLPC350 Data Sheet).

2.3.1 Chipset Configuration and Control Commands

The Chipset and Configuration Control commands manage software reset, power down modes, buffer freeze, and image curtain display.

2.3.1.1 Software Reset

(**I²C**: 0x13)

(**USB**: CMD2: 0x08, CMD3: 0x02)

This command issues a software reset to the DLPC350, regardless of the argument sent. This command provides a back-up recovery mechanism.

Table 2-12. Software Reset Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Software Reset. A set or reset of this bit will perform a software reset: 0 – No Software Reset 1 – Perform a Software Reset	d0	w

2.3.1.2 Power Control

(**I²C**: 0x07)

(**USB**: CMD2: 0x02, CMD3: 0x00)

The Power Control places the DLPC350 in a low-power state and powers down the DMD interface. Standby mode should only be enabled after all data for the last frame to be displayed has been transferred to the DLPC350. Standby mode must be disabled prior to sending any new data. After executing this command, poll the system status using I²C commands: 0x20, x21, and 0x22 or USB commands: 0x1A0A, 0x1A0B, and 0x1A0C.

Table 2-13. Interface Sleep Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	1:0	Power Control 0 = Normal operation. The selected external source will be displayed 1 = Standby mode. Places DLPC350 in low power state and powers down the DMD interface	d0	wr
	7:2	Reserved	d0	r

2.3.1.3 Buffer Controls

The buffer control commands allow buffer swaps, provide the current buffer pointer, and freeze the buffer.

2.3.1.3.1 Force Buffer Swap

(**I²C**: 0x71)

(**USB**: CMD2: 0x1A, CMD3: 0x26)

The Force Buffer Swap command switches between the two internal memory buffers by swapping the read and write pointers. After a buffer swap, the 24 bit-plane buffer that was streaming data to the DMD is now used for input, while the previous 24 bit-plane input buffer, now streams data to the DMD. The buffer should be frozen before executing this command.

Table 2-14. Force Buffer Swap Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Buffer Swap 1 - Swap internal memory buffer pointers 0 - No change to the internal memory buffer pointers	d0	wr
	7:1	Reserved	d0	r

2.3.1.3.2 Display Buffer Freeze

(**I²C**: 0x7C)

(**USB**: CMD2: 0x06, CMD3: 0x0A)

The Display Buffer Freeze command disables swapping the memory buffers. When reconfiguring the chipset through a series of commands that change the input source or operating mode, the Display Buffer Swap Freeze command is recommended to prevent temporary artifacts from reaching the display. When the display buffer is frozen, the last image streamed to the DMD continues to be displayed.

Table 2-15. Display Buffer Freeze Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Display Buffer Swap Freeze 0 - Enable Buffer Swapping 1 - Disable Buffer Swapping (freeze display buffer)	d1	wr

2.3.1.3.3 Buffer Write Disable

(**I²C**: 0x72)

(**USB**: CMD2: 0x1A, CMD3: 0x27)

The Buffer Write Disable command prevents the overwriting of the contents of the 48 bit-planes of the internal memory buffer.

Table 2-16. Buffer Write Disable Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Buffer Write Disable 1 = Disables writes to all the internal memory buffer 0 = Normal operation	d0	wr
	7:1	Reserved	d0	r

2.3.1.3.4 Current Read Buffer Pointer

(**I²C**: 0x73)

(**USB**: CMD2: 0x1A, CMD3: 0x28)

The Current Read Buffer Pointer command returns the pointer to the current internal memory buffer whose data is streamed to the DMD.

Table 2-17. Current Buffer Pointer Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Current Read Buffer Pointer Command 1 = Buffer #1 is streaming to DMD 0 = Buffer #0 is streaming to DMD	d0	wr
	7:1	Reserved	d0	r

2.3.1.4 Display Curtain Control

(**I²C**: 0x06)

(**USB**: CMD2: 0x11, CMD3: 0x00)

This register provides image curtain control. When enabled and the input source is set to external video with no video source connected, a solid color field is displayed on the entire DMD display. The Display Curtain Control provides an alternate method of masking temporary source corruption from reaching the display due to on-the-fly reconfiguration. It is also useful for optical test and debug support.

Table 2-18. Display Curtain Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
1:0	9:0	Red color intensity in a scale from 0 to 1023	x0	wr
3:2	9:0	Green color intensity in a scale from 0 to 1023	x0	wr
5:4	9:0	Blue color intensity in a scale from 0 to 1023	x0	wr

2.3.2 Interface Configuration and Control

The Interface Configuration and Control manage the operation of the parallel and FPD-link interfaces.

2.3.2.1 Input Data Channel Swap

(**I²C**: 0x04)

(**USB**: CMD2: 0x1A, CMD3: 0x37)

The Input Data Channel Swap commands configure the specified input data port and map the data sub-channels. The DLPC350 interprets Channel A as Green, Channel B as Red, and Channel C as Blue.

Table 2-19. Input Data Channel Swap Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	2:0	Swap Parallel Interface Data Sub-Channel: 0 - ABC = ABC, No swapping of data sub-channels 1 - ABC = CAB, Data sub-channels are right shifted and circularly rotated 2 - ABC = BCA, Data sub-channels are left shifted and circularly rotated 3 - ABC = ACB, Data sub-channels B and C are swapped 4 - ABC = BAC, Data sub-channels A and B are swapped 5 - ABC = CBA, Data sub-channels A and C are swapped 6 - Reserved 7 - Reserved	x4	wr
	6:3	Reserved	b0	r
	7	Specified Port 0 - Parallel Interface 1 - FPD-link interface	b0	wr

2.3.3 FPD-Link Interface Configuration and Control

The following commands are unique to the FPD-link interface.

2.3.3.1 FPD-Link Mode and Field Select

(**I²C**: 0x05)

(**USB**: CMD2: 0x1A, CMD3: 0x04)

The FPD-Link Mode and Field Select command configures the FPD-link pixel map, polarity, and signal select.

Table 2-20. FPD-Link Mode and Field Select Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	2:0	Field Signal Select: 0 = Map FPD-Link output from CONT1 onto Field Signal for FPD-link interface port 1 = Map FPD-Link output from CONT2 onto Field Signal for FPD-link interface port 2 = Force 0 onto Field Signal for FPD-link interface port 3 = Reserved	x0	wr
	3	Swap Polarity	x1	wr
	5:4	Reserved	x0	r
	7:6	FPD-link Pixel Mapping Mode (see Table 2-21) 0 = Mode 1 1 =Mode 2 2 = Mode 3 3 =Mode 4	x1	wr

Table 2-21. FPD-Link Pixel Mapping Modes

PIXEL	MODE1	MODE2	MODE3	MODE4
Green[9]	RDB4	RDD3	RDE1	RDB4
Green[8]	RDB3	RDD2	RDE2	RDB3
Green[7]	RDB2	RDB4	RDD1	RDB2
Green[6]	RDB1	RDB3	RDD2	RDB1
Green[5]	RDB0	RDB2	RDB4	RDB0
Green[4]	RDA6	RDB1	RDB3	RDA6
Green[3]	RDD3	RDB0	RDB2	0
Green[2]	RDD2	RDA6	RDB1	0
Green[1]	RDE3	RDE3	RDB0	0
Green[0]	RDE2	RDE2	RDA6	0
Red[9]	RDA5	RDD1	RDE1	RDA5
Red[8]	RDA4	RDD0	RDE0	RDA4
Red[7]	RDA3	RDA5	RDD1	RDA3
Red[6]	RDA2	RDA4	RDD0	RDA2
Red[5]	RDA1	RDA3	RDA5	RDA1
Red[4]	RDA0	RDA2	RDA4	RDA0
Red[3]	RDD1	RDA1	RDA3	0
Red[2]	RDD0	RDA0	RDA2	0
Red[1]	RDE1	RDE1	RDA1	0
Red[0]	RDE0	RDE0	RDA0	0
Blue[9]	RDC3	RDD5	RDE5	RDC3
Blue[8]	RDC2	RDD4	RDE4	RDC2
Blue[7]	RDC1	RDC3	RDD5	RDC1
Blue[6]	RDC0	RDC2	RDD4	RDC0
Blue[5]	RDB6	RDC1	RDC3	RDB6
Blue[4]	RDB5	RDC0	RDC2	RDB5
Blue[3]	RDD5	RDB6	RDC1	0
Blue[2]	RDD4	RDB5	RDC0	0
Blue[1]	RDE5	RDE5	RDB6	0
Blue[0]	RDE4	RDE4	RDB5	0

Table 2-21. FPD-Link Pixel Mapping Modes (continued)

PIXEL	MODE1	MODE2	MODE3	MODE4
DATA_EN	RDC6	RDC6	RDC6	RDC6
VSYNC	RDC5	RDC5	RDC5	RDC5
HSYNC	RDC4	RDC4	RDC4	RDC4
CONT1	RDD6	RDD6	RDD6	RDD6
CONT2	RDE6	RDE6	RDE6	RDE6

2.3.4 Input Source Control

The Input Source Selection determines the input source for the DLPC350 data display.

2.3.4.1 Port Clock Select

(**I²C**: 0x03)

(**USB**: CMD2: 0x1A, CMD3: 0x03)

This command selects the Port 1 clock for the parallel interface. For the FPD-Link, the Port Clock is automatically set to Port 2.

Table 2-22. Input Source Selection Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	2:0	Select Port Input Clock 0: Port 1, Clock A 1: Port 1, Clock B 2: Port 1, Clock C	x0	wr
	7:3	Reserved	x0	r

2.3.4.2 Input Source Selection

(**I²C**: 0x00)

(**USB**: CMD2: 0x1A, CMD3: 0x00)

The Input Source Selection command selects the input source to be displayed by the DLPC350: 30-bit Parallel Port, Internal Test Pattern, Flash memory, or FPD-link interface. After executing this command, poll the system status using I²C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0b, and 0x1A0C.

Table 2-23. Input Source Selection Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	2:0	Select the input source and interface mode: 0 = Parallel interface with 8-bit, 16-bit, 20-bit, 24-bit, or 30-bit RGB or YCrCb data formats 1 = Internal test pattern; I²C command 0x11 is used to select the test pattern type. 2 = Flash. Images are 24-bit single-frame, still images stored in flash that are uploaded on command. 3 = FPD-link interface	x0	wr
	5:3	Parallel Interface bit depth 0 = 30-bits 1 = 24-bits 2 = 20-bits 3 = 16-bits 4 = 10-bits 5 = 8-bits	x1	wr
	7:6	Reserved	x0	r

2.3.4.3 Input Pixel Data Format

(**I²C**: 0x02)

(**USB**: CMD2: 0x1A, CMD3: 0x02)

The Input Pixel Data Format command defines the pixel data format input into the DLPC350.

Table 2-24. Input Pixel Data Format Command

BYTE	BIT(S)	DESCRIPTION					RESET	TYPE
0	3:0	Select the pixel data format: Supported Pixel Formats vs Source Type					d0	wr
			Parallel	Test Pattern	Flash Image	FPD-Link		
		0 - RGB 4:4:4 (30-bit)	Yes	Yes	Yes	Yes		
		1 - YCrCb 4:4:4 (30-bit)	Yes	No	No	No		
		2 - YCrCb 4:2:2	Yes	No	Yes	No		
	7:6	Reserved					x0	r

2.3.4.4 Internal Test Patterns Select

(**I²C**: 0x0A)

(**USB**: CMD2: 0x12, CMD3: 0x03)

When the internal test pattern is the selected input, the Internal Test Patterns Select defines the test pattern displayed on the screen. These test patterns are internally generated and injected into the beginning of the DLPC350 image processing path. Therefore, all image processing is performed on the test images. All command registers should be set up as if the test images are input from an RGB 8:8:8 external source. The resolution of the Test Pattern should be configured with the Input Display Resolutions commands. Frame Rate should be configured with the Frame Rate commands.

Table 2-25. Internal Test Patterns Select Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	3:0	Internal Test Patterns Select: 0x0 = Solid Field 0x1 = Horizontal Ramp 0x2 = Vertical Ramp 0x3 = Horizontal Lines 0x4 = Diagonal Lines 0x5 = Vertical Lines 0x6 = Grid 0x7 = Checkerboard 0x8 = RGB Ramp 0x9 = Color Bars 0xA = Step Bars	x8	wr
	7:4	Reserved		

2.3.4.5 Internal Test Patterns Color Control

(**I²C**: 0x1A)

(**USB**: CMD2: 0x12, CMD3: 0x04)

When the internal test pattern is the selected input, the Internal Test Patterns Color Control defines the colors of the test pattern displayed on the screen. These test patterns are internally generated and injected into the beginning of the DLPC350 image processing path. Therefore, all image processing is performed on the test images. All command registers should be set up as if the test images are input from an RGB 8:8:8 external source. The foreground color setting affects all test patterns. The background color setting affects those test patterns that have a foreground and background component, such as, Horizontal Lines, Diagonal Lines, Vertical Lines, Grid, and Checkerboard.

Table 2-26. Internal Test Patterns Color Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
1:0	9:0	Red Foreground Color intensity in a scale from 0 to 1023 0x0 = No Red Foreground color intensity ... 0x3FF = Full Red Foreground color intensity	x3FF	wr
3:2	9:0	Green Foreground Color intensity in a scale from 0 to 1023 0x0 = No Green Foreground color intensity ... 0x3FF = Full Green Foreground color intensity	x3FF	wr
5:4	9:0	Blue Foreground Color intensity in a scale from 0 to 1023 0x0 =No Blue Foreground color intensity ... 0x3FF = Full Blue Foreground color intensity	x3FF	wr
7:6	9:0	Red Background Color intensity in a scale from 0 to 1023 0x0 = No Red Background color intensity ... 0x3FF = Full Red Background color intensity	x0	wr
9:8	9:0	Green Background Color intensity in a scale from 0 to 1023 0x0 = No Green Background color intensity ... 0x3FF = Full Green Background color intensity	x0	wr

Table 2-26. Internal Test Patterns Color Control Command (continued)

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
11:10	9:0	Blue Background Color intensity in a scale from 0 to 1023 0x0 = No Blue Background color intensity ... 0x3FF = Full Blue Background color intensity	x0	wr

2.3.4.6 Load Image

(**I²C**: 0x7F)

(**USB**: CMD2: 0x1A, CMD3: 0x39)

This command loads an image from flash memory and then performs a buffer swap to display the loaded image on the DMD. After executing this command, poll the system status using I²C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C.

Table 2-27. Load Image Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Image Index. Loads the image at this index. Reading this back provides the index that was loaded most recently via this command.	x0	wr

2.3.4.7 Image Load Timing

(**I²C**: 0x61)

(**USB**: 0x02/0x04, CMD2: 0x1A, CMD3: 0x3A)

When this command is executed, the system will load the image index mentioned in Section 2.3.4.6 and collect the amount of time it took to load that image. The busy status of the system will be high until the images have been loaded and the timing information is collected. This command cannot be executed while the system is already displaying patterns from flash. After executing this command, poll the system status using I²C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C.

Table 2-28. Image Load Timing Write Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Starting index of the image for which the timing information is required	x0	w
1	7:0	Number of images for which the timing information is required	x0	w

When reading back the load timing information, the following data format will be received:

Table 2-29. Image Load Timing Read Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
3:0	31:0	Time taken for image load. Divide this value by 18667 to get the time in milliseconds.	x0	r

2.3.5 Image Flip

The DLPC350 supports long and short axis image flips to support rear-, and front-projection, as well as, table and ceiling mounted projection.

2.3.5.1 Long Axis Image Flip:

(**I²C**: 0x08)

(**USB**: CMD2: 0x10, CMD3: 0x08)

The Long-Axis Image Flip defines whether the input image is flipped across the long axis of the DMD. If this parameter is changed while displaying a still image, the input still image should be re-sent. If the image is not re-sent, the output image might be slightly corrupted. Figure 2-1 shows an example of a long axis image flip. In Structured Light mode, the image flip will take effect on the next bit-plane, image, or video frame load.

Table 2-30. Long Axis Image Flip Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Flips image along the long side of the DMD: 0 = Disable flip 1 = Enable flip	d0	wr
	7:1	Reserved	d0	r

Figure 2-1. Image Long-Axis Flip Example

2.3.5.2 Short Axis Image Flip

(**I²C**: 0x09)

(**USB**: CMD2: 0x10, CMD3: 0x09)

The Short-Axis Image Flip defines whether the input image is flipped across the short axis of the DMD. If this parameter is changed while displaying a still image, the input still image should be resent. If the image is not re-sent, the output image might be slightly corrupted. Figure 2-2 shows an example of a short axis image flip. In Structured Light mode, the image flip will take effect on the next bit-plane, image, or video frame load.

Table 2-31. Short Axis Image Flip Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Flips image along the short side of the DMD: 0 - Disable flip 1 - Enable flip	d0	wr
	7:1	Reserved	d0	r

Figure 2-2. Image Short-Axis Flip Example

2.3.6 Image Processing Control

2.3.6.1 Color Space Conversion

(**I²C**: 0x26)

(**USB**: CMD2: 0x1A, CMD3: 0x0D)

The Color Space Conversion (CSC) command specifies the color matrix used to translate the input data to RGB data or to color correct the RGB input data. The Color Space Converter contains one color space matrix with nine elements. All nine command bytes must be sent as one contiguous block to ensure that all the coefficient values are updated simultaneously.

Table 2-32. Color Space Conversion Command

BYTE	BIT(S)	DESCRIPTION	RESET			TYPE
0	1:0	Attributes of input source: 0 - RGB 4:4:4 1 - YCrCb 4:4:4 2 - YCrCb 4:2:2	d0			wr
	7:2	Reserved	d0			r
			RGB 4:4:4	YCrCb 4:4:4	YCrCb 4:2:2	
1	12:0	CSC Coefficient 1	x0400	x04A8	x04A8	wr
2	12:0	CSC Coefficient 2	x0000	xFDC7	xFCC0	wr
3	12:0	CSC Coefficient 3	x0000	xFF26	xFE6F	wr
4	12:0	CSC Coefficient 4	x0000	x04A8	x04A8	wr
5	12:0	CSC Coefficient 5	x0400	x0715	x0662	wr
6	12:0	CSC Coefficient 6	x0000	x0000	x0000	wr
7	12:0	CSC Coefficient 7	x0000	x04A8	x04A8	wr
8	12:0	CSC Coefficient 8	x0000	x0000	x0000	wr
9	12:0	CSC Coefficient 9	x0400	x0875	x0812	wr

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} C1 & C2 & C3 \\ C4 & C5 & C6 \\ C7 & C8 & C9 \end{bmatrix} \begin{bmatrix} A \\ B \\ C \end{bmatrix}$$

Figure 2-3. Color Space Conversion Matrix

All programmable CSC coefficient values represent numbers less than +4 but greater than or equal to -4. The CSC coefficient values are 13-bit signed 2's complement numbers with the binary point between bits 9 and 10 (s2.10 format).

Table 2-33. Color Space Conversion Coefficient Format

Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sign	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

2.3.7 LED Driver Control

LED driver operation is a function of the individual red, green and blue LED-enable software-control parameters. The recommended order for initializing LED drivers is to:

1. Program the individual red, green and blue LED driver currents.

2. Program the LED PWM polarity.
3. Enable the individual LED enable outputs.
4. Turn ON the DLP® display sequence. See Section 2.4.1.

The LED-current software-control parameters define PWM values that drive corresponding LED current. The LED enables indicate which LED will be activated.

CAUTION

Careful control of LED current is needed to prevent damage to LEDs. Follow all LED manufacturer recommendations and maintain LED current levels within recommended operating conditions. The setting of the LED current depends on many system and application parameters (including projector thermal design, LED specifications, selected display mode, etc.). Therefore, the recommended and absolute-maximum settings vary greatly.

2.3.7.1 LED Enable Outputs

(**I²C**: 0x10)

(**USB**: CMD2: 0x1A, CMD3: 0x07)

The DLPC350 offers three sets of pins to control the LED enables:

- LEDR_EN for the Red LED
- LEDG_EN for the Green LED
- LEDB_EN for the Blue LED

After reset, all LED enables are placed in the inactive state until the board initializes.

Table 2-34. LED Enable Outputs

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Red LED Enable 0 - Red LED is disabled 1 - Red LED is enabled	x0	wr
	1	Green LED Enable 0 - Green LED is disabled 1 - Green LED is enabled	x0	wr
	2	Blue LED Enable 0 - Blue LED is disabled 1 - Blue LED is enabled	x0	wr
	3	LED enable control 0 - All LED enables are controlled by bits 2:0 and ignore Sequencer control 1 - All LED enables are controlled by the Sequencer and ignore the settings in bits 2:0	x1	wr
	7:4	Reserved	x0	r

2.3.7.1.1 LED PWM Polarity

(**I²C**: 0x0B)

(**USB**: CMD2: 0x1A, CMD3: 0x05)

The LED PWM Polarity command sets the polarity of all PWM signals. This command must be issued before powering up the LED drivers.

Table 2-35. LED PWM Polarity Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	1:0	Polarity of PWM signals 0 - Normal polarity, PWM 0 value corresponds to no current while PWM 255 value corresponds to maximum current. 1 - Inverted polarity. PWM 0 value corresponds to maximum current while PWM 255 value corresponds to no current.	x0	wr
	7:2	Reserved	x0	r

2.3.7.2 LED Driver Current Control

(**I²C**: 0x4B)

(**USB**: CMD2: 0x0B, CMD3: 0x01)

This parameter controls the pulse duration of the specific LED PWM modulation output pin. The resolution is 8 bits and corresponds to a percentage of the LED current. The PWM value can be set from 0 to 100% in 256 steps . If the LED PWM polarity is set to normal polarity, a setting of 0xFF gives the maximum PWM current. The LED current is a function of the specific LED driver design.

CAUTION

Care should be taken when using this command. Improper use of this command can lead to damage to the system. The setting of the LED current depends on many system and application parameters (including projector thermal design, LED specifications, selected display mode, etc.). Therefore, recommended and absolute-maximum settings vary greatly.

Table 2-36. LED Driver Current Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Red LED PWM current control Valid range, assuming normal polarity of PWM signals, is: 0x00 (0% duty cycle → Red LED driver generates no current) to 0xFF (100% duty cycle → Red LED driver generates maximum current)) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus varies by design.	x97	wr
1	7:0	Green LED PWM current control Valid range, assuming normal polarity of PWM signals, is: 0x00 (0% duty cycle → Green LED driver generates no current) to 0xFF (100% duty cycle → Green LED driver generates maximum current)) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus varies by design.	x78	wr
2	7:0	Blue LED PWM current control Valid range, assuming normal polarity of PWM signals, is: 0x00 (0% duty cycle → Blue LED driver generates no current) to 0xFF (100% duty cycle → Blue LED driver generates maximum current)) The current level corresponding to the selected PWM duty cycle is a function of the specific LED driver design and thus varies by design.	x7D	wr

2.3.8 GPIO Control

DLPC350 offers twenty general purpose input-output pins (GPIO). Some of these pins can be configured for PWM Output, PWM input, or Clock output functionality

2.3.8.1 GPIO Configuration

(**I²C**: 0x44)

(**USB**: CMD2: 0x1A, CMD3: 0x38)

The GPIO Configuration command enables GPIO functionality on a specific set of DLPC350 pins. The command sets their direction, output buffer type, and output state.

Table 2-37. GPIO Configuration Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	GPIO selection. See Table 2-38 for description of available pins	n/a	wr
1	1:0	Reserved	x0	r
	2	Input Value 0 = Low 1 = High	x0	r
	3	Output State 0 = Drive selected GPIO pin low, if the direction is set to output 1 = Drive selected GPIO pin high, if the direction is set to output and the pin is not set to Open Drain buffer type	GPIO Dependent	wr
	4	Output Buffer Type 0 = Standard buffer (drives high or low) 1 = Open Drain buffer (drives low only)	GPIO Dependent	wr
	5	GPIO Direction 0 = Input 1 = Output	GPIO Dependent	wr
	6	Reserved	x0	r
	7	GPIO Disable 0 = Enable GPIO 1 = Disable GPIO	GPIO Dependent	wr

Table 2-38. GPIO Selection

GPIO Selection	DLPC350 GPIO Pin	Function	Alternate Function
0	GPIO_01	GPIO	PWM Output
1	Reserved		
2	GPIO_02	GPIO	PWM Output
4:3	Reserved		
5	GPIO_05	GPIO	PWM Input
6	GPIO_06	GPIO	PWM Input
9:7	Reserved		
11	GPIO_11	GPIO	Clock Out1
12	GPIO_12	GPIO	Clock Out2
13	GPIO_13	GPIO	
14	GPIO_14	GPIO	
15	GPIO_15	GPIO	
19:16	Reserved		
20	GPIO_20	GPIO	
21	GPIO_21	GPIO	

Table 2-38. GPIO Selection (continued)

GPIO Selection	DLPC350 GPIO Pin	Function	Alternate Function
23:22	Reserved		
24	GPIO_24	GPIO	
25	GPIO_25	GPIO	
26	Reserved		
27	GPIO_27	GPIO	
28	GPIO_28	GPIO	
29	GPIO_29	GPIO	
32:30	Reserved		
33	GPIO_33	GPIO	
34	GPIO_34	GPIO	
35	GPIO_35	GPIO	
36	GPIO_36	GPIO	
56:37	Reserved		

2.3.8.2 GPIO Clock Configuration

(**I²C**: 0x48)

(**USB**: CMD2: 0x08, CMD3: 0x07)

DLPC350 supports two pins with clock output capabilities: GPIO_11 and GPIO_12. The GPIO Clock Configuration command enables the clock output functionality and sets the clock frequency.

Table 2-39. GPIO Clock Configuration Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Clock Selection 0 = GPIO_11 1 = GPIO_12	n/a	wr
	7:1	Reserved	x0	r
1	0	Clock Functionality Disable 0 = Enable clock functionality on selected pin 1 = Disable clock functionality on selected pin	x0	wr
	7:1	Reserved	x0	r
2	7:0	Clock Divider. Allowed values in the range of 2 to 127. Output frequency = 96MHz / (Clock Divider) 0x0 = Reserved 0x1 = Reserved 0x2 = 2 ... 0x7F = 127 0xFF:0x80 = Reserved	x7F	wr

2.3.9 PWM Control

DLPC350 provides two general purpose Pulse Modulated Width (PWM) channels that can be used for a variety of control applications, such as fan speed. If the PWM functionality is not needed, these signals can be programmed as general purpose input-output (GPIO) pins. To enable the PWM signals:

1. Program the PWM signal using the PWM Setup command
2. Enable the PWM signal with the PWM Enable command.

2.3.9.1 PWM Setup

(**I²C**: 0x41)

(**USB**: CMD2: 0x1A, CMD3: 0x11)

The PWM Setup command sets the clock period and duty cycle of the specified PWM channel. The PWM frequency and duty cycle is derived from an internal 18.67MHz clock. To calculate the desired PWM period, divide the desired clock frequency from the internal 18.67Mhz clock. For example, a PWM frequency of 2kHz, requires a 18666667 / 2000 = 9333 or 0x2475. Thus, Byte1 is programmed to 0x24 and Byte3 is programmed to 0x75.

Table 2-40. PWM Setup Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	4:0	Reserved	x0	r
	7:5	PWM Channel Select 0 - PWM channel 0 (GPIO_0) 1 - Reserved 2 - PWM channel 2 (GPIO_2) 3-7 - Reserved	x0	wr
3:1	23:0	Clock Period in increments of 53.57ns. Clock Period = (value + 1) * 53.5ns	Channel Dependent	wr
4	6:0	Duty Cycle = (value + 1)% Value range is 1%-99%	Channel Dependent	wr
	7	Reserved	x0	r

2.3.10 PWM Enable

(**I²C**: 0x40)

(**USB**: CMD2: 0x1A, CMD3: 0x10)

After the PWM Setup command configures the clock period and duty cycle, the PWM Enable command activates the PWM signals.

Table 2-41. PWM Enable Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	2:0	PWM Channel Select 0 - PWM channel 0 (GPIO_0) 1 - Reserved 2 - PWM channel 2 (GPIO_2)	n/a	wr
	6:3	Reserved	x0	r
	7	PWM Channel Enable 0 -Disable selected PWM Channel 1 - Enable selected PWM Channel	Channel 2 Enabled Channel 0 Disabled	wr

2.3.11 PWM Capture Configuration

(**I²C**: 0x43)

(**USB**: CMD2: 0x1A, CMD3: 0x12)

The PWM Capture Configuration command samples the specified PWM input signals and returns the PWM clock period in a 4 byte packet.

Table 2-42. PWM Capture Configuration Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	PWM Capture Port 0 - PWM Input channel 0 (GPIO_5) 1 - PWM Input channel 1 (GPIO_6)	n/a	wr
	7:1	Reserved	x0	r
4:1	24:0	PWM Sample Rate (285 Hz to 18,666,667 Hz) Sample Rate = Pulse Frequency / Duty Cycle	Port Dependent	wr

2.3.12 PWM Capture Read

(**I²C**: 0x4E)

(**USB**: CMD2: 0x1A, CMD3: 0x13)

The PWM Capture Read command indicates both the number of clock cycles the signal was low and high. The PWM Capture Read command is used by sending the PWM Input channel (x00 or x01) and reading back 4 bytes of data. The first two bytes indicate how many samples were taken during a low signal, and the third and fourth bytes indicate how many samples were taken during a high signal.

Table 2-43. PWM Capture Read Values

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	PWM Capture Port 0 - PWM Input channel 0 (GPIO_5) 1 - PWM Input channel 1 (GPIO_6)	n/a	wr
	7:1	Reserved	x0	r
1:0	15:0	Low Period	n/a	r
3:2	15:0	High Period	n/a	r

2.4 Display Sequences

A DLP® display sequence consists of several parameters which dictate the loading of the DMD and the control of PWM to the LEDs. The DLPC350 supports two main sequence modes:

- Video Mode
- Pattern Display Mode

The Display Mode Selection Command (Section 2.4.1) selects between video or pattern display mode.

In video mode, the DLPC350 supports up to 1280 x 800 pixel resolution at 120 Hz through its 30-bit RGB or FPD-link interfaces. The DLPC350 processes the digital input image and converts the data into the appropriate format for the DLP4500 DMD. The DLPC350 processing functions include format conversion, chroma interpolation, and color space conversion. The DLPC350 also offers several image enhancement functions: degamma, primary color correction, chroma interpolation, scaling, and overlap color processing.

In pattern display mode, the DLPC350 provides a high speed, pixel accurate 912 x 1140 resolution that bypasses the video processing and image enhancement functions. This mode supports data input through the DLPC350 24-bit RGB or FPD-link interfaces, as well as flash memory. This functionality is well-suited for techniques such as structured light, additive manufacturing, or digital exposure. The DLPC350 also has the capability to display a set of patterns and signal a camera to capture when these patterns are displayed. Figure 2-4 shows the DLPC350 block diagram and the main functional blocks for video and pattern display mode. Table 2-44 lists the allowed pattern combinations of bit-depth, number of patterns, and maximum pattern speed.

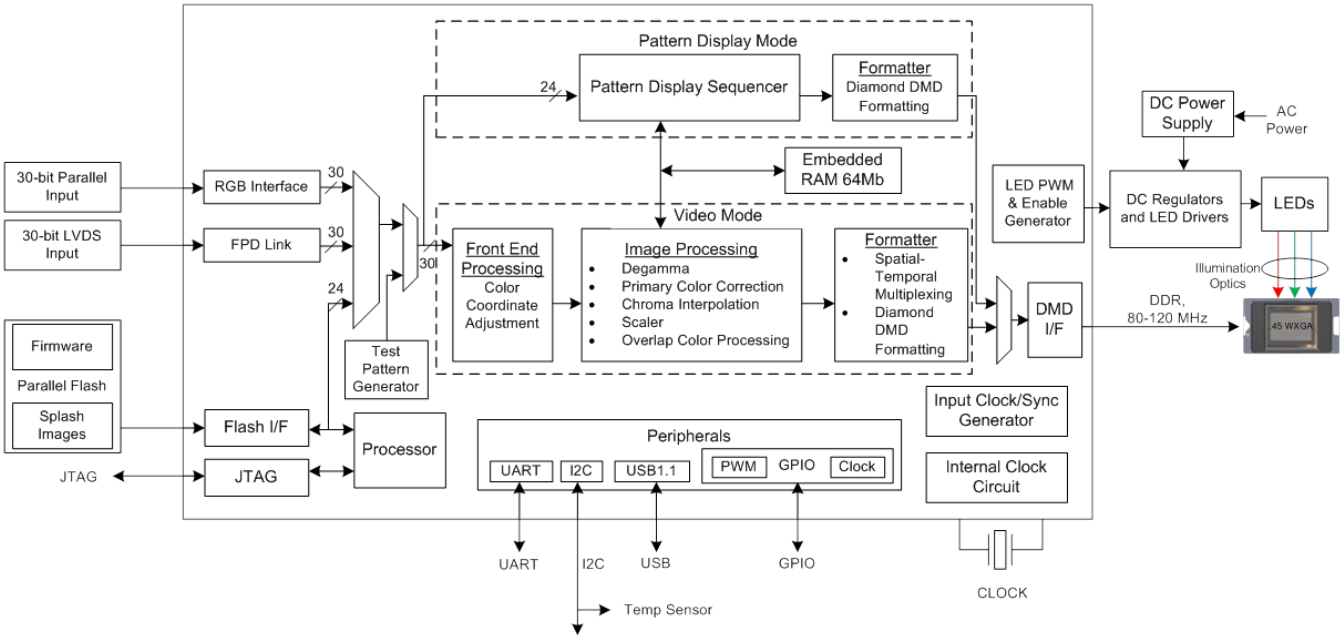

Figure 2-4. DLPC350 Functional Block Diagram

Table 2-44. Allowed Pattern Display Combinations

BIT-DEPTH	MAXIMUM EXTERNAL INPUT PATTERN RATE	MAXIMUM PATTERN RATE FOR PRE-LOADED PATTERNS	MAXIMUM NUMBER OF PATTERNS FOR PRE-LOADED PATTERNS
1	2880	4225	48
2	1428	1428	24
3	636	636	16
4	588	588	12
5	480	500	8
6	400	400	8
7	222	222	6
8	120	120	6

The video output modes operate on a per-frame basis where the DLPC350 takes the input data and appropriately allocates it in a frame. For example, a 24-bit RGB input image is allocated into a 60 Hz frame by dividing each color (red, green, and blue) into specific percentages of the frame (See Figure 2-5). Therefore, for 40% red, 45% green, and 15% blue ratio; the red, green, and blue colors have a 6.67 ms, 7.5 ms, and 2.54 ms time slot allocated, respectively. Because each color has an 8-bit depth, each color time slot is further divided into bit-planes, as shown in Figure 2-5. A bit-plane is the two-dimensional arrangement of one bit extracted from all the pixels in the full color 2D image.

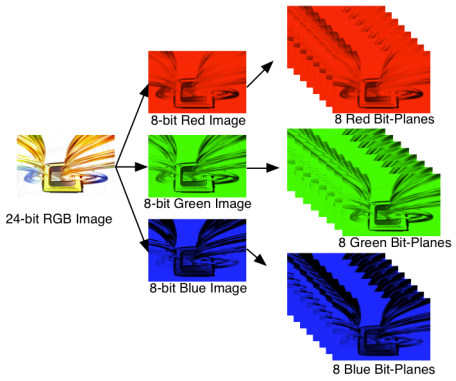

Figure 2-5. Bit-Planes of a 24-bit RGB Image

The length of each bit-plane in the time slot is weighted by the corresponding power of 2 of its binary representation. This provides a binary pulse-width modulation of the image. In the 24-bit RGB streaming input, Figure 2-6 shows that each color time slot is divided into eight bit-planes. The sum of all bit weighs in the color time slot equal 255, with each bit-plane weighted by its binary representation.

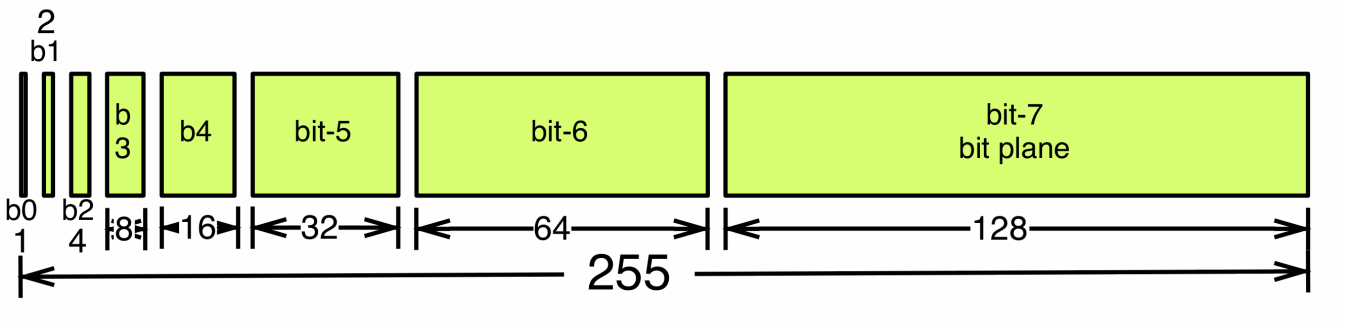

Figure 2-6. Bit Partition in a Frame for an 8-bit Monochrome Image

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane and shining light on them. With the binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on and illuminated. For a 24-bit RGB frame image input to the DLPC350, the DLPC350 creates 24 bit-planes, stores them on the internal memory buffer, and sends them to the DLP4500 DMD on the next frame, one bit-plane at a time. Depending on the bit weight of the bit-plane, the DLPC350 controls the time this bit-plane is exposed to light. The time a bit plane is illuminated is directly proportional to the intensity of the bit-plane. To improve image quality in video frames, these bit-planes, time slots, and color frames are intertwined and interleaved with spatial-temporal algorithms by the DLPC350.

For other applications where this image enhancement is not desired, the video processing algorithms can be bypassed and replaced with a specific set of bit-planes. The bit-depth of the pattern is then allocated into the corresponding binary weighted time slots. Furthermore, output trigger signals are also synchronized with these time slots to indicate when the image is displayed. For structured light applications this mechanism provides the capability to display a set of patterns and signal a camera to capture these patterns overlaid on an object .

As shown in Figure 2-7, the DLPC350 stores two 24-bit frames in its internal memory buffer. This 48 bit-plane display buffer allows the DLPC350 to send one 24-bit buffer to the DMD array while the second buffer is filled from Flash or streamed in through the 24-bit RGB interface. In streaming mode, the DMD array displays the previous 24-bit frame while the current frame fills the second 24-bit frame of the display buffer. Once a 24-bit frame is displayed, the buffer rotates accessing the next 24-bit frame to the DMD. Thus, the displayed image is a 24-bit frame behind the data streamed through the 24-bit RGB parallel interface.

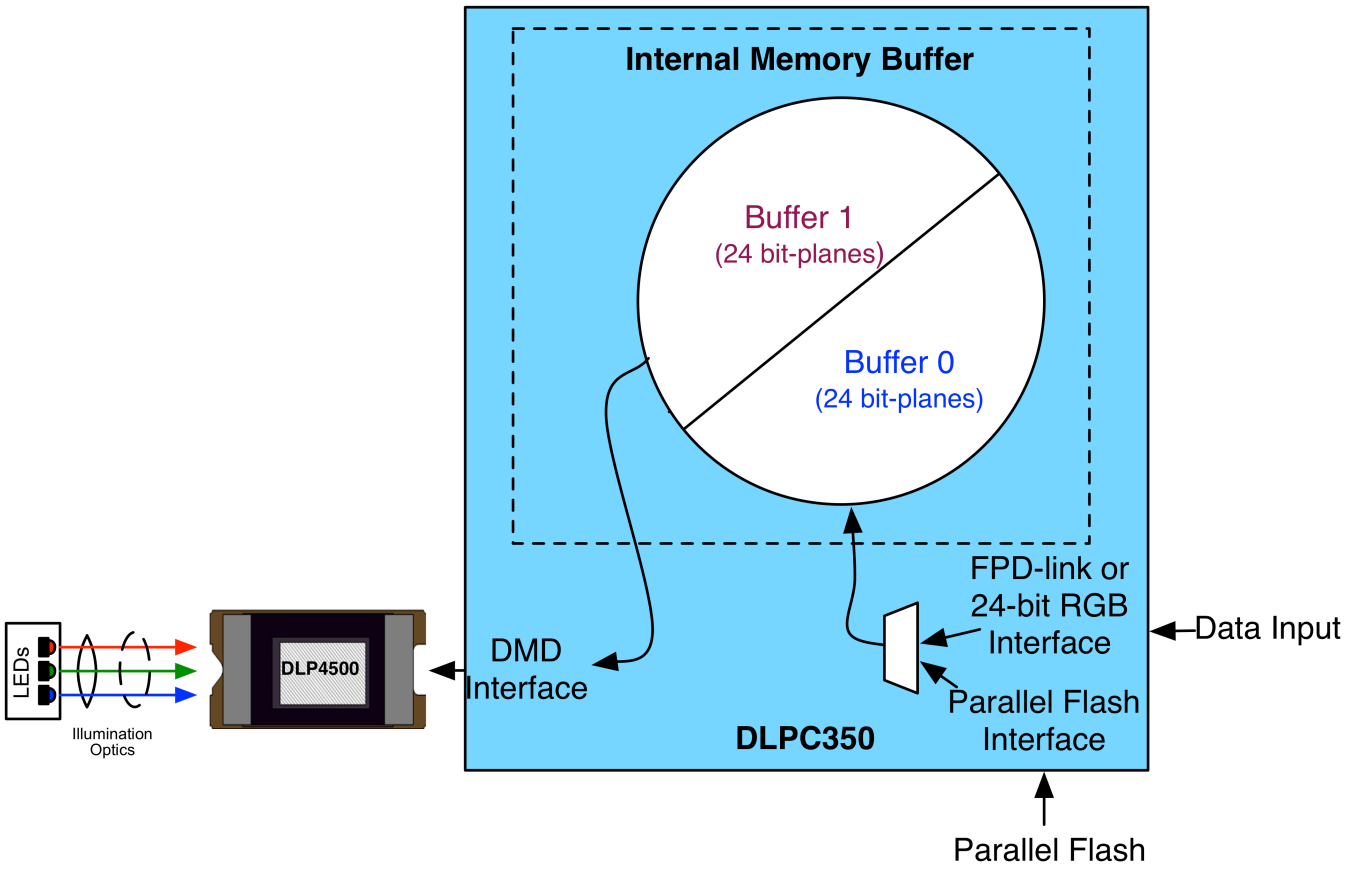

Figure 2-7. DLP4500 Frame Buffer

Note that the displayed image is frame delayed in relation to the data streamed through the 24-bit RGB parallel bus, as shown in Figure 2-8.

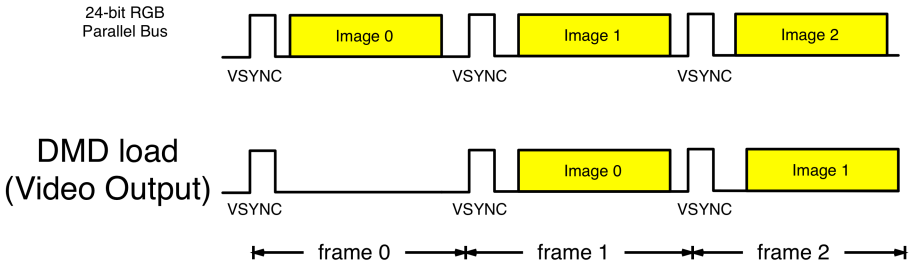

Figure 2-8. Frame Delay Between RGB Input and Video Output

2.4.1 Display Mode Selection Command

(**I²C**: 0x69)

(**USB**: CMD2: 0x1A, CMD3: 0x1B)

The Display Mode Selection Command enables the DLPC350 internal image processing functions for video mode or bypasses them for pattern display mode. This command selects between video or pattern display mode of operation. After executing this command, poll the system status using I²C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C.

Table 2-45. Display Mode Selection Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Display Mode Selection 0 = Pattern Display mode. Assumes a 1-bit through 8-bit image with a pixel resolution of 912 x 1140 and bypasses all the image processing functions of DLPC350 1 = Video Display mode. Assumes streaming video image from the 30-bit RGB or FPD-link interface with a pixel resolution of up to 1280 x 800 up to 120 Hz.	d0	wr

2.4.2 Video Mode Commands

In video mode, the DLPC350 supports up to 1280 x 800 pixel resolution at 120 Hz through its 30-bit RGB or FPD-link interfaces. The following commands are only supported in External Video Mode:

- Gamma Correction
- Input Display Resolution

2.4.2.1 Gamma Correction

(**I²C**: 0x31)

(**USB**: CMD2: 0x1A, CMD3: 0x0E)

Since the DMD is inherently linear in response, the Gamma Correction command specifies the removal of the gamma curve applied to the video data at the source. Four degamma tables are provided: TI Film, TI Graphics Enhanced, TI Video Enhanced, and Linear. After executing this command, poll the system status using I²C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C.

Table 2-46. Gamma Correction Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	3:0	Degamma Correction Table Pointer 0 = TI Film 1 =TI Graphics Enhanced 2 = TI Video Enhanced (NTSC, PAL, SECAM) 3 =Linear 4-15 = Reserved	d0	wr
	6:4	Reserved	d0	r
	7	Gamma Correction Enable: 0 = Disable, no gamma correction 1 = Enable, gamma correction	d1	wr

2.4.2.2 Input Display Resolution

(**I²C**: 0x7E)

(**USB**: CMD2: 0x10, CMD3: 0x00)

The Input Display Resolution command defines the active input resolution and active output (displayed) resolution. The maximum supported input and output resolutions for the DLP4500 0.45 WXGA DMD is 1280 pixels (columns) by 800 lines (rows). This command provides the option to define a subset of active input frame data using pixel (column) and line (row) counts relative to the source-data enable signal (DATEN). In other words, this feature allows the source image to be cropped as the first step in the processing chain. After executing this command, poll the system status using I²C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C.

Table 2-47. Input Display Resolution Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
1:0	15:0	Input image, first active pixel (column) of cropped area	d0	wr
3:2	15:0	Input image, first active line (row) of cropped area	d0	wr
5:4	15:0	Input image vertical resolution, pixels (columns) per line (row) of cropped area	d0	wr
7:6	15:0	Input image horizontal resolution, lines (rows) per frame of cropped area	d0	wr
9:8	15:0	Output image, first active pixel (column) of displayed image	d0	wr
11:10	15:0	Output image, first active line (row) of displayed image	d0	wr
13:12	15:0	Output image horizontal resolution, pixels (columns) per line (row)	d1280	wr
15:14	15:0	Output image vertical resolution, lines (rows) per frame	d800	wr

2.4.3 Pattern Display Commands

In pattern display mode, the DLPC350 supports 1-, 2-, 3-, 4-, 5-, 6-, 7-, and 8-bit images with a 912 x 1140 pixel resolution streamed through the 24-bit RGB or FPD-link interface, or stored in the flash memory locations. The following commands are only supported in Pattern Display Mode:

- Validate Data
- Trigger Controls
- LED Enable Delay Controls
- Pattern Display Controls
- Exposure Controls
- Buffer Controls

2.4.3.1 Validate Data Command

(**I²C**: 0x7D)

(**USB**: CMD2: 0x1A, CMD3: 0x1A)

The Validate Data Command checks the programmed pattern display modes and indicates any invalid settings. To execute the command, write a dummy byte followed by a one byte read. The byte read contains the status byte. This command needs to be executed after all pattern display configurations have been completed.

Table 2-48. Validate Data Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Validity of exposure or frame period settings 1 = Selected exposure or frame period settings are invalid 0 =Selected exposure or frame period settings are valid	d0	wr
	1	Validity of pattern numbers in lookup table (LUT) 1 = Selected pattern numbers in LUT are invalid 0 = Selected pattern numbers in LUT are valid	d0	wr
	2	Status of Trigger Out1 1 = Warning, continuous Trigger Out1 request or overlapping black sectors 0 = Trigger Out1 settings are valid	d0	wr
	3	Status of post sector settings 1 = Warning, post vector was not inserted prior to external triggered vector 0 = Post vector settings are valid	d0	wr
	4	Status of frame period and exposure difference 1 = Warning, frame period or exposure difference is less than 230usec 0 = Frame period or exposure difference is valid	d0	wr

2.4.3.2 Trigger Controls

To synchronize a camera with the displayed patterns, the DLPC350 supports three trigger modes:

- Trigger Mode 0:
  - VSYNC used as trigger input.
  - TRIG_OUT1 frames the exposure time of the pattern.
  - TRIG_OUT2 indicates the start of the pattern sequence or internal buffer boundary of a 24-bit plane.
- Trigger Mode 1:
  - TRIG_IN1 advances to next pattern, while TRIG_IN2 starts and pauses the pattern sequence.
  - TRIG_OUT1 frames the exposure time of the pattern.
  - TRIG_OUT2 indicates the start of the pattern sequence or internal buffer boundary of a 24-bit plane.
- Trigger Mode 2:
  - TRIG_IN1 toggles between two consecutive patterns
  - TRIG_IN2 advances to the next pair of patterns
  - TRIG_OUT1 frames the exposure time of the pattern.
  - TRIG_OUT2 indicates the start of the pattern sequence or internal buffer boundary of a 24-bit plane.

Figure 2-9 shows an example of Trigger Mode 0, where the VSYNC starts the pattern sequence display. Frame Time indicates the time between VSYNC triggers, and Display Time indicates the length of pattern sequence. This Display Time should be less than the Frame Time. The pattern sequence consists of a series of three consecutive patterns. The first pattern sequence consists of P1, P2, and P3. Since P3 is an RGB pattern, it is shown with its time sequential representation of P3.1, P3.2, and P3.3. The second pattern sequence consists of three patterns: P4, P5, and P6. The third sequence consists of P7, P8, and P9. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each of the three pattern sequences. Go to Section 4.2 to see detailed steps on how to generate this pattern sequence.

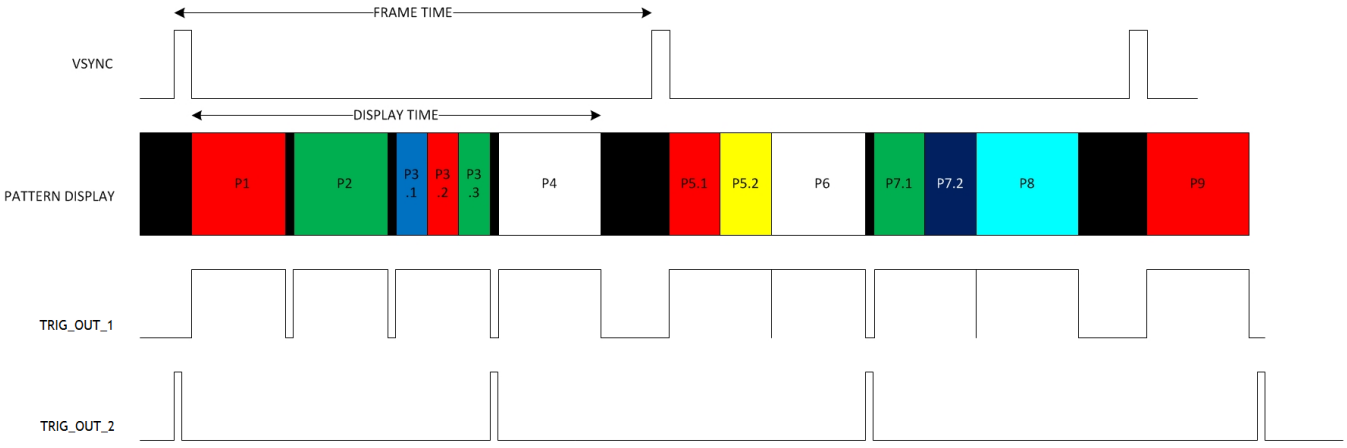

Figure 2-9. Trigger Mode 0 Timing Diagram Example

Figure 2-10 shows an example of Trigger Mode 1. A set of three-pattern sequences are displayed. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each three-pattern sequence. TRIG_IN_2 serves as a start/stop signal. By raising TRIG_IN_2, the pattern sequence starts. By lowering TRIG_IN_2, the pattern sequence stops. If the pattern sequence had been previously started, raising TRIG_IN_2 continues the pattern sequence until this signal is lowered. If TRIG_IN_2 is lowered while a pattern is displayed (see P4 in Figure 2-10), when this pattern sequence is continued, this pattern is displayed again since its full exposure was not completed.

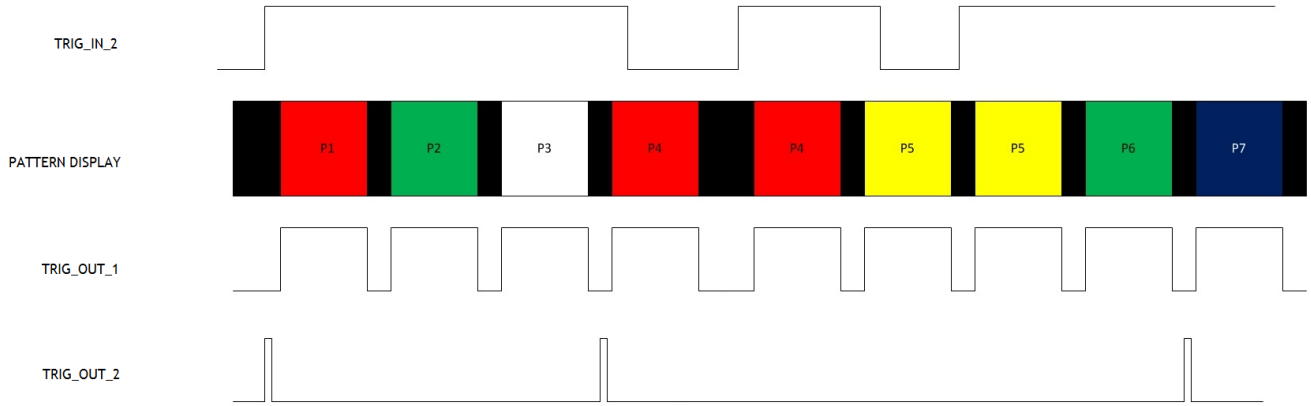

Figure 2-10. Trigger Mode 1 Timing Diagram Example

An example of trigger mode 2 is shown in Figure 2-11, where TRIG_IN_1 alternates between two patterns while TRIG_IN_2 advances to the next pair of patterns. Table 2-66 shows the allowed pattern combinations in relation to the bit depth of the pattern.

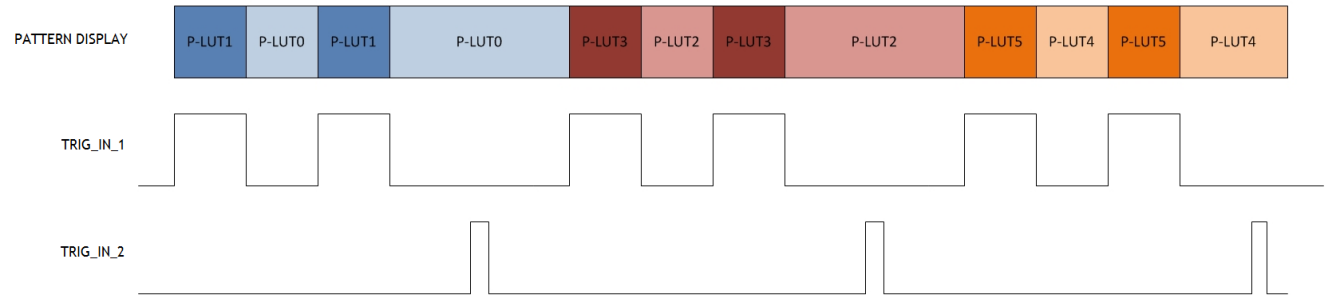

Figure 2-11. Trigger Mode 2 Timing Diagram Example

2.4.3.2.1 Pattern Trigger Mode Selection

(**I²C**: 0x70)

(**USB**: CMD2: 0x1A, CMD3: 0x23)

The Pattern Trigger Mode Selection command selects between one of the three pattern Trigger Modes. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I²C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-49. Pattern Trigger Mode Selection Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	1:0	Pattern Trigger Mode Selection 0 = Pattern Trigger Mode 0: VSYNC serves to trigger the pattern display sequence 1 = Pattern Trigger Mode 1: Internally or Externally (through TRIG_IN_1 and TRIG_IN_2) generated trigger 2 = Pattern Trigger Mode 2: TRIG_IN_1 alternates between two patterns, while TRIG_IN_2 advances to the next pair of patterns	d1	wr
	7:2	Reserved	d0	r

2.4.3.2.2 Trigger Out1 Control

(**I²C**: 0x6A)

(**USB**: CMD2: 0x1A, CMD3: 0x1D)

The Trigger Out1 Control command sets the polarity, rising edge delay, and falling edge delay of the DLPC350's TRIG_OUT_1 signal. The delays are compared to when the pattern is displayed on the DMD. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I²C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-50. Trigger Out1 Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Reserved	d0	r
	1	TRIG_OUT_1 Polarity 1 = Invert TRIG_OUT_1 polarity to an active low signal 0 = Normal TRIG_OUT_1 polarity, active high signal	d0	wr
	7:2	Reserved	d0	r
1	7:0	TRIG_OUT_1 rising edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB = 0.00 µs (default) ... 0xD4 =+2.68 µs 0xD5 = +2.787 µs	xBB	wr
2	7:0	TRIG_OUT_1 falling edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB =0.00 µs (default) ... 0xD4 = +2.68 µs 0xD5 = +2.787 µs	xBB	wr

2.4.3.2.3 Trigger Out2 Control

(**I²C**: 0x6B)

(**USB**: CMD2: 0x1A, CMD3: 0x1E)

The Trigger Out2 Control command sets the polarity and rising edge delay of the DLPC350's TRIG_OUT_2 signal. The delay is compared to when the pattern is displayed on the DMD. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I²C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-51. Trigger Out2 Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Reserved	d0	r
	1	TRIG_OUT_2 Polarity 1 = Invert TRIG_OUT_2 polarity to an active low signal 0 = Normal TRIG_OUT_2 polarity, active high signal	d0	wr
	7:2	Reserved	d0	r

Table 2-51. Trigger Out2 Control Command (continued)

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
1	7:0	TRIG_OUT_2 rising edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB =0.00 µs (default) ... 0xFE = +7.1828 µs 0xFF = +7.29 µs	xBB	wr

2.4.3.2.4 Trigger In1 Control

(**I²C**: 0x79)

(**USB**: CMD2: 0x1A, CMD3: 0x35)

The Trigger In1 Control command sets the rising edge delay of the DLPC350's TRIG_IN_1 signal compared to when the pattern is displayed on the DMD. The polarity of TRIG_IN_1 is set in the lookup table of the pattern sequence. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I²C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-52. Trigger In1 Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
3:0	18:0	TRIG_IN_1 rising edge delay. Each bit adds 107.136 ns delay	d0	wr

2.4.3.2.5 Trigger In2 Control

(**I²C**: 0x7A)

(**USB**: CMD2: 0x1A, CMD3: 0x36)

The Trigger In2 Control command sets the polarity of the DLPC350's TRIG_IN_2 signal in Trigger Mode 2. For Trigger Mode 0 or 1, TRIG_IN_2 acts as a start or stop signal. If the sequence was not already started already by a software command, the rising edge on TRIG_IN_2 signal input will start or resume the pattern sequence. If the pattern sequence is active, the falling edge on TRIG_IN_2 signal input stops the pattern sequence. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I²C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-53. Trigger In2 Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Advance pattern polarity for Trigger Mode 2 0 = Advance pattern to the next pair on rising edge of TRIG_IN_2 signal 1 = Advance pattern to the next pair on falling edge of TRIG_IN_2 signal	d0	wr
	7:1	Reserved	d0	r

2.4.3.3 LED Enable Delay Controls

The LED Enable Delay Controls commands set the rising and falling edge offsets of the LED enable signals compared to when the pattern is displayed on the DMD. This command is only for Pattern Display mode; When in a video mode, these delays should be set to 0x0.

2.4.3.3.1 Red LED Enable Control

(**I²C**: 0x6C)

(**USB**: CMD2: 0x1A, CMD3: 0x1F)

The Red LED Enable Delay Control command sets the rising and falling edge delay of the Red LED enable signal.

Table 2-54. Red LED Enable Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Red LED enable rising edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB = 0.00 µs (default) ... 0xFE = +7.1828 µs 0xFF = +7.29 µs	xBB	wr
1	7:0	Red LED enable falling edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB = 0.00 µs (default) ... 0xFE = +7.1828 µs 0xFF = +7.29 µs	xBB	wr

2.4.3.3.2 Green LED Enable Control

(**I²C**: 0x6D)

(**USB**: CMD2: 0x1A, CMD3: 0x20)

The Green LED Enable Delay Control command sets the rising and falling edge delay of the Green LED enable signal.

Table 2-55. Green LED Enable Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Green LED enable rising edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB = 0.00 µs (default) ... 0xFE = +7.1828 µs 0xFF = +7.29 µs	xBB	wr

Table 2-55. Green LED Enable Control Command (continued)

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
1	7:0	Green LED enable falling edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB = 0.00 µs (default) ... 0xFE = +7.1828 µs 0xFF = +7.29 µs	xBB	wr

2.4.3.3.3 Blue LED Enable Control

(**I²C**: 0x6E)

(**USB**: CMD2: 0x1A, CMD3: 0x21)

The Blue LED Enable Delay Control command sets the rising and falling edge delay of the Blue LED enable signal.

Table 2-56. Blue LED Enable Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Blue LED enable rising edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB = 0.00 µs (default) ... 0xFE = +7.1828 µs 0xFF = +7.29 µs	xBB	wr
1	7:0	Blue LED enable falling edge delay control. Each bit adds 107.2 ns 0x00 = -20.05 µs 0x01 = -19.9428 µs 0x02 = -19.835 µs .. 0xBB = 0.00 µs (default) ... 0xFE = +7.1828 µs 0xFF = +7.29 µs	xBB	wr

2.4.3.4 Pattern Display Controls

2.4.3.4.1 Pattern Display Data Input Source

(**I²C**: 0x6F)

(**USB**: CMD2: 0x1A, CMD3: 0x22)

The Pattern Display Data Input Source command selects the source of the data for pattern display: streaming through the 24-bit RGB/FPD-link interface or stored data in the flash image memory area from external Flash. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-57. Pattern Display Data Input Source Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	1:0	Pattern Display Data Input Source 0x00 = Pattern Display Data is streamed through the 24-bit RGB/FPD-link interface 0x01 = Reserved 0x10 =Reserved 0x11 = Pattern Display Data is fetched from flash memory	x3	wr
	7:2	Reserved	d0	r

2.4.3.4.2 Pattern Display Start/Stop Pattern Sequence

(**I^2C**: 0x65)

(**USB**: CMD2: 0x1A, CMD3: 0x24)

The Pattern Display Start/Stop Pattern sequence command starts or stops the programmed patterns sequence. After executing this command, poll the system status using I^2C commands: 0x20, 0x21, and 0x22 or the respective USB commands: 0x1A0A, 0x1A0B, and 0x1A0C.

Table 2-58. Pattern Display Start/Stop Pattern Sequence Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	1:0	Pattern Display Start/Stop Pattern Sequence 0x00 = Stop Pattern Display Sequence. The next "Start" command will restart the pattern sequence from the beginning. 0x01 = Pause Pattern Display Sequence. The next "Start" command will start the pattern sequence by re-displaying the current pattern in the sequence. 0x10 = Start Pattern Display Sequence	d0	wr
	7:2	Reserved	d0	r

2.4.3.4.3 Pattern Display Exposure and Frame Period

(**I^2C**: 0x66)

(**USB**: CMD2: 0x1A, CMD3: 0x29)

The Pattern Display Exposure and Frame Period dictates the time a pattern is exposed and the frame period. Either the exposure time must be equivalent to the frame period, or the exposure time must be less than the frame period by 230 microseconds. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I^2C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-59. Pattern Display Exposure and Frame Period Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
3:0	31:0	Exposure time (µs)	x4010	wr
7:4	31:0	Frame period (µs)	x411A	wr

2.4.3.4.4 Pattern Display Invert Data

(**I²C**: 0x74)

(**USB**: CMD2: 0x1A, CMD3: 0x30)

The Pattern Display Invert Data command dictates how the DLPC350 interprets a value of 0 or 1 to control mirror position for displayed patterns. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I²C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-60. Pattern Display Invert Data Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	0	Pattern Display Invert Data 0 = Normal operation. A data value of 1 will flip the mirror to output light, while a data value of 0 will flip the mirror to block light 1 = Inverted operation. A data value of 0 will flip the mirror to output light, while a data value of 1 will flip the mirror to block light	d0	wr
	7:1	Reserved	d0	r

2.4.3.4.5 Pattern Display LUT Control

(**I²C**: 0x75)

(**USB**: CMD2: 0x1A, CMD3: 0x31)

The Pattern Display LUT Control Command controls the execution of patterns stored in the lookup table. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I²C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-61. Pattern Display LUT Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	6:0	Number of LUT entries.. Value + 1 (range 1 through 128) 0 = One entry 1 = Two entries ... 127 = 128 entries	x15	wr
	7	Reserved	x0	wr
1	0	Repeat pattern sequence 0 = execute the pattern sequence once 1 = always repeat the pattern sequence, once a sequence is completed	x1	wr
	7:1	Reserved	x0	r
2	7:0	Number of patterns to display. Value + 1 (range 1 through 256). If in repeat mode (Byte 1, bit 0), then this value dictates how often TRIG_OUT_2 is generated.	x15	wr
3	5:0	Number of Image Index LUT Entries. Value + 1 (range 1 through 64). Field is irrelevant for Pattern Display Data Input Source set to a value other than 0x3.	x0	wr
	7:6	Reserved	x0	r

2.4.3.4.6 Pattern Display Look-Up Table

The DLPC350 supports a Pattern Display Look-Up Table (LUT) that defines the pattern sequence and the configuration parameters for each pattern in the sequence. To create this LUT, the programmer must first setup the display mode, trigger mode, exposure, frame rate, etc., before writing data to the LUT. Once properly configured, the Pattern Display LUT Access control command writes the LUT.

2.4.3.4.6.1 Pattern Display LUT Offset Pointer

(**I²C**: 0x76)

(**USB**: CMD2: 0x1A, CMD3: 0x32)

The Pattern Display LUT Offset Pointer defines the location of the LUT entries in the DLPC350 memory

Table 2-62. Pattern Display LUT Offset Pointer Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Defines offset for LUT entries (data mailbox)	x0	w

2.4.3.4.6.2 Pattern Display LUT Access Control

(**I²C**: 0x77)

(**USB**: CMD2: 0x1A, CMD3: 0x33)

The LUT on the DLPC350 has a mailbox to send data to different registers, and this command selects which register will receive the data. To select the flash image indexes or define the patterns used in the pattern sequence for the pattern display mode, first open the mailbox for the appropriate function by writing the appropriate bit. Second, write the desired data to the mailbox using the Pattern Display LUT Data command (I2C: 0x78 or USB 0x1A34) and then use this command to close the mailbox. Before executing this command, stop the current pattern sequence. After executing this command, send the Validation command (I²C: 0x7D or USB: 0x1A1A) once before starting the pattern sequence.

Table 2-63. Pattern Display LUT Access Control Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Write the appropriate value to the mailbox 0 = Disable (close) the mailboxes 1 = Open the mailbox for image index configuration 2 = Open the mailbox for pattern definition 3-127 = Reserved	x0	w

2.4.3.4.6.3 Pattern Display LUT Data

(**I²C**: 0x78)

(**USB**: CMD2: 0x1A, CMD3: 0x34)

The following parameters: display mode, trigger mode, exposure, and frame rate must be set up before sending any mailbox data. If the Pattern Display Data Input Source is set to streaming, the image indexes do not need to be set. Regardless of the input source, the pattern definition must be set.

If the mailbox was opened to define the flash image indexes, list the index numbers in the mailbox. For example, if image indexes 0-3 are desired, write 0x0 0x1 0x2 0x3 to the mailbox. Similarly, if the desired image index sequence is 0, 1, 2, 1, then write 0x0 0x1 0x2 0x1 to the mailbox.

Table 2-64. Pattern Display LUT Data - Image Index Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	7:0	Image Index (0 based index)	x0	w

If the mailbox was opened to define the individual patterns, write three bytes of data per pattern to the mailbox.

Table 2-65. Pattern Display LUT Data - Pattern Definition Command

BYTE	BIT(S)	DESCRIPTION	RESET	TYPE
0	1:0	Select the trigger type for the pattern b00 = Internal b01 = External Positive b10 = External Negative b11 = No Input Trigger (Continue from previous; Pattern still has full exposure time)	LUT Entries (1) x042120 x002124 x002128 x00212C x002130 x002134 x002138 x00213C x002100 x002104 x002108 x00210C x002110 x002114 x002118 x00211C x002140 x002144 x002148 x00214C x002150 x002154	w
	7:2	Pattern number (0 based index). For pattern number 0x3F, there is no pattern display. The maximum number supported is 24 for 1 bit-depth patterns. Setting the pattern number to be 25, with a bit-depth of 1 will insert a white-fill pattern. Inverting this pattern will insert a black-fill pattern. These patterns will have the same exposure time as defined in the Pattern Display Exposure and Frame Period command. Table 2-66 helps illustrate which bit planes are illuminated by each pattern number.		w
1	3:0	Select desired bit-depth b0000 = Reserved b0001 = 1 bit b0010 = 2 bit ... b1000 = 8 bit 0x9-0xF = Reserved		w
	7:4	Choose the LEDs that are on: b0 = Red, b1 = Green, b2 = Blue b000 = No LED (Pass Through) b001 = Red b010 = Green b011 = Yellow (Green + Red) b100 = Blue b101 = Magenta (Blue + Red) b110 = Cyan (Blue + Green) b111 = White (Blue + Green + Red)		w
2	0	0 = Do not invert pattern 1 = Invert Pattern		w
	1	0 = Do not insert any post pattern 1 = Insert black-fill pattern after current pattern. This setting requires 230 µs of time before the start of the next pattern.		w
	2	0 = Do not perform a buffer swap 1 = Perform a buffer swap		w
	3	0 = Trigger Out 1 has a rising edge at the start of a pattern, and a falling edge at the end of the pattern 1 = Trigger Out 1 will continue to be high. There will be no falling edge between the end of the previous pattern and the start of the current pattern. Exposure time is shared between all patterns defined under a common trigger out). This setting cannot be combined with the black-fill pattern (Byte 2, bit 1).		w
	7:4	Reserved		r

(1) The default LUT entries are listed. Each hex value describes an individual pattern (bytes 2:0).

The following table describes the mapping between the DLPC350 24-bit RGB interface and the display sequence expected image contents. For example, when displaying an 8-bit pattern, 3 patterns are inputted through the 24-bit RGB interface. One pattern is streamed through the green data pins, a second pattern is streamed through the red data pins, and a third pattern is streamed through the blue data pins. When displaying a 1-bit pattern, 24 patterns are inputted through the 24-bit RGB interface, with each pattern streamed through a bit of this interface.

Table 2-66. Pattern Number Mapping

Pattern Number	1-bit	2-bit	3-bit	4-bit	5-bit	6-bit	7-bit	8-bit
0	G0	G1 G0	G2 G1 G0	G3 G2 G1 G0	G5 G4 G3 G2 G1	G5 G4 G3 G2 G1 G0	G7 G6 G5 G4 G3 G2 G1	G7 G6 G5 G4 G3 G2 G1 G0
1	G1	G3 G2	G5 G4 G3	G7 G6 G5 G4	R3 R2 R1 R0 G7	R3 R2 R1 R0 G7 G6	R7 R6 R5 R4 R3 R2 R1	R7 R6 R5 R4 R3 R2 R1 R0
2	G2	G5 G4	R0 G7 G6	R3 R2 R1 R0	B1 B0 R7 R6 R5	B1 B0 R7 R6 R5 R4	B7 B6 B5 B4 B3 B2 B1	B7 B6 B5 B4 B3 B2 B1 B0
3	G3	G7 G6	R3 R2 R1	R7 R6 R5 R4	B7 B6 B5 B4 B3	B7 B6 B5 B4 B3 B2		
4	G4	R1 R0	R6 R5 R4	B3 B2 B1 B0				
5	G5	R3 R2	B1 B0 R7	B7 B6 B5 B4				
6	G6	R5 R4	B4 B3 B2					
7	G7	R7 R6	B7 B6 B5					
8	R0	B1 B0						
9	R1	B3 B2						
10	R2	B5 B4						
11	R3	B7 B6						
12	R4							
13	R5							
14	R6							
15	R7							
16	B0							
17	B1							
18	B2							
19	B3							
20	B4							
21	B5							
22	B6							
23	B7							
24	Black							

Power-Up/Down and Initialization Considerations

This chapter describes the initial power-up and power-down considerations as well as other initialization considerations.

3.1 Power Up

The DLPC350 is initialized and ready to process commands 0.1 seconds after the signal $\overline{\text{RESET}}$ is driven high. Detailed power-up timing is given in the DLPC350 Datasheet.

3.2 Power Down

No commands are required at power down of the DLPC350. The DC power supplies must be turned off, and PWRGOOD must be set low, according to the timing in the DLPC350 Datasheet.

3.3 Power-Up Auto-Initialization

Upon release of system reset, the DLPC350 executes an auto-initialization routine that is automatically uploaded from flash. This initialization process consists of setting specific register configurations, uploading specific configuration tables (such as sequence), displaying a defined splash screen. The goal of the auto-initialization process is to allow the DLPC350 to fully configure itself for default operation with no external I^2C control.

An *auto-initialization* status flag, INIT_DONE, is held high to indicate that auto initialization is in progress. It is set low when auto-initialization is complete. Subsequently, INIT_DONE is configured as an output interrupt signal that outputs an active high pulse when an error condition exists. Additionally, after INIT_DONE is set low, the EXT_PWR_ON signal is set high to indicate to the host processor or power supply that the DLPC350 is powered on.

Pattern Display Mode Examples

4.1 Pattern Display Mode Example

The following steps illustrate how to set up pattern sequences. The corresponding USB Command bytes are listed next to each step.

1. Enable pattern display mode (bypass video processing algorithms) 0x1A1B -> 0x01.
2. Set pattern display mode to flash image or external video. 0x1A22 -> 0x03 or 0x00.
3. Set the number of patterns. 0x1A31
   (a) Byte 0- number of LUT entries
   (b) Byte 1- setting 0x00 means the pattern sequence will be executed once; setting x01 means the pattern sequence will be repeated
   (c) Byte 2- determines the number of patterns in the pattern sequence (how many patterns between trigger out2 pulses)
   (d) Byte 3- if pattern display mode (Step 2) is set to flash images, this indicates the number of flash images used as patterns
4. Set the pattern trigger mode. 0x1A23 -> 0x00, 0x01, or 0x02 for mode 0, 1, or 2
5. Set the exposure and frame rate (4 bytes for each). 0x1A29
6. Set up the image indexes if using flash images.
   (a) Open mailbox. 0x1A33 -> 0x01 for image indexes
   (b) Set mailbox offset. 0x1A32
   (c) Set image indexes. 0x1A34
      (i) Choosing 1 or 2 image indexes will pre-fill the buffer
   (d) Close mailbox. 0x1A33 -> 0x00
7. Set up the LUT.
   (a) Open mailbox. 0x1A33 -> 0x02 for LUT
   (b) Set mailbox offset. 0x1A32
   (c) Fill pattern data. 0x1A34
      (i) Byte 0, b1:0- choose trigger: internal (0x00), external positive (0x01), external negative (0x02), continue from previous (0x03)
      (ii) Byte 0, b7:2- choose pattern number (what bit planes will be illuminated). Max is 24 for 1 bit-depth
      (iii) Byte 1, b3:0, choose bit weight (1-8)
      (iv) Byte 1, b6:4, choose which LEDs are on (Blue, Green, Red)
      (v) Byte 2
         (i) b0- invert pattern if 1
         (ii) b1- insert black pattern after current pattern if 1 (should be 0 if continuous trigger)
         (iii) b2- perform buffer swap if 1
         (iv) b3- trigger out1 stays high (if this stays high for n patterns, then exposure time is shared between n patterns)
      (vi) Repeat (I) through (v) for each pattern in the sequence
   (d) Close mailbox. 0x1A33 -> 0x00

8. Execute the Validate command. 0x1A1A
9. Read statuses. 0x1A0A, 0x1A0B, 0x1A0C
10. If the Validate or Status commands show an error, change the system configuration to remove the error.
11. Start the pattern sequence, either with trig in2 or 0x1A24.

4.2 Trigger Mode 0 Example

To generate the pattern sequence displayed in Figure 2-9, the pattern should be configured as listed below:

1. Enable pattern display mode (bypass video processing algorithms) 0x1A1B -> 0x01.
2. Set pattern display mode to external video. 0x1A22 -> 0x00.
3. Set the number of patterns. 0x1A31
   (a) Byte 0- number of LUT entries = 0xD
   (b) Byte 1- repeat the pattern sequence = 0x1
   (c) Byte 2- determines the number of patterns in the pattern sequence (how many patterns between TRIG_OUT_2 pulses) = 0x3
   (d) Byte 3- if pattern display mode (Step 2) is set to flash images, this indicates the number of flash images used as patterns = 0x0
4. Set the pattern trigger mode to vsync. 0x1A23 -> 0x00
5. Set the exposure and frame rate (4 bytes for each) so that the time between vsync triggers will allow three patterns to be shown For example, for a 60Hz vsync, the maximum exposure time is 16,667 ÷ 3. 0x1A29
6. Set up the LUT.
   (a) Open mailbox. 0x1A33 -> 0x02 for LUT
   (b) Set mailbox offset. 0x1A32
   (c) Fill pattern data. 0x1A34
      (i) Byte 0, b1:0- choose trigger. The first pattern in the sequence should have an external positive trigger. The next patterns in the sequence should be set to the continuous trigger.
      (ii) Byte 0, b7:2- choose pattern number (what bit planes will be illuminated). Max is 24 for 1 bit-depth
      (iii) Byte 1, b3:0, choose bit weight (1-8)
      (iv) Byte 1, b6:4, choose which LEDs are on (Blue, Green, Red)
      (v) Byte 2
         (i) b0- invert pattern if 1
         (ii) b1- insert black pattern after current pattern if 1 (should be 0 if continuous trigger)
         (iii) b2- perform buffer swap if 1 (this should be done at every external positive trigger in streaming mode)
         (iv) b3- trigger out1 stays high (if this stays high for n patterns, then exposure time is shared between n patterns)
      (vi) Repeat (I) through (v) for each pattern in the sequence
   (d) The LUT for this example is: 0x62101 0x21107 0x0410B 0x8110B 0xA210B 0x27117 0x41119 0x8311B 0x27123 0x02127 0x84127 0x2612F 0x61131
   (e) Close mailbox. 0x1A33 -> 0x00
7. Execute the Validate command. 0x1A1A
8. Read statuses. 0x1A0A, 0x1A0B, 0x1A0C
9. If the Validate or Status commands show an error, change the system configuration to remove the error.
10. Start the pattern sequence, either with TRIG_IN_2 or 0x1A24.

Register Quick Reference

This appendix provides a quick reference summary of all available registers.

A.1 I²C Register Quick Reference

Table A-1. Register Quick Reference

I²C Address	Description	Type	Reset Value	Default Action
0x00	Input Source Select	WR	0x8	24-bit Parallel Interface
0x02	Pixel Format	WR	0x0	RGB 4:4:4
0x03	Port Clock Select	WR	0x0	Port Clock A
0x04	Channel Swap	WR	0x4	ABC = BAC
0x05	FPD Mode	WR	0x20	Pixel Mapping Mode 2 with FPD-Link output mapped from CONT1 onto Field Signal for FPD-link interface port
0x06	Curtain Color Control	WR	0x0 0x0 0x0 0x0 0x0 0x0	Curtain is Black
0x07	Power Control	WR	0x0	Normal Operation
0x08	Long Axis Flip	WR	0x0	Flip Disabled
0x09	Short Axis Flip	WR	0x0	Flip Disabled
0x0A	Test Pattern Select	WR	0x8	RGB Ramp
0x0B	LED PWM Polarity	WR	0x0	Normal Polarity
0x10	LED Enable	WR	0x8	LEDs Controlled by Sequencer
0x11	Get Version	R	0x00010100	Version 1.1.0
0x13	Reset	W	0x0	n/a
0x1A	Test Pattern Color	WR	0x3FF 0x3FF 0x3FF 0x0 0x0 0x0	White Foreground, Black Background
0x20	Hardware Status	R	0x1	No Errors
0x21	System Status	R	0x1	No Errors
0x22	Main Status	R	0x0	No Errors
0x26	CSC Data	WR	0x400 0x0 0x0 0x0 0x400 0x0 0x0 0x0 0x400	RGB 4:4:4 Color-Space Coefficients
0x31	Gamma Control	WR	0x8	Gamma Correction Enabled
0x40	PWM Enable	WR	Channel Dependent	Channel Dependent
0x41	PWM Setup	WR	Channel Dependent	Channel Dependent
0x43	PWM Capture	WR	Channel Dependent	Channel Dependent
0x44	GPIO Configuration	WR	Channel Dependent	Channel Dependent
0x48	Clock Configuration	WR	Channel Dependent	Channel Dependent
0x4B	LED Current	WR	0x97 0x78 0x7D	LED PWMs

Table A-1. Register Quick Reference (continued)

I²C Address	Description	Type	Reset Value	Default Action
0x4E	PWM Capture Read	R	Channel Dependent	Channel Dependent
0x61	Image Load Timing	WR	0x0	n/a
0x65	Pattern Start/Stop	WR	0x0	Pattern Stopped
0x66	Pattern Exposure/Frame Rate Period	WR	0x4010 0x411A	100 ms Exposure with 100 ms Frame Rate
0x69	Display Mode	WR	0x0	Video Mode (Opposed to Pattern Display Mode)
0x6A	Trigger Out 1 Control	WR	0x0 0xBB 0xBB	Normal Polarity with No Rising/Falling Delay
0x6B	Trigger Out 2 Control	WR	0x0 0xBB	Normal Polarity with No Rising Delay
0x6C	Red Enable Delay	WR	0xBB 0xBB	No Rising/Falling Delay
0x6D	Green Enable Delay	WR	0xBB 0xBB	No Rising/Falling Delay
0x6E	Blue Enable Delay	WR	0xBB 0xBB	No Rising/Falling Delay
0x6F	Pattern Display Mode	WR	0x3	Display Patterns from Flash
0x70	Pattern Trigger Mode	WR	0x1	Control Pattern Sequence with Internal/External Trigger
0x71	Buffer Swap	WR	0x0	No Buffer Swap Performed
0x72	Buffer Write Disable	WR	0x0	Buffer Write Enabled
0x73	Current Read Buffer	WR	0x0	Current Buffer Streaming to DMD is Buffer #0
0x74	Invert Data	WR	0x0	Normal Operation
0x75	Pattern Configuration	WR	0x17 0x1 0x17 0x0	24 LUT Entries to be Repeated in a Pattern Sequence of Length 24, From 1 Flash Image
0x76	Mailbox Address	W	0x0	No Offset to LUT Location
0x77	Mailbox Control	W	0x0	Malbox Closed
0x78	Mailbox Data	W	See Command Description	See Command Description
0x79	Trigger In 1 Control	WR	0x0	No Delay
0x7A	Trigger In 2 Control	WR	0x0	Advance Pattern Pair on Rising Edge (For Trigger Mode 2)
0x7C	Buffer Freeze	WR	0x1	Disable Buffer Swapping
0x7D	Validate	R	0x0	Pattern Display Mode Settings are Valid
0x7E	Manual Input Display Resolution	WR	0x0 0x0 0x0 0x0 0x0 0x0 0x500 0x320	Output Display Resolution is 1280 x 800
0x7F	Image Load	WR	0xFF	Last Image Index

A.2 Command Guide

This section illustrates which commands can be used in which modes.

Table A-2. Command Matrix

Command Name	I2C	USB	Number of Bytes	External Video Mode	Flash Image Mode	Test Pattern Mode	Pattern Streaming Mode	Patterns from Flash Mode
Input Source Select	0x00	0x1A00	1	x	x	x	x	x
Pixel Format	0x02	0x1A02	1	x			x	
Port Clock Select	0x03	0x1A03	1	x			x	

Table A-2. Command Matrix (continued)

Command Name	I2C	USB	Number of Bytes	External Video Mode	Flash Image Mode	Test Pattern Mode	Pattern Streaming Mode	Patterns from Flash Mode
Channel Swap	0x04	0x1A37	1	x			x	
FPD Mode	0x05	0x1A04	1	x			x	
Curtain Color Control	0x06	0x1100	6	x			x	
Power Control	0x07	0x0200	1	x	x	x	x	x
Long Axis Flip	0x08	0x1008	1	x	x	x	x	x
Short Axis Flip	0x09	0x1009	1	x	x	x	x	x
Test Pattern Select	0x0A	0x1203	1	x	x	x		
LED PWM Polarity	0x0B	0x1A05	1	x	x	x	x	x
LED Enable	0x10	0x1A07	1	x	x	x	x	x
Get Version	0x11	0x0205	16	x	x	x	x	x
Reset	0x13	0x0802	1	x	x	x	x	x
Test Pattern Color	0x1A	0x1204	12			x		
Hardware Status	0x20	0x1A0A	1	x	x	x	x	x
System Status	0x21	0x1A0B	1	x	x	x	x	x
Main Status	0x22	0x1A0C	1	x	x	x	x	x
CSC Data	0x26	0x1A0D	18	x			x	
Gamma Control	0x31	0x1A0E	1	x	x	x		
PWM Enable	0x40	0x1A10	1	x	x	x	x	x
PWM Setup	0x41	0x1A11	6	x	x	x	x	x
PWM Capture	0x43	0x1A12	5	x	x	x	x	x
GPIO Configuration	0x44	0x1A38	2	x	x	x	x	x
Clock Configuration	0x48	0x0807	2	x	x	x	x	x
LED Current	0x4B	0x0B01	3	x	x	x	x	x
PWM Capture Read	0x4E	0x1A13	5	x	x	x	x	x
Image Load Timing	0x61	0x1A3A	4	x		x	x	x
Pattern Start/Stop	0x65	0x1A24	1				x	x
Pattern Exposure/Frame Rate Period	0x66	0x1A29	8				x	x
Display Mode	0x69	0x1A1B	1	x	x	x	x	x
Trigger Out 1 Control	0x6A	0x1A1D	3				x	x
Trigger Out 2 Control	0x6B	0x1A1E	2				x	x
Red Enable Delay	0x6C	0x1A1F	2				x	x
Green Enable Delay	0x6D	0x1A20	2				x	x
Blue Enable Delay	0x6E	0x1A21	2				x	x
Pattern Display Mode	0x6F	0x1A22	1				x	x
Pattern Trigger Mode	0x70	0x1A23	1				x	x
Buffer Swap	0x71	0x1A26	1	x	x	x	x	x

Table A-2. Command Matrix (continued)

Command Name	I2C	USB	Number of Bytes	External Video Mode	Flash Image Mode	Test Pattern Mode	Pattern Streaming Mode	Patterns from Flash Mode
Buffer Write Disable	0x72	0x1A27	1	x	x	x	x	x
Current Read Buffer	0x73	0x1A28	1	x	x	x	x	x
Invert Data	0x74	0x1A30	1				x	x
Pattern Configuration	0x75	0x1A31	4				x	x
Mailbox Address	0x76	0x1A32	1				x	x
Mailbox Control	0x77	0x1A33	1				x	x
Mailbox Data	0x78	0x1A34	4				x	x
Trigger In 1 Control	0x79	0x1A35	4				x	x
Trigger In 2 Control	0x7A	0x1A36	1				x	x
Buffer Freeze	0x7C	0x100A	1	x	x	x	x	x
Validate	0x7D	0x1A1A	1				x	x
Manual Input Display Resolution	0x7E	0x1000	16	x				
Image Load	0x7F	0x1A39	1	x	x	x		x

Revision A History

Changes from Original (May 2013) to A Revision	Page
• Changed Version Number to 1.1.0	12
• Added DLPC350 Programming Commands Section	12
• Added Input Value Bits for GPIO Configuration	28
• Added GPIO Channel Byte for PWM Capture	31
• Changed Max TRIG_OUT_1 Delays	39
• Changed Pattern Exposure and Frame Period Values	43
• Changed Default Number of Patterns in LUT	44
• Changed Default Pattern LUT	46
• Deleted Temperature Commands from Register Quick Reference	51
• Deleted Temperature Commands from Command Matrix	52

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision B History

Changes from A Revision (July 2013) to B Revision	Page
• Changed Version Number for Future Releases	12
• Changed Current Control Unit From 1/2 256 Steps to 256 Steps	27
• Changed Trigger Signals to follow TRIG_X_X Format	37
• Changed Description of Pattern Exposure and Frame Period	43
• Changed Description of Number of Patterns in LUT Control Command	44
• Changed Black-Fill Time from 225 µs to 230 µs	46

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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