Evaluation Board for a Custom Incremental Delta-Sigma Analog-to-Digital Converter Chip

By:
Maxwell Pauly
Dylan Sodetani

Advisor:
Dr. Boris Murmann

A report submitted in partial fulfillment
of the requirements for

Master's Plan B Project

Date: May 16, 2025

Department of Electrical and Computer Engineering
University of Hawaii at Manoa

ABSTRACT:

This project involved the design and testing of an evaluation board for a custom-designed analog-to-digital converter (ADC) chip and to perform testing on the chip to characterize its functionality and performance. The primary goal was to develop a board capable of interfacing with the ADC's pinout while ensuring signal integrity across both of the analog and digital domains. The design focused on minimizing crosstalk, isolating power, analog, and digital components, and successfully interfacing with external testing equipment, specifically the Analog and Digital Discovery boards. Once the evaluation board was fabricated, a series of tests were performed to verify its functionality and assess the chip's performance across six circuits. The key findings included characterizing the approximately linear transfer characteristic for each circuit and measuring the variance in output measurements, both of which was found to be sensitive to the clock speed. Lowering the clock speed helped to reduce measurement variance and improve precision allowing the team to characterize the capabilities of the chip. Despite these improvements, further investigations are required to address the sources of measurement error, such as analog noise and circuit offsets. The results demonstrate the successful creation of the evaluation board and highlight the chip's ability to produce accurate readings under optimized conditions. Further testing and refinement can be performed to enhance the chip's overall performance, but this work has provided a steady foundation for the chip's evaluation.

TABLE OF CONTENTS

I. INTRODUCTION

This project focuses on the design and fabrication of a printed circuit board (PCB) to evaluate a custom analog-to-digital converter (ADC) chip. Developed by students in the Spring 2024 EE 628 course, the chip is a 12-bit incremental delta-sigma ADC housed in a 32-pin package and contains six distinct ADC circuits. The evaluation board was designed to interface with this chip and facilitate performance testing. Over the semester, the team constructed and simulated the board's schematics, prepared for PCB layout, and tested the supporting hardware framework. The design process was completed in KiCAD, with collaboration managed via GitHub.

II. EVALUATION BOARD DESIGN OVERVIEW

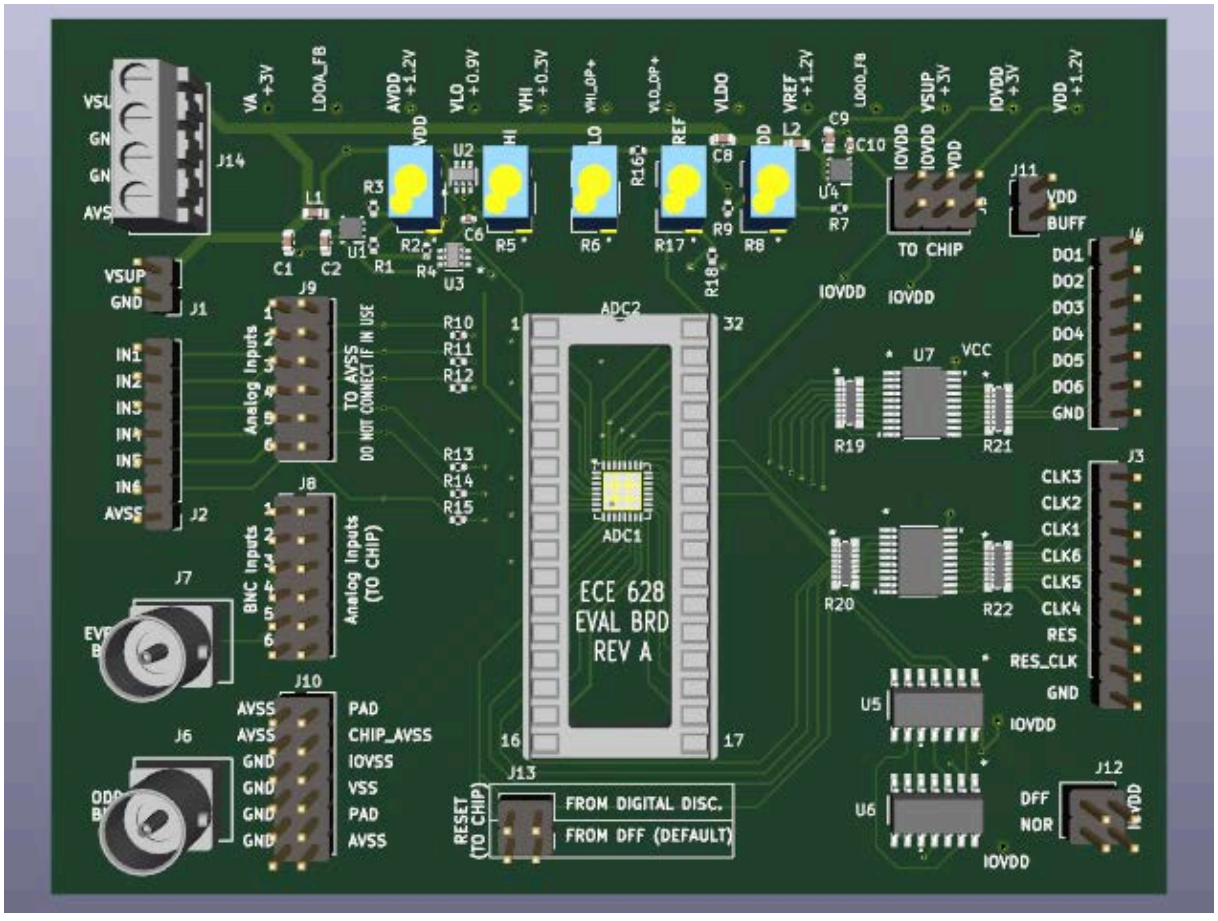


Fig. 1. Evaluation Board Design (KiCAD 3D Rendering)

Figure 1 shows a 3D rendering of the evaluation board, generated from the KiCAD layout. The evaluation board is a 4-layer mixed-signal PCB designed to support analog, digital, and power subsystems for testing packaged chips. It supplies power and reference voltages to the chip, transmits analog and digital clock signals, and captures the chip's digital output. The board accepts an external analog input, which is filtered through a low-pass filter to minimize high-frequency noise before reaching the ADC chip. A high-speed clock signal is also provided externally, buffered on-board, and used to drive the ADC's sampling process. After conversion, the chip's digital output is buffered and routed to high-speed digital I/O pins for capture and analysis. External software tools and simple processing scripts are then used to interpret the digital output and evaluate the ADC's performance. The PCB interfaces with Digilent's Analog Discovery and Digital Discovery boards, as shown in Figure 1 [1,2].

(a) (b)

Fig. 1. (a) Analog Discovery Board and (b) Digital Discovery Board by Digilent [1,2]

Table I lists the pins on the ADC chip and summarizes how the board interacts with each.

TABLE I
Pin Guide for ADC & Board Functionality

#	Name	I/O	Description:	What the Eval Board Does:
1	IN1	I	ADC Input 1	Pass signal from Analog Input
2	IN2	I	ADC Input 2	Pass signal from Analog Input
3	IN3	I	ADC Input 3	Pass signal from Analog Input
4	VHI	I	HI reference (0.9V)	Generate 0.9V through voltage followers
5	VLO	I	LO reference (0.3V)	Generate 0.3V through voltage followers
6	IN4	I	ADC Input 4	Pass signal from Analog Input
7	IN5	I	ADC Input 5	Pass signal from Analog Input
8	IN6	I	ADC Input 6	Pass signal from Analog Input
9	PAD	I	Die paddle	Connect to board's Analog GND (AVSS)
10	AVSS	I	Analog VSS	Connect to board's Analog GND (AVSS)
11	RES	I	Reset line (all ADCs)	Buffer reset pulse & pass to ADC RES pin
12	IOVSS	I	VSS for output drivers	Connect to board's Digital GND (VSS)
13	CK4	I	ADC Clock Input 4	Buffer clock signal & pass to ADC pin
14	CK5	I	ADC Clock Input 5	Buffer clock signal & pass to ADC pin
15	CK6	I	ADC Clock Input 6	Buffer clock signal & pass to ADC pin
16	VSS	I	Digital logic VSS	Connect to board's Digital GND (VSS)
17	OUT6	O	ADC Output 6	Buffer chip's signal & pass to output header
18	OUT5	O	ADC Output 5	Buffer chip's signal & pass to output header
19	OUT4	O	ADC Output 4	Buffer chip's signal & pass to output header
20	IOVSS	I	VSS for output drivers	Connect to board's Digital GND (VSS)
21	IOVDD	O	VDD for output drivers (3V)	Pass +3V supply connected to board
22	OUT3	O	ADC Output 3	Buffer chip's signal & pass to output header
23	OUT2	O	ADC Output 2	Buffer chip's signal & pass to output header
24	OUT1	O	ADC Output 1	Buffer chip's signal & pass to output header
25	VDD	I	Digital logic VDD (1.2V)	Generate +1.2V source from on-board LDO
26	CK1	I	ADC Clock Input 4	Buffer clock signal & pass to ADC pin
27	CK2	I	ADC Clock Input 5	Buffer clock signal & pass to ADC pin
28	CK3	I	ADC Clock Input 6	Buffer clock signal & pass to ADC pin
29	IOVDD	I	VDD for output drivers (3V)	Pass +3V supply connected to board
30	VLDO	I	Internal LDO output	Connect to test point for voltmeter measurement
31	VREF	I	Ref. for LDO (1.2V)	Generate +1.2V from resistive divider
32	AVDD	I	Analog VDD (1.2V)	Generate +1.2V source from on-board LDO

The overall board layout and stackup were carefully designed with a focus on isolating the analog and digital circuits from one another. The top and bottom layers of the board are dedicated to routing signal lines, while layer 2 serves as the digital ground and layer 3 is dedicated to analog ground (AVSS). The component placement, as shown in Figure 2, was planned to clearly separate analog and digital components. This separation was key to minimizing interference and optimizing the performance of both subsystems.

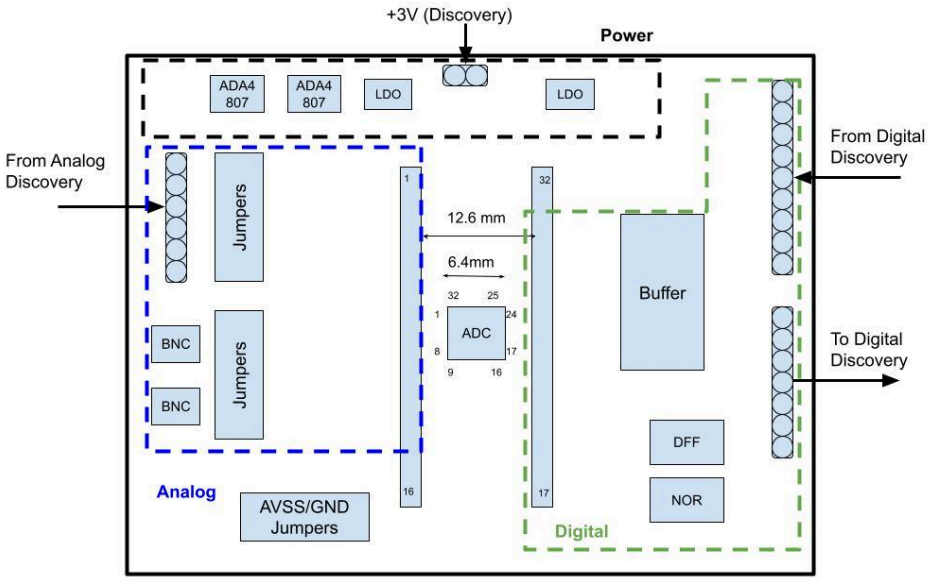


Fig. 2. PCB layout floor plan

A. Power Supply

The PCB operates on a single +3 V power rail supplied externally, labeled VA on the board's test points. The board can be powered through a 2.54 mm male header or through a 4-pin terminal block power connector. This voltage is filtered on-board using capacitors and ferrite beads to ensure clean power delivery. Two on-board low-dropout (LDO) regulators independently supply +1.2 V to the ADC's analog (AVDD) and digital (VDD) domains.

The analog supply also generates the ADC's reference voltages. VHI and VLO, the high and low references for the ADC, have nominal values of +0.9 V and +0.3 V, respectively. These

are derived from the +1.2 V AVDD rail using a resistive divider followed by voltage followers to ensure low impedance and stable output. Additionally, the ADC's on-chip LDO requires a +1.2 V reference (VREF), which is generated from the +3 V input using another resistive divider.

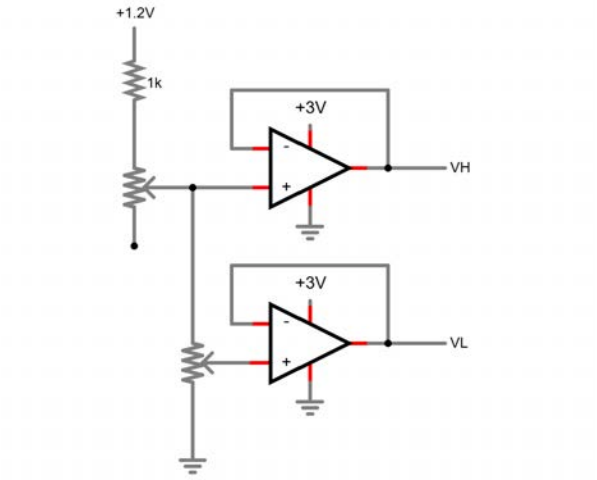


Fig. 3. Voltage Follower Circuit for VHI and VLO References

To support adjustable biasing and troubleshooting, potentiometers are included in the resistive dividers at key points to adjust particular references (VLO, VHI, VREF, AVDD, and VDD). Test points throughout the board allow users to measure and verify these voltages. The AVDD and VDD outputs are connected to the LDO regulators' feedback pins through adjustable voltage dividers. According to the TPS745 datasheet, the feedback pin is regulated to 0.55 V [3]. By tuning the potentiometer—configured as a variable resistor (0–10 kΩ) with 3600 degrees of rotation [4]—the output voltage can be finely adjusted using the standard LDO equation.

Additional design considerations enhance board flexibility and integrity. Jumper-configurable headers allow selective power isolation or current measurement for each

rail. Bypass capacitors are also placed near each IC's supply pins to suppress high-frequency noise and voltage spikes, supporting stable operation of sensitive circuitry.

B. ADC

The ADC chip on the board supports six independent analog input channels, each corresponding to a separate internal circuit. For this design, analog signals can be routed to the ADC through either a male pin header compatible with the Analog Discovery board or a mini BNC connector for direct connection to a function generator. To minimize noise coupling from unused channels, a dedicated male header is provided that allows users to ground any unused ADC inputs using jumpers. Additionally, each analog input passes through an on-board low-pass filter to suppress high-frequency noise sent to the chip.

The ADC is intended to be swapped between tests, allowing different chips to be evaluated on the same PCB. To support this, the board includes a socket interface that connects the QFN-32 package to a DIP-32 footprint on the board. The socket, shown in Figure 4, secures the chip in place without solder, enabling easy removal and replacement between tests. For a more permanent setup, the board also includes a solderable footprint directly beneath the socket, allowing a chip to be soldered in place if needed.

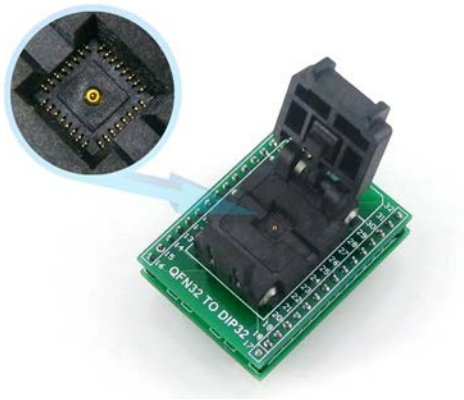


Fig. 4. QFN-32 to DIP-32 Socket

C. Digital Section

The digital circuitry on the PCB includes three key integrated circuits: a buffer, a NOR gate, and a D flip-flop. All digital signals—such as the ADC's digital outputs, clock signals from the Digital Discovery, and the reset pulse—are routed through the buffer. This design isolates the signal source from downstream components and improves signal integrity. To further optimize performance, each active buffer input is paired with a 22 Ω series resistor for impedance matching. Unused inputs are tied to ground, while unused outputs are left floating to avoid potential shorts due to crosstalk.

According to the buffer's datasheet [6] and the group's simulations, its switching speed is sufficient to handle clock frequencies up to 50 MHz, meeting the timing requirements of this board.

The D flip-flop and NOR gate ICs form a circuit that shapes the reset pulse. The team was worried the Digital Discovery would be limited in its ability to generate short-duration pulses directly, so this circuit ensures a reliable reset signal with a duration of precisely half a clock cycle (5 ns for a 50 MHz clock). It operates using two inputs: the reset pulse and the 50 MHz clock. Figure 5 illustrates the logic arrangement of the flip-flop and NOR gate, while Figure 6 shows the corresponding timing diagram. As with the buffer, all unused logic inputs are grounded, and unused outputs are left floating to protect the ICs and prevent erratic behavior.

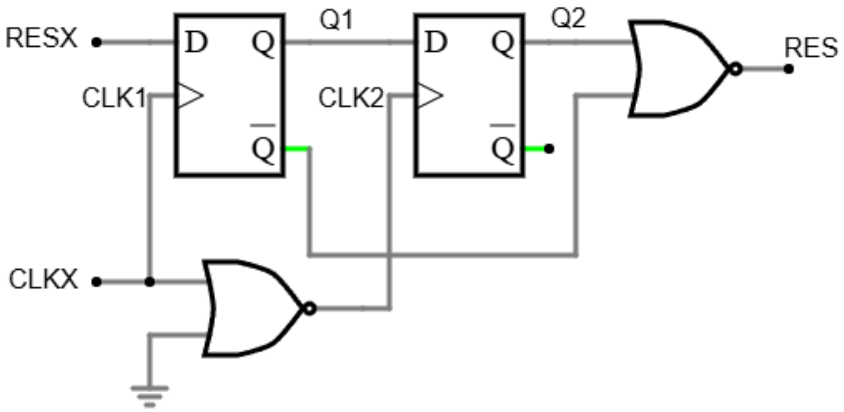


Fig. 5. Reset pulse circuit schematic

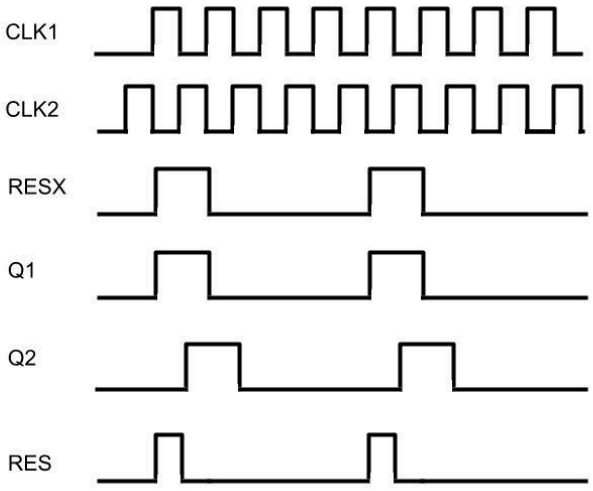


Fig. 6. Timing diagram for the reset line

D. Bill of Materials

Table II displays the bill of materials for the PCB with the reference designators for each part along with the part description and information. Throughout the creation of the schematic, parts were selected with consideration for their size and placement on the board with a bias towards cost effective options.

TABLE II

Bill of Materials

Qty.	Reference Designators	Description	Manufacturer	Manufacturer Part No.
1	ADC1	Custom ADC Chip	N/A	N/A
2	ADC2	DIP-32 Header for Socket	Adam Tech	PH1-16-UA
16	C1-C3, C8, C9, C11, C13, C15, C23, C25, C27, C29, C31, C33, C35, C36	4.7 UF TANT CAP 1206	KEMET	T491A475M016AT
15	C4-C7, C10, C12, C14, C16, C24, C26, C28, C30, C32, C34, C37	100 NF CER CAP 0603	YAGEO	CC0603KRX5R8BB104
6	C17-C22	100 PF CER CAP 0603	Murata Electronics	GRM1885C1H101JA01D
2	J1, J11	1x02_P2.5mm Male Header	Adam Tech	PH1-02-UA
2	J2, J4	1x07_P2.5mm Male Header	Adam Tech	PH1-07-UA
1	J3	1x09_P2.5mm Male Header	Adam Tech	PH1-09-UA
1	J5	2x03_P2.5mm Male Header	Harwin Inc.	M20-9980346
2	J6, J7	Mini BNC Connector	TE Connectivity AMP Connectors	1274571-1
3	J8, J9, J10	2x07_P2.5mm Male Header	Molex	0010897140
2	J12, J13	2x02_P2.5mm Male Header	TE Connectivity AMP Connectors	87227-2
2	L1, L2	Ferrite Bead 120Ohm	Murata Electronics	BLM18PG121SN1D
9	R1, R4, R7, R10-R15	1k RES 0603	YAGEO	RC0603FR-071KL
5	R2, R5, R6, R8, R31	POT 10K OHM	Bourns Inc.	PV37W103C01B00
4	R3, R9, R30, R32	4.7k RES 0603	Panasonic	ERJ-3EKF4701V

14	R16-R29	22 RES 0603	YAGEO	RC0603FR-0722RL
2	U1, U4	IC REG LIN POS ADJ 500MA 6WSON	Texas Instruments	TPS74501PDRVR
2	U2, U3	IC OPAMP VFB 1 CIRCUIT SC70-6	Analog Devices Inc.	ADA4807-1AKSZ-R7
1	U5	IC FF D-TYPE DUAL 1BIT 14SOIC	Texas Instruments	SN74HC74DR
1	U6	IC GATE NOR 4CH 2-INP 14SOIC	Texas Instruments	SN74AHC02PWR
2	U7, U8	8-BIT BUFFER/DRIVER	Texas Instruments	SN74LVC245APWR

III. BOARD SETUP & TEST

A. Board Assembly & Headers

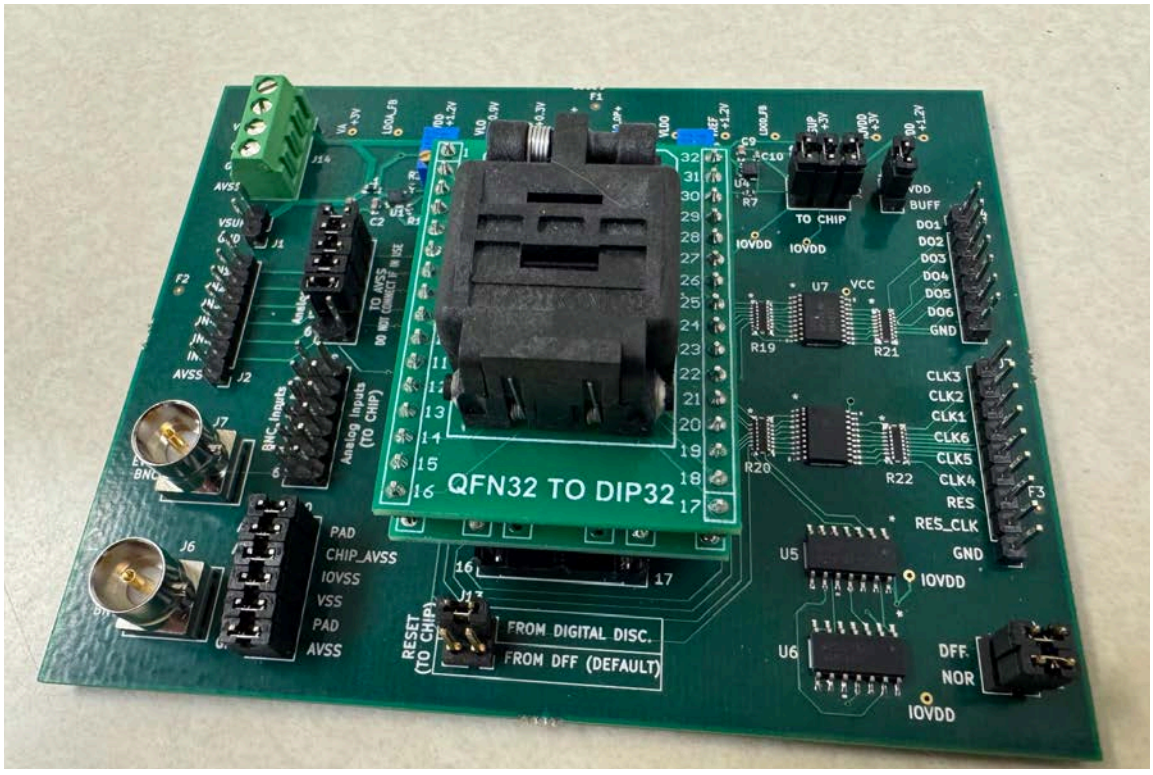
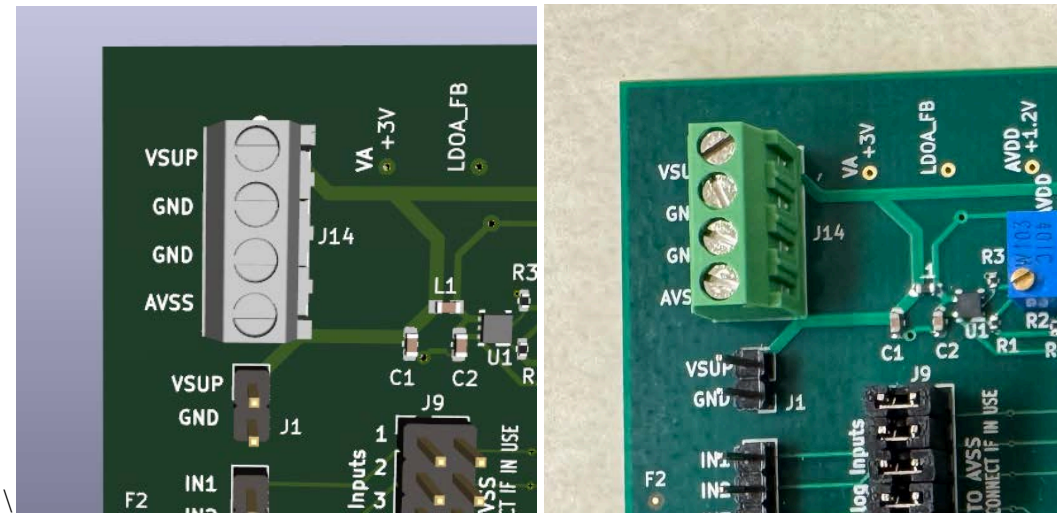


Fig. 7. Fully Assembled Evaluation Board

Figure 7 shows the fully assembled evaluation PCB, including the socket and jumper configurations necessary for testing. Proper setup of the headers and connectors is essential for powering the board and interfacing with the ADC chip.

The PCB supports two options for supplying the required +3 V input voltage: through the male header at J1 or the 4-pin terminal block at J14, as highlighted in Figure 8. The male headers are intended for direct connection to the Analog Discovery or Digital Discovery power pins (V+ for Analog Discovery, VIO for Digital Discovery), while the terminal block provides the flexibility to power the board from an external bench supply.

Throughout the board, GND refers to the digital ground and AVSS is reserved for the analog ground domain. This difference is important when connecting test equipment or troubleshooting to ensure the correct ground reference is used in each test.



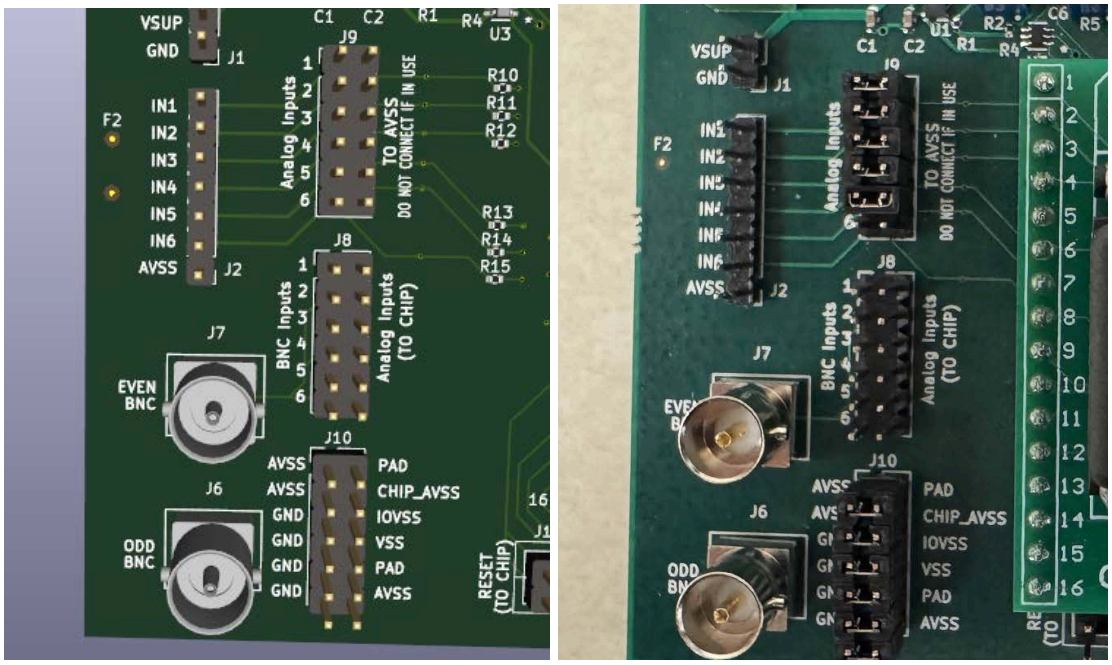
(a) (b)

Fig. 8. Board Power Connectors (a) 3D Rendering (b) Actual Board

Analog signals are routed to the board through headers J2, J6, J7, J8, and J9, as shown in Figure 9. Header J2 provides a row of male pins compatible with the Analog Discovery's waveform generator. The adjacent silkscreen labels indicate which ADC input each pin connects to. Alternatively, header J9—a 2×6 male header—offers an additional set of analog input connections. The left column of J9 carries the analog input signals, while the right column is tied to AVSS (analog ground).

J9 enables grounding of unused analog inputs: placing a jumper across a row connects the input to AVSS, which helps reduce noise coupling from floating pins. Figure 8b shows a typical configuration, where all analog inputs are grounded except for Input #6. This example setup is used when testing the ADC circuit #6. It is essential to avoid grounding an input when a signal is being applied to avoid shorting the signal to ground.

Analog signals can also be applied through the board's mini BNC connectors. Connector J6 routes signals to the odd-numbered analog inputs, while J7 connects to the even-numbered inputs. When using the BNC interface, the waveform generator must be connected to the appropriate connector, and a jumper must be placed on header J8 in the row corresponding to the desired input channel.

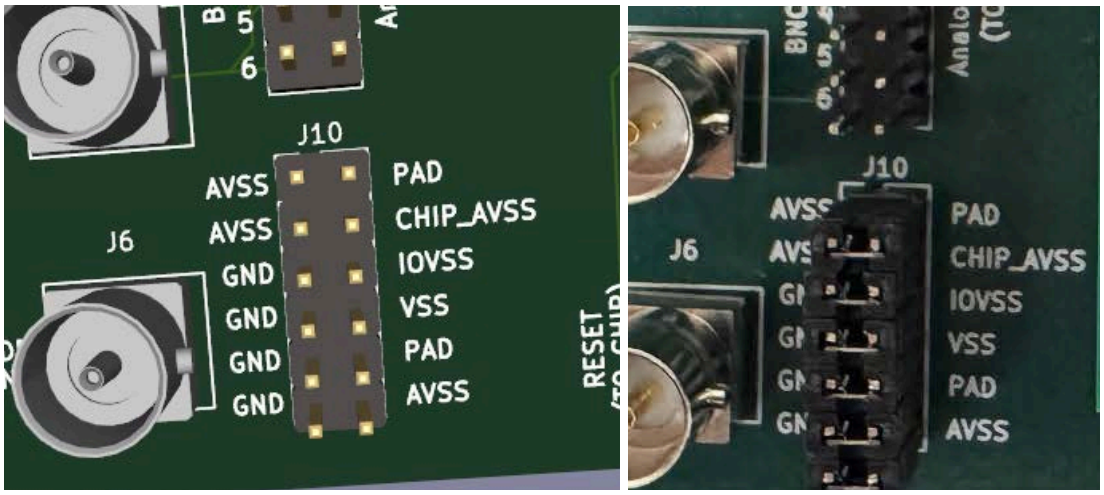


(a) (b)

Fig. 9. Board Analog Signal Connectors (a) 3D Rendering (b) Actual Board

Header J10 is used to ensure that specific pins on the chip are properly grounded, as shown in Figure 10. In a typical setup, each row of this header should include a jumper to connect the corresponding chip pins to their appropriate ground.

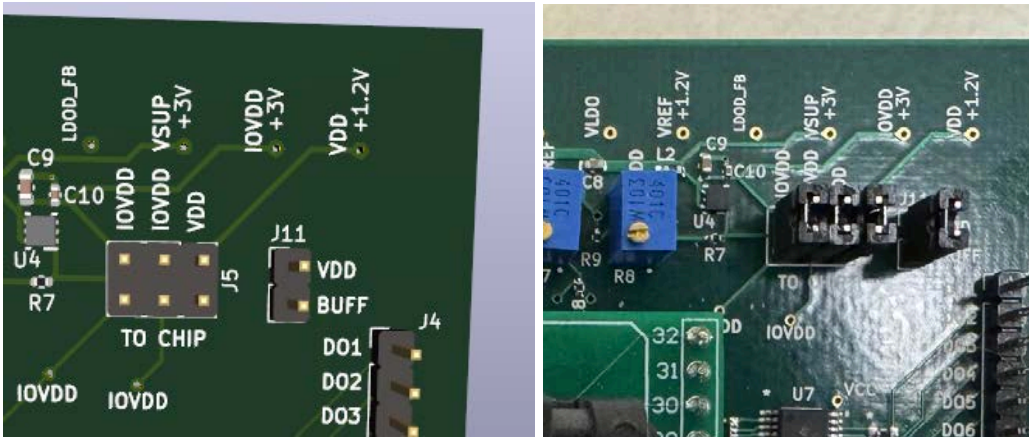
The bottom row of J10 controls the connection between the analog and digital grounds. Removing this jumper electrically isolates the two ground domains, while inserting it ties them together.



(a) (b)

Fig. 10. Board GND Connectors (a) 3D Rendering (b) Actual Board

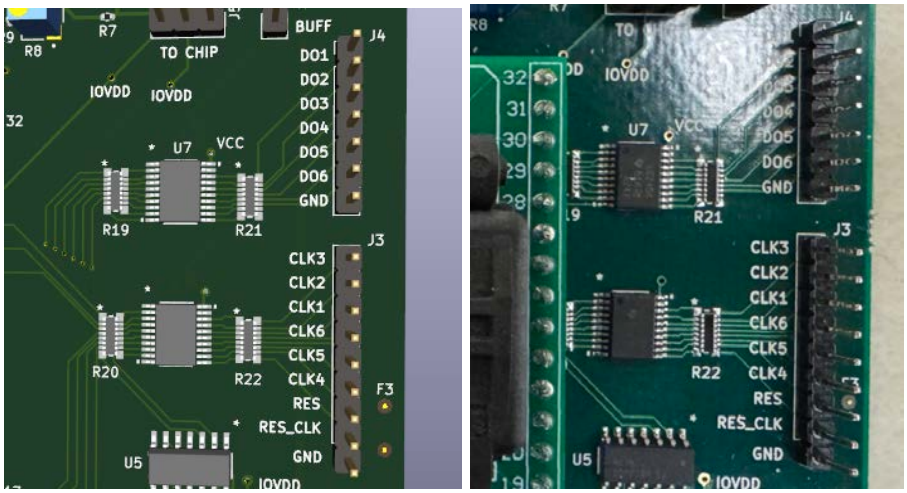
Headers J5, J11, and J12 control which ICs on the board receive supply voltage, as shown in Figure 11. For the ADC's digital circuitry to receive the correct supply voltage, jumpers must be placed vertically across all three columns of J5. Placing a jumper on J11 connects the 3V supply to power the buffers on the board. Similarly, inserting jumpers horizontally on J12 powers the D flip-flop and NOR gate ICs. These jumpers give the user control over which components receive power, allowing for current measurements and power management during testing.



(a) (b)

Fig. 11. Digital Power Supply Connectors (a) 3D Rendering (b) Actual Board

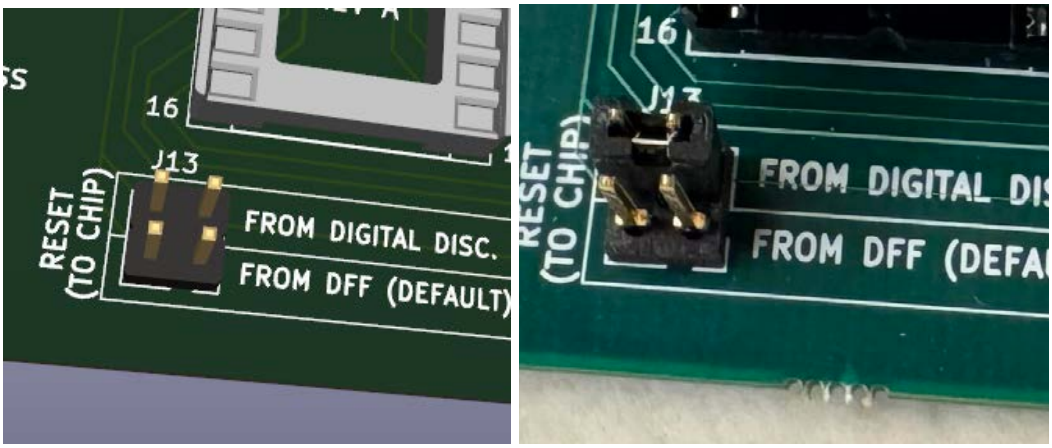
Headers J3 and J4 are used to connect the PCB to the source of digital input and output signals, as shown in Figure 12. Header J3 receives the clock and reset signal lines from the Discovery Boards, routing them to the buffer and their respective pins on the ADC. Header J4 connects the Discovery Boards to the digital output of the chip, allowing the user to read the output signals. The silkscreen labels on the board clearly indicate which pin corresponds to each clock signal and digital output (1-6).



(a) (b)

Fig. 12. Digital Signal Lines (a) 3D Rendering (b) Actual Board

Finally, header J13 allows the user to select which signal line is routed to the reset pin on the ADC, as shown in Figure 13. In a typical setup, the top row of the header should be jumpered to directly connect the reset pin to the signal from the Discovery Boards. Although the original design intended for the reset signal to pass through the on-board digital circuitry, connecting it directly to the Discovery Board ensures more precise timing in the output data file for the post-processing steps.



(a) (b)

Fig. 13. Digital Signal Lines (a) 3D Rendering (b) Actual Board

B. Initial Board Functionality Checks

Before integrating the chip into the evaluation board, several preliminary checks must be performed to verify the board's functionality and ensure it is free from manufacturing defects. These tests are crucial to prevent any potential damage to the chip upon insertion. By conducting these checks after the board's fabrication, any issues can be identified and addressed before the chip is tested.

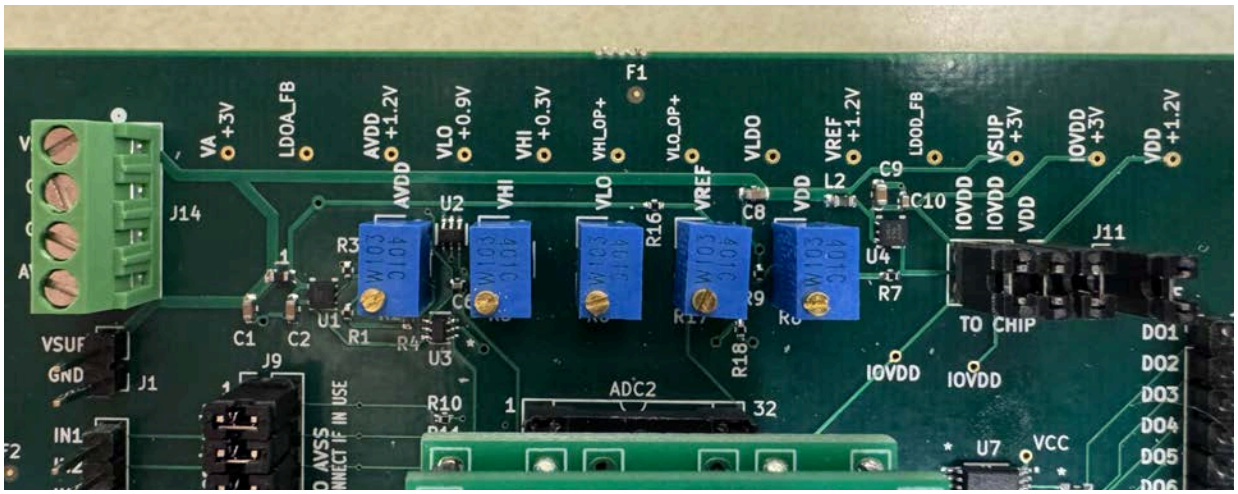


Fig. 14. On-Board Test Points & Potentiometers

The first step involves connecting the +3V supply to the PCB and verifying the proper voltages at each test point. Figure 14 displays the board's several test points located at the top of the board. The silkscreen near each critical test point displays the nominal voltage of what the test point should be at. A multimeter is used to measure the voltage at the VA test point to confirm that the board is properly receiving the +3V input. Once the supply is confirmed to be operational, the power distribution throughout the board can be checked. This includes ensuring that the various ICs, such as the buffer, are receiving the necessary voltages (VSUP & IOVDD). Potentiometers are then adjusted to ensure that the VDD, AVDD, VHI, VLO, and VREF points are set to their respective nominal values. Additionally, current measurements are taken to confirm that the board is drawing a safe and steady current.

Once the power integrity is confirmed, the next step is to assess signal integrity across the board. Analog signals are passed through the analog inputs, and an oscilloscope is used to verify that the signals reach their designated pins without distortion or interference. A similar process is applied to the digital signals, ensuring that clock signals are transmitted to the chip and that the output signals from the chip are correctly routed to the output pins. The reset pulse functionality is also verified to ensure proper operation of the digital circuitry. Readings are taken across multiple pins to confirm that there is no cross-talk between signal lines and that no unintended interactions occur between them. These tests ensure that the board is functioning as expected and that any issues found during chip testing can be attributed to the chip rather than the board design.

Figure 15 shows the pinout of the socket in relation to the ADC pins, indicating which signals should be checked before the chip is inserted into the socket. The team ensures that all

pins intended for grounding are properly connected to ground. Additionally, the team verified that the correct reference voltages are present up to the socket pins.

Fig. 15. Board Socket Pinout & Pin Description

Table III below shows a general check list of tests to perform before any chip is placed under test. These tests ensure the board is safe to accept the chip and minimizes faulty tests that are the result of the board.

TABLE III

Initial Board Testing Checklist

Analysis Stage:	Board Category:	Check Items:
Step 1: Verify Connections/Isolations on the Board	PWR	☐ Verify GND is connected throughout the board ☐ Verify AVSS is connected throughout the board ☐ Verify GND/AVSS connected when jumper added

		☐ Add jumpers to J10 and verify socket pins connect to GND/AVSS ☐ Verify continuity between power connections ☐ Verify isolation between all power test points and other power test points of different voltage ☐ Verify isolation between all power test points and GND/AVSS test points
	Analog	☐ Verify continuity from analog input pins at J2 to ADC socket ☐ Verify each analog input is isolated from one another ☐ Plug in jumpers in J9. Verify the analog inputs with jumpers get connected to AVSS while other analog inputs do not ☐ Plug in jumpers to J8. Verify continuity between BNC connectors and analog input pins in the socket
	Digital	☐ Verify all digital inputs have continuity to socket ☐ Verify all digital outputs have continuity to socket *Note: Unlikely to get good results from this check due to the buffer between all digital signal lines going from headers to the socket.
Step 2: Power Up the Board	PWR	Equipment: 1. PCB 2. Analog Discovery Board or DC power supply Checklist: ☐ Ensure NO jumper is plugged into the board. ☐ Plug in a +3V source into the PCB either through male headers or terminal block. For typical setup, the +3V VIO pin from the Digital Discovery is used to power. Before performing any tests, verify there is no damage inflicted on the board. No area of the board should heat up significantly with the introduction of the power supply. ☐ Use a voltmeter to verify 3V is being supplied to the board. Use test point VA to verify the voltage reading. ☐ Use a voltmeter to verify 3V is being supplied to IOVDD pins across the board's jumpers ☐ Tune potentiometer "AVDD" until AVDD test

		point is +1.2V. Verify voltage reading at the socket pin. ☐ Tune potentiometer “VHI” until VHI test point is +0.9V. Verify voltage reading at the socket pin. ☐ Tune potentiometer “VLO” until VLO test point is +0.3V. Verify voltage reading at the socket pin. ☐ Tune potentiometer “VREF” until VREF test point is +1.2V. Verify voltage reading at the socket pin. ☐ Tune potentiometer “VDD” until VDD test point is +1.2V. Verify voltage reading at the socket pin. ☐ Ensure each power supply going to an IC (Buffer, D flip-flop, NOR gate) is supplying an adequate 3V ☐ Plug in jumpers to power ICs and verify IC receives the correct +3V

C. Signal Analysis & Data Processing

The next objective of evaluation is to assess the performance characteristics of the six circuits. This involves measuring and processing the digital output in a controlled manner and performing the necessary post-processing steps to achieve a desired output reading. With the design of the delta-sigma ADC circuits, the output voltage is formulated through post-processing in software. A simple Python script can be used to take the output data and translate it into a tangible analog voltage value that can be compared to the input.

The main metric of each circuit’s performance is the accuracy of the output value to the input. There are several key tests to be performed on each of the six circuits on the chip:

- **Transfer Characteristics:** Plot the transfer function for the chip’s response to specific DC inputs to determine the linearity of its output relative to the input.

- **Variance/Distribution:** Check the variance of many readings with the same DC input and assess whether the distribution appears normal with a mean at the expected value.
- **Memory Effects:** Investigate the effects of switching the input value to assess any memory effects in the chip's behavior (i.e. does the changing the analog input a certain way affect the new reading).
- **ADC Resolution:** Examine how changing the number of clock cycles between reset pulses affects the output resolution to compare it with expectations.
- **Clock Speed:** Test the impact of varying the clock speed on the chip performance.

IV. CHIP TESTING RESULTS & ANALYSIS

A. DC Measurements

Upon inserting the chip into the socket and powering the board, the reference voltages were measured at the designated test points. All reference voltages—VHI, VLO, VREF, VDD, and IOVDD—remained stable and unchanged with the chip installed. No indications of chip malfunction, such as excessive heating or physical damage, were observed.

The current draw of the board was also assessed to estimate the power consumption of the chip. With the chip removed, the board drew approximately 23.5 mA, as measured by a handheld multimeter. Upon inserting the chip, the current draw increased to approximately 46.0 mA. This suggests that the chip itself draws roughly 22.5 mA, which is consistent with the expected current consumption.

In addition to the DC measurements, the VLDO test point was checked using a multimeter. The VLDO pin, connected to the ADC's on-chip LDO, provided an output of approximately +1.199 V, which is within close tolerance of the desired +1.2 V, confirming that the LDO circuit is functioning as intended.

B. Transfer Characteristics

The Analog Discovery was used to generate the ADC's analog inputs, reset pulse, clock inputs, power supplies, and capture the ADC's output bitstream. A script was created in a *WaveForms* workspace to automate the tests and a *Python* script was used to plot the results. The code can be found on the EE628 github. A detailed testing procedure can be found in *Appendix A* to assist others in recreating the tests and using the scripts to automate the equipment.

1. Linear Sweep

The analog input voltage was swept from 0V to 1.2V in 0.05V increments. This input voltage was applied to each team's input pin. First the analog input was applied to a Team's pin, then a reset pulse was applied to ensure the IDSM integrators were cleared out and no memory of any previous measurements was present. Then a clock signal was applied to the corresponding team's clock input pin. The clock was set to 50MHz, which is the fastest the ADC was designed to operate at. The Analog Discovery's logic analyzer was used to sample at 100MHz at the corresponding team's output in order to capture a sample twice per clock cycle. 5000 samples were collected, allowing us to test different levels of precision during post processing (indicated by different values of N on the plot). The notable results of this test will be discussed below.

The results of performing the linear sweep test on Team 6 can be seen in Figure 16, and Team 2 in Figure 17. An ideal plot would look like a straight linear line that saturates somewhere around 0.3V (VLO) and 0.9V (VHI). The results measured for Team 6 look similar to the ideal depiction, indicating Team 6's ADC is working as expected. The results measured for Team 2 also look similar to the ideal depiction, with a little more noise. We observed the transfer characteristic became closer to ideal linear as N increased, which corresponds to the level of

precision for each ADC reading, an expected result. Similar results were found when the linear sweep test was performed on Team 3 and 5's input pins.

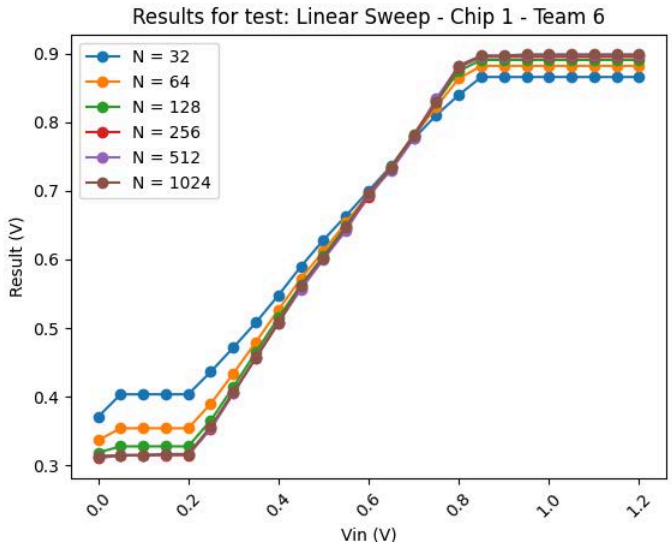


Fig. 16. Plot For Team 6 Linear Sweep Results

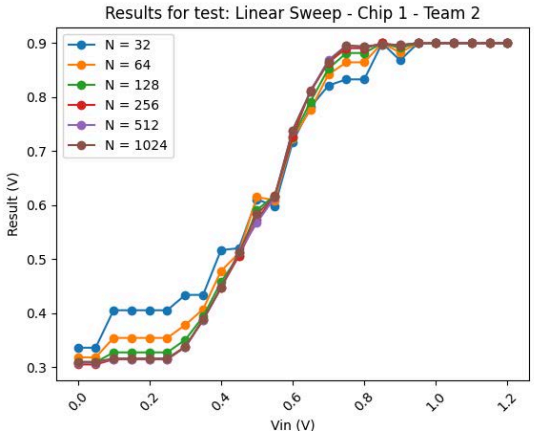


Fig. 17. Plot For Team 2 Linear Sweep Results

Team 1's results can be seen in Figure 18. The ADC produced the same output (0.9V), regardless of its input voltage or the value of N. This behavior was observed for every chip tested, which suggests the faulty results are due to a design error and not a manufacturing error.

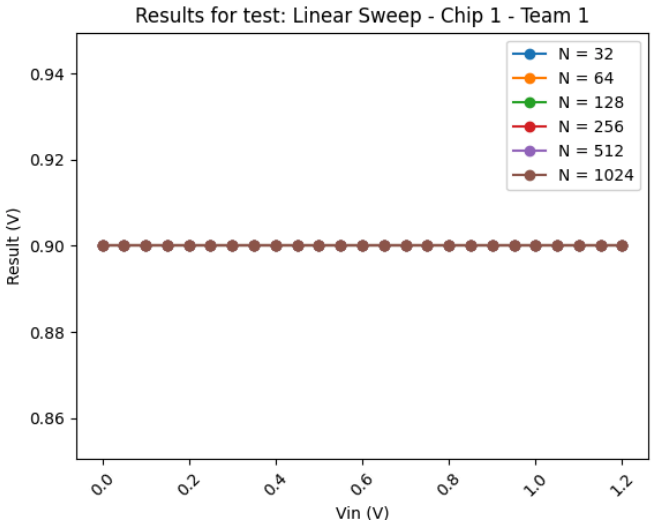


Fig. 18. Plot For Team 1 Linear Sweep Results

Team 4's results can be seen in Figure 19, which exhibited a strange constant effect that varied between 0.6V and 0.8V, depending on the value of N used. This behavior was observed for every test done, but only from chip 1. Team 4's results looked close to linear for the other chips tested, making chip 1 an outlier, likely due to a manufacturing error or a physical error made during testing that damaged the chip.

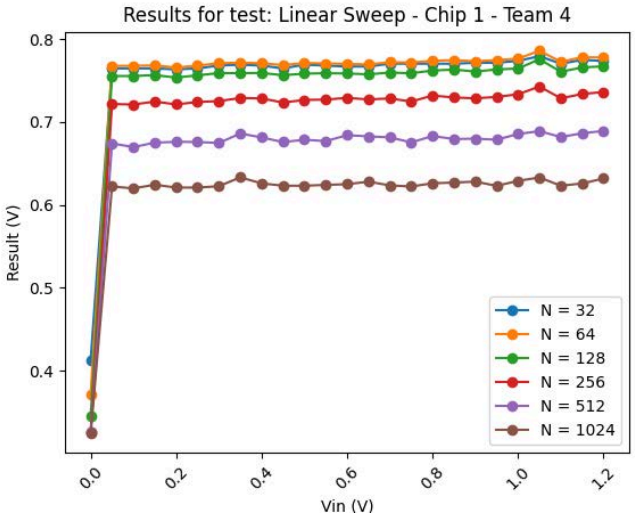


Fig. 19. Plot For Team 4 Linear Sweep Results

In an exploratory effort to attempt to make the transfer characteristic closer to ideal linearity, the first few samples were skipped during post processing on the same output data for each ADC. The theory behind this experiment came from the idea that errors in the first few samples have a larger effect on the output voltage, due to the double cumulative sum operation used in the output equation. The results of this experiment did not lead to any significant changes and the graphs looked identical to the ones where no samples were skipped.

The clock speed was slowed down to test its effect on the transfer characteristic's linearity. The clock was set to 10MHz and the output was sampled at 20MHz in order to remain consistent with the previous experiment which sampled twice per clock cycle. This change did have a significant effect on the linearity. Results for Team 6 and 2 can be seen in Figure 20 and Figure 21 below. The effects of non-idealities in the transistor cells, chip's layout, board's layout, board components, and measuring devices, and the negative effects of the gaps between simulated models used in design, and the actual manufactured transistor cells are exacerbated at higher frequencies, which explains why the results are closer to ideal at lower frequencies. The value of N also has a lessened effect on the linearity of the transfer characteristic at lower clock speeds.

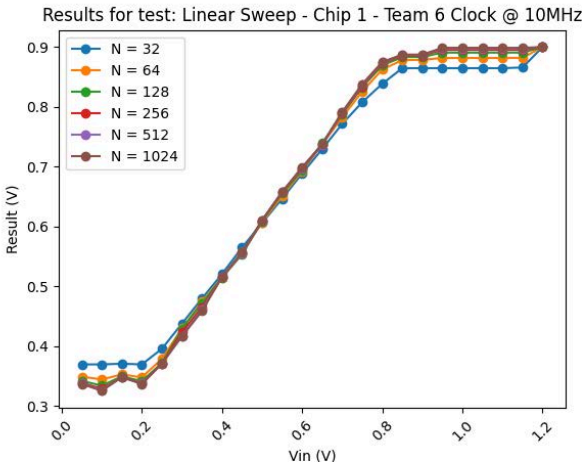


Fig. 20. Plot For Team 6 Linear Sweep Results @ 10MHz

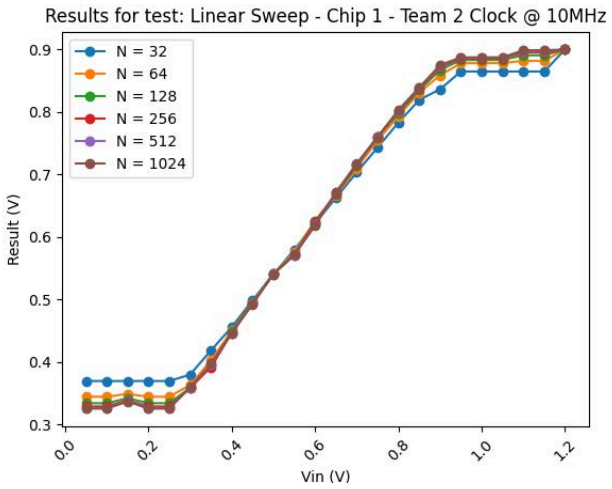


Fig. 21. Plot For Team 2 Linear Sweep Results @ 10MHz

2. Memory Effects

The ADC has internal capacitor based integrators that are designed to reset and drain all their charge when a logic high voltage is applied to the reset pin on the chip. The effects of any previous voltage conversion should not affect the current conversion allowing the ADC to treat each conversion as independent from one another.

To test this functionality, two separate input voltages that varied by 200mV were applied to the ADC one after the other, to verify there was no memory of the previous conversion. The clock was set to 50MHz and 5000 samples were taken to allow for enough to post process multiple precision levels. A 0.5V was applied to the input of Team 6 20 times, then 0.7V was applied to the same input 20 more times, and the results were plotted in Figure 22. The ideal outcome of this test would look like a step function, with the lower level at 0.5V and the higher level at 0.7V.

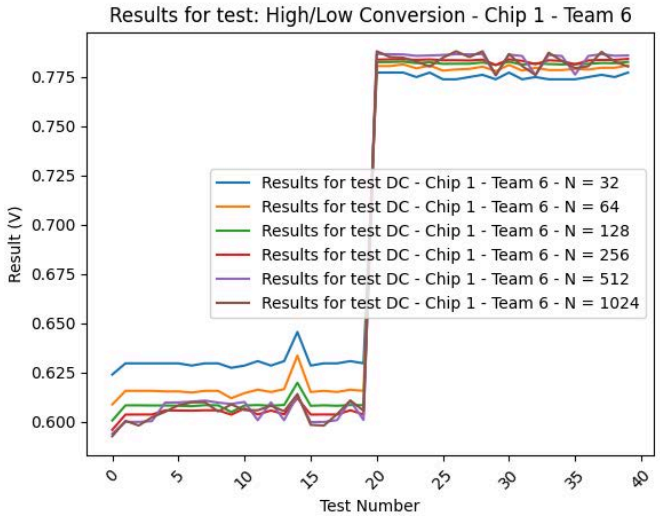


Fig. 22. Plot for Team 6 Memory Test

The plotted result does resemble the shape of a step function with acceptable levels of noise. This result implies the ADC reset functionality works as intended as there is no sign of any memory effects. It is notable that the ADC reads the 0.5V input as around 0.6V, but the 0.7V input as around 0.775V. Assuming the Analog Discovery is applying accurate voltages, this result showcases the ADCs positive bias for lower voltages that decreases for voltages that approach its saturation level. Although the bias magnitude varies slightly by approximately 100mV, the other teams showcased similar results as Team 6 with no significant differences.

The second test to verify the ADC has no memory effects was to perform the linear sweep test but in the opposite direction. Instead of incrementing 0.05V from 0V to 1.2V, the voltage was decremented 0.05V from 1.2V to 0V. This descending pattern was done right after the initial ascending pattern, in an attempt to give the ADC some data to remember. If memory effects are in fact present, then the descending pattern would not have the same general shape as the ascending pattern. The results of performing this test on the Team 6 input pin in Figure 23 show another plot with saturation regions and linear transfer characteristics in the operating

region, which are very similar to the ascending pattern's result in Figure 16 which reinforces the idea there are no memory effects present in the ADC. The same tests were performed on the other teams and very similar results were obtained.

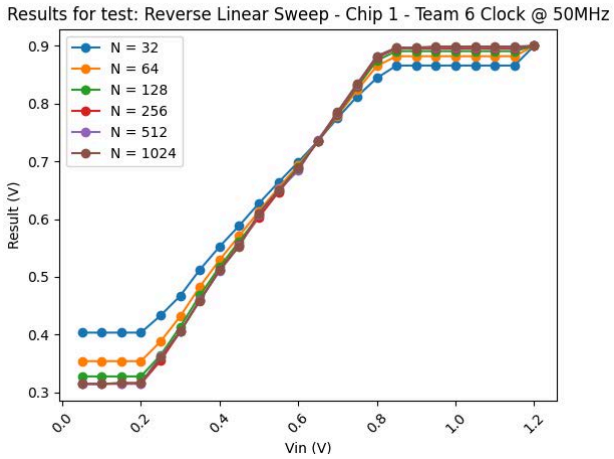


Fig. 23. Plot For Team 6 Reverse Linear Sweep Test

C. Standard Deviation of the Data

In addition to characterizing the transfer function of each circuit, the team sought to evaluate the variance of the measurements. To accomplish this, the input voltage to the circuit was maintained at a constant value using the Analog Discovery. The Digital Discovery supplied the clock and reset signals, allowing for the sampling of thousands of consecutive measurements at the specified input voltage. A post-processing script was used to process the digital output and calculate the corresponding analog voltage. The distribution of these measurements was then analyzed to determine the variance.

This procedure was repeated for each input voltage (Vin) in the range of 0V to 1.2V, with increments of 0.1V. The figure below displays a sample distribution for circuit #6, collected with 128 clock cycles between each reset pulse (N = 128), an input voltage of 600 mV, and a clock speed of 50 MHz.

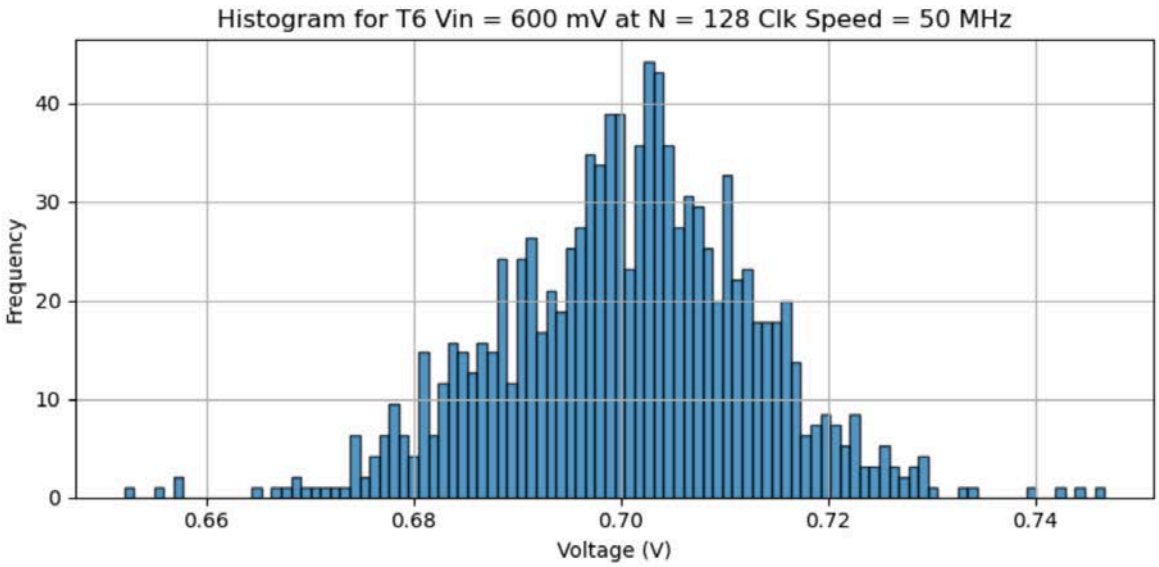


Fig. 24. Histogram of Measured Output Values from ADC Circuit #6

Based on an analysis of the data, the distribution showed a standard deviation of approximately 12.3 mV, and each circuit at this input voltage experienced a similar standard deviation. While it may be possible for this variance to be attributed to noise, the relatively large spread of output values suggests that the chip is encountering a significant degree of fluctuation in its output. However, there was an interesting result when the clock speed was reduced down to 2 MHz. The figure below displays the distribution with the same exact experiment setup but with the only change being the reduced clock speed.

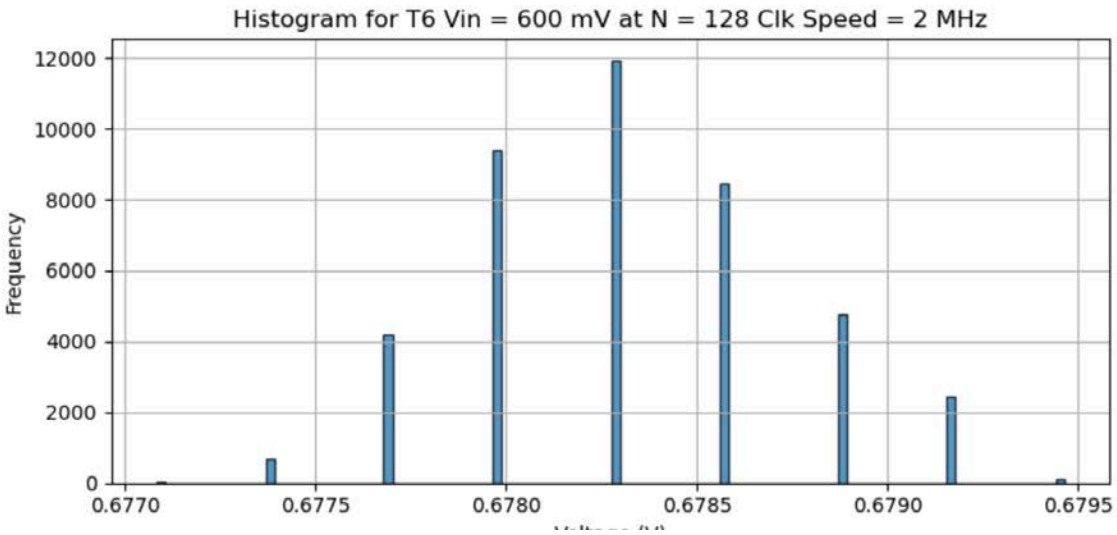


Fig. 25. Histogram of Measured Output Values from ADC Circuit #6 with Reduced Clock Speed

The distribution of output values at the reduced clock speed exhibited a standard deviation of approximately 0.42 mV, representing a significant reduction in variation compared to the previous test. Similarly, the other circuits on the chip experienced a comparable decrease in standard deviation, with most values falling below 0.5 mV. This notable improvement can likely be attributed to the more relaxed timing constraints and the longer clock cycles, which provide greater tolerance for the switching behavior of the digital circuitry. The results of this reduced clock speed experiment demonstrate a much lower variance, aligning more closely with the desired performance characteristics of the chip.

Table IV below presents the statistics for the data collected across 7,000 consecutive measurements for each test case, illustrating how the standard deviation decreases with the reduced clock speed.

TABLE IV

50MHz vs 2MHz Clock Speed on Accuracy & Deviation of ADC Outputs

Circuit #	Num Clk Cycles Between Reset (N)	Vin (mV)	Clock Speed (MHz)	Mean (mV)	Standard Deviation (mV)
1	128	600	50	N/A	N/A
1	128	600	2	N/A	N/A
2	128	600	50	610.16	4.53
2	128	600	2	605.95	**0.51**
3	128	600	50	655.72	9.10
3	128	600	2	616.72	**0.42**
4	128	600	50	708.56	9.50
4	128	600	2	631.10	**0.31**
5	128	600	50	627.57	4.29
5	128	600	2	618.78	**0.39**
6	128	600	50	700.68	12.31
6	128	600	2	678.32	**0.42**

While the results with the reduced clock speed are promising, there is still a discrepancy between the current standard deviation and the ideal standard deviation for the given setup. Increasing the value of N led to a reduction in the standard deviation, but the decrease was not as significant as expected with the given increase in N. This suggests there are other factors that are affecting the variation in readings being measured from the ADC.

One potential factor of concern is the isolation between the analog and digital grounds on the board. To maintain signal integrity, it is crucial that these two grounds remain isolated to prevent interference. To test this, the jumper connecting GND and AVSS was removed, ensuring complete separation between the Analog and Digital Discovery boards.

Despite this modification, the variation in the output results did not improve. The figures below illustrate the distribution of the recorded values for one of the circuits, comparing the scenarios where the grounds were isolated versus when they were connected. The only difference between the two setups was the presence or absence of the jumper connecting GND and AVSS. Interestingly, isolating the grounds resulted in an increase in variation, which is an unexpected outcome. However, this test serves to rule out the potential contamination of the analog and digital signals due to ground mixing. Further investigation will be needed to explore other possible sources of error.

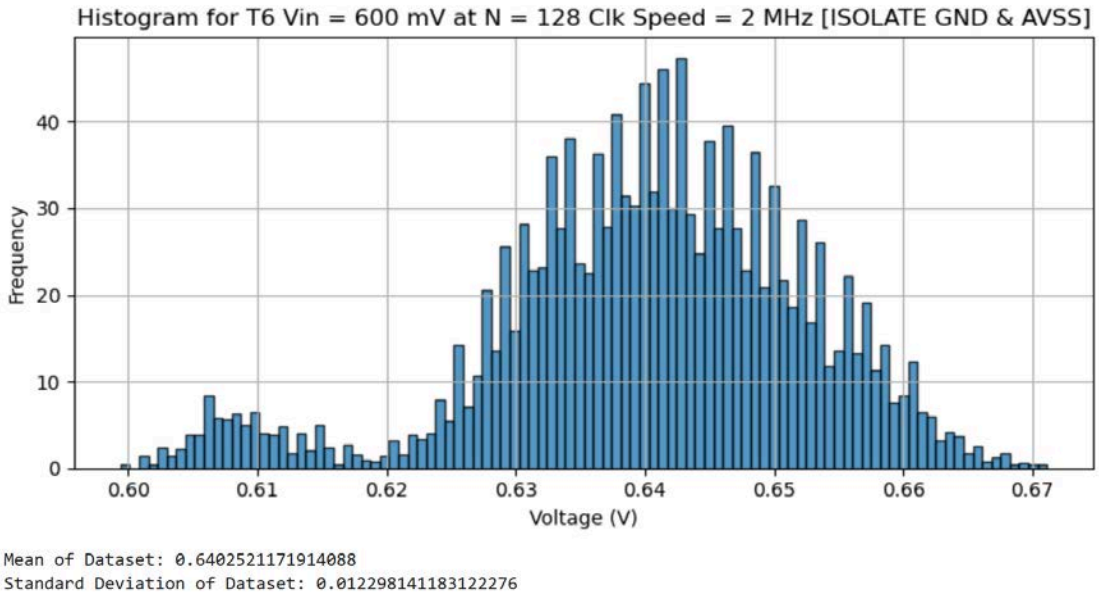


Fig. 26. Distribution of Measured Outputs with GND & AVSS Isolated

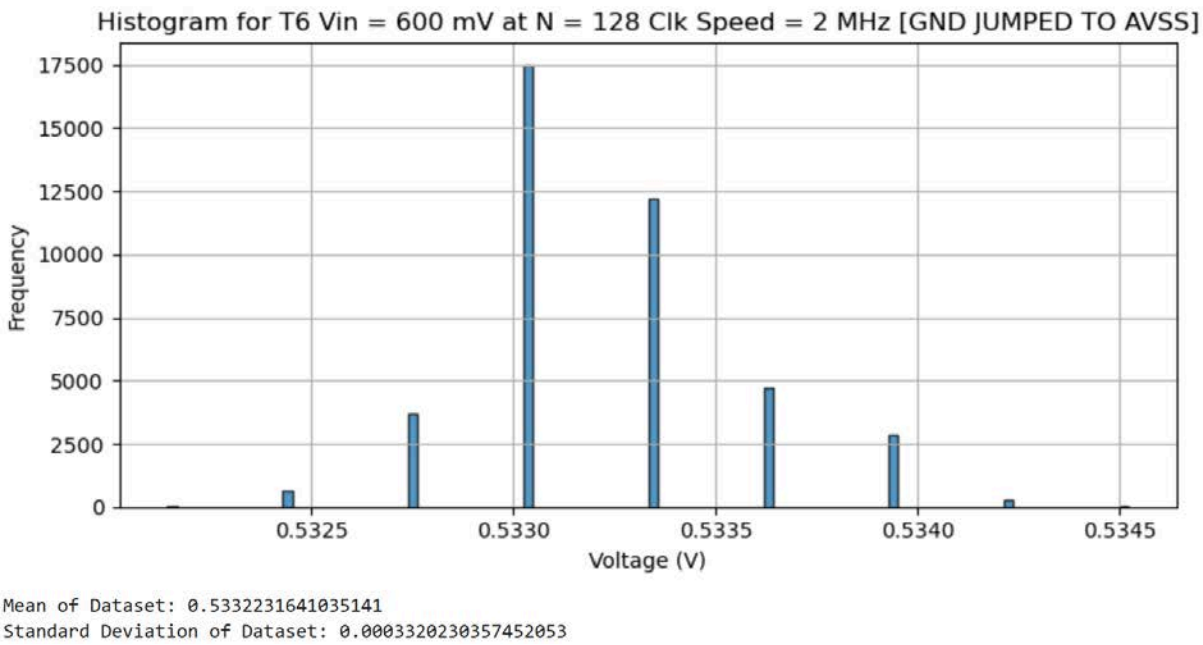


Fig. 27. Distribution of Measured Outputs with GND & AVSS Connected

V. DISCUSSION & FUTURE TESTING

A key observation from the test results is the impact of clock speed on the performance of the chip's six circuits. Across all tests, a slower clock speed improved the accuracy of the readings and reduced the variation between consecutive measurements. This suggests that while the chip is capable of producing accurate measurements, the clock speed is a significant factor influencing its performance. Ideally, the clock speed should not have a large effect on the output, and the lower clock speed reduces the ADC's ability to take real-time measurements efficiently.

Further investigation is needed to identify the main causes of the observed deviation in the measured values. Although a preliminary test was conducted to assess the effects of isolating the analog and digital grounds, there are additional factors that may contribute to the large standard deviation observed. One potential source of error is noise in the analog supplies driving the input signals. To address this, more stable analog supplies could be tested with the board.

One approach would be to use regular batteries, create a voltage divider, and route the resulting stable output to each of the analog inputs. This would help eliminate variations due to fluctuating power sources, providing a more consistent input signal for the chip.

Moreover, additional testing could be carried out to further improve the accuracy of the chip's readings. While each circuit under test exhibits a generally linear transfer characteristic, further analysis is required to investigate any anomalies that may arise within the circuit's operational range. Although the transfer characteristic remains linear, each measured output voltage shows a consistent offset from the expected value. Further work could focus on aligning these output values more closely with their intended values. Alternatively, the Python post-processing script could be adjusted to account for these offsets, thus reducing the error between the measured and desired values.

VI. CONCLUSION

The evaluation board was successfully designed and implemented to test a custom-designed ADC chip, with a thorough assessment of the chip's circuits and performance. The board was carefully engineered to easily interface with the custom ADC's pinout, ensuring the integrity of both analog and digital signals routed through the system. Extra attention was given to the separation of power, analog, and digital components, minimizing potential crosstalk between signals. Additionally, the board was designed to facilitate proper interfacing with the Analog and Digital Discovery boards.

After the design and fabrication of the PCB, a comprehensive series of tests confirmed the board's basic functionality and its ability to correctly route signals. Upon integrating the chip into the evaluation board, the team successfully powered the chip and evaluated the performance

of its six circuits. The transfer characteristics were found to be approximately linear, and the variance of the measurements was characterized with constant input signals. A key finding was that clock speed had a significant impact on the accuracy and precision of the output measurements. Lowering the clock speed allowed for better fine-tuning of the chip's measurements.

Although the testing conducted so far has provided valuable insights into the chip's functionality and characteristics, further investigation is necessary to identify and mitigate sources of measurement error. Overall, the project has been successful in creating the evaluation board for the custom ADC chip and executing a robust testing plan, confirming that the chip is functioning as expected.

Appendix A: Waaveforms/Python Script Test Procedure

Required Materials: Analog Discovery (with fly wire connectors), Jumpers, ADC Chip, Test Board, Computer (Waveforms and Python installed).

Procedure:

Board Setup

The board was designed to have more than one configuration to help facilitate testing different characteristics of the ADC. Table V shows which jumpers to connect in order to recreate the board environment of the tests in *IV.B Transfer Characteristics*.

Table V Board Jumper Configuration For Test Environment Recreation

Board Reference Designator	Silkscreen Label
J10	AVSS~PAD
J10	AVSS~CHIP_AVSS
J10	GND~IOVSS
J10	GND~VSS
J10	GND~PAD
J10	GND~AVSS

J12	DFF~IOVDD
J12	NOR~IOVDD
J5	CHIP~IOVDD
J5	CHIP~IOVDD
J5	CHIP~VDD
J11	VDD~BUFF
J9	*Place jumper on every team that you are not currently testing*

Connecting Analog Discovery

Table VI shows which fly wires to connect from the Analog Discovery to the board.

Table VI Analog Discovery Flywire Connections For Test Environment Recreation

Flywire Number	Board Reference Designator	Board Header Silkscreen Label
W1	J2	*Connect this to the team you want to test*
V+	J1	VSUP

GND	J1	GND
DIO 14	J3	RES
DIO 15	J3	*Connect to the same team number as W1*
DIO 13	J4	*Connect to the same team number as W1*

Script Setup

Plug in the Analog Discovery into your computer and ensure you have Waveforms and Python installed. You should have two windows open:

1. Waveforms (ADC_test_scripts workspace), and
2. Terminal in the ADC_test_scripts directory.

You'll need to install the python dependencies which are in the requirements.txt file.
Run command *pip install -r requirements.txt* from the terminal window to quickly install them all.

Running Tests (Linear Sweep Example)

Below is an example of the workflow for using the linear sweep script. Using the scripts for the other tests follow the exact same workflow, so only the linear sweep example will be shown here.

1. After all the Analog Discovery pins are connected go to the Waveforms workspace and click the supplies tab.

2. Click Master Enable is Off, wish should turn the X into a green check mark, turning the supplies on.
3. At the top click the scripts tab. You should see three files: linear_sweep_test, high_low_test, multiple_measurements_single_value (these names also correspond to the python script file names in the ADC_test_scripts directory).
4. Click the linear_sweep_test file.
5. Scroll down to the variables chipNumber and teamNumber. Ensure they have the same values as the team and chip you're currently testing.
6. Find the filePath variable and change it so that it matches the location of the ADC_test_scripts directory on your computer.
7. Look at the top of the file and click the green play button next to the linear_sweep_test file name. This will run that script. You should see the logging at the bottom "Starting test, Vin = …". When complete the data should appear in "ADC_test_scripts/chip_#/team_#"
8. Open the linear_sweep_test.py file in your code editor of choice. Scroll down to the variables chipNumber and teamNumber and change them to the same numbers you ran the test for in the workspace.
9. Run the command *python linear_sweep_test.py*. You should see the logging start. This will process the raw data, save the voltage readings into several results files, then plot the results and save the plots in png figures.
10. Open the figure to verify the test worked properly. "chip_#/team_#/results_DC_chip-#_team-#_N-1024.png"

Archiving Results

When you want to switch tests and are done with the data, move all the chip_# directories that were generated into a separate folder (ex. archived_test_data folder), and rename the folder to something else that describes what test was done. This scheme was done to avoid advanced saving and organizational techniques were not necessary to implement when developing the scripts.

REFERENCES:

[1] Digilent, “Analog Discovery 3 Reference Manual,” 2023. https://digilent.com/reference/test-and-measurement/analog-discovery-3/reference-manual (accessed Dec 12, 2024).

[2] Digilent, “Digital Discovery Reference Manual,” 2023. https://digilent.com/reference/test-and-measurement/digital-discovery/reference-manual (accessed Dec 12, 2024).

[3] Texas Instruments, “TPS745 500-mA, High Accuracy, Adjustable LDO With Power-Good in a Small Size Package,” SBVS326A datasheet, April 2018 [Revised Dec 2018]. https://www.ti.com/lit/ds/symlink/tps745.pdf?HQS=dis-dk-null-digikeymode-dsf-pf-null-wwe&ts=1734495548592

[4] Bourns Inc., “PV37 Series – Lead Sealed Type Multiturn Trimming Potentiometer,” PV37 datasheet, March 2015. https://www.bourns.com/docs/Product-Datasheets/pv37.pdf

[5] Murata Electronics, “CHIP FERRITE BEAD for Consumer equipment & Industrial equipment BLM18PG121SN1D REFERENCE SPECIFICATION,” JENF243A datasheet. https://www.murata.com/en-us/products/productdata/8796738650142/ENFA0003.pdf

[6] Texas Instruments, “SN74ALVCH162827 20-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS,” SCES013H datasheet, July 1995 [Revised Aug 2004]. https://www.ti.com/lit/ds/symlink/sn74alvch162827.pdf?ts=1734466572573&ref_url=https%253A%252F%252Fwww.google.com%252F

[7] Analog Devices, “Evaluation Board for the 16-Bit Continuous Time Sigma-Delta ADC,” AD9261EBZ datasheet, 2009. https://www.analog.com/media/en/technical-documentation/evaluation-documentation/EVAL-AD9261EBZ.pdf

[8] K. Chesser and M. Porley, “What Are the Basic Guidelines for Layout Design of Mixed-Signal PCBs?,” *Analog.com*, 2022. https://www.analog.com/en/resources/

analog-dialogue/articles/what-are-the-basic-guidelines-for-layout-design-of-mixed-signal-pcbs.html (accessed Dec. 18, 2024).

[9] E. Robledo, “Three Principles in PCB Design,” *www.nextpcb.com*. https://www.nextpcb.com/blog/three-principles-in-pcb-design

[10] “Serpentine Routing–Function Over Form in PCB Router,” *San Francisco Circuits*, 2024. https://www.sfcircuits.com/pcb-school/serpentine-routing (accessed Dec. 18, 2024).