Winstar Display Co., LTD
華凌光電股份有限公司

住址: 407 台中市中清路 163 號
No.163 Chung Ching RD.,
Taichune, Taiwan, R.O.C

WEB: http://www.winstar.com.tw
E-mail: sales@winstar.com.tw
Tel:886-4-24262208 Fax：886-4-24262207

SPECIFICATION

CUSTOMER ：

MODULE NO.: WH20232A-TMI-V#A

APPROVED BY: (FOR CUSTOMER USE ONLY)	PCB VERSION: DATA:

SALES BY	APPROVED BY	CHECKED BY	PREPARED BY

VERSION	DATE	REVISED PAGE NO.	SUMMARY
A	2008/11/25	24	Modify backlight information.

Winstar

ay Co., LTD

華凌光電股份有限公司

MODLE NO：

DOC. FIRST ISSUE

RECORDS OF REVISION

VERSION	DATE	REVISED PAGE NO.	SUMMARY
0	2006-8-17		First issue
A	2008/11/25	24	Modify backlight information.
B	2013/01/31		Command Summary Table

Contents

1.Module Classification Information

WG 20232 A－TML－ V#A
① ② ③ ④ ⑤ ⑥ ⑦ ⑧

① Brand：WINSTAR DISPLAY CORPORATION
② Display Type：H→Character Type, G→Graphic Type
③ Display Font： 202 x 32 dots.
④ Model serials no.

⑤	Backlight Type：	N→Without backlight	T→LED, White
		B→EL, Blue green	A→LED, Amber
		D→EL, Green	R→LED, Red
		W→EL, White	O→LED, Orange
		F→CCFL, White	G→LED, Green
		Y→LED, Yellow Green	T→LED, White
⑥	LCD Mode：	B→TN Positive, Gray	T→FSTN Negative
		N→TN Negative,	
		G→STN Positive, Gray	
		Y→STN Positive, Yellow Green	
		M→STN Negative, Blue	
		F→FSTN Positive	
⑦	LCD Polarizer Type/ Temperature range/ View direction	A→Reflective, N.T, 6:00	H→Transflective, W.T,6:00
		D→Reflective, N.T, 12:00	K→Transflective, W.T,12:00
		G→Reflective, W. T, 6:00	C→Transmissive, N.T,6:00
		J→Reflective, W. T, 12:00	F→Transmissive, N.T,12:00
		B→Transflective, N.T,6:00	I→Transmissive, W. T, 6:00
		E→Transflective, N.T.12:00	L→Transmissive, W.T,12:00
⑧	Special Code	V : Build in Negative Voltage	
		A: Avant IC	
		#:Fit in with the ROHS Directions and regulations	

2.Precautions in use of LCD Modules

(1)Avoid applying excessive shocks to the module or making any alterations or modifications to it.
(2)Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
(3)Don't disassemble the LCM.
(4)Don't operate it above the absolute maximum rating.
(5)Don't drop, bend or twist LCM.
(6)Soldering: only to the I/O terminals.
(7)Storage: please storage in anti-static electricity container and clean environment.
(8). Winstar have the right to change the passive components
(9). Winstar have the right to change the PCB Rev.

3.General Specification

Item	Dimension	Unit
Number of Characters	202 x 32	—
Module dimension	146.0 x 43.0 x 13.7(MAX)	mm
View area	123.0 x 23.0	mm
Active area	119.16 x 18.86	mm
Dot size	0.57 x 0.57	mm
Dot pitch	0.59x 0.59	mm
LCD type	STN Negative, Transmissive , Blue (In LCD production, It will occur slightly color difference. We can only guarantee the same color in the same batch.)	
Duty	1/32	
View direction	12 o'clock	
Backlight Type	LED , White	

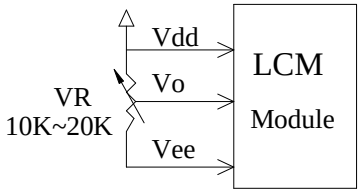
4.Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	—	+70	℃
Storage Temperature	T_{ST}	-30	—	+80	℃
Input Voltage	V_I	0	—	V_{DD}	V
Supply Voltage For Logic	V_{CC}	0	—	6.7	V
Supply Voltage For LCD	V_{CC}-V_{LCD}	0	—	-10	V
Supply Voltage For LCD	V_{OUT}	—	—	NC	V

5.Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	—	4.5	5.0	5.5	V
Supply Voltage For LCD *Note	V_{DD}-V_0	Ta=-20℃ Ta=25℃ Ta=+70℃	5.9 4.7 3.3	6.2 4.8 3.4	6.5 4.9 3.5	V V V V
Input High Volt.	V_{IH}	—	2.0	—	V_{DD}	V
Input Low Volt.	V_{IL}	—	0	—	0.8	V
Output High Volt.	V_{OH}	—	2.7	—	V_{DD}	V
Output Low Volt.	V_{OL}	—	0	—	0.4	V
Supply Current	I_{DD}	—	4.0	5.0	8.5	mA

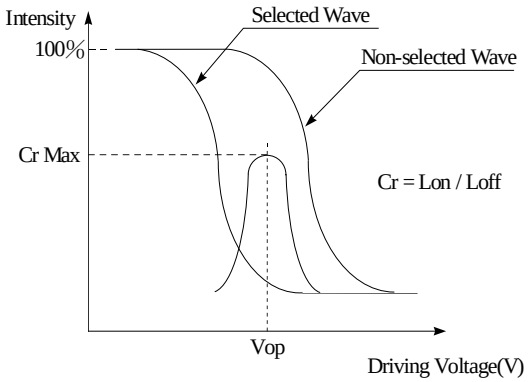
* Note: Please design the VOP adjustment circuit on customer's main board



6.Optical Characteristics

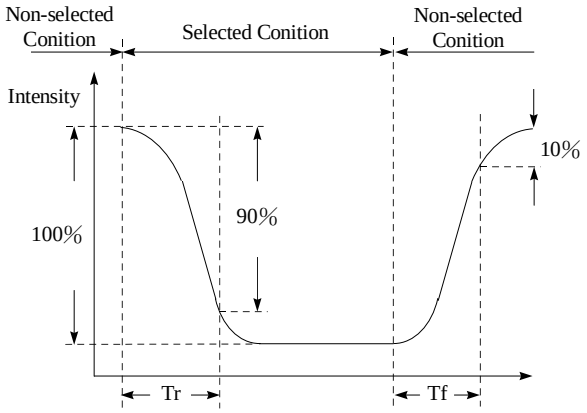
Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) θ	CR≧2	20	—	40	deg
	(H) φ	CR≧2	-30	—	30	deg
Contrast Ratio	CR	—	—	3	—	—
Response Time	T rise	—	—	100	150	ms
	T fall	—	—	100	150	ms

Definition of Operation Voltage (Vop)



[positive type]

Definition of Response Time (Tr , Tf)



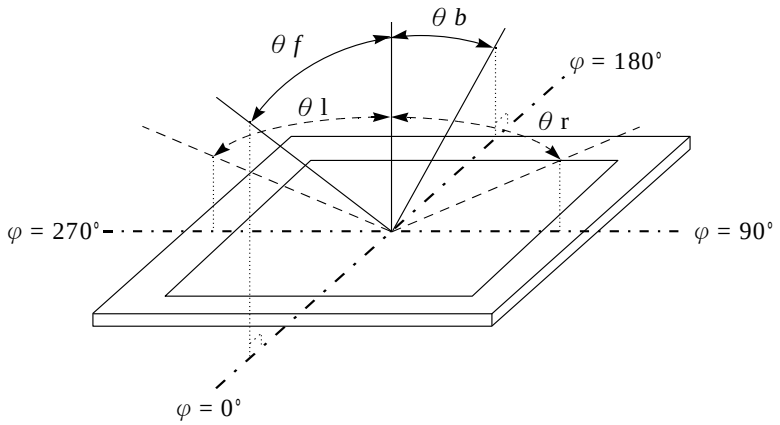
[positive type]

Conditions :

Operating Voltage : Vop　　Viewing Angle(θ ， φ) : 0°， 0°

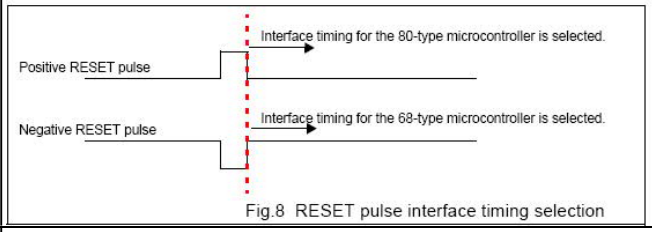
Frame Frequency : 64 HZ　Driving Waveform : 1/N duty , 1/a bias

Definition of viewing angle(CR ≧2)

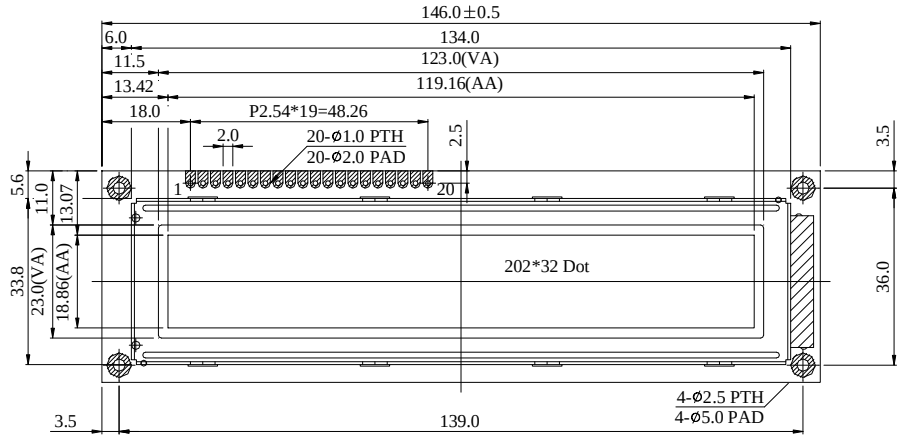


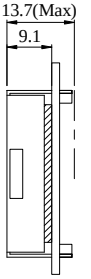
7.Interface Description

Pin No.	Symbol	Level	Description
1	V_{SS}	0V	Ground
2	V_{DD}	5.0V	Power Supply
3	V_O	(Variable)	Operating voltage for LCD
4	A0	H/L	H : Data L : Instruction
5	R/W(WR)	H/L	Read/Write (R/W) signal for the 68-type microcontroller, or WRITE(WR) signal for the 80-type microcontroller. If a 68-type microcotroller is selected as the host microcontroller, this pin should be connected to the R/W output of the microcontroller. A HIGH level on this pin indicates that the microcontroller intends to read from the SBN1661G_X series. A LOW level on this pin indicates that the microcontroller intends to write to the SBN1661G_X series. If a 80-type microcontroller is selected as the host microcontroller, this pin should be connected to the WR output of the microcontroller. A LOW level on this pin indicates that the microcontroller intends to write to the SBN1661G_X series.
6	CS1	H/L	Enable signal (E) for the 68-type microcontroller, or READ (RD) signal for the 80-type microcontroller. If a 68-type microcotroller is selected as the host microcontroller, this pin should be connected to the ENABLE output of the microcontroller. A HIGH level on this pin indicates that the microcontroller intends to select the SBN1661G_X series. If a 80-type microcontroller is selected as the host microcontroller, this pin should be connected to the RD output of the microcontroller. A LOW level on this pin indicates that the microcontroller intends to read from the SBN1661G_X series..
7	DB0	H/L	Bi-direction, tri-state 8-bit parallel data bus for interface with a host microcontroller. This data bus is for data transfer between the host microcontroller and the SBN1661G_X.
8	DB1	H/L	Bi-direction, tri-state 8-bit parallel data bus for interface with a host microcontroller.
9	DB2	H/L	This data bus is for data transfer between the host microcontroller and the SBN1661G_X.
10	DB3	H/L	Bi-direction, tri-state 8-bit parallel data bus for interface with a host microcontroller.
11	DB4	H/L	This data bus is for data transfer between the host microcontroller and the SBN1661G_X.
12	DB5	H/L	Bi-direction, tri-state 8-bit parallel data bus for interface with a host microcontroller.
13	DB6	H/L	This data bus is for data transfer between the host microcontroller and the SBN1661G_X.
14	DB7	H/L	Bi-direction, tri-state 8-bit parallel data bus for interface with a host microcontroller.
15	V_{EE}	-3.0V	Negative Voltage Output(Optional)
16	RES	H/L	Hardware RESET and interface type selection. This pin is a dual function pin. It can be used to reset the SBN1661G_X and select the type of interface timing. The hardware RESET is edge-sensitive. It is not level-sensitive. That is, either a falling edge or a rising edge on this pin can reset the chip. The

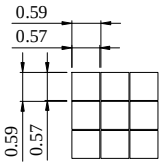
			voltage level after the reset pulse selects the type of interface timing. If the voltage level after the reset pulse stays at HIGH, interface timing for the 68-type microcontroller is selected. If the voltage level after the reset pulse stays at LOW, then interface timing for the 80-type microcontroller is selected. Therefore, a positive RESET pulse selects the 80-type microcontroller for interface and a negative RESET pulse selects the 68-type microcontroller for interface. The following diagram illustrates the reset pulse and the selected type of microcontroller.  Fig.8 RESET pulse interface timing selection
17	A	—	Power Supply for LED backlight (+)
18	K	—	Power Supply for LED backlight (-)
19	CS2	H/L	Enable signal (E) for the 68-type microcontroller, or READ (RD) signal for the 80-type microcontroller. If a 68-type microcotroller is selected as the host microcontroller, this pin should be connected to the ENABLE output of the microcontroller. A HIGH level on this pin indicates that the microcontroller intends to select the SBN1661G_X series. If a 80-type microcontroller is selected as the host microcontroller, this pin should be connected to the RD output of the microcontroller. A LOW level on this pin indicates that the microcontroller intends to read from the SBN1661G_X series..
20	CS3	H/L	Enable signal (E) for the 68-type microcontroller, or READ (RD) signal for the 80-type microcontroller. If a 68-type microcotroller is selected as the host microcontroller, this pin should be connected to the ENABLE output of the microcontroller. A HIGH level on this pin indicates that the microcontroller intends to select the SBN1661G_X series. If a 80-type microcontroller is selected as the host microcontroller, this pin should be connected to the RD output of the microcontroller. A LOW level on this pin indicates that the microcontroller intends to read from the SBN1661G_X series..

8.Contour Drawing &Block Diagram

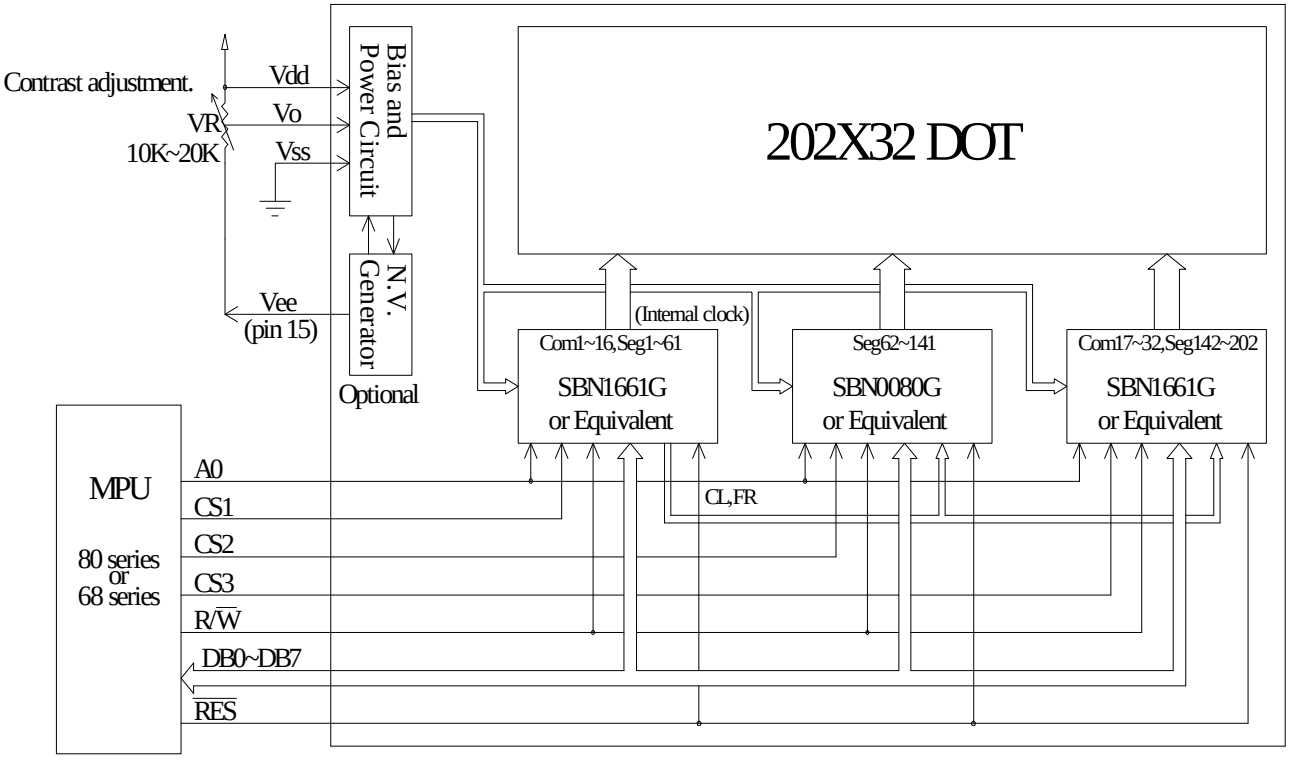




PIN NO.	SYMBOL
1	Vss
2	Vdd
3	Vo
4	A0
5	R/$\overline{W}$
6	CS1
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	Vee
16	$\overline{RESET}$
17	A
18	K
19	CS2
20	CS3



The non-specified tolerance of dimension is ±0.3mm.



9.Timing Characteristics

- **CL and FR timing**

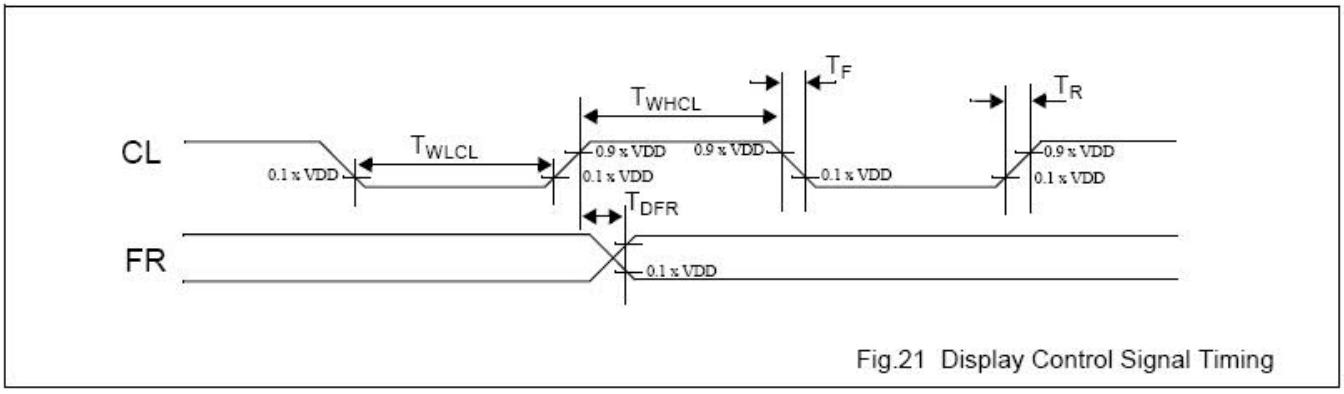


Fig.21 Display Control Signal Timing

CL and FR timing characteristics at VDD=5 volts
VDD = 5 V ±10%; VSS = 0 V; all voltages with respect to VSS unless otherwise specified;
Tamb = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WHCL}	CL clock high pulse width		33			µs
T_{WLCL}	CL cock low pulse width		33			µs
T_R	CL clock rise time			28	120	ns
T_F	CL clock fall time			28	120	ns
$T_{DFR(input)}$	FR delay time (input)	When used as input in Slave Mode application	-2.0	0.2	1.6	µS
$T_{DFR(output)}$	FR delay time (output)	When used as output in Master Mode application, with CL= 100 pF.		0.2	0.36	µS

CL and FR timing characteristics at VDD=3 volts
VDD = 3 V ±10%; VSS = 0 V; all voltages with respect to VSS unless otherwise specified;
Tamb = −20 to +75 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{WHCL}	CL clock high pulse width		65			µs
T_{WLCL}	CL cock low pulse width		65			µs
T_R	CL clock rise time			50	220	ns
T_F	CL clock fall time			50	220	ns
$T_{DFR(input)}$	FR delay time (input)	When used as input in Slave Mode application	-3.6	0.36	3.6	µS
$T_{DFR(output)}$	FR delay time (output)	When used as output in Master Mode application, with CL= 100 pF.		0.32	0.6	µS

AC timing for interface with an 80-type microcontroller

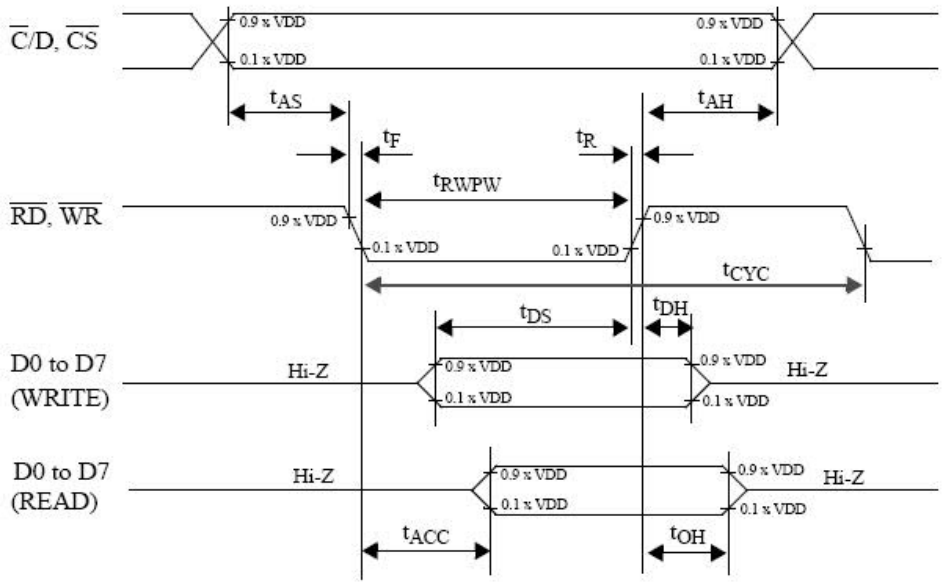


Fig.22 AC timing for interface with a 80-type microcontroller

AC timing for interface with a 80-type microcontorller at VDD=5 volts VDD = 5 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t_{AS}	Address set-up time	20			ns
t_{AH}	Address hold time	10			ns
t_F, t_R	Read/Write pulse falling/rising time		15		ns
t_{RWPW}	Read/Write pulse width	200			ns
t_{CYC}	System cycle time	1000			ns
t_{DS}	Data setup time	80			ns
t_{DH}	Data hold time	10			ns
t_{ACC}	Data READ access time		90	CL= 100 pF.	ns
t_{OH}	Data READ output hold time	10	60	Refer to Fig. 23.	ns

AC timing for interface with an 80-type microcontorller at VDD=3 volts VDD = 3 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t_{AS}	Address set-up time	40			ns
t_{AH}	Address hold time	20			ns
t_F, t_R	Read/Write pulse falling/rising time		15		ns
t_{RWPW}	Read/Write pulse width	400			ns
t_{CYC}	System cycle time	2000			ns
t_{DS}	Data setup time	160			ns

symbol	parameter	min.	max.	test conditons	unit
t_{DH}	Data hold time	20			ns
t_{ACC}	Data READ access time		180	CL= 100 pF,	ns
t_{OH}	Data READ output hold time	20	120	Refer to 23.	ns

Note:

The measurement is with the load circuit connected. The load circuit is shown in Fig. 23.

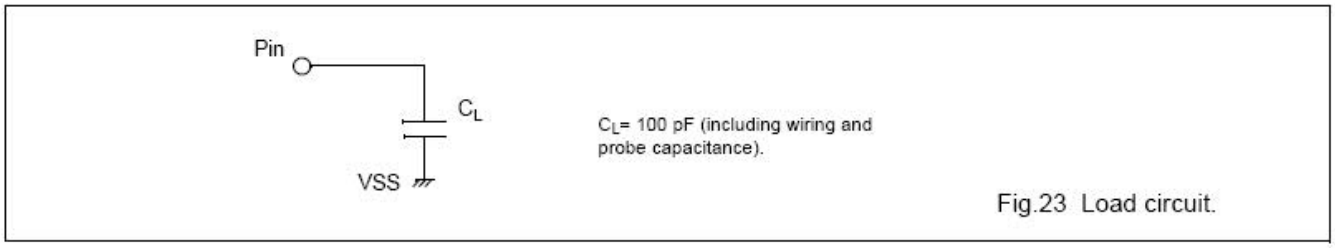


Fig.23 Load circuit.

AC timing for interface with a 68-type microcontroller

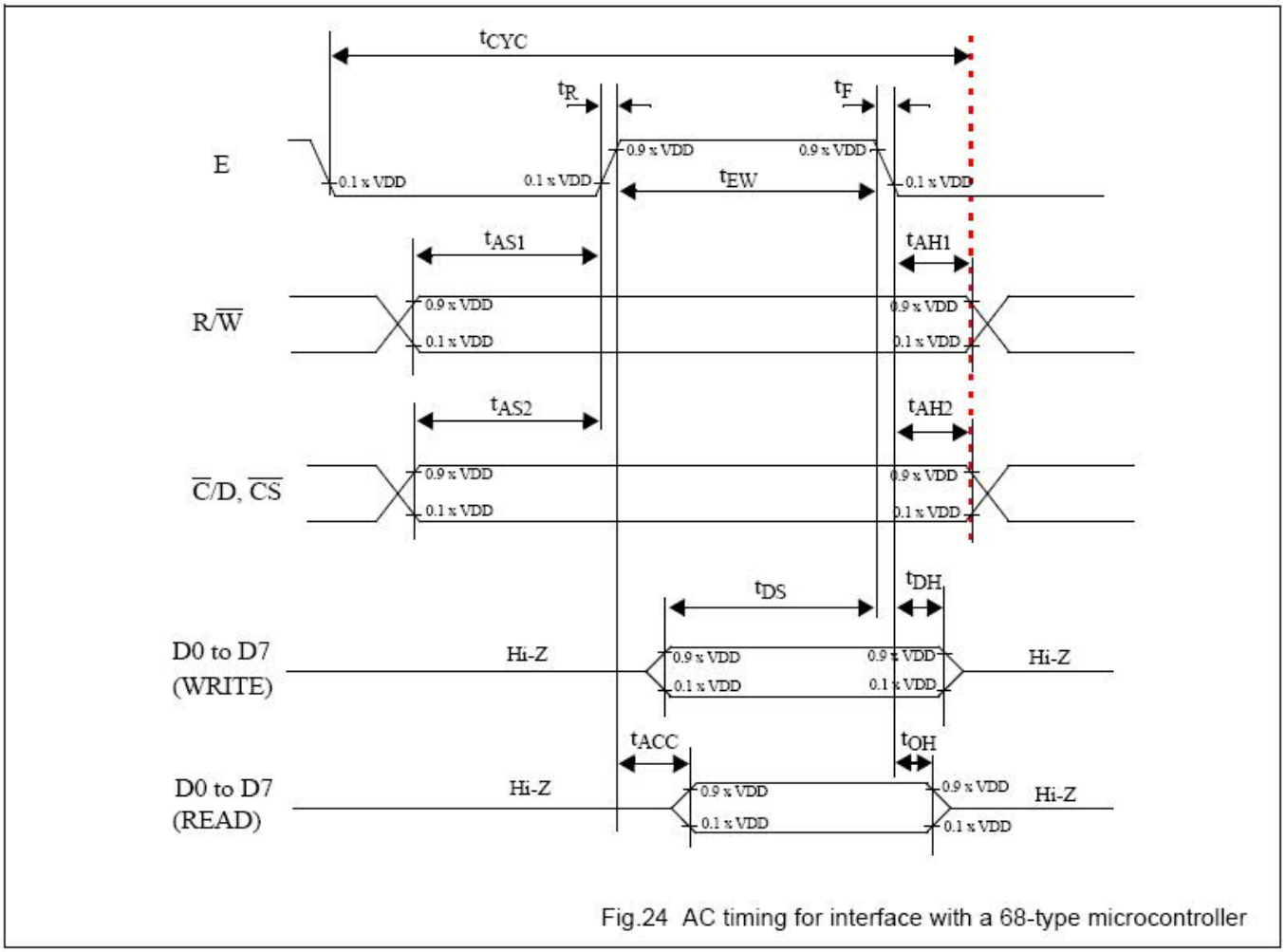


Fig.24 AC timing for interface with a 68-type microcontroller

AC timing for interface with a 68-type microcontroller at VDD=5 volts VDD = 5 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t_{AS1}	Address set-up time with respect to R/$\overline{W}$	20			ns
t_{AS2}	Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$	20			ns
t_{AH1}	Address hold time with respect to R/$\overline{W}$	10			ns
t_{AH2}	Address hold time respect with to $\overline{C}$/D, $\overline{CS}$	10			ns
t_F, t_R	Enable (E) pulse falling/rising time		15		ns
t_{CYC}	System cycle time	1000		Note 1	ns
t_{EWR}	Enable pulse width for READ	100			ns
t_{EWW}	Enable pulse width for WRITE	80			ns
t_{DS}	Data setup time	80			ns
t_{DH}	Data hold time	10			ns
t_{ACC}	Data access time		90	CL= 100 pF.	ns
t_{OH}	Data output hold time	10	60	Refer to Fig. 23.	ns

AC timing for interface with a 68-type microcontroller at VDD=3 volts VDD = 3 V ±10%; VSS = 0 V; Tamb = -20 °C to +75°C.

symbol	parameter	min.	max.	test conditons	unit
t_{AS1}	Address set-up time with respect to R/$\overline{W}$	40			ns
t_{AS2}	Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$	40			ns
t_{AH1}	Address hold time with respect to R/$\overline{W}$	20			ns
t_{AH2}	Address hold time respect with to $\overline{C}$/D, $\overline{CS}$	20			ns
t_F, t_R	Enable (E) pulse falling/rising time		15		ns
t_{CYC}	System cycle time	2000		Note 1	ns
t_{EWR}	Enable pulse width for READ	200			ns
t_{EWW}	Enable pulse width for WRITE	160			ns
t_{DS}	Data setup time	160			ns
t_{DH}	Data hold time	20			ns
t_{ACC}	Data access time		180	CL= 100 pF.	ns
t_{OH}	Data output hold time	20	120	Refer to Fig. 23.	ns

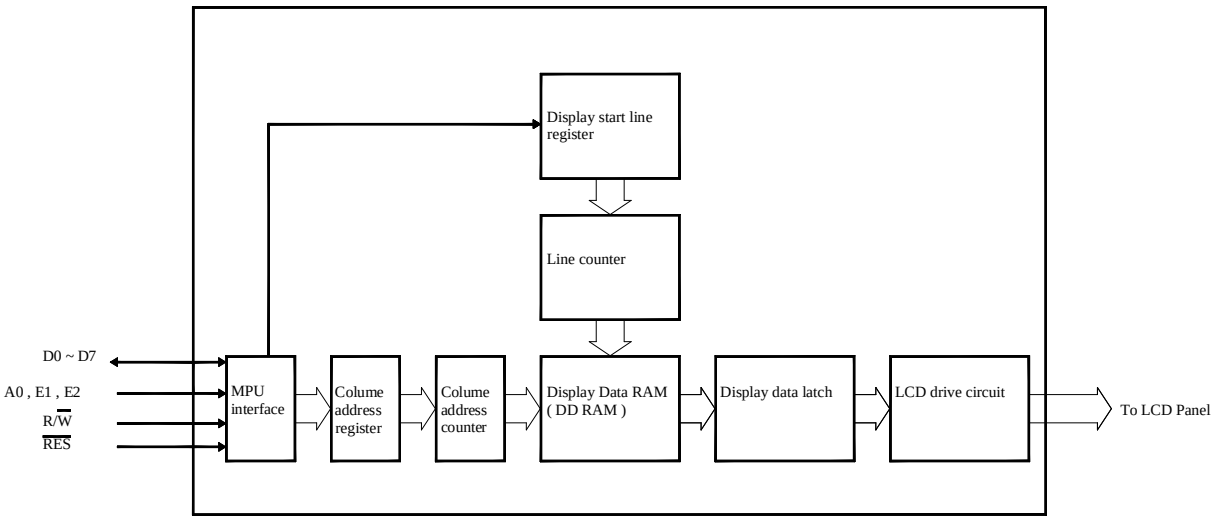
Note:

1. The system cycle time(tCYC) is the time duration from the time when Chip Enable is enabled to the time when Chip Select is released.

10.Function Description

◆Block Diagram

This 122×32 dots LCD Module built in two SBN1661G_M18-D LSI controller.



◆MPU interface

The SBN1661G_M18-D controller transfers data via 8-bit bidirecional data buses (Do to D7), it can fit any MPU if it corresponds to SBN1661G_M18-D Read and Write Timing Characteristics.

◆Data transfer

The SBN1661G_M18-D driver uses the A0, E and R/W signals to transfer data between the system MPU and internal registers, The combinations used are given in the table below.

A0	R/W	Function
1	1	Read display data
1	0	Write display data
0	1	Read status
0	0	Write to internal register (command)

◆Busy flag

When the Busy flag is logical 1, the SBN1661G_M18-D series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (t_{CYC}) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

◆Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command.

◆Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 1. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

◆Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 1.

◆Page Register

The page register is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 1. The contents of the page register are set by the Set Page Register command.

Page address	DATA	Line address	Common output
D1,D2= 0,0	D0	00H	COM 0
	D1	01H	COM 1
	D2	02H	COM 2
	D3	03H	COM 3
	D4	04H	COM 4
	D5	05H	COM 5
	D6	06H	COM 6
	D7	07H	COM 7
0,1	D0	08H	COM 8
	D1	09H	COM 9
	D2	0AH	COM 10
	D3	0BH	COM 11
	D4	0CH	COM 12
	D5	0DH	COM 13
	D6	0EH	COM 14
	D7	0FH	COM 15
1,0	D0	10H	COM 16
	D1	11H	COM 17
	D2	12H	COM 18
	D3	13H	COM 19
	D4	14H	COM 20
	D5	15H	COM 21
	D6	16H	COM 22
	D7	17H	COM 23
1,1	D0	18H	COM 24
	D1	19H	COM 25
	D2	1AH	COM 26
	D3	1BH	COM 27
	D4	1CH	COM 28
	D5	1DH	COM 29
	D6	1EH	COM 30
	D7	1FH	COM 31

Coloum address																						
ADC	D0=0	00H	01H	02H	03H	04H	05H	06H	——	——	——	3AH	3BH	3CH	——	4DH	4EH	4FH
	D0=1	4FH	4EH	4DH	4CH	4BH	4AH	49H	——	——	——				——	02H	01H	00H
	seg pin	1	2	3	4	5	6	7	——	——	——	59	60	61	——	78	79	80

SED1520

SED1521

Figure 1: page and column address

* The 122*32 dots display area is consist of two 61*32, The interface control pin E1 enable the left 61*32,E2 enable the right 61*32.

11.Commands Descriptions

The host microcontroller can issue commands to the SBN1661G_X. Table 27 lists all the commands. When issuing a command, the host microcontroller should put the command code on the data bus. The host microcontroller should also give the control bus C/D, E(RD), and R/W(WR) proper value and timing.

Commands

COMMAND	COMMAND CODE								FUNCTION
	D7	D6	D5	D4	D3	D2	D1	D0	
Write Display Data	Data to be written into the Display Data Memory.								Write a byte of data to the Display Data Memory.
Read Display Data	Data read from the Display Data Memory.								Read a byte of data from the Display Data Memory.
Read-Modify-Write	1	1	1	0	0	0	0	0	Start Read-Modify-Write operation.
END	1	1	1	0	1	1	1	0	Stop Read-Modify-Write operation.
Software Reset	1	1	1	0	0	0	1	0	Software Reset.

Write Display Data

The Write Display Data command writes a byte (8 bits) of data to the Display Data Memory. Data is put on the data bus by the host microcontroller. The location which accepts this byte of data is pointed to by the Page Address Register and the Column Address Register. At the end of the command operation, the content of the Column Address Register is automatically incremented by 1.

The setting of the control bus for issuing Write Display Data command

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
1	1	0

Read Display Data

The Read Display Data command starts a 3-step operation.

1. First, the current data of the internal 8-bit output latch of the Display Data Memory is read by the microcontroller, via the 8-bit data bus DB0~DB7.
2. Then, a byte of data of the Display Data Memory is transferred to the 8-bit output latch from a location specified by the Page Address Register and the Column Address Register,
3. Finally, the content of the Column Address Register is automatically incremented by one.

Fig. 16 shows the internal 8-bit ouptut latch located between the 8-bit I/O data bus and the Display Data Memory cell array. Because of this internal 8-bit output latch, a dummy read is needed to obtain correct data from the Display Data Memory. For Display Data Write operation, a dummy write **is not** needed, because data can be directly written from the data bus to internal memory cells.

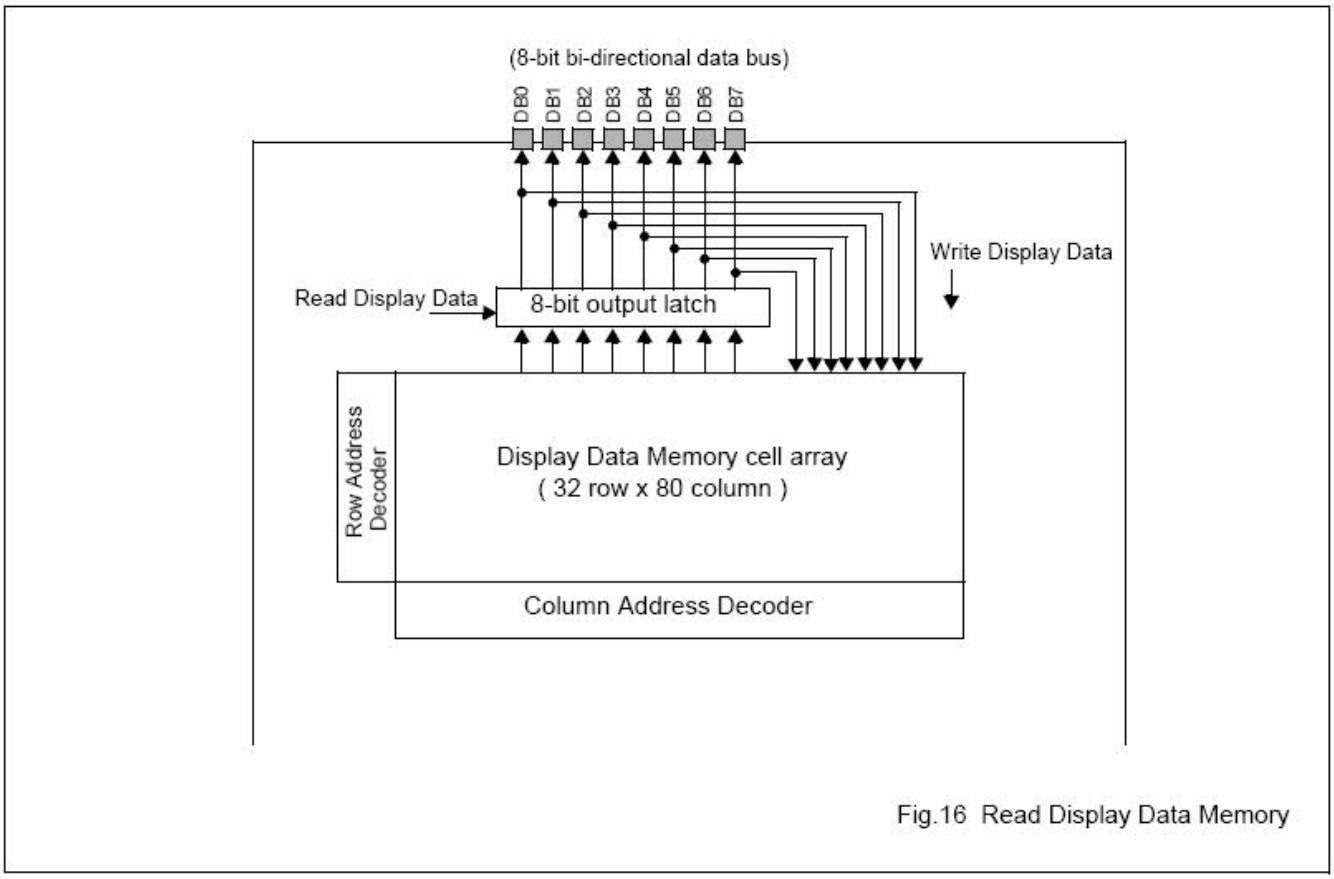


Fig.16 Read Display Data Memory

The setting of the control bus for issuing Read Display Data command

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
1	0	1

Read-Modify-Write

When the Read-Modify-Write command is issued, the SBN1661G_X enters into Read-Modify-Write mode. In normal operation, when a Read Display Data command or a Write Display Data command is issued, the content of the Column Address Register is automatically incremented by one after the command operation is finished. However, during Read-Modify-Write mode, the content of the Column Address Register is not incremented by one after a Read Display Data command is finished; only the Write Display Data command can make the content of the Column Address Register automatically incremented by one after the command operation is finished.

During Read-Modify-Write mode, any other registers, except the Column Address Register, can be modified. This command is useful when a block of the Display Data Memory needs to be repeatedly read and updated.

Fig. 17 gives the change sequence of the Column Address Register during Read-Modify-Write mode. Figure 18 gives the flow chart for Read-Modify-Write command.

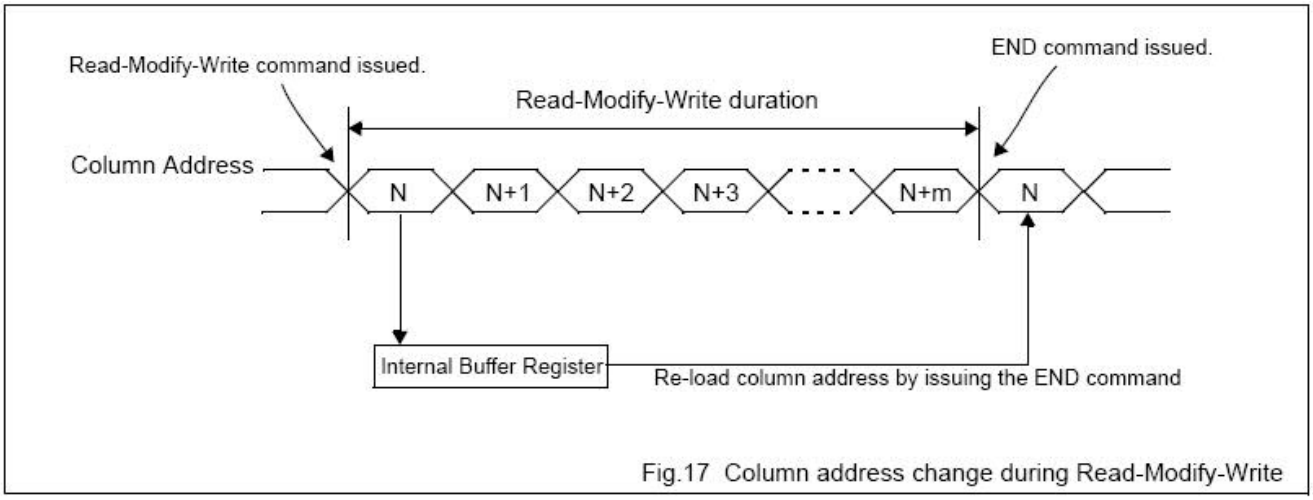


Fig.17 Column address change during Read-Modify-Write

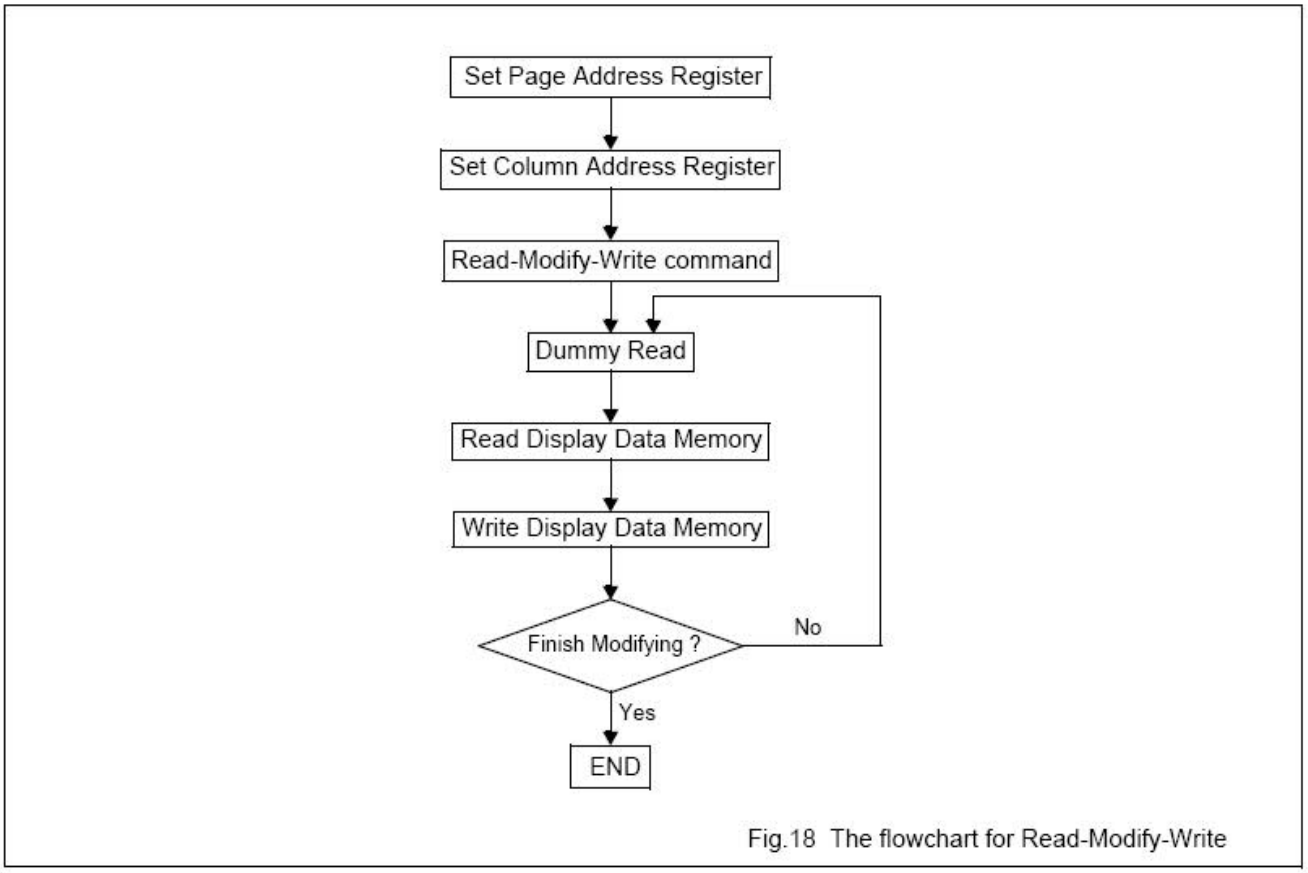


Fig.18 The flowchart for Read-Modify-Write

The setting of the control bus for the Read-Modify-Write command

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
0	1	0

The setting of the data bus for the Read-Modify-Write command

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	0	0	0	0

The END command

The END command releases the Read-Modify-Write mode and re-loads the Column Address Register with the value previously stored in the internal buffer (refer to Fig. 17) when the Read-Modify-Write command was issued.

The setting of the control bus for the END command

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
0	1	0

The setting of the data bus for the END command

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	1	1	1	0

The command code is EE Hex.

Software RESET command

The Software Reset command is different from the hardware reset and can not be used to replace hardware reset.

When Software Reset is issued by the host microcontroller,

• the content of the Display Start Line Register is cleared to zero(A4~A0=00000),
• the Page Address Register is set to 3 (A1 A0 = 11),
• the content of the Display Data Memory remains unchanged.
• the content of all other registers remains unchanged.

The setting of the control bus for Software RESET

$\overline{C}$/D	E/($\overline{RD}$)	R/$\overline{W}$($\overline{WR}$)
0	1	0

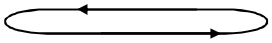
The setting of the data bus for Software RESET

D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	1	1	0	0	0	1	0

The command code is E2 Hex.

12.Reliability

Content of Reliability Test (wide temperature, -20℃~70℃)

Environmental Test			
Test Item	**Content of Test**	**Test Condition**	**Note**
High Temperature storage	Endurance test applying the high storage temperature for a long time.	80℃ 200hrs	2
Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-30℃ 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70℃ 200hrs	——
Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	-20℃ 200hrs	1
High Temperature/ Humidity Operation	The module should be allowed to stand at 60℃,90%RH max For 96hrs under no-load condition excluding the polarizer, Then taking it out and drying it at normal temperature.	60℃,90%RH 96hrs	1,2
Thermal shock resistance	The sample should be allowed stand the following 10 cycles of operation -20℃ 25℃ 70℃  30min 5min 30min 1 cycle	-20℃/70℃ 10 cycles	——
Vibration test	Endurance test applying the vibration during transportation and using.	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X,Y,Z for Each 15 minutes	3
Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after remove from the test chamber.

Note3: Vibration test will be conducted to the product itself without putting it in a container.

13.Backlight Information

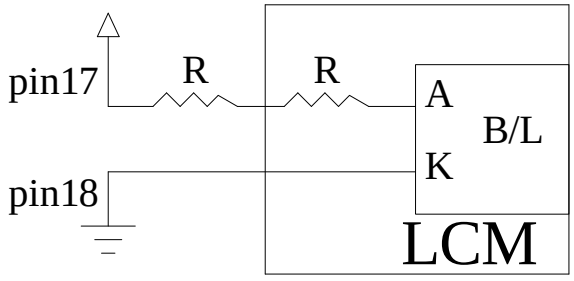
Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	ILED	43.2	48	75	mA	V=3.5V
Supply Voltage	V	3.4	3.5	3.6	V	—
Reverse Voltage	VR	—	—	5	V	—
Luminous Intensity	IV	128	160	—	cd/m^2	ILED=48mA
LED Life Time (For Reference only)	—	—	50K	—	Hr.	ILED≦48mA 25℃,50-60%RH, (Note 1)
Color	White					

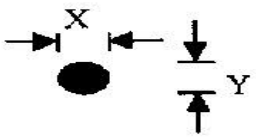
Note: The LED of B/L is drive by current only, drive voltage is for reference only. drive voltage can make driving current under safety area (current between minimum and maximum).

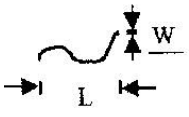
Note 1:50K hours is only an estimate for reference.

2.Drive from pin17,pin18



14. Inspection specification

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character , dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
1.8 Contrast defect.</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or white spots on LCD (display only)</td><td>2.1 White and black spots on display ≦0.25mm, no more than three white or black spots present.
2.2 Densely spaced: No more than two spots or lines within 3mm</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD black spots, white spots, contamination (non-display)</td><td>3.1 Round type : As following drawing
Φ=(x + y) / 2
 

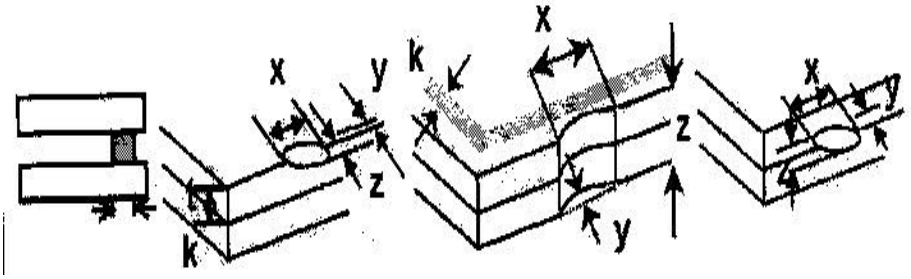
SIZE / Acceptable Q TY
Φ≦0.10 : Accept no dense
0.10＜Φ≦0.20 : 2
0.20＜Φ≦0.25 : 1
0.25＜Φ : 0</td><td>2.5</td></tr>
<tr><td>3.2 Line type : (As following drawing)
 

Length / Width / Acceptable Q TY
--- / W≦0.02 / Accept no dense
L≦3.0 / 0.02＜W≦0.03 / 2
L≦2.5 / 0.03＜W≦0.05 / 2
--- / 0.05＜W / As round type</td><td>2.5</td></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction.
Size Φ / Acceptable Q TY
Φ≦0.20 : Accept no dense
0.20＜Φ≦0.50 : 3
0.50＜Φ≦1.00 : 2
1.00＜Φ : 0
Total Q TY : 3</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
05	Scratches	Follow NO.3 LCD black spots, white spots, contamination	
06	Chipped glass	Symbols Define: x: Chip length y: Chip width z: Chip thickness k: Seal width t: Glass thickness a: LCD side length L: Electrode pad length:	2.5

6.1 General glass chip :

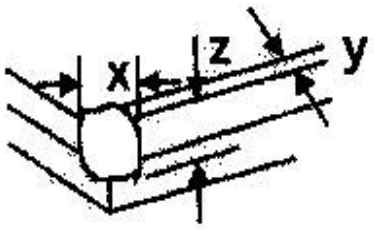
6.1.1 Chip on panel surface and crack between panels:



z: Chip thickness	y: Chip width	x: Chip length
Z≦1/2t	Not over viewing area	x≦1/8a
1/2t＜z≦2t	Not exceed 1/3k	x≦1/8a

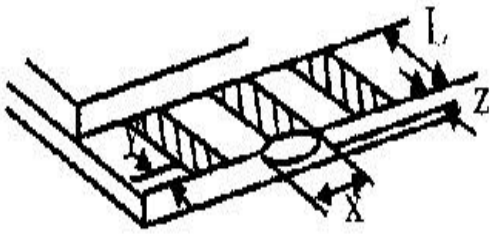
⊙If there are 2 or more chips, x is total length of each chip.

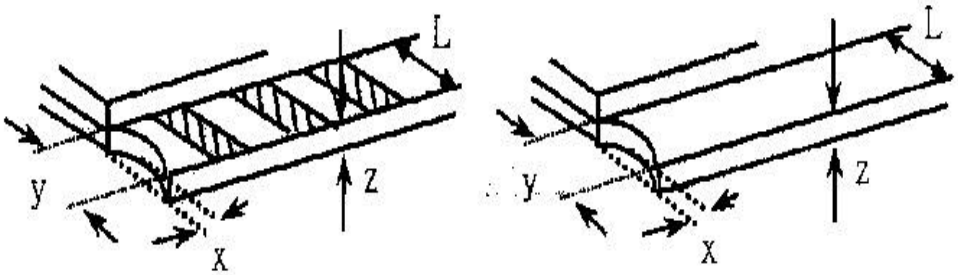
6.1.2 Corner crack:

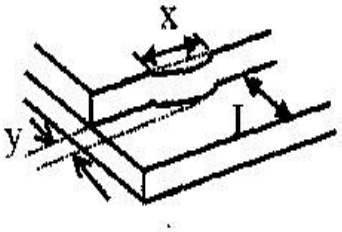


z: Chip thickness	y: Chip width	x: Chip length
Z≦1/2t	Not over viewing area	x≦1/8a
1/2t＜z≦2t	Not exceed 1/3k	x≦1/8a

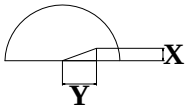
⊙If there are 2 or more chips, x is the total length of each chip.

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>06</td><td>Glass crack</td><td>
Symbols :
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length
6.2 Protrusion over terminal :
6.2.1 Chip on electrode pad :


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
6.2.2 Non-conductive portion:


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦ L</td><td>x≦1/8a</td><td>0 ＜ z ≦ t</td></tr>
</table>
⊙If the chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙If the product will be heat sealed by the customer, the alignment mark not be damaged.
6.2.3 Substrate protuberance and internal crack.


<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>x ≦ a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
07	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
08	Backlight elements	8.1 Illumination source flickers when lit. 8.2 Spots or scratched that appear when lit must be judged. Using LCD spot, lines and contamination standards. 8.3 Backlight doesn ' t light or color wrong.	0.65 2.5 0.65
09	Bezel	9.1 Bezel may not have rust, be deformed or have fingerprints, stains or other contamination. 9.2 Bezel must comply with job specifications.	2.5 0.65
10	PCB、COB	10.1 COB seal may not have pinholes larger than 0.2mm or contamination. 10.2 COB seal surface may not have pinholes through to the IC. 10.3 The height of the COB should not exceed the height indicated in the assembly diagram. 10.4 There may not be more than 2mm of sealant outside the seal area on the PCB. And there should be no more than three places. 10.5 No oxidation or contamination PCB terminals. 10.6 Parts on PCB must be the same as on the production characteristic chart. There should be no wrong parts, missing parts or excess parts. 10.7 The jumper on the PCB should conform to the product characteristic chart. 10.8 If solder gets on bezel tab pads, LED pad, zebra pad or screw hold pad, make sure it is smoothed down. 10.9 The Scraping testing standard for Copper Coating of PCB  **X * Y<=2mm^2**	2.5 2.5 0.65 2.5 2.5 0.65 0.65 2.5 2.5
11	Soldering	11.1 No un-melted solder paste may be present on the PCB. 11.2 No cold solder joints, missing solder connections, oxidation or icicle. 11.3 No residue or solder balls on PCB. 11.4 No short circuits in components on PCB.	2.5 2.5 2.5 0.65

NO	Item	Criterion	AQL
12	General appearance	12.1 No oxidation, contamination, curves or, bends on interface Pin (OLB) of TCP. 12.2 No cracks on interface pin (OLB) of TCP. 12.3 No contamination, solder residue or solder balls on product. 12.4 The IC on the TCP may not be damaged, circuits. 12.5 The uppermost edge of the protective strip on the interface pin must be present or look as if it cause the interface pin to sever. 12.6 The residual rosin or tin oil of soldering (component or chip component) is not burned into brown or black color. 12.7 Sealant on top of the ITO circuit has not hardened. 12.8 Pin type must match type in specification sheet. 12.9 LCD pin loose or missing pins. 12.10 Product packaging must the same as specified on packaging specification sheet. 12.11 Product dimension and structure must conform to product specification sheet.	2.5 0.65 2.5 2.5 2.5 2.5 2.5 0.65 0.65 0.65 0.65

15. Material List of Components for RoHs

1. WINSTAR Display Co., Ltd hereby declares that all of or part of products (with the mark "#"in code), including, but not limited to, the LCM, accessories or packages, manufactured and/or delivered to your company (including your subsidiaries and affiliated company) directly or indirectly by our company (including our subsidiaries or affiliated companies) do not intentionally contain any of the substances listed in all applicable EU directives and regulations, including the following substances.

Exhibit A：The Harmful Material List

.

Material	(Cd)	(Pb)	(Hg)	(Cr6+)	PBBs	PBDEs
Limited Value	100 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm	1000 ppm
Above limited value is set up according to RoHS.						

2.Process for RoHS requirement：

(1) Use the Sn/Ag/Cu soldering surface ；the surface of Pb-free solder is rougher than we used before.

(2) Heat-resistance temp.：

Reflow：250℃,30 seconds Max.；

Connector soldering wave or hand soldering ：320℃, 10 seconds max.

(3) Temp. curve of reflow, max. Temp.：235±5℃；

Recommended customer's soldering temp. of connector ：280℃, 3 seconds.

winstar **LCM Sample Estimate Feedback Sheet**

Module Number：_____ **Page: 1**

1、Panel Specification：

1.	Panel Type：	☐ Pass	☐ NG , _____
2.	View Direction：	☐ Pass	☐ NG , _____
3.	Numbers of Dots：	☐ Pass	☐ NG , _____
4.	View Area：	☐ Pass	☐ NG , _____
5.	Active Area：	☐ Pass	☐ NG , _____
6.	Operating Temperature：	☐ Pass	☐ NG , _____
7.	Storage Temperature：	☐ Pass	☐ NG , _____
8.	Others：_____		

2、Mechanical

1.	PCB Size：	☐ Pass	☐ NG , _____
2.	Frame Size：	☐ Pass	☐ NG , _____
3.	Materal of Frame：	☐ Pass	☐ NG , _____
4.	Connector Position：	☐ Pass	☐ NG , _____
5.	Fix Hole Position：	☐ Pass	☐ NG , _____
6.	Backlight Position：	☐ Pass	☐ NG , _____
7.	Thickness of PCB：	☐ Pass	☐ NG , _____
8.	Height of Frame to PCB：	☐ Pass	☐ NG , _____
9.	Height of Module：	☐ Pass	☐ NG , _____
10.	Others：	☐ Pass	☐ NG , _____

3、Relative Hole Size：

1.	Pitch of Connector：	☐ Pass	☐ NG , _____
2.	Hole size of Connector：	☐ Pass	☐ NG , _____
3.	Mounting Hole size：	☐ Pass	☐ NG , _____
4.	Mounting Hole Type：	☐ Pass	☐ NG , _____
5.	Others：	☐ Pass	☐ NG , _____

4、Backlight Specification：

1.	B/L Type：	☐ Pass	☐ NG , _____
2.	B/L Color：	☐ Pass	☐ NG , _____
3.	B/L Driving Voltage (Reference for LED Type)：	☐ Pass	☐ NG , _____
4.	B/L Driving Current：	☐ Pass	☐ NG , _____
5.	Brightness of B/L：	☐ Pass	☐ NG , _____
6.	B/L Solder Method：	☐ Pass	☐ NG , _____
7.	Others：	☐ Pass	☐ NG , _____

>> **Go to page 2** <<

5、Electronic Characteristics of Module：

1.	Input Voltage：	☐ Pass	☐ NG , _____
2.	Supply Current：	☐ Pass	☐ NG , _____
3.	Driving Voltage for LCD：	☐ Pass	☐ NG , _____
4.	Contrast for LCD：	☐ Pass	☐ NG , _____
5.	B/L Driving Method：	☐ Pass	☐ NG , _____
6.	Negative Voltage Output：	☐ Pass	☐ NG , _____
7.	Interface Function：	☐ Pass	☐ NG , _____
8.	LCD Uniformity：	☐ Pass	☐ NG , _____
9.	ESD test：	☐ Pass	☐ NG , _____
10.	Others：	☐ Pass	☐ NG , _____

6、Summary：

Sales signature：_____
Customer Signature：_____ **Date**：___/___/___