

Specification Preliminary

Version: V1.02

Document No.: ILI9341_DS_V1.02.pdf

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1. Introduction

ILI9341 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9341 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

ILI9341 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9341 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9341 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [240xRGB](H) x 320(V)
- Output:
 - > 720 source outputs
 - > 320 gate outputs
 - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
 - ➤ 8-bits, 9-bits, 16-bits, 18-bits interface with 8080- I /8080- II series MCU
 - ➤ 6-bits, 16-bits, 18-bits RGB interface with graphic controller
 - > 3-line / 4-line serial interface
- Display mode:
 - > Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
 - > Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
 - Sleep mode
 - Deep standby mode
- On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Line/frame inversion
 - > 1 preset Gamma curve with separate RGB Gamma correction
- Content Adaptive Brightness Control
- MTP (3 times):
 - > 8-bits for ID1, ID2, ID3
 - > 7-bits for VCOM adjustment



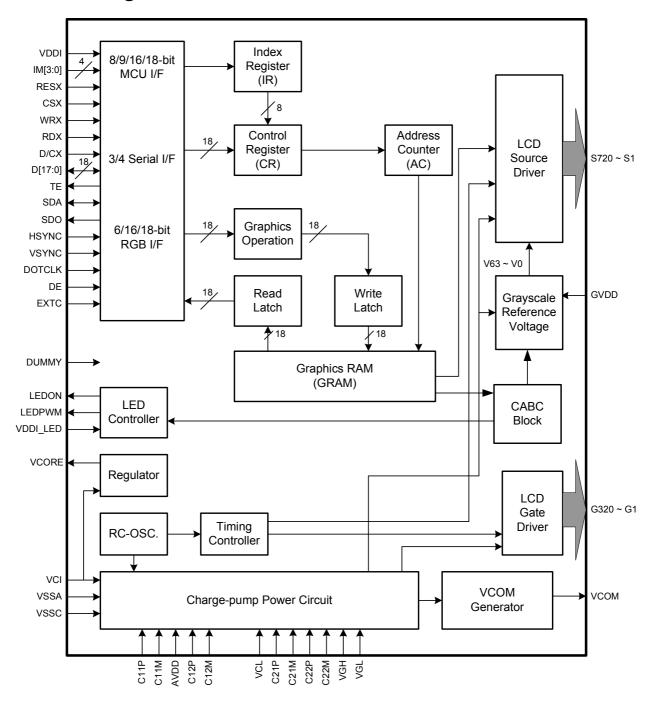


- Low -power consumption architecture
 - Low operating power supplies:
 - VDDI = 1.65V ~ 3.3V (logic)
 - VCI = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
 - Source/VCOM power supply voltage
 - AVDD GND = 4.5V ~ 5.5V
 - VCL GND = -2.0V ~ -3.0V
 - > Gate driver output voltage
 - VGH GND = 10.0V ~ 20.0V
 - VGL GND = -5.0V ~ -15.0V
 - VGH VGL \leq 32V
 - VCOM driver output voltage
 - VCOMH = 3.0V ~ (AVDD 0.5)V
 - VCOML = (VCL+0.5)V ~ 0V
 - VCOMH VCOML ≤ 6.0 V
- lacktriangle Operate temperature range: -40 $^\circ$ C to 85 $^\circ$ C
- ◆ a-Si TFT LCD storage capacitor : Cst on Common structure only



ILI9341

3. Block Diagram







4. Pin Descriptions

	Power Supply Pins									
Pin Name	I/O	Type	Descriptions							
VDDI	I	Р	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)							
VDDI_LED I			Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VDDI.							
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)							
Vcore	0	Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad							
VSS3	I	I/O Ground	System ground level for I/O circuits.							
VSS	I	Digital Ground	System ground level for logic blocks							
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.							
VSSC I Ar		Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise							

Interface Logic Signals																				
Pin Name	I/O	Type	Descriptions - Select the MCLL interface mode																	
			- Select the MCU interface mode IM3 IM2 IM1 IM0 MCU-Interface Mode DB Pin in use																	
			IM3	IM2	IM1	IMO	MCU-Interface Mode	DB Pin in ι	ise											
						11010		Register/Content	GRAM											
			0	0	0	0	80 MCU 8-bit bus interface I	D[7:0]	D[7:0]											
			0	0	0	1	80 MCU 16-bit bus interface I	D[7:0]	D[15:0]											
			0	0	1	0	80 MCU 9-bit bus interface I	D[7:0]	D[8:0]											
		0 0 1 1 80 MCU 18-bit bus interface I 0 1 0 1 3-wire 9-bit data serial interface I 0 1 1 0 4-wire 8-bit data serial interface I	D[7:0]	D[17:0]																
	I		(VDDI/VSS)									0	1	0	1		SDA: In/O	JT		
				0	1	1	0		SDA: In/O	JT										
IM[3:0]				(VDDI/VSS)	1	0	0	0		D[8:1]	D[17:10], D[8:1]									
							1	0	0	1		D[17:10]	D[17:10]							
			1	0	1	0		D[8:1]	D[17:0]											
							1	0	1	1		D[17:10]	D[17:9]							
														1	1	0	1		SDI: In SDO: Օս	t
														1	1	1	0		SDI: In SDO: Ou	t
			MPU	Paral	lel int	erface	bus and serial inter	face select												
			If usa	RGR	Inter	face n	nust salact sarial inte	arface												
								711d0C.												
			*: Fix this pin at VDDI or VSS.																	





			T					
RESX	_	MCU	This signal will reset the device and must be applied to properly					
TILOX	'	(VDDI/VSS)	initialize the chip.					
EXTC	1	MCU (VDDI/VSS)	Signal is active low. Extended command set enable. Low: extended command set is discarded. High: extended command set is accepted. Please connect EXTC to VDDI to read/write extended registers (RB0h~RCFh, RE0h~RFFh)					
CSX	I	MCU (VDDI/VSS)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. * note1,2					
			This pin is used to select "Data or Command" in the parallel interface					
			or 4-wire 8-bit serial data interface.					
			When DCX = '1', data is selected.					
D/CX (SCL)	- 1	MCU (VDDI/VSS)	When DCX = '0', command is selected.					
		,	This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit					
			serial data interface.					
			If not used, this pin should be connected to VDDI or VSS.					
RDX	I	MCU (VDDI/VSS)	8080- I /8080- II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use.					
WRX (D/CX)	Ι	MCU (VDDI/VSS)	 - 8080- I /8080- II system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use. 					
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use					
			When IM[3] : Low, Serial in/out signal.					
SDI/SDA	I/O	MCU	When IM[3]: High, Serial input signal.					
SDI/SDA	1/0	(VDDI/VSS)	The data is applied on the rising edge of the SCL signal.					
			If not used, fix this pin at VDDI or VSS.					
		MCU	Serial output signal.					
SDO	0	(VDDI/VSS)	The data is outputted on the falling edge of the SCL signal.					
			If not used, open this pin					
		MOLL	Tearing effect output pin to synchronize MPU to frame writing,					
TE	0	MCU (VDDI/VSS)	activated by S/W command. When this pin is not activated, this pin is					
		,	low. If not used, open this pin.					
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation.					
		(VDDI/VSS) MCU	Fix to VDDI or VSS level when not in use. Frame synchronizing signal for RGB interface operation.					
VSYNC	Ι	(VDDI/VSS)	Fix to VDDI or VSS level when not in use.					
HSYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.					
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use.					





Note.

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module.

Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions.

Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.



LCD Driver Input/Output Pins									
Pin Name	I/O	Туре	Descriptions						
S720~S1	0	Source	Source output signals Leave the pin to open when not in use.						
G320~G1	0	Gate	Gate output signals. Leave the pin to open when not in use.						
AVDD	0	Power Stabilizing capacitor	Output voltage of 1st step up circuit (2 x VCI). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.						
VGH	0	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.						
VGL	0	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.						
VCL	0	Power Stabilizing capacitor	Power supply for VCOML. VCL = 0~ - VCI Connect this pad with a stabilizing capacitor.						
C11P, C11M C12P, C12M	Р	Stabilizing capacitor	Connect the charge-pumping capacitor for generating AVDD level.						
C21P, C21M C22P, C22M	Р	Stabilizing capacitor	Connect the charge-pumping capacitor for generating VGH, VGL level.						
GVDD	0		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.						
VCOM	0		Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.						
LEDPWM	0		Output pin for PWM (Pulse Width Modulation) signal of LED driving. If not used, open this pad.						
LEDON	0		Output pin for enabling LED driving. If not used, open this pad.						

	Test Pins									
Pin Name	I/O	Type	Descriptions							
DUMMY	_	Open	Input pads used only for test purpose at IC-side.							
BOWINT		Ореп	During normal operation, leave these pads open.							





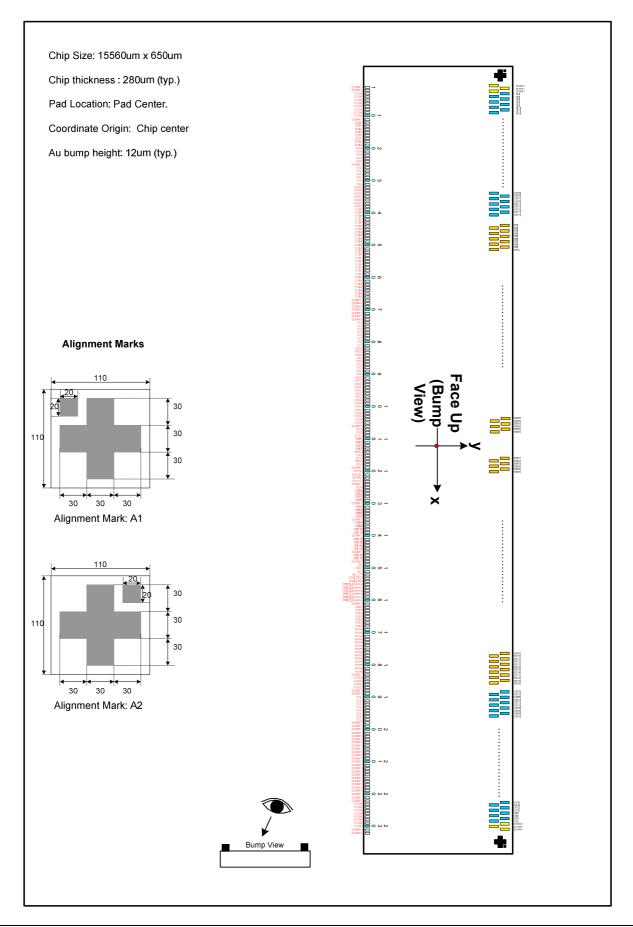
Liquid crystal power supply specifications Table

No.	Item		Description				
1	TFT Source Driver		720 pins (240 x RGB)				
2	TFT Gate Driver		320 pins				
3	TFT Display's Capacitor Structu	re	Cst structure only (Cs on Common)				
		S1 ~ S720	V0 ~ V63 grayscales				
4	Liquid Crystal Drive Output	G1 ~ G320	VGH - VGL				
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes				
5	Input Voltage	VDDI	1.65V ~ 3.30V				
5	Input Voltage	VCI	2.50V ~ 3.30V				
		AVDD	4.5V ~ 5.5V				
	Liquid Crystal Drive Voltages	VGH	10.0V ~ 20.0V				
6		VGL	-5.0V ~ -15.0V				
		VCL	-1.9V ~ -3.0V				
		VGH - VGL	Max. 32.0V				
		AVDD	VCI x2,				
7	Internal Stan un Circuita	VGH	VCI x6, x7				
'	Internal Step-up Circuits	VGL	VCI x-5, x-6,				
		VCL	VCI x-1				





5. Pad Arrangement and Coordination







No.	Pad name	Χ	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
1	DUMMY	-7292.5	-248	51	C12M	-4292.5	-248	101	VSSA	-1292.5	-248	151	LEDPWM	2245	-248
2	DUMMY	-7232.5	-248	52	C12M	-4232.5	-248	102	VSSA	-1232.5	-248	152	LEDON	2330	-248
3	VCOM	-7172.5	-248	53	C11P	-4172.5	-248	103	VSSA	-1172.5	-248	153	VDDI LED	2402.5	-248
4	VCOM	-7112.5	-248	54	C11P	-4112.5	-248	104	VSSA	-1112.5	-248	154	VDDI LED	2462.5	-248
5	VCOM	-7052.5	-248	55	C11P	-4052.5	-248	105	VSSA	-1052.5	-248	155	DB[18] Dummy		-248
6	VCOM	-6992.5	-248	56	C11P	-3992.5	-248	106	DUMMY	-992.5	-248	156	DB[19] Dummy		-248
7	VCOM	-6932.5	-248	57	C11P	-3932.5	-248	107	VGS	-932.5	-248	157	DB[20] Dummy		-248
8	VCOM	-6872.5	-248	58	C11P	-3872.5	-248	108	VGS	-872.5	-248	158	DB[21] Dummy		-248
9	VCOM	-6812.5	-248	59	C11P	-3812.5	-248	109	EXTC	-812.5	-248	159	DB[22] Dummy	2875	-248
10	VCOM	-6752.5	-248	60	C11M	-3752.5	-248	110	IM<3>	-752.5	-248	160	DB[23]_Dummy	2960	-248
11	DUMMY	-6692.5	-248	61	C11M	-3692.5	-248	111	IM<2>	-692.5	-248	161	DUMMY	3032.5	-248
12	C22P	-6632.5	-248	62	C11M	-3632.5	-248	112	IM<1>	-632.5	-248	162	VDDI	3092.5	-248
13	C22P	-6572.5	-248	63	C11M	-3572.5	-248	113	IM<0>	-572.5	-248	163	VDDI	3152.5	-248
14	C22M	-6512.5	-248	64	C11M	-3512.5	-248	114	RESX	-512.5	-248	164	VDDI	3212.5	-248
15	C22M	-6452.5	-248	65	C11M	-3452.5	-248	115	CSX	-452.5	-248	165	VDDI	3272.5	-248
16	C21P	-6392.5	-248	66	C11M	-3392.5	-248	116	DCX	-392.5	-248	166	VDDI	3332.5	-248
17	C21P	-6332.5	-248	67	(GND)	-3332.5	-248	117	WRX	-332.5	-248	167	VDDI	3392.5	-248
18	C21M	-6272.5	-248	68	(GND)	-3272.5	-248	118	RDX	-272.5	-248	168	VDDI	3452.5	-248
19	C21M	-6212.5	-248	69	(GND)	-3212.5	-248	119	DUMMY	-212.5	-248	169	Vcore	3512.5	-248
20	VGH	-6152.5	-248	70	(GND)	-3152.5	-248	120	VSYNC	-152.5	-248	170	Vcore	3572.5	-248
21	VGH	-6092.5	-248	71	(GND)	-3092.5	-248	121	HSYNC	-92.5	-248	171	Vcore	3632.5	-248
22	VGH	-6032.5	-248	72	(GND)	-3032.5	-248	122	ENABL	-32.5	-248	172	Vcore	3692.5	-248
23	VGH	-5972.5	-248	73	(GND)	-2972.5	-248	123	DOTCLK	27.5	-248	173	Vcore	3752.5	-248
24	VGH	-5912.5	-248	74	VCI	-2912.5	-248	124	DUMMY	87.5	-248	174	Vcore	3812.5	-248
25	DUMMY	-5852.5	-248	75	VCI	-2842.5	-248	125	SDA	160	-248	175	Vcore	3872.5	-248
26	VGL	-5792.5	-248	76	VCI	-2792.5	-248	126	DB[0]	245	-248	176	Vcore	3932.5	-248
27	VGL	-5732.5	-248	77	VCI	-2732.5	-248	127	DB[1]	330	-248	177	Vcore	3992.5	-248
28	VGL	-5672.5	-248	78	VCI	-2672.5	-248	128	DB[2]	415	-248	178	Vcore	4052.5	-248
29	VGL	-5612.5	-248	79	VCI	-2612.5	-248	129	DB[3]	500	-248	179	Vcore	4112.5	-248
30	VGL	-5552.5	-248	80	VCI	-2552.5	-248	130	DUMMY	572.5	-248	180	Vcore	4172.5	-248
31	VGL	-5492.5	-248	81	VCI	-2492.5	-248	131	DB[4]	645	-248	181	Vcore	4232.5	-248
32	AVDD	-5432.5	-248	82	VSS3	-2432.5	-248	132	DB[5]	730	-248	182	Vcore	4292.5	-248
33	AVDD	-5372.5	-248	83	VSS3	-2372.5	-248	133	DB[6]	815	-248	183	DUMMY	4352.5	-248
34	AVDD	-5312.5	-248	84	VSS3	-2312.5	-248	134	DB[7]	900	-248	184	GVDD	4412.5	-248
35	AVDD	-5252.5	-248	85	VSS	-2252.5	-248	135	DUMMY	972.5	-248	185	GVDD	4472.5	-248
36	AVDD	-5192.5	-248	86	VSS	-2192.5	-248	136	DB[8]	1045	-248	186	GVDD	4532.5	-248
37	AVDD	-5132.5	-248	87	VSS	-2132.5	-248	137	DB[9]	1130	-248	187	GVDD	4592.5	-248
38	AVDD	-5072.5	-248	88	VSS	-2072.5	-248	138	DB[10]	1215	-248	188	DUMMY	4652.5	-248
39	C12P	-5012.5	-248	89	VSS	-2012.5	-248	139	DB[11]	1300	-248	189	DUMMY	4712.5	-248
40	C12P	-4952.5	-248	90	VSS	-1952.5	-248	140	DUMMY	1372.5	-248	190	VCL	4772.5	-248
41	C12P	-4892.5	-248	91	VSSC	-1892.5	-248	141	DB[12]	1445	-248	191	VCL	4832.5	-248
42	C12P	-4832.5	-248	92	VSSC	-1832.5	-248	142	DB[13]	1530	-248	192	VCL	4892.5	-248
43	C12P	-4772.5	-248	93	VSSC	-1772.5	-248	143	DB[14]	1615	-248	193	VCL	4952.5	-248
44	C12P	-4712.5	-248	94	VSSC	-1712.5	-248	144	DB[15]	1700	-248	194	VCL	5012.5	-248
45	C12P	-4652.5	-248	95	VSSC	-1652.5	-248	145	DUMMY	1772.5	-248	195	VCL	5072.5	-248
46	C12M	-4592.5	-248	96	VSSC	-1592.5	-248	146	DB[16]	1845	-248	196	VCL	5132.5	-248
47	C12M	-4532.5	-248	97	VSSC	-1532.5	-248	147	DB[17]	1930	-248	197	VCL	5192.5	-248
48	C12M	-4472.5	-248	98	VSSA	-1472.5	-248	148	DUMMY	2002.5	-248	198	DUMMY	5252.5	-248
49	C12M	-4412.5	-248	99	VSSA	-1412.5	-248	149	TE	2075	-248	199	DUMMY	5312.5	-248
50	C12M	-4352.5	-248	100	VSSA	-1352.5	-248	150	SDO	2160	-248	200	DUMMY	5372.5	-248





No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
201	DUMMY	5432.5	-248	251	G32	7147	224	301	G132	6447	224	351	G232	5747	224
202	DUMMY	5492.5	-248	252	G34	7133	93	302	G134	6433	93	352	G234	5733	93
203	DUMMY	5552.5	-248	253	G36	7119	224	303	G136	6419	224	353	G236	5719	224
204	DUMMY	5612.5	-248	254	G38	7105	93	304	G138	6405	93	354	G238	5705	93
205	DUMMY	5672.5	-248	255	G40	7091	224	305	G140	6391	224	355	G240	5691	224
206	(GND)	5732.5	-248	256	G42	7077	93	306	G142	6377	93	356	G242	5677	93
207	(GND)	5792.5	-248	257	G44	7063	224	307	G144	6363	224	357	G244	5663	224
208	(GND)	5852.5	-248	258	G46	7049	93	308	G146	6349	93	358	G246	5649	93
209	(GND)	5912.5	-248	259	G48	7035	224	309	G148	6335	224	359	G248	5635	224
210	(GND)	5972.5	-248	260	G50	7021	93	310	G150	6321	93	360	G250	5621	93
211	(GND)	6032.5	-248	261	G52	7007	224	311	G152	6307	224	361	G252	5607	224
212	(GND)	6092.5	-248	262	G54	6993	93	312	G154	6293	93	362	G254	5593	93
213	(GND)	6152.5	-248	263	G56	6979	224	313	G156	6279	224	363	G256	5579	224
214	DUMMY	6212.5	-248	264	G58	6965	93	314	G158	6265	93	364	G258	5565	93
215	DUMMY	6272.5	-248	265	G60	6951	224	315	G160	6251	224	365	G260	5551	224
216	DUMMY	6332.5	-248	266	G62	6937	93	316	G162	6237	93	366	G262	5537	93
217	DUMMY	6392.5	-248	267	G64	6923	224	317	G164	6223	224	367	G264	5523	224
218	DUMMY	6452.5	-248	268	G66	6909	93	318	G166	6209	93	368	G266	5509	93
219	DUMMY	6512.5	-248	269	G68	6895	224	319	G168	6195	224	369	G268	5495	224
220	DUMMY	6572.5	-248	270	G70	6881	93	320	G170	6181	93	370	G270	5481	93
221	DUMMY	6632.5	-248	271	G72	6867	224	321	G172	6167	224	371	G272	5467	224
222	DUMMY	6692.5	-248	272	G74	6853	93	322	G174	6153	93	372	G274	5453	93
223	VCOM	6752.5	-248	273	G76	6839	224	323	G176	6139	224	373	G276	5439	224
224	VCOM	6812.5	-248	274	G78	6825	93	324	G178	6125	93	374	G278	5425	93
225	VCOM	6872.5	-248	275	G80	6811	224	325	G180	6111	224	375	G280	5411	224
226	VCOM	6932.5	-248	276	G82	6797	93	326	G182	6097	93	376	G282	5397	93
227	VCOM	6992.5	-248	277	G84	6783	224	327	G184	6083	224	377	G284	5383	224
228	VCOM	7052.5	-248	278	G86	6769	93	328	G186	6069	93	378	G286	5369	93
229	VCOM	7112.5	-248	279	G88	6755	224	329	G188	6055	224	379	G288	5355	224
230	VCOM	7172.5	-248	280	G90	6741	93	330	G190	6041	93	380	G290	5341	93
231	DUMMY	7232.5	-248	281	G92	6727	224	331	G192	6027	224	381	G292	5327	224
232	DUMMY	7292.5	-248	282	G94	6713	93	332	G194	6013	93	382	G294	5313	93
233	DUMMY	7399	224	283	G96	6699	224	333	G196	5999	224	383	G296	5299	224
234	DUMMY	7385	93	284	G98	6685	93	334	G198	5985	93	384	G298	5285	93
235	DUMMY	7371	224	285	G100	6671	224	335	G200	5971	224	385	G300	5271	224
236	G2	7357	93	286	G102	6657	93	336	G202	5957	93	386	G302	5257	93
237	G4	7343	224	287	G104	6643	224	337	G204	5943	224	387	G304	5243	224
238	G6	7329	93	288	G106	6629	93	338	G206	5929	93	388	G306	5229	93
239	G8	7315	224	289	G108	6615	224	339	G208	5915	224	389	G308	5215	224
240	G10	7301	93	290	G110	6601	93	340	G210	5901	93	390	G310	5201	93
241	G12	7287	224	291	G112	6587	224	341	G212	5887	224	391	G312	5187	224
242	G14	7273	93	292	G114	6573	93	342	G214	5873	93	392	G314	5173	93
243	G16	7259	224	293	G116	6559	224	343	G216	5859	224	393	G316	5159	224
244	G18	7245	93	294	G118	6545	93	344	G218	5845	93	394	G318	5145	93
245	G20	7231	224	295	G120	6531	224	345	G220	5831	224	395	G320	5131	224
246	G22	7217	93	296	G122	6517	93	346	G222	5817	93	396	S720	5075	93
247	G24	7203	224	297	G124	6503	224	347	G224	5803	224	397	S719	5061	224
248	G26	7189	93	298	G126	6489	93	348	G226	5789	93	398	S718	5047	93
249	G28	7175	224	299	G128	6475	224	349	G228	5775	224	399	S717	5033	224
250	G30	7161	93	300	G130	6461	93	350	G230	5761	93	400	S716	5019	93





No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
401	S715	5005	224	451	S665	4305	224	501	S615	3605	224	551	S565	2905	224
402	S714	4991	93	452	S664	4291	93	502	S614	3591	93	552	S564	2891	93
403	S713	4977	224	453	S663	4277	224	503	S613	3577	224	553	S563	2877	224
404	S712	4963	93	454	S662	4263	93	504	S612	3563	93	554	S562	2863	93
405	S711	4949	224	455	S661	4249	224	505	S611	3549	224	555	S561	2849	224
406	S710	4935	93	456	S660	4235	93	506	S610	3535	93	556	S560	2835	93
407	S709	4921	224	457	S659	4221	224	507	S609	3521	224	557	S559	2821	224
408	S708	4907	93	458	S658	4207	93	508	S608	3507	93	558	S558	2807	93
409	S707	4893	224	459	S657	4193	224	509	S607	3493	224	559	S557	2793	224
410	S706	4879	93	460	S656	4179	93	510	S606	3479	93	560	S556	2779	93
411	S705	4865	224	461	S655	4165	224	511	S605	3465	224	561	S555	2765	224
412	S704	4851	93	462	S654	4151	93	512	S604	3451	93	562	S554	2751	93
413	S703	4837	224	463	S653	4137	224	513	S603	3437	224	563	S553	2737	224
414	S702	4823	93	464	S652	4123	93	514	S602	3423	93	564	S552	2723	93
415	S701	4809	224	465	S651	4109	224	515	S601	3409	224	565	S551	2709	224
416	S700	4795	93	466	S650	4095	93	516	S600	3395	93	566	S550	2695	93
417	S699	4781	224	467	S649	4081	224	517	S599	3381	224	567	S549	2681	224
418	S698	4767	93	468	S648	4067	93	518	S598	3367	93	568	S548	2667	93
419	S697	4753	224	469	S647	4053	224	519	S597	3353	224	569	S547	2653	224
420	S696	4739	93	470	S646	4039	93	520	S596	3339	93	570	S546	2639	93
421	S695	4725	224	471	S645	4025	224	521	S595	3325	224	571	S545	2625	224
422	S694	4711	93	472	S644	4011	93	522	S594	3311	93	572	S544	2611	93
423	S693	4697	224	473	S643	3997	224	523	S593	3297	224	573	S543	2597	224
424	S692	4683	93	474	S642	3983	93	524	S592	3283	93	574	S542	2583	93
425	S691	4669	224	475	S641	3969	224	525	S591	3269	224	575	S541	2569	224
426	S690	4655	93	476	S640	3955	93	526	S590	3255	93	576	S540	2555	93
427	S689	4641	224	477	S639	3941	224	527	S589	3241	224	577	S539	2541	224
428	S688	4627	93	478	S638	3927	93	528	S588	3227	93	578	S538	2527	93
429	S687	4613	224	479	S637	3913	224	529	S587	3213	224	579	S537	2513	224
430	S686	4599	93	480	S636	3899	93	530	S586	3199	93	580	S536	2499	93
431	S685	4585	224	481	S635	3885	224	531	S585	3185	224	581	S535	2485	224
432	S684	4571	93	482	S634	3871	93	532	S584	3171	93	582	S534	2471	93
433	S683	4557	224	483	S633	3857	224	533	S583	3157	224	583	S533	2457	224
434	S682	4543	93	484	S632	3843	93	534	S582	3143	93	584	S532	2443	93
	S681		224	485	S631	3829	224		S581	3129	224	585	S531	2429	224
436	S680	4515	93	486	S630	3815	93	536	S580	3115	93	586	S530	2415	93
437	S679	4501	224	487	S629	3801	224	537	S579	3101	224	587	S529	2401	224
	S678	4487	93	488	S628	3787	93	538	S578	3087	93	588	S528	2387	93
439	S677	4473	224	489	S627	3773	224	539	S577	3073	224	589	S527	2373	224
440	S676	4459	93	490	S626	3759	93	540	S576	3059	93	590	S526	2359	93
441	S675	4445	224	491	S625	3745	224	541	S575	3045	224	591	S525	2345	224
442	S674	4431	93	492	S624	3731	93	542	S574	3031	93	592	S524	2331	93
	S673	4417	224	493	S623	3717	224	543	S573	3017	224	593	S523	2317	224
443	S672	4403	93	493	S622	3703	93	544	S573	3003	93		S523	2303	93
444	S672 S671	4389	224		S622 S621	3689	224		S572	2989	224	594 595	S522 S521	2289	224
445	S670	4389	93	495 496	S620	3675	93	545	S571		93	595 596	S521	2275	93
446 447	S669		93 224	496	S619			546 547	S569	2975	93 224		S520 S519	22/5	224
		4361				3661	224			2961	1 1	597	1		1 1
448	S668	4347	93	498	S618	3647	93	548	S568	2947	93	598	S518	2247	93
449	S667	4333	224	499	S617	3633	224	549	S567	2933	224	599	S517	2233	224
450	S666	4319	93	500	S616	3619	93	550	S566	2919	93	600	S516	2219	93





No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
601	S515	2205	224	651	S465	1505	224	701	S415	805	224	751	S365	105	224
602	S514	2191	93	652	S464	1491	93	702	S414	791	93	752	S364	91	93
603	S513	2177	224	653	S463	1477	224	703	S413	777	224	753	S363	77	224
604	S512	2163	93	654	S462	1463	93	704	S412	763	93	754	S362	63	93
605	S511	2149	224	655	S461	1449	224	705	S411	749	224	755	S361	49	224
606	S510	2135	93	656	S460	1435	93	706	S410	735	93	756	S360	-49	93
607	S509	2121	224	657	S459	1421	224	707	S409	721	224	757	S359	-63	224
608	S508	2107	93	658	S458	1407	93	708	S408	707	93	758	S358	-77	93
609	S507	2093	224	659	S457	1393	224	709	S407	693	224	759	S357	-91	224
610	S506	2079	93	660	S456	1379	93	710	S406	679	93	760	S356	-105	93
611	S505	2065	224	661	S455	1365	224	711	S405	665	224	761	S355	-119	224
612	S504	2051	93	662	S454	1351	93	712	S404	651	93	762	S354	-133	93
613	S503	2037	224	663	S453	1337	224	713	S403	637	224	763	S353	-147	224
614	S502	2023	93	664	S452	1323	93	714	S402	623	93	764	S352	-161	93
615	S501	2009	224	665	S451	1309	224	715	S401	609	224	765	S351	-175	224
616	S500	1995	93	666	S450	1295	93	716	S400	595	93	766	S350	-189	93
617	S499	1981	224	667	S449	1281	224	717	S399	581	224	767	S349	-203	224
618	S498	1967	93	668	S448	1267	93	718	S398	567	93	768	S348	-217	93
619	S497	1953	224	669	S447	1253	224	719	S397	553	224	769	S347	-231	224
620	S496	1939	93	670	S446	1239	93	720	S396	539	93	770	S346	-245	93
621	S495	1925	224	671	S445	1225	224	721	S395	525	224	771	S345	-259	224
622	S494	1911	93	672	S444	1211	93	722	S394	511	93	772	S344	-273	93
623	S493	1897	224	673	S443	1197	224	723	S393	497	224	773	S343	-287	224
624	S492	1883	93	674	S442	1183	93	724	S392	483	93	774	S342	-301	93
625	S491	1869	224	675	S441	1169	224	725	S391	469	224	775	S341	-315	224
626	S490	1855	93	676	S440	1155	93	726	S390	455	93	776	S340	-329	93
627	S489	1841	224	677	S439	1141	224	727	S389	441	224	777	S339	-343	224
628	S488	1827	93	678	S438	1127	93	728	S388	427	93	778	S338	-357	93
629	S487	1813	224	679	S437	1113	224	729	S387	413	224	779	S337	-371	224
630	S486	1799	93	680	S436	1099	93	730	S386	399	93	780	S336	-385	93
631	S485	1785	224	681	S435	1085	224	731	S385	385	224	781	S335	-399	224
632	S484	1771	93	682	S434	1071	93	732	S384	371	93	782	S334	-413	93
633	S483	1757	224	683	S433	1057	224	733	S383	357	224	783	S333	-427	224
634	S482	1743	93	684	S432	1043	93	734	S382	343	93	784	S332	-441	93
635	S481	1729	224	685	S431	1029	224	735	S381	329	224	785	S331	-455	224
636	S480	1715	93	686	S430	1015	93	736	S380	315	93	786	S330	-469	93
637	S479	1701	224	687	S429	1001	224	737	S379	301	224	787	S329	-483	224
638	S478	1687	93	688	S428	987	93	738	S378	287	93	788	S328	-497	93
639	S477	1673	224	689	S427	973	224	739	S377	273	224	789	S327	-511	224
640	S476	1659	93	690	S426	959	93	740	S376	259	93	790	S326	-525	93
641	S475	1645	224	691	S425	945	224	741	S375	245	224	791	S325	-539	224
642	S474	1631	93	692	S424	931	93	742	S374	231	93	792	S324	-553	93
643	S473	1617	224	693	S423	917	224	743	S373	217	224	793	S323	-567	224
644	S472	1603	93	694	S422	903	93	744	S372	203	93	794	S322	-581	93
645	S471	1589	224	695	S421	889	224	745	S371	189	224	795	S321	-595	224
646	S470	1575	93	696	S420	875	93	746	S370	175	93	796	S320	-609	93
647	S469	1561	224	697	S419	861	224	747	S369	161	224	797	S319	-623	224
648	S468	1547	93	698	S418	847	93	748	S368	147	93	798	S318	-637	93
649	S467	1533	224	699	S417	833	224	749	S367	133	224	799	S317	-651	224
650	S466	1519	93	700	S416	819	93	750	S366	119	93	800	S316	-665	93





Bot Sa15	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ	No.	Pad name	Х	Υ
902 8314				224		S265		224				224				224
803 \$313 707 224 853 \$263 -1407 224 903 \$213 -210 224 953 \$163 -2007 804 \$312 -721 93 854 \$562 -1442 93 905 \$211 213 224 955 \$261 -2235 48 162 -2821 806 \$300 -763 224 857 \$259 -1443 224 905 \$211 213 224 955 \$160 -28263 807 \$309 -763 224 859 \$2559 -1497 39 908 \$200 2216 2824 957 \$159 2268 809 \$307 -791 224 859 \$257 -1491 224 907 \$209 \$207 2191 224 915 \$158 289 956 \$156 309 916 \$200 \$201 \$260 \$261 \$241 \$241 \$241 \$24				93		S264		93	902	1	-2093	93		S164		93
805 \$311 .735 224 855 \$261 .1435 224 905 \$211 .2135 224 955 \$161 .2835 806 \$310 .749 93 856 \$269 .1463 224 907 \$209 .2163 224 957 \$299 .1263 224 907 \$309 \$300 .777 93 858 \$258 .1477 93 908 \$209 .2177 93 958 \$157 .2881 908 \$200 .2177 93 958 \$157 .2881 909 \$207 .2191 224 951 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 959 \$157 .2881 911 \$205 .2219 .224 961 \$155 .2916 .952 .1561 93 911 \$205 .2247 2	803	S313	-707	224	853	S263	-1407	224	903	S213	-2107	224	953	S163	-2807	224
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808 \$308 -777 93 858 \$258 1477 93 908 \$2007 -791 224 859 \$257 1491 224 909 \$207 -2191 224 909 \$11 \$306 \$306 805 39 860 \$256 \$1509 909 \$207 -2191 224 909 \$155 2255 93 908 \$205 959 \$157 -2891 224 961 \$155 -2919 94 \$12 \$304 833 93 862 \$254 1153 93 911 \$205 -2219 224 961 \$155 -2919 93 861 \$253 11561 93 912 \$204 -2233 93 962 \$154 -2933 93 962 \$154 -2931 941 \$202 -2261 93 962 \$154 -2933 93 965 \$151 -2989 861 \$151 -2989 914 \$202 <td< td=""><td>807</td><td>S309</td><td>-763</td><td>224</td><td>857</td><td>S259</td><td>-1463</td><td>224</td><td>907</td><td></td><td>-2163</td><td>224</td><td>957</td><td>S159</td><td>-2863</td><td>224</td></td<>	807	S309	-763	224	857	S259	-1463	224	907		-2163	224	957	S159	-2863	224
810 \$306 -805 93 860 \$256 -1505 93 910 \$206 2219 224 961 \$255 -1519 224 961 \$255 -1519 224 961 \$255 -2919 224 961 \$155 2219 224 961 \$155 2291 224 961 \$155 2219 224 963 \$155 2219 224 963 \$155 221 363 \$255 -1561 93 914 \$202 -2261 93 964 \$152 -2961 804 \$152 -1561 93 914 \$202 -2261 93 966 \$150 -2993 964 \$152 -2967 91 224 865 \$250 -1589 93 916 \$200 -2289 93 966 \$150 -2969 91 91 224 869 \$151 -22975 91 224 868 \$249 -1603 224 917 <td< td=""><td>808</td><td>S308</td><td>-777</td><td>93</td><td>858</td><td>S258</td><td>-1477</td><td>93</td><td>908</td><td>S208</td><td>-2177</td><td>93</td><td>958</td><td>S158</td><td>-2877</td><td>93</td></td<>	808	S308	-777	93	858	S258	-1477	93	908	S208	-2177	93	958	S158	-2877	93
811 \$305 819 \$24 861 \$255 1519 \$24 911 \$204 \$219 \$24 961 \$155 \$2919 812 \$304 833 93 947 \$24 863 \$253 1547 \$224 913 \$203 \$2247 \$244 963 \$153 \$2937 \$246 \$66 \$251 1575 \$224 \$158 \$203 \$247 \$224 \$66 \$255 \$1589 \$203 \$224 \$66 \$150 \$2969 \$966 \$150 \$2989 \$93 \$66 \$150 \$2989 \$93 \$66 \$150 \$2989 \$93 \$66 \$150 \$2989 \$93 \$66 \$1510 \$296 \$945 \$93 \$66 \$250 \$1589 \$201 \$22289 \$93 \$66 \$1510 \$2989 \$93 \$66 \$1510 \$2989 \$93 \$168 \$248 \$178 \$248 \$178 \$248 \$178 \$248 <t< td=""><td>809</td><td>S307</td><td>-791</td><td>224</td><td>859</td><td>S257</td><td>-1491</td><td>224</td><td>909</td><td>S207</td><td>-2191</td><td>224</td><td>959</td><td>S157</td><td>-2891</td><td>224</td></t<>	809	S307	-791	224	859	S257	-1491	224	909	S207	-2191	224	959	S157	-2891	224
811 \$305 819 \$24 861 \$255 -1519 \$24 911 \$205 -2219 \$24 961 \$155 -2919 812 \$304 -833 93 947 \$244 863 \$253 -1547 \$24 863 \$253 -1547 \$24 863 \$253 -1547 \$24 863 \$253 -1576 \$244 863 \$255 -1561 93 914 \$202 -2261 93 964 \$152 -2961 816 \$300 -889 93 866 \$250 -1589 93 916 \$200 -2289 93 966 \$150 -2969 817 \$299 -903 \$224 866 \$250 -1631 \$24 917 \$199 \$2303 \$24 9667 \$149 9003 \$146 \$93 \$165 \$2919 \$165 \$201 \$2289 93 9667 \$149 903 \$146 \$149	810	S306	-805	93	860	S256	-1505	93	910	S206	-2205	93	960	S156	-2905	93
813 \$303 -847 224 863 \$253 -1547 224 913 \$203 -2247 224 963 \$152 -2961 815 \$3001 -875 224 865 \$251 -1575 224 915 \$201 -2275 224 965 \$151 -2975 816 \$3001 -889 93 866 \$250 -1589 93 916 \$200 -2289 93 966 \$150 -2988 817 \$299 -903 224 867 \$249 -1603 224 917 \$199 -2303 224 967 \$149 -3003 818 \$298 -917 93 868 \$248 -1631 224 917 \$199 -2303 224 966 \$147 -3031 819 \$297 -931 224 869 \$247 -1631 224 918 \$197 -2345 93 966 \$147 <t< td=""><td></td><td>S305</td><td>-819</td><td>224</td><td></td><td>S255</td><td>-1519</td><td>224</td><td>911</td><td>S205</td><td>-2219</td><td>224</td><td>961</td><td>S155</td><td>-2919</td><td>224</td></t<>		S305	-819	224		S255	-1519	224	911	S205	-2219	224	961	S155	-2919	224
814 S302 -861 93 864 S252 -1561 93 914 S202 -2261 93 964 S152 -2961 816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 817 S299 -903 224 867 S249 -1603 224 917 S199 -2303 224 967 S149 -3003 818 S298 -917 93 868 S248 -1617 93 918 S197 -2331 224 967 S149 -3003 820 S296 -945 39 870 S246 -1645 93 970 S146 -3045 821 S295 -959 224 871 S245 -1669 224 921 S195 -2359 224 971 S145 -3069 822 S292 -1001 </td <td>812</td> <td>S304</td> <td>-833</td> <td>93</td> <td>862</td> <td>S254</td> <td>-1533</td> <td>93</td> <td>912</td> <td>S204</td> <td>-2233</td> <td>93</td> <td>962</td> <td>S154</td> <td>-2933</td> <td>93</td>	812	S304	-833	93	862	S254	-1533	93	912	S204	-2233	93	962	S154	-2933	93
814 S302 -861 93 864 S252 -1561 93 914 S202 -2261 93 964 S152 -2961 816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 817 S299 -903 224 867 S249 -1603 224 917 S199 -2303 224 967 S149 -3003 818 S298 -917 93 868 S248 -1617 93 918 S197 -2331 224 967 S149 -3003 820 S296 -945 39 870 S246 -1645 93 970 S146 -3045 821 S295 -959 224 871 S245 -1669 224 921 S195 -2359 224 971 S145 -3069 822 S292 -1001 </td <td>813</td> <td>S303</td> <td>-847</td> <td>224</td> <td>863</td> <td>S253</td> <td>-1547</td> <td>224</td> <td>913</td> <td>S203</td> <td>-2247</td> <td>224</td> <td>963</td> <td>S153</td> <td>-2947</td> <td>224</td>	813	S303	-847	224	863	S253	-1547	224	913	S203	-2247	224	963	S153	-2947	224
816 S300 -889 93 866 S250 -1589 93 916 S200 -2289 93 966 S150 -2989 817 S299 -903 224 867 S249 -1603 224 917 S199 -2303 224 967 5149 -3003 818 S298 -917 33 868 S248 -1617 93 918 S198 -2317 23 968 S148 -3017 820 S296 -945 93 870 S246 -1645 93 920 S196 -2345 93 970 S146 -3045 821 S293 -997 224 873 S243 -1667 224 921 S196 -2345 93 972 S144 -3073 822 S293 -987 224 873 S243 -1667 224 923 S193 -2367 224 971 S144 -3073	814	S302	-861	93	864	S252	-1561	93	914		-2261	93	964	S152	-2961	93
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819 S297 -931 224 869 S247 -1631 224 919 S197 -2331 224 969 S147 -3031 820 S296 -945 93 820 S294 -973 33 871 S245 -1659 224 921 S196 -2345 93 970 S146 -3045 822 S294 -973 38 787 S244 -1673 33 922 S194 -2373 93 972 S144 -3073 824 S292 -1001 93 874 S242 -1701 93 924 S192 -2401 93 973 S143 -3067 826 S290 -1015 224 875 S241 -1715 224 925 S191 -2415 224 975 S141 -3101 826 S290 -1043 224 876 S241 -1772 93 928 S199 -24		S299	-903	224		S249	-1603	224	917		-2303	224	967	S149	-3003	224
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821 S295 -959 224 871 S245 -1659 224 921 S195 -2359 224 971 S145 -3059 822 S294 -973 93 873 S244 -1673 93 922 S194 -2373 93 972 S144 -3073 824 S292 -1001 93 874 S242 -1701 93 924 S192 -2401 93 974 S142 -3101 826 S291 -1015 224 875 S241 -1715 224 925 S191 -2415 224 975 S141 -3115 826 S290 -1029 93 876 S240 -1729 93 926 S190 -2429 93 976 S140 -3129 829 S287 -1071 224 877 S239 -1771 224 925 S189 -2443 224 977 S139		S296		93		S246		93	920			93				93
822 S294 -973 93 872 S244 -1673 93 922 S194 -2373 93 972 S144 -3073 823 S293 -987 224 873 S243 -1687 224 923 S193 -2387 224 973 S143 -3087 824 S292 -1001 93 874 S242 -1701 93 926 S190 -2401 93 976 S140 -3101 93 976 S140 -3101 925 S191 -2415 224 977 S139 -3143 -315 926 S190 -2429 93 976 S140 -3129 928 8190 -2443 224 977 S139 -3143 828 -2488 -1057 93 878 S238 -1757 93 928 S188 -2457 93 978 S133 -3143 936 S186 -2485 93 980 S136																224
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824 \$292 -1001 93 874 \$242 -1701 93 924 \$192 -2401 93 974 \$142 -3101 825 \$291 -1015 \$224 875 \$241 -1715 \$224 925 \$191 -2415 \$224 975 \$141 -3115 826 \$290 -1029 93 876 \$240 -1729 93 926 \$190 -2429 93 977 \$139 3143 828 \$288 -1057 93 878 \$239 -1773 328 \$188 -2457 93 978 \$133 -3143 829 \$287 -1071 \$224 879 \$237 -1775 93 988 \$188 -2457 93 978 \$133 -3171 830 \$286 -1085 93 880 \$236 -1785 93 930 \$186 -2485 93 980 \$136 -3185 <																224
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826 S290 -1029 93 876 S240 -1729 93 926 S190 -2429 93 976 S140 -3129 827 S289 -1043 224 878 S239 -1743 224 927 S189 -2443 224 977 S139 -3143 828 S288 -1057 93 878 S238 -1757 93 928 S188 -2457 93 976 S139 -3143 829 S287 -1071 224 879 S237 -1771 224 929 S187 -2471 224 979 S137 -3171 830 S286 -1089 93 880 S236 -1785 93 930 S186 -2485 93 980 S136 -3185 831 S281 -1113 93 882 S234 -1813 93 932 S184 -2513 93 982 S134 -																224
827 S289 -1043 224 877 S239 -1743 224 927 S189 -2443 224 977 S139 -3143 828 S288 -1057 93 878 S238 -1757 93 928 S188 -2457 93 978 S138 -3157 829 S286 -1085 93 880 S236 -1785 93 930 S186 -2485 93 980 S136 -3171 8315 -2471 224 979 S137 -3171 831 2828 -1085 93 880 S236 -1785 93 930 S186 -2485 93 980 S136 -3185 930 S186 -2485 93 981 S231			-1029	93				93		1		1				93
828 S288 -1057 93 878 S238 -1757 93 928 S188 -2457 93 978 S138 -3157 829 S287 -1071 224 879 S237 -1771 224 929 S187 -2471 224 979 S137 -3171 830 S286 -1085 93 880 S236 -1785 93 980 S136 -3185 831 S285 -1099 224 881 S235 -1799 224 931 S186 -2485 93 980 S136 -3185 833 S283 -1127 224 883 S233 -1827 224 933 S186 -2499 224 981 S135 -3199 835 S281 -1141 93 884 S232 -1841 93 933 S183 -2527 224 985 S131 -3251 836 S280 <td< td=""><td>827</td><td>S289</td><td>-1043</td><td>224</td><td>877</td><td>S239</td><td>-1743</td><td>224</td><td>927</td><td>S189</td><td>-2443</td><td>224</td><td>977</td><td>S139</td><td>-3143</td><td>224</td></td<>	827	S289	-1043	224	877	S239	-1743	224	927	S189	-2443	224	977	S139	-3143	224
829 S287 -1071 224 879 S237 -1771 224 929 S187 -2471 224 979 S137 -3171 830 S286 -1085 93 880 S236 -1785 93 930 S186 -2485 93 980 S136 -3185 831 S285 -1099 224 881 S235 -1799 224 832 S284 -1113 93 882 S234 -1813 93 932 S184 -2513 93 982 S134 -3199 833 S283 -1127 224 883 S233 -1827 224 933 S183 -2527 224 983 S133 -3227 834 S282 -1141 93 884 S232 -1841 93 934 S182 -2541 93 984 S132 -3241 835 S281 -1169 93 886 S2	828	S288	-1057	93	878	S238	-1757	93	928	S188	-2457		978	S138	-3157	93
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832 \$\scrip{834}\$ -1113 93 \$\scrip{882}\$ \$\scrip{224}\$ \$\scrip{883}\$ \$\scrip{224}\$ \$\scrip{884}\$ \$\scrip{224}\$ \$\scrip{884}\$ \$\scrip{224}\$ \$\scrip{884}\$ \$\scrip{224}\$ \$\scrip{884}\$ \$\scrip{224}\$ \$\scrip{885}\$ \$\scrip{244}\$ \$\scrip{983}\$ \$\scrip{133}\$ \$\scrip{982}\$ \$\scrip{983}\$ \$\scrip{133}\$ \$\scrip{9227}\$ \$\scrip{984}\$ \$\scrip{133}\$ \$\scrip{9227}\$ \$\scrip{984}\$ \$\scrip{133}\$ \$\scrip{9227}\$ \$\scrip{983}\$ \$\scrip{133}\$ \$\scrip{9227}\$ \$\scrip{983}\$ \$\scrip{133}\$ \$\scrip{9227}\$ \$\scrip{984}\$ \$\scrip{133}\$ \$\scrip{9227}\$ \$\scrip{983}\$ \$\scrip{134}\$ \$\scrip{9224}\$ \$\scrip{983}\$ \$\scrip{983}\$ \$\scrip{133}\$ \$\scrip{9227}\$ \$\scrip{985}\$ \$\scrip{131}\$ \$\scrip{9224}\$ \$\scrip{985}\$ \$\scrip{134}\$ \$\scrip{9213}\$	830	S286	-1085	93	880	S236	-1785	93	930	S186	-2485	93	980	S136	-3185	93
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1031 S85 -3899 224 1032 S84 -3913 93 1033 S83 -3927 224 1034 S82 -3941 93 1035 S81 -3955 224 1036 S80 -3969 93 1038 S78 -3997 93 1039 S77 -4011 224 1040 S76 -4025 93 1041 S75 -4039 224 1091 S25 -4739 224 11131 G289 -5341 224 1133 G285 -5369 224 1134 G283 -5383 93 1184 G187 -60 1135 G281 -5397 224 1136 G279 -5411 93 1136 G279 -5411 93 1136 G279 -5425 224 1137 G277		-6027		1180	93		G291	1130	93		S36	1080	93	-3885	S86	
1032 S84 -3913 93 1033 S83 -3927 224 1034 S82 -3941 93 1035 S81 -3955 224 1036 S80 -3969 93 1037 S79 -3983 224 1038 S78 -3997 93 1039 S77 -4011 224 1040 S76 -4025 93 1041 S75 -4039 224	041 22	-6041	3189	1181	224	-5341	G289	1131	224	-4599		1081	224		S85	1031
1034 S82 -3941 93 1035 S81 -3955 224 1036 S80 -3969 93 1037 S79 -3983 224 1038 S78 -3997 93 1039 S77 -4011 224 1040 S76 -4025 93 1041 S75 -4039 224 1091 S25 -4739 224 1134 G283 -5383 93 1135 G281 -5397 224 1136 G279 -5411 93 1136 G279 -5411 93 1137 G277 -5425 224 1138 G275 -5439 93 1188 G175 -61 1139 G273 -5453 224 1140 G271 -5467 93 1141 G269 -5481 224 1191 G169	055 93	-6055	3187	1182	93	-5355	G287	1132	93	-4613		1082	93	-3913	S84	1032
1035 S81 -3955 224 1036 S80 -3969 93 1037 S79 -3983 224 1038 S78 -3997 93 1039 S77 -4011 224 1040 S76 -4025 93 1041 S75 -4039 224 1091 S25 -4739 224 1135 G281 -5397 224 1136 G279 -5411 93 1137 G277 -5425 224 1138 G275 -5439 93 1188 G177 -61 1138 G275 -5439 93 1140 G271 -5467 93 1140 G271 -5467 93 1190 G171 -61 1141 G269 -5481 224 1191 G169 -61	069 22	-6069	3185	1183	224	-5369	G285	1133	224	-4627	S33	1083	224	-3927	S83	1033
1036 S80 -3969 93 1086 S30 -4669 93 1136 G279 -5411 93 1186 G179 -61 1037 S79 -3983 224 1087 S29 -4683 224 1137 G277 -5425 224 1187 G177 -61 1038 S78 -3997 93 1088 S28 -4697 93 1138 G275 -5439 93 1188 G175 -61 1039 S77 -4011 224 1089 S27 -4711 224 1139 G273 -5453 224 1189 G173 -61 1040 S76 -4025 93 1090 S26 -4725 93 1140 G271 -5467 93 1190 G171 -61 1041 S75 -4039 224 1091 S25 -4739 224 1141 G269 -5481 224 1191 G169	083 93	-6083	3183	1184	93	-5383	G283	1134	93	-4641	S32	1084	93	-3941	S82	1034
1036 S80 -3969 93 1086 S30 -4669 93 1136 G279 -5411 93 1186 G179 -61 1037 S79 -3983 224 1087 S29 -4683 224 1137 G277 -5425 224 1187 G177 -61 1038 S78 -3997 93 1088 S28 -4697 93 1138 G275 -5439 93 1188 G175 -61 1039 S77 -4011 224 1089 S27 -4711 224 1139 G273 -5453 224 1189 G173 -61 1040 S76 -4025 93 1090 S26 -4725 93 1140 G271 -5467 93 1190 G171 -61 1041 S75 -4039 224 1091 S25 -4739 224 1141 G269 -5481 224 1191 G169	097 22	-6097	3181	1185	224	-5397	G281	1135	224	-4655	S31	1085	224	-3955	S81	1035
1037 S79 -3983 224 1038 S78 -3997 93 1039 S77 -4011 224 1040 S76 -4025 93 1041 S75 -4039 224 1090 S25 -4739 224 11137 G277 -5425 224 11187 G177 -61 1138 G275 -5439 93 1139 G273 -5453 224 1140 G271 -5467 93 1190 G171 -61 1141 G269 -5481 224 1191 G169 -61		-6111					G279								S80	
1038 S78 -3997 93 1039 S77 -4011 224 1040 S76 -4025 93 1041 S75 -4039 224 1090 S26 -4725 93 11138 G275 -5439 93 11188 G175 -61 1139 G273 -5453 224 1140 G271 -5467 93 1190 G171 -61 1141 G269 -5481 224 1191 G169 -61		-6125		1187	224					-4683		1087				
1039 S77 -4011 224 1040 S76 -4025 93 1041 S75 -4039 224 1090 S26 -4725 93 1041 S75 -4039 224 1091 S25 -4739 224 11140 G271 -5467 93 1141 G269 -5481 224 1191 G169 -61		-6139					1									
1040 S76 -4025 93 1090 S26 -4725 93 1140 G271 -5467 93 1190 G171 -61 1041 S75 -4039 224 1091 S25 -4739 224 1141 G269 -5481 224 1191 G169 -61		-6153			224		i e									
1041 S75 -4039 224 1091 S25 -4739 224 1141 G269 -5481 224 1191 G169 -61		-6167			93		l .				S26					
		-6181			224											
1042 S74 -4053 93 1092 S24 -4753 93 1142 G267 -5495 93 1192 G167 -61		-6195					1									
		-6209														
		-6223														
		-6237														
		-6251					l .									
		-6265														
		-6279					1									
		-6293														



		.,		
No.	Pad name	Х	Υ	
1201	G149	-6321	224	1.
1202	G147	-6335	93	1
1203	G145	-6349	224	1:
1204	G143	-6363	93	1
1205	G141	-6377	224	1:
1206	G139	-6391	93	1:
1207	G137	-6405	224	1
1208	G135	-6419	93	13
1209	G133	-6433	224	1:
1210	G131	-6447	93	1
1211	G129	-6461	224	1:
1212	G127	-6475	93	1:
1213	G125	-6489	224	1:
1214	G123	-6503	93	1:
1215	G121	-6517	224	1:
1216	G119	-6531	93	1:
1217	G117	-6545	224	1:
1218	G115	-6559	93	1:
1219	G113	-6573	224	1:
1220	G111	-6587	93	1:
1221	G109	-6601	224	1:
1222	G107	-6615	93	1:
1223	G105	-6629	224	1:
1224	G103	-6643	93	1:
1225	G101	-6657	224	1:
1226	G99	-6671	93	1:
1227	G97	-6685	224	1:
1228	G95	-6699	93	1:
1229	G93	-6713	224	
1230	G91	-6727	93	
1231	G89	-6741	224	
1232	G87	-6755	93	
1233	G85	-6769	224	
1234	G83	-6783	93	
1235	G81	-6797	224	
1236	G79	-6811	93	
1237	G77	-6825	224	
1238	G75	-6839	93	
1239	G73	-6853	224	
1240	G71	-6867	93	
1241	G69	-6881	224	
1242	G67	-6895	93	
1243	G65	-6909	224	
1244	G63	-6923	93	
1245	G61	-6937	224	
1246	G59	-6951	93	
1247	G57	-6965	224	
1248	G55	-6979	93	
1015	0.50	2225		

1249 G53

1250 G51

-6993 224

-7007 93

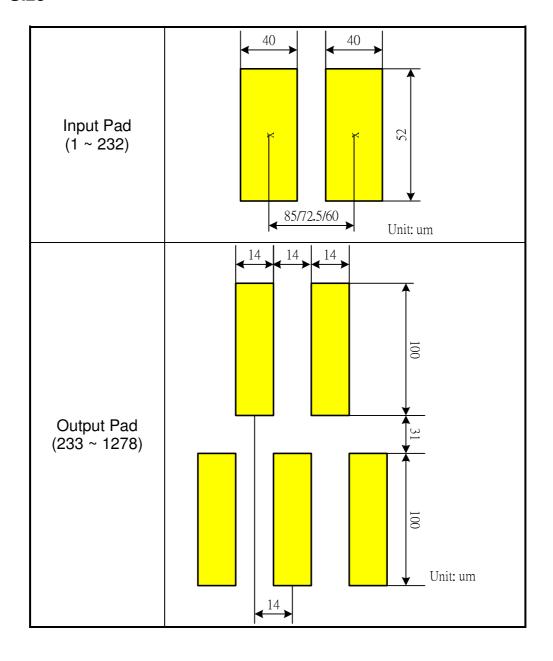
,	No.	Pad name	Χ	Υ
4	1251	G49	-7021	224
	1252	G47	-7035	93
4	1253	G45	-7049	224
	1254	G43	-7063	93
4	1255	G41	-7077	224
	1256	G39	-7091	93
4	1257	G37	-7105	224
	1258	G35	-7119	93
4	1259	G33	-7133	224
	1260	G31	-7147	93
4	1261	G29	-7161	224
	1262	G27	-7175	93
4	1263	G25	-7189	224
	1264	G23	-7203	93
4	1265	G21	-7217	224
	1266	G19	-7231	93
4	1267	G17	-7245	224
	1268	G15	-7259	93
4	1269	G13	-7273	224
	1270	G11	-7287	93
4	1271	G9	-7301	224
	1272	G7	-7315	93
4	1273	G5	-7329	224
	1274	G3	-7343	93
4	1275	G1	-7357	224
	1276	DUMMY	-7371	93
4	1277	DUMMY	-7385	224
	1278	DUMMY	-7399	93
4		<u></u>	-	

Alignment mark	X	Υ
Left COG Align	-7480	225
Right COG Align	7480	225





BUMP Size







6. Block Function Description

MCU System Interface

ILI9341 provides four kinds of MCU system interface with 8080- I /8080- II series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IMO	MCU-Interface Mode	Pins in use				
IIVIO	IIVIZ	IIVII	IIVIO	MCO-interface Mode	Register/Content	GRAM			
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX			
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX			
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX			
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0] D[17:0],WRX,RDX,CSX,D/C				
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX				
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX				
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1] D[17:10],D[8:1],WRX,RDX,CSX				
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10] D[17:10],WRX,RDX,CSX,D/				
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1] D[17:0],WRX,RDX,CSX,D/C				
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10] D[17:9],WRX,RDX,CSX,D/CX				
1	1	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO, CSX				
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,D/CX,SDO, CSX				

In 8080- I /8080- II series parallel interface, the registers are accessed by the D[17:0] data pins.

	8080- I	Series			8080- п	Series		Operation
CSX	D/CX	RDX	WRX	CSX	D/CX	RDX	WRX	
"L"	"L"	"H"		"L"	"L"	"H"		Write command
"L"	"H"		"H"	"L"	"H"		"H"	Read parameter
"L"	"H"	"H"		"L"	"H"	"H"		Write parameter

Parallel RGB Interface

ILI9341 also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9341 can display maximum 262,144 colors.





Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as GVDD, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9341 incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 720-output source driver (S1~S720), 320-output gate driver (G1~G320), and VCOM signal.





7. Function Description

7.1. MCU interfaces

ILI9341 provides the 8-/9-/16-/18-bit parallel system interface for 8080- I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IMO	11/44	IMO	MCU-Interface Mode	Pins in use			
IIVI3	IM2	IM1	IM0	MCO-Interface Mode	Register/Content	GRAM		
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0] D[7:0],WRX,RDX,CSX,D/C			
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0] D[15:0] ,WRX,RDX,CSX,D/0			
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0] D[8:0] ,WRX,RDX,CSX,D/C			
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0] D[17:0] ,WRX,RDX,CSX,D/C			
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX			
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX			
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1] D[17:10],D[8:1],WRX,RDX,CS			
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10] D[17:10],WRX,RDX,CSX,D/			
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1] D[17:0],WRX,RDX,CSX,D/C			
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10] D[17:9],WRX,RDX,CSX,D/CX			
1	1	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO, CSX			
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,D/CX,SDO, CSX			





7.1.2. 8080- I Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080- I series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080- I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080- I Interface selection is done when IM3 pin is low state (VSS level). Interface bus width can be selected by IM [2:0] bits.

The selection of 8080- I series parallel interface is shown as the table in the following.

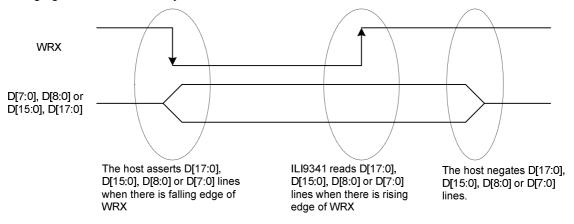
IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
					"L"	<u></u>	"H"	"L"	Write command code.
0	0	0	0	0000 MOLLO hit hun interfere. I	"L"	"H"	ſ	"H"	Read internal status.
0	0	0	0	8080 MCU 8-bit bus interface I	"L"	$ \downarrow $	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
					"L"	ſ	"H"	"L"	Write command code.
0	0	0	4	0000 MOLL to bit bus interfered.	"L"	"H"	ſ	"H"	Read internal status.
0	0	0	1	8080 MCU 16-bit bus interface I	"L"	\vdash	"H"	"H"	Write parameter or display data.
					"L"	"H"	ſ	"H"	Reads parameter or display data.
					"L"		"H"	"L"	Write command code.
0	0	1	0	8080 MCU 9-bit bus interface 1	"L"	"H"		"H"	Read internal status.
0	0	ı	U	8080 MCO 9-bit bus interface 1	"L"	\vdash	"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
					"L"	\vdash	"H"	"L"	Write command code.
		4	4	8080 MCU 18-bit bus interface I	"L"	"H"	<u></u>	"H"	Read internal status.
0	0	1	1	OUOU MOU 18-DIL DUS INTERIACE 1	"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.



7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080- I MCU interface.



Note: WRX is an unsynchronized signal (It can be stopped)



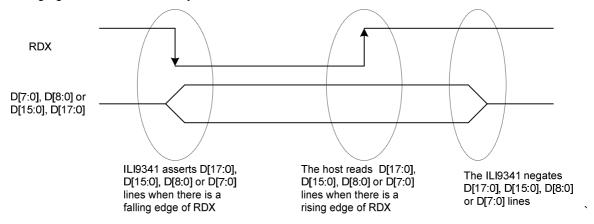




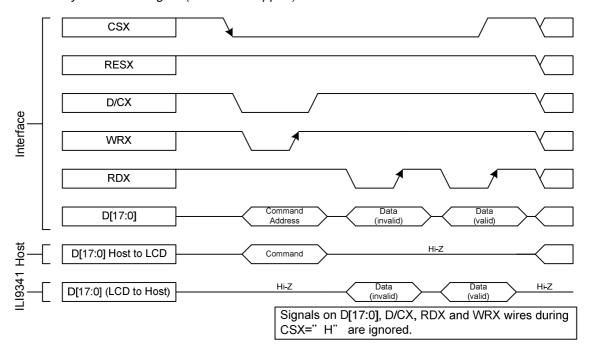
7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- I MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.





7.1.5. 8080- II Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080- series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

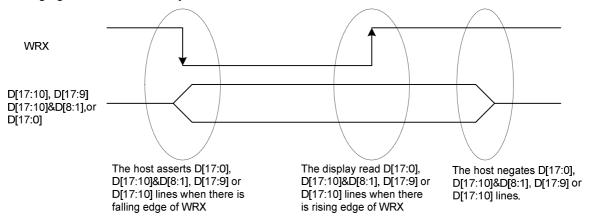
The 8080- II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080- II Interface selection is done when IM3 pin is high state (VDDI level). Interface bus width can be selected by IM [2:0] bits.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
1	0	0	0	8080 MCU 16-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"	$ \leftarrow $	"H"	Read internal status.
					"L"	\vdash	"H"	"H"	Write parameter or display data.
					"L"	"H"	$ \leftarrow $	"H"	Reads parameter or display data.
	0	0	1	8080 MCU 8-bit bus interface II	"L"		"H"	"L"	Write command code.
1					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
	0	1	0	8080 MCU 18-bit bus interface II	"L"		"H"	"L"	Write command code.
1					"L"	"H"	\vdash	"H"	Read internal status.
					"L"	\vdash	"H"	"H"	Write parameter or display data.
					"L"	"H"	\vdash	"H"	Reads parameter or display data.
	0	1	1	8080 MCU 9-bit bus interface II	"L"		"H"	"L"	Write command code.
1					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"	ſ	"H"	Reads parameter or display data.

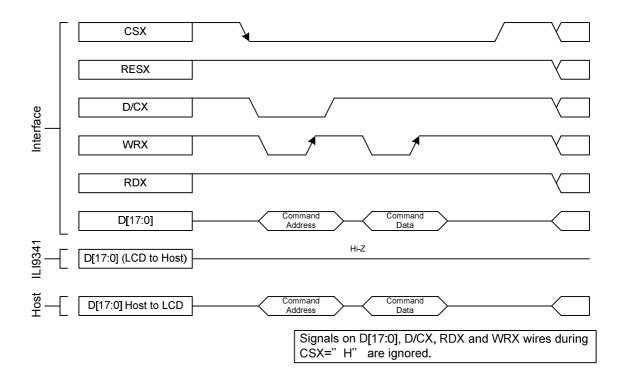


7.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.



Note: WRX is an unsynchronized signal (It can be stopped)



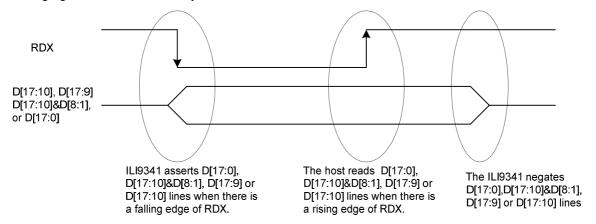




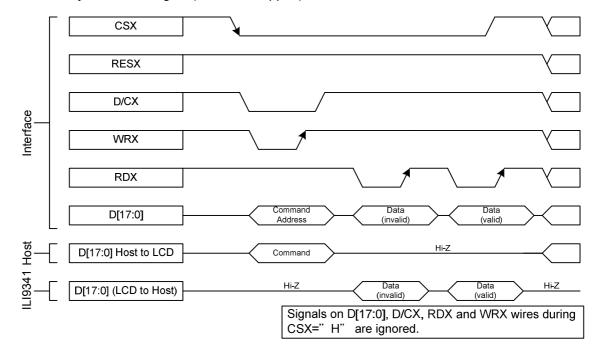
7.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- II MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.





7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

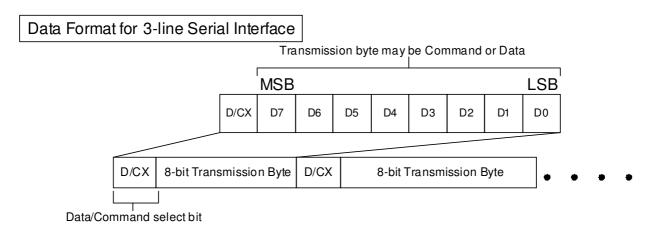
IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	"L"	-		Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	"L"	'H/L"	ſ	Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	"L"	-	ſ	Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	"L"	'H/L"	ſ	Read/Write command, parameter or display data.

ILI9341 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9341. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to ILI9341. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

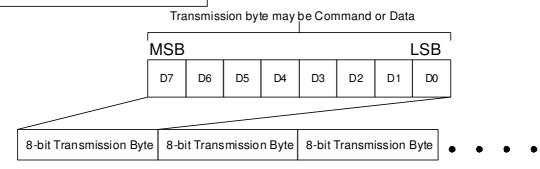
Any instruction can be sent in any order to ILI9341 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.







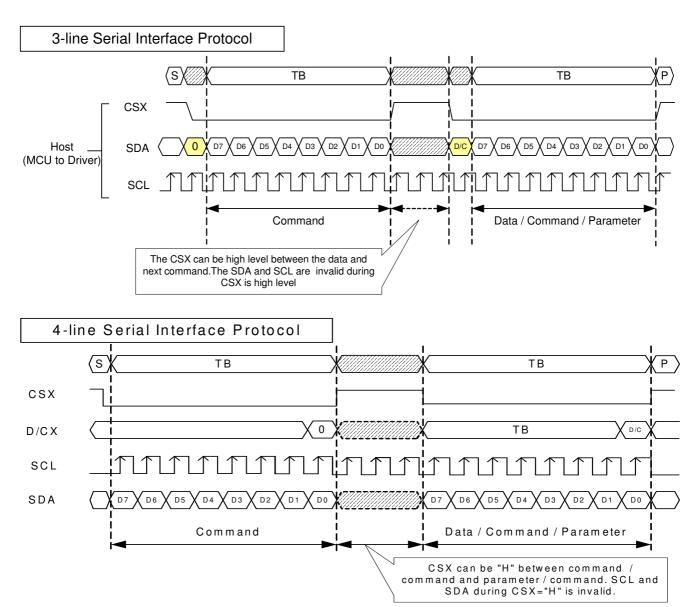
Data Format for 4-line Serial Interface







Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI93401 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.



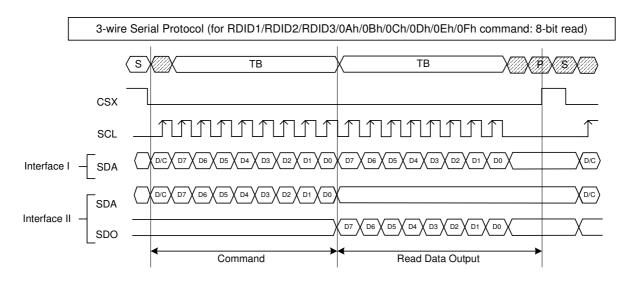


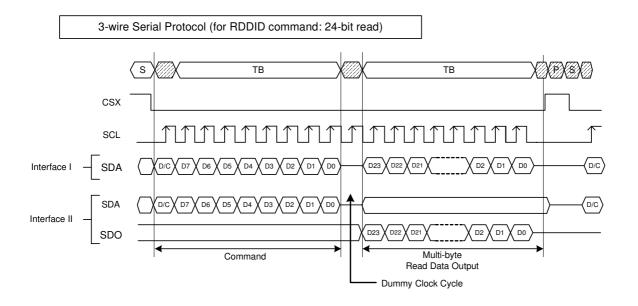


7.1.10. Read Cycle Sequence

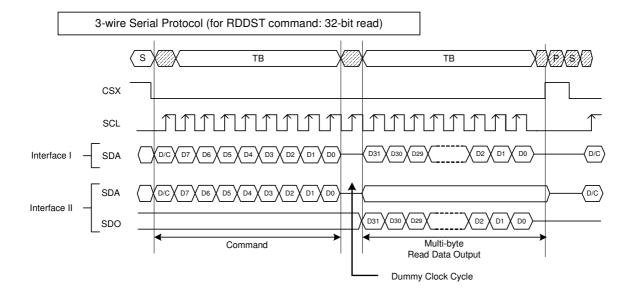
The read mode of interface means that the host reads register's parameter or display data from ILI9341. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9341 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol





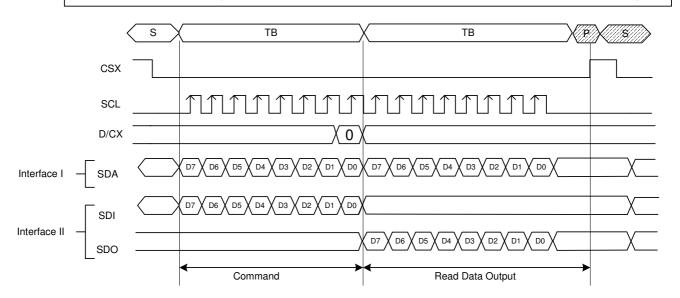




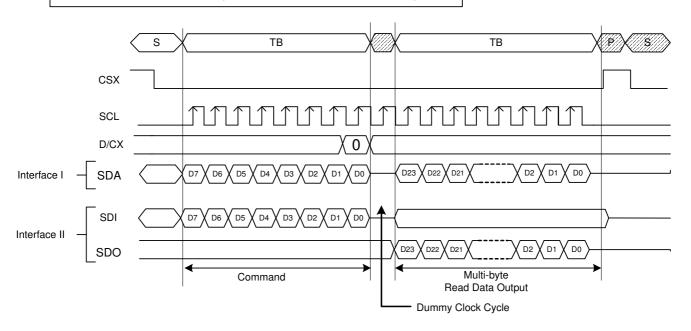


4-wire Serial Interface Protocol

4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)

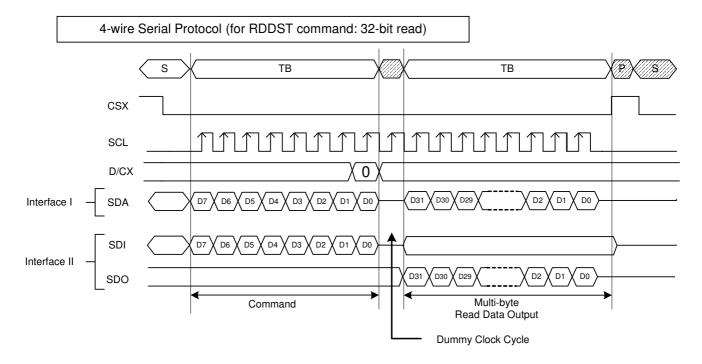


4-wire Serial Protocol (for RDDID command: 24-bit read)





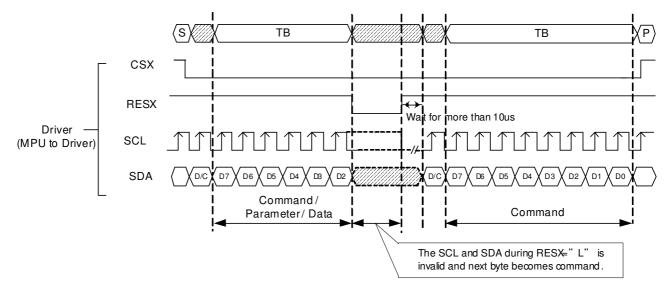
ILI9341



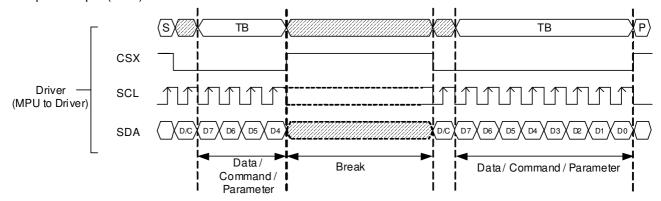


7.1.11. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

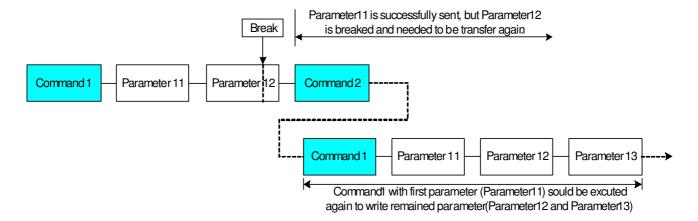


If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

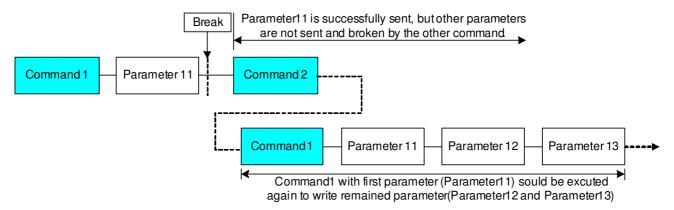


If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.





If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.





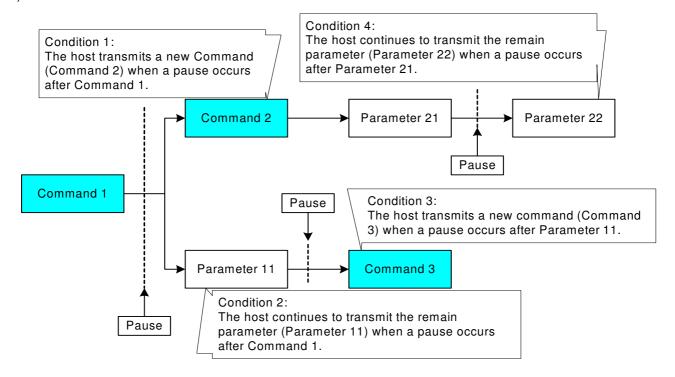


7.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9341 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

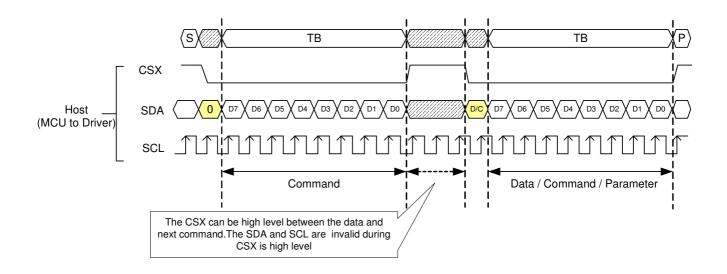
This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

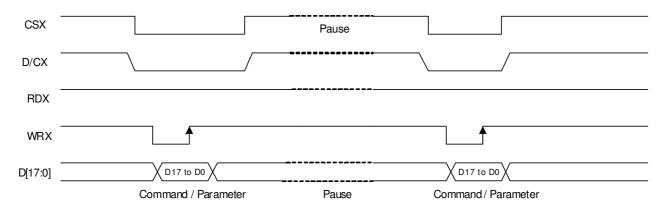




7.1.13. Serial Interface Pause (3_wire)



7.1.14. Parallel Interface Pause





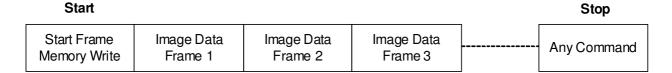


7.1.15. Data Transfer Mode

ILI9341 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.

Start						Stop	
Start Frame Memory Write	Image Data Frame 1	Any Command	Start Frame Memory Write	Image Data Frame 2	Any Command	 Any Command	

Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.





7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9341 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to "10", the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to "11", the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9341 supports several pixel formats that can be selected by DPI [2:0] bits of "Pixel Format Set (3Ah)" and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM	I[1:0]	RIM	DPI[2:0]		:0]	RGB Interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, DE, DOTCLK,D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)	DE Mode	VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1]
1	0	1	1	1	0	6-bit RGB interface (262K colors)	Valid data is determined by the DE signal	VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	0	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DE, DOTCLK, D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)		VSYNC, HSYNC, DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)	SYNC Mode In SYNC mode, DE signal is ignored;	VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1]
1	1	1	1	1	0	6-bit RGB interface (262K colors)	blanking porch is determined by B5h command.	VSYNC, HSYNC, DOTCLK, D[5:0]
1	1	1	1	0	1	6-bit RGB interface (65K colors)		VSYNC, HSYNC, DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , DPI[2:0] = 110, and RIM=0

D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

[18bpp Frame Memory Write R5] R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] R[5] B[4] R[3] R[2] R[1] R[0]

16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

[16bpp Frame Memory Write R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] R[4] R[3] R[2] R[1] R[0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 110, and RIM=1

D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0

[18bpp Frame Memory Write R[5] R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] R[5] R[4] R[3] R[2] R[1] R[0]

D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0

[18bpp Frame Memory Write R[5] R[4] R[3] R[2] R[1] R[0] G[5] G[4] G[3] G[2] G[1] G[0] R[5] R[4] R[3] R[2] R[1] R[0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

16bpp Frame Memory Write

6-bit data bus interface (D[5:0] is used), DPI[2:0] = 101, and RIM=1

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when

D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1 D0 D5 D4 D3 D2 D1

G[5] | G[4] | G[3] | G[2] | G[1] | G[0] | B[4] | B[3] | B[2] | B[1] | B[0]

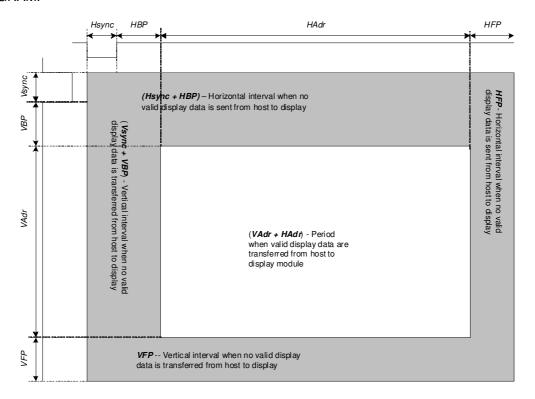




there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Тур.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		ı	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame





frequency about 70Hz.

Notes:

- 1. Vertical period (one frame) shall be equal to the sum of Vsync + VBP + VAdr + VFP.
- 2. Horizontal period (one line) shall be equal to the sum of Hsync + HBP + HAdr + HFP.
- 3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

(Number of PCLK per 1 line) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV

Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction (Number of PCLK in 1H) ≥ (Number of RTN clock) x Division ratio (DIV) x PCDIV.

Setting Example: To set frame frequency to 70Hz:

Internal Clock

```
Internal Oscillation Clock: 615KHz
DIV[1:0] = 2'b0 (x 1/1)
RTN[4:0] = 5'h1b (27 clocks)
FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h27 (320 lines)
Frame Rate \rightarrow 70.30Hz
```

DOTCLK

```
HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz x (2 + 320 + 2) lines x (10 + 20 + 240 + 10) clocks = 6.35MHz

DOTCLK frequency = 6.35MHz

6.35 MHz / 615KHz = 10.32 \Box Set PCDIV so that PCLK is divided by 10.

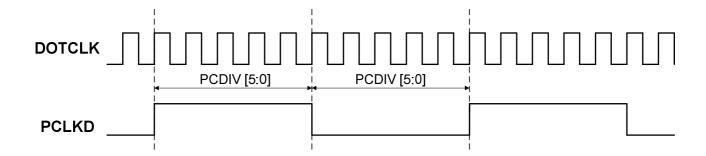
external fosc = 6.35 MHz / 10 = 635KHz

PCDIV = [6.35MHz / 10 = 635KHz

PCDIV = [6.35MHz / 10 = 635KHz

PCDIV = [6.35MHz / 10 = 635KHz
```



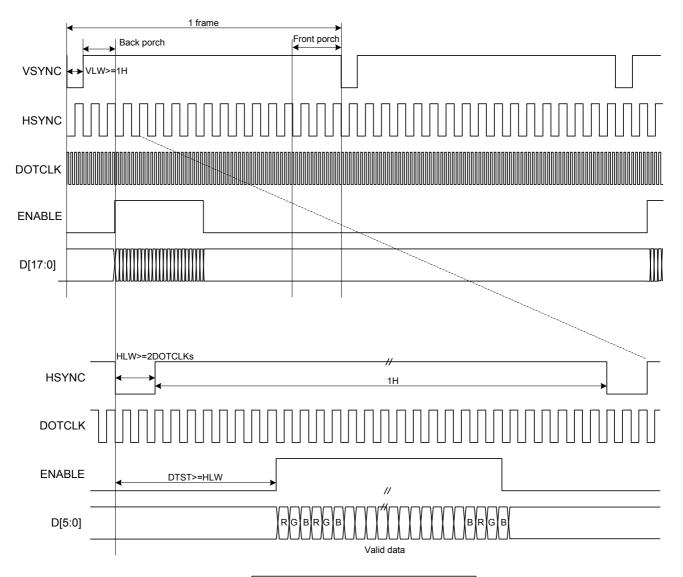






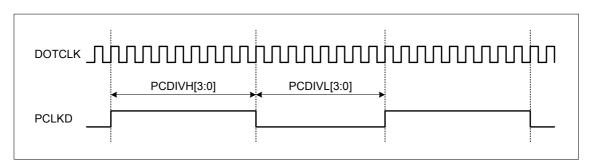
7.2.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.



VLW: VSYNC Low Width HLW: HSYNC Low Width

DTST: Data Transfer Startup Time



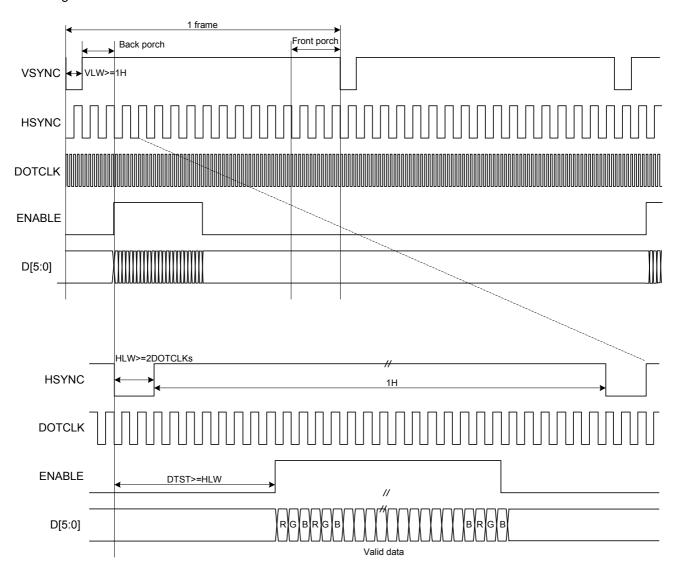
Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.



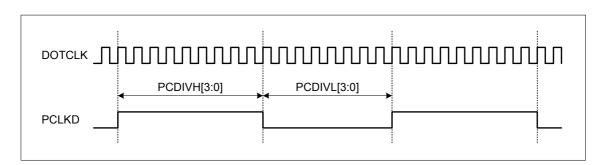


The timing chart of 6-bit RGB interface mode is shown as below:



VLW: VSYNC Low Width HLW: HSYNC Low Width

DTST: Data Transfer Startup Time



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.



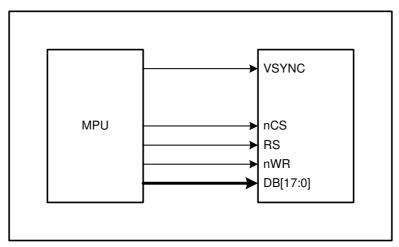


Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

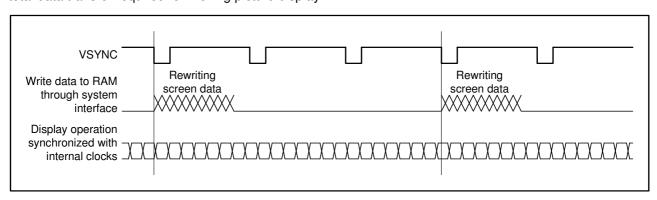


7.3. VSYNC Interface

ILI9341 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080- I /8080- I system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".

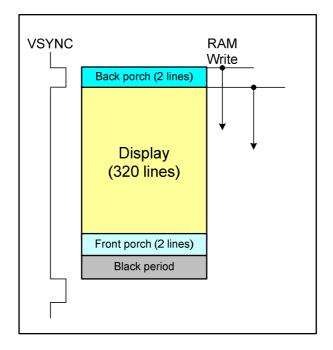


In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.









The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\textit{Minimum RAM write speed [Hz]} > \frac{240 \times \textit{DisplayLines(NL)}}{[\textit{BackPorch(VBP)} + \textit{DisplayLines(NL)} - \textit{margins]} \times \textit{Clocks per line} \times (1/\textit{fosc})}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 320 lines Lines: 320 lines (NL = 100111)

Back porch: 2 lines (VBP = 0000010) Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz
Frequency fluctuation: 10%

Internal oscillator clock (fosc.) [Hz] = $70 \times [320+2+2] \times 27$ clocks $\times (1.1/0.9) = 748$ KHz





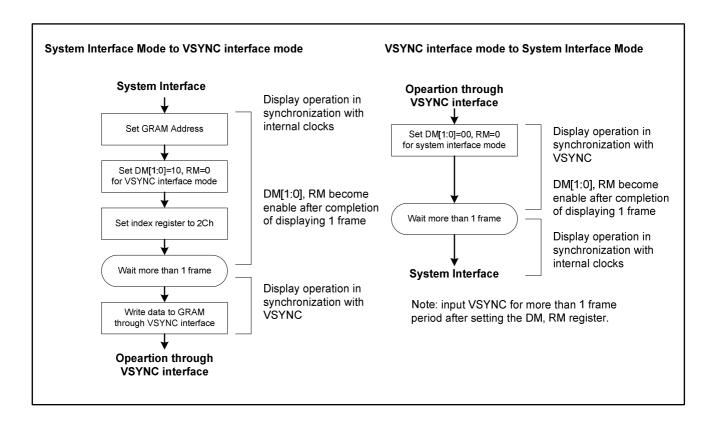
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz] > $240 \times 320 \times 748 \text{K} / [(2 + 320 - 2) \text{lines } \times 27 \text{clocks}] = 6.65 \text{ MHz}$

The above theoretical value is calculated based on the premise that the ILI9341 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9341 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

- 1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
- 2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
- 3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
- 4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.







7.4. Color Depth Conversion Look Up Table

When ILI9341 operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel -mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R ₀₀₅ R ₀₀₄ R ₀₀₃ R ₀₀₂ R ₀₀₁ R ₀₀₀	1
00001	R ₀₁₅ R ₀₁₄ R ₀₁₃ R ₀₁₂ R ₀₁₁ R ₀₁₀	2
00010	R ₀₂₅ R ₀₂₄ R ₀₂₃ R ₀₂₂ R ₀₂₁ R ₀₂₀	3
00011	R ₀₃₅ R ₀₃₄ R ₀₃₃ R ₀₃₂ R ₀₃₁ R ₀₃₀	4
00100	R ₀₄₅ R ₀₄₄ R ₀₄₃ R ₀₄₂ R ₀₄₁ R ₀₄₀	5
00101	R ₀₅₅ R ₀₅₄ R ₀₅₃ R ₀₅₂ R ₀₅₁ R ₀₅₀	6
00110	R ₀₆₅ R ₀₆₄ R ₀₆₃ R ₀₆₂ R ₀₆₁ R ₀₆₀	7
00111	R ₀₇₅ R ₀₇₄ R ₀₇₃ R ₀₇₂ R ₀₇₁ R ₀₇₀	8
01000	R ₀₈₅ R ₀₈₄ R ₀₈₃ R ₀₈₂ R ₀₈₁ R ₀₈₀	9
01001	R ₀₉₅ R ₀₉₄ R ₀₉₃ R ₀₉₂ R ₀₉₁ R ₀₉₀	10
01010	R ₁₀₅ R ₁₀₄ R ₁₀₃ R ₁₀₂ R ₁₀₁ R ₁₀₀	11
01011	R ₁₁₅ R ₁₁₄ R ₁₁₃ R ₁₁₂ R ₁₁₁ R ₁₁₀	12
01100	R ₁₂₅ R ₁₂₄ R ₁₂₃ R ₁₂₂ R ₁₂₁ R ₁₂₀	13
01101	R ₁₃₅ R ₁₃₄ R ₁₃₃ R ₁₃₂ R ₁₃₁ R ₁₃₀	14
01110	R ₁₄₅ R ₁₄₄ R ₁₄₃ R ₁₄₂ R ₁₄₁ R ₁₄₀	15
01111	R ₁₅₅ R ₁₅₄ R ₁₅₃ R ₁₅₂ R ₁₅₁ R ₁₅₀	16
10000	$R_{165}R_{164}R_{163}R_{162}R_{161}R_{160}$	17
10001	R ₁₇₅ R ₁₇₄ R ₁₇₃ R ₁₇₂ R ₁₇₁ R ₁₇₀	18
10010	R ₁₈₅ R ₁₈₄ R ₁₈₃ R ₁₈₂ R ₁₈₁ R ₁₈₀	19
10011	$R_{195} R_{194} R_{193} R_{192} R_{191} R_{190}$	20
10100	$R_{205} R_{204} R_{203} R_{202} R_{201} R_{200}$	21
10101	$R_{215}R_{214}R_{213}R_{212}R_{211}R_{210}$	22
10110	$R_{225} \: R_{224} \: R_{223} \: R_{222} \: R_{221} \: R_{220}$	23
10111	R ₂₃₅ R ₂₃₄ R ₂₃₃ R ₂₃₂ R ₂₃₁ R ₂₃₀	24
11000	R ₂₄₅ R ₂₄₄ R ₂₄₃ R ₂₄₂ R ₂₄₁ R ₂₄₀	25
11001	R ₂₅₅ R ₂₅₄ R ₂₅₃ R ₂₅₂ R ₂₅₁ R ₂₅₀	26
11010	R ₂₆₅ R ₂₆₄ R ₂₆₃ R ₂₆₂ R ₂₆₁ R ₂₆₀	27
11011	R ₂₇₅ R ₂₇₄ R ₂₇₃ R ₂₇₂ R ₂₇₁ R ₂₇₀	28
11100	R ₂₈₅ R ₂₈₄ R ₂₈₃ R ₂₈₂ R ₂₈₁ R ₂₈₀	29
11101	R ₂₉₅ R ₂₉₄ R ₂₉₃ R ₂₉₂ R ₂₉₁ R ₂₉₀	30
11110	R ₃₀₅ R ₃₀₄ R ₃₀₃ R ₃₀₂ R ₃₀₁ R ₃₀₀	31
11111	$R_{315}R_{314}R_{313}R_{312}R_{311}R_{310}$	32



G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G ₀₀₅ G ₀₀₄ G ₀₀₃ G ₀₀₂ G ₀₀₁ G ₀₀₀	33
000001	G ₀₁₅ G ₀₁₄ G ₀₁₃ G ₀₁₂ G ₀₁₁ G ₀₁₀	34
000010	$G_{025} \ G_{024} \ G_{023} \ G_{022} \ G_{021} \ G_{020}$	35
000011	$G_{035} \ G_{034} \ G_{033} \ G_{032} \ G_{031} \ G_{030}$	36
000100	G ₀₄₅ G ₀₄₄ G ₀₄₃ G ₀₄₂ G ₀₄₁ G ₀₄₀	37
000101	G ₀₅₅ G ₀₅₄ G ₀₅₃ G ₀₅₂ G ₀₅₁ G ₀₅₀	38
000110	G ₀₆₅ G ₀₆₄ G ₀₆₃ G ₀₆₂ G ₀₆₁ G ₀₆₀	39
000111	G ₀₇₅ G ₀₇₄ G ₀₇₃ G ₀₇₂ G ₀₇₁ G ₀₇₀	40
001000	G ₀₈₅ G ₀₈₄ G ₀₈₃ G ₀₈₂ G ₀₈₁ G ₀₈₀	41
001001	G ₀₉₅ G ₀₉₄ G ₀₉₃ G ₀₉₂ G ₀₉₁ G ₀₉₀	42
001010	G ₁₀₅ G ₁₀₄ G ₁₀₃ G ₁₀₂ G ₁₀₁ G ₁₀₀	43
001011	$G_{115}G_{114}G_{113}G_{112}G_{111}G_{110}$	44
001100	$G_{125}G_{124}G_{123}G_{122}G_{121}G_{120}$	45
001101	$G_{135}G_{134}G_{133}G_{132}G_{131}G_{130}$	46
001110	$G_{145}G_{144}G_{143}G_{142}G_{141}G_{140}$	47
001111	$G_{155}G_{154}G_{153}G_{152}G_{151}G_{150}$	48
010000	$G_{165}G_{164}G_{163}G_{162}G_{161}G_{160}$	49
010001	$G_{175}G_{174}G_{173}G_{172}G_{171}G_{170}$	50
010010	$G_{185}G_{184}G_{183}G_{182}G_{181}G_{180}$	51
010011	$G_{195}G_{194}G_{193}G_{192}G_{191}G_{190}$	52
010100	$G_{205}\:G_{204}\:G_{203}\:G_{202}\:G_{201}\:G_{200}$	53
010101	$G_{215}G_{214}G_{213}G_{212}G_{211}G_{210}$	54
010110	$G_{225}G_{224}G_{223}G_{222}G_{221}G_{220}$	55
010111	$G_{235}\:G_{234}\:G_{233}\:G_{232}\:G_{231}\:G_{230}$	56
011000	$G_{245}G_{244}G_{243}G_{242}G_{241}G_{240}$	57
011001	$G_{255} \; G_{254} \; G_{253} \; G_{252} \; G_{251} \; G_{250}$	58
011010	$G_{265}G_{264}G_{263}G_{262}G_{261}G_{260}$	59
011011	$G_{275}G_{274}G_{273}G_{272}G_{271}G_{270}$	60
011100	$G_{285}G_{284}G_{283}G_{282}G_{281}G_{280}$	61
011101	$G_{295}G_{294}G_{293}G_{292}G_{291}G_{290}$	62
011110	$G_{305}\:G_{304}\:G_{303}\:G_{302}\:G_{301}\:G_{300}$	63
011111	$G_{315}G_{314}G_{313}G_{312}G_{311}G_{310}$	64
100000	$G_{325}G_{324}G_{323}G_{322}G_{321}G_{320}$	65
100001	$G_{335}G_{334}G_{333}G_{332}G_{331}G_{330}$	66



G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G ₃₄₅ G ₃₄₄ G ₃₄₃ G ₃₄₂ G ₃₄₁ G ₃₄₀	67
100011	G ₃₅₅ G ₃₅₄ G ₃₅₃ G ₃₅₂ G ₃₅₁ G ₃₅₀	68
100100	G ₃₆₅ G ₃₆₄ G ₃₆₃ G ₃₆₂ G ₃₆₁ G ₃₆₀	69
100101	G ₃₇₅ G ₃₇₄ G ₃₇₃ G ₃₇₂ G ₃₇₁ G ₃₇₀	70
100110	G ₃₈₅ G ₃₈₄ G ₃₈₃ G ₃₈₂ G ₃₈₁ G ₃₈₀	71
100111	G ₃₉₅ G ₃₉₄ G ₃₉₃ G ₃₉₂ G ₃₉₁ G ₃₉₀	72
101000	G ₄₀₅ G ₄₀₄ G ₄₀₃ G ₄₀₂ G ₄₀₁ G ₄₀₀	73
101001	G ₄₁₅ G ₄₁₄ G ₄₁₃ G ₄₁₂ G ₄₁₁ G ₄₁₀	74
101010	G ₄₂₅ G ₄₂₄ G ₄₂₃ G ₄₂₂ G ₄₂₁ G ₄₂₀	75
101011	G ₄₃₅ G ₄₃₄ G ₄₃₃ G ₄₃₂ G ₄₃₁ G ₄₃₀	76
101100	G ₄₄₅ G ₄₄₄ G ₄₄₃ G ₄₄₂ G ₄₄₁ G ₄₄₀	77
101101	G ₄₅₅ G ₄₅₄ G ₄₅₃ G ₄₅₂ G ₄₅₁ G ₄₅₀	78
101110	G ₄₆₅ G ₄₆₄ G ₄₆₃ G ₄₆₂ G ₄₆₁ G ₄₆₀	79
101111	G ₄₇₅ G ₄₇₄ G ₄₇₃ G ₄₇₂ G ₄₇₁ G ₄₇₀	80
110000	G ₄₈₅ G ₄₈₄ G ₄₈₃ G ₄₈₂ G ₄₈₁ G ₄₈₀	81
110001	G ₄₉₅ G ₄₉₄ G ₄₉₃ G ₄₉₂ G ₄₉₁ G ₄₉₀	82
110010	G ₅₀₅ G ₅₀₄ G ₅₀₃ G ₅₀₂ G ₅₀₁ G ₅₀₀	83
110011	G ₅₁₅ G ₅₁₄ G ₅₁₃ G ₅₁₂ G ₅₁₁ G ₅₁₀	84
110100	G ₅₂₅ G ₅₂₄ G ₅₂₃ G ₅₂₂ G ₅₂₁ G ₅₂₀	85
110101	G ₅₃₅ G ₅₃₄ G ₅₃₃ G ₅₃₂ G ₅₃₁ G ₅₃₀	86
110110	G ₅₄₅ G ₅₄₄ G ₅₄₃ G ₅₄₂ G ₅₄₁ G ₅₄₀	87
110111	G ₅₅₅ G ₅₅₄ G ₅₅₃ G ₅₅₂ G ₅₅₁ G ₅₅₀	88
111000	G ₅₆₅ G ₅₆₄ G ₅₆₃ G ₅₆₂ G ₅₆₁ G ₅₆₀	89
111001	G ₅₇₅ G ₅₇₄ G ₅₇₃ G ₅₇₂ G ₅₇₁ G ₅₇₀	90
111010	G ₅₈₅ G ₅₈₄ G ₅₈₃ G ₅₈₂ G ₅₈₁ G ₅₈₀	91
111011	$G_{595} G_{594} G_{593} G_{592} G_{591} G_{590}$	92
111100	G ₆₀₅ G ₆₀₄ G ₆₀₃ G ₆₀₂ G ₆₀₁ G ₆₀₀	93
111101	G ₆₁₅ G ₆₁₄ G ₆₁₃ G ₆₁₂ G ₆₁₁ G ₆₁₀	94
111110	G ₆₂₅ G ₆₂₄ G ₆₂₃ G ₆₂₂ G ₆₂₁ G ₆₂₀	95
111111	G ₆₃₅ G ₆₃₄ G ₆₃₃ G ₆₃₂ G ₆₃₁ G ₆₃₀	96



B input (5-bit) 16-bit/pixel -mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B ₀₀₅ B ₀₀₄ B ₀₀₃ B ₀₀₂ B ₀₀₁ B ₀₀₀	97
00001	B ₀₁₅ B ₀₁₄ B ₀₁₃ B ₀₁₂ B ₀₁₁ B ₀₁₀	98
00010	B ₀₂₅ B ₀₂₄ B ₀₂₃ B ₀₂₂ B ₀₂₁ B ₀₂₀	99
00011	B ₀₃₅ B ₀₃₄ B ₀₃₃ B ₀₃₂ B ₀₃₁ B ₀₃₀	100
00100	B ₀₄₅ B ₀₄₄ B ₀₄₃ B ₀₄₂ B ₀₄₁ B ₀₄₀	101
00101	B ₀₅₅ B ₀₅₄ B ₀₅₃ B ₀₅₂ B ₀₅₁ B ₀₅₀	102
00110	B ₀₆₅ B ₀₆₄ B ₀₆₃ B ₀₆₂ B ₀₆₁ B ₀₆₀	103
00111	B ₀₇₅ B ₀₇₄ B ₀₇₃ B ₀₇₂ B ₀₇₁ B ₀₇₀	104
01000	B ₀₈₅ B ₀₈₄ B ₀₈₃ B ₀₈₂ B ₀₈₁ B ₀₈₀	105
01001	B ₀₉₅ B ₀₉₄ B ₀₉₃ B ₀₉₂ B ₀₉₁ B ₀₉₀	106
01010	B ₁₀₅ B ₁₀₄ B ₁₀₃ B ₁₀₂ B ₁₀₁ B ₁₀₀	107
01011	B ₁₁₅ B ₁₁₄ B ₁₁₃ B ₁₁₂ B ₁₁₁ B ₁₁₀	108
01100	B ₁₂₅ B ₁₂₄ B ₁₂₃ B ₁₂₂ B ₁₂₁ B ₁₂₀	109
01101	B ₁₃₅ B ₁₃₄ B ₁₃₃ B ₁₃₂ B ₁₃₁ B ₁₃₀	110
01110	B ₁₄₅ B ₁₄₄ B ₁₄₃ B ₁₄₂ B ₁₄₁ B ₁₄₀	111
01111	B ₁₅₅ B ₁₅₄ B ₁₅₃ B ₁₅₂ B ₁₅₁ B ₁₅₀	112
10000	B ₁₆₅ B ₁₆₄ B ₁₆₃ B ₁₆₂ B ₁₆₁ B ₁₆₀	113
10001	B ₁₇₅ B ₁₇₄ B ₁₇₃ B ₁₇₂ B ₁₇₁ B ₁₇₀	114
10010	B ₁₈₅ B ₁₈₄ B ₁₈₃ B ₁₈₂ B ₁₈₁ B ₁₈₀	115
10011	B ₁₉₅ B ₁₉₄ B ₁₉₃ B ₁₉₂ B ₁₉₁ B ₁₉₀	116
10100	B ₂₀₅ B ₂₀₄ B ₂₀₃ B ₂₀₂ B ₂₀₁ B ₂₀₀	117
10101	B ₂₁₅ B ₂₁₄ B ₂₁₃ B ₂₁₂ B ₂₁₁ B ₂₁₀	118
10110	B ₂₂₅ B ₂₂₄ B ₂₂₃ B ₂₂₂ B ₂₂₁ B ₂₂₀	119
10111	B ₂₃₅ B ₂₃₄ B ₂₃₃ B ₂₃₂ B ₂₃₁ B ₂₃₀	120
11000	B ₂₄₅ B ₂₄₄ B ₂₄₃ B ₂₄₂ B ₂₄₁ B ₂₄₀	121
11001	B ₂₅₅ B ₂₅₄ B ₂₅₃ B ₂₅₂ B ₂₅₁ B ₂₅₀	122
11010	B ₂₆₅ B ₂₆₄ B ₂₆₃ B ₂₆₂ B ₂₆₁ B ₂₆₀	123
11011	B ₂₇₅ B ₂₇₄ B ₂₇₃ B ₂₇₂ B ₂₇₁ B ₂₇₀	124
11100	B ₂₈₅ B ₂₈₄ B ₂₈₃ B ₂₈₂ B ₂₈₁ B ₂₈₀	125
11101	B ₂₉₅ B ₂₉₄ B ₂₉₃ B ₂₉₂ B ₂₉₁ B ₂₉₀	126
11110	B ₃₀₅ B ₃₀₄ B ₃₀₃ B ₃₀₂ B ₃₀₁ B ₃₀₀	127
11111	B ₃₁₅ B ₃₁₄ B ₃₁₃ B ₃₁₂ B ₃₁₁ B ₃₁₀	128





7.5. Display Data RAM (DDRAM)

ILI9341 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.



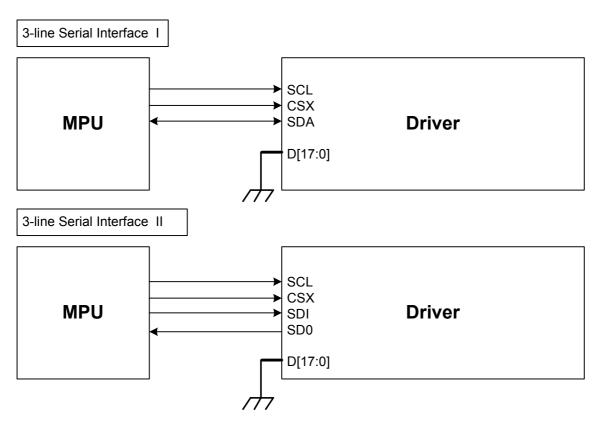


7.6. Display Data Format

ILI9341 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080- I /8080- II series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.6.1. 3-line Serial Interface

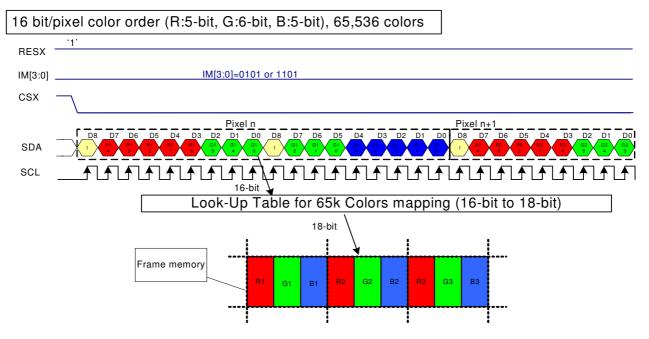
The 3-line/9-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0101" for serial interface I or IM [3:0] to "1101" for serial interface II. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

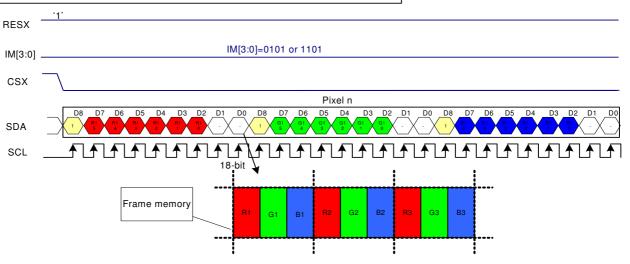
- -65k colors, RGB 5, 6, 5 -bits input
- -262k colors, RGB 6, 6, 6 -bits input.





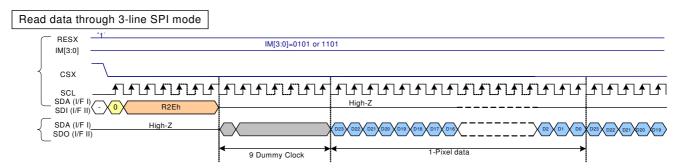
- Note 1: The pixel data with 16-bit color depth information.
- Note 2: The most significant bits are: Rx4, Gx5 and Bx4.
- Note 3: The least significant bits are: Rx0, Gx0 and Bx0.
- Note 4: '-'= Don't care -Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



- Note 1: The pixel data with 18-bit color depth information.
- Note 2: The most significant bits are: Rx5, Gx5 and Bx5.
- Note 3: The least significant bits are : Rx0, Gx0 and Bx0.
- Note 4: '-'= Don't care Can be set "0" or "1".





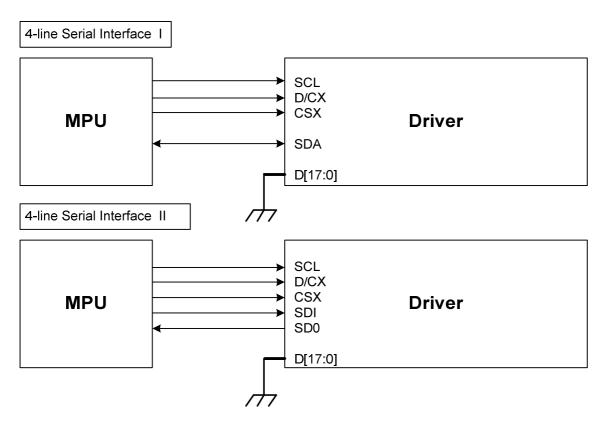
Note 1: '-'= Don't care -Can be set "0" or "1".





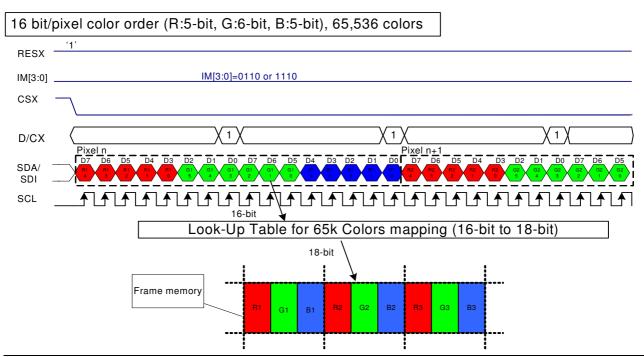
7.6.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0110" for serial interface I or IM [3:0] to "1110" for serial interface II. The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

- -65k colors, RGB 5, 6, 5 -bits input.
- -262k colors, RGB 6, 6, 6 -bits input.



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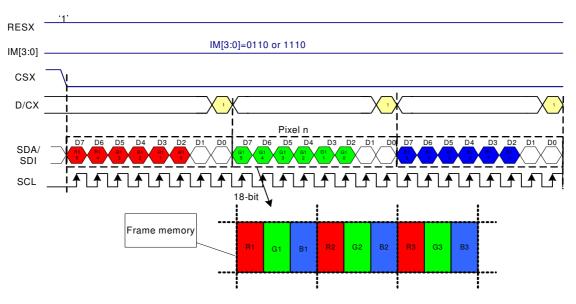
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care -Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



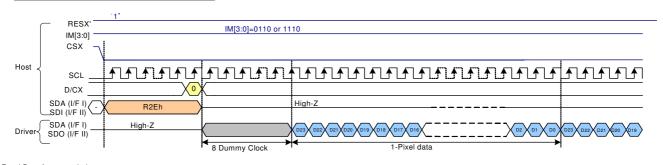
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care -Can be set "0" or "1".

Read data through 4-line SPI mode





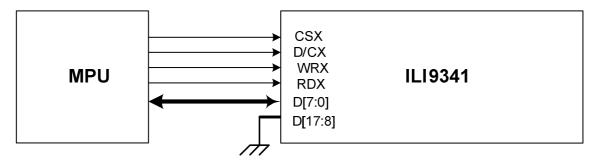
Note 1: '-'= Don't care - Can be set "0" or "1".





7.6.3. 8-bit Parallel MCU Interface

The 8080- I system 8-bit parallel bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0000". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	 238R0		239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	 238G5		239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	 238G3		239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

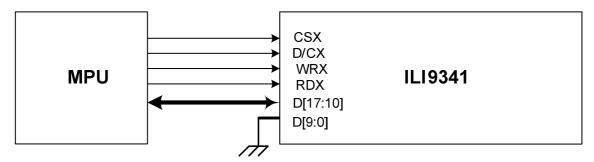
One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D7	C7	0R5	0G5	0B5	 239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	 239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	 239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	 239R0	239G0	239B0
D1	C1						
D0	C0						





The 8080- Π system 8-bit parallel bus interface of ILI9341 can be used by settings as IM [3:0] ="1001". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D13	C3	0R0		1R0	1B3	 238R0		239R0	239B3
D12	C2	0G5		1G5	1B2	 238G5		239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

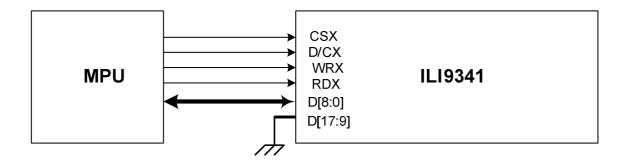
Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D17	C7	0R5	0G5	0B5	 239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	 239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	 239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	 239R0	239G0	239B0
D11	C1						
D10	C0						





7.6.4. 9-bit Parallel MCU Interface

The 8080- I system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "0010". The following shown figure is the example of interface with 8080- I MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D8									
D7	C7	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0		1R0	1B3	 238R0		239R0	
D2	C2	0G5		1G5	1B2	 238G5		239G5	
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3		1G3	1B0	 238G3		239G3	

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	4	 478	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D8		0R5	0G2	1R5	1G2	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	 238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	 238R3	238G0	239R3	239G0
D5	C5	0R2		1R2	1B5	 238R2		239R2	
D4	C4	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D3	C3	0R0		1R0	1B3	 238R0		239R0	
D2	C2	0G5		1G5	1B2	 238G5		239G5	
D1	C1	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0

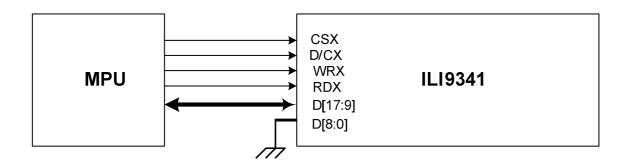




MDT[1:0]="01"

Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D8							
D7	C7	0R5	0G5	0B5	 239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	 239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	 239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	 239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	 239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	 239R0	239G0	239B0
D1	C1						
D0	C0						

The 8080- Π system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "1011". The following shown figure is the example of interface with 8080- Π MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	 477	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7								
D16	C6	0R4	0G2	1R4	1G2	 238R4	238G2	239R4	239G2
D15	C5	0R3	0G1	1R3	1G1	 238R3	238G1	239R3	239G1
D14	C4	0R2	0G0	1R2	1G0	 238R2	238G0	239R2	239G0
D13	C3	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D12	C2	0R0		1R0	1B3	 238R0		239R0	
D11	C1	0G5		1G5	1B2	 238G5		239G5	
D10	C0	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	4	 478	478	479	480
D/CX	0	1	1	1	1	 1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	 238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	 238R3	238G0	239R3	239G0
D14	C4	0R2		1R2	1B5	 238R2		239R2	
D13	C3	0R1	0B4	1R1	1B4	 238R1	238B4	239R1	239B4
D12	C2	0R0		1R0	1B3	 238R0		239R0	
D11	C1	0G5		1G5	1B2	 238G5		239G5	
D10	C0	0G4	0B1	1G4	1B1	 238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	 238G3	238B0	239G3	239B0

MDT[1:0]="01"

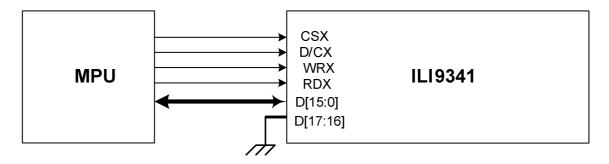
Count	0	1	2	3	 718	719	720
D/CX	0	1	1	1	 1	1	1
D17	C7						
D16	C6	0R5	0G5		 239R5	239G5	239B5
D15	C5	0R4	0G4	0B4	 239R4	239G4	239B4
D14	C4	0R3	0G3		 239R3	239G3	239B3
D13	C3	0R2	0G2		 239R2	239G2	239B2
D12	C2	0R1	0G1	0B1	 239R1	239G1	239B1
D11	C1	0R0	0G0		 239R0	239G0	239B0
D10	C0						
D9							





7.6.5. 16-bit Parallel MCU Interface

The 8080- I system 16-bit parallel bus interface of ILl9341 can be selected by setting hardware pin IM[3:0] to "0001". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

	•	, ,		•		0	
Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8		0G3	1G3	2G3	 237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3	0B3	1B3				239B3
D2	C2	0B2	1B2				239B2
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0	0B0	1B0				239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	 358	359	360
D/CX	0	1	1	1	 1	1	1
D15		0R5		1G5	 238R5		239G5
D14		0R4	0B4	1G4	 238R4	238B4	239G4
D13		0R3		1G3	 238R3		239G3
D12		0R2		1G2	 238R2		239G2
D11		0R1	0B1	1G1	 238R1	238B1	239G1
D10		0R0		1G0	 238R0		239G0
D9							
D8							
D7	C7	0G5	1R5	1B5	 238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	 238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	 238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	 238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	 238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	 238G0	239R0	239B0
D1	C1						
D0	C0						

MDT[1:0]="01"

[] -	-								
Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15		0R5		1R5	1B5	 238R5		239R5	239B5
D14		0R4	0B4	1R4	1B4	 238R4	238B4	239R4	239B4
D13		0R3		1R3	1B3	 238R3		239R3	239B3
D12		0R2		1R2	1B2	 238R2		239R2	239B2
D11		0R1	0B1	1R1	1B1	 238R1	238B1	239R1	239B1
D10		0R0		1R0	1B0	 238R0		239R0	239B0
D9									
D8									
D7	C7	0G5		1G5		 238G5		239G5	
D6	C6	0G4		1G4		 238G4		239G4	
D5	C5	0G3		1G3		 238G3		239G3	
D4	C4	0G2		1G2		 238G2		239G2	
D3	C3	0G1		1G1		 238G1		239G1	
D2	C2	0G0		1G0		 238G0		239G0	
D1	C1		·						
D0	C0								





MDT[1:0]="10"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15		0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D14		0R4		1R4	1B0	 238R4		239R4	239B0
D13		0R3		1R3		 238R3		239R3	
D12		0R2		1R2		 238R2		239R2	
D11		0R1		1R1		 238R1		239R1	
D10		0R0		1R0		 238R0		239R0	
D9		0G5		1G5		 238G5		239G5	
D8		0G4		1G4		 238G4		239G4	
D7	C7	0G3		1G3		 238G3		239G3	
D6	C6	0G2		1G2		 238G2		239G2	
D5	C5	0G1		1G1		 238G1		239G1	
D4	C4	0G0		1G0		 238G0		239G0	
D3	C3			1B5					
D2	C2	0B4		1B4		 238B4		239B4	
D1	C1			1B3					
D0	C0			1B2					

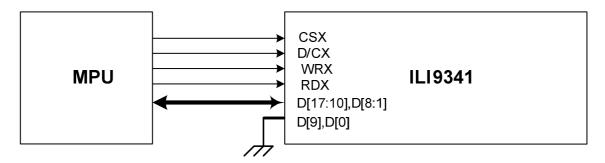
MDT[1:0]="11"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D15			0R3		1R3		238R3		239R3
D14			0R2		1R2		238R2		239R2
D13			0R1		1R1		238R1		239R1
D12			0R0		1R0		238R0		239R0
D11			0G5		1G5		238G5		239G5
D10			0G4		1G4		238G4		239G4
D9			0G3		1G3		238G3		239G3
D8			0G2		1G2		238G2		239G2
D7	C7		0G1		1G1		238G1		239G1
D6	C6		0G0		1G0		238G0		239G0
D5	C5				1B5				
D4	C4		0B4		1B4		238B4		239B4
D3	C3				1B3				
D2	C2				1B2				
D1	C1	0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	 238R4	238B0	239R4	239B0





The 8080- Π system 16-bit parallel bus interface of ILI9341 can be selected by settings IM [3:0] ="1000". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R4	1R4	2R4	 237R4	238R4	239R4
D16		0R3	1R3	2R3	 237R3	238R3	239R3
D15		0R2	1R2	2R2	 237R2	238R2	239R2
D14		0R1	1R1	2R1	 237R1	238R1	239R1
D13		0R0	1R0	2R0	 237R0	238R0	239R0
D12		0G5	1G5	2G5	 237G5	238G5	239G5
D11		0G4	1G4	2G4	 237G4	238G4	239G4
D10		0G3	1G3	2G3	 237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	237B4	238B4	239B4
D4	C3		1B3				239B3
D3	C2		1B2				239B2
D2	C1	0B1	1B1	2B1	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]="00"

Count	0	1	2	3	 358	359	360
D/CX	0	1	1	1	 1	1	1
D17		0R5		1G5	 238R5		239G5
D16		0R4	0B4	1G4	 238R4	238B4	239G4
D15		0R3		1G3	 238R3		239G3
D14		0R2		1G2	 238R2		239G2
D13		0R1	0B1	1G1	 238R1	238B1	239G1
D12		0R0		1G0	 238R0		239G0
D11							
D10							
D8	C7	0G5	1R5	1B5	 238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	 238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	 238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	 238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	 238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	 238G0	239R0	239B0
D2	C1						
D1	C0						

MDT[1:0]="01"

[] -	-								
Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17		0R5		1R5	1B5	 238R5		239R5	239B5
D16		0R4	0B4	1R4	1B4	 238R4	238B4	239R4	239B4
D15		0R3		1R3	1B3	 238R3		239R3	239B3
D14		0R2		1R2	1B2	 238R2		239R2	239B2
D13		0R1	0B1	1R1	1B1	 238R1	238B1	239R1	239B1
D12		0R0		1R0	1B0	 238R0		239R0	239B0
D11									
D10									
D8	C7	0G5		1G5		 238G5		239G5	
D7	C6	0G4		1G4		 238G4		239G4	
D6	C5	0G3		1G3		 238G3		239G3	
D5	C4	0G2		1G2		 238G2		239G2	
D4	C3	0G1		1G1		 238G1		239G1	
D3	C2	0G0		1G0		 238G0		239G0	
D2	C1		·						
D1	C0								





MDT[1:0]="10"

Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17		0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D16		0R4		1R4	1B0	 238R4		239R4	239B0
D15		0R3		1R3		 238R3		239R3	
D14		0R2		1R2		 238R2		239R2	
D13		0R1		1R1		 238R1		239R1	
D12		0R0		1R0		 238R0		239R0	
D11		0G5		1G5		 238G5		239G5	
D10		0G4		1G4		 238G4		239G4	
D8	C7	0G3		1G3		 238G3		239G3	
D7	C6	0G2		1G2		 238G2		239G2	
D6	C5	0G1		1G1		 238G1		239G1	
D5	C4	0G0		1G0		 238G0		239G0	
D4	C3			1B5				239B5	
D3	C2	0B4		1B4		 238B4		239B4	
D2	C1			1B3				239B3	
D1	C0	0B2		1B2		 238B2		239B2	

MDT[1:0]="11"

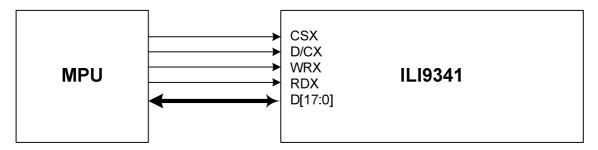
Count	0	1	2	3		 357	358	479	480
D/CX	0	1	1	1			1	1	1
D17			0R3		1R3		238R3		239R3
D16			0R2		1R2		238R2		239R2
D15			0R1		1R1		238R1		239R1
D14			0R0		1R0		238R0		239R0
D13			0G5		1G5		238G5		239G5
D12			0G4		1G4		238G4		239G4
D11			0G3		1G3		238G3		239G3
D10			0G2		1G2		238G2		239G2
D8	C7		0G1		1G1		238G1		239G1
D7	C6		0G0		1G0		238G0		239G0
D6	C5				1B5				239B5
D5	C4		0B4		1B4		238B4		239B4
D4	C3				1B3				239B3
D3	C2				1B2				239B2
D2	C1	0R5	0B1	1R5	1B1	 238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	 238R4	238B0	239R4	239B0





7.6.6. 18-bit Parallel MCU Interface

The 8080- I system 18-bit parallel bus interface of ILl9341 can be selected by setting hardware pin IM[3:0] to "0011". The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17							
D16							
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8		0G3	1G3	2G3	 237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3		1B3				239B3
D2	C2		1B2				239B2
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0		1B0				239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

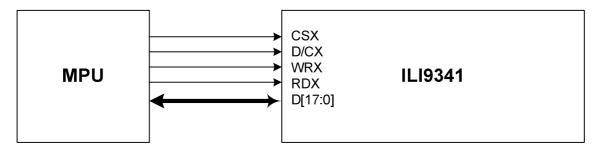
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R5	1R5	2R5	 237R5	238R5	239R5
D16		0R4	1R4	2R4	 237R4	238R4	239R4
D15		0R3	1R3	2R3	 237R3	238R3	239R3
D14		0R2	1R2	2R2	 237R2	238R2	239R2
D13		0R1	1R1	2R1	 237R1	238R1	239R1
D12		0R0	1R0	2R0	 237R0	238R0	239R0
D11		0G5	1G5	2G5	 237G5	238G5	239G5
D10		0G4	1G4	2G4	 237G4	238G4	239G4
D9		0G3	1G3	2G3	 237G3	238G3	239G3
D8		0G2	1G2	2G2	 237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C5		1B5				239B5
D4	C4	0B4	1B4	2B4	237B4	238B4	239B4
D3	C3		1B3				239B3
D2	C2		1B2				239B2
D1	C1	0B1	1B1	2B1	237B1	238B1	239B1
D0	C0		1B0				239B0





The 8080- Π system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="1010". The following shown figure is the example of interface with 8080- Π MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17							
D16							
D15		0R4	1R4	2R4	 237R4	238R4	239R4
D14		0R3	1R3	2R3	 237R3	238R3	239R3
D13		0R2	1R2	2R2	 237R2	238R2	239R2
D12		0R1	1R1	2R1	 237R1	238R1	239R1
D11		0R0	1R0	2R0	 237R0	238R0	239R0
D10		0G5	1G5	2G5	 237G5	238G5	239G5
D9		0G4	1G4	2G4	 237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	 237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	 237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	 237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	 237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	237B4	238B4	239B4
D3	C2		1B3				239B3
D2	C1		1B2				
D1	C0	0B1	1B1	2B1	237B1	238B1	239B1
D0		0B0	1B0	2B0	 237B0	238B0	239B0





262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	 238	239	240
D/CX	0	1	1	1	 1	1	1
D17		0R5	1R5	2R5	 237R5	238R5	239R5
D16		0R4	1R4	2R4	 237R4	238R4	239R4
D15		0R3	1R3	2R3	 237R3	238R3	239R3
D14		0R2	1R2	2R2	 237R2	238R2	239R2
D13		0R1	1R1	2R1	 237R1	238R1	239R1
D12		0R0	1R0	2R0	 237R0	238R0	239R0
D11		0G5	1G5	2G5	 237G5	238G5	239G5
D10		0G4	1G4	2G4	 237G4	238G4	239G4
D9		0G3	1G3	2G3	 237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	 237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	 237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	 237G0	238G0	239G0
D5	C4		1B5				239B5
D4	C3	0B4	1B4	2B4	237B4	238B4	239B4
D3	C2		1B3				239B3
D2	C1		1B2				239B2
D1	C0	0B1	1B1	2B1	237B1	238B1	239B1
D0			1B0				239B0

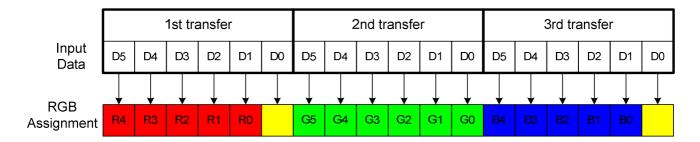




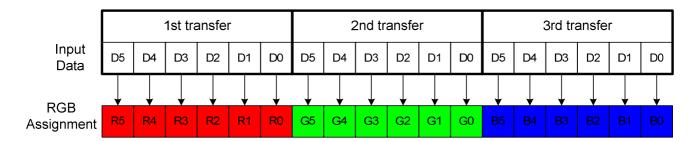
7.6.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to "110". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



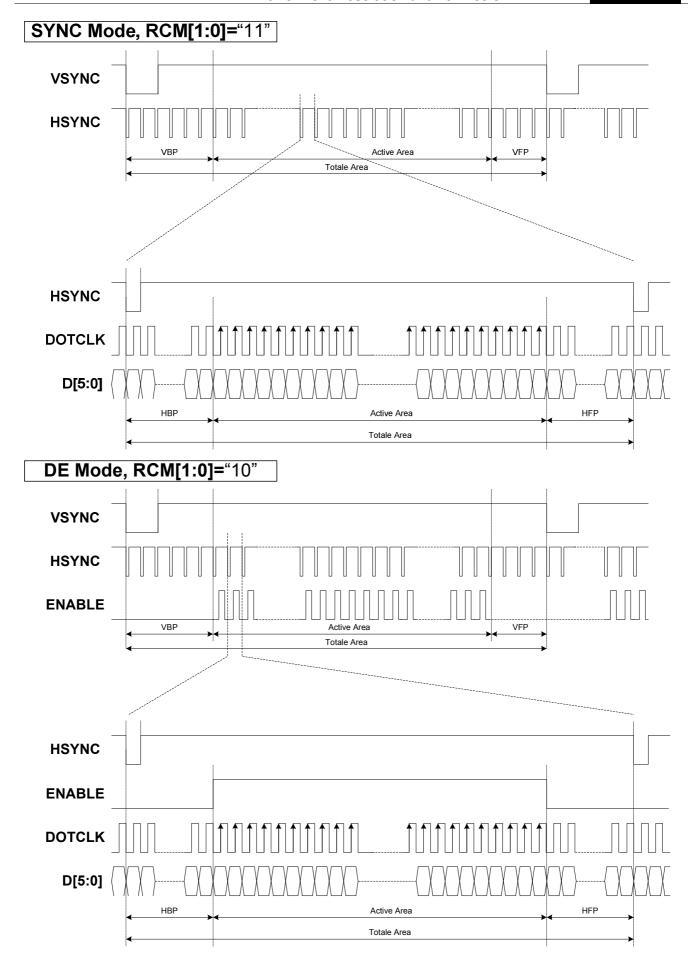
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

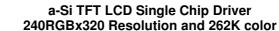


ILI9341 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



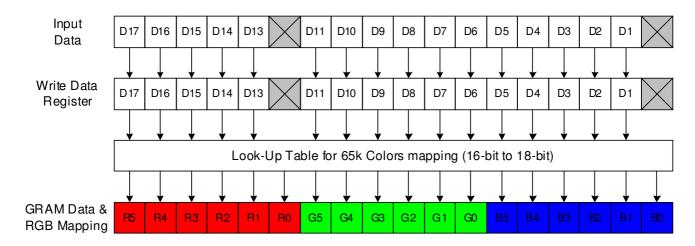






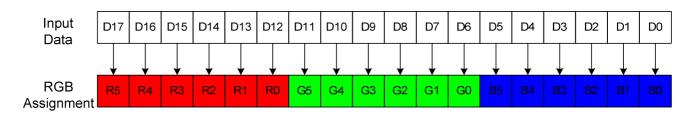
7.6.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to "101". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [17:13] & D [11:1]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [17:13] and D [11:1] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



7.6.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to "110". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.







8. Command

8.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex
No Operation	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
	0	1	1	XX	0	0	0	0	0	1	0	0	04h
	1	1	1	XX	Х	Χ	Х	Х	Х	Х	Х	Χ	XX
Read Display Identification	1	<u>†</u>	1	XX		•	•	ID1 [•			XX
Information	1	1	1	XX				ID2 [XX
	1	1	1	XX				ID3 [XX
	0	1	1	XX	0	0	0	0	1	0	0	1	09h
	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
	1	<u> </u>	1	XX		1		[31:25]				X	00
Read Display Status	1	<u> </u>	1	XX	Х		D [22:20			D [1	9:16]		61
	1	<u> </u>	1	XX	X	Х	X	Х	Х		D [10:8]		00
	1	<u> </u>	1	XX		D [7:5]		X	X	Х	X	Х	00
	0	1	·	XX	0	0	0	0	1	0	1	0	0Ah
Read Display Power Mode	1	<u> </u>	1	XX	X	X	X	X	X	X	Х	X	XX
rioda Biopidy i owoi iliodo	1	<u> </u>	1	XX			D [7				0	0	08
	0	1	<u>'</u>	XX	0	0	0	0	1	0	1	1	0Bh
Read Display MADCTL	1	<u> </u>	1	XX	X	X	X	X	Х	X	X	X	XX
ricad Display WADOTE	1	<u> </u>	1	XX			D [7		Λ.		0	0	00
	0	1	_ i	XX	0	0	0	0	1	1	0	0	0Ch
Read Display Pixel Format	1	<u> </u>	1	XX	X	X	X	X	X	X	X	X	XX
nead Display Fixer Format	1	<u> </u>	1	XX	RIM			•	X		DBI [2:0]		06
							DPI [2:0]						0Dh
Dood Dioploy Imaga Format	0	1		XX	0	0	0	0	1	1	0 X	1	
Read Display Image Format	1	↑ ↑	1	XX	X	X	X	X	X	Х		Х	XX
	1		1	XX		X	X	X	X		D [2:0]	_	00
Dood Disaless Cissed Made	0	1	1	XX	0	0	0	0	1	1	1	0	0Eh
Read Display Signal Mode	1	1	1	XX	Х	Х	X	X	Х	Х	X	X	XX
	1	1	1	XX	_		D [7				0	0	00
Read Display Self-Diagnostic	0	1	1	XX	0	0	0	0	1	1	1	1	0Fh
Result	1	1	1	XX	X	X	X	X	X	X	X	X	XX
	1	<u> </u>	1	XX	D [7	Γ.	X	X	X	X	X	X	00
Enter Sleep Mode	0	1	1	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	1	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1		XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1		XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	1	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	1	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1		XX	0	0	1	0	0	1	1	0	26h
	1	1		XX			1	GC [1		01
Display OFF	0	1	1	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	1	XX	0	0	1	0	1	0	0	1	29h
	0	1	1	XX	0	0	1	0	1	0	1	0	2Ah
	1	1		XX				SC [1					XX
Column Address Set	1	1	1	XX				SC [XX
	1	1	1	XX				EC [1					XX
	1	1	1	XX		1	1	EC [7:0]	ı	1		XX
	0	1	1	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	1	XX				SP [1					XX
Page Address Set	1	1	1	XX				SP [7:0]				XX
	1	1	1	XX				EP [1	5:8]				XX
	1	1	↑	XX				EP [7	7:0]				XX





	_			207	T _	_			Ι.		_	_	
Memory Write	0	1	1	XX	0	0	1 -	0	1	1	0	0	2Ch
•	1	1	1	V/V		_) [17:0] 					XX
	0	1	1	XX	0	0	1	0	1	1	0	1	2Dh
	1	1	1	XX						00 [5:0]			XX
	1	1	1	XX						nn [5:0]			XX
	1	1	1	XX						31 [5:0]			XX
Color SET	1	1	1	XX						00 [5:0]			XX
	1	1	1	XX						nn [5:0]			XX
	1	1	1	XX						64 [5:0]			XX
	1	1	1	XX						00 [5:0]			XX
	1	1	1	XX						nn [5:0]			XX
	1	Î	1	XX	_		 			31 [5:0]			XX
Maman, Dood	0	1	1	XX	0	0	1	0	1	1	1	0	2Eh
Memory Read	1	1	1	XX	Х	Χ	Х	X 2 [47:0]	Х	Х	Х	Х	XX
	1	1	1	XX		0	1	1 [17:0]		0	0	0	30h
	<u>0</u> 1	1	<u> </u>	XX	0	U	1	· · · · · · · · · · · · · · · · · · ·	0 R [15:8]	U	0	U	00
Partial Area	1	1	<u> </u>	XX					R [7:0]				00
i aitiai Alea	1	1	<u> </u>	XX					R [15:8]				01
	1	1		XX					R [7:0]				3F
	0	1	<u> </u>	XX	0	0	1	1	0	0	1	1	33h
	1	1	<u></u>	XX	-		_ '		A [15:8]		'	'	00
	1	1		XX					FA [7:0]				00
Vertical Scrolling Definition	1	1	1	XX					A [15:8]				01
Vortical Coloning Deminion	1	1	<u></u>	XX					SA [7:0]				40
	1	1	1	XX					A [15:8]				00
	1	1	1	XX					FA [7:0]				00
Tearing Effect Line OFF	0	1	1	XX	0	0	1	1	0	1	0	0	34h
	0	1	1	XX	0	0	1	1	0	1	0	1	35h
Tearing Effect Line ON	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	М	00
	0	1	1	XX	0	0	1	1	0	1	1	0	36h
Memory Access Control	1	1	1	XX	MY	MX	MV	ML	BGR	МН	Х	Х	00
	0	1	1	XX	0	0	1	1	0	1	1	1	37h
Vertical Scrolling Start Address	1	1	1	XX				VS	P [15:8]		•		00
, and the second	1	1	1	XX					SP [7:0]				00
Idle Mode OFF	0	1	1	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	1	XX	0	0	1	1	1	0	0	1	39h
	0	1	1	XX	0	0	1	1	1	0	1	0	3Ah
Pixel Format Set	1	1	1	XX	Χ		DPI [2:0)]	Χ		DBI [2:0	0]	66
Meito Maraan Caratina	0	1	1	XX	0	0	1	1	1	1	0	0	3Ch
Write Memory Continue	1	1	1					0 [17:0]					XX
	0	1	1	XX	0	0	1	1	1	1	1	0	3Eh
Read Memory Continue	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
	1	1	1					0 [17:0]					XX
	0	1	1	XX	0	1	0	0	0	1	0	0	44h
Set Tear Scanline	1	1	1	XX	Χ	Χ	Χ	Х	Χ	Χ	Х	STS [8]	00
	1	1	1	XX		-	-	S	TS [7:0]	-			00
	0	1	1	XX	0	1	0	0	0	1	0	1	45h
Cot Coonline	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
Get Scanline	1	1	1	XX	Χ	Χ	Χ	Χ	Х	Χ	GT	S [9:8]	00
	1	1	1	XX				G	TS [7:0]				00
Write Display Brightness	0	1	1	XX	0	1	0	1	0	0	0	1	51h
vviite Display Dilgittless	1	1	1	XX				D	BV [7:0]				00





	0	1	1	XX	0	1	0	1	0	0	1	0	52h
Read Display Brightness	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
	1	1	1	XX			•	DBV	[7:0]				00
Mile OTDI Diseles	0	1	1	XX	0	1	0	1	0	0	1	1	53h
Write CTRL Display	1	1	1	XX	Х	Х	BCTRL	Х	DD	BL	Х	Х	00
	0	1	1	XX	0	1	0	1	0	1	0	0	54h
Read CTRL Display	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
	1	1	1	XX	Х	Х	BCTRL	Х	DD	BL	Х	Х	00
Write Content Adaptive	0	1	1	XX	0	1	0	1	0	1	0	1	55h
Brightness Control	1	1	1	XX	Х	Х	Х	Х	Х	Х	C [1:0]	00
Deed Content Adouting	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
Read Content Adaptive Brightness Control	1	1	1	XX	Х	Χ	Х	Х	Х	Х	Х	Х	XX
Brightiness Control	1	1	1	XX	Х	Х	Х	Х	Х	Х	0 [1:0]	00
Write CABC Minimum	0	1	1	XX	0	1	0	1	1	1	1	0	5Eh
Brightness	1	1	↑	XX				CME	8 [7:0]				00
Read CABC Minimum	0	1	1	XX	0	1	0	1	0	1	1	1	5Fh
Brightness	1	1	1	XX	Χ	Χ	Χ	X	Х	Х	Х	Χ	XX
Brighthood	1	↑	1	XX				CME	8 [7:0]				00
	0	1	1	XX	1	1	0	1	1	0	1	0	DAh
Read ID1	1	1	1	XX	Χ	Χ	Χ	X	Х	Х	Х	Χ	XX
	1	1	1	XX			Modu	ıle's Maı	nufacture	e [7:0]			XX
	0	1	1	XX	1	1	0	1	1	0	1	1	DBh
Read ID2	1	1	1	XX	Х	X	Х	X	Х	Х	Χ	Χ	XX
	1	1	1	XX			LCD Mo	dule / Di	river Ver	sion [7:0]		XX
	0	1	1	XX	1	1	0	1	1	1	0	0	DCh
Read ID3	1	1	1	XX	Х	Χ	X	Χ	Χ	Х	Х	Χ	XX
	1	1	1	XX			LCD I	Module /	Driver I	D [7:0]			XX

									l .				
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	He
RGB Interface	0	1	1	XX	1	0	1	1	0	0	0	0	В0
Signal Control	1	1	↑	XX	ByPass_MODE	RCM	[1:0]	Χ	VSPL	HSPL	DPL	EPL	40
France Combrel	0	1	↑	XX	1	0	1	1	0	0	0	1	B1
Frame Control	1	1	↑	XX	X	Χ	Χ	Χ	Х	Х	DIVA	[1:0]	00
(In Normal Mode)	1	1	↑	XX	X	Χ	Χ		R	TNA [4:0	0]		16
F O	0	1	↑	XX	1	0	1	1	0	0	1	0	B2
Frame Control	1	1	↑	XX	X	Χ	Χ	Χ	Х	Х	DIVE	3 [1:0]	0
(In Idle Mode)	1	1	↑	XX	Х	Χ	Χ		R	TNB [4:0	0]		11
Farmer Orantural	0	1	↑	XX	1	0	1	1	0	0	1	1	ВЗ
Frame Control	1	1	↑	XX	X	Χ	Χ	Χ	Х	Х	DIVC	[1:0]	0
(In Partial Mode)	1	1	↑	XX	Х	Χ	Χ		R	TNC [4:0	0]		1
Disales Incoming Octobel	0	1	↑	XX	1	0	1	1	0	1	0	0	Β4
Display Inversion Control	1	1	↑	XX	Х	Χ	Χ	Χ	Х	NLA	NLB	NLC	0:
	0	1	↑	XX	1	0	1	1	0	1	0	1	B
	1	1	↑	XX	0				VFP [6:	0]			0
Blanking Porch Control	1	1	↑	XX	0				VBP [6:	0]			0
Sidinang Foron Control	1	1	1	XX	0	0	0			HFP [4:0]		0.
	1	1	<u></u>	XX	0	0	0			HBP [4:0	 11		1





	0	1	1	XX	1	0	1	1	0	1	1	0	B6h
	1	1	1	XX	Х	Х	Х	Х	PTG	i [1:0]	PT	[1:0]	0A
Display Function Control	1	1	↑	XX	REV	GS	SS	SM			SC [3:0]		82
	1	1	1	XX	Х	Х				NL [5:0]			27
	1	1	1	XX	Х	Х			PO	DIV [5:	0]		XX
Entry Mode Set	0	1	1	XX	1	0	1	1	0	1	1	1	B7h
Liftly Mode Set	1	1	1	XX	X	Х	Χ	Х	DSTB	GON	DTE	GAS	07
	0	1	1	XX	1	0	1	1	1	0	0	0	B8h
Backlight Control 1	1	1	1	XX	Х	Х	Χ	Х	Χ	Χ	Х	X	XX
	1	1	1	XX	Х	Х	Χ	Х		T⊦	I_UI [3:0]		04
	0	1	1	XX	1	0	1	1	1	0	0	1	B9h
Backlight Control 2	1	1	1	XX	Х	Χ	Х	Х	Χ	Χ	X	X	XX
	1	1	1	XX		TH_MV	[3:0]	ı		TH	_ST [3:0]		B8
	0	1		XX	1	0	1	1	1	0	1	0	BAh
Backlight Control 3	1	1	1	XX	Х	Х	Χ	Х	Х	Χ	X	Х	XX
	1	1	1	XX	Х	Х	Χ	Х			H_UI [3:0] I	1	04
	0	1		XX	1	0	1	1	1	0	1	1	BBh
Backlight Control 4	1	1	1	XX	Х	Х	Χ	Χ	X	Χ	Х	Х	XX
	1	1		XX		DTH_M\					H_ST [3:0]		C9
B 181.0 . 15	0	1		XX	1	0	1	1	1	1	0	0	BCh
Backlight Control 5	1	1		XX	Х	X	X	Х	X	Х	X	X	XX
	1	1		XX		DIM2		l ,	X		DIM1 [2:		44
Backlight Control 7	0	1	<u></u>	XX	1	0	1	1	1	1	1	0	BEh
	1	1	1	XX	4		_		I_DIV [7	_			0F
Backlight Control 8	0	1	1	XX	1	0	1	1	1	1	1	1	BFh
	1	1		XX	1 X	1 1	0 0	X 0	0 0	LEDONR 0		LEDPWMOPL	_ 00 C0h
Power Control 1	<u>0</u> 1	1		XX	X		U	U			0	0	1
		1	<u>↑</u>	XX	1	1	0	0	l o	<u>'RH [5:0</u> 0	0	1	26 C1h
Power Control 2	1	1	<u> </u>	XX	X	X	X	X	X	Т	BT [2:		00
	0	1	<u> </u>	XX	1	1	0	0	0	1	0	1 1	C5h
VCOM Control 1	1	1		XX	X			U	VMH	<u> </u>	0	<u> </u>	31
VOOW CONTON	1	1	<u> </u>	XX	X				VML				3C
	0	1	<u> </u>	XX	1	1	0	0	0	1	1	1	C7h
VCOM Control 2	1	1		XX	nVM	-		U	VMF			<u>'</u>	CO
	0	1	1	XX	1	1	0	1	0	0	0	0	D0h
NV Memory Write	1	1	<u> </u>	XX	X	X	Х	X	X		GM_ADR		00
Ter momory tritto	1	1	<u></u>	XX			Λ.	•	DATA [GIVI_/\DIT	[2.0]	XX
	0	1	<u></u>	XX	1	1	0	1	0	0	0	1	D1h
	1	1	<u> </u>	XX	<u> </u>	· ·			Y [23:16		. <u> </u>	· · ·	55
NV Memory Protection Key	1	1	<u> </u>	XX					Y [15:8]				AA
	1	1	<u></u>	XX					EY [7:0]				66
	0	1	<u> </u>	XX	1	1	0	1	0	0	1	0	D2h
	1	<u> </u>	1	XX	X	X	Х	Х	Х	X	X	X	XX
NV Memory Status Read	1	<u></u>	1	XX	X		_CNT		Х		D1_CNT	1	XX
	1	1	1	XX	BUSY		CNT		Х		D3_CNT		XX





	_		,	1									
	0	1	1	XX	1	1	0	1	0	0	1	1	D3h
	1	1	1	XX	Х	Χ	Х	Χ	Х	Χ	Χ	Х	XX
Read ID4	1	1	1	XX	0	0	0	0	0	0	0	0	00
	1	1	1	XX	1	0	0	1	0	0	1	1	93
	1	1	1	XX	0	1	0	0	0	0	0	1	41
	0	1	1	XX	1	1	1	0	0	0	0	0	E0h
	1	1	1	XX	Х	Χ	X	Χ		VP	0 [3:0]		08
	1	1	1	XX	Х	Х			VP1 [5	:0]			0E
	1	1	1	XX	Х	Х			VP2 [5	:0]			12
	1	1	1	XX	Х	Х	Х	Χ		VP	4 [3:0]		05
	1	1	1	XX	Х	Χ	Χ		V	P6 [4	:0]		03
	1	1	1	XX	Х	X	Χ	Χ		VP1	13 [3:0]		09
Positive Gamma	1	1	1	XX	Х			VI	P20 [6:0]				47
Correction	1	1	1	XX		VP36	[3:0]			VP2	27 [3:0]		86
	1	1	1	XX	X			VI	P43 [6:0]				2B
	1	1	↑	XX	X	Χ	Х	Χ		VP	50 [3:0]		0B
	1	1	1	XX	Х	Χ	Χ		VF	P57 [4	1:0]		04
	1	1	1	XX	Х	Χ	Χ	Χ		VPS	59 [3:0]		00
	1	1	1	XX	X	Χ			VP61 [5	5:0]			00
	1	1	1	XX	X	X			VP62 [5	5:0]			00
	1	1	↑	XX	Х	Χ	Χ	Χ		VP6	3 [3:0]	_	00
	0	1	1	XX	1	1	1	0	0	0	0	1	E1h
	1	1	1	XX	X	Χ	X	Χ		VN	0 [3:0]		08
	1	1	↑	XX	Χ	Χ			VN1 [5	:0]			1A
	1	1	↑	XX	Х	Χ			VN2 [5	:0]			20
	1	1	1	XX	Х	Χ	Χ	Χ		VN	4 [3:0]		07
	1	1	↑	XX	Χ	Χ	Χ		V	N6 [4	:0]		0E
	1	1	1	XX	X	Χ	Χ	Χ		VN1	13 [3:0]		05
Negative Gamma	1	1	1	XX	X			1V	N20 [6:0]				3A
Correction	1	1	↑	XX		VN36	[3:0]			VN2	27 [3:0]		8A
	1	1	1	XX	X			1V	N43 [6:0]				40
	1	1	↑	XX	Х	X	X	Χ		VNS	50 [3:0]		04
	1	1	↑	XX	Χ	Χ	Χ		1V	N57 [4	1:0]		18
	1	1	↑	XX	Х	Х	Х	Χ		VNS	59 [3:0]		0F
	1	1	↑	XX	Х	Χ			VN61 [5:0]			3F
	1	1	↑	XX	Х	Χ			VN62 [5:0]			3F
	1	1	↑	XX	Х	Х	Х	Χ		VN6	33 [3:0]		0F
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1 st Parameter	1	1	<u></u>	XX		RCA0	[3:0]			BCA	A0 [3:0]		XX
:	1	1	1	XX		RCAx	[3:0]			BCA	Ax [3:0]		XX
16 th Parameter	1	1	↑	XX		RCA15					15 [3:0]		XX
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1 st Parameter	1	1	1	XX		RFA0	[3:0]			BF/	0:6]		XX
:	1	1	<u></u>	XX		RFAx	[3:0]				Ax [3:0]		XX
64 th Parameter	1	1		XX		RFA63	[3:0]				63 [3:0]		XX
	0	1		XX	1	1	1	1	0	1	1	0	F6h
late (O : 1	1	1	1	XX	MY_EOR	MX_EOR	MV_EOR	Х	BGR_EOR	Χ	Х	WEMODE	01
Interface Control	1	1	1	XX	X	X	EPF [X	Χ		T [1:0]	00
	1	1	1	XX	Х	Х	ENDIAN	X	DM [1:		RM	RIM	00
	<u> </u>												

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP





(00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9341 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.







8.2. Description of Level 1 Command

8.2.1. NOP (00h)

00h					NOP (No	o Opera	ation)								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h		
Parameter					No P	aramete	er.								
Description		emory Writ		nmand; it does not ha	-			-					erminate		
Restriction	None														
		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes													
Register				Normal Mode On,					Yes						
Availability				Partial Mode On,	Idle Mod	le Off, S	Sleep Ou	ıt	Yes						
,				Partial Mode On,	Idle Mod	le On, S	Sleep Ou	ıt	Yes						
					Sleep In				Yes						
				5	Status		Default '	Value							
Default				Power C	n Seque	ence	N/A	١							
Boladit				SV	V Reset		N/A	١							
				HV	V Reset		N/A	١							
Flow Chart	None														





8.2.2. Software Reset (01h)

01h					SV	VRESET							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Parameter					No F	Paramete	er.						
	When the	Software	Reset com	mand is written, it c	auses a	software	e reset.	It reset	s the co	mmand	s and pa	ırameter	s to thei
	S/W Rese	et default v	alues. (See	default tables in each	ch comm	nand des	cription	.)					
Description	Note: The	Frame M	emory conte	ents are unaffected b	y this co	ommand							
	X = Don't	care.											
			n wait 5mse	ec before sending ne	w comm	and follo	owina sa	oftware r	eset Th	e displa	v module	e loads a	all displa
		•		o the registers during			•			•	•		
Restriction		-								_			
	necessary	y to wait 12	20msec bef	ore sending Sleep o	ut comm	nand. So	ftware F	Reset Co	ommand	cannot	be sent	during S	Sleep Ou
	sequence).											
					_								
				Normal Mode On,	Status Idlo Mo	do Off (Sloop O		ailability Voc				
Register				Normal Mode On,					Yes Yes				
Availability				Partial Mode On,					Yes				
•				Partial Mode On,			Sleep Ou		Yes				
					Sleep In				Yes				
					Status		Default						
Default				Power (N/A						
					V Reset V Reset		N/ <i>A</i>						
								<u>'</u>					
				SWRESET(01h)									
							ı— — ·				- ¬		
							į	Le	egend				
										\neg	Ì		
						\		Co	mmand	Щ,	į		
			Dis	play whole blank scr	een		1 /	Pai	rameter		ļ		
					/	/	i	D	isplay	_	-		
Flow Chart					/								
				\downarrow					Action	<i>></i>	į		
				V			(N	Mode		i		
			/	/ Set Commands to			į						
			(S/W Default			! (Sequen	tial trans	sfer	-		
				Values	/					<u> </u>	j		
							= -	- •	- 	-			
			,	_									
				Sleep In Mode									
			\		/								





8.2.3. Read display identification information (04h)

04h				RDDIDIF (Re	ad Disp	lay Ider	ntificatio	n Inforr	nation)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h		
1 st Parameter	1	1	1	XX	Χ	Χ	Х	Χ	Χ	Χ	Χ	Χ	Х		
2 nd Parameter	1	1	1	XX				ID1	[7:0]				XX		
3 rd Parameter	1	1	1	XX				ID2	[7:0]				XX		
4 th Parameter	1	1	1	XX				ID3	[7:0]				XX		
Description	The 1 st The 2 nd The 3 rd	paramete paramete paramete	r is dumm er (ID1 [7:0 r (ID2 [7:0	its display identificati y data.)]): LCD module's ma]): LCD module/drive]): LCD module/drive	anufactur er versior	er ID.									
Restriction															
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes Status Default Value													
Default					Status On Seq SW Rese	et	See de	It Value scription scription scription	1						
Flow Chart			2nd Param 3rd Param	eter: Dummy Read leter: Send LCD module' eter: Send panel type an eter: Send module/driver	s manufac	turer inforver versio		ion	/	7	F	Command Parameter Display Action Mode			



Description

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K color



8.2.4. Read Display Status (09h)

09h				RDI	OST (Re	ad Disp	lay Stat	us)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1 st Parameter	1	↑	1	XX	Χ	Х	Х	Х	Х	Х	Х	Х	Χ
2 nd Parameter	1	↑	1	XX				D [31:25]			0	00
3 rd Parameter	1	↑	1	XX	0	I	D [22:20]		D [1	9:16]		61
4 th Parameter	1	↑	1	XX	0 0 0			0	0		D [10:8]		00
5 th Parameter	1	↑	1	XX		D [7:5]		0	0	0	0	0	00

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
Dot	Poostor voltage status	0	Booster OFF
D31	Booster voltage status	1	Booster ON
D30	Row address order	0	Top to Bottom (When MADCTL B7='0')
D30	now address order	1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	0	Left to Right (When MADCTL B6='0').
DZ9	Column address order	1	Right to Left (When MADCTL B6='1').
Dae	Pow/oolumn ovohongo	0	Normal Mode (When MADCTL B5='0').
D28	Row/column exchange	1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	0	LCD Refresh Top to Bottom (When MADCTL B4='0')
DZI	Vertical refresh	1	LCD Refresh Bottom to Top (When MADCTL B4='1').
Doc	DCD/DCD order	0	RGB (When MADCTL B3='0')
D26	RGB/BGR order	1	BGR (When MADCTL B3='1')
DOE	Llovizontal rafrach ardar	0	LCD Refresh Left to Right (When MADCTL B2='0')
D25	Horizontal refresh order	1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	0	
D23	Not used	0	
D22		101	4.C. lait/aireal
D21	Interface color pixel format	101	16-bit/pixel
521	definition	110	18-bit/pixel
D20			
D19	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON.
D17	Sleep IN/OUT	0	Sleep IN Mode
	5.55p, 5 5 .	1	Sleep OUT Mode.
D16	Display normal mode ON/OFF	0	Display Normal Mode OFF.
	Diopiay normal mode of the fi	1	Display Normal Mode ON.
D15	Vertical scrolling status	0	Scroll OFF
D14	Not used	0	
D13	Inversion status	0	Not defined
D12	All pixel ON	0	Not defined
D11	All pixel OFF	0	Not defined
D10	Display ON/OFF	0	Display is OFF
טוט	Display Olv/Ol 1	1	Display is ON
D9	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
פט	rearing enect line ON/OFF	1	Tearing Effect ON
		000	GC0
		001	
D[8:6]	Gamma curve selection	010	
		011	
		other	Not defined

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				0		Mode 1, V-BI	anking only
		D5	Tearing effect line mode	1	Mode		king and V-Blanking.
		D4	Not used	0			
		D3	Not used	0			
		D2	Not used	0			-
		D1	Not used	0			-
		D0	Not used	0			-
	X = Don	't care					
Restriction							
				Status		Availability	
			Normal Mode On		Off. Sleep Out	Yes	
Register			Normal Mode On			Yes	
Availability			Partial Mode On,			Yes	
			Partial Mode On,	Idle Mode C	n, Sleep Out	Yes	
				Sleep In		Yes	
			Sta	atus	Default Va	lue	
Default			Power Or	Sequence	32'h006100	00h	
				Reset	32'h006100		
			HW	Reset	32'h006100	00h	
							Li
							Legend
			RDDST(09	9h)			Command
					Host		Parameter
					Driver		
Flow Chart	_	1	st Parameter: Dummy Read		Dilvei		Display
		2	and Parameter: Send D[31:25] display and Parameter: Send D[19:16] display			/	Action
		4	th Parameter: Send D[10:8] display s	tatus			Mode
		5	th Parameter: Send D[7:5] display st	atus		/	
							Sequential transfer





8.2.5. Read Display Power Mode (0Ah)

0.2.5. nea		י ניייקי	31701 IV	.540	<u> </u>	M (Read	Display	v Power	Mode)					
VAII				I		-					I	Ι		
	D/CX	RDX	WRX		D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1		XX	0	0	0	0	1	0	1	0	0Ah
1 st Parameter	1	1	1		XX	X	X	X	X	X	X	X	X	X
2 nd Parameter	1	<u> </u>	1		XX	D7	D6	D5	D4	D3	D2	D1	D0	80
	This cor	mmand inc	licates the (current	status of the	display	as desc	ribed in t	he table	below::				
				Bit	Value	D	escription	on	(Commer	nt			
				D7	0	Booster								
			-			Booster C)K					
				D6	0		e Mode							
			-		1		e Mode							
				D5	0		ial Mode							
Description			}		1		ial Mode							
Description				D4	1		ep In M ep Out N							
			ŀ		0	Display I			f					
				D3	1	Display I								
				D2	0		splay is		•					
			Ī	Set to '0)'									
)'										
	X = Dor	ı't care												
Restriction														
						Status	3		Av	ailability	,			
				No	rmal Mode C			, Sleep (Yes				
Register				No	rmal Mode C	n, Idle M	ode On	, Sleep (Out	Yes				
Availability				Pa	artial Mode C	n, Idle M	ode Off,	Sleep C	ut	Yes				
				Pa	artial Mode C	n, Idle M	ode On,	Sleep C	ut	Yes				
						Sleep I	n			Yes				
						Status		Default	t Value					
5 ();					Powe	r On Seq	uence	8'h(
Default						SW Rese		8'h(
						HW Rese		8'h()8h					
				-			1				į	L	egend	il
					RDDPM	(0Ah)					į			$\neg : \square$
				L				1			į	$\overline{}$	ommand	⇒ ;
								lost			- į	P	arameter	_/
Flow Chart	_				₩		D	river			i		Display	_)
1 low Chart			4 - 4 D 4 -	D	DI						/ i		Action	> 1
	/		1st Paramete 2nd Paramet		ny Read d D[7:2] display	power mo	de status			/	/ ¦		Mode	<u> </u>
										/	į		woue	ノ il
											į	Seque	ntial trans	sfer i
											į			≤
<u> </u>	L										- '-			





8.2.6. Read Display MADCTL (0Bh)

0.2.0. nea		, t t		(0	RDDMA	DCTL (Read Di	enlav M	ADCT!	1					
OBII			ı			1	1	1		T	ı	ı	ı		
	D/CX	RDX	WR	X	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1		XX	0	0	0	0	1	0	1	1	0Bh	
1 st Parameter	1		1		XX	X	X	X	X	X	X	X	X	X	
2 nd Parameter	1	<u> </u>			XX	D7	D6	D5	D4	D3	D2	D1	D0	00	
	I his co	mmand ind	dicates	the curre	nt status of the	display	as desc	ribed in 1	the table	e below:					
			Bit	Value		[Descript	ion			Comi	ment			
			D7	0		Bottom	`					-			
				1		to Top).		-			
			D6	0		o Right (
				1		to Left (
			D5	0		al Mode									
Description				0	LCD Refresh	Se Mode									
			D4	1	LCD Refresh		,								
				0		GB (Wh				<u> </u>					
			D3	1		GR (Whe									
				-											
		D2 1 LCD Refresh Right to Left (When MADCTL B2='1') D1 Switching between Segment outputs and RAM Set to '0'													
			D1	RAM	Set t	o '0'									
			Set t	o '0'											
	X = Dor	D0 Switching between Segment outputs and RAM Set to '0' X = Don't care													
Restriction															
ricotriction															
						Status			۸,	/ailability	,				
					lormal Mode O			Sleen (Yes	_				
Register					Iormal Mode O					Yes					
Availability					Partial Mode Or					Yes					
Availability					Partial Mode Or					Yes					
						Sleep I				Yes					
									·						
										1					
						Status		Defaul	t Value						
Default						On Seq			00h						
						W Rese		No Cl		1					
					<u> </u>	IW Rese	Σ	8'h	Jun]					
							7				ŗ		 egend	1	
											- !	_	egenu	il	
					RDDMADCT	L(0Bh)					į		Command		
							_ -	lost			- !	P	'arameter	-	
								 river			-			= $ $	
Flow Chart	_				V						\neg !		Display	-/ il	
	/				mmy Read						/ !		Action	>	
			2nd Par	ameter: Se	end D[7:2] display	power mo	de status			/	/ ! !		Mode	$\supset $	
										/	!			\subset \Box	
											!	Seque	ential trans	sfer	
											 -				





8.2.7. Read Display Pixel Format (0Ch)

		piay		<u> </u>	<u> </u>	PDDCO	LMOD /	Dood Di	onlo	v Dis	ral E	'o uma	a#\				
0Ch		ı				RDDCO	1	1	1						I	l	I
	D/CX	RDX	W	/RX		D17-8	D7	D6	D:		D4	_	D3	D2	D1	D0	HEX
Command	0	1		1		XX	0	0	0		0	-	1	1	0	0	0Ch
1 st Parameter	1	1		1		XX	X	Х	X		Х		X	Х	X	Х	X
2 nd Parameter	1	1		1 .		XX	RIM		<u>DPI </u>				0		DBI [2:0]		06
	This co	mmano r	indica			urrent status of th	ne dispia	y as des	cribe								
			RIM		PI [2:			ormat		DI	BI [2		MCL		ce Forma	at	
		-	0	0	0		eserved		4	0	0	0		Reser		_	
		-	0	0	0		eserved		_	0	0	1		Reser			
		ŀ	0	0	1		eserved		-	0	1	0		Reser			
		ŀ	0	1	0		eserved eserved		-	1	0	0		Reser			
Description		-	0	1	0		oits / pixe	اد	-	1	0	1		16 bits /			
·		-	0	1	1		oits / pixe			1	1	0		18 bits /			
		Ī	0	1	1		eserved			1	1	1		Reser			
			-	4	^	16 k	oits / pixe	el								<u></u>	
			1	1	0	1 (6-bit 3 tim											
			1	1	1	()	oits / pixe										
		L				(6-bit 3 tim	es data	transfer)									
	X = Doi	n't care															
Restriction																	
					.y												
						Normal Mode	On, Idle	Mode O	ff, SI	еер	Out		Yes				
Register						Normal Mode	On, Idle	Mode O	n, SI	еер	Out		Yes				
Availability						Partial Mode (On, Idle	Mode Of	ff, Sle	ер (Out		Yes				
						Partial Mode (n, Sle	еер (Out	-	Yes				
							Slee	o In					Yes				
						Ctatus			D	efau	lt Va	lue					
						Status		RIM		DP	I [2:0)]	DB	I [2:0]			
Default				-	Pov	er On Sequence		1'b0		3't	000		3'l	b110			
				=		SW Reset	+	Chang		No (Chang			
				<u>_</u>		HW Reset		1'b0		3't	0000		3'l	b110			
								7						Ţ		egenc	
														į	L	-cyciic	<u> </u>
						RDDCOLN	MOD(0Ch)							į		Command	
									Hos	t				į	F	Parameter	-7
							 ,		– – - Drive	– – – er				i		Display	= $ $
Flow Chart	_					· · · · · · · · · · · · · · · · · · ·	<u> </u>							─7			\prec \sqcup
			1st	Para	mete	: Dummy Read r: Send D[7:2] displa	u nival far	mat atatu	_					/ i	\leq	Action	<u> </u>
	/		2n	u rari	amete	i. פווט טן ו.צן aispia	y pixel 101	ıııaı Statüs	5				/	/ į		Mode	
													/	į			-
														į	Sequ	ential tran	ster
														<u>i.</u>			





8.2.8. Read Display Image Format (0Dh)

0Dh					RDD	IM (Read	d Displa	y Image	Mode)					
	D/CX	RDX	WRX	D1	7-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	>	Χ	0	0	0	0	1	1	0	1	0Dh
1 st Parameter	1	1	1	>	X	Х	Χ	Χ	Χ	Х	Χ	Χ	Χ	Χ
2 nd Parameter	1	1	1	>	ΧX	0	0	0	0	0		D [2:0]		00
Description	This cor		dicates the	e current s	D [2 00 00 01 01 Oth	2:0] 00 11 0	Gamr	Descripent of the control of the con	tion e 1 (G2.2					
Restriction														
Register Availability				Norn Part	nal Mode (nal Mode (ial Mode C ial Mode C	On, Idle I On, Idle I	Mode Of Mode Or Mode Off Mode Or	n, Sleep , Sleep (Out Out Out	vailability Yes Yes Yes Yes Yes Yes Yes	/			
Default					Power On SW I	atus Sequen Reset Reset	ice	3'b 3'b	o000 0000 0000					
Flow Chart				eter: Dummy eter: Send [RDDIM]	Host Driver		/		P	Command Carameter Display Action Mode	





8.2.9. Read Display Signal Mode (0Eh)

0Eh				·	RDDSM (Read Disp	lay Sign	al Mode	<u>:</u>)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	0	0	1	1	1	0	0Eh
1 st Parameter	1	1	1	XX	Х	Х	Х	Χ	Х	Χ	Х	Х	Х
2 nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00
Description				he current state Bit Va D7 C D6 C D5 C D4 C D3 C D1 C D0 C	us of the dis ue Tearir Tearir Tearir Tearir Horizo Vertic Vertic Pixel o Data e Data e Reser	g effect ling ling effect ling effect ling effect ling effect ling ling effect	pescribed in Descript e OFF e ON e mode 1 e mode 2 (RGB int (RGB int GB interf GB interf GB interf GLK, RG CLK, RG , RGB int	the tablicant th	DFF DN F ace) OFF	:	,		
Restriction													
Register Availability		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes											
Default					Power Or SW	atus Sequence Reset Reset	e 8'	ult Value h00h h00h h00h	9				
Flow Chart				meter: Dummy R meter: Send D[7		al mode stat	Host Driver					Command Parameter Display Action Mode	





8.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh				RDDSDF	R (Read D	isplay S	Self-Dia	gnostic	Result)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	0	0	1	1	1	1	0Fh
1 st Parameter	1	1	1	XX	Х	Х	Χ	Χ	Х	Х	Х	Х	Χ
2 nd Parameter	1	1	1	XX	D7	D6	0	0	0	0	0	0	00
	Bit		Descripti						ction				
	D7		ter Loading		Invert th						operly.		
	D6	Fur	nctionality D		Invert th	e D6 bit	if the dis	splay is t		lity			
Description	D5 D4		Not Use						ʻ0'				
Description	D3		Not Use						ʻ0'				
	D2		Not Use						·0'				
	D1		Not Use						'0'				
	D0		Not Use						'0'				
		•											
Restriction													
		Status Availability											
										ity			
Register				Normal Mod					Yes				
				Normal Mod					Yes				
Availability				Partial Mode Partial Mode					Yes Yes				
				Fartial Mou	Slee		ni, Sieel	Out	Yes				
					0.00	P		•	100				
					0			11.37.1					
				Da	Statu			ault Valu	e				
Default				PC	wer On S SW Re			3'h00h 3'h00h					
					HW Re			3'h00h					
					1100 110	,00t		7110011					
						\neg				[Legend	
				RDD:	SDR(0Fh)								-
					1							Command	
							Host					Paramete	
	Driver												\equiv
Flow Chart					·							Action	\leq \Box
				Dummy Read : Send D[7:6] disp	olay self-dia	anostic st	atus			/ ¦	\sim		\leq \Box
					,					/ ¦		Mode	_)
										 	Sen	uential trar	nsfer
										 	000	-	
										I			'





8.2.11. Enter Sleep Mode (10h)

10h	SPLIN (Enter Sleep Mode)														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h		
Parameter						No Para	meter								
	This comm	nand cause	es the LCD	module to e	nter the	minimur	m power	consun	nption m	ode. In t	this mod	le e.g. th	e DC/DC		
	converter i	s stopped,	Internal osci	llator is stopp	ed, and	panel sc	anning is	stoppe	d.						
Description															
	MCLL inter	face and m	emory are si	ill working an	nd the me	emory ke	ens its c	ontents							
	X = Don't		oo., a.o.			,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	opoo o								
				en module is		•		-			-	-	•		
Restriction	Command	(11h). It w	vill be neces	sary to wait	5msec b	efore se	nding ne	ext to co	mmand,	this is to	allow t	ime for th	ne supply		
1100111011011	voltages a	nd clock cir	cuits to stab	ilize. It will be	necessa	ary to wa	it 120ms	ec after	sending §	Sleep Ou	ut comma	and (wher	n in Sleep		
ı	In Mode) b	efore Slee	o In commar	nd can be ser	nt.										
			-	Name al Made		atus	O# Olass		Availabili	ty					
Register				Normal Mode					Yes Yes						
Availability									Yes						
,		Partial Mode On, Idle Mode On, Sleep Out Yes													
			L		Sle	ep In			Yes						
									_						
					Statu			ult Value							
Default				Pov	sw Re	equence		IN Mod IN Mod							
					HW Re			IN Mod							
	It takes 12	0msec to g	et into Sleep	In mode afte	er SLPIN	commar	nd issued	l.		.—					
						_				į	L	egend	İ		
							\neg			-			つ !		
		SPLIN (10	lh)			DO/DO				ľ		ommand	<u></u> i		
		01 2.11 (10	,			op DC/DC onverter	,)			-	P	arameter	_/ !		
										 		Display	$\overline{}$		
							_			İ		Action	<u> </u>		
		y whole blai		\			\neg			į			\leq \mid		
Flow Chart		natic No effe)	/		. \			į		Mode	_) ¦		
		., 61 1 661111	/	/	Sto	op Interna Oscillator				į	Sogue	ential trans	for		
										-	Seque		į		
										'_ .			نـــــ		
	/	Drain char													
		from LCI			Sle	ep In Mod	le)								
		panel					/								
	\		/												

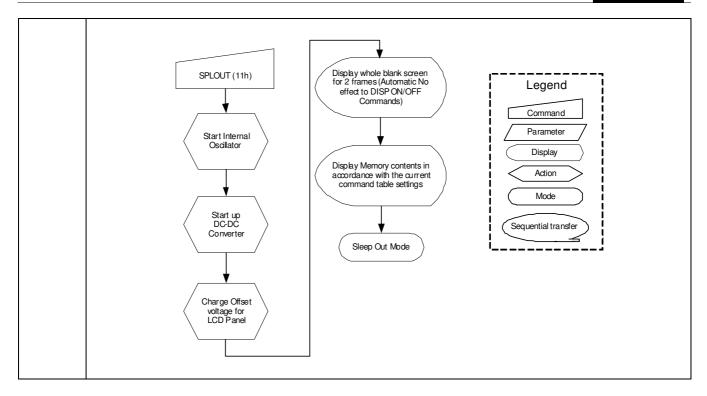




8.2.12. Sleep Out (11h)

11h	SLPOUT (Sleep Out)														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h		
Parameter						No Para	meter								
Description		de e.g. the I	off sleep mo	de. erter is enabl	ed, Inter	nal oscill	ator is st	arted, a	nd panel :	scanning	j is starte	ed.			
Restriction	Command and clock 5msec and when this functions of	is command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In mmand (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages diclock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this sec and there cannot be any abnormal visual effect on the display image if factory default and register values are same en this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic actions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) fore Sleep Out command can be sent.													
Register Availability				Normal Mode Normal Mode Partial Mode Partial Mode	e On, Idle e On, Idle e On, Idle e On, Idle	e Mode C e Mode C e Mode C	on, Sleep	Out Out Out	Availabili Yes Yes Yes Yes Yes	ty					
Default				Pov	Statu ver On S SW Re HW Re	equence set	Sleep	ult Valu IN Mod IN Mod IN Mod	le le						
Flow Chart	It takes 12	0msec to b	ecome Slee	p Out mode a	after SLP	OUT cor	nmand is	ssued.							









8.2.13. Partial Mode ON (12h)

12h					PTLOI	N (Partia	l Mode	On)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h		
Parameter						No Para	meter								
Description		de, the Nor	-	node The part				-	the Part	ial Area	commar	nd (30H).	To leave		
Restriction	This comm	nis command has no effect when Partial mode is active.													
.		Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes													
Register				Normal Mode	On, Idle	Mode C	On, Sleep	o Out	Yes						
Availability				Partial Mode	On, Idle	Mode C	ff, Sleep	Out	Yes						
				Partial Mode	On, Idle	Mode C	n, Sleep	Out	Yes						
					Slee	ep In			Yes						
Default															
Flow Chart	See Partia	l Area (30h)												





8.2.14. Normal Display Mode ON (13h)

13h				NORON	(Norm	al Displa	ay Mode	e On)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Parameter					No F	Paramete	er						
Description	Normal di	splay mode	e on means	ay to normal mode. Partial mode off. mode On command	l (12h)								
Restriction	This com	mand has r	no effect wh	en Normal Display n	node is	active.							
Register Availability				Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes									
Default				Status Power On Sec SW Rese	et	Norma Norma	Default ' al Displa al Displa al Displa	y Mode y Mode	ON				
Flow Chart	See Partia	al Area (30	h)										





8.2.15. Display Inversion OFF (20h)

20h DINVOFF (Display Inversion D/CX RDX WRX D17-8 D7 D6 D5 D4 Command 0 1 ↑ XX 0 0 1 0 Parameter No Parameter This command is used to recover from display inversion mode.	D3 0	D2	D1	T 50	DISPIRY ITVEISION OFF (2011) DINVOFF (Display Inversion OFF)													
Command 0 1 ↑ XX 0 0 1 0 Parameter No Parameter					HEX													
Parameter No Parameter		0	0	D0 0	20h													
			<u> </u>		20													
This command makes no change of the content of frame memory.																		
This command doesn't change any other status.																		
Memory	Display	Panel																
	1111		_															
Description																		
			_															
			<u> </u>															
 																		
X = Don't care																		
Restriction This command has no effect when module already is inversion OFF mode.																		
	Status Availability																	
Register Normal Mode On, Idle Mode Off, Sleep O	Normal Mode On, Idle Mode Off, Sleep Out Yes																	
Availability Partial Mode On, Idle Mode Off, Sleep Or																		
Partial Mode On, Idle Mode On, Sleep O	ıt Yes	5																
Sleep In	Yes	3																
Status Default																		
Default Power On Sequence Display Inverse SW Reset Display Inverse SW Reset Display Inverse Di																		
HW Reset Display Inve																		
<u></u>	Legen																	
(Display Inversion On Mode	Logon	<u> </u>	l I															
	Commar	nd	į															
<u> </u>			l I															
	Paramet	er /	1															
Flow Chart INVOFF(20h)	Display		į															
Flow Ghart	Action	>	į															
			İ															
	Mode		l l															
Display Inversion Off Mode		un afe ::	į															
	equential tra	inster	į															
i																		





8.2.16. Display Inversion ON (21h)

0.2.10.	DINVON (Display Inversion ON)														
21h		I			T	T		ı	ı				1=		
0	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command Parameter	0	1	1 1	XX	0	0 No	1 Paramete	0 r	0	0	0	1	21h		
Parameter	This or		l is used t	o enter into disp	alas dias da ra			r							
				·	•										
	This co	ommano	l makes n	o change of the	e content o	of frame m	emory. Ev	ery bit is	inverted f	rom the fr	ame men	nory to the	e display.		
	This co	ommano	l doesn't d	change any othe	er status.										
	To exit	t Display	inversior	n mode, the Dis	play invers	sion OFF	command	(20h) sho	ould be wi	ritten.					
		, ,						,				_			
		•		$\bot \bot \bot \bot$	Ш	_		_							
			-		$\sqcup \!\!\!\! \perp$	_		_				_			
Description		•			$\vdash\vdash\vdash$	_	N	_				_			
					$\vdash\vdash\vdash$	-						_			
		•			 	_	$\neg /$	_				_			
		•				_	V								
		•				_									
					\Box			_							
			1 1							1 1 1		l			
	X - Dc	n't care													
Restriction	This co	This command has no effect when module already is inversion ON mode.													
				Norm	nal Mode C	Status		loop Out	Availab Yes						
Register					nal Mode C				Yes						
Availability					al Mode O				Yes						
7					al Mode O				Yes						
						Sleep II	า		Yes	;					
					Status		Г	efault Va	lue						
Defeat				Powe	er On Sequ	uence		ay Inversi							
Default					SW Reset			ay Inversi							
					HW Reset	t	Displa	ay Inversi	on OFF						
							ŗ		Logor		- 7				
							¦		Leger	iu -	į				
				Display Inv	vorsion Or	Modo			Commar	ad	i				
				Display III	version or	i wode	/ i		Comma	<u>iu</u>	1				
							- !		Paramet	er/	į				
					▼		į		Display	}	-				
Flow Chart							i				į				
				IN	VON(21h)		!		Action	_>	i				
							į		Mode		-				
					\downarrow		I I				į				
1							į	San	uential tra	ansfer					
				Display Inv	version Of	T Mode	<i>)</i> ¦	Joeq			ļ				
							1				_				





8.2.17. Gamma Set (26h)

0.2.17.	GAMSET (Gamma Set)												
26h					GAM	ISET (Ga	ımma Se	et)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	0	1	1	0	26h
Parameter	1	1	1	XX					[7:0]				01
	This comn	nand is use	d to select t	he desired G	amma cı	irve for t	ne currei	nt displa	ay. A max	imum of	4 fixed (gamma cı	ırves can
	be selecte	d. The curv	e is selected	d by setting th	e approp	oriate bit	in the pa	ramete	r as desci	ibed in t	he Table	:	
				GC [7:	0]	Cur	ve Selec	ted					
				01h		Gamma	a curve 1	(G2.2)					
Description				02h									
				04h									
	Noto: All o	thor volues	ara undafin	08h									
			are undefin	eu.									
	X = Don't	care											
Doctriction	Values of	GC [7:0] no	t shown in ta	able above ar	e invalid	and will	not chan	ge the	current se	lected G	amma c	urve until	valid
Restriction	value is re	ceived.											
						atus			Availabili	ty			
Register				Normal Mode					Yes				
			-	Normal Mode					Yes				
Availability			F	Partial Mode Partial Mode					Yes Yes				
			F	T artial Mode		ep In	п, оксор	Out	Yes				
			_					u.					
							I						
				D	Stati			ult Valu	е				
Default				P0'	SW R	Sequence		<u>'h01h</u> 'h01h					
					HW R			'h01h					
						7	ı						
									Lege	HIU	į		
				GAMSET	(26h)		į	_]		
								<u> </u>	Comm	and			
				\downarrow					Param	eter	/ ¦		
				V			7		Displa	av.			
Flow Chart			/ 1	st Parameter	: GC[7:0]	Ι,	/			·,	/ į		
		,	/			/		<	Actio	n	>		
							i		Mod				
				\forall					14100		/ <u> </u>		
					_		į	(S	equential	transfer	\		
						\rangle	i	3		a. 13161	ノi		
							ı						
				New Gamma Loade				S	equential	transfer			





8.2.18. Display OFF (28h)

0.2.10.	DISPOFF (Display OFF)															
28h		ı			T	1	T			T	T		T			
0	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
Command	0	1	1 ↑	XX	0	0	1	0	1	0	0	0	28h			
Parameter	This s		1:1	e antanimta DIC	PDL AV OF		Paramet			Гиана в M		مام مامام ما	بامرها امرا			
		ommano nserted.	i is used t	o enter into DIS	SPLAY OF	·F mode. I	n this mo	ide, the out	tput from	Frame M	emory is o	disabled a	nd blank			
			l makes n	o change of co	ntents of f	rame men	norv.									
				t change any ot			,									
				nal visible effect												
ı				Mei	mory				Display I	Panel						
Description						+	_	#			_ _ _					
											— —- —					
						+		#			<u> </u>					
	X = Do	n't care														
Restriction	This co	This command has no effect when module is already in display off mode.														
	Status Availability															
				Norm	al Mode (On, Idle M	ode Off, S	Sleep Out	Yes	3						
Register								Sleep Out	Yes							
Availability						On, Idle Mo			Yes							
				Parti	al Mode C	On, Idle Mo		Sleep Out	Yes							
						Sleep I	n		Yes	<u> </u>						
						Status		Default Va	lue							
Default					Powe	er On Seq	uence	Display Ol	FF							
						SW Rese		Display Of								
						HW Rese	t	Display Ol	FF							
								<u> </u>	 Lege		- 7					
				Displa	ay On Mod	de		<u> </u>								
						/	/	¦	Comma		İ					
					▼			<u> </u>	Parame	=	İ					
Flow Chart				DISF	POFF (28h	1)			Display	=						
					<u> </u>				Action Mode		i i					
l				Displa	y Off Mod	de		Sea	uential tr							
						/	/				_					





8.2.19. Display ON (29h)

0.2.13.		· , ·	14 (23)	-,									
29h			1		T	DISPO	N (Display	(ON)		T			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	0	0	1	29h
Parameter							Paramete						
	This co	ommano	l makes n	o recover from to change of corchange any other	ntents of f	rame men		from the	Frame Me	emory is e	nabled.		
				Memory					Disp	olay Par	nel		
			+	++++	+++	_		4	+	H	H	_	
Description						- - - -						- - - - - -	
	X = Do	on't care						•	' '				
Restriction	This co	ommano	l has no e	ffect when mod	lule is alre	ady in dis	play on m	ode.					
Register Availability				Norm Partia	al Mode C al Mode C al Mode C al Mode C	On, Idle Mo	ode Off, S ode On, S ode Off, S ode On, S	leep Out	Availab Yes Yes Yes Yes	i			
Default						Status er On Sequ SW Rese HW Rese	uence I	Default Va Display O Display O Display O	FF FF				
Flow Chart				DI	SPON(29)	h)			Commander Parameter Display Action Mode				

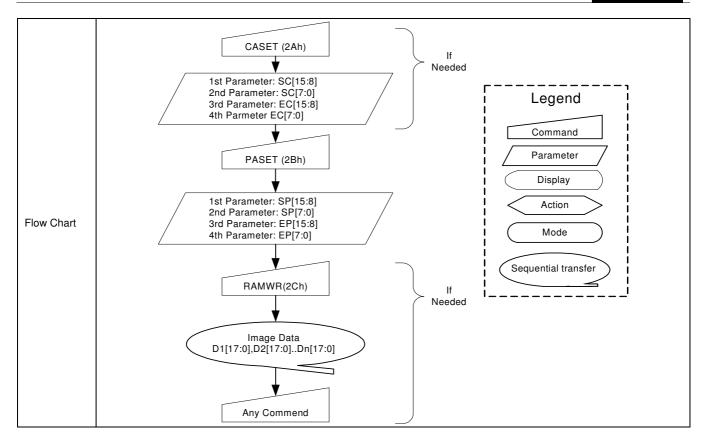




8.2.20. Column Address Set (2Ah)

2Ah				oct (ZAII)	CA	SET (Col	lumn Add	dress Set)				
	D/OV	DDV	MDV	D47.0		1		1	•			Do.	ШБУ
Commercial	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command 1 st Parameter	0	1	<u></u>	XX	0	0	1 0040	0	1	0	1	0	2Ah
2 nd Parameter	1	1	<u></u>	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
3 rd Parameter	1	1	<u></u> ↑	XX	SC7	SC6 EC14	SC5	SC4 EC12	SC3	SC2	SC1	SC0	
4 th Parameter	1	1		XX	EC15	EC14	EC13	EC12	EC11 EC3	EC10 EC2	EC9 EC1	EC8 EC0	Note1
4 Farameter			:		EC7		EC5						
Description	other o	driver st	atus. Th	to define area of e values of SC line in the Frame	[15:0] aı	nd EC [1:			vhen RAN			_	
Restriction	SC [15	: When	SC [15:0	be equal to or les or EC [15:0] is of the control of the control or EC [15:0] is of the control or	greater th	nan 00EF		MADCTL'	s B5 = 0)	or 013Fh			
Register Availability				Normal Partial	Mode C Mode O	n, Idle Mo n, Idle Mo	ode On, S ode Off, S ode On, S	Sleep Out Sleep Out Sleep Out	Availab Yes Yes Yes Yes	; ;			
Default			Por	Status wer On Sequence SW Reset HW Reset	SC [15:0]=000 15:0]=000 15:0]=000	00h 00h	MADCTL's MADCTL's	C [15:0]=0 B5 = 0: E	C [15:0]= C [15:0]=			





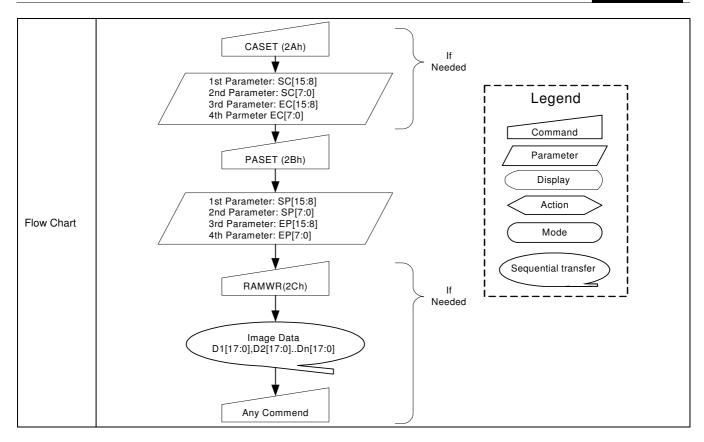




8.2.21. Page Address Set (2Bh)

	aye I	-uui c	,33 3	et (2Bn)									
2Bh					Р	ASET (Pa	age Add	ress Set)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	0	1	1	2Bh
1 st Parameter	1	1	1	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
2 nd Parameter	1	1	1	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	140101
3 rd Parameter	1	1	1	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1
4 th Parameter	1	1	1	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	
Description	other of	driver st	atus. Th	to define area of e values of SP [ne in the Frame M SP[1!	[15:0] all lemory.	nd EP [1						_	
Restriction	Note 1	: When	SP [15:0	be equal to or less] or EP [15:0] is g			n (When	MADCTL's	s B5 = 0)	or 00EFh	(When M	ADCTL's	B5 = 1),
						Status			Availab				
Register								Sleep Out					
· ·								Sleep Out					
Availability								Sleep Out	Yes				
				Partial	ivioue O	n, idie ivid Sleep Ir		Sleep Out	Yes				
						Sieep II	1		1 68	•			
				_									
				Status	00.	45.01.000		Default Va					
Default			Po	wer On Sequence SW Reset		15:0]=000 15:0]=000	ooh If I	P [15:0]=01 MADCTL's MADCTL's	B5 = 0: E				
				HW Reset	SPI	15:0]=000		P [15:0]=01		[10.0]-	- UOL1 11		









8.2.22. Memory Write (2Ch)

2Ch			ite (2				RAMW	/R (Mem	orv	Write)					
	D/CX	RDX	WRX	D1	7-8	D7	D6	Ì	-	D4	D3	D2	D1	D0	HEX
Command	0	1	VV □ ∧		<u>7-о</u> Х	0	0	1	,	0	1	1	0	0	2Ch
1 st Parameter	1	1	<u></u>	^					D1	[17:0]	•	<u> </u>			XX
:	1	1	<u> </u>							[17:0]					XX
N th Parameter	1	1	1							[17:0]					XX
	This co	ommano	d is used	to trans	sfer data	from MC	U to fr	rame me	mory	y. This co	mmand r	nakes no	change to	o the othe	er drive
	etatue	When	thic com	mand is	accent	ed the c	olumn	rogietor	and	the page	register	are recei	t to the S	tart Colur	nn/Starl
					•			_			_				
Description	Page p	ositions	s. The St	art Colu	mn/Star	t Page po	sitions	are diffe	rent	in accord	dance with	n MADCT	L setting.) Then D	[17:0] is
	stored	in frame	e memor	y and the	e columi	n register	and th	e page r	egist	ter increm	ented. S	ending ar	y other co	mmand o	can stop
	frame '	Write. X	. = Don't	care.											
Restriction	In all c	olor mo	des, ther	e is no r	estrictio	n on leng	th of pa	arameter	s.						
				-			Stat	tus			Availab	ility			
					Norma	ıl Mode O			ff. SI	leen Out	Yes				
Register						al Mode O					Yes				
Availability						l Mode O					Yes				
, , , , , , , , , , , , , , , , , , , ,						l Mode O					Yes	i			
							Sleep	p In			Yes				
					5	Status			D	efault Va	lue				
Default						On Seque	nce			memory is					
				_		V Reset				memory					
				L	HV	V Reset		Conten	is of	memory	is not cle	ared			
								_	<u> </u>						
				С	ASET (2	2Ah)				lf					
										Needed					
				st Param nd Param							Г			:	
		/	3	rd Paran	neter: E0	C[15:8]					-	Leg	end	-	
			4	th Parme	eter EC[.	7:0]						Com	mand] ¦	
											į L	Com		J 	
				Р	ASET (2	Bh)					<u> </u>	Parai	meter	/ i	
					V						-	Disp	olay) [
			/ 1	st Param	neter: SF	P[15:8]		7				Act	tion		
Flow Chart		/	/ 2	nd Parar	meter: S	P[7:0]					`	ACI		1	
Flow Chart				rd Paran th Paran							. (Mo	ode)	
								_						į	
								_			1 (Sequentia	al transfer	\geq :	
				R	AMWR(2	2Ch)				If				;	
					\bigvee					Needed					
					mage Da ,D2[17:0	ata]Dn[17:0)							
						\leq]								
				Ar	ny Comm	nend									





8.2.23. Color Set (2Dh)

2Dh		•				RGBSE	T (Color :	Set)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	1	0	1	2Dh
1 st Parameter	1	1	1	XX	0	0		•	R00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Rnn	[5:0]			XX
32 nd Parameter	1	1	1	XX	0	0			R31	[5:0]			XX
33 rd Parameter	1	1	1	XX	0	0			G00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Gnn	[5:0]			XX
96 th Parameter	1	1	1	XX	0	0			G64	[5:0]			XX
97 th Parameter	1	1	1	XX	0	0			B00	[5:0]			XX
n th Parameter	1	1	1	XX	0	0			Bnn	[5:0]			XX
128 th Parameter	1	1	1	XX	0	0			B31	[5:0]			XX
Description	128 by	tes mus ommand	t be writt has no e	to define the LU en to the LUT re effect on other o mory is written t	egardless command	of the co	lor mode.	Only the	values in				s effect
Restriction													
						Status			Availab	lity			
				Norma	Mode O	n, Idle Mo	de Off SI	een Out	Yes	iity			
Register						n, Idle Mo		•	Yes				
Availability						n, Idle Mo			Yes				
Availability						n, Idle Mo			Yes				
						Sleep In		Jop Gut	Yes				
Default				Pov	Status ver On Se SW Res HW Res	equence	Ra Contents	efault Val ndom val s of LUT ndom val	ues orotected				
Flow Chart				RGBSE* 1st Paramete: 32nd Parame 33rd Parame : 96th Parame 97th Parame : 128th Parame	er: R00[5: ter: R31[5 ter: G00[5 ter: G63[5 ter: B00[5	5:0] 5:0] 5:0] 5:0]			Comm Param Displ Actic	eter / ay / on / de	7		

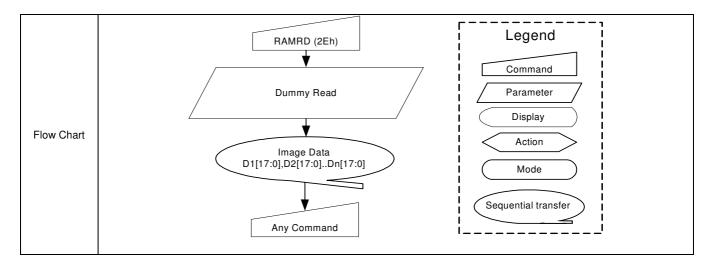




8.2.24. Memory Read (2Eh)

8.2.24. I	Memo	ry Ke	aa (2	En)									
2Eh						RAMRD	(Memory	Read)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	0	1	1	1	0	2Eh
1 st Parameter	1	1	1	XX	X	Χ	X	X	X	X	X	X	Х
2 nd Parameter	1	1	1				D.	1 [17:0]					XX
:th	1	1	1				D	k [17:0]					XX
(N+1) th Parameter	1	1	1				Dr	า [17:0]					XX
	This co	ommano	transfe	rs image data	from ILI9	341's fra	me memo	ry to the	host prod	cessor sta	irting at t	he pixel l	ocation
	specifie	ed by pr	eceding	set_column_ac	ldress and	set_pag	e_address	comman	ds.				
	If Mem	ory Acc	ess conti	rol B5 = 0:									
			. •	registers are re			, ,		• ,		•		
			•	SP). The colu								•	
		_	-	the End Colu				-					
	ıncrem	ented. F	rixels are	e read from the	e frame me	emory ur	itil the pag	e register	equals th	ne End Pa	age (EP) v	/alue or t	ne host
Description	proces	sor send	ds anoth	er command.									
	If Mem	ory Acc	ess Cont	rol B5 = 1:									
	The co	lumn ar	ıd page ı	registers are re	set to the	Start Co	umn (SC)	and Start	Page (SF), respect	ively. Pixe	els are rea	ad from
	frame	memory	at (SC,	SP). The page	register is	s then in	cremented	and pixel	s read fro	m the fra	me memo	ry until th	ie page
	registe	r equals	the End	d Page (EP) va	alue. The p	oage reg	ister is the	n reset to	SP and	the colum	ın register	r is increr	nented.
	Pixels	are reac	d from th	e frame memo	ry until the	column	register ed	quals the I	End Colur	mn (EC) v	alue or th	e host pro	ocessor
	sends	another	commar	nd.									
Restriction	There	s no res	striction o	on length of par	ameters.								
						Status			Availab	ility			
Dogister				Norm	al Mode O	n, Idle M	ode Off, SI	eep Out	Yes				
Register						•	ode On, SI	•	Yes				
Availability							ode Off, Sle		Yes				
				Partia	al Mode Oi		ode On, Sle	eep Out	Yes				
						Sleep I	n		Yes				
					Status			Default Va	lue				
Default				Power	On Seque	ence C	ontents of			omly			
Deiauit				S	W Reset	С	ontents of	memory is	s set rand	omly			
				Н	IW Reset	С	ontents of	memory is	s set rand	omly			









8.2.25. F	Partia	l Area	a (30h)									
30h						PLTAR	(Partial	Area)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	0	1	1	0	0	0	0	30h
1 st Parameter	1	1	1	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2 nd Parameter	1	1	1	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3 rd Parameter	1	1	1	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4 th Parameter	1	1	1 - 6	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	3F
				the partial mod	•			-					
	defines	the Sta	art Row (SR) and the se	cond the	End Row	(ER), as	illustrate	d in the f	igures be	low. SR a	and ER re	fer to the
	Frame	Memory	Line Po	inter.									
	If End	Row>Sta	art Row v	when MADCTL	B4=0:-								
			1	Start Row SR[15:0] End Row ER[15:0]							Partial Area		
	If End	Row>Sta	art Row v	when MADCTL	B4=1:-								
				End Row _									
				ER[15:0] →						‡ <			
Description			Ş	Start Row - SR[15:0] -						}	Partial Area		
	If End	Row <st< th=""><th>art Row v</th><th>when MADCTL</th><th>B4=0:-</th><th></th><th></th><th></th><th></th><th>_</th><th></th><th></th><th></th></st<>	art Row v	when MADCTL	B4=0:-					_			
				End Row = ER[15:0] -> -						}	Partial Area		
				Start Row - SR[15:0] ->- - - -						}	Partial Area		
	If End	Row = S	tart Row	then the Partia	l Area wil	l be one r	ow deep.						
	X = Do	n't care.											
Restriction	SR [15	0] and	ER [15	0] cannot be	0000h noi	exceed	013Fh.						





Normal Mode On, Idle Mode Off, Sleep Out		
Normal Mode On, Idle Mode Off, Sleep Out		Status Availability
Normal Mode On, Idle Mode On, Sleep Out		
Partial Mode On, Idle Mode Off, Sleep Out Yes	Register	
Partial Mode On, Idle Mode On, Sleep Out Yes		
Sleep in	Availability	
Default Value SR 15:0 ER 15:0		
Default		Gicep III 103
PLTAR(30h) Legend Ist Parameter: SR[15:8] 2nd Parameter SR[7:0] Parameter Display Action Mode Partial Mode 2. To Leave Partial Mode Partial Mode Partial Mode Partial Mode Legend Command Parameter Display Action Mode Partial Mode Partial Mode Sequential transfer Display Action NORON(13h) Parameter Display Action Mode Sequential transfer Display Action Mode Sequential transfer	Default	Status SR [15:0] ER [15:0] Power On Sequence 16'h0000h 16'h013Fh SW Reset 16'h 0000h 16'h 013Fh
PLTAR(30h) Legend Ist Parameter: SR[15.8] 2nd Parameter SR[7.0] Parameter Display Action Mode Partial Mode 2. To Leave Partial Mode Partial Mode Partial Mode Partial Mode Partial Mode Legend Command Parameter Display Action NORON(13h) Parameter Display Action Mode Parameter Display Action Mode RAMPW(2Ch) Sequential transfer Sequential transfer		1. To Enter Portial Made
DISPOFF (28h) Command Parameter NORON(13h) Display Action Mode RAMRW(2Ch) Sequential transfer		PLTAR(30h) 1st Parameter: SR[15:8] 2nd Parameter: SR[7:0] Parameter Parameter: ER[15:8] 4th Parameter: ER[7:0] Partial Mode Legend Display Action Mode PTLON(12h) Sequential transfer
	Flow Chart	DISPOFF(28h) Command Parameter Display Partial Mode OFF Mode RAMRW(2Ch) Sequential transfer





8.2.26. Vertical Scrolling Definition (33h)

33h					VSCRDE	F (Vertic	al Scrolli	ng Defini	tion)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h	
1 st Parameter	1	1	1	XX				TFA	[15:8]				00	
2 nd Parameter	1	1	1	XX	TFA [15:8] TFA [7:0]									
3 rd Parameter	1	↑	1	XX				VSA	[15:8]				01	
4 th Parameter	1	1	1	XX				VSA	[7:0]				40	
5 th Parameter	1	1	1	XX				BFA	[15:8]				00	
6 th Parameter	1	1	1	XX				BFA	[7:0]				00	

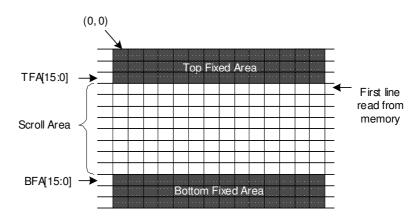
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.



Description

When MADCTL B4=1

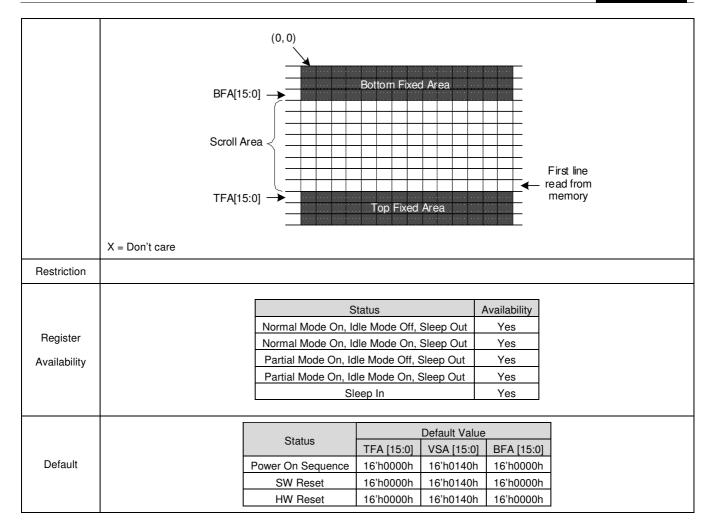
The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

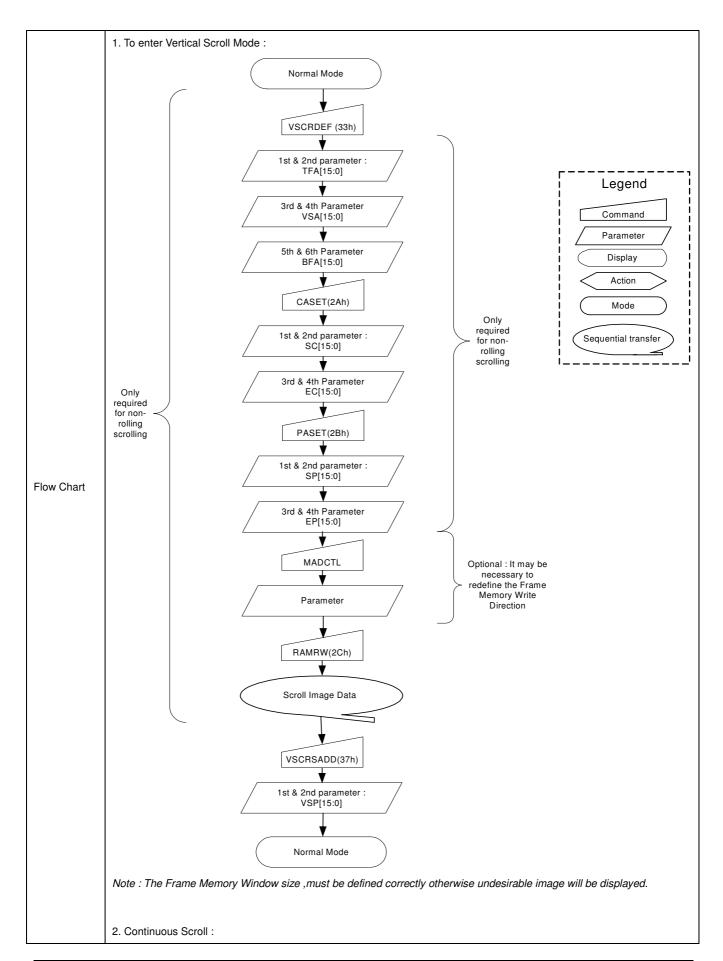
The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).





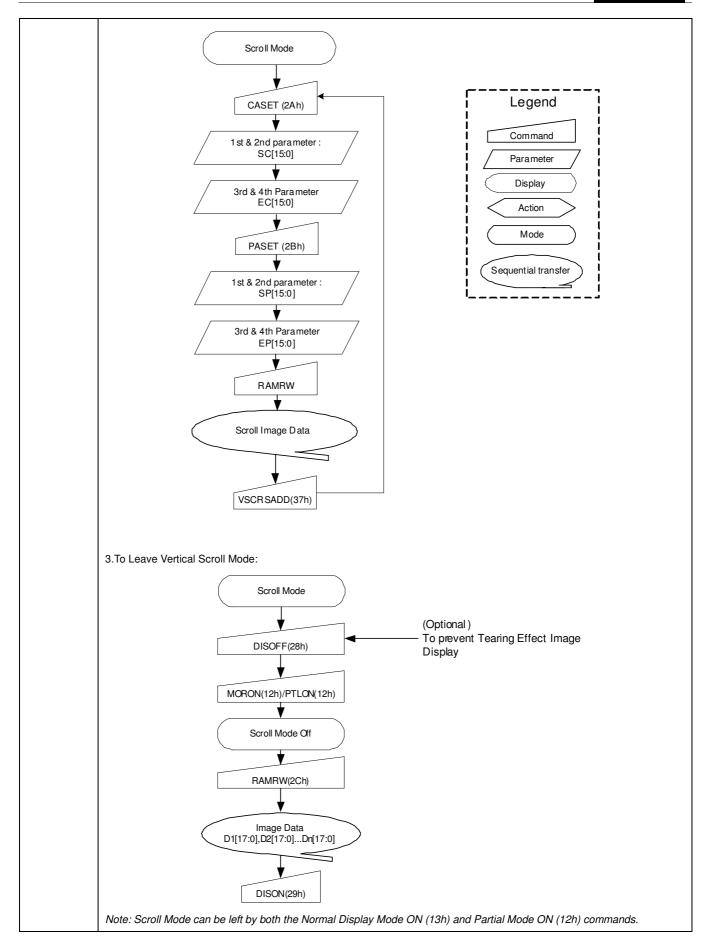
















8.2.27. Tearing Effect Line OFF (34h)

34h						TEOF	F (Tearin	g Effect	Line OFF	.)				
	D/CX	RDX	WRX	D17	7-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	X	X	0	0	1	1	0	1	0	0	34h
Parameter							No P	arameter						
Description		mmand n't care.		to turn OF	F (Activ	e Low) the	e Tearing	Effect out	tput signa	Il from the	TE signa	al line.		
Restriction	This co	mmand	has no e	effect whe	n Tearin	g Effect o	output is a	lready OF	F.					
Register Availability					Normal Partial	Mode On	Status n, Idle Moo n, Idle Moo n, Idle Moo n, Idle Moo Sleep In	de On, Sle le Off, Sle	eep Out	Availabil Yes Yes Yes Yes	ity			
Default						Power	Status On Seque W Reset W Reset		OFF OFF OFF	ue				
Flow Chart					TEOF	Output O F(34h) V Output OF			C Pa	egend ommand arameter Display Action Mode				

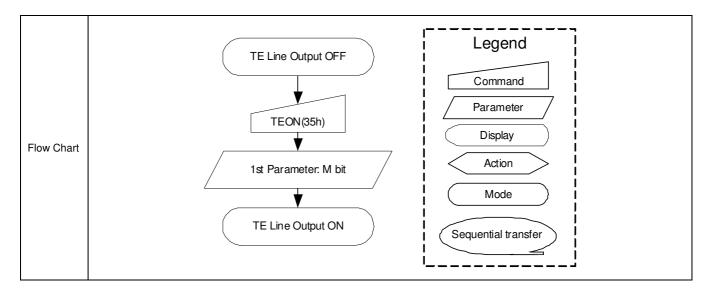




8.2.28. Tearing Effect Line ON (35h)

0.2.20.	100.	y -		Lille Old (33		NI /T: .	F.(1 ! 01"							
35h					TEO	N (Tearin	g Effect	Line ON)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	0	0	1	1	0	1	0	1	35h		
Parameter	1	1	1	XX	0	0	0	0	0	0	0	М	00		
	This co	ommand	l is used	to turn ON the T	earing Ef	fect outpu	ıt signal	from the	TE signal	line. Th	is output	is not aff	ected by		
	changi	ng MAD	CTL bit I	B4. The Tearing I	Effect Line	e On has	one par	ameter wh	ich descr	ibes the	mode of	the Teari	ng Effect		
	Output	Line.													
	Carpar														
	When I	M=0:													
	The Te	aring Ef	fect Outp	out line consists of	f V-Blanki	ng informa	ation only	y:							
					←	tv	dl		tvdh	>					
Description	Verti	ical Tir	ne Sca	le /	7				<i>f</i>	7					
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,					†				f	*					
	When I	M=1:													
	The Te	arina Ef	fact Outr	out Line consists o	of both V-F	Blanking a	nd H-RI	ankina info	rmation:						
	1116 16	ailig Li	ieci Ouiț	out Line consists t	n botti v-t	Jianking a	110 11-016	anking inic	illiation.						
		Vertical Time Scale													
		Vertical Time Scale													
	Verti	Vertical Time Scale													
	Note: Γ	Vertical Time Scale Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.													
		_		.ouo mur roumg		o o, . o	9 =	oor oarpar	p 2 .	, 400 -					
	X = D0	n't care.													
Restriction	This co	mmand	has no e	effect when Tearin	g Effect o	utput is a	ready O	N							
						Status			Availabi	ity					
Register						, Idle Mod			Yes						
						, Idle Mod , Idle Mod			Yes Yes						
Availability						, Idle Mod			Yes						
				- Tartiar	Wode On	Sleep In	0 011, 01	cop out	Yes						
				<u> </u>				J							
						Status		Default Val	ue						
Default						On Seque	nce	OFF							
						W Reset		OFF							
					н	W Reset		OFF							









8.2.29. Memory Access Control (36h)

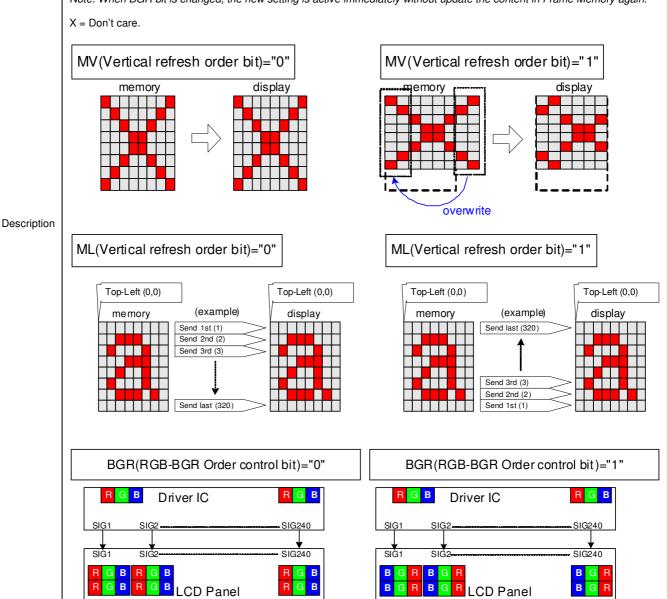
36h				MAI	DCTL (N	lemory /	Access (Control))				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	МН	0	0	00

This command defines read/write scanning direction of frame memory.

This command makes no change on the other driver status.

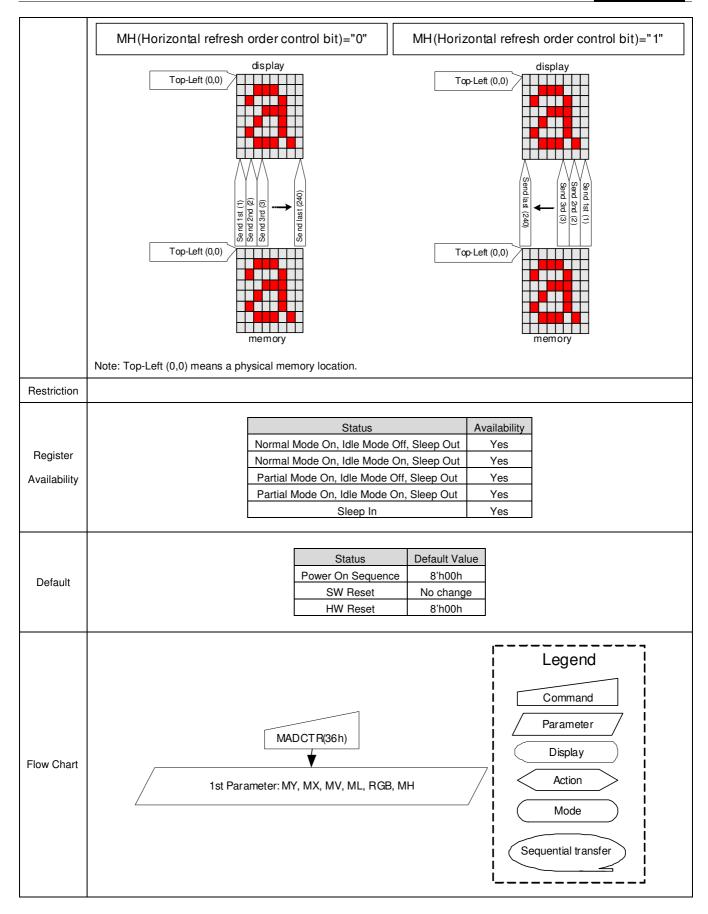
Bit	Name	Description
MY	Row Address Order	
MX	Column Address Order	These 3 bits control MCU to memory write/read direction.
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control
ban	NGB-BGN Older	(0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.













8.2.30. Vertical Scrolling Start Address (37h)

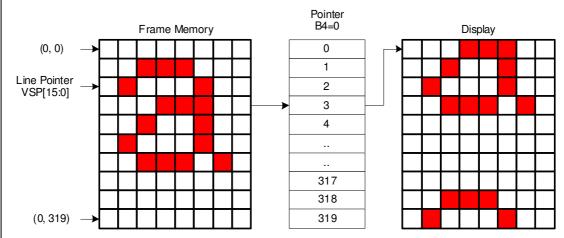
37h				VS	CRSADI) (Vertica	l Scrollin	g Start A	ddress)						
	D/CX	RDX													
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h		
1 st Parameter	1	↑	1	XX				VSP	[15:8]				00		
2 nd Parameter	1	1	1	XX	VSP [7:0] 00										

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-

When MADCTL B4=0

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.

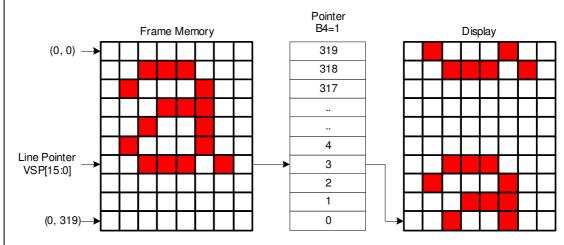


Description

When MADCTL B4=1

Example:

When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.



Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan

to avoid tearing effect. VSP refers to the Frame Memory line Pointer.

(2) This command is ignored when the ILI9341 enters Partial mode.

X = Don't care





Restriction					
			Status		Availability
		Norm	al Mode On, Idle Mode (Off, Sleep Out	Yes
Register		Norm	al Mode On, Idle Mode (On, Sleep Out	Yes
Availability		Partia	al Mode On, Idle Mode C	Off, Sleep Out	No
		Partia	al Mode On, Idle Mode C	n, Sleep Out	No
			Sleep In		Yes
			Status	Default Val	ue
			Status	VSP [15:0)]
Default			Power On Sequence	16'h0000l	ı
			SW Reset	16'h0000l	1
			HW Reset	16'h0000l	า
Flow Chart	See Vertical Scrolling Definition	(33h)	description.		





8.2.31. Idle Mode OFF (38h)

38h					IDM	OFF (Idle	Mode Ol	FF)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	0	0	1	1	1	0	0	0	38h		
Parameter						No Para	meter								
	This con	nmand is ι	used to rec	over from Idle	e mode o	n.									
Description			e, LCD car	ı display max	imum 262	2,144 colo	rs.								
	X = Don	't care.													
Restriction	This con	nmand has	s no effect	when module	e is alread	ly in idle o	ff mode.								
						Status			Availabilit	ty					
Register				Normal M					Yes						
				Normal M					Yes						
Availability						dle Mode (Yes						
		Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes													
Default				F	Power On SW F	itus Sequence Reset Reset	ldle m	ult Value node OF node OF node OF	F F						
Flow Chart				Idle mod	(38h)			Cool Part Di A	egend mmand rameter sisplay action Mode						



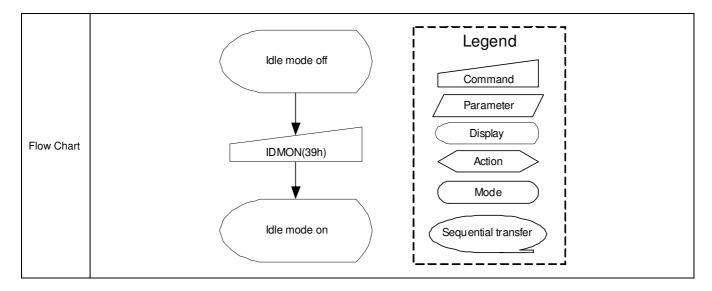


8.2.32. Idle Mode ON (39h)

39h	IDMON (Idle Mode ON)													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h	
Parameter	_				- 1	No	Paramet	er			-	1		
	This co	mmand	is used t	o enter into Idl	e mode on									
	In the i	dlo on n	anda nak	or expression is	roducod	The prim	any and th	no cocond	ary color	s ucina MS	P of oach	D G and	N R in the	
				•		me piim	ary and ti	ie second	ary colors	s using ivid	ob oi eaci	in, G and	יוו ט ג	
	Frame	Memory	, 8 color	depth data is c	lisplayed.									
				Memory					F	anel Di	splav			
] [
						_								
						_								
						_								
								_						
								\rangle $-$						
Description		-				<u> </u>	V							
Description						_								
		_				_						-		
						_								
					NA			2'			_			
		Memory Contents vs. Display Color R ₅ R ₄ R ₃ R ₂ R ₁ R ₀ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀ RICAL AND AND AND AND AND AND AND AND AND AND												
	Black 0XXXXX 0XXXXX 0XXXXX													
	Blue 0XXXXX 0XXXXX 1XXXXX Red 1XXXXX 0XXXXX 0XXXXX													
				Magenta	1XXX	XX	0X	XXXX	12	XXXXX				
				Green	0XXX	XX	1X	XXXX	0.	XXXXX				
				Cyan Yellow	0XXX 1XXX			XXXX		XXXXX				
				White	1XXX			XXXX		XXXXX				
	X = Do	n't care.												
Restriction	This co	mmand	has no e	ffect when mo	dule is alre	adv in idl	e off mod	e						
1100111011011	11110 00		1140 110 0			ady iii idi								
						Status	2		Availal	hility				
				Norn	nal Mode C			Sleep Out	Yes					
Register					nal Mode C	,	,		Ye					
Availability					ial Mode C				Ye					
					ial Mode C				Ye					
						Sleep	ln		Ye	S				
						Ctatus		Dofordt \/-	luo					
					Power	Status r On Sequ		Default Va dle mode (
Default						SW Rese		dle mode (
						HW Rese		dle mode (
	<u></u>								'					











8.2.33. COLMOD: Pixel Format Set (3Ah)

0.2.33.	PIXSET (Pixel Format Set)																
3Ah							PIX	SET (Pix	kel Fo	rmat	Set)						
	D/CX	RDX	WRX		D17	'-8	D7	D6	D5		D4	С)3	D2	D1	D0	HEX
Command	0	1	1		XX	<	0	0	1		1		1	0	1	0	3Ah
Parameter	1	1	1		XX		0		DPI				0		DBI [2:0		66
	This cor	mmand s	ets the p	oixel	format	t for the	RGB ima	age data	used	by th	e inte	erface. D)PI [2	:0] is the	pixel for	mat select	of RGB
	interface	e and DE	3I [2:0] is	the	pixel f	ormat c	of MCU int	terface. I	f a pa	ticul	ar inte	erface, e	either	RGB int	erface or	MCU inte	rface, is
	not use	d then the	e corres	oon	ding bit	s in the	paramete	er are igr	nored.	The	pixel	format i	s sho	wn in the	e table be	elow.	
				DPI	[2:0]	RGB	Interface	Format		DBI [2:01	MCU	Interf	ace Forr	nat		
			(0 0		Reserved		0					erved			
			() (0 1		Reserved	d	0	0	1		Rese	erved			
Description			()	1 0		Reserved	d	0	1	0		Reserved				
			(1 1		Reserved		0	_	1			erved			
					0 0 0 1	4	Reserved 6 bits / pix		1			1	Reserved 16 bits / pixel				
			-	_	1 0		8 bits / pi		1		0			/ pixel			
			1		1 1		Reserved		1		1			erved			
	If using	RGB Inte	erface m	ust :	selection	on seria	l interface	€.									
	X = Dor	z = Don't care															
Restriction																	
							Ç	Status				Av	/ailab	ility			
Register							lode On, I						Yes				
							lode On, I ode On, Id						Yes Yes				
Availability							ode On, Id						Yes				
								leep In	,				Yes				
					C.	tatua					Defa	ult Valu	е				
					31	tatus		DPI [2:0] DBI [2:0]									
Default			Po	wer		quence	9	3'b110 3'b110									
						Reset		Γ	No Ch 3'b1					Change 'b110			
					1100	ricaci		1	0.01	10				D110			
					_						L – .	– – – Le	- – - egei	 nd	₁		
						COLI	MOD (3Ah)			 				ļ		
								<u></u>			i I	Co	mma	nd	l I		
							\downarrow				i /	Pa	rame	ter /	' 		
							V			7	i -	D	isplay		l I		
Flow Chart			,				GB pixel for CU				i I		Action		l l		
			\angle				-		_/		i I		ACTION		i i		
							\downarrow				 		Mode		ļ		
					_						 /	0			. !		
					L	Any	Command	ı			۱ (Sequer	ıtıai tr	anster)		
											' – –				'		
	<u> </u>																





8.2.34. Write Memory Continue (3Ch)

3Ch					Write_	Memory	_Contin	iue					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
1 st Parameter	1	4		D1	D1	D1	D1	D1	D1	D1	D1	D1	000
		1	Ţ	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF
X th Parameter	4	4		Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	000
X Parameter	Į	Į	T	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF
N th Parameter	1			Dn	Dn	Dn	Dn	Dn	Dn	Dn	Dn	Dn	000
N Parameter		1	Î	[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF

This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.

If set_address_mode B5 = 0:

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

If set_address_mode B5 = 1:

Description

Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.

Sending any other command can stop frame Write.

Frame Memory Access and Interface setting (B3h), WEMODE=0

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

Frame Memory Access and Interface setting (B3h), WEMODE=1

When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

Restriction

A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.





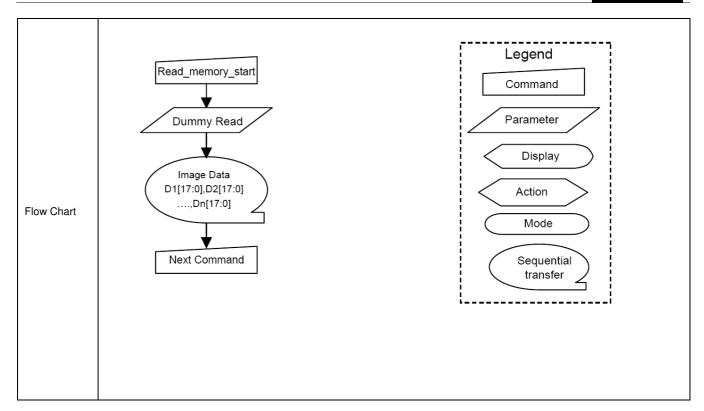
					 1
		Status		Availability	
		Normal Mode On, Idle M		Yes	
Register	<u> </u>	Normal Mode On, Idle M	ode On, Sleep Out	Yes	
Availability	<u> </u>	Partial Mode On, Idle Mo	ode Off, Sleep Out	Yes	
	<u> </u>	Partial Mode On, Idle Mo	ode On, Sleep Out	Yes	
	S	Sleep In		No	
		Status	Default Val	ue	
Defect		Power On Sequence	Random va	lue	
Default		SW Reset	No chang	е	
		HW Reset	No chang	е	
Flow Chart	Image Data D1[17:0],D2[17,Dn[17:0] Next Comma	7:0]		Pa	egend ommand rameter Display Action Mode Sequential transfer





3Eh	Read_Me			. ,	Read	Memory	Contin	IIIE					
JEII	D/CX	RDX	WRX	D17-8	_	D6	_Contin	D4	Da	D2	D4	DO	HEX
Command			WHA.		D7				D3		D1	D0	
Command	0	1	1	XX	0	0	1	1	1	1	1	0	3Eh
1 st Parameter	1	<u> </u>	1	XX	X	X	X	X	X	X D1	X	X	X
2 nd Parameter	1	1	1	D1	D1	D1	D1	D1	D1	D1	D1	D1	000
				[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF
x st Parameter	1	↑	1	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	Dx	000
				[178]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	3FF
N st Parameter	1	↑	1	Dn [178]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF
Description	If set_addre Pixels are re read_memore column region incremented column region If set_addre Pixels are re read_memore register equ Pixels are re equals the If	ess_mode ead continue ester equals d. Pixels and ester equals ess_mode ead continue ead continue ead from the EP value, continue and makes	orevious reads and the state of the End Core read from the EC value of the EC value of the EC value of the EC value of the EC value of the EC value of the the EC value of the the the the the the the the the the	ata from the cad_memory_cad_memory_cad_memory_cad_memory_cad_memory_cad_memory expenses and the pixel location of the pixel location	on after the street on after the page regular excellent another the column and another state of the column another state of the column and another state of the column and another state of the column and another state of the column and another state of the column and another state of the column another state of the column and another state of the column and another state of the column and another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of the column another state of th	the read crement e column ntil the passor sen the read emented ister is the register comment of the comment of	range of ed and p n registe age regi ds anoth range of and pixe nen rese r equals nand.	emory_interpretation the pre-	vious readeread from and the column	d_mem m the fr SC and ind Page d_mem the fran olumn r (EC) va	ory_star rame me the page e (EP) va ory_star ne meme egister is	t or mory uni e registe alue and t or ory until t s increme	til the r is the the pag ented.
Restriction	_	•-		h read_mem	_		_, -	_					
					Stat	tus			Availabilit	ty			
			1	Normal Mode			ff, Sleep		Yes				
Register				Normal Mode					Yes				
Availability				Partial Mode					Yes				
•				Partial Mode					Yes				
				Sleep In	,		, F		Yes				
				•									
										_			
				Stat	us		Defa	ult Value	e				
				Danier On C			D						
D - (!)				Power On S	<u>seq</u> uenc	е	Ranc	lom data	<u>1</u>				
Default				SW Reset	sequence	е		iom data change	1	1			









8.2.36. Set_Tear_Scanline (44h)

0.2.30. S	et_rear_			-,	Set	Tear S	Scanline						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	0	0	1	0	0	44h
1 st Parameter	1	1	1	XX	0	0	0	0	0	0	0	STS [8]	00
2 nd Parameter	1	1	1	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00
Description	The TE sign describes the Vertical T	nal is not a ne Tearing ime Scal	e	ay Tearing Etchanging set_	_address	_mode b	tvo	ne Tearii				e parame	
				STS=0 is equ					ı Sleep m	node.			
Restriction	-												
Register Availability			1	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In	On, Idle On, Idle	Mode C Mode C	n, Sleep	Out Out Out	Availabili Yes Yes Yes Yes Yes Yes	ity			
Default				Power On S SW Reset HW Reset		e	STS [8	ult Value 3:0]=000 3:0]=000 3:0]=000	0h 0h				
Flow Chart	TE Output On or Off Set_tear_scanline Parameter Send 1st parameter STS[8] Display Action Mode TE Output On the Nth line Sequential transfer												





8.2.37. Get_Scanline (45h)

45h		•	-			Get_Sca	ınline							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	0	1	0	0	0	1	0	1	45h	
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	X	Х	X	Х	Х	
2 nd Parameter	1	<u>†</u>	1	XX	0	0	0	0	0	0	GTS [9]	GTS [8]	00	
3 rd Parameter	1	1	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00	
Description	display devi	ice is defin	ed as VSYI	can line, GTS NC + VBP + \ eturned by ge	VACT + '	VFP. The	e first sc	-						
Restriction	None													
					Sta	tus			Availabili	itv				
				Normal Mode			Off. Sleer							
Register				Normal Mode					Yes					
Availability				Partial Mode					Yes					
				Partial Mode					Yes					
				Sleep In					Yes					
Default				Power On S SW Reset HW Reset		e	GTS [9	ult Value [S [9:0] [9:0]=000 [9:0]=000 [9:0]=000	0h 0h					
Flow Chart			Send 1	get_scanline Wait 3us Dummy Read st parameter GT	\$[9:8]	··			Pa	egend ommand orameter Display Action Mode Sequentia transfer				





8.2.38. Write Display Brightness (51h)

51h		WRDISBV (Write Display Brightness) D/CX RDX WRX D17-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX				
Command	0	1	1	XX	0	1	0	1	0	0	0	1	51h				
Parameter	1	1	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00				
Description	It should	be chec	ked what	is the rel	brightness ationship b ecification. value mean	etween thi	s written v	alue and o					ionship				
Restriction	None																
						Stat	us		Availab	oility							
				N	ormal Mod			Sleep Out									
Register				Ν	ormal Mod	e On, Idle	Mode On,	Sleep Out	t Yes	3							
Availability				F	artial Mode	On, Idle	Mode Off,	Sleep Out	Yes	3							
	Partial Mode On, Idle Mode On, Sleep Out Yes																
		Sleep In Yes															
Default					State Power On SW R	Sequence leset		Default V DBV [7 8'h00l 8'h00l	:0] า า								
Flow Chart					WRDISB DBV[70	lay		¥	Leger Comm Parame Displ Actio Mod Seque: trans	and ter ay on le ntial							





8.2.39. Read Display Brightness (52h)

52h					RDD	ISBV (Rea	ad Display	/ Brightne	ss Value)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	<u> </u>	XX	0	1	0	1	0	0	1	0	52h
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	Χ
2 nd Parameter	1	1	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00
Description	It shou	ld be ch	ecked w	hat the re	tness valu elationship splay modu at 00h valu	between t	his returne		•			olay. This hest bright	ness.
Restriction				_	e nd parame BI Mode.	ter value c	n the data	lines if the	e MCU wai	nts to read	l more thai	n one para	meter
			-		SI (The 1s	t paramete	er is not se	nt).					
						St	atus		Avail	ability			
					Normal Mo	de On, Idl	e Mode O	ff, Sleep C	out Yo	es			
Register					Normal Mo					es			
Availability					Partial Mo					es			
					Partial Mo	de On, Idle	e Mode Or	ı, Sleep O		es			
					Sleep In				Y	es			
Default	Status Default V DBV [7 Power On Sequence 8'h00l SW Reset 8'h00l HW Reset 8'h00l								[7:0] 0h 0h				
Flow Chart					Send	1 RDDISB 1 st Parame 1 price	Dis	Host play	Para D A See	egend mmand ameter isplay action Mode quential ansfer			



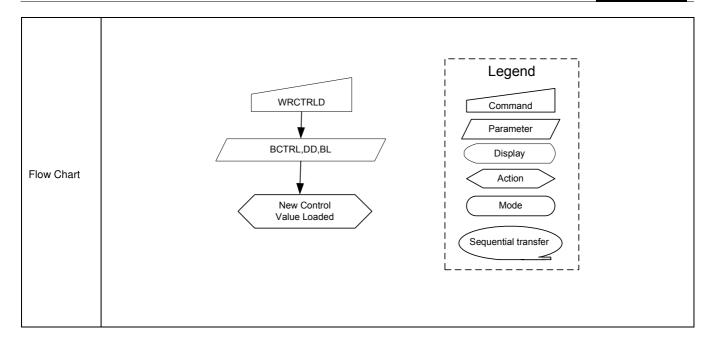


8.2.40. Write CTRL Display (53h)

53h				WR	CTRLD	(Write	Control D	isplay)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	0	1	0	1	0	0	1	1	53h		
Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00		
	This command is used to control display brightness.														
	BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.														
		0 = Off (Brightness registers are 00h, DBV[70])													
	0 = 01	f (Brightne	ss registers	are oon, DB	V[70])										
	1 = Or	n (Brightne	ss registers	are active, a	ccordin	g to the	other parar	meters.)							
	DD: Display	/ Dimming,	only for ma	anual brightne	ess setti	ng									
	DD = 0	0: Display	Dimming is	off											
	DD =	1: Display l	Dimming is	on											
		Biopiay	Dimming to	011											
Description	51 5 11		0 10"												
	BL: Backlig	nt Control	On/Off												
	0 = Of	f (Complet	ely turn off l	oacklight circu	uit. Con	trol lines	s must be lo	ow.)							
	1 = Or	1													
	Dimming fu	nction is a	danted to th	e brightness	register	s for dis	nlav when	bit BCT	RI is ch	anged a	t DD=1	ea BC	TDI . 0 . N		
			aaptoa to ti.		. 09.0.0.								IBI:U 🔿		
	4 - 4 > 0						17			angea a		9	IRL: U J		
	1 or 1→ 0.									ungou u	(55-1,	9	IRL: U J		
	1 or 1→ 0.						, -9			agou a	, ,		IKL: U J		
		it change f	rom "On" to	"Off", backlig	ht is tur										
	When BL bi	it change f	rom "On" to	"Off", backlig	ht is tur										
		it change f	rom "On" to	"Off", backlig	ht is tur										
	When BL bi	it change f	rom "On" to	"Off", backlig	ht is tur										
Restriction	When BL bi	it change f	rom "On" to	"Off", backlig	ht is tur										
Restriction	When BL bi	it change f	rom "On" to	"Off", backlig		ned off		dual din	nming, e	ven if di					
Restriction	When BL bi	it change f			Sta	ned off	without gra	dual din	nming, e	ven if di					
Restriction Register	When BL bi	it change f		"Off", backlig	Sta On, Idle	ned off	without gra	dual din	nming, e	ven if di					
	When BL bi	it change f	1	Normal Mode	Sta On, Idle On, Idle	ned off	without gra	dual din	nming, e vailabilit Yes	ven if di					
Register	When BL bi	it change f	1	Normal Mode Normal Mode	Sta On, Idle On, Idle	ned off atus a Mode Mode Mode	without gra Off, Sleep On, Sleep Off, Sleep ()	A Out Out Out	nming, e vailabilit Yes Yes	ven if di					
Register	When BL bi	it change f	1	Normal Mode Normal Mode Partial Mode	Sta On, Idle On, Idle	ned off atus a Mode Mode Mode	without gra Off, Sleep On, Sleep Off, Sleep ()	A Out Out Out	wailabilii Yes Yes Yes	ven if di					
Register	When BL bi	it change f	1	Normal Mode Normal Mode Partial Mode Partial Mode	Sta On, Idle On, Idle	ned off atus a Mode Mode Mode	without gra Off, Sleep On, Sleep Off, Sleep ()	A Out Out Out	vailabilii Yes Yes Yes Yes	ven if di					
Register	When BL bi	it change f	N	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In	Sta On, Idle On, Idle	ned off atus a Mode Mode Mode	Off, Sleep On, S	A Out Out Out	vailabilii Yes Yes Yes Yes	ven if di					
Register	When BL bi	it change f	N	Normal Mode Normal Mode Partial Mode Partial Mode	Sta On, Idle On, Idle On, Idle	ned off atus a Mode Mode Mode	Off, Sleep On, S	Out Out Out	vailabilit Yes Yes Yes Yes Yes	ven if di					
Register Availability	When BL bi	it change f	1	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In	Sta On, Idle On, Idle On, Idle	ned off	Off, Sleep On, S	dual din Out Out Out Out Out Out It Value	vailabilit Yes Yes Yes Yes Yes	ven if di					
Register	When BL bi	it change f	Power	Normal Mode Normal Mode Partial Mode Partial Mode Sleep In Status	Sta On, Idle On, Idle On, Idle	ned off atus Mode Mode Mode Mode Mode Mode Mode Mode	Off, Sleep On, Sleep Off, Sleep On, Sleep On, Sleep Defau Defau	dual din A Out Out Out Out Out Out Out Out Out Out	vailabilii Yes Yes Yes Yes Yes	ven if di					







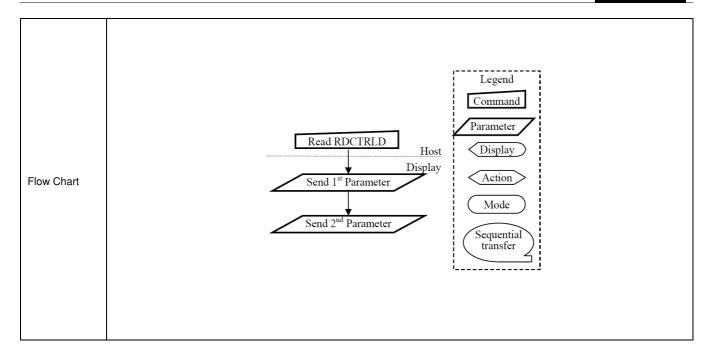




8.2.41. Read CTRL Display (54h)

54h	RDCTRLD (Read Control Display)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	<u> </u>	XX	0	1	0	1	0	1	0	0	54h
1 st Parameter	1	↑	1	XX	Χ	Х	Х	Χ	Х	Χ	Х	Χ	XX
2 nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00
	BCTRL : E	Brightness Off (Brightne	Control Blo	n brightness ock On/Off, rs are 00h) rs are active			e DBV[70] p	arameto	ers.)				
Description	'0' = D	DD: Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on											
				f backlight c	ircuit. C	ontrol lir	es must be lo	w.)					
Restriction	(= more th	nan 2 RDX	cycle) on I	DBI.			data lines if the	ne MCU	wants to	read m	nore tha	n one pa	arameter
Register Availability	Only 2nd parameter is sent on DSI (The 1st parameter is not sent). Status Availability Normal Mode On, Idle Mode Off, Sleep Out Yes Normal Mode On, Idle Mode On, Sleep Out Yes Partial Mode On, Idle Mode Off, Sleep Out Yes Partial Mode On, Idle Mode On, Sleep Out Yes Sleep In Yes												
Default				Status er On Seque SW Reset HW Reset	nce	BCTR 1'b0 1'b0 1'b0	Default L D 1'1 1'1 1'1	D 00 00	B 1'1 1'1 1'1	00			









8.2.42. Write Content Adaptive Brightness Control (55h)

55h				WRCABC (\	e Bright	ness C	control)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	0	1	0	1	55h
Parameter	1	1	1	XX	0	0	0	0	0	0	C [1]	C [0]	00
				parameters				•				•	ble
Description				CI	1:0]	Г	Default \	ا میراد/					
					000		Off						
					000	l lea		ce Imag	Δ				
					010	0301	Still Pic						
					011	N	Noving I						
					,			ago					
Restriction	None												
					9	Status			Ava	ilability			
			•	Normal Mod			e Off, S	leep Ou		Yes			
Register				Normal Mod	de On, I	dle Mod	e On, S	leep Ou	t '	Yes			
Availability				Partial Mod	le On, Id	dle Mode	e Off, SI	eep Out	,	Yes			
				Partial Mod	le On, Id	dle Mode	e On, SI	eep Out	,	Yes			
				Sleep In					,	Yes]		
Default				Power On	atus Sequel Reset Reset	nce		efault V C [1:0]=(C [1:0]=(C [1:0]=(00h 00h				
Flow Chart			,	WRC 1st parame New At Image	daptive		7			Leger Comm Parame Displ Action Mod Seque trans	ter lay on le ntial		





8.2.43. Read Content Adaptive Brightness Control (56h)

56h			•	RDCABC (F					ess Cor	ntrol)			
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	0	1	1	0	56h
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	Х	Х	Х	Х	XX
2 nd Parameter	1	<u>†</u>	1	XX	0	0	0	0	0	0	C [1]	C [0]	00
				the settings f	_			-	_			-	v .
Description				C	[1:0]	Г	Default \	/alue					
•					b00		Off						
					b01	User		ce Image	!				
					b10		Still Pic						
				2'	b11	N	loving I	mage					
Restriction	(= more th	nan 2 RDX	cycle) on	2nd paramet DBI. DSI (The 1st				es if the N	ICU wai	nts to re	ad more t	han one p	arameter
			L		St	atus			Availa	bility			
				Normal Mod					Ye	s			
Register			-	Normal Mod					Ye				
Availability				Partial Mode					Ye				
			-	Partial Mode	On, Idle	e Mode	On, Sle	ep Out	Ye				
			L	Sleep In					Ye	!S			
Default				Sta Power On SW F HW F	Sequen	се	C	efault Va (2 [1:0]=00 (2 [1:0]=00 (2 [1:0]=00)h)h				
Flow Chart				Read R Send 1 st I	Parame	eter	H Disp	ost lay	Par	egendomman ameter Display Action Mode	nd r		





8.2.44. Write CABC Minimum Brightness (5Eh)

5Eh				Backlight Control 1									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	0	1	0	1	1	1	1	0	5Eh
Parameter	1	1	1	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00
	This cor	nmand is	s used to	set the mir	nimum brig	htness va	ue of the	display for	CABC fur	nction.			
		•		J	•			ed to avoic		J			
			•				Ü	s to less t		minimur	m brightne	ss setting	. Image
		ŭ			·	ŭ		nnot be ch	Ü				
Description							_	tness setti	•	•			
·	brightne	ss to les	s than CA	BC minim	um brightn	ess. Smo	oth transiti	on and din	nming fun	ction can	be worked	l as norma	al.
	When d	lisplay br	rightness	is turned	off (BCTR	L=0 of "V	/rite CTRI	L Display	(53h)"), C	ABC min	nimum brig	htness se	etting is
	ignored.												
	In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest												
	brightne	ss for CA	ABC.										
						Statu	S		Availab	ility			
				Nor	mal Mode	On, Idle M	lode Off, S	Sleep Out	Yes	i			
Register				Nor	mal Mode	On, Idle M	lode On, S	Sleep Out	Yes	i			
Availability					tial Mode	· ·			Yes				
					tial Mode	On, Idle M	ode On, S	Sleep Out	Yes				
		Sleep In Yes											
	Status Default Value CMB [7:0]												
Default				Power On Sequence 8'h00h									
					SW R	eset		No Chan	ge				
					HW R	leset		8'h00h	1				





8.2.45. Read CABC Minimum Brightness (5Fh)

Backlight Control 1													
D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
0	1	1	XX	0	1	0	1	1	1	1	1	5Fh	
1	1	1	XX	Х	Х	Χ	Χ	Χ	Х	Х	Х	Х	
1	↑	1	XX	CMB	CMB	CMB	CMB	CMB	CMB	CMB	CMB	00	
·	'		,,,,	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	00	
In princi													
					Status			Availab	oility				
			Norr	nal Mode	On, Idle M	ode Off, S	Sleep Out	Yes	3				
			Norr	nal Mode	On, Idle M	ode On, S	Sleep Out	Yes	3				
			Part	ial Mode (On, Idle M	ode Off, S	leep Out	Yes	3				
			Part	ial Mode (On, Idle M	ode On, S	leep Out	Yes	3				
			Slee	p In				Yes	3				
			F	Power On SW F	Sequence Reset		CMB [7: 8'h00h	:0] n nge					
	0 1 1 This cor In princi CMB[7:0	0 1 1 ↑ 1 ↑ This command re In principle the re CMB[7:0] is CAB	0 1 ↑ 1 1 ↑ 1 This command returns the In principle the relationship CMB[7:0] is CABC minim relationship is that 00h variationship is that 00h variationship.	0 1 ↑ XX 1 ↑ 1 XX 1 ↑ 1 XX This command returns the minimum In principle the relationship is that 00 CMB[7:0] is CABC minimum brighter relationship is that 00h value mean CABC. Norresident Norresident Part Silee	O 1 ↑ ↑ XX O 1 ↑ 1 XX X I ↑ 1 XX CMB [7] This command returns the minimum brightness In principle the relationship is that 00h value m CMB[7:0] is CABC minimum brightness spectorelationship is that 00h value means the low CABC. Normal Mode Partial Mode O Partial Mode O Sleep In Sta Power On SW F	D/CX RDX WRX D17-8 D7 D6 0 1 ↑ XX 0 1 1 ↑ 1 XX X X X 1 ↑ 1 XX X X X This command returns the minimum brightness value of In principle the relationship is that 00h value means the I CMB[7:0] is CABC minimum brightness specified with relationship is that 00h value means the lowest brightness. Status	D/CX RDX WRX D17-8 D7 D6 D5 0 1 ↑ XX 0 1 0 1 ↑ 1 XX X X X X 1 ↑ 1 XX CMB CMB CMB CMB [6] [5] This command returns the minimum brightness value of CABC fur In principle the relationship is that 00h value means the lowest brightness specified with "Write CA relationship is that 00h value means the lowest brightness for CABC. Status Normal Mode On, Idle Mode Off, SA Partial Mode On, Idle Mode On, SA Partial Mode On, Idle Mode On, SA Sleep In Status Power On Sequence SW Reset	D/CX RDX WRX D17-8 D7 D6 D5 D4 0 1 ↑ XX 0 1 0 1 1 ↑ 1 XX X X X X X 1 ↑ 1 XX CMB CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB [7] [6] [5] [4] This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness ar CMB[7:0] is CABC minimum brightness specified with "Write CABC minimal relationship is that 00h value means the lowest brightness for CABC and CABC. Status	D/CX RDX WRX D17-8 D7 D6 D5 D4 D3 0 1 ↑ XX 0 1 0 1 0 1 1 1 ↑ 1 XX X X X X X X X 1 ↑ 1 XX CMB CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX CMB CMB CMB CMB CMB 1 ↑ 1 XX X X X X X X X X X X X X X X X X	D/CX	D/CX RDX WRX D17-8 D7 D6 D5 D4 D3 D2 D1 0 1 ↑ XX 0 1 0 1 0 1 1 1 1 1 1 ↑ 1 XX X X X X X X X X X X X X X X X X	D/CX	





8.2.46. Read ID1 (DAh)

DAh						RDID1 (F	Read ID1)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	0	1	1	0	1	0	DAh
1 st Parameter	1	1	1	XX	Χ	X	Χ	Χ	Х	Χ	Χ	Х	Х
2 nd Parameter	1	1	1	XX				ID1	[7:0]				XX
Description	The 1 st pa	aramete aramete	r is dumı	he LCD module's r my data. I module's manufa			nd it is s	pecified	by User				
Restriction													
Register Availability				Normal Mo Normal Mo Partial Mo Partial Mo	de On, de On, de On, de On,	ldle Mode Idle Mode	On, Sle Off, Slee	ep Out ep Out	Availabi Yes Yes Yes Yes	lity			
Default			-	Status Power On Sequel SW Reset HW Reset		Before MT 8'h 8'h	00h 00h	am) (A		program alue alue)		
Flow Chart	HW Reset 8'h00h MTP value Let RDID1(DAh) Host Driver Dis 1st Parameter: Dummy Read 2nd Parameter: Send ID1[7:0]											Legend Command Carameter Display Action Mode	





8.2.47. Read ID2 (DBh)

DBh						RDID2	(Read ID	2)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1 st Parameter	1	1	1	XX	Χ	X	Х	Х	Х	Х	Х	Χ	Х
2 nd Parameter	1	↑	1	XX	1				ID2 [6:0]				XX
Description	changes The 1 st pa	each tim aramete aramete can be p	ne a revis r is dumr er is LCD	erack the LCD m sion is made to t my data. module/driver v ned by MTP fund	he displa	ay, materia	al or const	ruction	specificatio	ons.		greement) and
Restriction													
Register Availability				Normal Partial	Mode O Mode O	Status n, Idle Mo n, Idle Mo n, Idle Moo n, Idle Moo Sleep In	de On, Sl de Off, Sle	eep Out	t Yes Yes	ility			
Default				Status Power On Sec SW Rese	et .	(Before N	ault Value MTP progr 6'h80h 6'h80h		Default (After MTP MTP v MTP v	program) ralue ralue			
Flow Chart						ummy Read					Pa D	egend mmand rameter isplay Action Mode	





8.2.48. Read ID3 (DCh)

DCh	RDID3 (Read ID3)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	0	1	1	1	0	0	DCh
1 st Parameter	1	1	1	XX	Х	Χ	Χ	Х	Х	Χ	Х	X	Х
2 nd Parameter	1	1	1	XX				ID	3 [7:0]				XX
	This re	ad byte	identifies	the LCD modu	le/driver a	nd It is sp	ecified by	User.					
	The 1 st	parame	eter is dur	nmy data.									
Description	The 2 ⁿ	param	eter is LC	D module/drive	r ID.								
	The ID	3 can be	e program	nmed by MTP fu	unction.								
	X = Do	n't care											
Restriction													
						Status			Availat	oility			
				Norm	al Mode (ode Off, S	Sleen O					
Register							ode On, S						
Availability							ode Off, S						
, wanabinty							ode On, S		1				
						Sleep l			Yes	5			
Default				Statu Power On S SW Re	equence		fault Value MTP pro 8'h00h 8'h00h		(After MTF MTP MTP	t Value P program) value value)		
				HW Re	eset		8'h00h		MIP	value			
Flow Chart					RDID3(Dummy Rea					P P	egend command arameter Display Action Mode	



8.3. Description of Level 2 Command

8.3.1. RGB Interface Signal Control (B0h)

B0h					IFMODE (Inte	erface M	ode Cor	ntrol)													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	XX	1	0	1	1	0	0	0	0	B0ł								
Parameter	1	1	1	xx	ByPass_MODE	RCM [1]	RCM [0]	0	VSPL	HSPL	DPL	EPL	40								
	Sets th	e operat	ion statı	us of the display	interface. The sett	ing beco	mes effe	ective as	soon as	the comn	nand is	received									
	EPL: D	E polari	ty ("0"= I	High enable for I	RGB interface, "1"=	Low en	able for	RGB inte	erface)												
	DPL: D	OTCLK	polarity	set ("0"= data fe	tched at the rising	time, "1"	'= data fe	etched at	the fallin	ng time)											
	HSPL:	HSYNC	polarity	("0"= Low level	sync clock, "1"= Hi	gh level	sync clo	ck)													
	VSPL:	VSPL: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock)																			
December	RCM [RCM [1:0]: RGB interface selection (refer to the RGB interface section).																			
Description																					
	ByPas	ByPass_MODE: Select display data path whether Memory or Direct to Shift register when RGB Interface is used.																			
		ByPass_MODE Display Data Path																			
				0	Di	rect to SI	hift Regis	ster (def	ault)												
				1			Memor	у													
Restriction	EXTC	should b	e high to	o enable this cor	nmand																
					Status																
	Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes																				
Register																					
_				Norma	Mode ON, Idle Me	ode ON,	Sleep O	UT	Yes Yes												
Register Availability				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo	ode ON, de OFF, ode ON,	Sleep O Sleep O	UT	Yes Yes Yes												
_				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo	ode ON, de OFF, ode ON,	Sleep O Sleep O	UT	Yes Yes												
-				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo	ode ON, de OFF, ode ON,	Sleep O Sleep O Sleep Ol	UT UT UT	Yes Yes Yes												
-				Norma Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	ode ON, de OFF, ode ON, N	Sleep O Sleep Ol Sleep Ol	UT UT UT Value	Yes Yes Yes Yes		- FDI										
Availability			Power	Norma Partial Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	ode ON, de OFF, ode ON, N	Sleep O Sleep Ol Sleep Ol Default [1:0] V	UT UT UT Value	Yes Yes Yes Yes HSPL	DPL 1'h0	EPL 1'h1										
_				Norma Partial Partial	Mode ON, Idle Mo Mode ON, Idle Mo Mode ON, Idle Mo Sleep I	ode ON, de OFF, ode ON, N	Sleep O Sleep Ol Sleep Ol Default [1:0] V	Value (SPL 1'b0	Yes Yes Yes Yes	DPL 1'b0 1'b0	EPL 1'b1 1'b1										





8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h		FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h
1 st Parameter	1	1	1	XX	0	0	0	0	0	0	DIVA	· [1:0]	00
2 nd Parameter	1	1	1	XX	0	0	0		F	RTNA [4:0]		1B

Formula to calculate frame frequency:

Frame Rate= $\frac{\text{fosc}}{\text{Clocks per line } \text{x Division ratio x (Lines + VBP + VFP)}}$

Sets the division ratio for internal clocks of Normal mode at MCU interface.

fosc: internal oscillator frequency
Clocks per line: RTNA setting
Division ratio: DIVA setting
Lines: total driving line number
VBP: back porch line number
VFP: front porch line number

	RT	NA [4:0]		Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

	RTI	NA [4:0]		Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

Description

DIVA [1:0]: division ratio for internal clocks when Normal mode.

DIVA	[1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNA [4:0]: RTNA[4:0] is used to set 1H (line) period of Normal mode at MCU interface.

	RTI	NA [4:0]		Clock per
					Line
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

	RT	NA [4:0]	Clock per Line	
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

	RTI	NA [4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Restriction	EXTC should be high to enable this command							
			Status			Availability		
		Normal Mode ON, Idle Mode OFF, Sleep OUT Yes						
Register		Normal Mode ON, Idle Mode ON, Sleep OUT Yes						
Availability		Par	tial Mode ON, Idle Mode	OFF, Sleep (TUC	Yes		
•		Pai	rtial Mode ON, Idle Mode	ON, Sleep C	DUT	Yes		
			Sleep IN			Yes		
			Status	Defau				
				DIVA [1:0]	RTN	A [4:0]		
Default		Power ON Sequence		2'b00	5'ł	n1Bh		
	SW Reset 2'b00 5'h1Bh							
		HW Reset 2'b00 5'h1Bh						





8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h		FRMCTR2 (Frame Rate Control (In Idle Mode / 8I colors))											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h
1 st Parameter	1	1	1	XX	0	0	0	0	0	0	DIVE	B [1:0]	00
2 nd Parameter	1	1	1 ↑ XX 0 0 0 RTNB [4:0] 1E									1B	

Formula to calculate frame frequency

Frame Rate= $\frac{\text{fosc}}{\text{Clocks per line } \text{x Division ratio x (Lines + VBP + VFP)}}$

Sets the division ratio for internal clocks of Idle mode at MCU interface.

fosc: internal oscillator frequency
Clocks per line: RTNB setting
Division ratio: DIVB setting
Lines: total driving line number
VBP: back porch line number
VFP: front porch line number

	RT	NB [4:0]	Frame Rate (Hz)	
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

	RTI	NB [4:0]	Frame Rate (Hz)	
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

Description

DIVB [1:0]: division ratio for internal clocks when Idle mode.

DIVE	[1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNB [4:0]: RTNB[4:0] is used to set 1H (line) period of Idle mode at MCU interface.

	RTI	NB [4:0]	Clock per Line	
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

	RTI	NB [4:0]	Clock per Line	
0	1	0	1	1	Setting prohibited
0	1	1	0	0	Setting prohibited
0	1	1	0	1	Setting prohibited
0	1	1	1	0	Setting prohibited
0	1	1	1	1	Setting prohibited
1	0	0	0	0	16 clocks
1	0	0	0	1	17 clocks
1	0	0	1	0	18 clocks
1	0	0	1	1	19 clocks
1	0	1	0	0	20 clocks
1	0	1	0	1	21 clocks

	RT	NB [4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Restriction	EXTC should be high to enable this command								
			Status			Availability			
		Nor	mal Mode ON, Idle Mode	OFF, Sleep	OUT	Yes			
Register		Nor	mal Mode ON, Idle Mod	e ON, Sleep (DUT	Yes			
Availability		Par	tial Mode ON, Idle Mode	OFF, Sleep (TUC	Yes			
-		Pa	rtial Mode ON, Idle Mode	e ON, Sleep C	DUT	Yes			
			Sleep IN			Yes			
				5.4					
			Status	Defau					
				DIVB [1:0]	RTN	IB [4:0]			
Default			Power ON Sequence	2'b00	5'l	n1Bh			
			SW Reset	2'b00	5'l	n1Bh			
			HW Reset	2'b00	5'l	n1Bh			





8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)

B3h		FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	DIVC	[1:0]	00
2 nd Parameter	1	1	1	XX	0	0	0		F	RTNC [4:0	0]		1B

Formula to calculate frame frequency:

Frame Rate= $\frac{\text{fosc}}{\text{Clocks per line } \text{x Division ratio x (Lines + VBP + VFP)}}$

Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.

fosc: internal oscillator frequency
Clocks per line: RTNC setting
Division ratio: DIVC setting
Lines: total driving line number
VBP: back porch line number
VFP: front porch line number

	RTI	NC [4:0]	Frame Rate (Hz)				
1	0	0	0	0	119			
1	0	0	0	1	112			
1	0	0	1	0	106			
1	0	0	1	1	100			
1	0	1	0	0	95			
1	0	1	0	1	90			
1	0	1	1	0	86			
1	0	1	1	1	83			

	RT	NC [4:0]	Frame Rate (Hz)			
1	1	0	0	0	79		
1	1	0	0	1	76		
1	1	0	1	0	73		
1	1	0	1	1	70(default)		
1	1	1	0	0	68		
1	1	1	0	1	65		
1	1	1	0	1	63		
1	1	1	1	1	61		

Description

DIVC [1:0]: division ratio for internal clocks when Partial mode.

DIVC	[1:0]	Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNC [4:0]: RTNC [4:0] is used to set 1H (line) period of Partial mode at MCU interface.

	RTI	NC [4:0]		Clock per
		_			LINE
0	0	0	0	0	Setting prohibited
0	0	0	0	1	Setting prohibited
0	0	0	1	0	Setting prohibited
0	0	0	1	1	Setting prohibited
0	0	1	0	0	Setting prohibited
0	0	1	0	1	Setting prohibited
0	0	1	1	0	Setting prohibited
0	0	1	1	1	Setting prohibited
0	1	0	0	0	Setting prohibited
0	1	0	0	1	Setting prohibited
0	1	0	1	0	Setting prohibited

	RTI	NC [4:0]		Clock per Line			
0	1	0	1	1	Setting prohibited			
0	1	1	0	0	Setting prohibited			
0	1	1	0	1	Setting prohibited			
0	1	1	1	0	Setting prohibited			
0	1	1	1	1	Setting prohibited			
1	0	0	0	0	16 clocks			
1	0	0	0	1	17 clocks			
1	0	0	1	0	18 clocks			
1	0	0	1	1	19 clocks			
1	0	1	0	0	20 clocks			
1	0	1	0	1	21 clocks			

	RTI	NC [4:0]	Clock per Line	
1	0	1	1	0	22 clocks
1	0	1	1	1	23 clocks
1	1	0	0	0	24 clocks
1	1	0	0	1	25 clocks
1	1	0	1	0	26 clocks
1	1	0	1	1	27 clocks
1	1	1	0	0	28 clocks
1	1	1	0	1	29 clocks
1	1	1	1	0	30 clocks
1	1	1	1	1	31 clocks





Restriction	EXTC should be high to enable this command									
			Status			Availability				
		Nor	mal Mode ON, Idle Mode	e OFF, Sleep	OUT	Yes				
Register		Noi	rmal Mode ON, Idle Mod	e ON, Sleep (TUC	Yes				
Availability		Par	rtial Mode ON, Idle Mode	OFF, Sleep (TUC	Yes				
		Pa	rtial Mode ON, Idle Mode	e ON, Sleep C	DUT	Yes				
			Sleep IN			Yes				
			Status	Default Valu		е				
			Clarab	DIVC [1:0]	RTN	IC [4:0]				
Default			Power ON Sequence	2'b00	5'l	n1Bh				
		SW Reset 2'b00 5'h1Bh								
			HW Reset	2'b00	5'l	n1Bh				





8.3.5. Display Inversion Control (B4h)

B4h		INVTR (Display Inversion Control)											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1 st Parameter	1	1	↑	XX	0	0	0	0	0	NLA	NLB	NLC	02
		Display inversion mode set NLA: Inversion setting in full colors normal mode (Normal mode on)											
	NLB: I	LB: Inversion setting in Idle mode (Idle mode on)											
Description	NLC: I	NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off)											
Description					NLA / N	NLB / NLC		version					
						0		inversion					
						1	Fram	e inversio	n				
Restriction	EXTC	should be	e high to e	nable this com	mand								
Register Availability		Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes											
Default				-	Sta Power ON SW F H/W I	Sequence Reset	NLA	1'b1 1'b1	ne NLC 1'b0 1'b0 1'b0				





8.3.6. Blanking Porch Control (B5h)

B5h		PRCTR (Blanking Porch)											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1 st Parameter	1	1	↑	XX	0	VFP [6:0]							02
2 nd Parameter	1	1	↑	XX	0				VBP [6:0]				02
3 rd Parameter	1	1	↑	XX	0	0	0			HFP [4:0]			0A
4 th Parameter	1	1	↑	XX	0	0	0			HBP [4:0]			14

VFP [6:0] / **VBP [6:0]:** The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
0000110	6	1000110	70
0000111	7	1000111	71
0001000	8	1001000	72
0001001	9	1001001	73
0001010	10	1001010	74
0001011	11	1001011	75
0001100	12	1001100	76
0001101	13	1001101	77
:	:	:	:
:	:	:	:
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Description

Note: VFP + VBP ≤ 254 HSYNC signals

HFP [4:0] / **HBP [4:0]:** The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.

HFP [4:0] HBP [4:0]	Number of DOTCLK of the front/back por				
00000	Setting prohibited				
00001	Setting prohibited				
00010	2				
00011	3				
00100	4				
00101	5				
00110	6				
00111	7				
01000	8				
01001	9				
01010	10				
01011	11				
01100	12				
01101	13				
01110	14				
01111	15				

HFP [4:0] HBP [4:0]	Number of DOTCLK of front/back porch
10000	16
10001	17
10010	18
10011	19
10100	20
10101	21
10110	22
10111	23
11000	24
11001	25
11010	26
11011	27
11100	28
11101	29
11110	30
11111	31

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Restriction	EXTC should be high to enable this command								
		[Status Ava						
			Normal Mode	ON, Idle Mode	OFF, Sleep O	UT Y	'es		
Register			Normal Mode	ON, Idle Mode	e ON, Sleep Ol	JT Y	'es		
Availability			Partial Mode	ON, Idle Mode	OFF, Sleep Ol	JT Y	'es		
-			Partial Mode	JT Y	'es				
					Y	'es			
					Default	Value			
			Status	VFP [6:0]	VBP [6:0]	HFP [4:0] НВІ	P [4:0]	
Default		Power C	N Sequence	7'h02h	7'h02h	5'h0Ah	5'l	h14h	
		SV	V Reset	7'h02h	7'h02h	5'h0Ah	5'l	h14h	
		HV	V Reset	7'h02h	7'h02h	5'h0Ah	5'	h14h	





8.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	0	1	1	0	B6h
1 st Parameter	1	1	1	XX	0	0	0	0	PTG	[1:0]	PT	[1:0]	0A
2 nd Parameter	1	1	1	XX	REV	GS	SS	SM		ISC	[3:0]		82
3 rd Parameter	1	1	1	XX	0	0	NL [5:0]			27			
4 th Parameter	1	1	1	XX	0	0	PCDIV [5:0]					XX	

PTG [1:0]: Set the scan mode in non-display area.

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output
0	0	Normal scan	Set with the PT [2:0] bits	VCOMH/VCOML
0	1	Setting prohibited		
1	0	Interval scan	Set with the PT [2:0] bits	
1	1	Setting prohibited		

PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode.

Source output on no			non-display area	VCOM output on non-display area		
PI	PT [1:0] Positive polarity		Negative polarity	Positive polarity	Negative polarity	
0	0	V63	V0	VCOML	VCOMH	
0	1	V0	V63	VCOML	VCOMH	
1	0	AGND	AGND	AGND	AGND	
1	1	Hi-Z	Hi-Z	AGND	AGND	

SS: Select the shift direction of outputs from the source driver.

SS	Source Output Scan Direction						
0	S1 → S720						
1	S720 → S1						

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.

Description

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

REV: Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan.

Then scan cycle is set as odd number from $0\sim29$ frame periods. The polarity is inverted every scan cycle.

ISC [3:0]	Scan Cycle	f _{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms



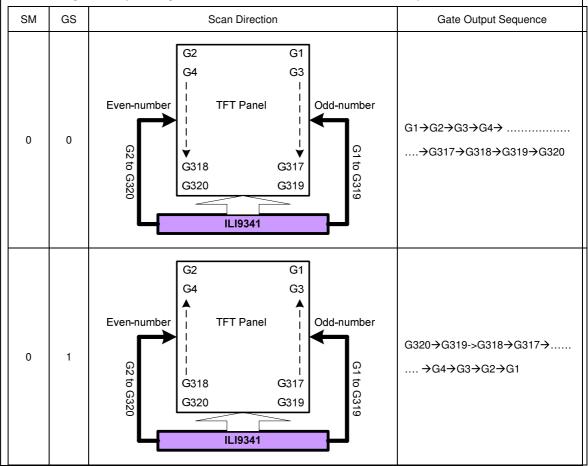


1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

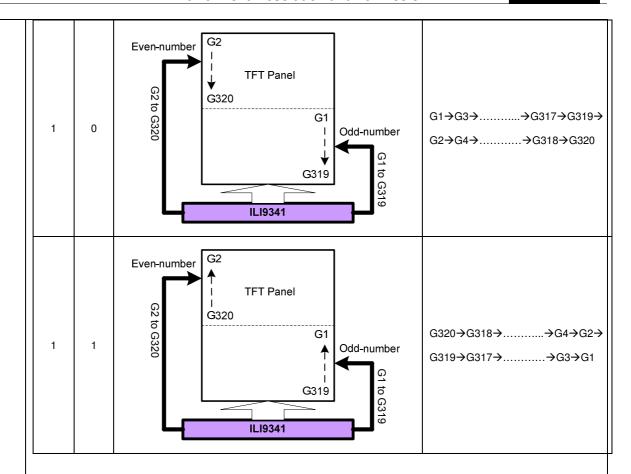
GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction				
0	G1 → G320				
1	G320 → G1				

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.







NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

		NL J	[5:0]	LCD Drive Line		
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	0	1	0	0	1	80 lines
0	0	1	0	1	0	88 lines
0	0	1	0	1	1	96 lines
0	0	1	1	0	0	104 lines
0	0	1	1	0	1	112 lines
0	0	1	1	1	0	120 lines
0	0	1	1	1	1	128 lines
0	1	0	0	0	0	136 lines
0	1	0	0	0	1	144 lines
0	1	0	0	1	0	152 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

		NL	[5:0]			LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
0	1	1	1	1	0	248 lines
0	1	1	1	1	1	256 lines
1	0	0	0	0	0	264 lines
1	0	0	0	0	1	272 lines
1	0	0	0	1	0	280 lines
1	0	0	0	1	1	288 lines
1	0	0	1	0	0	296 lines
1	0	0	1	0	1	304 lines
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
		Oth	ers			Setting inhibited

PCDIV [5:0]:





			exte	rnal fosc=	DC 2×(P	TCLK CDIV	+1)				
Restriction	EXTC should be high to ena	able thi	is command								
				01-1				A ! I = I = !	Pa.		
		Norn	nal Mode ON	Status Idle Mode	OFF. S	Sleen O		Availabi Yes	iity		
Register			nal Mode ON					Yes			
Availability			ial Mode ON,					Yes			
		Par	tial Mode ON		ON, SI	eep Ol	JT	Yes			
				Sleep IN				Yes			
	Status				Default Value						
Default			PTG [1:0]	PT [1:0]	REV	GS	SS	SM	ISC [3:0]	NL [5:0]	
Deiduit	Power ON Sequ SW Reset		2'b10 2'b10	2'b10 2'b10	1'b1 1'b1	1'b0 1'b0	1'b0 1'b0	1'b0 1'b0	4'b0010 4'b0010	6'h27h 6'h27h	
	HW Reset		2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h	





8.3.8. Entry Mode Set (B7h)

B7h					E	TMOD	(Entry M	ode Set)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D	4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1		0	1	1	1	B7h
Parameter	1	1	↑	XX	0	0	0	0)	DSTB	GON	DTE	GAS	06
Description	DSTB: The ILI9341 driver enters the Deep Standby Mode when DSTB is set to high ("1"). In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited. Note: ILI9341 provides two ways to exit the Deep Standby Mode: (1) Exit Deep Standby Mode by pull down CSX to low ("0") 6 times. (2) Input a RESX pulse with effective low level duration to start up the inside logic regulator and makes a transition to the initial state. CSX WRX "High" D/CX "Low" or "High" D[17:0] Don Care Don Disable GON/DTE: Set the output level of gate driver G1 ~ G320 as follows GON DTE G1~G320 Gate Output 0 0 WGH 0 1 VGH													
					1	1	Norr	VGL nal disp	lay					
Restriction	EXTC :	should be	e high to	enable this com	ımand									
Register Availability	Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes Normal Mode ON, Idle Mode ON, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode OFF, Sleep OUT Yes Partial Mode ON, Idle Mode ON, Sleep OUT Yes Sleep IN Yes													
Default					Status r ON Seq SW Rese HW Rese	t	DSTB 1'b0 1'b0 1'b0	Default GON 1'b1 1'b1	Value DTE 1'b1 1'b1 1'b1	1'b()			





8.3.9. Backlight Control 1 (B8h)

B8h	Backlight Control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	0	0	0	B8h
Parameter		1	1	XX	0	0	0	0	TH_UI [3]	TH_UI [2]	TH_UI [1]	TH_UI [0]	0C
	TH_UI [3	(UI) m		atio of ma	ximum	_		-		umulate histo			
i		TH_UI[Descr	iption		TH UI	[3:0]	Description		
Description			4'0h			99	•		4'8	• •	84%		
			4'1h	1		98	%		4'9	h	82%		
			4'2h	1		96	%		4'A	4'Ah			
			4'3h	1	94%				4'Bh		78%		
			4'4h	1		92	%		4'C	h	76%		
			4'5h			90			4'D		74%		
			4'6h		88%				4'E		72%		
			4'7h	1	86%				4'F	h	70%		
						Sta	atus			Availability			
					Mode On, Idle Mode Of				Sleep Out Yes				
Register									Sleep Out	Yes	_		
Availability									Sleep Out	Yes	_		
						Jn, Idle	e Mode	e On,	Sleep Out	Yes			
				Sleep I	n					Yes			
l				Status					Default Va				
Default					Power (On Sec	quence	Э	4'b0110				
					S۱	N Res	et		No chang	ıe			
					Н\	N Res	et		4'b0110				





8.3.10. Backlight Control 2 (B9h)

B9h		Backlight Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	1	0	1	1	1	0	0	1	B9h	
Parameter	1	1	↑	XX	TH_MV [3]	TH_MV [2]	TH_MV [1]	TH_MV [0]	TH_ST [3]	TH_ST [2]	TH_ST [1]	TH_ST [0]	СС	

TH_ST [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

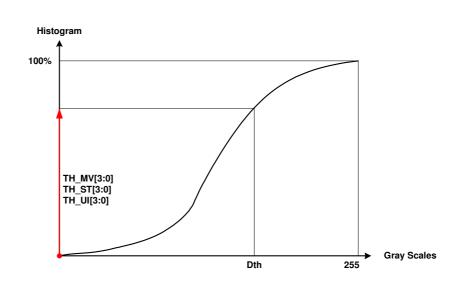
TH_ST [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_ST [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

TH_MV [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_MV [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_MV [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%







		Status					
	Normal Mode On	Normal Mode On, Idle Mode Off, Sleep Out					
Register	Normal Mode On	Normal Mode On, Idle Mode On, Sleep Out					
Availability	Partial Mode On	, Idle Mode Off, Sleep Out	Yes				
	Partial Mode On	Partial Mode On, Idle Mode On, Sleep Out					
Availability	Sleep In	Sleep In					
	Chahua	Default Va	lue				
	Status	TH_MV [3:0]	TH_ST [3:0				
Default	Power On Sequence	4'b1100	4'b1100				
	SW Reset	No change	No change				
	HW Reset	4'b1100	4'b1100				



Description

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K color



8.3.11. Backlight Control 3 (BAh)

BAh		Backlight Control 3											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	0	1	0	BAh
Parameter	1	1	1	XX	0	0	0	0	DTH_UI [3]	DTH_UI [2]	DTH_UI [1]	DTH_UI [0]	04

DTH_UI [3:0]: This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode.

This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_UI [3:0]	Description
4'0h	252
4'1h	248
4'2h	244
4'3h	240
4'4h	236
4'5h	232
4'6h	228
4'7h	224

Description
220
216
212
208
204
200
196
192

	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Register	Normal Mode On, Idle Mode On, Sleep Out	Yes
Availability	Partial Mode On, Idle Mode Off, Sleep Out	Yes
	Partial Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes

	Status	Default Value
	Status	DTH_UI [3:0]
F	Power On Sequence	4'b0100
	SW Reset	No change
	HW Reset	4'b0100





8.3.12. Backlight Control 4 (BBh)

BBh						Bacl	klight Con	trol 4					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	0	1	1	BBh
Parameter	1	1	1	XX	DTH_MV [3]	DTH_MV [2]	DTH_MV [1]	DTH_MV [0]	DTH_ST [3]	DTH_ST [2]	DTH_ST [1]	DTH_ST [0]	65

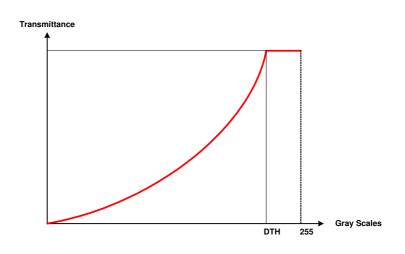
DTH_ST [3:0]/DTH_MV [3:0]: This parameter is used set the minimum limitation of grayscale threshold value. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.

DTH_ST [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_ST [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164

DTH_MV [3:0]	Description
4'0h	224
4'1h	220
4'2h	216
4'3h	212
4'4h	208
4'5h	204
4'6h	200
4'7h	196

DTH_MV [3:0]	Description
4'8h	192
4'9h	188
4'Ah	184
4'Bh	180
4'Ch	176
4'Dh	172
4'Eh	168
4'Fh	164



Register	
Availability	

Description

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes





		Obstant	Default Value		
	Status	DTH_MV [3:0]	DTH_ST [3:0]		
Default		Power On Sequence	4'b0110	4'b0101	
		SW Reset	No change	No change	
		HW Reset	4'b0110	4'b0101	





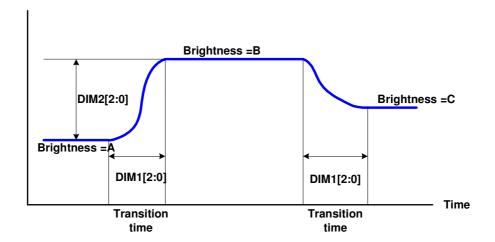
8.3.13. Backlight Control 5 (BCh)

BCh						Backl	ight Contr	ol 5					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	1	0	0	BCh
Parameter	1	1	1	XX	DIM2 [3]	DIM2 [2]	DIM2 [1]	DIM2 [0]	0	DIM1 [2]	DIM1 [1]	DIM1 [0]	44

DIM1 [2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.

DIM1 [2:0]	Description
3'0h	1 frame
3'1h	1 frame
3'2h	2 frames
3'3h	4 frames
3'4h	8 frames
3'5h	16 frames
3'6h	32 frames
3'7h	64 frames

Description



DIM2 [3:0]: This parameter is used to set the threshold of brightness change.

When the brightness transition difference is smaller than DIM2 [3:0], the brightness transition will be ignored.

For example:

If | brightness B - brightness A| < DIM2 [2:0], the brightness transition will be ignored and keep the brightness A.

Register
Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Defaul	t Value				
DIM2 [3:0]	DIM1 [2:0]				
4'b0100	4'b0100				
No change	No change				
4'b0100	4'b0100				
	DIM2 [3:0] 4'b0100 No change				





8.3.14. Backlight Control 7 (BEh)

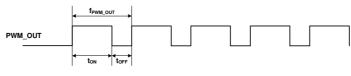
BEh						Bac	klight Co	ntrol 7					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	0	1	1	1	1	1	0	BEh
Parameter	1	1	1	XX	PWM_ DIV[7]	PWM_ DIV[6]	PWM_ DIV[5]	PWM_ DIV[4]	PWM_ DIV[3]	PWM_ DIV[2]	PWM_ DIV[1]	PWM_ DIV[0]	0F

PWM_DIV [7:0]: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of

PWM_OUT. The PWM frequency can be calculated by using the following equation.

$$f_{PWM_OUT} = \frac{16MHz}{(PWM_DIV[7:0]+1)\times255}$$

PWM_DIV [7:0]	f _{PWM_OUT}
8'h0	62.74 KHz
8'h1	31.38 KHz
8'h2	20.915KHz
8'h3	15.686KHz
8'h4	12.549 KHz
8'hFB	249Hz
8'hFC	248Hz
8'hFD	247Hz
8'hFE	246Hz
8'hFF	245Hz



Note: The output frequency tolerance of internal frequency divider in CABC is ±10%

Register
Availability

Description

Availability
Yes
Yes
Yes
Yes
Yes

Default

Default Value
PWM_DIV [7:0]=0Fh
No change
PWM_DIV [7:0]=0Fh





8.3.15. Backlight Control 8 (BFh)

BFh		_		J. U (<u>-</u>	,		Bac	cklight Co	ntrol 2						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	0	1	1	1	1	1	1	BFh		
Parameter	1	1	1	XX	0	0	0	0	0	LEDONR	LEDONPO	LEDPWMPOL	00		
	LEDF	WMPC)L: The	bit is use	d to d	efine polari	ty of L	EDPWM s	ignal.						
				•	BL	LEDPWM									
				-	0	0			0						
				-	0	<u>1</u> 0		Origina	al polarity	of PWM si	anal				
				•	1	1				of PWM s					
	LEDONPOL: This bit is used to control LEDON pin.														
					BL	LEDONP	OL		LEDON	l pin					
Description					0	0			0						
Description					0	1			1						
					1	1		lr	LEDOI oversed Li						
						1			iversed Li	EDOINH					
	LEDO	ONR: TI	his bit is	used to	contro	l LEDON p	in.				_				
						LEDONR		De	escription						
						0			Low						
					L	1			High						
							Sta	tus		Availa	ability				
						nal Mode C									
Register						nal Mode C									
Availability						ial Mode O									
					Slee		n, idie	wode On	, Sieep Ot	ıt Ye					
					0.00	P									
									Default	Value	lue				
					St	atus	LE	EDONR	LEDONF		PWMPOL				
Default				Ро	wer O	n Sequence	Э	1'b0	1'b0		1'b0				
					SW	Reset	No	change	No char	nge No	change				
					HW	Reset		1'b0	1'b0		1'b0				





8.3.16. Power Control 1 (C0h)

	OWEI	PWCTRL 1 (Power Control 1)																				
C0h										PWCTRL '	(Powe	r Co	ontro	ol 1)								
	D/CX	RDX	W	RX			17-8			07 D6	D5	<u> </u>	D4 D3			D2	D1 0	D0	HEX			
Command	0	1		<u> </u>			XX			1 1 0					0 0 0					0	C0h	
1 st Parameter	1	1 1 ↑ XX 0 0 0 VRH [5:0] VRH [5:0]: Set the GVDD level, which is a reference level for the VCOM level and the grayscale voltage level.														21						
	VRH [5	5:0]: Set	the •	GVE	DD I	evel,	el, which is a reference level for the VCOM level and															
			-				[5:0			GVD						[5:0			GVDD			
			-	0	0	0	0	0	1	Setting pro			1	0	0	0	0	0	4.45 V 4.50 V			
			_	0	0	0	0	1	0	Setting pro			1	0	0	0	1	0	4.55 V			
			-	0	0	0	0	1	1	3.00			1	0	0	0	1	1	4.60 V			
			-	0	0	0	1	0	1	3.05 3.10			1	0	0	1	0	1	4.65 V 4.70 V			
			-	0	0	0	1	1	0	3.15			1	0	0	1	1	0	4.75 V			
				0	0	0	1	1	1	3.20			1	0	0	1	1	1	4.80 V			
			-	0	0	1	0	0	0	3.25			1	0	1	0	0	0	4.85 V			
			-	0	0	1	0	1	0	3.30 3.35			1	0	1	0	1	0	4.90 V 4.95 V			
			-	0	0	1	0	1	1	3.40			1	0	1	0	1	1	5.00 V			
				0	0	1	1	0	0	3.45	V		1	0	1	1	0	0	5.05 V			
			-	0	0	1	1	0	1	3.50			1	0	1	1	0	1	5.10 V			
			-	0	0	1	1	1	1	3.55 3.60			1	0	1	1	1	1	5.15 V 5.20 V			
Description				0	1	0	0	0	0	3.65	V		1	1	0	0	0	0	5.25 V			
			_	0	1	0	0	0	1	3.70			1	1	0	0	0	1	5.30 V			
			-	0	1	0	0	1	1	3.75 3.80			1	1	0	0	1	1	5.35 V 5.40 V			
			-	0	1	0	1	0	0	3.85			1	1	0	1	0	0	5.45 V			
				0	1	0	1	0	1	3.90	V		1	1	0	1	0	1	5.50 V			
			-	0	1	0	1	1	0	3.95			1	1	0	1	1	0	5.55 V			
			-	0	1	1	0	0	0	4.00 4.05			1	1	1	0	0	0	5.60 V 5.65 V			
				0	1	1	0	0	1	4.10			1	1	1	0	0	1	5.70 V			
			-	0	1	1	0	1	0	4.15			1	1	1	0	1	0	5.75 V			
			-	0	1	1	1	0	0	4.20 4.25			1	1	1	0	0	0	5.80 V 5.85 V			
			-	0	1	1	1	0	1	4.30			1	1	1	1	0	1	5.90 V			
				0	1	1	1	1	0	4.35			1	1	1	1	1	0	5.95 V			
				0	1	1	1	1	1	4.40			1	1	1	1	1	1	6.00 V			
	Note1:	Make sı	ure ti	hat \	/C a	and	VRH	sett	ing i	estriction: G	VDD ≦	(AV	'DD	- 0.5) V.							
Restriction	EVTC	should b	o hic	nh to	one	abla	thic	com	man	.d												
Restriction	LXIU	SHOUIU D	e mç	JII LO	CIIC	abie	uns	COIII	IIIai	lu												
										- · ·					Ι.							
							N.I		41	Statu		- 01		O		Avail		ty				
Register										ON, Idle M							es					
										e ON, Idle M ON, Idle Mo							es es					
Availability						-				ON, Idle M							es es					
						-	ı uı	tiai	viouc	Sleep		Oic	СР	, , , , , , , , , , , , , , , , , , , 			es					
						<u> </u>				Олоор							.					
																1						
										Status				It Va								
Doforth									_					1 [5:0								
Default									P	ower ON Sec		<u> </u>		121h		-						
									-	SW Res				121h		1						
									<u> </u>	HW Res	J l		σr	121h		1						
			_	_	_	_	_	_	_			_	_	_	_	_	_	_		·	_	





8.3.17. Power Control 2 (C1h)

C1h					PW	CTRL 2 (I	Power Co	ontrol 2)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	1	XX	1	1	0	0	0	0	0	1	C1h	
Parameter	1	1	1	XX	0	0	0	1	0		BT [2:0]		10	
Description	Note1:	Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.												
Restriction	EXTC should be high to enable this command													
Register Availability				Normal Partial N	Mode ON, Mode ON, Mode ON, Mode ON,	Idle Mod	e ON, Sle OFF, Sle	eep OUT eep OUT	Availal Yes Yes Yes Yes	S S S S S S S S S S S S S S S S S S S				
Default					Power (Status ON Seque W Reset W Reset		efault Val BT [2:0] 3'b000 3'b000 3'b000	ue					





0010010

0010011

-2.050

-2.025

C5h							VMCTRL1 (V	/CC	M Control 1	1)				
	D/CX	RDX	WRX	D1	7-8	D7	D6	[D5 D4	D3	D2	D1	D0	НЕ
Command	0	1	1	Х	Х	1	1		0 0	0	1	0	1	C:
st Parameter	1	1	1	Х	XX)			VMH [6:0]				3
nd Parameter	1	1	1	Х	X	0				VML [6:0]				3
	VMH [6:0] : Se	et the VCOMI	l vol	tage.									
	VMI	H [6:0]	VCOMH(V)		VMH [6:0]		VCOMH(V)	1	VMH [6:0]	VCOMH(\	/)	VMH [6:0	1 VCO	MH(V
		00000	2.700	1	01000		3.500		1000000	4.300	')	1100000	-	100
	000	00001	2.725		01000	01	3.525		1000001	4.325		1100001	5.	125
		00010	2.750]	01000		3.550		1000010	4.350		1100010	_	150
	0000011				01000		3.575		1000011	4.375		1100011		175
	0000100				01001 01001		3.600 3.625	-	1000100	4.400 4.425		1100100		200 225
		0110		2.850		10	3.650	-	1000101	4.423		1100101		250 250
	0000111			2.875		11	3.675	1	1000111	4.475	-	1100111		275
		1000	2.900		01010		3.700		1001000	4.500		1101000		300
		1001	2.925		01010	_	3.725	1	1001001	4.525		1101001		325
Description		1010	2.950		01010		3.750	-	1001010	4.550	_	1101010		350
)1011)1100	2.975 3.000	+	01010 01011		3.775 3.800	-	1001011	4.575 4.600		1101011		375 400
)1101	3.025	+ 1	01011		3.825		1001100	4.625		1101101		425
)1110	3.050	1	01011	_	3.850		1001110	4.650		1101110		450
	000)1111	3.075		01011	11	3.875		1001111	4.675		1101111	5.	475
		0000	3.100		01100		3.900		1010000	4.700		1110000		500
		0001	3.125	4	01100		3.925		1010001	4.725		1110001		525
		0010 0011	3.150 3.175	+	01100 01100		3.950 3.975		1010010 1010011	4.750 4.775		1110010		550 575
		0100	3.200	+	01101		4.000	-	1010011	4.800		1110100		600
		0101	3.225	1	01101		4.025		1010101	4.825		1110101		625
		0110	3.250]	01101		4.050		1010110	4.850		1110110		650
		0111	3.275	4	01101		4.075		1010111	4.875		1110111		675
		1000	3.300	4	01110		4.100	_	1011000	4.900		1111000		700
		1001 1010	3.325 3.350	+ 1	01110		4.125 4.150		1011001 1011010	4.925 4.950		1111001		725 750
		1011	3.375		01110		4.175		1011011	4.975		1111011		775
		0011100 3.400			01111		4.200		1011100 5.000			1111100		800
		0011101 3.425			011110		4.225		1011101 5.025			1111101		825
		1110	3.450 3.475	4	01111				1011110	5.050 5.075		1111111		850
	0011111 3.475 0111111 4.275 1011111 5.075 1111111 5.875													
	VML [6:0] : Set the VCOML voltage													
	I	/L [6:0]	VCOML(V)	VML [6		VCOML(V)	-	VML [6:0]	VCOML(V)	VML [6:0]	_	
	I	000000	-2.500 -2.475	\dashv	01000		-1.700 -1.675		1000000 1000001	-0.900 -0.875	-	1100000 1100001	-0.1 -0.0	
	I	00001	-2.475	\dashv	01000		-1.650	1	1000001	-0.875	⊣	1100001	-0.0	
	I	00011	-2.425		01000		-1.625	ĺ	1000011	-0.825	-	1100011	-0.0	
	I	00100	-2.400		01001		-1.600		1000100	-0.800] [1100100	0	
	I	000101	-2.375		01001		-1.575	1	1000101	-0.775	⅃ [1100101	Rese	
	I	000110	-2.350	4	01001		-1.550	-	1000110	-0.750	4	1100110	Rese	
	I	000111	-2.325 -2.300	\dashv	01001		-1.525 -1.500	1	1000111	-0.725 -0.700	- 	1100111	Rese Rese	
	I	01000	-2.300 -2.275	\dashv	01010		-1.500		1001000 1001001	-0.700	\dashv \dagger	1101000 1101001	Rese	
	I	01010	-2.250		01010		-1.450	1	1001001	-0.650	⊣	1101001	Rese	
	I	01011	-2.225		01010		-1.425	j	1001011	-0.625	<u> </u>	1101011	Rese	
	00	01100	-2.200		01011	00	-1.400		1001100	-0.600	□ [1101100	Rese	
	I	01101	-2.175	4	01011		-1.375	-	1001101	-0.575	-	1101101	Rese	
	I	01110	-2.150	\dashv	01011		-1.350	-	1001110	-0.550	⊣ ∤	1101110	Rese	
		01111	-2.125		01011	H	-1.325	1	1001111	-0.525	11	1101111	Rese	
	00	10000	-2.100		01100	nn l	-1.300		1010000	-0.500		1110000	Rese	rved

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-1.250

-1.225

1010010

1010011

-0.450

-0.425

1110010

1110011

Reserved

Reserved

0110010

0110011





	0010100 -2.000		0110100	-1.200		1010100	-0.400	1110100	Reserved
					-				
	0010101 -1.975		0110101	-1.175	_	1010101	-0.375	1110101	Reserved
	0010110 -1.950		0110110	-1.150	_	1010110	-0.350	1110110	Reserved
	0010111 -1.925		0110111	-1.125	_	1010111	-0.325	1110111	Reserved
	0011000 -1.900		0111000	-1.100		1011000	-0.300	1111000	Reserved
	0011001 -1.875		0111001	-1.075	_	1011001	-0.275	1111001	Reserved
	0011010 -1.850		0111010	-1.050		1011010	-0.250	1111010	Reserved
	0011011 -1.825		0111011	-1.025		1011011	-0.225	1111011	Reserved
	0011100 -1.800		0111100	-1.000		1011100	-0.200	1111100	Reserved
	0011101 -1.775		0111101	-0.975		1011101	-0.175	1111101	Reserved
	0011110 -1.750		0111110	-0.950		1011110	-0.150	1111110	Reserved
	0011111 -1.725		0111111	-0.925		1011111	-0.125	1111111	Reserved
Restriction	EXTC should be high to e	nabl	e this command	d					
		Ī		Status			Availability	,	
			Normal Mode			EE Cloop OI	1	_	
Register		ŀ							
l regions			Normal Mode	,					
Availability			Partial Mode	ON, Idle Mo	de Ol	FF, Sleep OU	T Yes		
			Partial Mode	ON, Idle Mo	de O	N, Sleep OU	T Yes		
				Sleep II	N		Yes		
		L		'			· · · · · · · · · · · · · · · · · · ·		
			-			Default V	/alue		
			Sta	tus	VM	H [6:0]	VML [6:0]		
Default			Power ON	Sequence	7	"h31	7'h3C		
			SW F	Reset	7	"h31	7'h3C		
			HW	Rest	7	"h31	7'h3C		
							_		



Description

a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K color



8.3.19. VCOM Control 2(C7h)

C7h					VM	CTRL1 (VCOM Co	ontrol 1)							
	D/CX	RDX WRX D17-8 D7 D6 D5 D4 D3 D2 D1 D0 HEX													
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h		
Parameter	1	1	1	XX	nVM	1 VMF [6:0] CC									

nVM: nVM equals to "0" after power on reset and VCOM offset equals to program MTP value. When nVM set to "1", setting of VMF [6:0] becomes valid and VCOMH/VCOML can be adjusted.

VMF [6:0]: Set the VCOM offset voltage.

]: Set the V	COM offset	voltage.				
	VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML
	0000000	VMH	VML	1000000	VMH	VML
	0000001	VMH - 63	VML - 63	1000001	VMH + 1	VML + 1
	0000010	VMH - 62	VML - 62	1000010	VMH + 2	VML + 2
	0000011	VMH – 61	VML - 61	1000011	VMH + 3	VML + 3
	0000100	VMH - 60	VML - 60	1000100	VMH + 4	VML + 4
	0000101	VMH – 58	VML – 58	1000101	VMH + 5	VML + 5
	0000110	VMH – 58	VML – 58	1000110	VMH + 6	VML + 6
	0000111	VMH – 57	VML – 57	1000111	VMH + 7	VML + 7
	0001000	VMH – 56	VML – 56	1001000	VMH + 8	VML + 8
	0001001	VMH – 55	VML – 55	1001001	VMH + 9	VML + 9
	0001010	VMH – 54	VML – 54	1001010	VMH + 10	VML + 10
	0001011	VMH – 53	VML – 53	1001011	VMH + 11	VML + 11
	0001100	VMH – 52	VML – 52	1001100	VMH + 12	VML + 12
	0001101	VMH – 51	VML -51	1001101	VMH + 13	VML + 13
	0001110	VMH – 50	VML – 50	1001110	VMH + 14	VML + 14
	0001111	VMH – 49	VML – 49	1001111	VMH + 15	VML + 15
	0010000	VMH – 48	VML – 48	1010000	VMH + 16	VML + 16
	0010001	VMH – 47	VML – 47	1010001	VMH + 17	VML + 17
	0010010	VMH – 46	VML – 46	1010010	VMH + 18	VML + 18
	0010011	VMH – 45	VML – 45	1010011	VMH + 19	VML + 19
	0010100	VMH – 44	VML - 44	1010100	VMH + 20	VML + 20
	0010101	VMH – 43 VMH – 42	VML – 43 VML – 42	1010101	VMH + 21 VMH + 22	VML + 21
	0010110	VMH – 42	VML – 42	1010110 1010111	VMH + 23	VML + 22 VML + 23
	0010111	VMH – 40	VML – 41	10111000	VMH + 24	VML + 24
	0011000	VMH – 39	VML – 39	1011000	VMH + 25	VML + 25
	0011010	VMH – 38	VML – 38	1011010	VMH + 26	VML + 26
	0011011	VMH – 37	VML – 37	1011011	VMH + 27	VML + 27
	0011100	VMH – 36	VML – 36	1011100	VMH + 28	VML + 28
	0011101	VMH – 35	VML – 35	1011101	VMH + 29	VML + 29
	0011110	VMH – 34	VML – 34	1011110	VMH + 30	VML + 30
	0011111	VMH - 33	VML - 33	1011111	VMH + 31	VML + 31
	0100000	VMH - 32	VML – 32	1100000	VMH + 32	VML + 32
	0100001	VMH – 31	VML – 31	1100001	VMH + 33	VML + 33
	0100010	VMH – 30	VML – 30	1100010	VMH + 34	VML + 34
	0100011	VMH – 29	VML – 29	1100011	VMH + 35	VML + 35
	0100100	VMH – 28	VML – 28	1100100	VMH + 36	VML + 36
	0100101	VMH – 27	VML – 27	1100101	VMH + 37	VML + 37
	0100110	VMH – 26	VML – 26	1100110	VMH + 38	VML + 38
	0100111	VMH – 25	VML – 25	1100111	VMH + 39	VML + 39
	0101000	VMH – 24	VML – 24	1101000	VMH + 40	VML + 40
	0101001	VMH – 23	VML – 23	1101001	VMH + 41	VML + 41
	0101010	VMH – 22	VML – 22	1101010	VMH + 42	VML + 42
	0101011	VMH – 21 VMH – 20	VML - 21	1101011	VMH + 43	VML + 43
	0101100	VMH – 20 VMH – 19	VML - 20	1101100	VMH + 44 VMH + 45	VML + 44
	0101101	VMH – 19 VMH – 18	VML – 19 VML – 18	1101101	VMH + 45	VML + 45 VML + 46
	0101110	VMH – 18	VML – 18	11011110	VMH + 47	VML + 46
	0110000	VMH – 17	VML – 17	1110000	VMH + 48	VML + 47
	0110000	VMH – 15	VML – 15	1110001	VMH + 49	VML + 49
	0110001	VMH – 14	VML – 14	1110001	VMH + 50	VML + 50
	0110011	VMH – 13	VML – 13	1110011	VMH + 51	VML + 51
	0110100	VMH – 12	VML – 12	1110100	VMH + 52	VML + 52

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	0110101	\/\/III 44	1/1/11		4440404	\ /A	4LL . FO	\/MI . FO	
	0110101		VML - 11	_	1110101	_	/IH + 53	VML + 53	
	0110110		VML - 10		1110110		ЛН + 54	VML + 54	
	0110111		VML – 9		1110111		ЛН + 55	VML + 55	
	0111000		VML – 8		1111000		ЛH + 56	VML + 56	
	0111001		VML – 7		1111001		ЛН + 57	VML + 57	
	0111010		VML – 6		1111010		/IH + 58	VML + 58	
	0111011		VML – 5		1111011	_	ЛH + 59	VML + 59	
	0111100		VML – 4		1111100	_	ЛH + 60	VML + 60	
	0111101		VML – 3		1111101	_	/IH + 61	VML + 61	
	0111110		VML – 2		1111110		ЛH + 62	VML + 62	
	0111111	VMH – 1	VML – 1		1111111	V۱	ЛH + 63	VML + 63	
Restriction	EXTC should be high to enable	this command							
	Г		Statu				Availabil	ity	
	F							ity	
Register		Normal Mode C	ON, Idle Mo	ode ()FF, Sleep	OUT	Yes		
negistei	<u> </u>	Normal Mode (ON, Idle M	ode (ON, Sleep	OUT	Yes		
Availability		Partial Mode O	N, Idle Mo	de C	FF, Sleep	OUT	Yes		
,		Partial Mode C	ON. Idle Mo	ode C	N. Sleep (OUT	Yes		
			Sleep		,		Yes		
	L		Sieep	IN			168		
					D (1			
		Status	, -		Defau	ilt valu	ie		
		2.0.00		ı	nVM	VI	ИF [6:0]		
Default		Power ON Se	equence		1'b1	7	7'h40h		
					1'b1	7	7'h40h		
		HW Res			1'b1		7'h40h	_	
	I	I IIVV NES	οCι		101	- /	114011	1	
Default		Status Power ON Se	equence		nVM	7	MF [6:0]		





8.3.20. NV Memory Write (D0h)

D0h					NV	MWR (I	NV Memor	y Write)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h		
1 st Parameter	1	1	↑	XX	0	0	0	0	0	PG	M_ADR [2:0]	00		
2 nd Parameter	1	1	↑	XX				PGM_	DATA [7:0]				XX		
	This co	mmand	is used to	program the	NV memor	y data. A	After a succ	essful M	ITP operat	ion, the in	formation	of PGM_	_DATA		
	[7:0] wi	ill progra	ımmed to	NV memory.											
	PGM_A	ADR [2:0	0] : The se	lect bits of ID1	, ID2, ID3	and VM	F [6:0] prog	gramming	g.						
				PGM	_ADR [2:0	Prog	grammed N	IV Memo	ry Selection	n					
Description				0	0 0		ID1 pr	ogramm	ing						
				0	0 1			ogramm							
				0	1 0		ID3 pr	ogramm	ing						
				1 0 0 VMF [6:0] programming											
l			Others Reserved												
Restriction		PGM_DATA [7:0]: The programmed data. EXTC should be high to enable this command													
						Ctatus			A! a	.:!!!					
				Normal	Mada ON	Status			Availat						
Register							de OFF, Sl ode ON, Sl	· ·							
Avoilability							de OFF, Sl								
Availability							de ON, Sle								
						Sleep I		ж с	Yes						
							D	efault Va	alue						
					Status	P	 GM_ADR [2		GM_DATA	[7:0]					
Default				Power (ON Sequen		3'b000		MTP valu						
				SI	V Reset		3'b000		MTP valu	е					
				H\	V Reset		3'b000		MTP valu	е					





8.3.21. NV Memory Protection Key (D1h)

D1h					NVMP	KEY (NV	Memory	Protection	Key)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
Command	0	1	1	XX	1	1	0	1	0	0	0	1	D1h			
1 st Parameter	1	1	1	XX				KEY [2	3:16]				55h			
2 nd Parameter	1	1	1	XX				KEY [15:8]				AAh			
3 rd Parameter	1	1	1	XX				KEY	[7:0]				66h			
Description	_	- 466h to		y programming		•		· ·	•	ŭ			ing will			
Restriction	EXTC	XTC should be high to enable this command														
					Status Availability											
				Norma	al Mode O	N, Idle M	ode OFF	Sleep OUT	Yes	5						
Register				Norma	al Mode C	N, Idle M	lode ON,	Sleep OUT	Yes	3						
Availability				Partia	l Mode Of	N, Idle M	ode OFF,	Sleep OUT	Yes	3						
				Partia	l Mode O	N, Idle M	ode ON,	Sleep OUT	Yes	5						
						Sleep	IN		Yes	3						
				Ļ	Status Default Value											
Default					Power O		nce KE	Y [23:0]=55/	AA66h							
					SW Reset KEY [23:0]=55AA66h											
				L	HW Reset KEY [23:0]=55AA66h KEY [23:0]=55AA66h											





8.3.22. NV Memory Status Read (D2h)

D2h					RDNVM	(NV I	Memory St	tatus Read)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
1 st Parameter	1	1	1	XX	Х	Х	Х	Х	Х	Χ	Х	Х	Х
2 nd Parameter	1	↑	1	XX	0		ID2_CNT [[2:0]	0		D1_CNT	[2:0]	XX
3 rd Parameter	1	↑	1	XX	BUSY	'	VMF_CNT	[2:0]	0	I	D3_CNT	[2:0]	XX
Description	automa	 itically aft	er writing		T [2:0] to N T [2:0] / II T [2:0] / V Statu 0 0 1	D2_CI	emory. NT [2:0] CNT [2:0] 0 1 1 1	Avai No Programi Programn Programn	ription ability grammed ned 1 time ned 2 time ned 3 time	e ess	. The bits	will increa	se "+1"
Restriction	EXTC s	should be	high to e	nable this comm	and								
						Status	3		Availabi	ility			
				Normal Mo				leep OUT	Yes				
Register							ode ON, SI		Yes				
Availability							de OFF, SI		Yes				
,				Partial Mo	de ON, lo	dle Mo	ode ON, Sl	eep OUT	Yes				
					S	Sleep I	IN		Yes				
				0				Default Valu	е				
				Status	ID3_C	NT	ID2_CNT	ID1_CNT		CNT	BUSY		
Default			Powe	er ON Sequence	Х		Χ	Х	Х		Χ		
				SW Reset	Х		Χ	Х	Х		Х		
ı				HW Reset	Х		Χ	Х	Х		Χ		





8.3.23. Read ID4 (D3h)

D3h						RDID4	(Read II	04)							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	1	0	1	0	0	1	1	D3h		
1 st Parameter	1	1	1	XX	Χ	Х	Χ	Х	Х	Х	Х	Χ	Х		
2 nd Parameter	1	1	1	XX	0	0	0	0	0	0	0	0	00h		
3 rd Parameter	1	↑	1	XX	1	0	0	1	0	0	1	1	93h		
4 th Parameter	1	↑	1	XX	0	1	0	0	0	0	0	1	41h		
Description	The 1 st	parame	eter is dun eter mean	nmy read period as the IC version or mean the IC n		ne.									
Restriction	EXTC :	TC should be high to enable this command													
						Status			Availa	bility					
				Normal N	/lode ON	Idle Mod	e OFF, S	leep OUT	Yes						
Register				Normal I	Mode ON	, Idle Mod	le ON, SI	eep OUT	Yes	S					
Availability				Partial M	lode ON,	Idle Mode	e OFF, SI	eep OUT	Yes	S					
				Partial N	∕lode ON	Idle Mod	e ON, Sle	eep OUT	Yes	s					
						Sleep IN			Yes	S					
Default		Sleep IN Yes Status Default Value Power ON Sequence 24'h009341h SW Reset 24'h009341h													
					Н	W Reset	2	4'h009341	h						





8.3.24. Positive Gamma Correction (E0h)

E0h					PGAM	CTRL (Po	sitive Ga	amma Con	trol)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0	0	0	0	0	E0h
1 st Parameter	1	1	1	XX	0	0	0	0		VP63	[3:0]		08
2 nd Parameter	1	1	1	XX	0	0			VP62	[5:0]			
3 rd Parameter	1	1	↑	XX	0	0			VP61	[5:0]			
4 th Parameter	1	1	↑	X	0	0	0	0		VP59	[3:0]		05
5 th Parameter	1	1	1	XX	0	0	0		\	/P57 [4:0]			
6 th Parameter	1	1	1	XX	0	0	0	0		VP50	[3:0]		09
7 th Parameter	1	1	1	XX	0			\	/P43 [6:0]				
8 th Parameter	1	1	1	XX		VP2	7 [3:0]			VP36	[3:0]		
9 th Parameter	1	1	1	XX	0			\	/P20 [6:0]				
10 th Parameter	1	1	1	XX	0	0	0	0		VP13	[3:0]		0B
11 th Parameter	1	1	1	XX	0	0	0		,				
12 th Parameter	1	1	1	XX	0	0	0	0		VP4	[3:0]		00
13 th Parameter	1	1	1	XX	0	0			VP2				
14 th Parameter	1	1	1	XX	0	0			VP1				
15 th Parameter	1	1	1	XX	0	0	0	0			00		
Description	Set the	1 1 ↑ XX 0 0 0 0 VP0 [3:0] Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.											
Restriction	EXTC	should l	oe high to	enable this co	ommand								
						Status			Availa	oility			
				Norma	l Mode Of	N, Idle Mo	de OFF,	Sleep OUT	Yes	S			
Register				Norma	al Mode O	N, Idle Mo	ode ON, S	Sleep OUT	Yes	S			
Availability				Partial	Mode ON	l, Idle Mo	de OFF, S	Sleep OUT	Yes	S			
_				Partia	l Mode Ol	N, Idle Mo	de ON, S	leep OUT	Yes	3			
						Sleep I	N		Yes	3			
Default													





8.3.25. Negative Gamma Correction (E1h)

E1h					NGAMCT	RL (Neg	ative Gar	nma Corre	ection)				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	0	0	0	0	1	E1h
1 st Parameter	1	1	1	XX	0	0	0	0		VN63	[3:0]		08
2 nd Parameter	1	1	1	XX	0	0			VN62	[5:0]			
3 rd Parameter	1	1	↑	XX	0	0			VN61	[5:0]			
4 th Parameter	1	1	↑	XX	0	0	0	0		VN59	[3:0]		07
5 th Parameter	1	1	1	XX	0	0	0		V	'N57 [4:0]			
6 th Parameter	1	1	1	XX	0	0	0	0		VN50	[3:0]		05
7 th Parameter	1	1	1	XX	0			,	/N43 [6:0]				
8 th Parameter	1	1	1	XX		VN3	6 [3:0]			VN27	[3:0]		
9 th Parameter	1	1	1	XX	0			,	/N20 [6:0]				
10 th Parameter	1	1	↑	XX	0	0	0	0		VN13	[3:0]		04
11 th Parameter	1	1	↑	XX	0	0	0		\	VN6 [4:0]			
12 th Parameter	1										0F		
13 th Parameter	1	1	↑	XX									
14 th Parameter	1	1	↑	XX	0	0			VN1				
15 th Parameter	1	1	1	XX									0F
Description	Set the	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.											
Restriction	EXTC	should b	oe high to	o enable this co	mmand								
						Status			Availal	oility			
				Normal	Mode Of			Sleep OUT	_				
Register								Sleep OUT					
Availability								Sleep OUT					
Atvailability								leep OUT	Yes				
						Sleep I		'	Yes				
Default													





8.3.26. Digital Gamma Control 1 (E2h)

E2h					DGAM	CTRL (Di	gital Gam	ma Co	ontro	l 1)					
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4		D3	D2	D1	D0	HEX	
Command	0	1	1	XX	1	1	1	0		0	0	1	0	E2h	
1 st Parameter	1	1	1	XX		RCA	0 [3:0]				BC	A0 [3:0]		XX	
:	1	1	1	XX		RCA	x [3:0]				BC	Ax [3:0]		XX	
16 th Parameter	1	1	1	XX		RCA1	5 [3:0]				BCA	15 [3:0]		XX	
Description				-	ment registe ment registe		-								
Restriction	EXTC :	TC should be high to enable this command													
		Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes													
Register				Nor	mal Mode O	N, Idle Mo	de ON, S	leep C	TUC	Ye	es				
Availability				Par	tial Mode ON	I, Idle Mo	de OFF, S	leep C	DUT	Ye	es				
				Par	tial Mode Of	N, Idle Mo	de ON, S	еер О	UT	Ye	es				
						Sleep I	N			Ye	es				
								Default	t Valu	10	1				
					Stat	us	RCAx			Ax [3:0]					
Default					Power ON	Sequence	тв	D	-	TBD					
					SW R	leset	ТВ	D	-	TBD					
					HW F	leset	TB	D	-	TBD					





8.3.27. Digital Gamma Control 2(E3h)

E3h					DGAM	CTRL (Dig	ital Gan	nma C	ontro	l 2)						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	ļ.	D3	D2	D1	D0	HEX		
Command	0	1	1	XX	1	1	1	0		0	0	1	1	E3h		
1 st Parameter	1	1	1	XX		RFA0	[3:0]				BF	A0 [3:0]		XX		
:	1	1	1	XX		RFAx	[3:0]				BF	Ax [3:0]		XX		
64 rd Parameter	1	1	1	XX		RFA6	3 [3:0]				BFA	(63 [3:0]		XX		
Description				icro-adjustm icro-adjustm												
Restriction	EXTC s	should b	e high to	n to enable this command												
					Status Availability Normal Mode ON, Idle Mode OFF, Sleep OUT Yes											
Register										Ye						
negistei					nal Mode Ol					Ye						
Availability					al Mode ON						es					
				Part	ial Mode ON	•		leep C	UT	Ye						
						Sleep IN	<u> </u>			Y€	es					
								Defaul	t Valu	е						
				Status RFAx [3:0] BFAx [3:0]												
Default				Ī	Power ON	Sequence				TBD						
				Ī	SW F		TE	3D	Т	ΓBD						
					HW F	Reset	TE	3D	1	ΓBD						





8.3.28. Interface Control (F6h)

F6h	IFCTL (16bits Data Format Selection)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	XX	1	1	1	1	0	1	1	0	F6h
1 st Parameter	1	1	1	XX	MY_ EOR	MX_ EOR	MV_ EOR	0	BGR_ EOR	0	0	WE MODE	01
2 nd Parameter	1	1	1	XX	0	0	EPF [1]	EPF [0]	0	0	MDT [1]	MDT [0]	00
3 rd Parameter	1	1	1	XX	0	0	ENDIAN	0	DM [1]	DM [0]	RM	RIM	00

MY_EOR / MX_EOR / MV_EOR / BGR_EOR:

The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.

MDT [1:0]: Select the method of display data transferring.

WEMODE: Memory write control

WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.

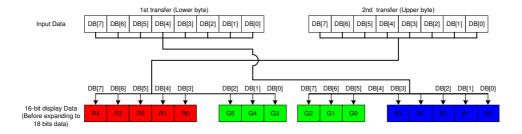
WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.

ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.

ENDIAN	Data transfer Mode					
0	Normal (MSB first, default)					
1	Little Endian (LSB first)					

Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.

Description



DM [1:0]: Select the display operation mode.

[OM [1]	DM [0]	Display Operation Mode					
	0	0	Internal clock operation					
	0	1	RGB Interface Mode					
	1	0	VSYNC interface mode					
	1	1	Setting disabled					

The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode.

However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.





RM: Select the interface to access the GRAM.

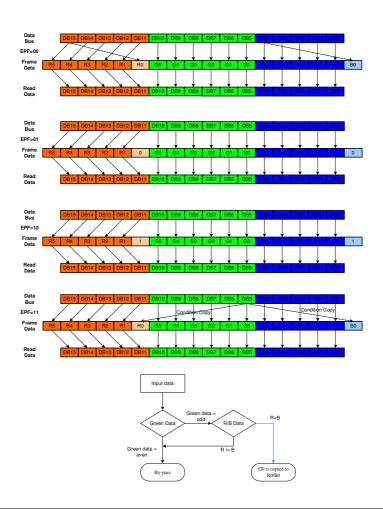
Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
0	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
1	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]: 65K color mode data format.



EPF [1:0]	Expand 16 bbp (R,G,B) to 18bbp (R,G,B)
00	MSB is inputted to LSB r [5:0] = {R [4:0], R [4]} g [5:0] = {G [5:0]} b [5:0] = {B [4:0], B [4]}





		r [5:0] = g [5:0] : b [5:0] : 01 Excepti R [4:0],	: {R = {G = {B ion: B[4	3 [4:0], 0}	5:0], b[5:0] = 6'	h3F							
		r [5:0] = g [5:0] = b [5:0] = Excepti	= {R = {G = {B	[4:0], 1} G [5:0]} G [4:0], 1}	5:0], b[5:0] = 6'	h00							
		Case 1 Case 2 Case 3	Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B \rightarrow r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]} Case 2: R=B \neq G \rightarrow r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 3: R=G \neq B \rightarrow r [5:0] = {R [4:0], G [0]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], B [0]} Case 4: B=G \neq R \rightarrow r [5:0] = {R [4:0], R [4]}, g [5:0] = {G [5:0]}, b [5:0] = {B [4:0], G [0]}										
Restriction	EXTC	should be high to ena	able	e this command									
					Status		Availab						
Register			ŀ	Normal Mode Of									
Availability			-		N, Idle Mode ON, Sleep OUT Yes N, Idle Mode OFF, Sleep OUT Yes								
				Partial Mode Of									
			L		Sleep IN		Yes						
						Defaul	t Value						
		Status		EPF [1:0]	MDT [1:0]	ENDIAN	WEMODE	DM [1:0]	RM	RIM			
Default		Power ON Seque	nce	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0			
		SW Reset		2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0			
		HW Reset		2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0			
											· 		

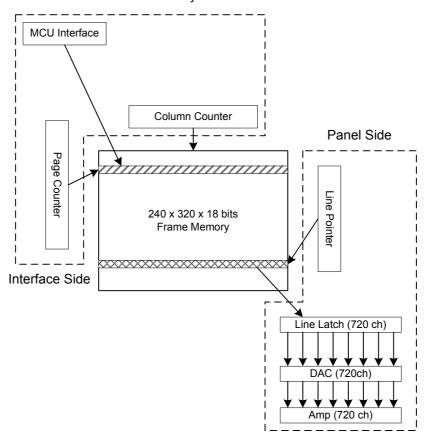




9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.





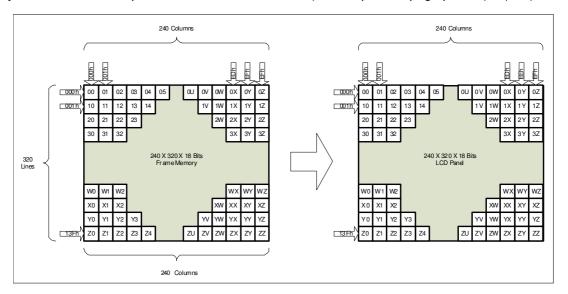


9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)





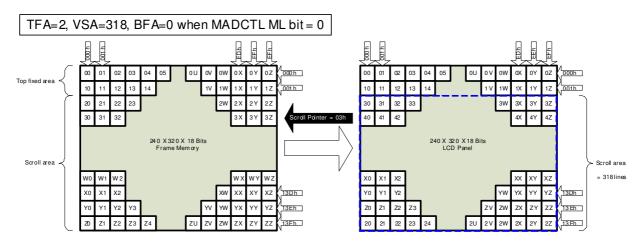


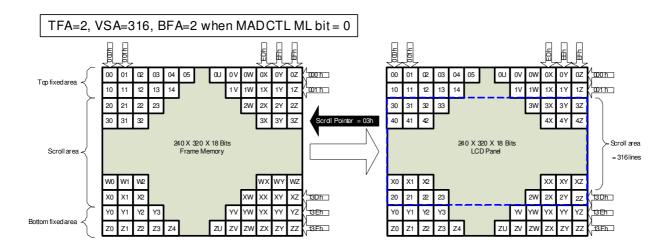


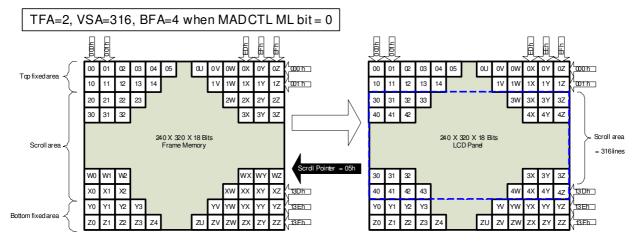
9.2.2. Vertical Scroll Mode

There is a vertical scrolling mode, which is determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

The Vertical Scroll Mode function is explained by these examples in the following.







Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.





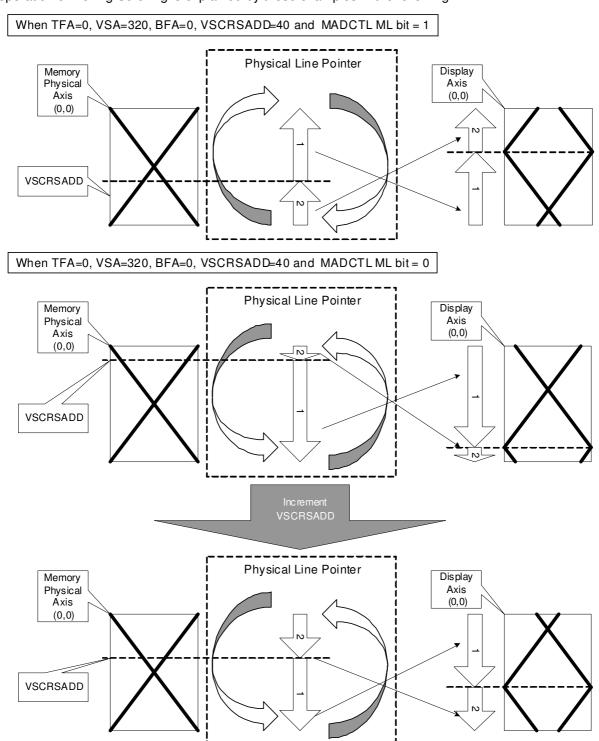
9.2.3. Vertical Scroll Example

9.2.4. Case1: TFA+VSA+BFA < 320

This setting is prohibited, unless unexpected picture will be shown.

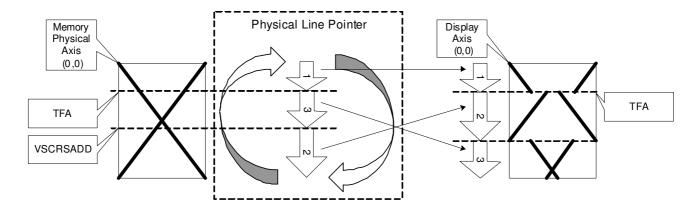
9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

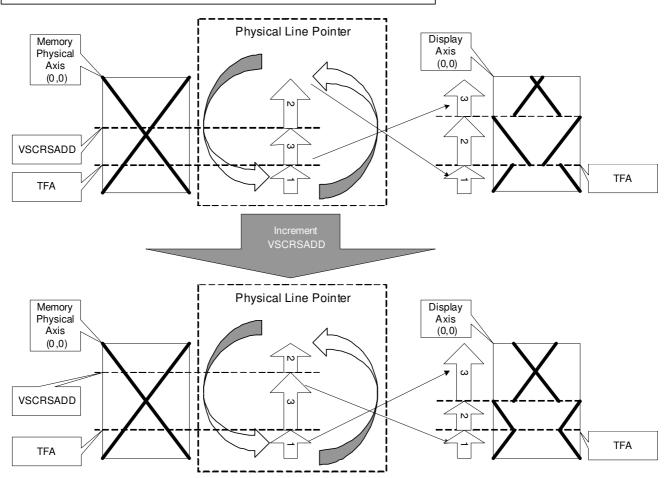




When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



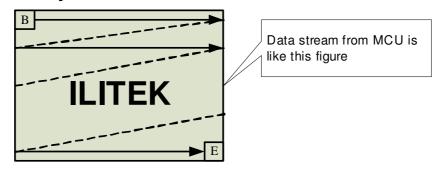
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



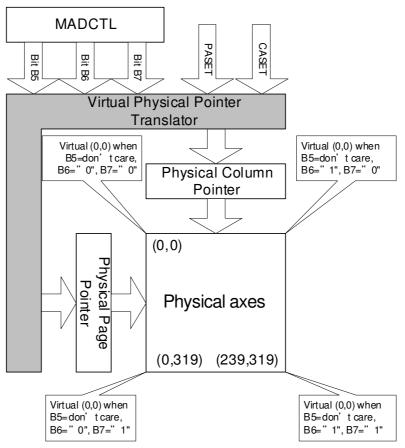




9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET			PASET			
0	0	0	Direct to Physical Column F	Pointer	Direct to Phy	ect to Physical Page Pointer			
0	0	1	Direct to Physical Column F	Pointer	Direct to (319-Physical Page Pointer)				
0	1	0	Direct to (239-Physical Col	umn Pointer)	Direct to Phy	sical Page Pointer			
0	1	1	Direct to (239-Physical Col	umn Pointer)	Direct to (319	9-Physical Page Pointer)			
1	0	0	Direct to Physical Page Poi	inter	Direct to Phy	sical Column Pointer			
1	0	1	Direct to (319-Physical Pag	je Pointer)	Direct to Physical Column Pointer				
1	1	0	Direct to Physical Page Poi	inter	Direct to (239-Physical Column Pointer)				
1	1	1	Direct to (319-Physical Pag	je Pointer)	Direct to (239-Physical Column Pointer)				
		Coi	ndition	Column	Counter	Page counter			
Whe	n RAMW	R/RAMF	RD command is accepted	Return to "Sta	art column"	Return to "Start Page"			
	Comple	ete Pixel	Read/Write action	Increment by	1	No change			
The (Column v	/alues is	large than "End Column"	Return to "Start column"		Increment by 1			
The	e Page c	ounter is	large than "End Page"	Return to "Start column" Return to "Start Page"					





Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

Display Data MADCTR Parameter		'R er	Image in the Memory	Image in the Driver (Frame Memory)					
Direction	MV	MX	MY	(MPU)	image in the Driver (Frame Memory)				
Normal	0	0	0	B	Memory(0,0) B Counter(0,0) E E				
Y-Mirror	0	0	1	B	Memory(0.0) E Counter(0.0)				
X-Mirror	0	1	0	B	Memory(0,0) B Counter(0,0)				
X-Mirror Y-Mirror	0	1	1	B	Memory(0,0) E Counter(0,0)				
X-Y Exchange	1	0	0	B	Memor(0,0) B Counter(0,0)				
X-Y Exchange Y-Mirror	1	0	1	B	Memory(0,0) E				
XY Exchange X-Mirror	1	1	0	B	Memory(0,0) B Counter(0,0)				
XY Exchange XY-Mirror	1	1	1	B	Memory(0,0) E Counter(0,0)				





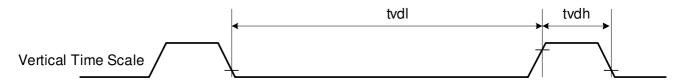
10. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

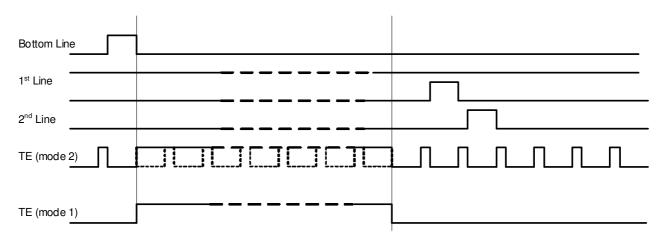
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

thdl = The LCD display is updated from the Frame Memory (except Invisible Line - see above).



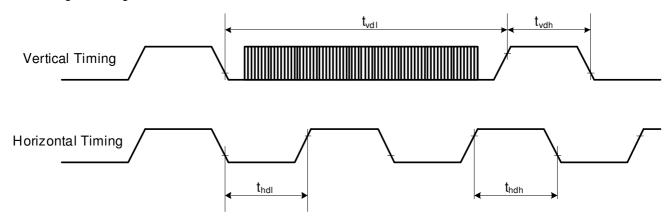
Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.





10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

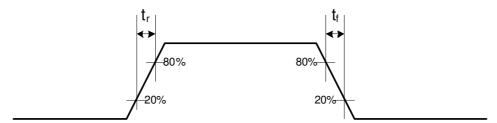


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Тур.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration				ms	
$t_{\rm vdh}$	Vertical timing high duration	1000			us	
t _{hdl}	Horizontal timing low duration				us	
t _{hdh}	Horizontal timing high duration			500	us	

Note:

- 1. The timings in Table as above apply when MADCTL B4=0 and B4=1
- 2. The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.





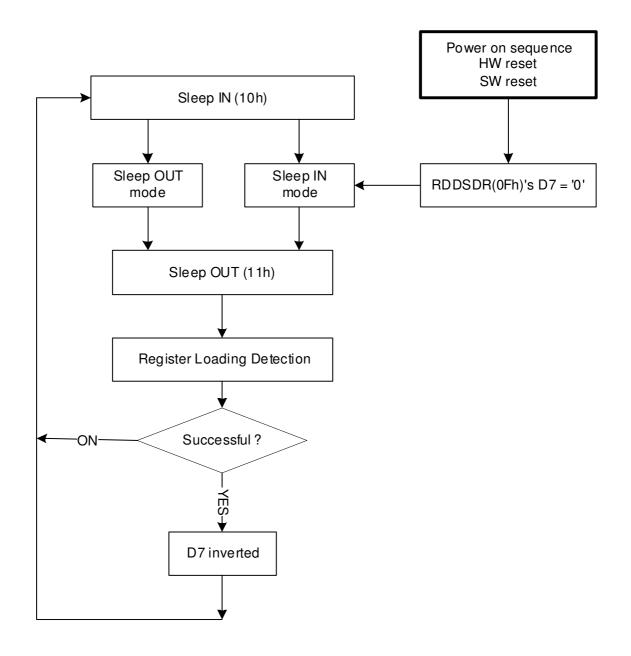
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

11.1. Register loading Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:





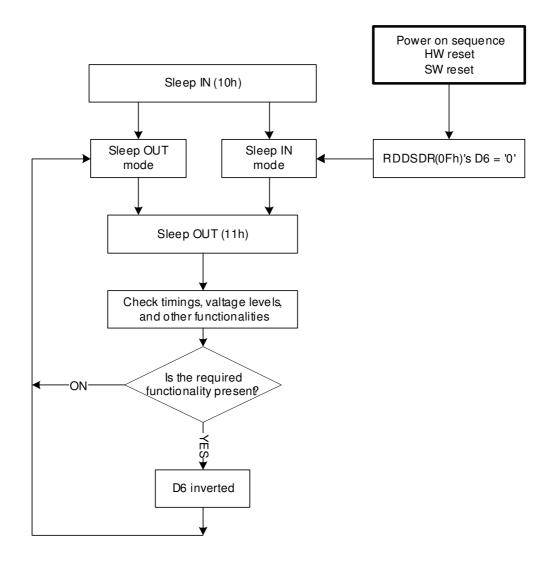


11.2. Functionality Detection

Sleep Out-command (Command "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command "Read Display Self- Diagnostic Result (0Fh)" (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if User's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.





12. Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

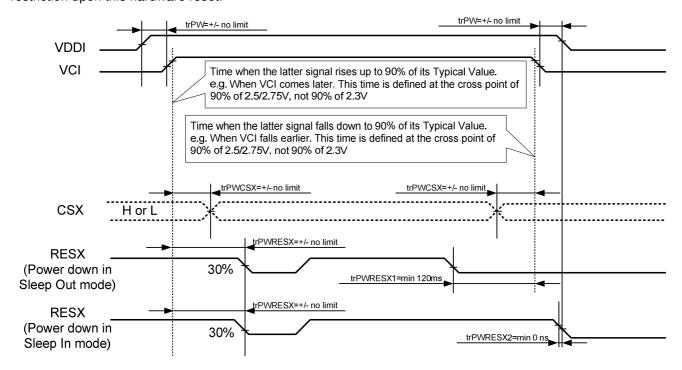
During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

- Note 1: There will be no damage to the display module if the power sequences are not met.
- Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
- Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
- Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode trPWRESX2 is applied to RESX falling in the Sleep In Mode

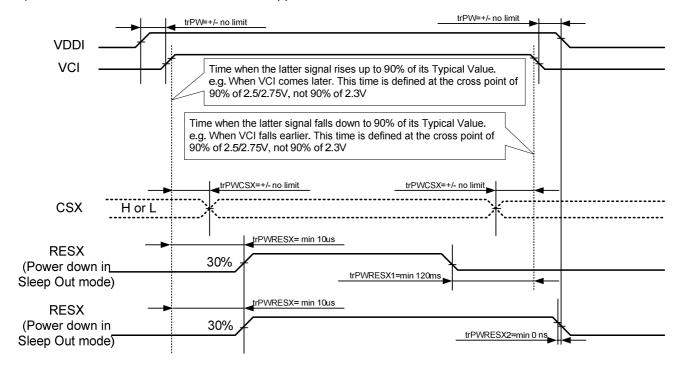
Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.





12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and VDDI have been applied.



trPWRESX1 is applied to RESX falling in the Sleep Out Mode trPWRESX2 is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.





12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9341 will force the display to blank and will not be any abnormal visible effects with in 1 second on the display and remains blank until "Power On Sequence" actives.





13. Power Level Definition

13.1. Power Levels

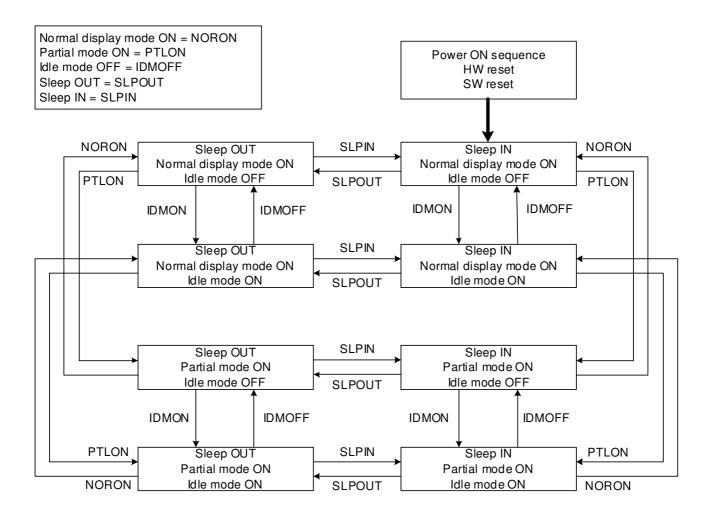
7 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

- 1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
 - In this mode, the display is able to show maximum 262,144 colors.
- 2. Partial Mode On, Idle Mode Off, Sleep Out.
 - In this mode part of the display is used with maximum 262,144 colors.
- 3. Normal Mode On (full display), Idle Mode On, Sleep Out.
 - In this mode, the full display area is used but with 8 colors.
- 4. Partial Mode On, Idle Mode On, Sleep Out.
 - In this mode, part of the display is used but with 8 colors.
- 5. Sleep In Mode.
 - In this mode, the DC: DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
- 6. Deep Standby Mode.
 - In Deep Standby mode, both internal logic power and SRAM power are turn off, the display data stored in the Frame Memory and the instructions are not saved. Rewrite Frame Memory content and instructions after the Deep Standby Mode is exited.
- 7. Power Off Mode.
 - In this mode, both VCI and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.



13.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.





14. Gamma Curves Selection

ILI9341 provide one gamma curve Gamma2.2. The gamma curve can be selected by the GC0 settings.

14.1. Gamma Default Values (for NW type LC)

	(101		Voltage	
Data	VCOM :		VCOM =	= High
Data	Gamma	2.2	Gamma	2.2
0	VOP			
0		4.084	VON	0.277
1	V1P	4.015	V1N	0.346
2	V2P	3.843	V2N	0.482
3	V3P	3.681	V3N	0.629
4	V4P	3.518	V4N	0.776
5	V5P	3.445	V5N	0.924
6	V6P	3.371	V6N	1.071
7	V7P	3.285	V7N	1.157
8	V8P	3.199	V8N	1.242
9	V9P	3.128	V9N	1.314
10	V10P	3.056	V10N	1.385
11	V11P	2.985	V11N	1.456
12	V12P	2.928	V12N	1.513
13	V12P	2.871	V12N	1.570
14	V131 V14P	2.802	V13N	
				1.619
15	V15P	2.733	V15N	1.668
16	V16P	2.674	V16N	1.710
17	V17P	2.615	V17N	1.753
18	V18P	2.557	V18N	1.795
19	V19P	2.508	V19N	1.830
20	V20P	2.458	V20N	1.865
21	V21P	2.425	V21N	1.899
22	V22P	2.391	V22N	1.932
23	V23P	2.357	V23N	1.966
24	V24P	2.323	V24N	2.000
25	V25P	2.289	V25N	2.034
26	V26P	2.256	V26N	2.068
27	V27P	2.222	V27N	2.102
28	V271 V28P	2.193	V27N	2.129
29	V29P	2.165	V29N	2.155
30	V30P	2.136	V30N	2.182
31	V31P	2.108	V31N	2.208
32	V32P	2.080	V32N	2.235
33	V33P	2.051	V33N	2.262
34	V34P	2.023	V34N	2.288
35	V35P	1.994	V35N	2.315
36	V36P	1.966	V36N	2.342
37	V37P	1.942	V37N	2.368
38	V38P	1.917	V38N	2.395
39	V39P	1.893	V39N	2.421
40	V40P	1.869	V40N	2.448
41	V41P	1.845	V41N	2.475
42	V41P	1.820	V41N	2.501
43	V42F V43P	1.796	V42N V43N	2.528
43	V43P V44P		V43N V44N	
45	V44P V45P	1.776 1.755	V44N V45N	2.549
46	V46P	1.730	V46N	2.597
47	V47P	1.706	V47N	2.623
48	V48P	1.681	V48N	2.649
49	V49P	1.653	V49N	2.679
50	V50P	1.624	V50N	2.710
51	V51P	1.598	V51N	2.735
52	V52P	1.573	V52N	2.761
53	V53P	1.541	V53N	2.793
54	V54P	1.508	V54N	2.825
55	V55P	1.476	V55N	2.857
56	V56P	1.438	V56N	2.895
57	V50F V57P	1.400	V50N V57N	2.933
58	V58P	1.359	V58N	2.982
59	V59P	1.319	V59N	3.031
60	V60P	1.246	V60N	3.109
61	V61P	1.173	V61N	3.186
62	V62P	1.070	V62N	3.289
63	V63P	0.279	V63N	4.083

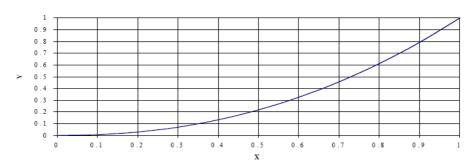




14.2. Gamma Curves

14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$



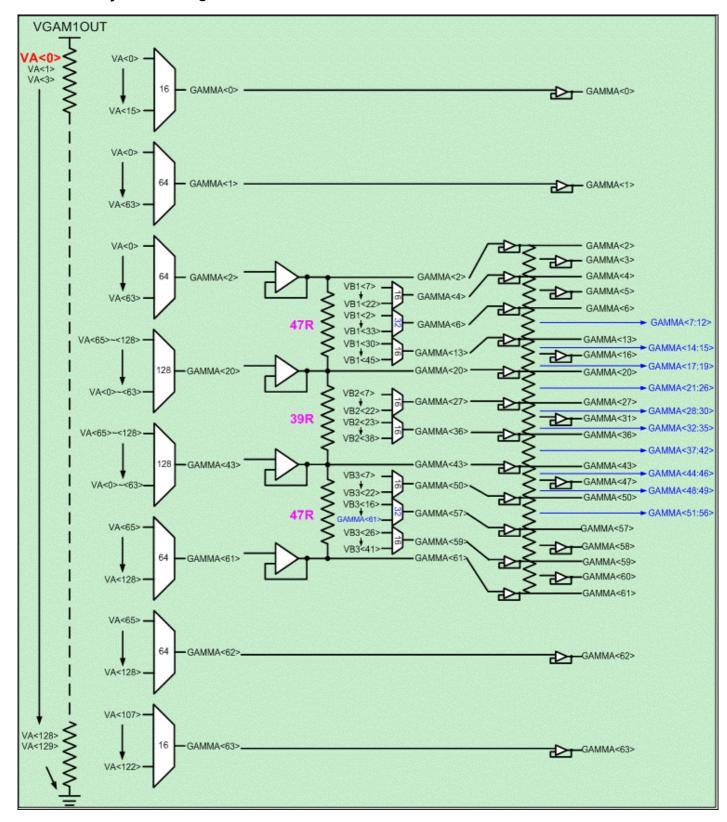






14.3. Gamma Curves

14.3.1. Grayscale Voltage Generation







14.3.2. Positive Gamma Correction

Gamma	Value "X"	Formula		
Level VP0	in Formula VP0[3:0]	(VREG1-VGS)*(130R-X*R)/130R		
VP1	VP0[3.0] VP1[5:0]	(VREG1-VGS) (130R-X*R)/130R (VREG1-VGS)*(130R-X*R)/130R		
VP2	VP2[5:0]	(VREG1-VGS) (130R-X R)/130R (VREG1-VGS)*(130R-X*R)/130R		
VP3	— —	(VP2-VP4)*35R/(35R*2)+VP4		
VP4	VP4[3:0]	(VP2-VP20)*(47R-X*R-7R)/47R+VP20		
VP5		(VP4-VP6)*35R/(35R*2)+VP6		
VP6	VP6[4:0]	(VP2-VP20)*(47R-X*R-2R)/47R+VP20		
VP7		(VP6-VP13)*(12R+10R*3+8R*2)/(12R*2+10R*3+8R*2)+VP13		
VP8		(VP6-VP13)*(10R*3+8R*2)/(12R*2+10R*3+8R*2)+VP13		
VP9		(VP6-VP13)*(10R*2+8R*2)/(12R*2+10R*3+8R*2)+VP13		
VP10		(VP6-VP13)*(10R+8R*2)/(12R*2+10R*3+8R*2)+VP13		
VP11	<u> </u>	(VP6-VP13)*(8R*2)/(12R*2+10R*3+8R*2)+VP13		
VP12	_	(VP6-VP13)*8R/(12R*2+10R*3+8R*2)+VP13		
VP13	VP13[3:0]	(VP2-VP20)*(47R-X*R-30R)/47R+VP20		
VP14		(VP13-VP20)*(14R+12R*3+10R*2)/(14R*2+12R*3+10R*2)+VP20		
VP15		(VP13-VP20)*(12R*3+10R*2)/(14R*2+12R*3+10R*2)+VP20		
VP16		(VP13-VP20)*(12R*2+10R*2)/(14R*2+12R*3+10R*2)+VP20		
VP17	_	(VP13-VP20)*(12R+10R*2)/(14R*2+12R*3+10R*2)+VP20		
VP18		(VP13-VP20)*(10R*2)/(14R*2+12R*3+10R*2)+VP20		
VP19		(VP13-VP20)*10R/(14R*2+12R*3+10R*2)+VP20		
VP20	VP20[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R		
\/D04	. ,	>=64 (VREG1-VGS)*(130R-X*R-1R)/130R		
VP21	_	(VP20-VP27)*(12R*6)/(12R*7)+VP27		
VP22	_	(VP20-VP27)*(12R*5)/(12R*7)+VP27		
VP23	<u> </u>	(VP20-VP27)*(12R*4)/(12R*7)+VP27		
VP24	_	(VP20-VP27)*(12R*3)/(12R*7)+VP27		
VP25		(VP20-VP27)*(12R*2)/(12R*7)+VP27		
VP26 VP27		(VP20-VP27)*12R/(12R*7)+VP27		
VP28	VP27[3:0]	(VP20-VP43)*(39R-X*R-7R)/39R+VP43		
VP29		(VP27-VP36)*(8R*8)/(8R*9)+VP36		
VP30		(VP27-VP36)*(8R*7)/(8R*9)+VP36 (VP27-VP36)*(8R*6)/(8R*9)+VP36		
VP31	_	(VP27-VP36)*(8R*5)/(8R*9)+VP36		
VP32		(VP27-VP36)*(8R*4)/(8R*9)+VP36		
VP33		(VP27-VP36)*(8R*3)/(8R*9)+VP36		
VP34	_	(VP27-VP36)*(8R*2)/(8R*9)+VP36		
VP35	_	(VP27-VP36)*8R/(8R*9)+VP36		
VP36	VP36[3:0]	(VP20-VP43)*(39R-X*R-23R)/39R+VP43		
VP37	—	(VP36-VP43)*(12R*6)/(12R*7)+VP43		
VP38	_	(VP36-VP43)*(12R*5)/(12R*7)+VP43		
VP39	_	(VP36-VP43)*(12R*4)/(12R*7)+VP43		
VP40	_	(VP36-VP43)*(12R*3)/(12R*7)+VP43		
VP41	_	(VP36-VP43)*(12R*2)/(12R*7)+VP43		
VP42	_	(VP36-VP43)*12R/(12R*7)+VP43		
VP43	VD43[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R		
VF43	VP43[6:0]	>=64 (VREG1-VGS)*(130R-X*R-1R)/130R		
VP44		(VP43-VP50)*(14R*2+12R*3+10R)/(14R*2+12R*3+10R*2)+VP50		
VP45		(VP43-VP50)*(14R*2+12R*3)/(14R*2+12R*3+10R*2)+VP50		
VP46		(VP43-VP50)*(14R*2+12R*2)/(14R*2+12R*3+10R*2)+VP50		
VP47		(VP43-VP50)*(14R*2+12R)/(14R*2+12R*3+10R*2)+VP50		
VP48		(VP43-VP50)*(14R*2)/(14R*2+12R*3+10R*2)+VP50		
VP49	<u> </u>	(VP43-VP50)*14R/(14R*2+12R*3+10R*2)+VP50		
VP50	VP50[3:0]	(VP43-VP61)*(47R-X*R-7R)/47R+VP61		
VP51	_	(VP50-VP57)*(12R*2+10R*3+8R)/(12R*2+10R*3+8R*2)+VP57		
VP52	-	(VP50-VP57)*(12R*2+10R*3)/(12R*2+10R*3+8R*2)+VP57		
VP53	_	(VP50-VP57)*(12R*2+10R*2)/(12R*2+10R*3+8R*2)+VP57		
VP54		(VP50-VP57)*(12R*2+10R)/(12R*2+10R*3+8R*2)+VP57		
VP55	_	(VP50-VP57)*(12R*2)/(12R*2+10R*3+8R*2)+VP57		
VP56		(VP50-VP57)*12R/(12R*2+10R*3+8R*2)+VP57		
VP57	VP57[4:0]	(VP43-VP61)*(47R-X*R-16R)/47R+VP61		
VP58		(VP57-VP59)*35R/(35R*2)+VP59		
VP59 VP60	VP59[3:0]	(VP43-VP61)*(47R-X*R-26R)/47R+VP61		
VP60 VP61	— VP61[5:0]	(VP59-VP61)*35R/(35R*2)+VP61 (VREG1-VGS)*(65R-X*R)/130R		
VP62	VP61[5.0] VP62[5:0]	(VREG1-VGS) (65R-X*R)/130R		
VP63	VP63[3:0]	(VREG1-VGS) (65R-X R)/130R (VREG1-VGS)*(23R-X*R)/130R		
	VI 00[0.0]	(Tital) Too, (Edit-A Tyrioott		





14.3.3. Negative Gamma Correction

Gamma	Value "X"	Formula		
Level VN63	in Formula VN63[3:0]	(VREG1-VGS)*(130R-X*R)/130R		
VN62	VN62[5:0]	(VREG1-VGS)*(130R-X*R)/130R		
VN61	VN61[5:0]	(VREG1-VGS)*(130R-X*R)/130R		
VN60	— — — — — — — — — — — — — — — — — — —	(VN61-VN59)*35R/(35R*2)+VN59		
VN59 VN58	VN59[3:0]	(VN61-VN43)*(47R-X*R-7R)/47R+VN43 (VN59-VN57)*35R/(35R*2)+VN57		
VN57	VN57[4:0]	(VN61-VN43)*(47R-X*R-2R)/47R+VN43		
VN56	—	(VN57-VN50)*(12R+10R*3+8R*2)/(12R*2+10R*3+8R*2)+VN50		
VN55	_	(VN57-VN50)*(10R*3+8R*2)/(12R*2+10R*3+8R*2)+VN50		
VN54	_	(VN57-VN50)*(10R*2+8R*2)/(12R*2+10R*3+8R*2)+VN50		
VN53		(VN57-VN50)*(10R+8R*2)/(12R*2+10R*3+8R*2)+VN50		
VN52	_	(VN57-VN50)*(8R*2)/(12R*2+10R*3+8R*2)+VN50		
VN51 VN50		(VN57-VN50)*8R/(12R*2+10R*3+8R*2)+VN50		
VN49	VN50[3:0] —	(VN61-VN43)*(47R-X*R-30R)/47R+VN43 (VN50-VN43)*(14R+12R*3+10R*2)/(14R*2+12R*3+10R*2)+VN43		
VN48	_	(VN50-VN43)*(12R*3+10R*2)/(14R*2+12R*3+10R*2)+VN43		
VN47	_	(VN50-VN43)*(12R*2+10R*2)/(14R*2+12R*3+10R*2)+VN43		
VN46		(VN50-VN43)*(12R+10R*2)/(14R*2+12R*3+10R*2)+VN43		
VN45		(VN50-VN43)*(10R*2)/(14R*2+12R*3+10R*2)+VN43		
VN44		(VN50-VN43)*10R/(14R*2+12R*3+10R*2)+VN43		
VN43	VN43[6:0]	<64 (VREG1-VGS)*(130R-X*R)/130R		
VN42		>=64 (VREG1-VGS)*(130R-X*R-1R)/130R		
VN41		(VN43-VN36)*(12R*6)/(12R*7)+VN36 (VN43-VN36)*(12R*5)/(12R*7)+VN36		
VN40		(VN43-VN36)*(12R*4)/(12R*7)+VN36		
VN39	_	(VN43-VN36)*(12R*3)/(12R*7)+VN36		
VN38	_	(VN43-VN36)*(12R*2)/(12R*7)+VN36		
VN37	_	(VN43-VN36)*12R/(12R*7)+VN36		
VN36	VN36[3:0]	(VN43-VN20)*(39R-X*R-7R)/39R+VN20		
VN35	_	(VN36-VN27)*(8R*8)/(8R*9)+VN27		
VN34		(VN36-VN27)*(8R*7)/(8R*9)+VN27		
VN33		(VN36-VN27)*(8R*6)/(8R*9)+VN27		
VN32 VN31		(VN36-VN27)*(8R*5)/(8R*9)+VN27		
VN30		(VN36-VN27)*(8R*4)/(8R*9)+VN27 (VN36-VN27)*(8R*3)/(8R*9)+VN27		
VN29	_	(VN36-VN27)*(8R*2)/(8R*9)+VN27		
VN28	_	(VN36-VN27)*8R/(8R*9)+VN27		
VN27	VN27[3:0]	(VN43-VN20)*(39R-X*R-23R)/39R+VN20		
VN26	_	(VN27-VN20)*(12R*6)/(12R*7)+VN20		
VN25		(VN27-VN20)*(12R*5)/(12R*7)+VN20		
VN24	_	(VN27-VN20)*(12R*4)/(12R*7)+VN20		
VN23	_	(VN27-VN20)*(12R*3)/(12R*7)+VN20		
VN22 VN21		(VN27-VN20)*(12R*2)/(12R*7)+VN20		
	_	(VN27-VN20)*12R/(12R*7)+VN20 <64 (VREG1-VGS)*(130R-X*R)/130R		
VN20	VN20[6:0]	>=64 (VREG1-VGS)*(130R-X*R-1R)/130R		
VN19	_	(VN20-VN13)*(14R*2+12R*3+10R)/(14R*2+12R*3+10R*2)+VN13		
VN18	_	(VN20-VN13)*(14R*2+12R*3)/(14R*2+12R*3+10R*2)+VN13		
VN17	_	(VN20-VN13)*(14R*2+12R*2)/(14R*2+12R*3+10R*2)+VN13		
VN16		(VN20-VN13)*(14R*2+12R)/(14R*2+12R*3+10R*2)+VN13		
VN15 VN14		(VN20-VN13)*(14R*2)/(14R*2+12R*3+10R*2)+VN13		
VN13	VN13[3:0]	(VN20-VN13)*14R/(14R*2+12R*3+10R*2)+VN13 (VN20-VN2)*(47R-X*R-7R)/47R+VN2		
VN12	— —	(VN13-VN6)*(12R*2+10R*3+8R)/(12R*2+10R*3+8R*2)+VN6		
VN11	_	(VN13-VN6)*(12R*2+10R*3)/(12R*2+10R*3+8R*2)+VN6		
VN10	_	(VN13-VN6)*(12R*2+10R*2)/(12R*2+10R*3+8R*2)+VN6		
VN9	_	(VN13-VN6)*(12R*2+10R)/(12R*2+10R*3+8R*2)+VN6		
VN8		(VN13-VN6)*(12R*2)/(12R*2+10R*3+8R*2)+VN6		
VN7	<u> </u>	(VN13-VN6)*12R/(12R*2+10R*3+8R*2)+VN6		
VN6 VN5	VN6[4:0]	(VN20-VN2)*(47R-X*R-16R)/47R+VN2		
VN4	— VN4[3:0]	(VN6-VN4)*35R/(35R*2)+VN4 (VN20-VN2)*(47R-X*R-26R)/47R+VN2		
VN3	v14 - [5.0]	(VN4-VN2)*35R/(35R*2)+VN2		
VN2	VN2[5:0]	(VREG1-VGS)*(65R-X*R)/130R		
VN1	VN1[5:0]	(VREG1-VGS)*(65R-X*R)/130R		
VN0	VN0[3:0]	(VREG1-VGS)*(23R-X*R)/130R		





15. Reset

15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
ldle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's B5=0:00EF h If MADCTL's B5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's B5 = 0:013F h If MADCTL's B5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	013F h	013F h	013F h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

- Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.
- Note 2: After Powered-On Reset finishes within 10µs after both VCI & VDDI are applied.
- Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.
- Note 4: When a RESX input is entered into the ILI9341 while it is in deep standby mode, the ILI9341 starts up the inside logic regulator and makes a transition to the initial state. During this period, the state of the interface pins may become unstable.





15.2. Output Pins, I/O Pins

	After Power ON	After Hardware Reset	After Software Reset	
TE line	Low	Low	Low	
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)	

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

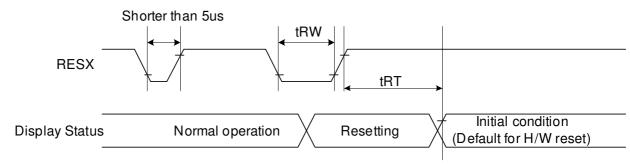
15.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid





15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	+DT	Depart samuel		5 (note 1,5)	mS
	tRT	Reset cancel		120 (note 1,6,7)	mS

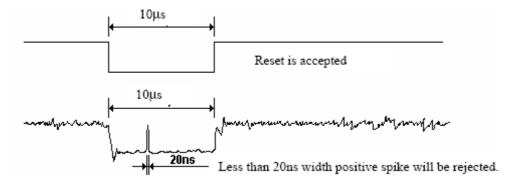
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

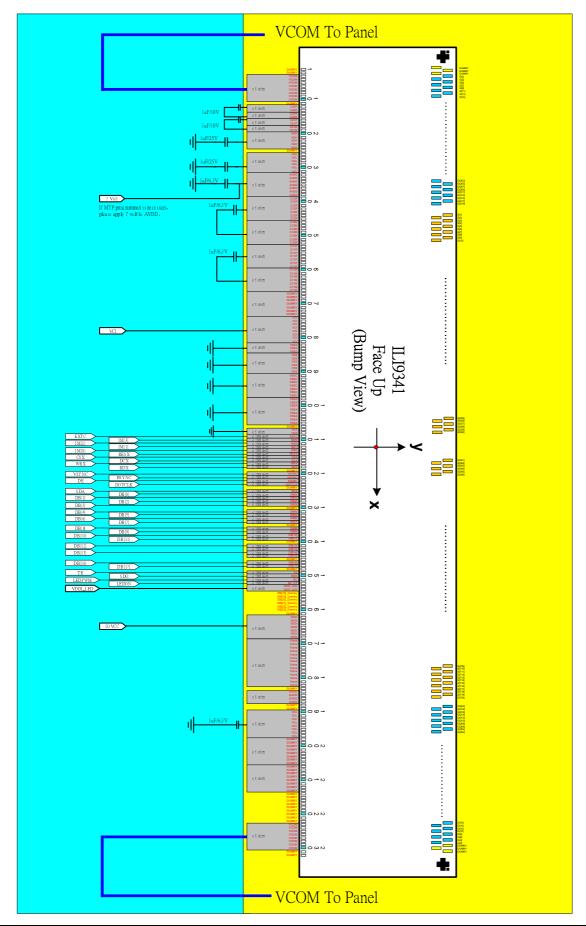


- Note 5: When Reset applied during Sleep In Mode.
- Note 6: When Reset applied during Sleep Out Mode.
- Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.





16. Configuration of Power Supply Circuit



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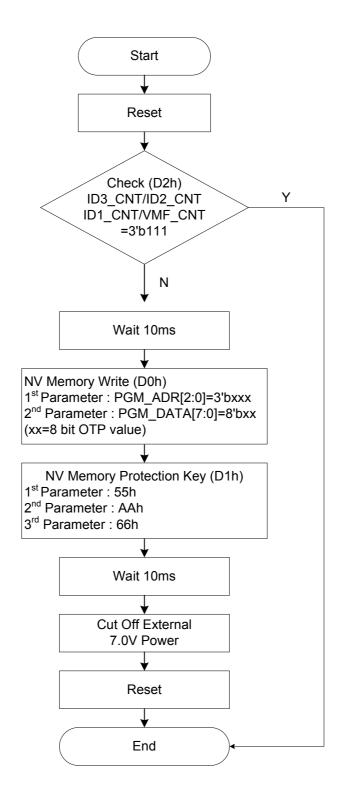
The Following tables shows specifications of external elements connected to the ILI9341's power supply circuit.

Items	Recommended Specification	Pin connection
Canaaihu	6.3V	AVDD ,VCL,C11P/M,C12P/M,
Capacity 1 µF (B characteristics)	10V	C21P/M,C22P/M
	25V	VGL, VGH



ILI9341

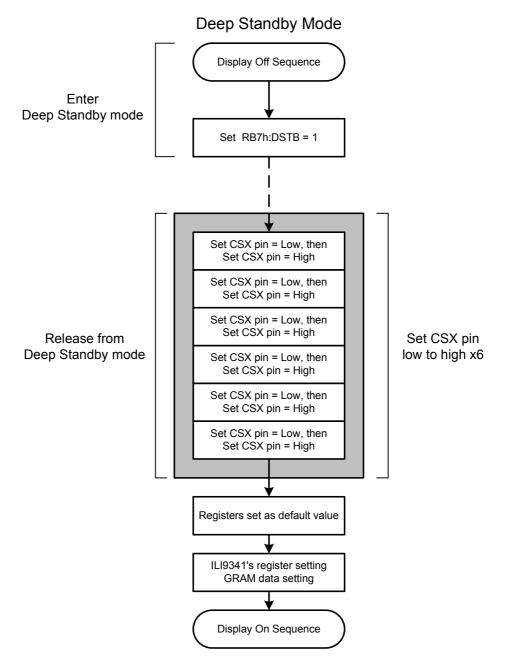
17. NV Memory Programming Flow







18. Deep Standby Mode Setting



Note: (1) To Return display mode according to normal display ON sequence when ILI9341 exits Deep standby mode to Sleep mode.

- (2) Leave at lease 1ms between the 2nd and 3rd inputs of CSX=Low.
- (3) This sequence must be completed before writing data to GRAM.
- (4) ILI9341 exits deep standby mode and enters to sleep mode when an effective RESX pulse is inputted during Deep Standby mode.







19. Electrical Characteristics

19.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9341 is used out of the absolute maximum ratings, ILI9341 may be permanently damaged. To use ILI9341 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9341 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ + <mark>2.0</mark>
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	$^{\circ}\mathbb{C}$	-40 ~ +85
Storage temperature	Tstg	$^{\circ}\!\mathbb{C}$	-55 ~ +110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.





19.2. DC Characteristics

19.2.1. General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Тур.	Max.	Note
Power and Operation V	oltage						
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	VGH-VGL	19	-	32	Note3
Input and Output		1					
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	VCOMH-VCOML	4.0	-	5.5	Note3
Source Driver				T		T	
Source Output Range	Vsout	V	-	0.1	-	AVDD-0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3
Output Deviation Voltage (Source	Vdev	mV	Sout>=4.2V Sout<=0.8V	-	-	20	Note4
Output channel)		, , ,	4.2V>Sout>0.8V	-	-	15	
Output Offset Voltage	VOFSET	mV	-	-	-	35	Note7
Booster Operation	<u> </u>	1		4.05			<u> </u>
1 st Booster (VCIx2) Voltage	AVDD	V	-	4.95 (Note 5)	-	5.5 (Note 6)	Note3
1 st Booster (VClx2 Drop Voltage	VCIx2 drop	%	loading=1mA	-	-	5	Note3
Liner Range	Vliner	V	-	0.2	-	AVDD-0.2	

Note 1: VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage) \mathcal{C} .

Note2: Please supply digital VDDI voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,

IM0, and Test pins.

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Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

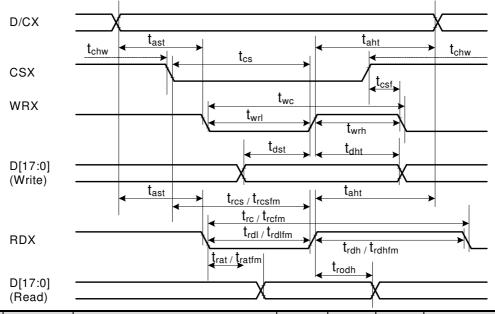
Note5: VCI=2.6V Note6: VCI=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value



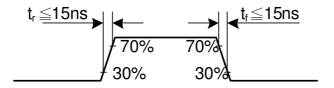
19.3. AC Characteristics

19.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)



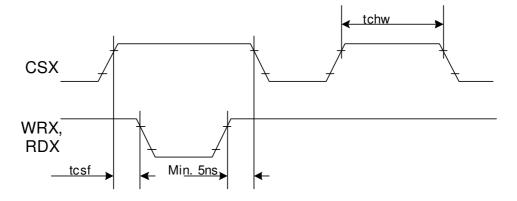
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
DCX	taht	Address hold time (Write/Read)	0	-	ns	
	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
CSX	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
	twc	Write cycle	66	-	ns	
WRX	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
	trcfm	Read Cycle (FM)	450	-	ns	
RDX (FM)	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
	trc	Read cycle (ID)	160	-	ns	
RDX (ID)	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[47.0]	tdst	Write data setup time	10	-	ns	
D[17:0],	tdht	Write data hold time	10	-	ns	For manifesture OL 20m F
D[15:0], D[8:0],	trat	Read access time	-	40	ns	For maximum CL=30pF For minimum CL=8pF
D[8.0], D[7:0]	tratfm	Read access time	-	340	ns	For minimum CL=opr
ره. ۱ ال	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V



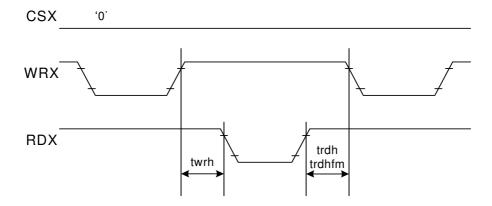


CSX timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

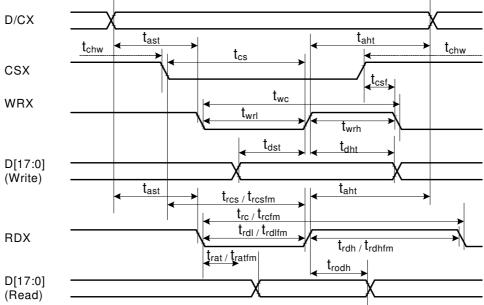
Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

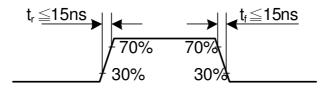


19.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080- II system)



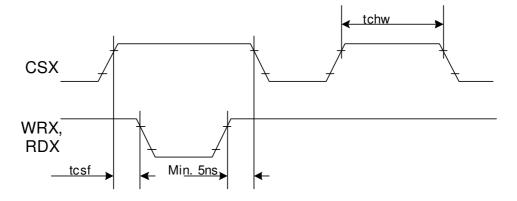
(1		
Signal	Symbo I	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
DCX	taht	Address hold time (Write/Read)	0	-	ns	
	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
CSX	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
	twc	Write cycle	66	-	ns	
WRX	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
	trcfm	Read Cycle (FM)	450	-	ns	
RDX (FM)	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
	trc	Read cycle (ID)	160	-	ns	
RDX (ID)	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[47.0]	tdst	Write data setup time	10	-	ns	
D[17:0], D[17:10]&D[8:1],	tdht	Write data hold time	10	-	ns	For movimum CL 20nF
	trat	Read access time	-	40	ns	For maximum CL=30pF For minimum CL=8pF
D[17:10], D[17:9]	tratfm	Read access time	-	340	ns	For minimum CL=opF
D[17.3]	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.



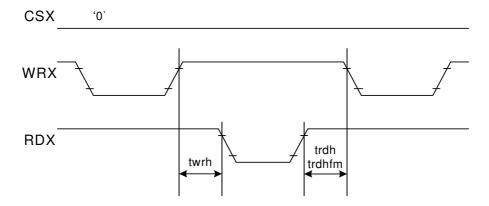


CSX timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:

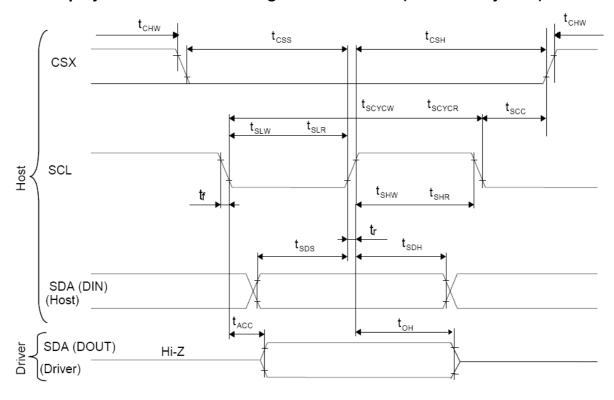


Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.



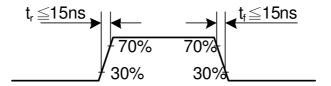


19.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)



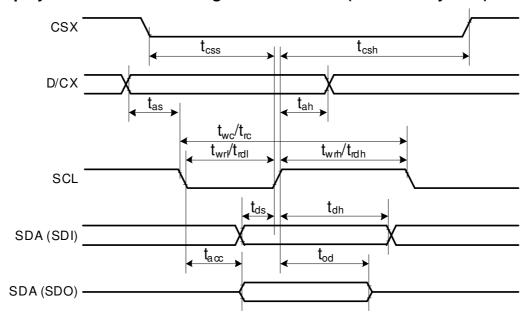
Signal	Symbol	Parameter	min	max	Unit	Description
	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
SCL	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
SCL	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI	tsds	Data setup time (Write)	30	-	ns	
(Input)	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO	tacc	Access time (Read)	10	-	ns	
(Output)	toh	Output disable time (Read)	10	50	ns	
	tscc	SCL-CSX	20	-	ns	
CSX	tchw	CSX "H" Pulse Width	40	-	ns	
037	tcss	CSX-SCL Time	60	-	ns	
	tcsh	COA-OCL TITLE	65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



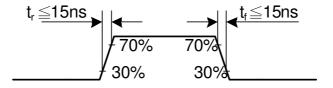


19.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)



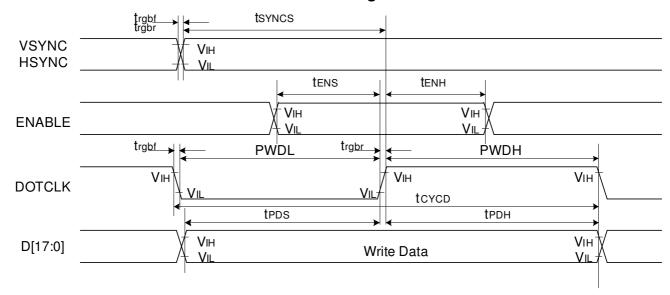
Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
USA	tcsh	Chip select hold time (Read)	40	-	ns	
	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
SCL	twrl	SCL "L" pulse width (Write)	40	-	ns	
SCL	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
D/GX	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI	tds	Data setup time (Write)	30	-	ns	
(Input)	tdh	Data hold time (Write)	30	-	ns	
SDA/SDO	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
(Output)	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: $Ta = 25 \, ^{\circ}$ C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



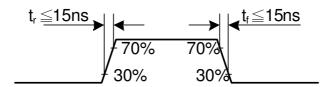


19.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC /	tsyncs	VSYNC/HSYNC setup time	15	-	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	t _{ENS}	DE setup time	15	-	ns	
DE	t _{ENH}	DE hold time	15	-	ns	
D[17:0]	t _{POS}	Data setup time	15	-	ns	18/16-bit bus RGB
D[17.0]	t _{PDH}	Data hold time	15	-	ns	interface mode
	PWDH	DOTCLK high-level period	15	-	ns	
DOTCLK	PWDL	DOTCLK low-level period	15	-	ns	
DOTOLK	tcycd	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC /	t _{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	
HSYNC	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	t _{ENS}	DE setup time	15	-	ns	
DE	t _{ENH}	DE hold time	15	-	ns	
D[17:0]	t _{POS}	Data setup time	15	-	ns	6-bit bus RGB
D[17:0]	t _{PDH}	Data hold time	15	-	ns	interface mode
	PWDH	DOTCLK high-level pulse period	15	-	ns	
DOTCLK	PWDL	DOTCLK low-level pulse period	15	-	ns	
DOTOLK	tcycd	DOTCLK cycle time	100	-	ns	
	t _{rgbr} , t _{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V







20. Revision History

Version No.	Date	Page	Description
V1.00	2010/10/12	All	New Created.
V1.01	2010/10/12	179	Update charge pump ratio
V1.02	2010/1206	All	Rename 9341