TRANSIENT ELECTRO-THERMAL ANALYSIS OF TRACTION INVERTERS

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By

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ABSTRACT

The thermal design constraint of power electronic converters under the specific power loss and heat sink is mainly determined by the maximum permissible junction temperature of the power devices. As the power density and switching frequency increase, transient electro-thermal models become more and more important for the thermal management system design of the power electronic converters. In traction inverters, the junction temperature has huge variation because the fundamental frequency and phase currents vary significantly during the load cycles. Thus, the junction temperature estimation becomes extremely important for the reliability of traction inverters.

In this thesis, the transient electro-thermal analysis of a traction inverter considering the inter-dependency of the power losses and junction temperature in an iterative process is implemented. Considering the impact of circuit stray parameters on the switching loss, the temperature dependent power loss model is built based on the datasheet values and the measured switching losses. A state-of-the-art thermal model of the entire inverter including the power modules and the heat sink is developed considering the thermal coupling effects of multiple power devices. By using transient thermal simulation, the linearity of the heat transfer process of the entire traction inverter is verified. The impact of the material thermal properties on the thermal impedance is also presented. In addition, the accuracy of the combination of the thermal subsystem models is verified with simulation. The developed transient electro-thermal model is then used to simulate the junction temperature profiles of the inverter under different operating conditions. Finally,

the developed model is experimentally verified. By considering the thermal impedance of the thermal grease layer, the simulation results match with the experimental results very well.

The proposed electro-thermal model can provide important information for the thermal management system design, package optimization, long-term reliability analysis, and maximum rating characterization of the traction inverters.

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Chapter 1

INTRODUCTION

1.1 BACKGROUND

Power electronics is the application of power semiconductor devices for the control and conversion of electric power. According to the types of the input and output power, power converters can be classified into four categories: AC-DC, DC-AC, DC-DC, and AC-AC converters. Power electronics converters are widely applied in the modern society such as the renewable energy applications, electric drives, and power supplies. In electric drive applications, power inverters are applied to convert the DC power to the AC power for electric machines. The reliability of power inverters is critical to the safety operation of the system, especially for the traction applications.

The key components in a power inverter are power semiconductor devices. In high power and high voltage power electronics applications, Insulated Gate Bipolar Transistor (IGBT) modules have become one of the most widely used power semiconductors. However, the rapid development of power semiconductor technology results in the increase of the power rating and decrease of the size, which bring inevitable challenges to the thermal management of power electronics converters.

As shown in Fig.1.1, the percentage of failures due to temperature issues of electronic components is as high as 55% [1]. It is also noted that the failure rate nearly doubles for every 10˚C operating temperature rise [2].

The temperature variation introduces mechanical stress to the components and, therefore, it affects the connections of solder and wire bond. The impact of the temperature on the life time of power semiconductor components is classified into two types: destruction damage and fatigue of the component. The destruction or permanent damage of components is caused by the long-term exposure to the junction temperature that exceeds the maximum permissible value. The fatigue of the component is mainly caused by the repetitive tensile and compressive stresses occurred in the adjacent layers such as the Silicon die, solder, and substrate. The repetitive thermal stress due to the temperature fluctuation induced by the power cycling is the main contribution of the repetitive tensile and compressive stresses [3].

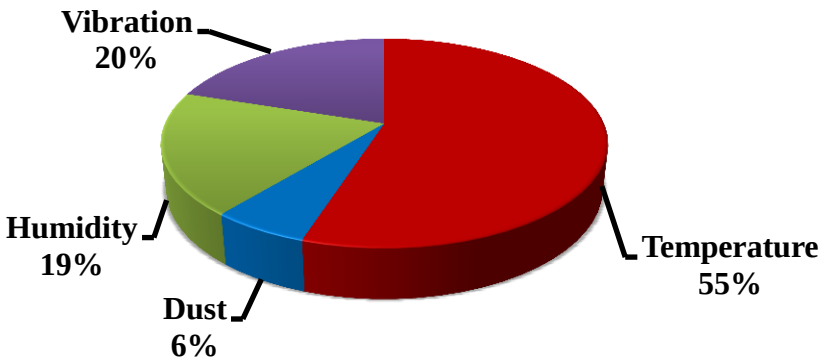


Fig. 1.1 Failures of electronic components[1]

In order to guarantee the safe operation and long-term reliability of a system, power electronics engineers may be conservative by allowing wider design margins such as applying of the overdesigned heat sink and reduction of the current or switching frequency of the IGBT power modules. However, these approaches contradict to the trends of higher power density and also lead to an increase of the cost and sacrifice of the system performance.

1.2 MOTIVATION

Since the reliability and performance are seriously affected by both the maximum junction temperature T_j and the temperature variations ΔT_j, accurate modeling of the entire power electronics converter, both electrically and thermally, is of great demand.

However, due to the large number of power devices and multiplicity of physical effects involved, it is not an easy task to create an electro-thermal model which can predict the transient power dissipation and junction temperature of the power devices instantaneously. An electrical engineer may focus more on the current and voltage waveforms than temperature prediction, while it is more likely for a mechanical engineer to regard the semiconductor device as a various layers of material for heat propagation. In addition, the electrical phenomenon (switching process) happens in several nanoseconds while the heat transfer process happens in a much larger time scale (several minutes or hours). Therefore, the simulation time step should be small enough to catch the transient detail while the total simulation time should be long enough to obtain the long-term temperature profile. This requirement makes the electro-thermal simulation very time consuming and

sometimes nearly impossible. Therefore, a compromise must be made between the simulation speed and accuracy.

Many efforts have been made to establish the electro-thermal model of inverters and typically three steps are required: building the power losses model, building the thermal model and coupling between these two models. The researches in this field are working on some or all of the following topics: the power losses model, the thermal model, and coupling between these two models. Details of the previous work on these three topics will be discussed in the following chapters. However, a brief introduction is listed here to explain the motivation of this thesis.

Hefner firstly stated the importance of coupling the electrical model with thermal model in the thermal management design of power electronics converters. A physical based dynamic electro-thermal model which is implemented in the Saber circuit simulator is developed [5-7]. There are also many other commercially circuit simulators such as PSpice and system simulators such as ANSYS-SIMPLORER and PLECS available for electro-thermal simulation. However, due to the fact that a typical inverter load cycle is always relatively long while the switching process happens in hundreds nanoseconds, simulating each switching process using even compact device models in the circuit simulators are prohibitively time consuming [8]. Meanwhile using the system simulators will result in rather poor accuracy of the switching behavior prediction and power losses calculation [9].

Considering the thermal parts, the thermal models can be classified into two categories: physical based thermal models (finite element method (FEM), finite difference method

(FDM), and computational fluid dynamic (CFD)) [10-13] and behavior based thermal models (also called compact thermal models or thermal network models).

The physical based model is based on the detailed model of the device and it can provide relatively accurate solutions at the expense of slow computing speed, especially when different components in the system are of large different time scales. For instance, the thermal time constant of the power module in a forced air cooled inverter is much smaller than that of the heat sink. Moreover, these models are hard to create an electro-thermal simulation with an electrical circuit simulator to predict the instantaneous power losses [14].

The behavior based model considers the heat conduction process in the power module as a linear system and it is implemented by extracting the RC network model from the temperature step response of the system [15-17]. The temperature step response defined as the transient thermal impedance curve (TTIC) is obtained by measurements or the FEM simulations. . The step response can fully represent the dynamic behavior of the system and it can be easily implemented in the general circuit simulators to predict the temperature response under arbitrary power loss profiles [18]. This method provides a new and simple way for co-simulation of the thermal and electrical models. However, the prerequisite of this method is the linear assumption of the system, and it is limited to the modeling of the heat conduction in the power module [19]. Since the heat convection in the cooling system is typically a nonlinear process, researches on the extension of the power module model to the cooling system model can be seldom found and the existing

studies focus only on the steady-state and long-pulse operation[14][20]. In addition, even for the heat conduction process, there are still some nonlinear factors such as the temperature dependencies of the thermal conductivity of materials need to be evaluated [21-23]. Besides, the thermal cross-coupling effects in the power module is also worthy to be considered [24-25]. All of these issues place a demand of more detailed and comprehensive thermal models.

The last and most important issue in this field is that the previous studies generally focus on only one aspect, either the power loss modeling, the thermal modeling, or the model verification. They seldom take into account the whole picture in the study. In this thesis, a fast and accurate power loss model is provided and a comprehensive thermal model of the entire system is developed. By coupling these two models together, an electro-thermal model is implemented. The developed electro-thermal model can predict the long-term temperature profile within a relatively short simulation time period and it can also guarantee the accuracy of the estimated temperature fluctuation in short-term transient.

This thesis concentrates on fast and accurate transient electro-thermal simulation of the commonly used power electronics converters: the IGBT based three-phase voltage-source traction inverters. This simulation model will be able to provide the information that can be applied for the thermal management system design, package optimization, analysis of the device long-term reliability, and maximum rating characterization.

1.3 CONTRIBUTION

The main contributions of this work are the following:

1. Development of a temperature dependent power loss model suitable for long-term electro-thermal analysis of the traction inverter.
2. Development of a comprehensive thermal model of the entire inverter as an extension of the traditional behavior based RC network model of the power module.
3. Analysis of the most controversial issues for the thermal analysis of the inverter, including the linearity of the thermal model of the whole inverter, impact of the temperature dependencies of the materials' thermal properties, and the feasibility of the combination of thermal subsystems by using different RC network model.
4. Transient electro-thermal analysis of the inverter considering the thermal coupling effects in the thermal model and the inter-dependency of the power loss and the junction temperature of the semiconductor device in an iterative process.
5. Experimental verification of the developed thermal model by using both direct and indirect temperature measurement approaches.

1.4 OUTLINE OF THE THESIS

The proposed master thesis concentrates on the transient electro-thermal analysis of an IGBT based three-phase inverter, and the rest of this thesis is organized as follows.

In Chapter 2, the temperature dependent power loss model of the power module is introduced. Firstly, the operating principle and power losses analysis of IGBTs and diodes are presented. Then, several power losses calculation approaches used in the literatures are reviewed. Finally, the formulas to calculate the temperature dependent conduction loss based on datasheet and the temperature dependent switching losses model based on the measurement results are presented.

Chapter 3 describes the thermal model of the entire inverter. Firstly, the literatures of existing thermal modeling methods are investigated, especially for the thermal network method which the proposed model in this thesis is based on. Then we detail the process of extracting the parameters of the RC network model of the whole inverter and discuss the feasibility and accuracy of using this model to describe the system's thermal characteristics. The linearity of the thermal model and influence of the temperature dependency of the materials on the thermal model are also discussed. After that, the thermal model of the inverter containing the power module and heat sink is developed by considering the thermal coupling effects. Furthermore, the accuracy and recommendation of direct combination of the subsystem models to build the whole inverter thermal model is presented, which is a good reference for engineering practice.

Based on the power loss model and thermal model, the transient electro-thermal simulation of the inverter is carried out and presented in Chapter 4. The temperature dependency of the power losses and thermal coupling effects are both considered and this

model is used to evaluate the dynamic performances of the junction temperature of the inverter under different operating conditions.

In Chapter 5, the experimental validation of the model is described. The direct measurement method using thermal couples and indirect measurement method using the temperature sensitive electrical parameters (TSEP) are both carried out to verify the transient thermal performance of the system.

Chapter 6 summarizes the work presented in this thesis and conclusions are made.

Chapter 2

POWER LOSSES OF IGBT MODULES

2.1 INTRODUCTION

In order to conduct the thermal analysis of an IGBT based inverter, the power losses of the IGBT power modules need to be calculated. For an ideal switch, the power consumption is zero. However, in a real power device like the IGBT, there are two kinds of losses: conduction losses and switching losses. These losses depend on the voltage and current, and also both of them are temperature dependant [26]. Therefore, there is coupling between the electric and thermal behaviors as mentioned in Chapter 1. Considering this fact, the junction temperatures have to be determined by iterations in an electro-thermal model, and a temperature dependent power loss model suitable for long-term simulation is essential.

In this chapter, the operational principle and power losses of the IGBT power module including the IGBTs and anti-parallel diodes are introduced firstly. Then, various approaches used in the literatures for power losses calculation are reviewed. Finally, the temperature dependent power loss model which will be used for electro-thermal analysis in this thesis is presented.

2.2 OPERATIONAL PRINCIPLE AND LOSSES IN AN IGBT MODULE

2.2.1 Operational Principle and Losses Composition of IGBT

With increasing requirements of high power rating and fast switching power devices, Insulated gate bipolar transistors (IGBTs) power devices were introduced in the 1980s. Fig. 2.1 shows the circuit symbol of the IGBT and freewheeling diode inside an IGBT power module. There are three terminals which are denoted as: Collector, Emitter, and Gate. The collector and emitter are related to the conductance path and the gate is designed for its control.

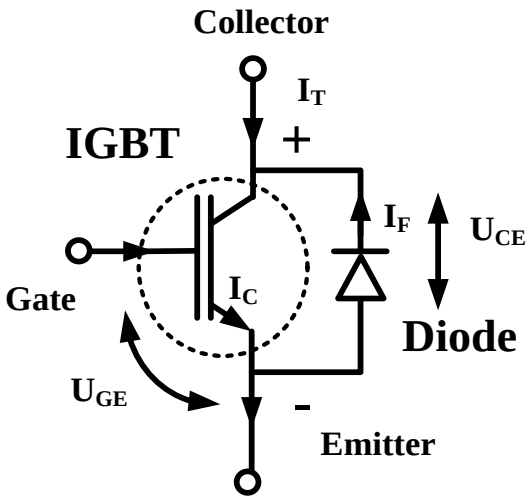


Fig. 2.1 Circuit symbol of the IGBT and anti-parallel diode

IGBT is a voltage-controlled device with a gate controlled signal (U_{GE}) applied between the gate and emitter. The working process and losses composition of it is showed in Fig. 2.2:

A positive gate-emitter voltage U_{GE} is applied during the turn-on transition period. When the positive voltage rises higher than the threshold voltage ($U_{GE}>U_{th}$) the collector current I_C starts to flow from the collector to the emitter. After a current rise time t_{ri}, I_c reaches the load current value I_0, and then the collector-emitter voltage U_{CE} starts to drop. After U_{CE} falls to its small on-state value of U_{on} the turn on process is over. The energy dissipation caused by the large values of switch voltage and current during the turn-on crossover interval $t_{s(on)}$ is called switching on loss.

During the turn-off transition period, the reverse process happens. Firstly, the current and voltage remain constant until U_{GE} drops below the level required to maintain the collector current I_C at the load current value. Then during the voltage rise time t_{ru}, the collector-emitter voltage U_{CE} starts to rise to the blocked voltage U_B while I_C still remains constant. After this period, I_C falls to zero with a current fall time t_{fi} and the current I_0 commutates from the switch to the diode. The energy dissipation caused by the large values of switch voltage and current during the turn-off crossover interval $t_{s(off)}$ is the switching off loss.

Between these two states, the switch remains in conduction with the on-state voltage U_{on} and the conducting current I_o. This time interval is defined as the on-state interval, which is much larger than the turn on and turn off time intervals. The energy dissipation during this on-state interval is called the conduction losses.

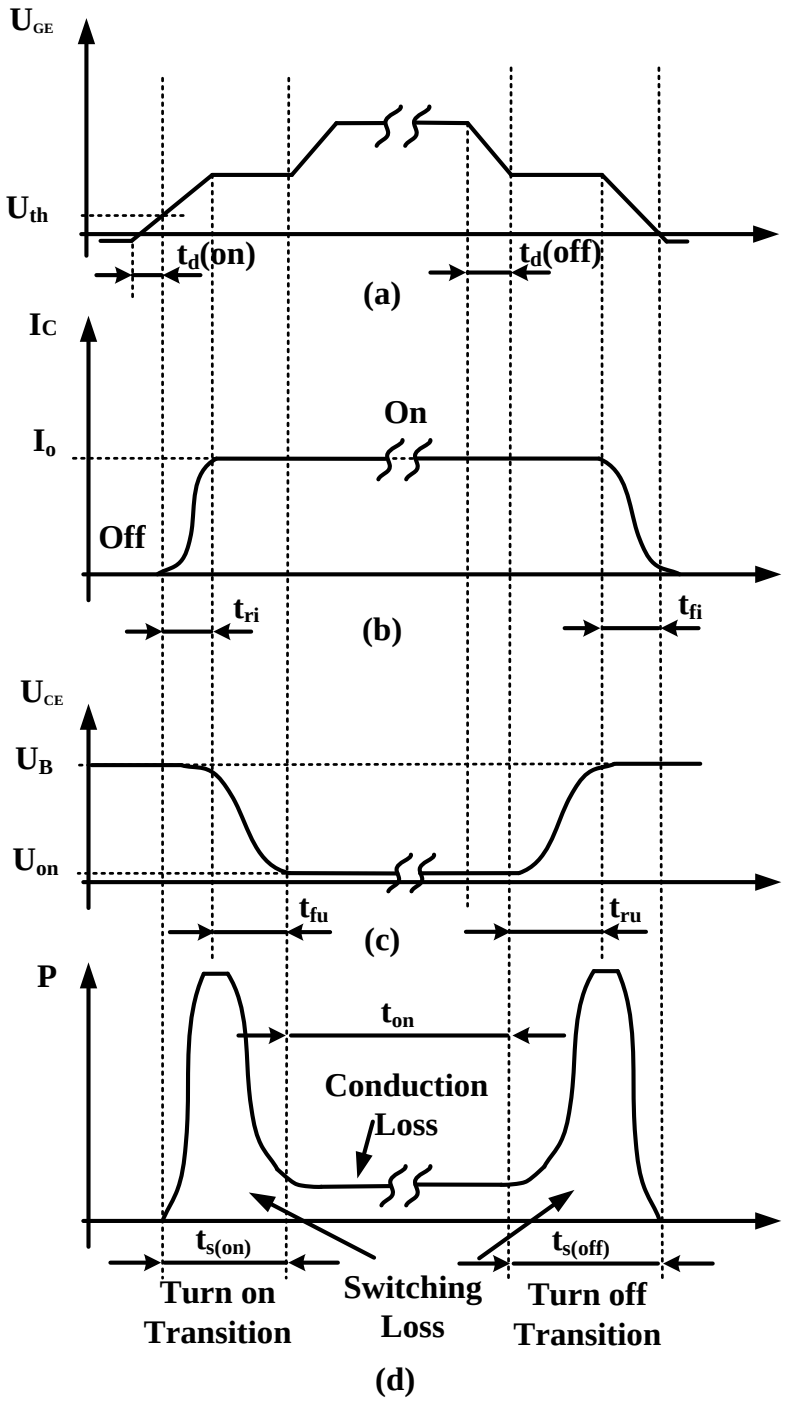


Fig. 2.2 Power losses of a switching cycle of an IGBT: (a) Gate-emitter voltage; (b) Collector current; (c) Collector-emitter voltage; (d) Power losses of the IGBT

2.2.2 Conduction Losses of IGBT

The conduction losses can be represented as the product of the instantaneous conducted current $i_c(t)$ and the corresponding collector-emitter voltage $u_{CE}(t)$:

$$p_{con}(t) = i_C(t) \bullet u_{CE}(t) \tag{2.1}$$

2.2.3 Switching Losses of IGBT

Similarly, the instantaneous power dissipate $p(t)$ of the IGBT during the switching on and off process is also equal to $i_C(t) \cdot u_{CE}(t)$. However, since these processes typically happen in a very short time interval such as several hundred nanoseconds, the energy dissipation during the switch-on and switch-off processes is more concerned about. The switching-on energy E_{on} and switching-off energy E_{off} can be expressed as:

$$E_{on}(t) = \int_{t_{on}} i_C(t) \bullet u_{CE}(t) \bullet dt \tag{2.2}$$

$$E_{off}(t) = \int_{t_{off}} i_C(t) \bullet u_{CE}(t) \bullet dt \tag{2.3}$$

2.2.4 Losses of the Freewheeling Diode

There are also conduction losses and switching losses of the freewheeling diode. The conduction losses are also represented by the product of the instantaneous forward voltage drop of the diode u_F and the current i_F flowing through the diode.

$$p_{Fcon}(t) = i_F(t) \bullet u_F(t) \tag{2.4}$$

Normally, due to the very short turn-on time with respect to the switching period, the switching-on losses of the diode are always neglected [27].

The switching-off losses of the diode are determined by the reversely recovery losses of the diode. The voltage and current waveforms of the diode during the turn off transition is illustrated in Fig.2.3.

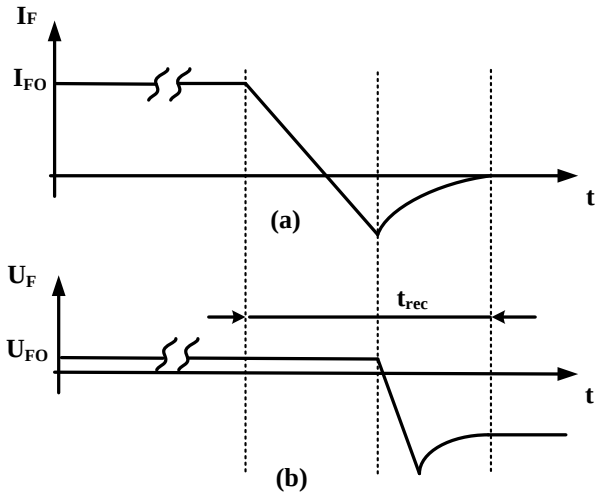


Fig. 2.3 Reverse recovery voltage and current waveforms of freewheeling diode: (a) Current of the freewheeling diode (b) Voltage of the freewheeling diode.

Similar to the switching energy dissipation of the IGBT, the diode recovery energy E_{rec} can be defined as:

$$E_{rec}(t) = \int_{t_{rec}} i_F(t) \bullet u_F(t) \bullet dt \tag{2.5}$$

It should be noted that the power loss calculation in this chapter is based on the external characteristics of the devices, such as the junction temperature, the collector current and the forward voltage drop. Therefore, the detailed inner physical structures of the IGBT and diode are not discussed in this thesis.

2.3 PREVIOUS WORK

Determination of power losses for the electro-thermal simulation is a challenge. On one hand, the shapes of the current and voltage waveforms mentioned above depend on the physics of the device, the load condition, and the junction temperature. As a result, very detailed and complicated models are required to accurately predict the power losses. On the other hand, the duration of the switching process is in the order of a few hundred nanoseconds while the thermal time constant of the system is much larger at a level of seconds or even hundred seconds. Therefore, millions or billions of switching events need to be calculated to fully represent the system properties.

There are several methods to estimate the power losses of IGBTs in a fast and accurate way. Based on physical model of power devices [28], the circuit can be simulated using software such as SPICE, PSpice, Saber and EMTP. In order to calculate power losses [29-31], complex formulas are implemented in the software by relating the external characteristics to the internal physical behaviour of the device. They can model the switching events accurately; however a very detailed model is needed because of the complicated physical switching process. Since the switching on and off processes happen in only several hundreds of nanoseconds, a very small simulation time step is required. All of these result in an unacceptably large computing time, especially in the case of long-term electro-thermal simulation for multi-device systems.

An alternative approach is to calculate the electrical behavior such as waveforms of the voltage and current of the circuit analytically. Based on the switching waveforms, simple

functions are applied to calculate the losses [32-33]. This method is much faster than the previous one. However the analytical calculation introduces errors.

A more commonly used and convenient way to estimate the power loss is based on the device datasheets provided by manufactures [34]. These results are extracted from simulated or measured power losses of the device under different conditions. However, considering the influence of the external circuit designed by the customers, it is impossible for the datasheets to cover all different work conditions of the devices.

2.4 TEMPERATURE DEPENDENT POWER LOSSES CHARACTERIZATION OF POWER DEVICES

In order to provide a fast and accurate model, the power losses calculation in this chapter is based on both the datasheet and the measured results. From (2.1)-(2.3), it can be found that the power losses depend on the current through the device i_C and the voltage across the device u_{CE}. Many factors have impacts on the shape of the current and voltage waveforms. The current and voltage waveforms during the conduction interval are quite simple. The current depends on the load and the voltage can be expressed as a function of the current and junction temperature by using the DC characteristics extracted from experiment or provided by the manufacturer in the datasheet [35].

However the parameters for calculating the switching losses, such as the delay time, the rise time and the fall time, will be significantly influenced by the stray parameters in the gate driver and bus bar, the gate resistance, the DC link voltage and the junction temperature [35]. Thus the accurate switching losses can only be obtained by measuring

the switch on and switch off transition with the power module connected to the customer designed external components (gate driver, DC link voltage, and bus bar). In this case, the switching losses are only influenced by the current and junction temperature.

From the above analysis, the fast and accurate power losses model should be able to accurately calculate the power losses according to the current and junction temperature. In order to satisfy these requirements, the conduction loss model in this thesis is based on the forward characteristics provided in the manufacturer's datasheet and the switching loss model is built by using a look-up table calculated by the measurement results.

2.4.1 Temperature Dependent Conduction Losses

The instantaneous conduction loss of the IGBT or diode can be calculated by using the multiplication of voltage drop $u_D(t)$ and the conducted current $i_C(t)$ as it shows in 2.6.

$$p_{Tcon} = u_D(t) \bullet i_C(t) \tag{2.6}$$

The typical relationship between voltage drop and conducted current of IGBT or Diode under certain junction temperature can be seen in Fig.2.4.

According to Fig.2.4, the voltage drop can be approximated by a linear function of the conducted current:

$$u_D(t) = u_{D0} + r_C \bullet i_C(t) \tag{2.7}$$

where the coefficients u_{D0} is the zero-current voltage drop of the device, and r_C represents the on-state resistance of the device.

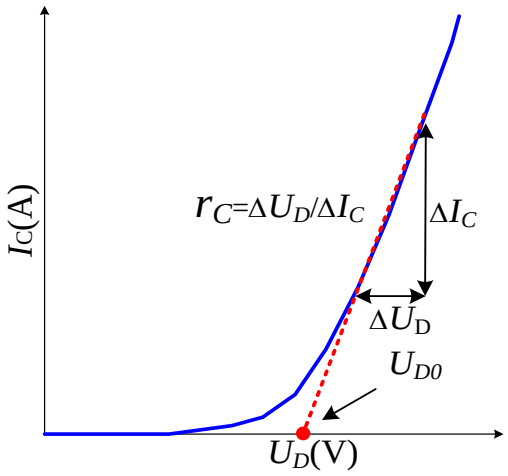


Fig. 2.4 Relationship between the voltage drop and conducted current of device under certain junction temperature

When considering the temperature dependence of the conduction loss, u_{D0} and r_C can be represented as a linear function of junction temperature as expressed in 2.8 and 2.9.

$$u_{D0} = a_0 + a_1(T_j - T_0) \tag{2.8}$$

$$r_C = b_0 + b_1(T_j - T_0) \tag{2.9}$$

where a_0 and b_0 are the coefficients when the junction temperature equals to the nominal temperature T_0; a_1 and b_1 represent the temperature sensitivity of these coefficients.

By applying 2.6-2.9, the conduction loss of IGBT and Diode can both be expressed as a function of the conducted current through the device and the junction:

$$p_{Tcon} = u_D(t) \bullet i_C(t) = (u_{D0} + r_C \bullet i_C(t)) i_C(t) = f(i_C(t), T_j(t)) \tag{2.10}$$

In this thesis, the temperature dependent conduction losses are calculated based on the Infineon datasheet and the relationships between the device voltage drop and the

conducted current of the IGBT and diode under different junction temperatures are shown in Fig.2.5 and Fig.2.6, respectively.

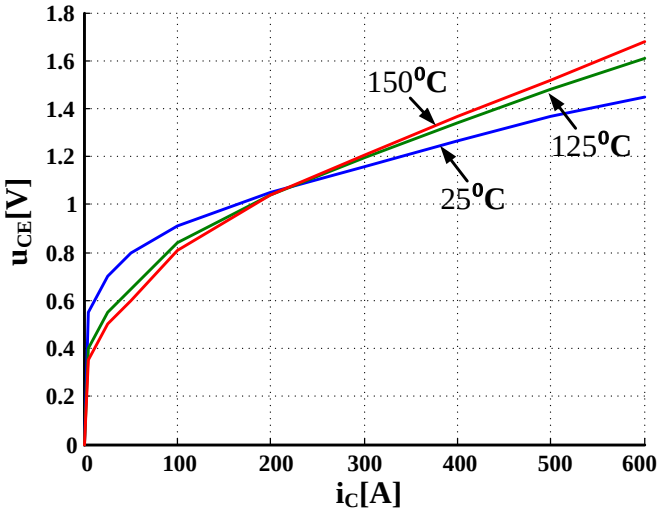


Fig. 2.5 u_{CE}-i_C characteristics of the IGBT at different junction temperature (u_{CE} - voltage drop of the IGBT, i_C - conducted current of the IGBT) [36]

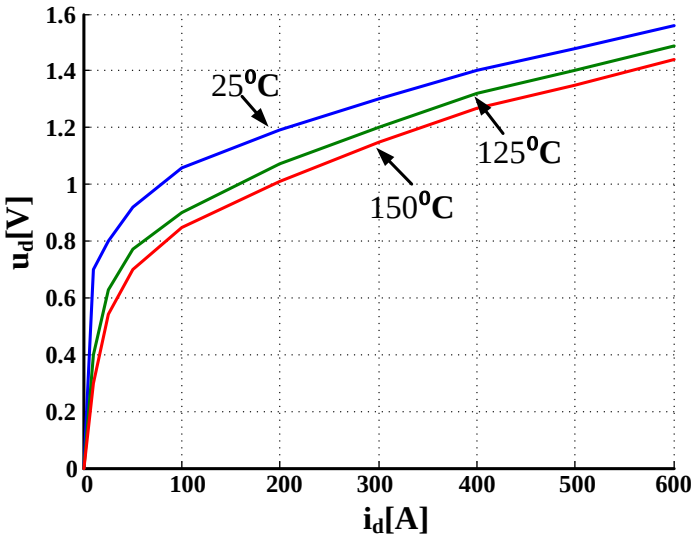


Fig. 2.6 U_D-I_D characteristics of the Freewheeling Diode at different junction temperatures (u_d - voltage drop of the diode, i_d - conducted current of the diode) [36]

2.4.2 Temperature Dependent Switching Losses

The manufacturer's data sheet also provides the measured switching-on losses and switching-off losses of the power module as functions of the collector current and junction temperatures under specified test conditions. However, in the practical traction inverter, these losses are also significantly influenced by the stray parameters in the bus bar, the DC-link voltage and the gate resistance. Thus directly applying the switching losses values in the datasheet to the power loss model will result in huge errors.

In this thesis, the accurate switching losses are obtained by applying double-pulse test experiments and measuring the switch on transition and switch off transition of the chips with the power module connected to the practical external components (gate driver, DC link voltage and bus bar). In this case, the switching losses are only affected by the device voltage, current and junction temperature and can be represented as a function of these factors.

Fig.2.7 shows the schematic of the switching loss test for the IGBT. To measure the switch on and switch off transient processes under different current levels (25-450A), a gate signal shown in Fig. 2.8 (a) is applied to the low-side IGBT. The first pulse (t_2-t_1) is used to raise the load current i_L to the desired value in Fig.2.8 (b), and the switch off transient process (wave forms of i_C and u_{CE} in Fig 2.8(c) and (d)) is recorded at time t_2. After a short interval t_3-t_2, the low-side IGBT is turned on and the switch on transient process of the same current level is recorded at time t_3.

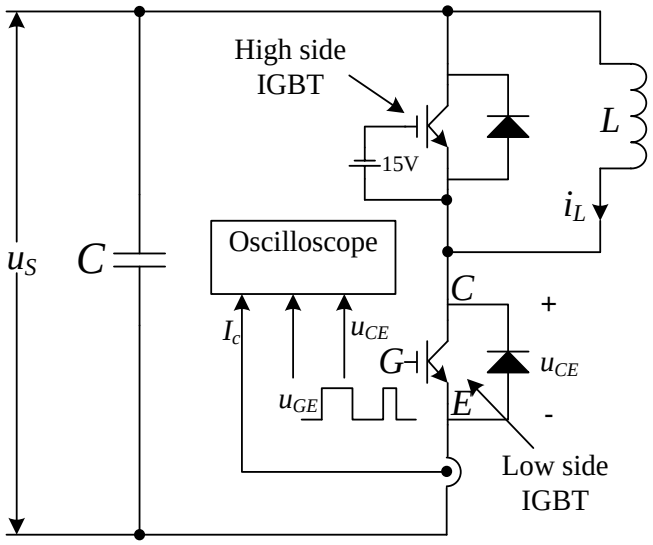


Fig. 2.7 Schematic of the switching losses test for the IGBT

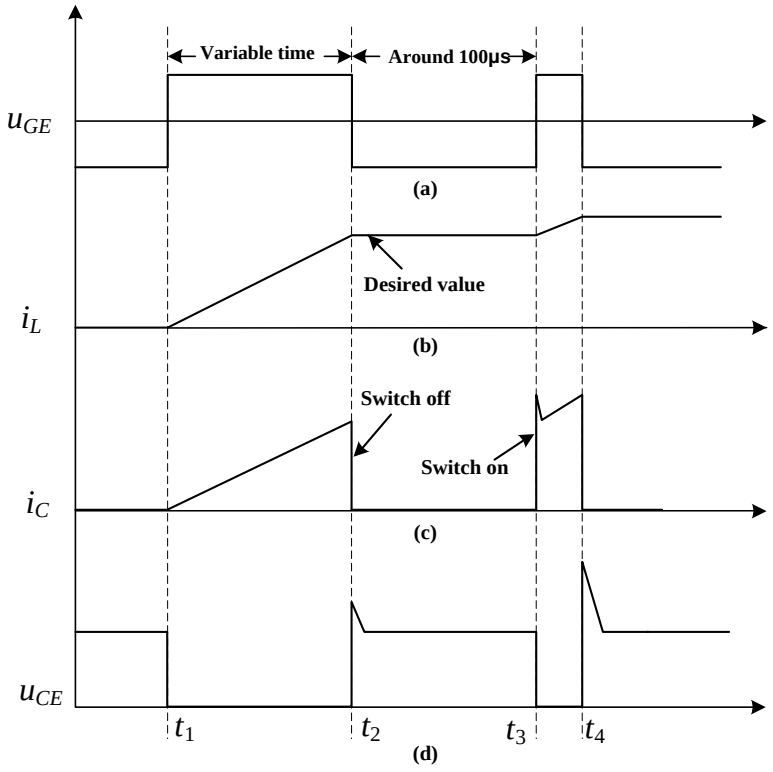


Fig. 2.8 Basic wave forms for the switching losses test for the IGBT: (a) gate-emitter voltage u_{GE}; (b) load current i_L; (c) collector current i_C; (d) collector-emitter voltage u_{CE}

To take into account the temperature effect, the device under test is mounted on a temperature controllable hotplate to measure the switching losses under different junction temperature (25-125˚C).

The typical measured current and voltage waveforms during the switch on process and switch off process are shows in Fig. 2.9 and Fig. 2.10 respectively. The test conditions are: 300 V DC-link voltage, 300 A collect current, and 75˚C junction temperature. It can be seen that these process happens in several microseconds, thus a 30MHz bandwidth Rogowski coil from PEM Corporation is applied to measure the collector current waveforms i_c and a 30MHz bandwidth isolated voltage probe is also used to measure the collector-emitter voltage waveforms u_{ce}.

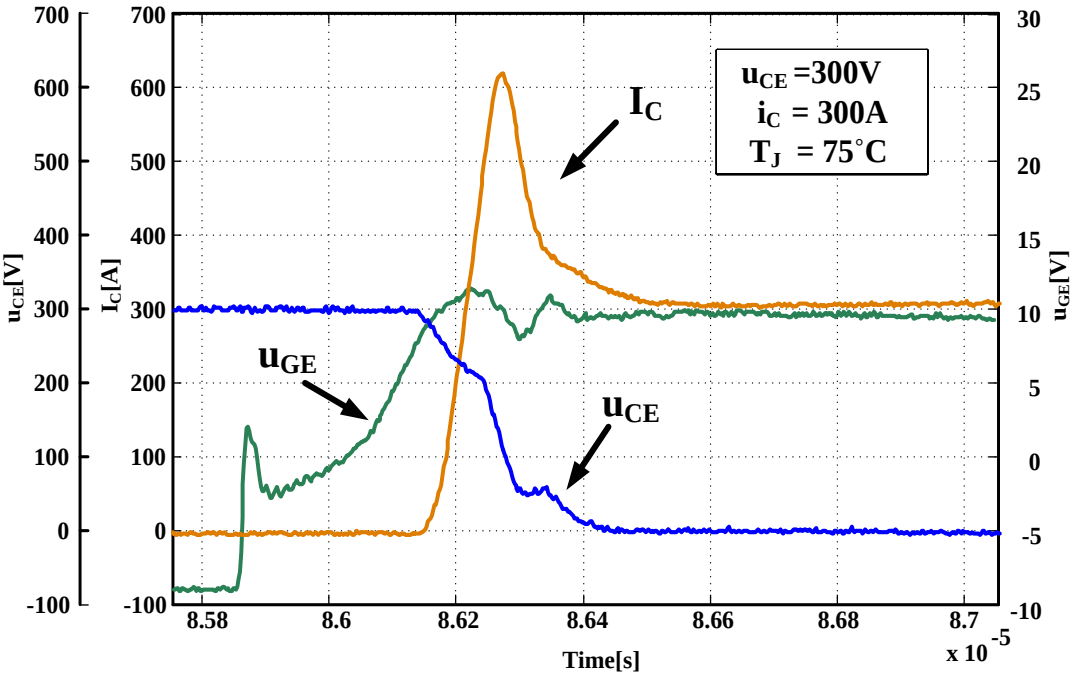


Fig. 2.9 Measured current and voltage: switch on transient process

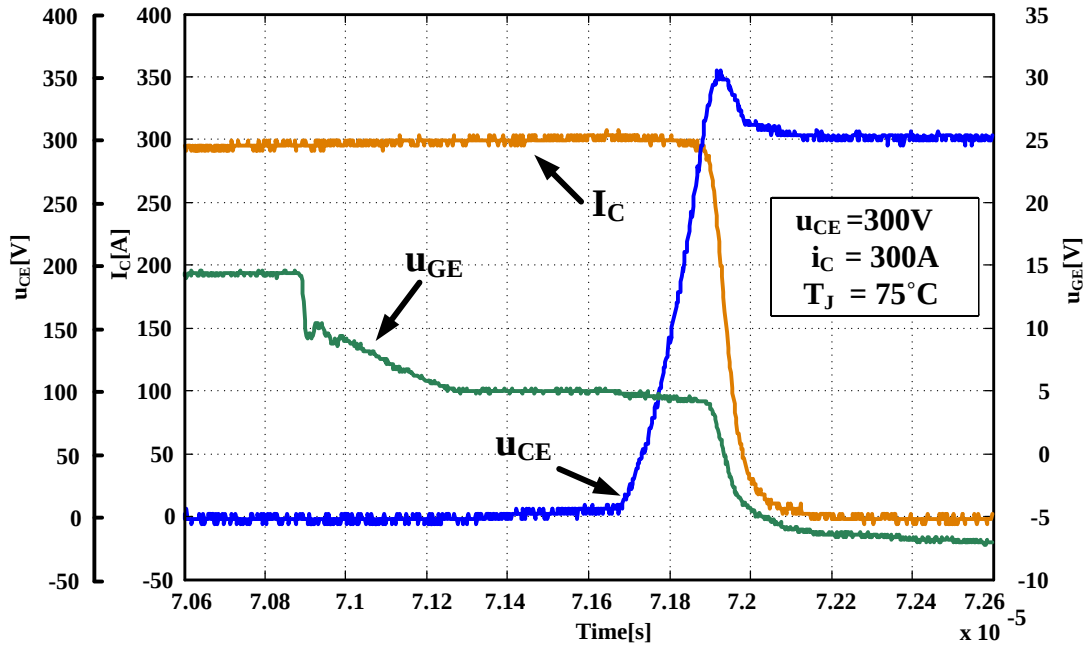


Fig. 2.10 Measured current and voltage: switch off transient process

Then the switching losses can be obtained by integrating the product of the instantaneous collector current i_C and collector emitter voltage u_{CE} measured during the switch transient processes. These processes are repeated several times under different collector current i_C and junction temperature T_j. The switching on and off losses under different i_C and T_j can be fitted into 3-dimensional look up tables as it shows in Fig. 2.11 and 2.12 for further electro-thermal simulation. It worth to mention that both the switching on losses and the switching off losses become larger as the junction temperature rises, and the difference between the values of the losses obtained 25 ˚C and 150 ˚C are about 19% of the total losses.

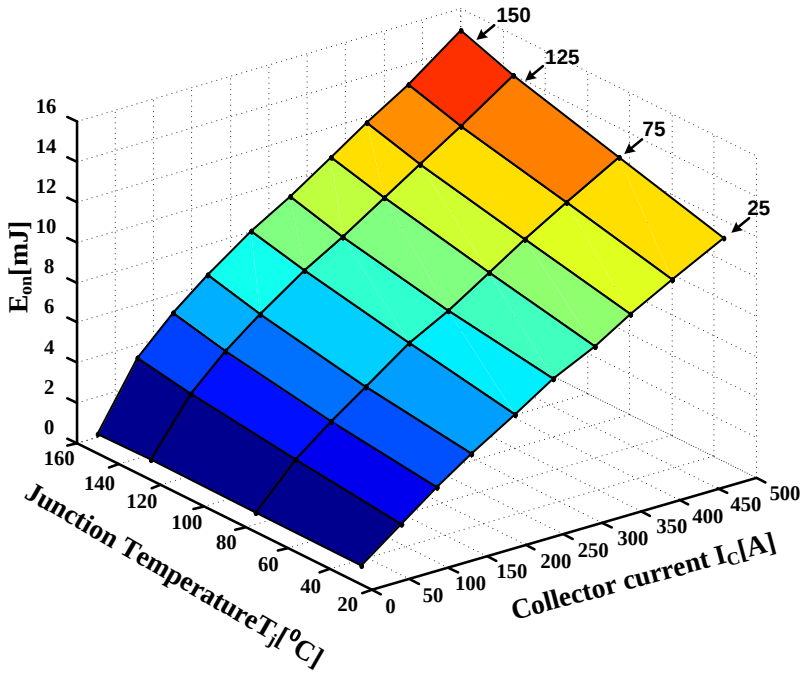


Fig. 2.11 IGBT switching on loss at different current and junction temperature

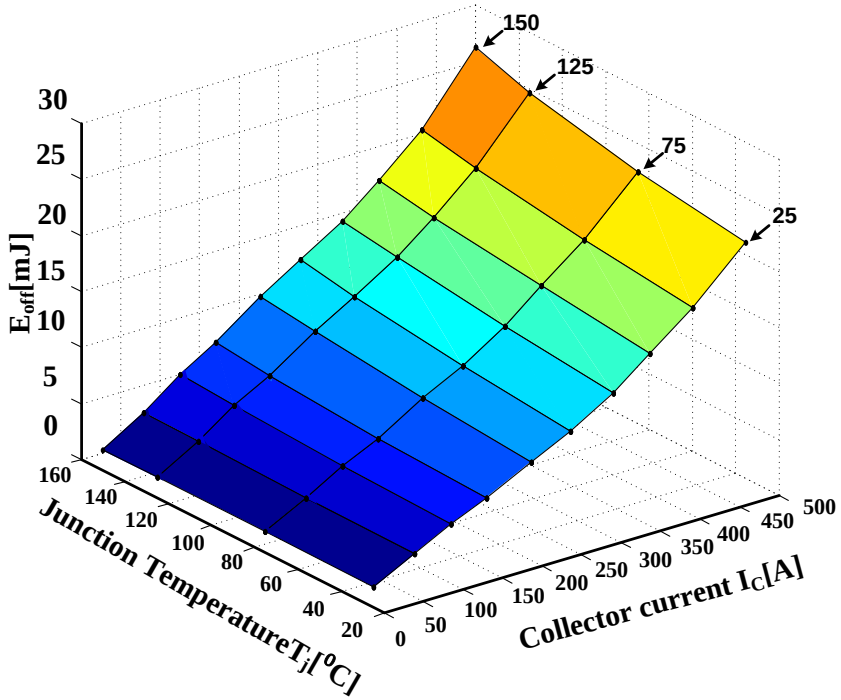


Fig. 2.12 IGBT switching off loss at different current and junction temperature

Similarly, a 3-D look up table can also be set up for the reverse recovery loss of the diode, which is given in Fig.2.13.

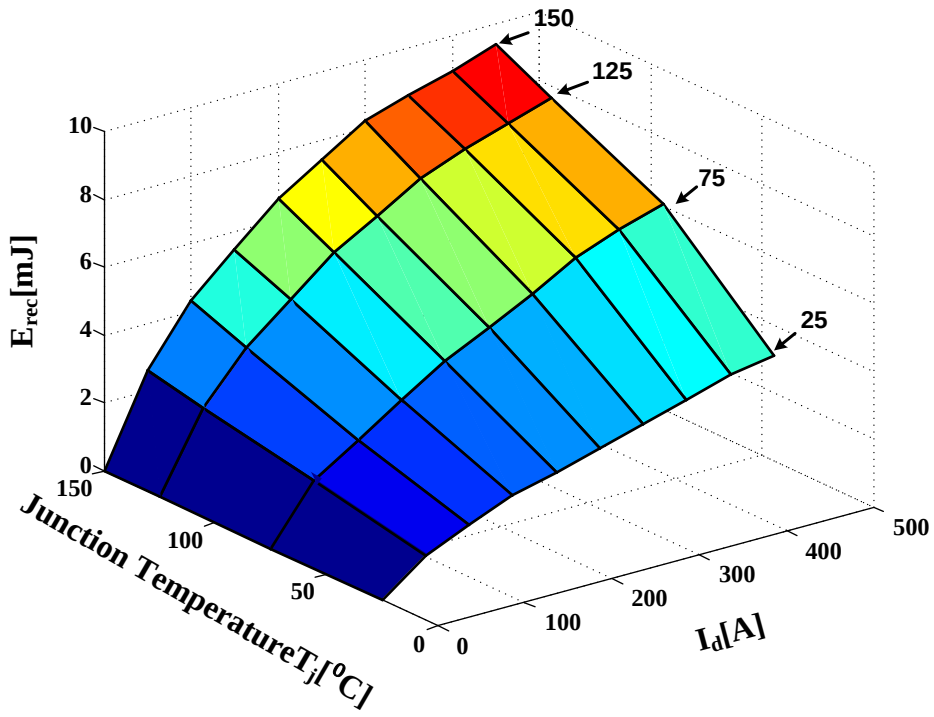


Fig. 2.13 Diode recovery loss at different current and junction temperature

2.5 CONCLUSION

In this chapter, the temperature dependent power loss models of the IGBT and diode are built, which will be used in long-term electro-thermal simulation of the traction inverter. In order to estimate the power losses in a fast and accurate way, the conduction loss model in this chapter is built based on the manufacturer's datasheet and the switching loss model is established by setting up a look-up table calculated from the measurement results.

Chapter 3

THERMAL MODEL OF IGBT MODULES

3.1 INTRODUCTION

In Chapter 2, the power loss of IGBT modules used in three-phase inverters was analyzed. However, to predict the transient junction temperature of IGBTs and diodes, a fast and accurate thermal model of the system is required.

In this chapter, a review of different approaches used to perform the thermal analysis of power electronics is presented. The difficulties and issues in building a thermal model of the whole traction inverter are discussed. Then, the feasibility of using thermal RC network method to describe the thermal behavior of the whole inverter is demonstrated. After that, the thermal model of the whole system based on an improved thermal RC network method is developed, the self-heating and thermal cross-coupling effects are all well considered. Moreover, the non-linearity issues in the thermal model caused by the temperature dependence of thermal properties of materials (the thermal conductivity and volumetric heat capacity) are evaluated. At the end of this chapter, the possibility and methods of extending the thermal model of the power module in IGBT datasheet to the thermal model of the heat sink is discussed.

3.2 PREVIOUS WORK

The difficulties caused by balancing the fast switch events and the long term simulation in building the power loss model has been discussed in Chapter 2. However, the situation is

similar and even worse when considering the thermal part, because thermal modeling of electronic system involves a hierarchy of length scales ranging from 10^{-4} to 1m and will result in a wide spreading time scales in the simulation [37]. For instance, in a inverter, heat is generated at the junction region, which is the active area of the device (typically the channel in a transistor) and of size in micron dimension. The heat will pass through a multilayer structure in the device and dissipate to the ambient air from the heat sink, the size of which is commensurable with humans or even bigger [38]. This goes for both space and time scales with ratios between biggest and smallest scales of the order of 10^9 and poses significant challenges to the thermal analysis of power electronics. The problem will become even severe when considering the electro-thermal effects which seriously affect both the reliability and performance of power electronic systems.

Typically, there are three ways for heat to transfer from one material to another: conduction, convection and radiation [39]. In electronic components, such as MOSFETs or IGBT, most of the heat is dissipated by the conduction and convection, and the heat radiation is negligible. A one-dimensional heat flow can be assumed for the sake of simplification, and the heat conduction problem is always assumed to be linear [40].

The purpose of using a thermal model is to calculate the junction temperature under certain power dissipation, and numerous modeling and analysis methods have been established during the past decades.

There are typically three methods to establish the thermal model of power electronics devices.

The first method is the numerical methods, which include the finite-element method (FEM) [41] and computational fluid dynamics (CFD) [42]. These methods have been published for steady and transient thermal analysis. The advantage of these methods is that any device geometry can be modeled and they can provide very exact solutions. However these numerical methods are based on detailed models of the devices, where the material properties and layers need to be known [43-44], while the manufacturer may not wish to reveal details of their design to protect intellectual property. In addition, these methods are very time consuming, especially when different components in the system are of various time scales. For instance, the thermal time constant of the power module in a forced air cooled inverter could be 10000 times smaller than the heat sink. It makes this method good for structure optimization [45] however it is impossible to be applied for evaluating the junction temperature variation under arbitrary load profiles [46] or under a real duty cycle in the operating condition, which are more important for the reliability analysis of the system.

Another method is the analytical method, which provides a Fourier series solution by solving the 1-D or 2-D heat diffusion equations [47]. This “mesh less” method offers an improved trade-off between the accuracy and computing speed compared to the numerical methods like FEM and CFD and it has been implemented in MATLAB/Simulink to solve a heat diffusion problem through a series of layers with a constant cross-sectional area [48]. The feasibility of using this 1-D analytical model in an electro-thermal simulation has also been demonstrated [49], and recent publications could even be found considering the 3D heat diffusion equations and thermal coupling effects in

the analytical thermal model [50]. The drawbacks of this method is that it still requires a detail dimensions and the inner structure of the IGBT package and the heat spreading effect in the material might not be accurately estimated and usually a typical heat spreading angle of 45° is assumed [51]. Furthermore, analytical solution is limited to describe the heat conduction in the power module packages and it can be only applied to simple layer structures accurately. The heat convection between the heat sink and the coolant cannot be accurately evaluated and a whole model considering both the power module and the heat sink cannot be expected.

The most widely used thermal modeling method is the thermal resistor-capacitor (RC) network. It produces an accurate and computationally efficient thermal model that can be easily realized in circuit simulators to estimate the instantaneous junction temperature in a long-term dynamic simulation [52-54].

3.3 THERMAL RC NETWORK

These thermal RC network methods can be further divided into two groups, structural based method and behavioral based method.

3.3.1 Structural Based RC network

The structural based RC network is also known as the physical based lumped parameter thermal networks (LPTN). The principle of this method is the heat conduction equation has a similar form as the transmission line equation.

The one-dimensional heat conduction problem in a homogeneous isotropic material without considering the temperature dependence of the thermal characteristics can be expressed as [39]:

$$\frac{\partial^2 T}{\partial x^2} = \frac{c \bullet \rho}{\lambda_{th}} \bullet \frac{\partial T}{\partial t} \tag{3.1}$$

where T is the temperature and x is the coordinates in the direction of heat propagation of the device, λ_{th} is the specific heat conductance, c is the specific thermal capacitance and ρ is the density of the material.

Meanwhile, differential equation of the electrical transmission line without inductance can be expressed as [55]:

$$\frac{\partial^2 U}{\partial x^2} = C' R' \bullet \frac{\partial U}{\partial t} \tag{3.2}$$

where U describes the voltage, C' is the capacitance per unit length and R' stands for the resistance per unit length.

So it is obvious that (3.1) and (3.2) have the same structure, and since a transmission line can be described by a RC network as it is shown in Fig. 3.1, it follows that the thermal conduction problem can also be described by a similar RC network.

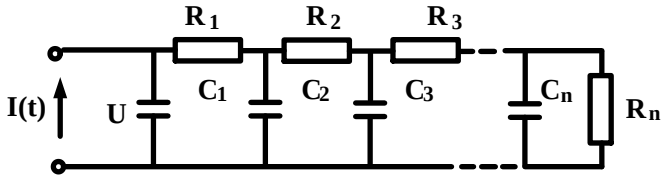


Fig. 3.1 Transmission line equivalent circuit diagram

Based on (3.1) and (3.2), the analogy between the thermal and electrical variables is listed in Table 3.1 [55].

Table. 3.1 Analogous of the physical variables of thermal and electrical systems

Thermal		Electrical	
Temperature	T in K	Voltage	U in V
Heat flow rate	P in W	Current	I in A
Thermal capacity	C_{th} in W·s/K	Electric capacitance	C in A·s/V
Thermal conductivity	R_{th} in K/W	Electric conductivity	R in V/A

IGBT is a vertical power device, which means its inner structure can be segmented to several layers as it is shown in Fig. 3.2, and for each layer, the thickness is much smaller than other dimensions, so a one dimensional conduction process is always assumed in the physical based RC network method [56].

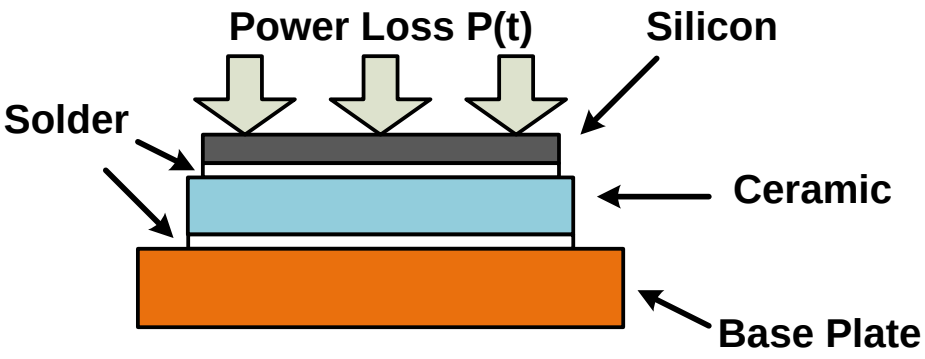


Fig. 3.2 Simplified physical structure of an IGBT module

And by using the analogous physical variables of the thermal system to the transmission line equivalent circuit, the thermal RC network corresponding to the IGBT module shows in Fig. 3.2 can be obtained as it is shown in Fig. 3.3, where each RC rings correspond to a different layer of material in the IGBT module.

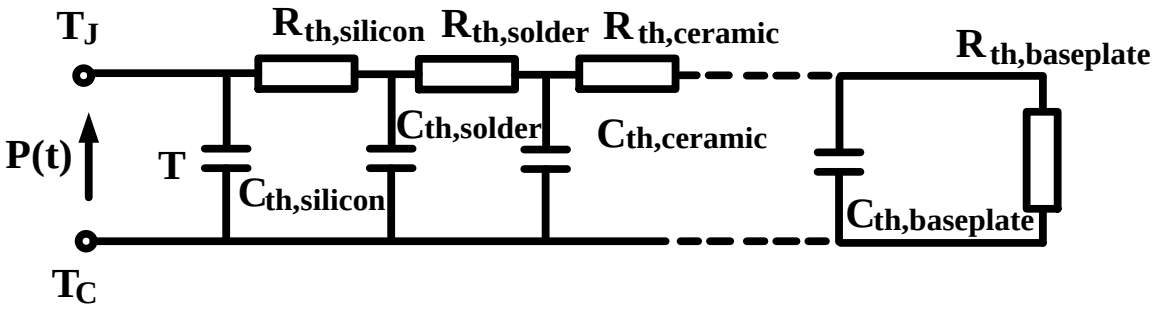


Fig. 3.3Transmission line equivalent circuit diagram for thermal conduction

As a quasi-1D heat-flow is assumed in the system, the thermal resistance R_i and thermal capacitance C_i of each layer can be estimated by the following equations.

$$R_{th,\mathrm{i}} = \frac{d_i}{\lambda_{th} A_{th,i}} \tag{3.3}$$

$$C_{th,i} = \rho \bullet c \bullet d_j \bullet A_j \tag{3.4}$$

Where A_i and d_i represent the cross sectional area and thickness of layer i as it shows in Fig.3.4.

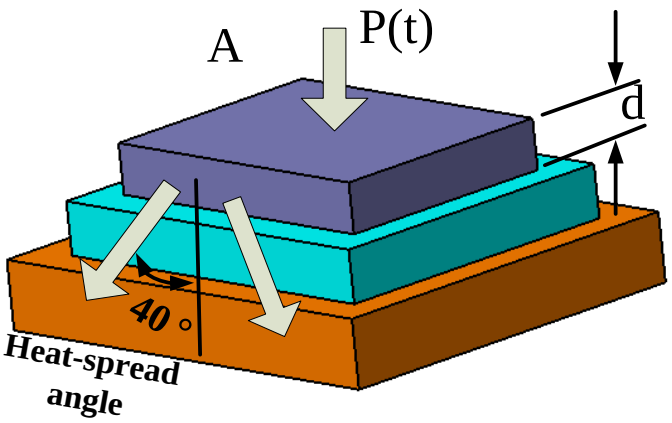


Fig. 3.4 Physical structure used for extracting thermal parameters

One issue for this method is that the temperature is assumed to be distributed uniformly on the surface of each layer, and this surface is regard as a node in the RC network circuit. However the real situation is the cross sectional areas of the heat conducting material in each layers are quite different thus the heat spreading effect need to be considered. Therefore a heat spreading angle of about 40° is assumed typically [57], but this kind of appropriation still introduces errors to the system. Especially when calculating the thermal capacitance because the active volume that heat propagates through has a decisive influence on the thermal capacitance and can be hardly exactly determined without considering the 3-D heat diffusion process. Therefore, the accuracy of using this thermal model to predict the dynamic performance of the junction temperature is a big issue. In addition, this method might not provide good estimation of the heat convection from the cold plate to the coolant because it is usually represented by only a constant heat transfer coefficient.

3.3.2 Behavioral Based RC (Foster) Network and Definition of Thermal Impedance

The structural based network model mentioned above has significant advantages in computation speed because it reduced the nodes or meshes in the numerical simulation from millions to dozens or even less. However experimental or numerical approaches like FEA and CFD have the strength of predicting the heat and coolant flow in complex regions much more accurately. Thus it is nature to wonder the possibility of developing a modeling method which combines the advantages of the thermal network, numerical tools, and experimental test.

The behavioral based RC network (also known as the foster network) is proposed to solve this problem. The R and C elements of the equivalent circuit in this model are extracted by fitting the measured thermal dynamic curve. The key step in using this method is to calculate the transient thermal impedance, which is obtained by heating or cooling the module with defined power dissipation P until the junction temperature reaches its steady-state value. The temperature rise ΔT is then determined by fixing the case at a constant temperature T_{ref} and measuring the changes of junction temperature T_j versus time t with infrared cameras or electrical temperature sensitive electrical parameters (TSEP) [58].

The definition of transient thermal impedance can be expressed as:

$$Z_{th}(t) = \frac{T_j(t) - T_{ref}}{P} \tag{3.5}$$

If the thermal system can be assumed to be a linear and time invariant (LTI) system, then obviously the transient thermal impedance corresponds in system theory to the step response of the system with zero initial condition, and therefore it contains the full thermal description of the system [59]. When the step response is obtained, no matter by measurements or numerical analysis, the transient junction temperature under any power dissipation profile $P(t)$ will be able to be predicted by applying follow equation [60]:

$$T_j(t)=T_0+\int P(t)\,\dot{Z}_{th}(t-t)\,\mathrm{d}\,\tau \tag{3.6}$$

Where T_0 is the initial temperature and $\dot{Z}_{th}(t)$ is the time derivative of the thermal impedance, which corresponds to the thermal impulse response of the system.

This method treats the thermal problem as a system with the power loss as input and the temperature rise as output. It focuses only on the thermal transient behavior of the system thus the physical structure is not concerned about.

Because of the advantages mentioned above, the manufacturer of IGBT module usually provides the transient thermal impedance curve of junction to case Z_{jc} to the users to carry out thermal analysis and a typical thermal impedance curve for IGBT module is shown in Fig.3.5.

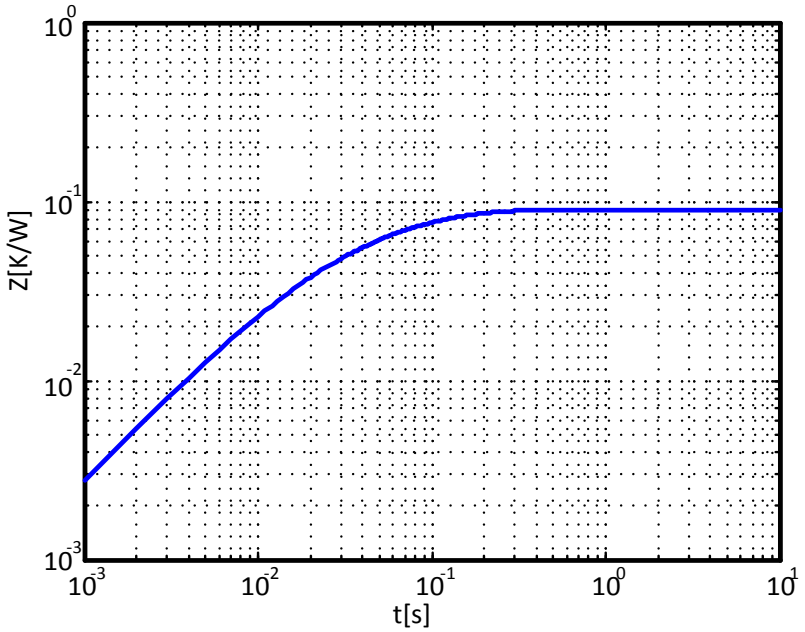


Fig. 3.5 Typical transient thermal impedance curve

The next problem is finding an equivalent network whose step response is the same as the measured or simulated transient thermal impedance curve. Actually, there are numerous networks whose step responses can meet this requirement. However the one called Foster network, which is shown in Fig. 3.6, is the most commonly used one because it is easy to extract the coefficient of it from the measured or simulated thermal impedance curve [61].

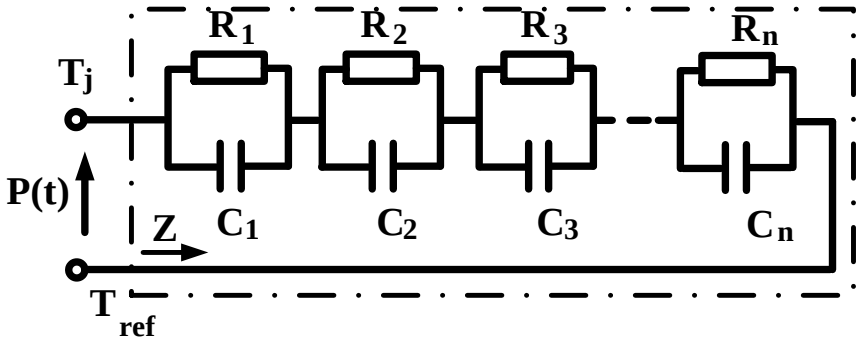


Fig. 3.6 Typical Foster network

When using the Foster network, the transient thermal impedance curve can be fitted into a series consists of a finite number of exponential terms as given in (3.7):

$$Z_{jc}(t)=\sum_{i=1}^{n} R_i \bullet (1-\exp(-\frac{t}{R_i C_i})) \tag{3.7}$$

The transfer function of the Foster network is found by applying Laplace transform to (3.7):

$$Z_{jc}(s)=\sum_{i=1}^{n} \frac{R_i / \tau_i}{s+1/\tau_i} \tag{3.8}$$

Where τ_i is the product of R_i and C_i, and it is called the thermal time constant.

The behavior based RC network model solves the conflict between fast calculating speed and high calculating accuracy. It can also be easily integrated to circuit simulator like SPICE or SABER to conduct electro-thermal simulation, so it becomes the most widely used method nowadays. However, there are still some drawbacks with this modeling methodology and these problems are what the model developed in this chapter wants to solve.

Firstly, this method focuses mainly on modeling of the power module. The case temperature is generally controlled or assumed to be a constant value T_{ref} as shown in (3.5)[52] [62]. However what user really concerns is the thermal performance of the entire system including both the power module and a realistic heat sink, which received much less attention [63]. Meanwhile, though building a network model of the entire

inverter has been mentioned in a few papers [42] [64], the feasibility of using the RC network model to describe the whole system has been rarely or never validated.

Secondly, the most important prerequisite and foundation of the behavior based thermal network is that the corresponding system should be a LTI (linear time invariant) system. The time invariant property of the system can be easily proved since the transfer function of the system is not a function of time. However, the linearity of the system need to be further discussed. It is widely accepted that the thermal model of the IGBT power module could be regarded as a linear. The assumptions are listed as 1) the temperature dependences of the density and specific thermal properties of the material can be ignored; 2) only the thermal conduction is considered; 3) the materials are thermally homogeneous and isotropic and. However, these assumptions have rarely been carefully validated. Also, the accuracy of the linear hypothesis without considering the temperature dependences and heat spreading effects in the system has seldom been evaluated.

In addition, if a model of the entire system is going to be established, the linearity of the system need to be checked again because heat convection between the heat sink and the ambient could be a nonlinear factor and a involving the heat sink to the system may also introduces a reverse effect on the thermal spreading within the IGBT power module.

Another drawback of the traditional behavior based RC networks is that it does not take the into account thermal coupling effect from multiple heat sources [65], which may also cause errors.

Based on the behavior based RC network method and its drawbacks mentioned above, the thermal model used in this paper will be developed. The summary of the problems that will be solved in the following part of this chapter is listed below.

1. Feasibility of applying the RC network method to build a thermal model of the entire inverter including both the IGBT power module and the heat sink will be discussed.
2. The linearity of the system will be checked and the errors caused by nonlinear issues such as the temperature dependence of materials' thermal properties will be evaluated.
3. Involving the thermal coupling effects in building the thermal model of multiple chips devices will be presented.
4. Furthermore, as the manufacturers always provide only the thermal network model for the power module and may not wish to reveal details of their, ways to build the thermal model without detailed dimensions and 3D model of the power modules will also be discussed. The errors by using this method will also be evaluated.

3.4 SYSTEM CONFIGURATION

The system configuration of the inverter is shown in Fig. 3.7, it is composed of a liquid cooled cold plate, a DC bus, a capacitance and three IGBT modules. When considering the thermal system, we focus mainly on the IGBTs which operate as the switching

elements and the main heat sources, and the cold plate that dissipates the heat to the coolant.

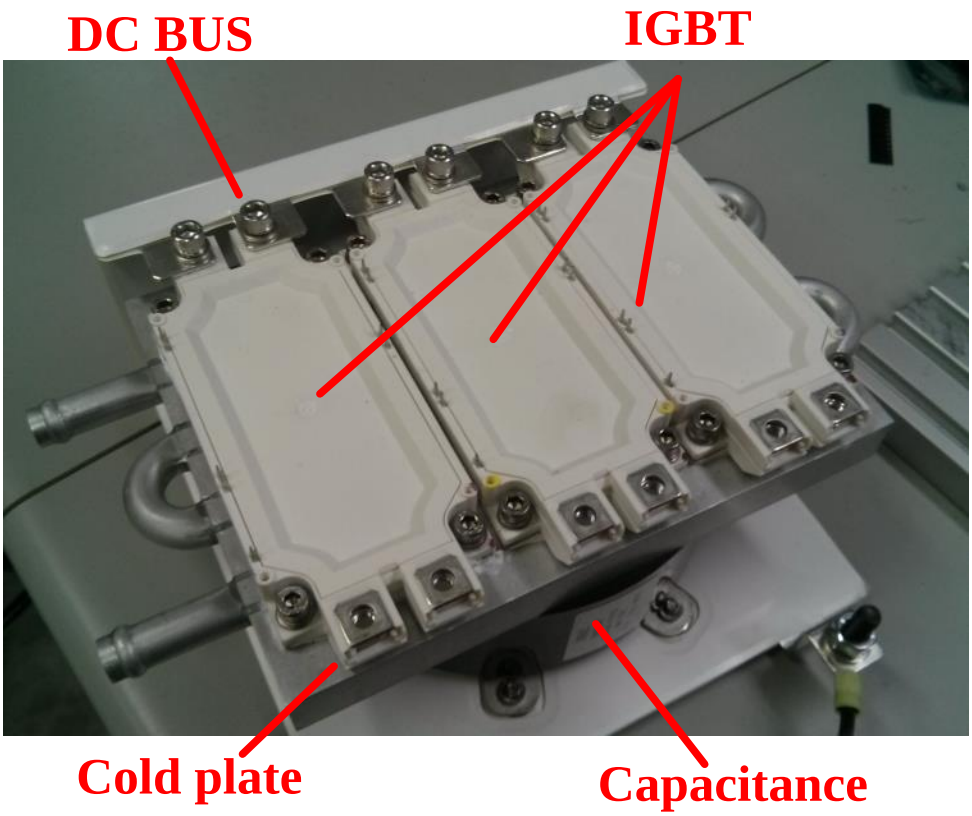


Fig. 3.7 Photo of the inverter

In order to describe the problem more intuitively, the heat propagation path and the vertical structure of a chip inside the power module with the heat sink is shown in the Fig.3.8 (left), and the thicknesses of layers which are applied to calculating the thermal resistances and capacitances are also presented. The succession of the layers is as follow: 1 – Silicon chip, 2 – Solder, 3 – Direct Copper Bond (DCB), 4 – Ceramic Bed, 5 – Direct Copper Bond (DCB), 6 – Solder, 7 – Baseplate, 8 – Thermal interface material, 9 – Heat sink, 10 – Coolant.

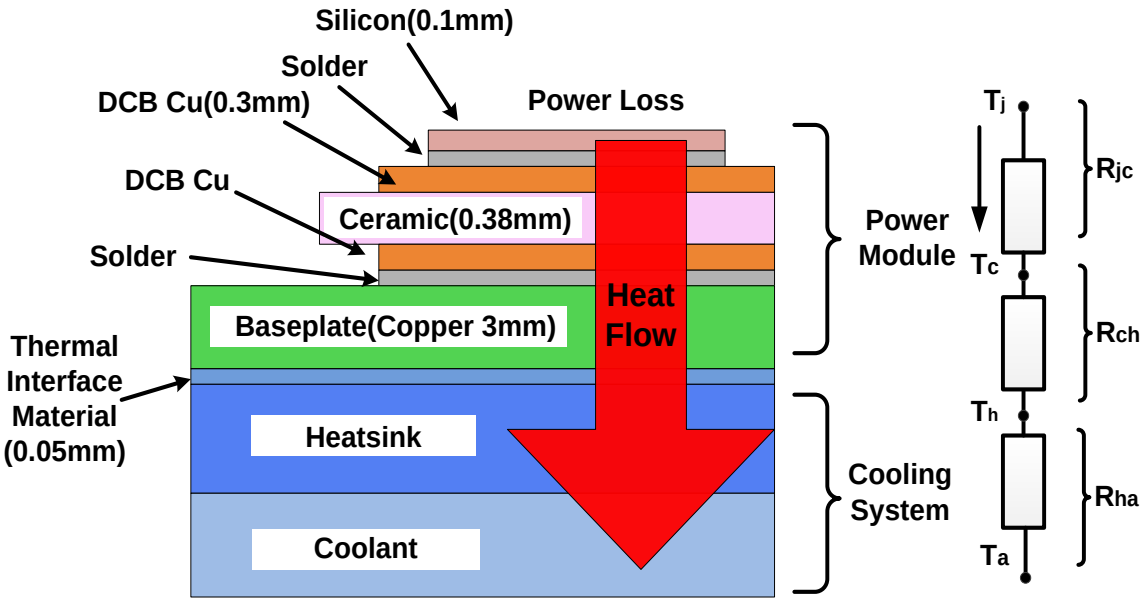


Fig. 3.8Power losses of a switching cycle of an IGBT

As it has been mentioned, there are typically three different ways for the heat propagation in a system – heat conduction, heat convection and radiation. In an inverter, most of the heat is dissipated by the conduction and convection, and one-dimensional heat flow can be assumed for the sake of simplification. The simplified thermal resistance network corresponding to the progress can be seen in the right of Fig. 3.8. T_j, T_c, T_h and T_a represent the temperature of the junction, case, heat sink and ambient (coolant) respectively.

R_{jc} represents the thermal resistances from junction-to-case, and it describes the heat conduction progress from the junction to the case (bottom of the baseplate), which happens in the power module.

R_{ch} represents the thermal resistance from case-to-heat sink, and it describes the heat flow in the thermal interface material (thermal grease normally).

R_{ha} represents the thermal resistance from heat sink-to-ambient (coolant), and it is mainly determined by the heat convection between the heat sink and the coolant, which happens in the cold plate of the inverter.

The relationship between these parameters can be expressed as in (3.9) and (3.10).

$$P_L = \frac{T_j - T_c}{R_{jc}} = \frac{T_c - T_h}{R_{ch}} = \frac{T_h - T_a}{R_{ha}} \tag{3.9}$$

$$T_{ja} = T_j - T_a = P_L \bullet \left(R_{jc} + R_{ch} + R_{ha} \right) \tag{3.10}$$

where P_L represents the power loss and T_{ja} represents the temperature difference between the junction and the ambient (coolant).

From 3.10 it can also be noticed that with the same power loss level, the junction temperature depends on a summation of R_{jc}, R_{ch} and R_{ha}. Specifically, the value of R_{jc} depends on the structure and materials of the electronic component and the manufacturing process of the manufacturers and R_{ch} depends on the contact conditions and the thermal interface material [66]. So both of them have a relatively fixed value thus R_{ha} is the crucial factor in the thermal management system design for inverters and the substance of the thermal design is to choose a cooling method and parameters to make sure R_{ha} satisfies the follow equation:

$$R_{ha} \le \frac{T_{j,\max} - T_a}{P_L} - R_{jc} - R_{ch} \tag{3.11}$$

where $T_{j,max}$ is the max allowable junction temperature of the chips.

3.5 MODEL VERIFICATION OF THE THERMAL BEHAVIOR OF A SINGLE IGBT MODULE

In this chapter, the thermal model of the whole system will be built by using data extracted from 3D numerical simulation. An accurate model of the IGBT power module is the most important prerequisite for any further analysis.

3.5.1 3D Model in the Simulation

The power module was opened in order to implement the dimension measurements and the internal structure of the module used in the inverter is shown in Fig. 3.9. It can be seen that there are totally 6 IGBTs and 6 diodes in the package.

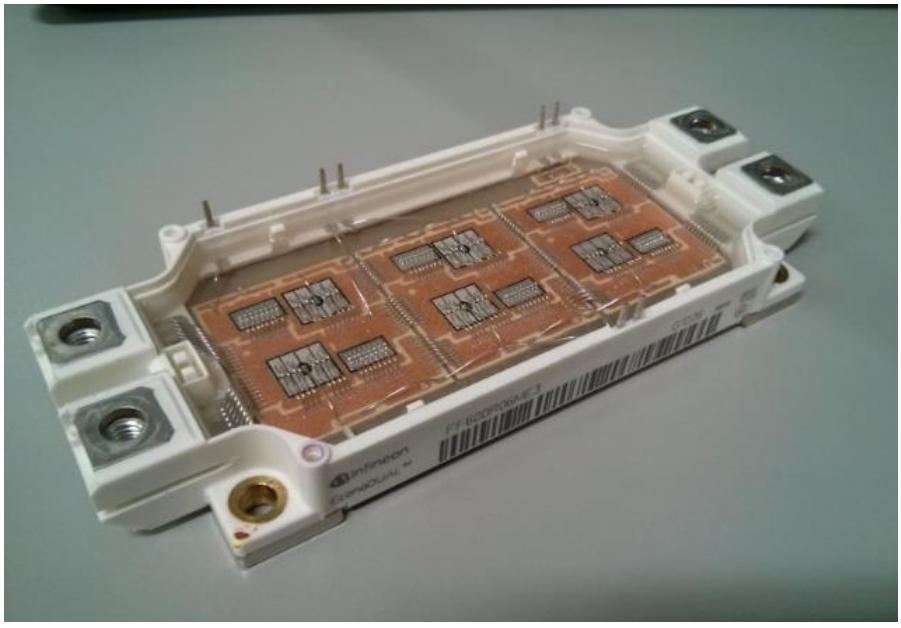


Fig. 3.9 Studied power module

A detailed 3D model of the device is built as it is shown in Fig. 3.10. Each power module includes 6 IGBTs and 6 Diodes, and there are seven layers of materials under each chip. The vertical structure of each chip is illustrated in Fig. 3.8. For each switching cycle, three of the IGBT chips or diodes in parallel will work together, so these chips are divided into 4 groups - #1 high-side IGBT, #2. low-side IGBT, #3. high-side diode and #4.low-side diode.

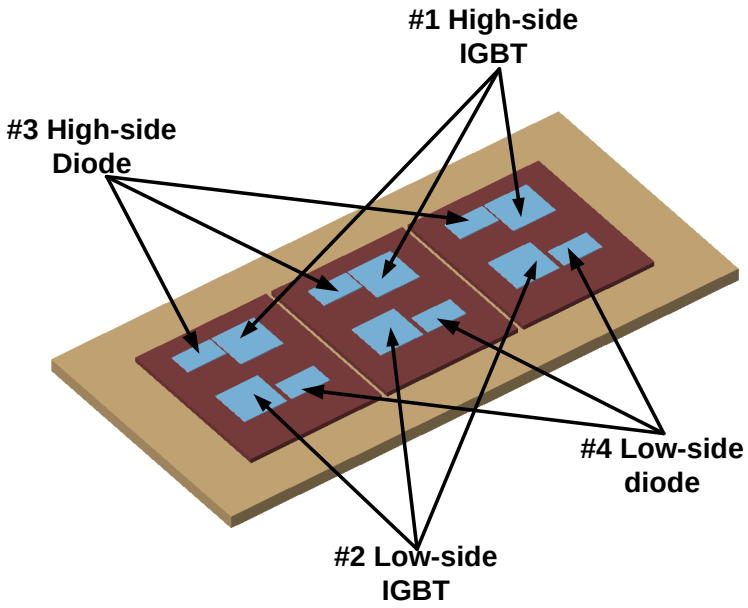


Fig. 3.10 3D Model of the power module

3.5.2 Model Verification

An accuracy model of the power module means accurate configurations, dimensions and material properties, but these parameters are hard to be checked. However, the manufacturer usually provides the transient thermal impedance curve of the power module to the users, and the thermal impedance is determined by all the parameters. Thus,

the accuracy of the 3D model can be checked by comparing the simulated thermal impedance based on this model and the value in the datasheet.

For the initial condition, a uniform temperature (303.15K) for the whole module is assumed.

And the boundary conditions in the simulation are listed as below:

1. The power dissipation is assumed to be uniformly injected on the top surfaces of the silicon dies of both the high-side IGBT and low-side IGBT, but excluding the guard ring region.
2. For each material layer, the thickness is much smaller than the width and length, so heat flux through the lateral sides of the material layers could be neglected and the corresponding surfaces is assumed to be adiabatic.
3. An aluminum heat sink with a thickness of 10mm is added to the case of the power module, and a layer of thermal grease with a thickness of 0.05mm is added between the case and the heat sink.
4. The temperature of the bottom of the heat sink is set to be a constant value (303.15K).

The transient numerical simulation is carried out in ANSYS-Fluent and the simulation time is set to be 10s. And the temperature field after the system is stable is shown in Fig. 3.11.

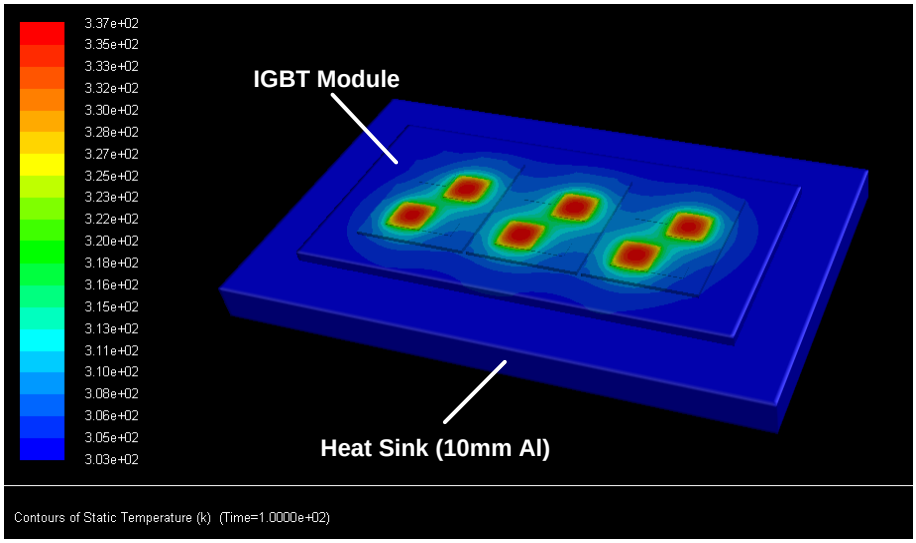


Fig. 3.11 Temperature field after applying the power loss for 100 second

The average temperatures on the top surface of the silicon dies are recorded as the junction temperature, and the thermal impedance can be obtained by applying (3.5). A comparison of the simulation result and the transient thermal impedance curve provided in the datasheet is illustrated in Fig. 3.12 (logarithmic time-scale).

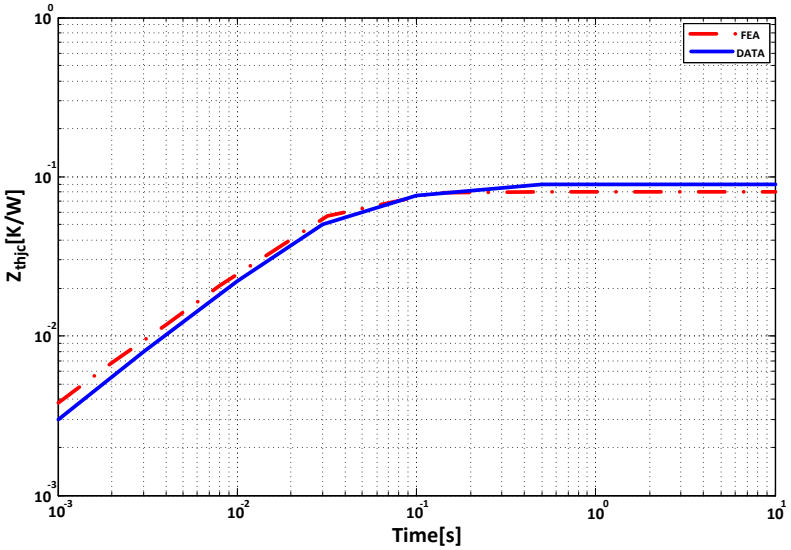


Fig. 3.12 Transient thermal impedance of the power module

It can be seen that these two values are very close to each other in the whole time range. The stable value of the thermal impedance obtained from FEA is a little smaller than that one in the datasheet but the error is within 5%. Thus the accuracy of the model is quite acceptable and this 3D model will later be combined with the liquid cooled heat sink model into the thermal model of the entire inverter for further analysis.

3.6 SELF-HEATING AND CROSS-COUPLING EFFECTS OF MULTICHIP DEVICES

As the model of the power module has been validated, the model of the whole inverter can be built by adding the heat sink model. In Fig. 3.7, the photo of the inverter is showed and the corresponding 3D model of the inverter is built as it is shown in Fig. 3.13. To simplify the geometry for meshing and further analysis, the components which are not relevant for thermal analysis of the prototype were removed, such as the bus bar, the controller boards, the DC-link capacitance, and the cover of the IGBT power module. There are two kinds of heating effects in the system, self-heating effect and mutual-heating effect (thermal cross-coupling effect). To verify the feasibility of using a behavior based network model to describe the thermal performance of the whole system, ways to evaluate these two kinds of heating effects will be discussed in this section.

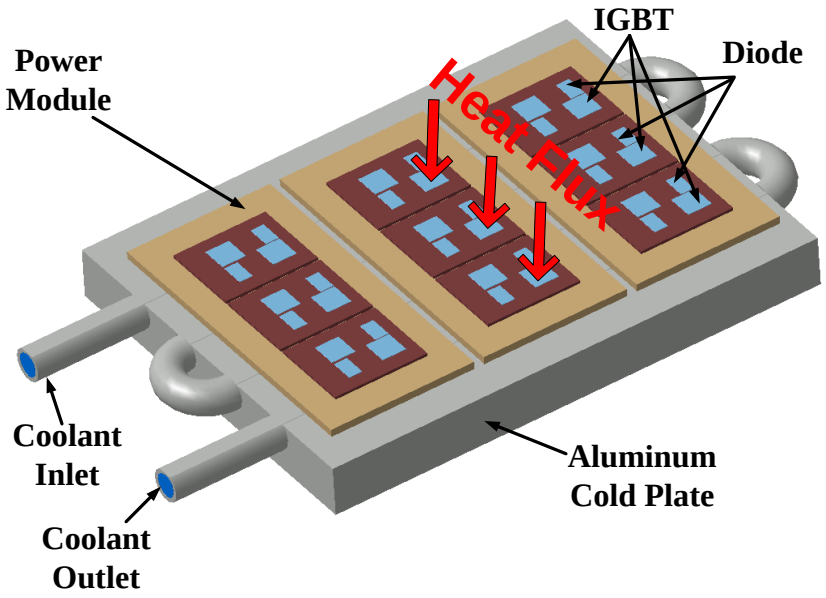


Fig. 3.13 3D model of the whole inverter

There are three power modules in the inverter as it is shown in Fig. 3.14, and each one corresponds to a phase of the inverter. The thermal parameters of the three power module are similar, so the power module of Phase B is chosen as an example for further discussion. As it has been mentioned in chapter 3.5.1, the 12 chips in one power module can be divided into four groups: #1. high-side IGBT, #2. low-side IGBT, #3. high-side diode and #4. low-side diode.

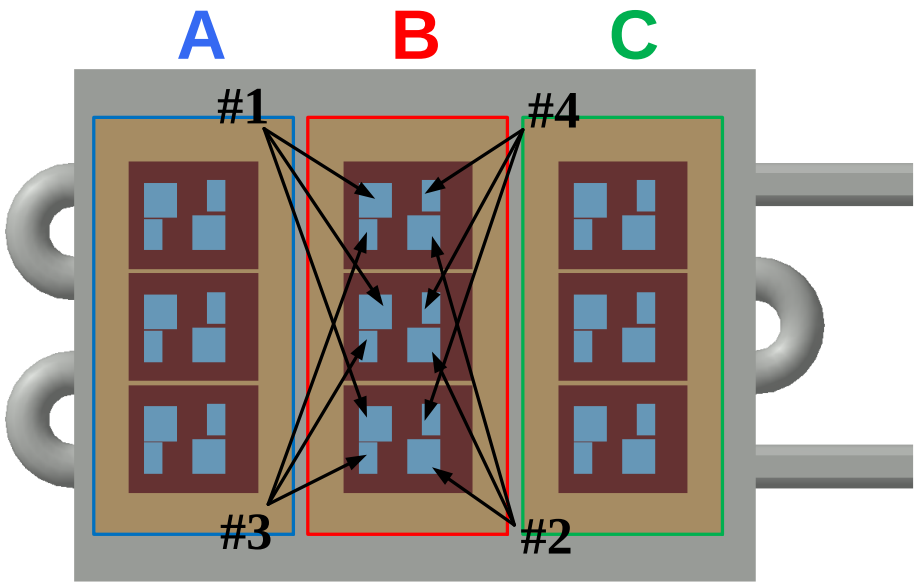


Fig. 3.14 Group of the chips in the studied power module

The chips in the same groups will always work together and dissipate heat simultaneously. Meanwhile, the layer structure and temperature of the chips in the same group are also similar to each other. So the self-heating and mutual-heating effects discussed in this chapter are all based on these groups instead of single chip.

3.6.1 Self-heating of the Chips

The self-heating thermal impedance for each group can be obtained by heating up all the chips in that group and calculating the step response by using (3.5). Again the average temperature on the top surfaces of all the heated chips in the group is record as the junction temperature. The temperature waveform is obtained from transient thermal analysis in ANSYS-FLUENT and the boundary conditions are listed in Table. 3.2.

Table. 3.2 Boundary conditions for the model in Fluent

Coolant Temperature at Inlet	338.15K (65℃)
Working Fluid	50% ethylene glycol 50% water mixture
Flow Rate	2L/min
Power Loss	100W per chip and 300W per group
Maximum Allowable Pressure Drop	5psi
Ambient Temperature	333.15K (60℃) in the case, 308.15K (35℃) in the ambient.
Coefficient of Convection with Air	6W/m^{2}K^{-1} in the case, 12W/m^{2}K^{-1} in the cabinet
Thermal Resistance of TIM(thermal interface material), R_{ch}	0.014K/W

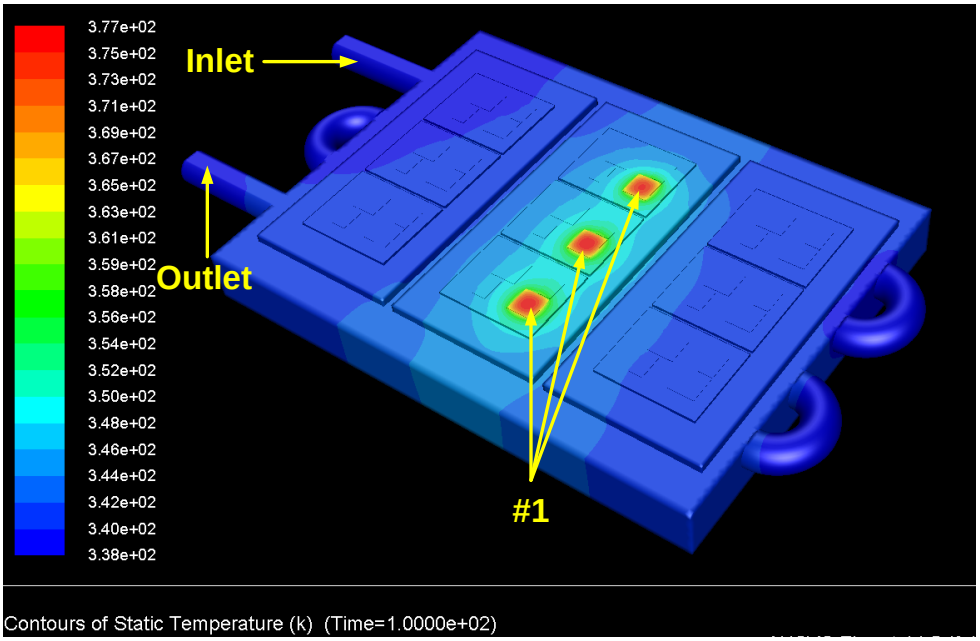


Fig. 3.15 Temperature distribution of the inverter at 100s when heat source is IGBT #1

To demonstrate the calculating progress, chips in IGBT #1(up-side IGBTs in Phase B) are heated as an example. The simulation time is set as 100s to make sure the junction

temperature reaches its stable value, and the temperature field of the whole system at 100s is shown in Fig. 3.15. It can be seen that the components located at the inlet side are of lower temperature, and the chips in the same group are of nearly the same temperature.

3.6.2 Thermal Cross-Coupling Effects

The temperature distribution of the chips is illustrated in Fig. 3.16, where obvious temperature rises can be observed in all the other chips beside IGBT#1 in phase B (the same power module). This is because these IGBTs and diode chips share the same substrates which sit on the same base plate of the power module. So when some IGBTs or diode chips are powered, the substrate and the base plate will be heated up and neighbor chips will also be heated up. This is what so called the thermal cross-coupling effect.

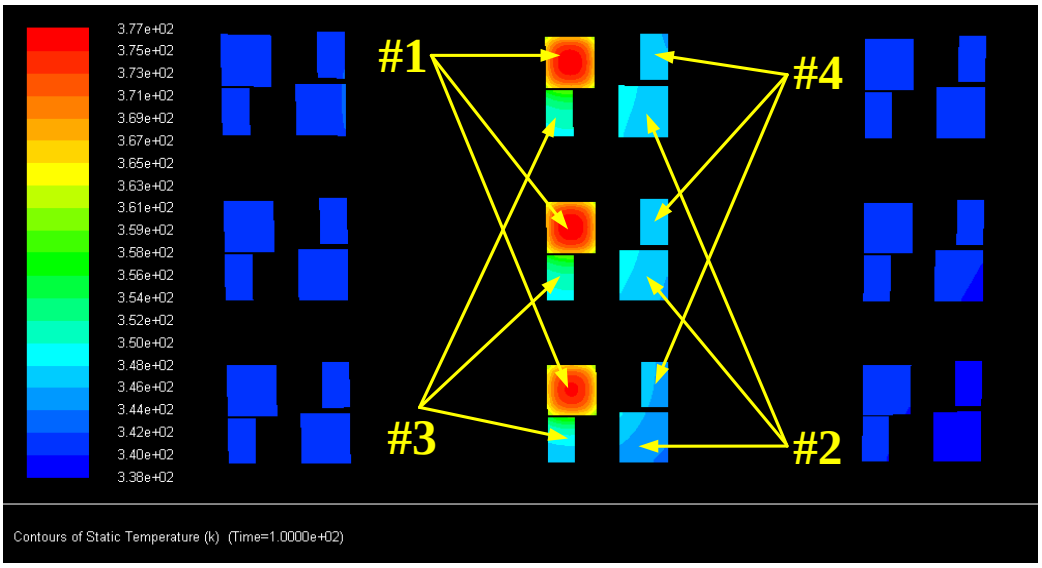


Fig. 3.16 Temperature distributions of the chips at 100s when heat source is IGBT #1

Since the thermal coupling effect cannot be neglect, ways to involve it into the thermal model need to be considered. When considering the thermal model of only the power

module, thermal cross-coupling effect has been described by using the mutual-heating thermal impedance and linear superposition in some recent literature [67]. This is because in this case only thermal conduction happened and a linear system can be assumed if the temperature dependency of the material's thermal conductivity and heat capacity can be ignored [68]. In the proposed model in this thesis, a similar way is used and the linearity of the entire system when considering the heat sink will be discussed later.

There are two groups of IGBTs and two groups of diodes in a power module, therefore 16 self-heating and mutual-heating thermal impedances should be calculated as it shows in Fig. 3. 17.

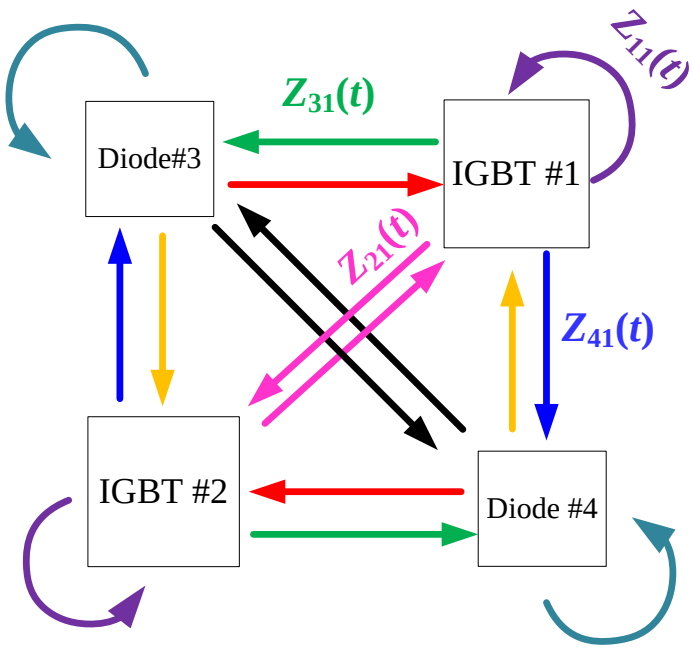


Fig. 3.17 Self-heating and mutual-heating thermal impedance

Then the total junction temperature rise of chips #i can be obtained by a linear superposition of the temperature rises caused by all of the heat sources around this chip in the same module.

$$\Delta T_i(\mathrm{s}) = \sum_{j=1}^{4} Z_{ij}(\mathrm{s})\,\mathrm{P_j}(\mathrm{s}) \tag{3.12}$$

where $P_j(s)$ is the heat flux on chip #j and $Z_{ij}(s)$ refers to the impact of the chip #i on the chip #j, when i=j, $Z_{ij}(s)$ represent the self-heating thermal impedance; and when i≠j, $Z_{ij}(s)$ represent the mutual-heating thermal impedance.

The mutual-heating thermal impedance can be calculated by heating one group of chips and measuring the thermal step responses of all other groups. The temperature rises of all the chips when IGBT#1 is heated up are shown in Fig. 3.18. As illustration, the maximum temperature rise happens at IGBT#1 itself. Meanwhile significant temperature can be found in diode#3 because it is closest to IGBT#1. Temperature rise for diode#3 and IGBT#2 are similar because they are of nearly the same distance to IGBT#1.

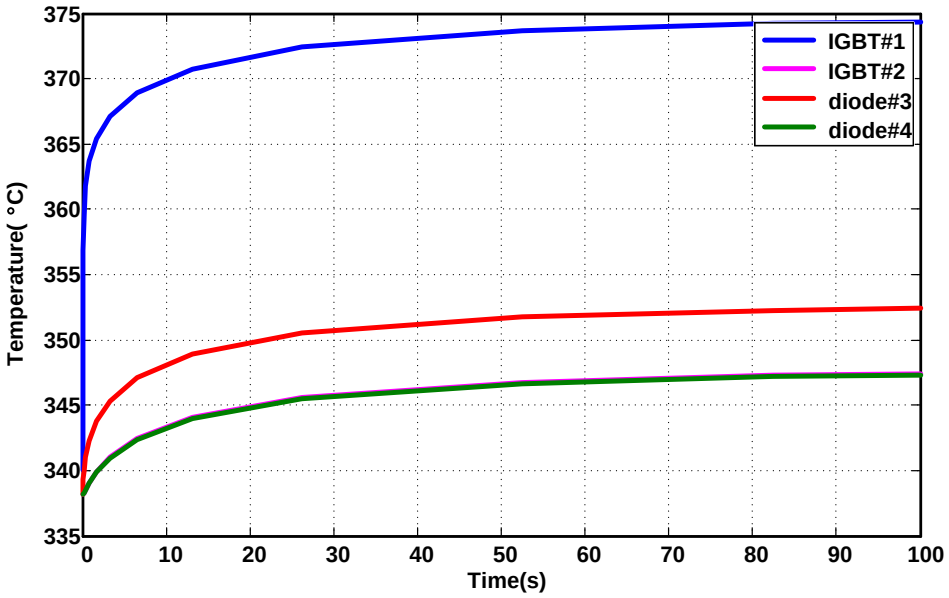


Fig. 3.18 Chips' temperature when heat source is IGBT #1

By using (3.5), the self-heating and mutual-heating thermal impedances when IGBT#1 is heated can be calculated as shown in Fig. 3.19. Comparing to the transient thermal impedance of the power module itself in Fig.3.12, it can be seen that the thermal time constant of the system increases from 0.04s to about 10s due to the large thermal inertia of the cold plate, and the chip temperature is not stable until 50s. In addition, it can be also seen that even a power loss lasting for 10^{-3}s will result in a noticeable temperature rise to the chips. For the mutual-heating thermal impedances, it is clear that and there is a delay in the temperature rise at the beginning because the chips only shares the same DCB layer and it takes time for the mutual heating effects to happen to the unheated chips.

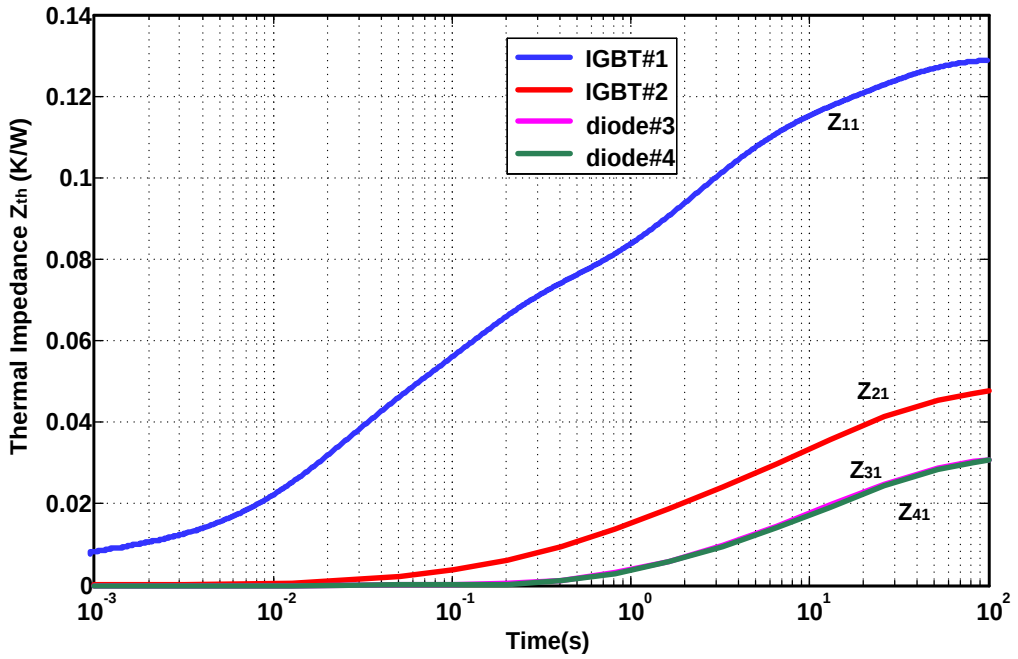


Fig. 3.19 Self-heating and mutual-heating thermal impedance when heat source is IGBT #1

As has been mentioned in chapter 3.3.2, these thermal impedance curves can be fitted into foster networks by least square method. Specifically, a fourth-order foster network can be used to describe the self-heating thermal impedance and a second-order foster network is enough to fit the mutual-heating thermal impedance. The schematic diagrams of these foster networks are shown in Fig.3.20 and the corresponding parameters are listed in Table. 3.3.

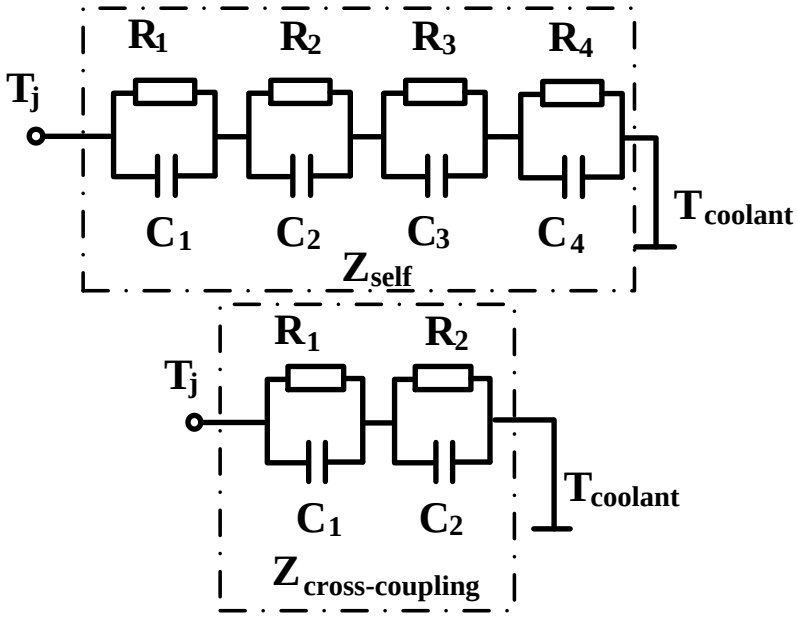


Fig. 3.20 Self-heating and mutual-heating thermal impedance foster network

Table. 3.3 Coefficients of the Foster Network for the IGBT#1

		1	2	3	4
IGBT#1-IGBT#1	R_i[K/W]	0.01201	0.05017	0.03859	0.02732
	τ_i[s]	0.000895	0.051706	1.47167	15.5521
IGBT#1-IGBT#2	R_i[K/W]	0.01204	0.01948		
	τ_i[s]	3.72301	24.474		
IGBT#1-Diode#3	R_i[K/W]	0.01771	0.02854		
	τ_i[s]	0.628536	13.7533		
IGBT#1-Diode#4	R_i[K/W]	0.01152	0.01806		
	τ_i[s]	3.644315	24.1371		

where τ_i is the time constant and $\tau_i = R_i \bullet C_i$

This process is repeated for 4 times to obtained all the 16 self-heating and mutual-heating thermal impedances in one power module and the self-heating and mutual-heating thermal impedances of diode#3 are shown in Fig. 3.21. It is easy to notice that the self-heating thermal impedance of the diode is larger than the IGBT because they are of much smaller areas.

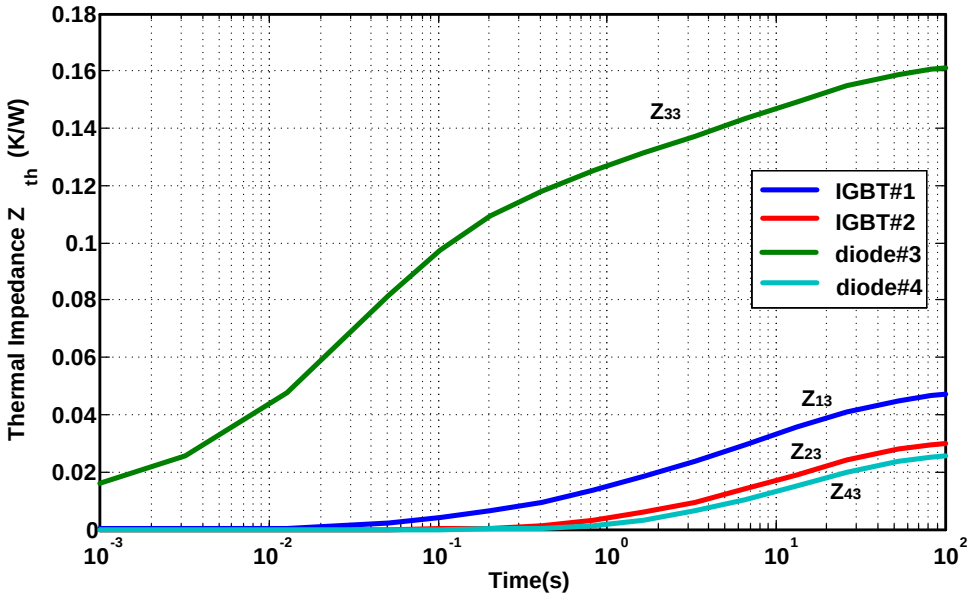


Fig. 3.21 Self-heating and mutual-heating thermal impedances when diode #3 is heated

3.7 VERIFICATION OF THE LINEARITY ASSUMPTION OF THE SYSTEM

Behavior based RC network model has been widely used in thermal modeling of power electronics, but it is based on the assumption of a linear system. It seems reasonable when applying this method to only the power module because it can be regarded as a quasi-one-dimensional heat conduction problem. However, the real system is not linear because

there is heat spreading effects in the 3D system and temperature dependences of the thermal properties of the materials. In addition, what users really concerns is the thermal performance of the entire system including both the power module and the heat sink. Involving the heat sink model will introduce heat convection to the system which could also be a nonlinear problem.

To establish confidence in the design and to support life-cycle-cost and reliability calculations, an accuracy of around 5% should be required for the thermal models in predicting chip temperature rise [69]. In this section, the linearity of the thermal model for the entire inverter will be discusses and the errors caused by the above factors will be presented.

3.7.1 Homogeneity of the System

Linear systems must satisfy two properties, superposition and homogeneity [70]. The property of homogeneity states that for a given input x, in the domain of the function F, and for any scalar α,

$$F(\alpha x) = \alpha F(x) \tag{3.13}$$

In the thermal model, the input is the power loss and the output is the temperature rise which can be regarded as $F(x)$. Model in ANSYS-FLUENT fully describes the 3D heat conduction and the heat convection process thus it is used to check the homogeneity of the system. Power losses of 30W per chip and 100W per chip are added to the system respectively, and the transient junction temperature rise in both conditions are recorded as it is shown in Fig. 3.22.

There are some differences of the temperature distribution since the power loss in the second simulation is about 3 times larger than the first one. However if the system is of good homogeneity, the transient junction temperature rise should increase by the same proportion and according to (3.5) the transient thermal impedances should be of the same value.

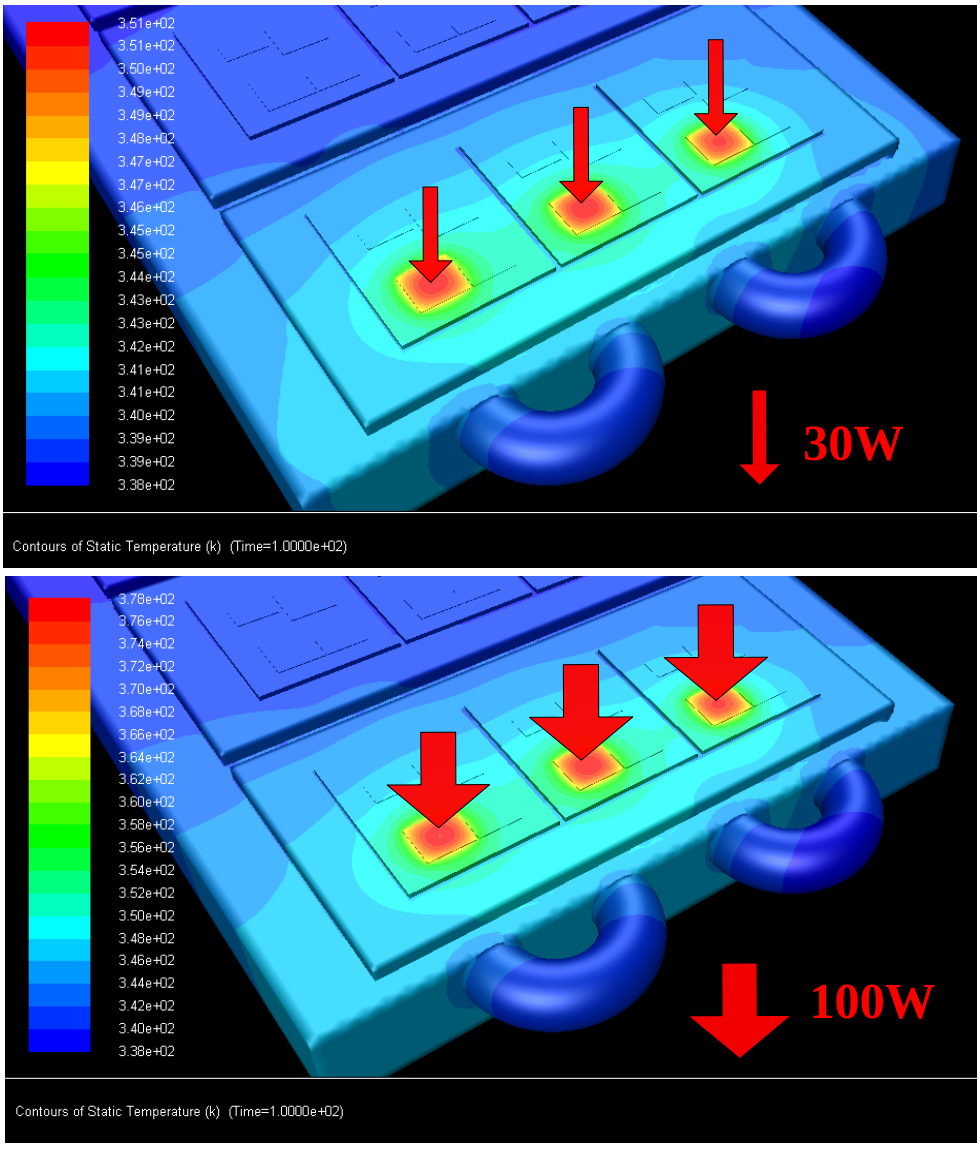


Fig. 3.22 Temperature rise distribution with 90w and 300w power loss respectively

The comparison of the transient thermal impedances under these two conditions is shown in Fig. 3.23. The thermal impedances are almost exactly the same except for the stable value with an error of 1.6%. The thermal impedance for 300w is smaller, because larger losses lead to higher temperature thus the heat spreads more widely on the heat sink, and the heat convection is more sufficient.

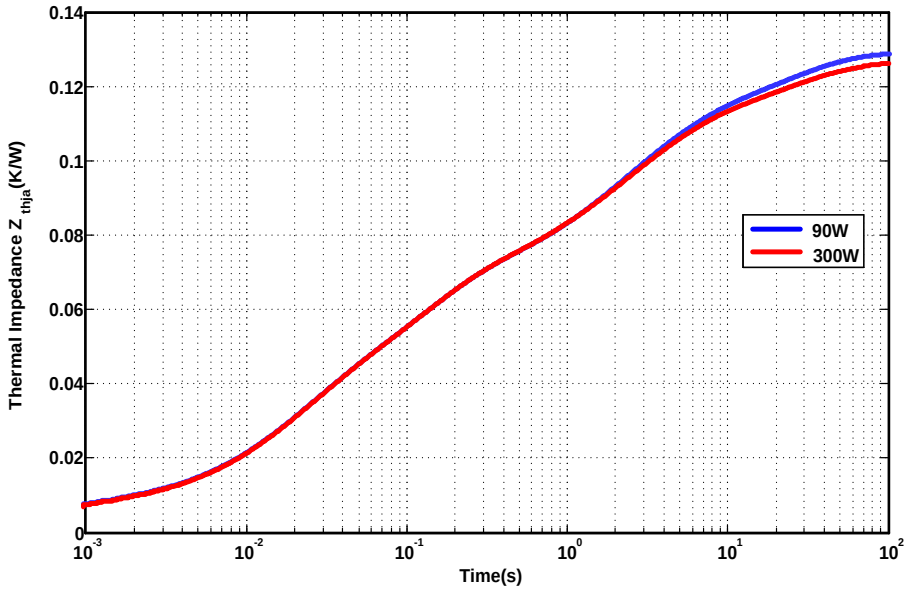


Fig. 3.23 Thermal impedance curves when heat source IGBT#1 in phase A with 90w and 300w power loss

3.7.2 Properties of Superposition of the System

The principle of superposition states that for different inputs x_i, in the domain of the function F,

$$F(x_1 + x_2 + \cdots) = F(x_1) + F(x_2) + \cdots \tag{3.14}$$

Again the input of the system is the power loss and the temperature rise can be regarded as F(x). Take phase B as an example, there are four independent heat sources IGBT #1, IGBT#2, Diode#1, Diode#2. Firstly, 4 simulations are proceed by adding 100W power loss to each of the heat source with other heat sources inactive, and the temperature rises of all the heat sources versus time are recorded. So there will be 16 groups of values and IGBT #1 is considered as an example.

The temperature rise of IGBT #1 when each of the heat sources is active respectively is listed in Table 3.4.

Table. 3.4 Temperature rise of IGBT#1 with 100W power loss adding to each heat source

Time Step	Time (s)	Temperature rise (K) of IGBT#1 when heat source is			
		IGBT #1 ($F(x_1)$)	IGBT #2 ($F(x_2)$)	Diode #3 ($F(x_3)$)	Diode #4 ($F(x_4)$)
0	0.0000	0.0000	0.0000	0.0000	0.0000
1	0.0002	0.3653	0.0000	0.0000	0.0000
2	0.0008	0.7960	0.0000	0.0000	0.0000
3	0.0032	1.2924	0.0000	0.0036	0.0000
4	0.0128	2.5184	0.0000	0.0422	0.0000
5	0.0512	4.6013	0.0012	0.2161	0.0000
6	0.1024	5.5950	0.0083	0.3866	0.0044
7	0.2048	6.5776	0.0367	0.6254	0.0302
8	0.4096	7.3917	0.1205	0.9520	0.1133
9	0.8192	8.1000	0.3003	1.3735	0.2894
10	1.6384	9.0133	0.5900	1.8637	0.5651
11	3.2768	10.0834	0.9748	2.3936	0.9285
12	6.5536	11.0316	1.4433	2.9603	1.3709
13	13.1070	11.7066	1.9780	3.5536	1.8758
14	26.2140	12.2340	2.5022	4.0953	2.3651
15	52.4290	12.6667	2.9036	4.4861	2.7336
16	82.4290	12.8167	3.0825	4.6537	2.8953
17	100.0000	12.8469	3.1351	4.7009	2.9403

Now, power losses of various values are added to all the heat sources simultaneously as shown in Fig. 3.24. If the system satisfies the properties of superposition, the temperature

rise transient of IGBT#1 obtained in ANSYS-FLUENT, which can be regarded as $F(3x_1+2*x_2+1.5*x_3+1*x_4)$, should equal to $3*F(x_1)+2*F(x_2)+1.5*F(x_3)+1*F(x_4)$ by using the value in Table 3.4. A comparison of these two values versus time is shown in Fig. 3.25 and it can be seen that the temperature rise when all the chips are heated in ANSYS-FLUENT is smaller than the superposition value. This phenomenon can be also attributed to the heat spreading effects which lead to more sufficient heat convection in the first case. The error in this case is within 2% thus the properties of superposition are also satisfied.

From the above discussion, the thermal model of the entire inverter satisfies both the properties of homogeneity and the properties of superposition and it can be regarded as a linear system. Thus the behavior based RC network method can be applied to the whole system.

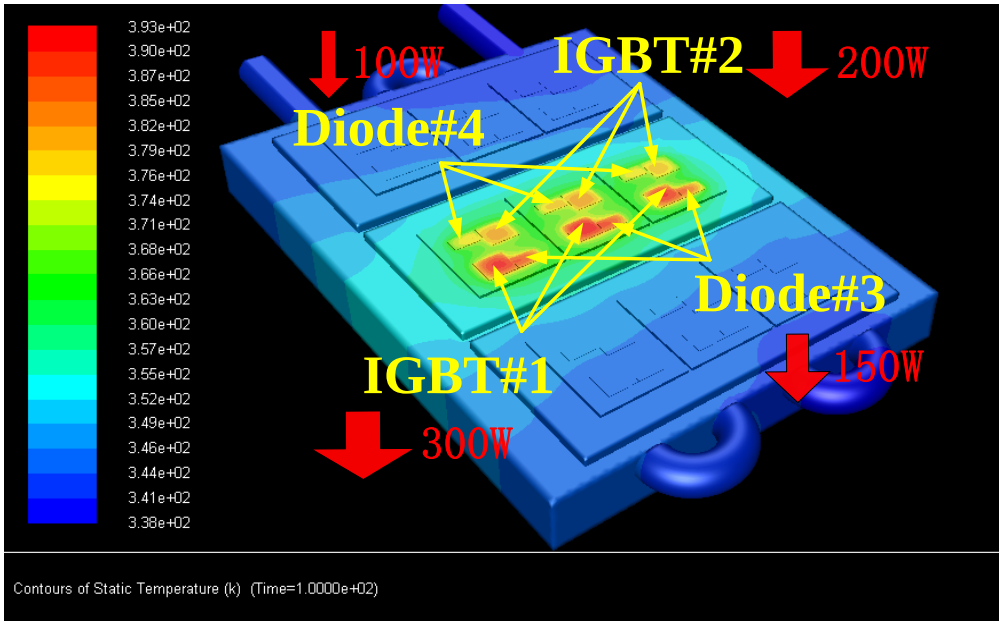


Fig. 3.24 Temperature rise distribution when all the chips in Phase B are heated

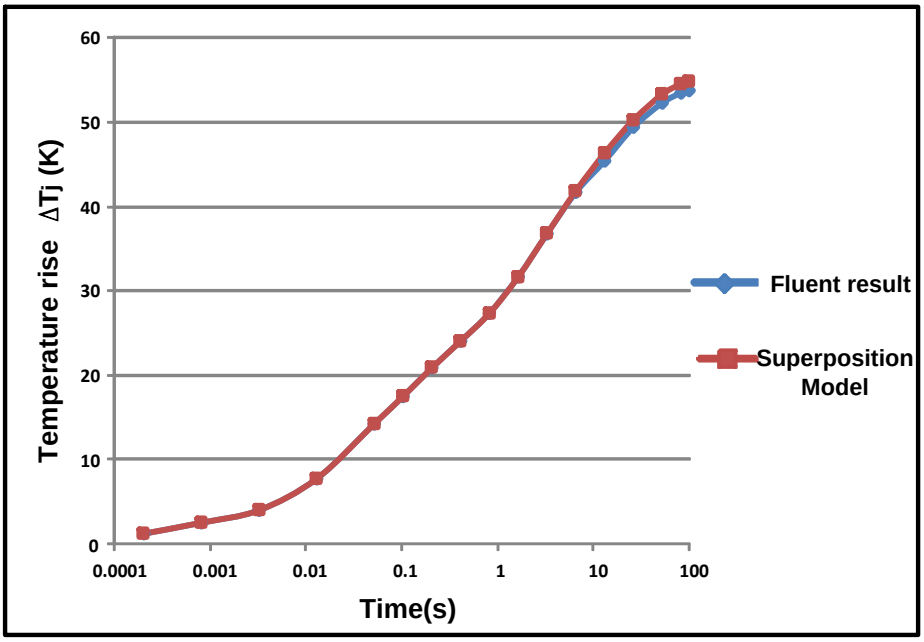


Fig. 3.25 Comparison between the temperature rise of IGBT#1 from ANSYS-Fluent and superposition model

3.8 TEMPERATURE DEPENDENCY OF THE THERMAL MODEL

As mentioned at the beginning of section 3.7, there are mainly three sources for the nonlinearities in the thermal model: the heat spreading effects, the heat convection process and the temperature dependence of the material properties. The first two factors have been evaluated in the previous section and the last factor will be discussed in this section.

3.8.1 Temperature Dependence of the Materials' Thermal Properties

The impact of the temperature dependence of materials' thermal properties to the thermal model has always been controversial. It has been ignored in practice for years [38] [71-

72], meanwhile errors from 4% to 12% caused by using the temperature independent assumption have been observed [64] [73].

There are two thermal properties of the materials, thermal conductivity λ and heat capacity C_{th}. Fortunately, the temperature dependence of heat capacity can be negligible in the 0-150°C range [74], so the thermal conductivity is the main factor need to be considered.

Materials' thermal conductivities may vary significantly in a wide temperature range. However the semiconductors work in a range of 250-450K.

Fig. 3.25 shows the temperature dependence of the thermal conductivities of materials commonly used in an inverter [75]. As illustrated in the figure, pure metals such as aluminum and copper show very little temperature dependence of λ and only the silicon and Al_2O_3 varies sufficiently over the temperature of interest.

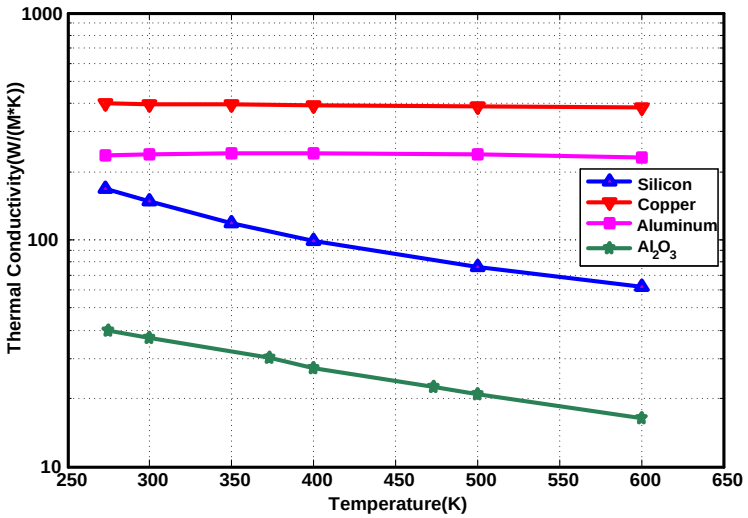


Fig. 3.26 Temperature dependent thermal conductivities of materials[73]

There are different ways to describe the relationship between the thermal conductivities and the temperature. And the exponential correlations of the thermal conductivities as functions of temperature in degrees K is of the most widely used and can be expressed as

$$\lambda(T) = \sum_{i}^{n} \lambda_i \exp(\alpha_i(T)) \tag{3.15}$$

where λ_i and α_i are the coefficients of temperature dependence of λ. By using the data in Fig.3.26，these values for silicon and Al_2O_3 can be obtained and are listed in Table 3.5.

Table. 3.5 α and λ values for the temperature dependence of thermal conductivity

	λ_1(W/(m·K))	α_1(1/K)	λ_2(W/(m·K))	α_2(1/K)
Silicon	1466	-0.01115	154.2	-0.001569
Al_2O_3	90.52	-0.002999	0.02319	0.006768

3.8.2 Influence on the Thermal Model

To evaluate the errors caused by neglecting the temperature dependence of the materials' thermal properties, a full nonlinear CFD model is built in ANSYS-FLUENT and the temperature dependence is defined by using the relationship in (3.15). The thermal impedance curve is a comprehensive description of the thermal model thus it is used again to evaluate the error. The transient simulation is repeated on gradually increasing ambient temperatures from 338.15K (65°C) to 418.15K (145°C), and a comparison between the linear model and the nonlinear model under different ambient temperature is shown in Fig.3.27.

As shown in the figure, the thermal impedance increases as the ambient temperature rises because the thermal conductivities of both Al_2O_3 and silicon become smaller at higher temperature.

Specifically, comparing to the linear model with a constant thermal conductivity at 338.15K, the error can be as large as 15% when the ambient temperature is set as 418.15K (145°C). And even comparing to the temperature dependent model with an ambient temperature of 338.15K, the error is still about 6%.

Furthermore, these errors are mainly caused by changes of the thermal conductivity of Al_2O_3, instead of the changes of the thermal conductivity of silicon which has been traditionally regarded as a main nonlinear source. The reason is that though both of their thermal conductivity changes significantly with temperature, the silicon layer is of much smaller area and thickness than the Al_2O_3 layer, and the thermal conductivity of silicon is also much larger than the Al_2O_3. Thus according to (3.3), the thermal resistance of the silicon layer takes up only a tiny fraction of the thermal resistance of the whole thermal system and would have very little impact on it.

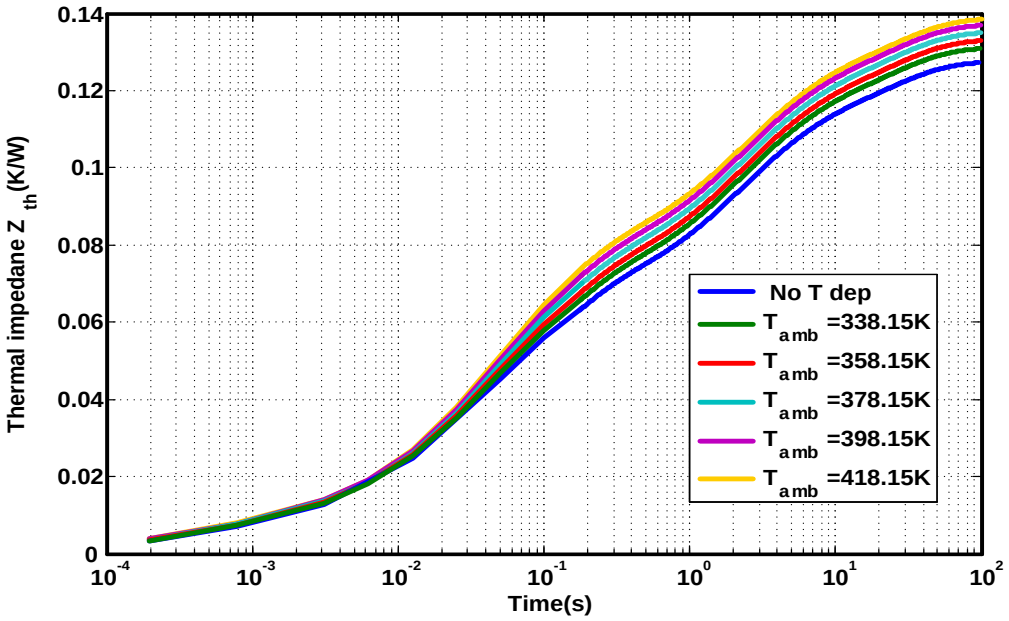


Fig. 3.27 Thermal impedance curves under different ambient temperatures

There are no perfect solutions in these cases. In literature [76], a method to generate a temperature dependent physical based thermal network model is proposed, but it is assumed there are only four layers in the power module while there should be at least 7 layers which will make the model very complicated.

A simple thermal model is very important for electro-thermal simulation. Normally the operating range and maximum temperature rise of the inverter is known. Therefore, thermal conductivity of silicon and Al_2O_3 at the average temperature rise is used to build the thermal model in this thesis. A comparison of this simplified model and the full temperature dependent model with the coolant inlet temperature at 338.15K is shown in Fig.3.28, and it can be seen that the error in this case can be reduced from 6% to 1.3%.

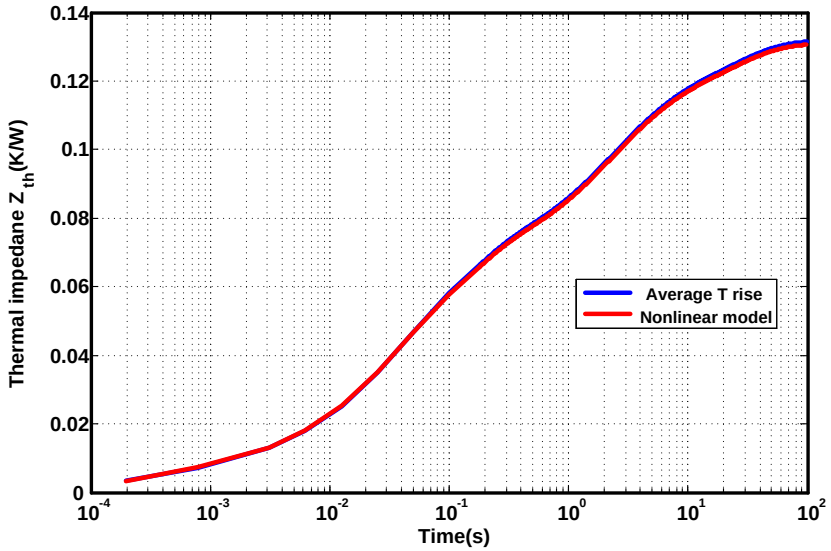


Fig. 3.28 Thermal impedance curves with constant thermal conductivities at the average temperature rise

It is also worth to note that boundary conditions may also be a nonlinear function of *T* due to the changes of coolant viscosity as shown in Fig. 3.29. However in most case the coolant temperature may not change too much thus the error without considering this factor is within 1% and can be ignored as illustrated in Fig. 3.30.

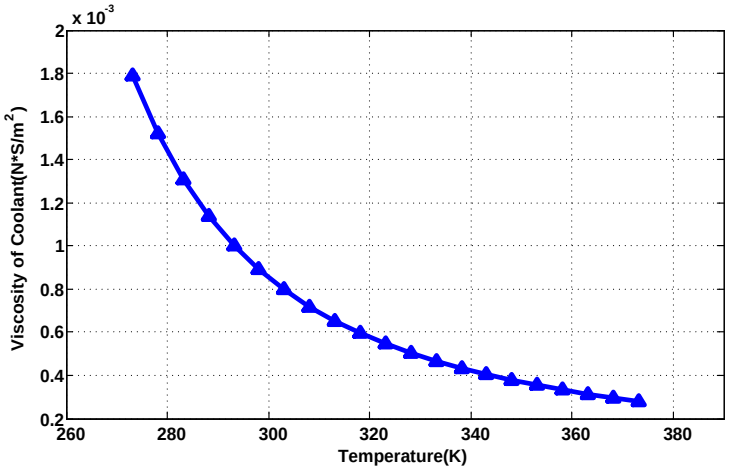


Fig. 3.29 Temperature dependence of the coolant viscosity

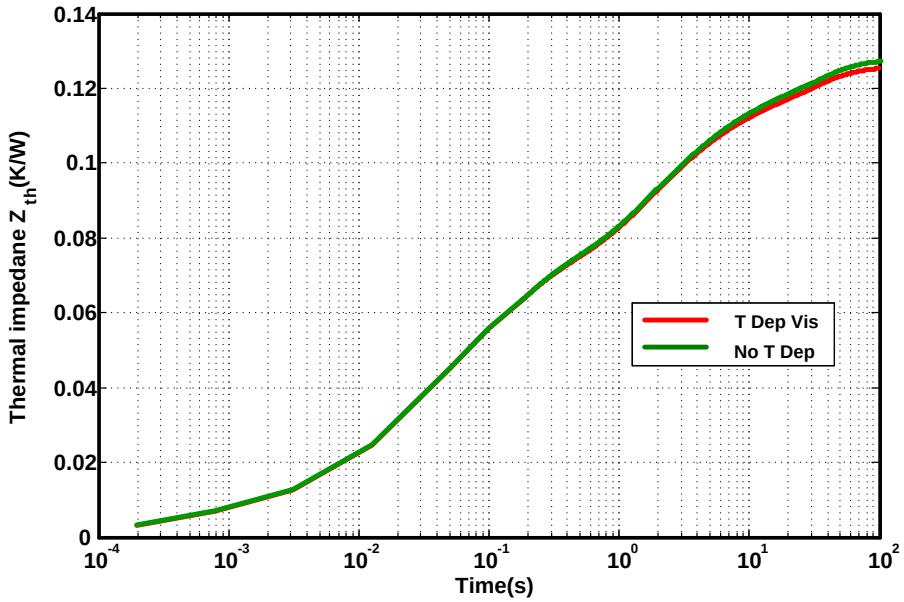


Fig. 3.30 Comparison of the thermal impedance curves with and without temperature dependence of the coolant viscosity

3.9 THERMAL MODEL FOR THE WHOLE INVERTER

The linearity of the thermal model of the whole system has been validated in chapter 3.7 and the errors caused by the nonlinear issues have also been discussed in chapter 3.8, thus the thermal model of the whole inverter can be developed based on the behavior based thermal network method.

In chapter 3.6, it has been mentioned that the chips in phase B can be divided into four groups and, therefore, there are 16 self-heating and mutual-heating thermal impedances, these thermal impedances can be obtained by repeating the simulation for 4 times with each chip group heated respectively. The temperature rise of any chips can be obtained by

a linear superposition of all the heat sources in the same module using (3.12). To simplify the problem, a 4x4 impedance matrix is defined to describe the model.

$$Z_B(\mathrm{s}) = \begin{bmatrix} Z_{\mathrm{B},11}(\mathrm{s}) & Z_{\mathrm{B},12}(\mathrm{s}) & Z_{\mathrm{B},13}(\mathrm{s}) & Z_{\mathrm{B},14}(\mathrm{s}) \\ Z_{\mathrm{B},21}(\mathrm{s}) & Z_{\mathrm{B},22}(\mathrm{s}) & Z_{\mathrm{B},23}(\mathrm{s}) & Z_{\mathrm{B},24}(\mathrm{s}) \\ Z_{\mathrm{B},31}(\mathrm{s}) & Z_{\mathrm{B},32}(\mathrm{s}) & Z_{\mathrm{B},33}(\mathrm{s}) & Z_{\mathrm{B},34}(\mathrm{s}) \\ Z_{\mathrm{B},41}(\mathrm{s}) & Z_{\mathrm{B},42}(\mathrm{s}) & Z_{\mathrm{B},43}(\mathrm{s}) & Z_{\mathrm{B},44}(\mathrm{s}) \end{bmatrix} \tag{3.16}$$

where $Z_{B,mn}(s)$ refers to the thermal impedance between chip #n and chip# m of phase B in s-domain. When n=m, $Z_{B,mn}(s)$ represents the self-heating thermal impedance, and when n≠m, $Z_{B,mn}(s)$ represents the thermal impedance due to mutual thermal coupling of chip #n on chip #m. hence, the temperature rise of chips in phase B can be expressed as:

$$\begin{bmatrix} \Delta T_{B1}(s) \\ \Delta T_{B2}(s) \\ \Delta T_{B3}(s) \\ \Delta T_{B4}(s) \end{bmatrix} = \begin{bmatrix} Z_{B,11}(s) & Z_{B,12}(s) & Z_{B,13}(s) & Z_{B,14}(s) \\ Z_{B,21}(s) & Z_{B,22}(s) & Z_{B,23}(s) & Z_{B,24}(s) \\ Z_{B,31}(s) & Z_{B,32}(s) & Z_{B,33}(s) & Z_{B,34}(s) \\ Z_{B,41}(s) & Z_{B,42}(s) & Z_{\mathrm{B},43}(s) & Z_{B,44}(s) \end{bmatrix} \begin{bmatrix} P_{B1}(s) \\ P_{B2}(s) \\ P_{B3}(s) \\ P_{B4}(s) \end{bmatrix} \tag{3.17}$$

where $T_{Bi}(s)$ and $P_{Bi}(s)$ refers to the temperature rise and power loss respectively in chip #i in s-domain.

To be more specific, the self-heating thermal impedance is in the form of a fourth-order foster network and the mutual-heating thermal impedance is in the form of a second-order foster network. The thermal network model of the corresponding to the thermal impedance matrix of phase B is shown in Fig.3.31, and the inverter can be represented by three thermal impedance matrixes.

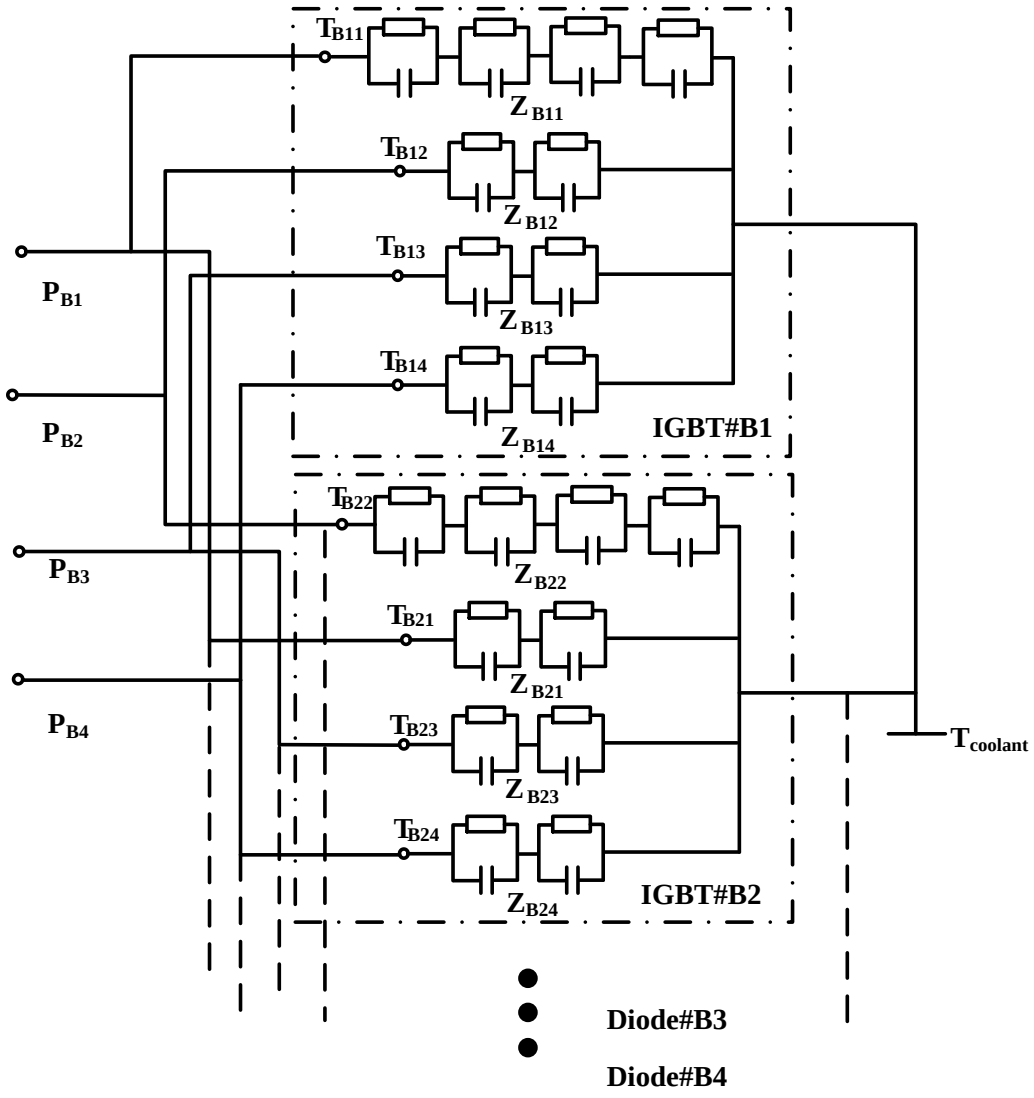


Fig. 3.31 Temperature network model for Phase B

3.10 EXTENSION OF THE THERMAL MODEL OF POWER MODULE WITH TO THE HEATSINK

In most cases, suppliers may not wish to reveal details of their design to preserve intellectual property and the inner structure and dimension of the IGBT module is unavailable to the thermal engineer. However the heat sink is designed or selected by the

engineer and the thermal impedance of the IGBT module is also available in the datasheet. So it is interesting and of great practical significance to discuss the possibility and accuracy of combining these two thermal subsystems to from the thermal model of the entire inverter.

3.10.1 Network Selection and Transformation

In most cases the thermal model is described as a Foster network as shown in Fig.3.32 because of its ease of parameter determination by linear-square fit to the measured or simulated thermal impedance. And it is fairly natural to consider to partition the network of a power module at node x and merge it to a foster network of the heat sink to extend the model.

However as it has been mentioned, the Foster network is only a behavior description of the system and has some natural contradictions to the physical features of heat transfer progress. For example, the heat propagation through the Foster network is instantaneous while in reality there is a delay because heat flow is driven by temperature difference and it needs time for the package to warm up before heating the heat sink. Meanwhile, in a Foster network the energy stored in a thermal capacitor depends on the temperature difference between adjacent nodes whereas in reality it depends on the absolute temperature of the components [61].

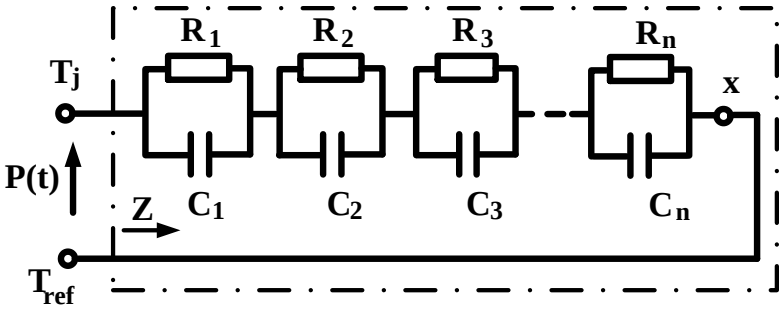


Fig. 3.32 Foster network of the package

Under this circumstance, the Cauer network is suggested to be a solution [61] [77]. The Cauer network, shows in Fig.3.33, has the same structure as the physical based RC network and provides a much more realistic physical description of the heat path.

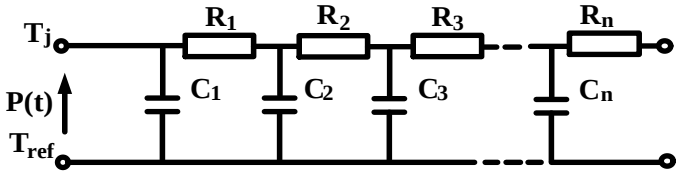


Fig. 3.33 Cauer network of the package

The transfer function corresponding to the Cauer network can be expressed as:

$$Z_{th}(s)=\cfrac{1}{sC_1+\cfrac{1}{R_1+\cfrac{1}{sC_2+\cdots+\cfrac{1}{R_n}}}} \tag{3.18}$$

And the transformation between Foster network and Cauer network can be achieved by using continuous-fraction expansion [54].

3.10.2 Comparison of Different Combination Methods of Thermal Subsystems

Although the Cauer network is supposed to be a better model than the Foster network for merging thermal subsystems, quantitative analysis of the errors can be hardly found for either method. Since combining models using Cauer and Foster networks are both very popular in literatures and practice [54][78][79][80], the feasibility and accuracy of applying these methods to the very typical liquid cooled cold plate and IGBT power modules will be discussed in this section as a reference for further application.

Firstly, the thermal impedance curve of the power module and the cold plate need to be obtained respectively. For the power module, the FEA result in Fig.3.12 is used, and for the cold plate a new simulation is carried out with a very important assumption that the heat flux is injected uniformly on the interface between the power module and the cold plate uniformly as shown in Fig.3.34. This assumption is reasonable. Because although there are hotspots where the IGBTs and diodes located, the materials of most layers inside the power module are of very high thermal conductivity, especially for the copper baseplate, which contacts the cold plate directly.

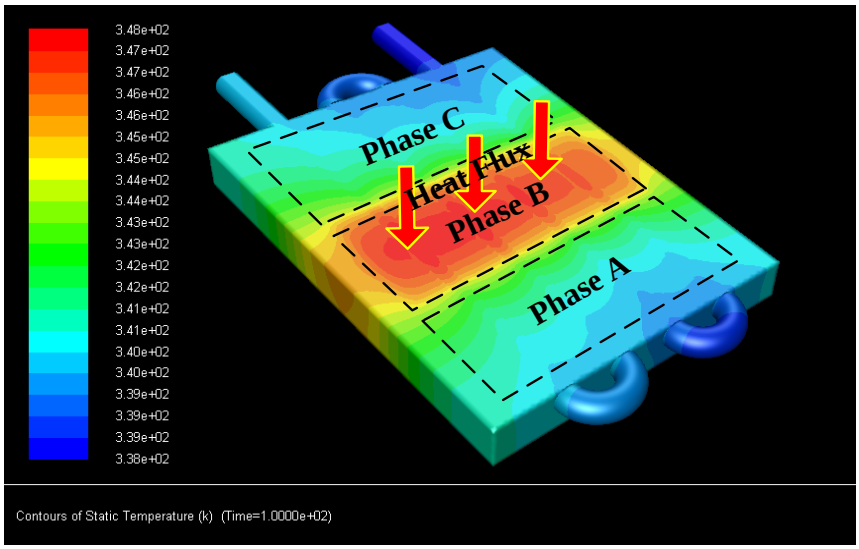


Fig. 3.34 Temperature distribution of the cold plate

Then the thermal impedance curve of the power module and the cold plate are fitted into a fourth order Foster network and a three order Foster network respectively and transformed into their corresponding Cauer networks. After that, they are merged together to form the whole thermal model of the system as it shows in Fig.3.35 and Fig 3.36. The corresponding R and C values of these networks are listed in Table 3.5 and a thermal grease model is also added between the power module and the cold plate to fully describe the system.

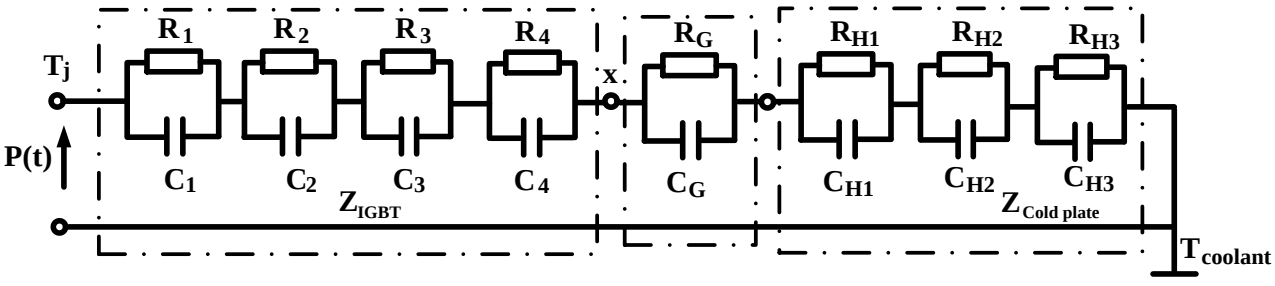


Fig. 3.35 Combined Foster network models of the IGBT and cold plate

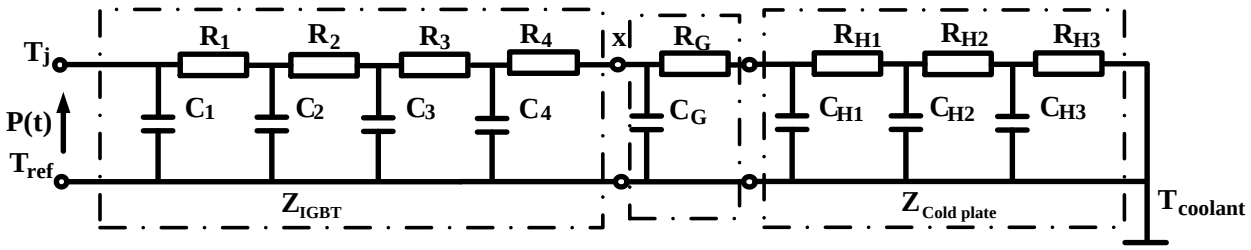


Fig. 3.36 Combined Cauer network models of the IGBT and cold plate

Table. 3.6 R and C values for the Foster and Cauer networks

	Foster		Cauer	
	R_i	C_i	R_i	C_i
1	0.007645	0.059778	0.009362	0.053956
2	0.02749	0.663696	0.036840	0.524654
3	0.03089	3.680803	0.026480	4.083481
4	0.02153	37.42685	0.014873	48.65232
G	0.014	3.889	0.014	3.889
H1	0.003984	31.29719	0.004984	27.906658
H2	0.007327	315.6408	0.009918	254.52028
H3	0.01587	1400.888	0.012280	1487.13352

The thermal impedance of the whole system has been obtained from transient simulation in Ansys-Fluent in section 3.5 based on detailed 3D system model, which can be regarded as an exact description of the systems' thermal response. And it is compared to the equivalent thermal impedances obtained from the combined Foster network model and combined Cauer network model, which are shown in Fig. 3.37.

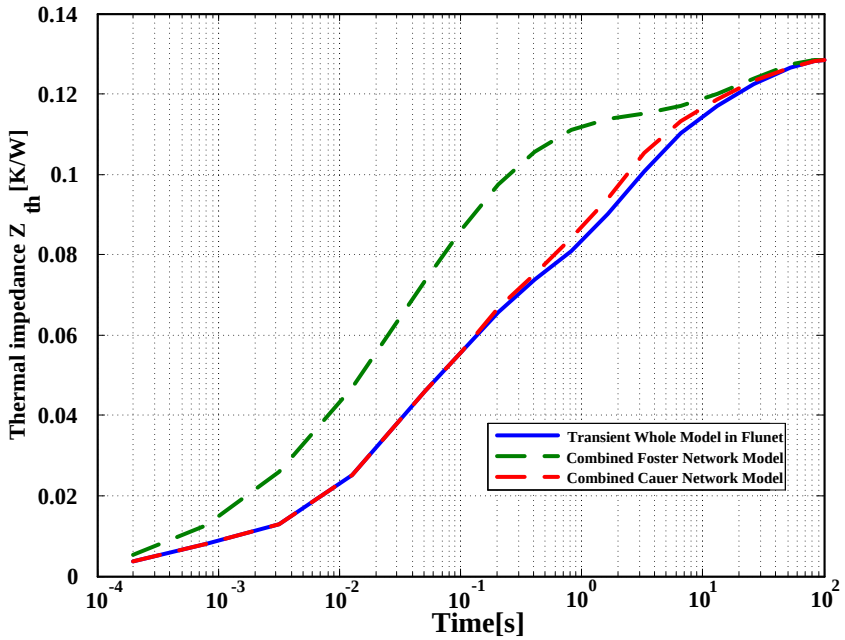


Fig. 3.37 Comparison of the thermal impedance obtained from different methods

From the figure, it can be seen that though both of the network model can finally provide an accurate steady state value, only the result obtained by combining separate Cauer network models is consistent with the transient simulation result. The maximum error in this case is just 5%, and this is because the Cauer network can maintain both the response characteristics and the independence of the subsystems. The tiny error is caused by the assumption of the uniformly distribution of heat flux on the contact surface between the power module and the cold plate.

On the other hand, combination of separate foster network models will result in enormous errors which can be as large as 107% at the first several hundred milliseconds. This can be attributed to the feature of simultaneous heating of different subsystems in Foster thermal network, which fails to describe heat flow and warm up progress of adjacent

systems. Specifically, the thermal time constant of the power module is around 0.1 second, and the thermal time constant of the liquid cooled cold plate used in the inverter is around 30 seconds and the simultaneous heating lead to a non-existent temperature rise on the cold plate at the first few milliseconds.

In conclusion, though the internal notes in these Cauer networks have no physical meanings, the combined Cauer network models can still be used to predict the case and junction temperature.

3.11 CONCLUSION

In this chapter, the advantages and drawbacks of different thermal modeling methods of power electronics are presented. Then the feasibility of using a behavior based RC network method to build the thermal model of the entire inverter contains both the power module and a liquid cooled heat sink is discussed. The existence condition of transient thermal impedance, linearity of the whole thermal system is validated and errors caused by some most controversial nonlinear issues are evaluated.

Based on the above results, the dynamic thermal network model of the entire inverter is proposed and the self-heating and thermal cross-coupling effects of different chips are both considered. A quantitative analysis is given about the errors when combining thermal subsystems of the power module and heat sink directly to form the thermal model of the entire inverter. Different network models are discussed and the result will be of great reference significance for the thermal system design when the inner structures and details of the power module are not available.

Chapter 4

TRANSIENT ELECTRO-THERMAL SIMULATION AND ANALYSIS

4.1 INTRODUCTION

The power loss of the IGBT modules used in the three-phase inverter was analyzed in chapter 2 and the thermal model of the whole inverter was developed in chapter 3. In this chapter, the model implementation for the transient electro-thermal simulation of the inverter in real time simulator will be presented.

Firstly, the electro-thermal simulation model will be built in MATLAB\SIMULINK. Then, this model is used to predict the transient behavior of junction temperature under different operating conditions, especially for the estimation of the "worst-case" junction temperature under stall torque condition. After that, the impact of the temperature dependency of power loss and the thermal cross coupling effects of multichip device to the transient junction temperature fluctuation will be discussed. These discussions will provide crucial information for the thermal system design, especially for the determination of the design margin and the reliability analysis of the inverter.

4.2 ELECTRO-THERMAL MODEL IMPLEMENTATION IN REAL TIME SIMULATOR

Simulink is a graphic block-oriented program for simulating dynamic systems which is widely used for simulation of control systems. In this thesis, the power loss model and thermal model will be built to carry out the electro-thermal simulation in Simulink.

4.2.1 Operating Principle of a Three Phase Inverter

The total power losses (conduction and switching losses) of IGBT and diode in an inverter are determined by the device characteristics and operating condition of the whole inverter (load, circuit topology, working sequence). On the device side, we have expressed the power losses of the IGBT and diodes as functions of the device current and junction temperature by using the datasheet and experimental results in Chapter 2. Thus it is now necessary to discuss the operating principle of the whole inverter to decide in what sequence and how the losses occur in each IGBT and diode during the operation.

The inverter used in this thesis is a three phase voltage-source inverter (VSI) and the objective of this inverter is to converts a DC input voltage to an AC output voltage to drive load. Fig. 4.1 shows the topology of the studied inverter. It is composed of three phases with two switches (IGBT) and two diodes in each phase.

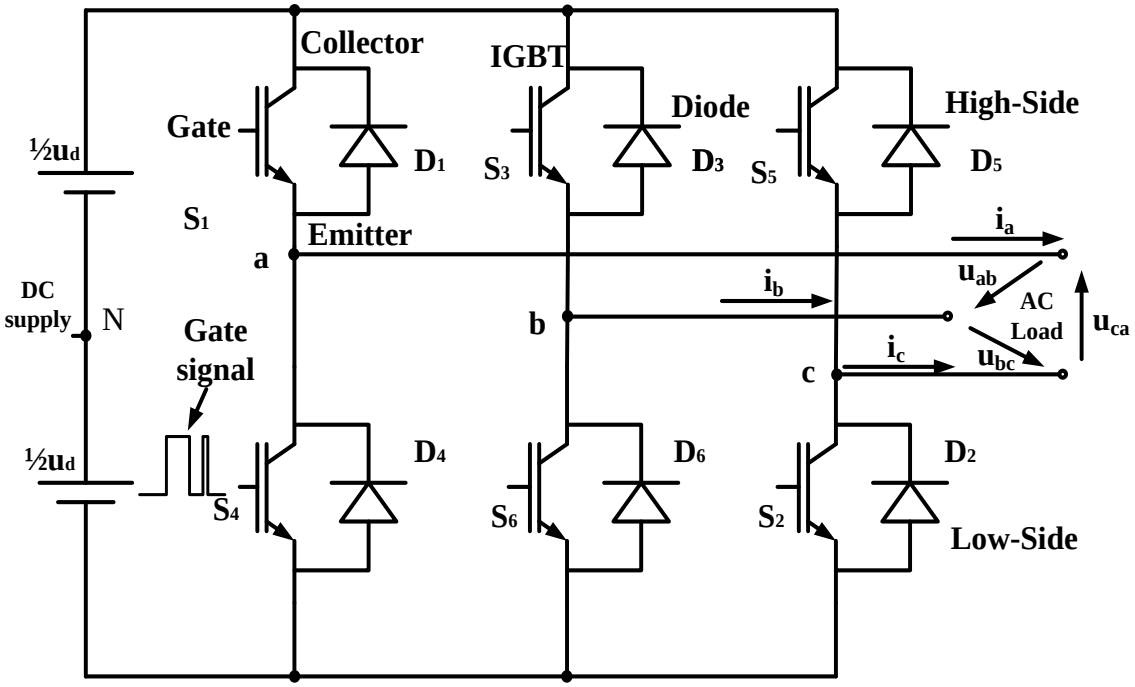


Fig. 4.1 Circuit diagram of the three phase inverter

In most applications, the amplitude, frequency and even phase of the AC output voltage generated in the inverter need to be adjustable and these requirements are realized by controlling the gate signal to turn on and turn off the switches (IGBT) at appropriate time periodically. Normally, the switching sequence is determined by using the pulse width modulation (PWM) technique and there are two typical types of PWM techniques: Sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) [81]. The SPWM technique is applied in this thesis, and the gate control signal in this method is generate by comparing a reference sine wave with a carrier triangular wave.

The detailed operating principle of the inverter is illustrated in Fig. 4.2. There are three output voltages u_{ab}, u_{bc} and u_{ca}, thus there are also three modulating signals u_{ma}, u_{mb} and u_{mc} (reference sinusoidal voltages to describe the desired ac output voltage). These modulating signals are compared to the triangular waveform (carrier signal) u_c to generate the gate control signals. The output voltages among different phases are of the same amplitude and frequency. Therefore, in order to simplify the problem, we only take phase *A* as an example to explain the signal generation process. The situations in phase *B* and phase *C* can be derived by applying a phase delay of 120˚, separately. In Fig. 4.2a and Fig. 4.2b, the gate control signal for switch S_1 and S_4 is generated by comparing the reference signal u_{ma} to the carrier signal u_c. When $u_{ma}>u_c$, the switch S_1 is on and the switch S_4 is off and the voltage $u_{an}=1/2u_d$; similarly, when $u_{ma}<u_c$, the switch S_1 is off and the switch S_4 is on and $u_{an}=-1/2u_d$. The state of switches S_3 and S_6 and waveform of u_{bo} can be obtained as shown in Fig. 4.2c. The line voltage $u_{ab}=u_{an}-u_{bn}$ is shown in Fig. 4.2d. It is consist of a series of discrete pulses; however it can be demonstrated that this waveform is equivalent to a continuous sinusoidal voltage $u_{ab,equ}$(the red dash line) [82]. The load current i_a is shown in Fig. 4.2e, and it becomes a continuous waveform with a delay to u_{ab} due to the inductive elements in the load devices (electric motor).

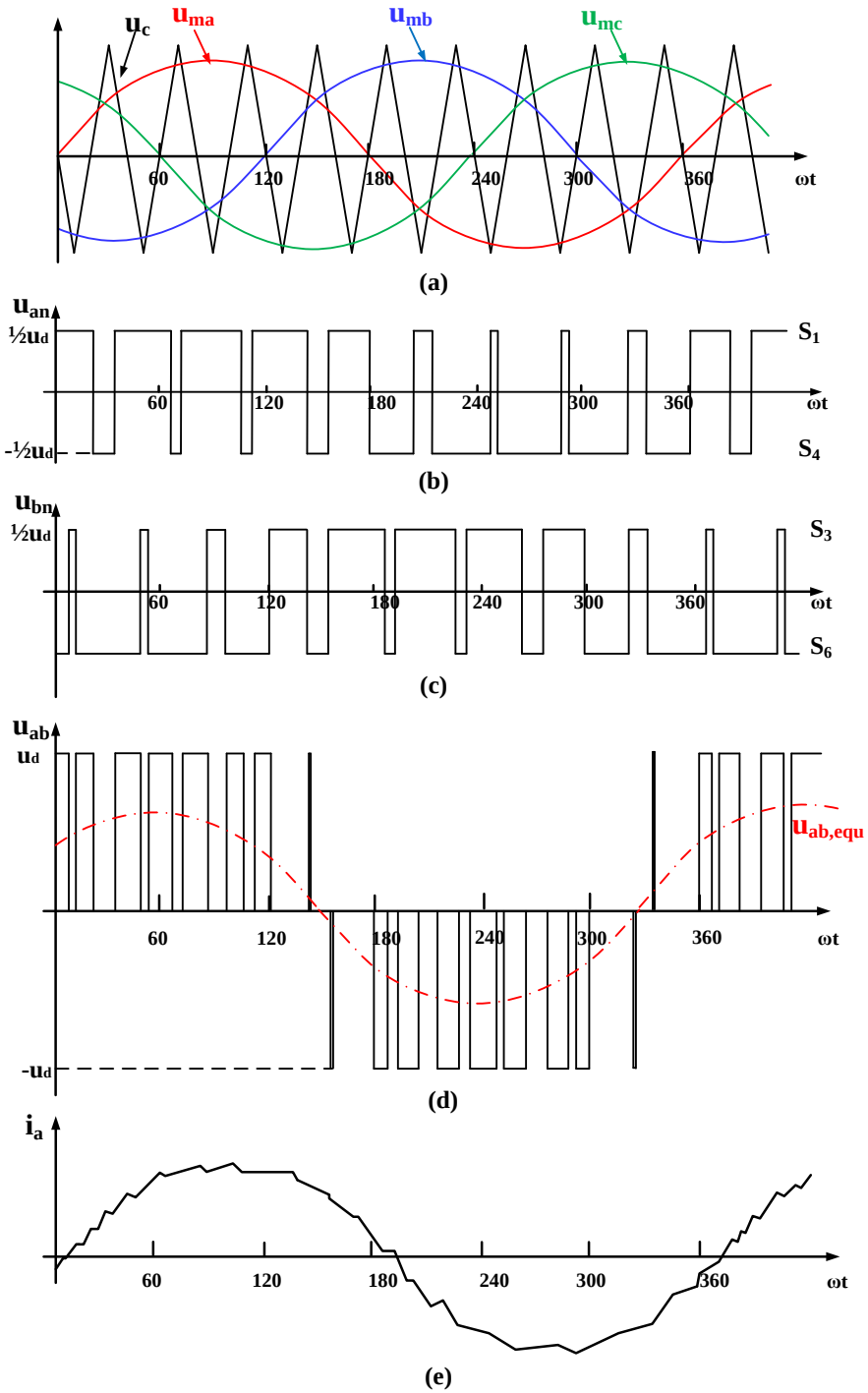


Fig. 4.2 Ideal waveforms for the SPWM (frequency-modulation ratio=9, amplitude-modulation ratio=0.8): (a) Carrier and modulating signals; (b) u_{an}; (c) u_{bn}; (d) Line-to-line voltage u_{ab}; (e) Load curren i_a

4.2.2 Electro-Thermal Model Implementation in Real Time Simulator

In chapter 2, the switching losses have been measured under different currents and device temperatures at certain DC-link voltage, applied gate-voltage and gate resistor. The conduction loss is expressed as a function of the device current and temperature as shown in 2.10. Meanwhile, in chapter 3 the thermal model of the whole system in the form of thermal impedance matrixes has been implemented. By combining these two models, the electro-thermal model can be built to predict in real time the junction temperature of the inverter.

The diagram of the electro-thermal model is shown in Fig. 4.3. In order to take into account the effects of the junction temperatures on the power losses, the estimated junction temperatures are fed back to the power loss calculation and the thermal coupling effects are considered in the thermal model. The total power losses of the IGBT are composed of the switching losses and the conduction losses, and the power losses of the diode are composed of the conduction losses and diode recovery losses. They are all functions of the current and junction temperature. Furthermore, the junction temperatures of the IGBTs and Diodes are different. Therefore, the power losses and junction temperatures of different devices are calculated separately. Actually, the power losses of the IGBTs or diodes in the high-side and low-side are also different. But the calculating methods for the same-side devices are similar and, therefore, they are not shown in the diagram.

As shown in Fig. 4.3, the power loss in each device (IGBT or diode) depends on the conducted current and temperature in that device, thus we need to decide when and which device is conducting the current to get the power loss profile of that device in the simulation model.

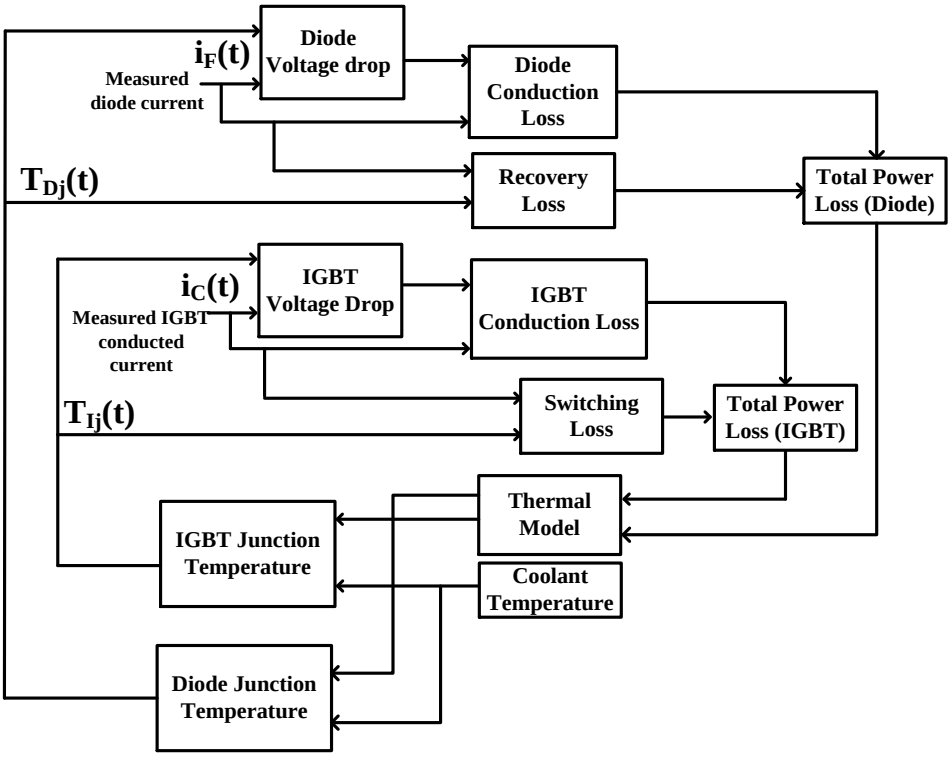


Fig. 4.3 Diagram of the electro-thermal model

The IGBTs and Diodes in phase *A* are discussed as an example as it shows in Fig. 4.4. The judgement method for the current path is as follow: when the high-side IGBT S_1 is on and S_2 is off, if the load current i_a is positive, then the current flows through the S_1 itself. However if the current is negative, then the current could only flow through the high-side diode D_1. Oppositely, when S_1 is off and S_4 is on, if the load current is positive, then the current flows through the low-side diode D_4, otherwise it flows though S_4.

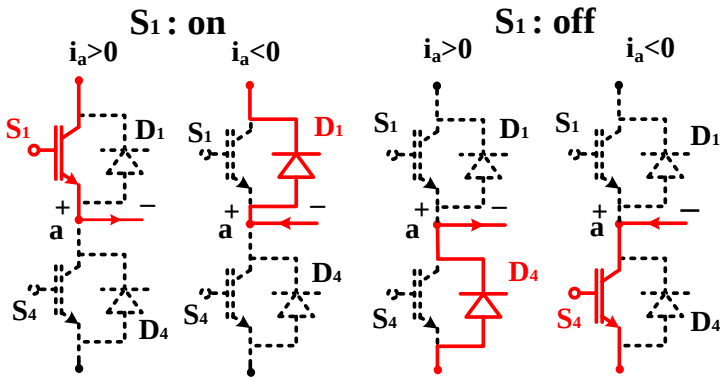


Fig. 4.4 Current commutation with current paths highlighted [83]

Now, by comparing the switch status of S_1 and the load current, the conducted current in IGBT S_1 and diode D_4 can be obtained as it shows in Fig.4.5. And similarly, the conducted current in IGBT S_4 and D_1 can be calculated.

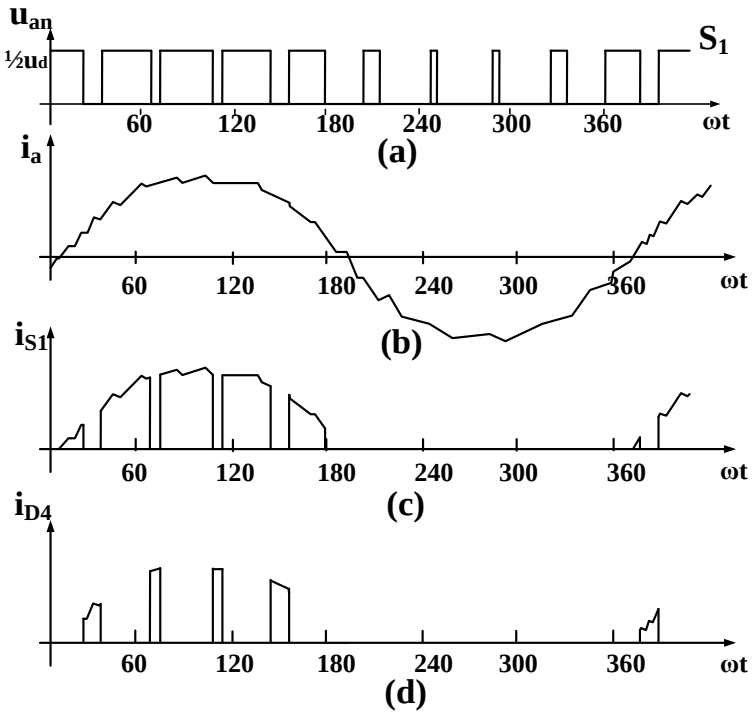


Fig. 4.5 Determination of the conducted current:(a) Switches state in phase *A*; (b) Load current i_a; (c) Conducted current in IGBT S_1; (d) Conducted current in Diode D_2

Since the conducted current in each device is decided, the power losses (conduction losses and switching losses) can be added as follow: when the current is positive, and if switching status of S_1 in the adjacent two steps are detected changing from off to on (0 to 1), then a switching on loss is add to the IGBT S_1, the value is obtained from the lookup table in Chapter.2 by using the instantaneous current and junction temperature of S_1. Oppositely, if a changing of the switch state from on to off (1 to 0) is detected, then a switching off loss is added to IGBT S_1. Meanwhile, the real-time conduction loss is calculated by applying 2.10 and added to S_1 between these two statuses as it shows in Fig.4.6.

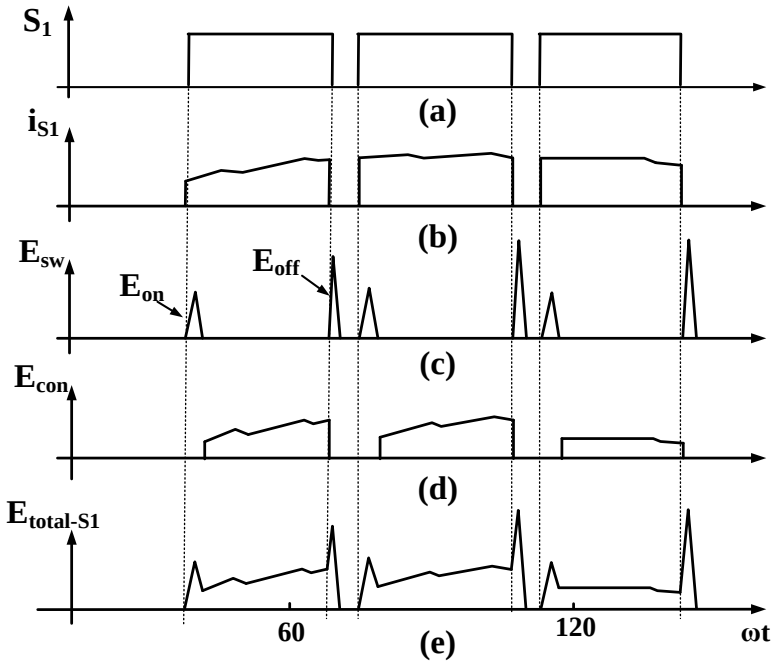


Fig. 4.6 Determination of the trigger signal for power losses in IGBT S_1: (a) Switches state of S_1; (b) Conducted current in IGBT S_1; (c) Switching losses on S_1; (d) Conduction losses on S_1; (e)Total losses on S_1

Similarly, when current is positive, and if the switching status of S_1 in the adjacent two steps changes from on to off (1 to 0), then a conduction loss is add to the diode D_4 until the switching status changes from off to on (0 to 1) when a recovery loss add on D_4 as it is shown in Fig 4.7.

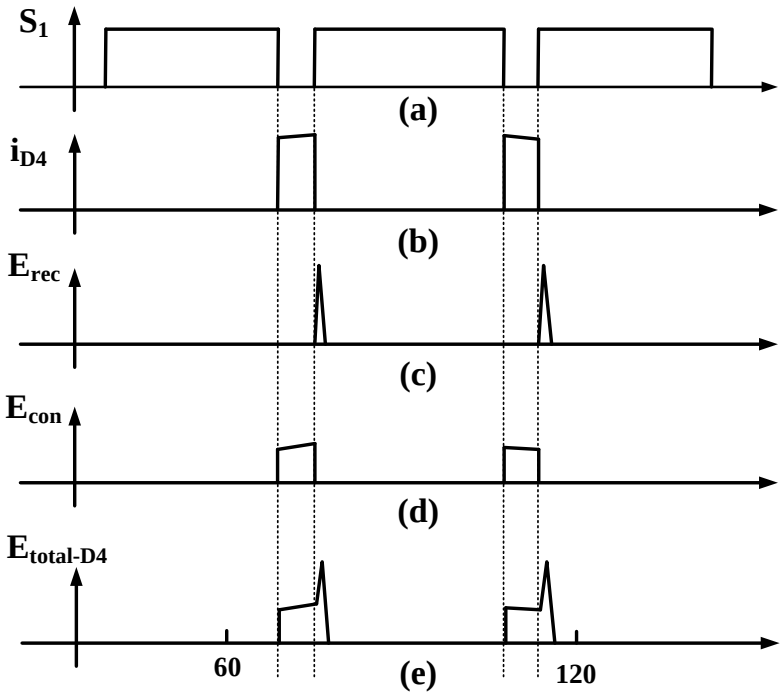


Fig. 4.7 Determination of the trigger signal for power losses in Diode D_4: (a) Switches state of S_1; (b) Conducted current in Diode D_4; (c) Recovery losses on D_4; (d) Conduction losses on D_4; (e)Total losses on D_4

4.2.3 Electro-Thermal Simulation and Time Step Determination (Instantaneous vs. Average Power Loss Over Long Time Operation) in Long Term Simulation

By using the above power loss model in each device and the thermal network model discussed in Chapter 3, the electro-thermal model can be built. To provide a realistic

power loss waveform for junction temperature evaluation, the model is composed of the inverter, a DC voltage source and an interior permanent magnet synchronous motor (IPMSM). The parameters of the inverter are set as follows: DC link voltage V_{DC}=300 V, switching frequency f_{sw}=10 kHz, fundamental frequency (modulation frequency) f=100 Hz and modulation index h=0.8. The next step is to determine the time step and simulation time, which is a big problem because the thermal and power loss properties of the system are both of wide spread time scales.

On one hand, from the perspective of the power loss, heat generated in any chips of the inverter oscillates at two frequencies, one in the range of 100 Hz corresponding to the load current modulation frequency, and another one at the level of 10 kHz corresponding to the switching frequency. The switching time is only about 300 to 400 nanoseconds, so even though we have used the measured switching loss instead of calculating it by modeling the detailed switching process, the time step still could not be too large.

On the other hand, as has been depicted in Fig. 3.19, it needs at least 40 seconds for the junction temperature to achieve its stable value, so the simulation time need to be larger than that. However, it can be also seen that the system could response to a very short heat impulse (even 10^{-3} second) because of the small thermal time constant of the chips. This might be a big problem when considering the switching losses which happens in a very short time but is of very large amplitude, thus the time step need to be small enough to fully describe the power loss model.

From the above discussion, it is clear that the time step depends on how detailed the loss need to be modeled, especially for the switching losses. In order to evaluate the impact of the losses to the temperature, the simulation is carried with a time step of 10^{-7}s and a simulation time of 1s.

The power loss waveform is shown in Fig. 4.8, and it was zoomed in to 40ms (Fig. 4.9) and 400μs (Fig. 4.10) which corresponds to the losses oscillating at the modulation frequency and the switching frequency respectively.

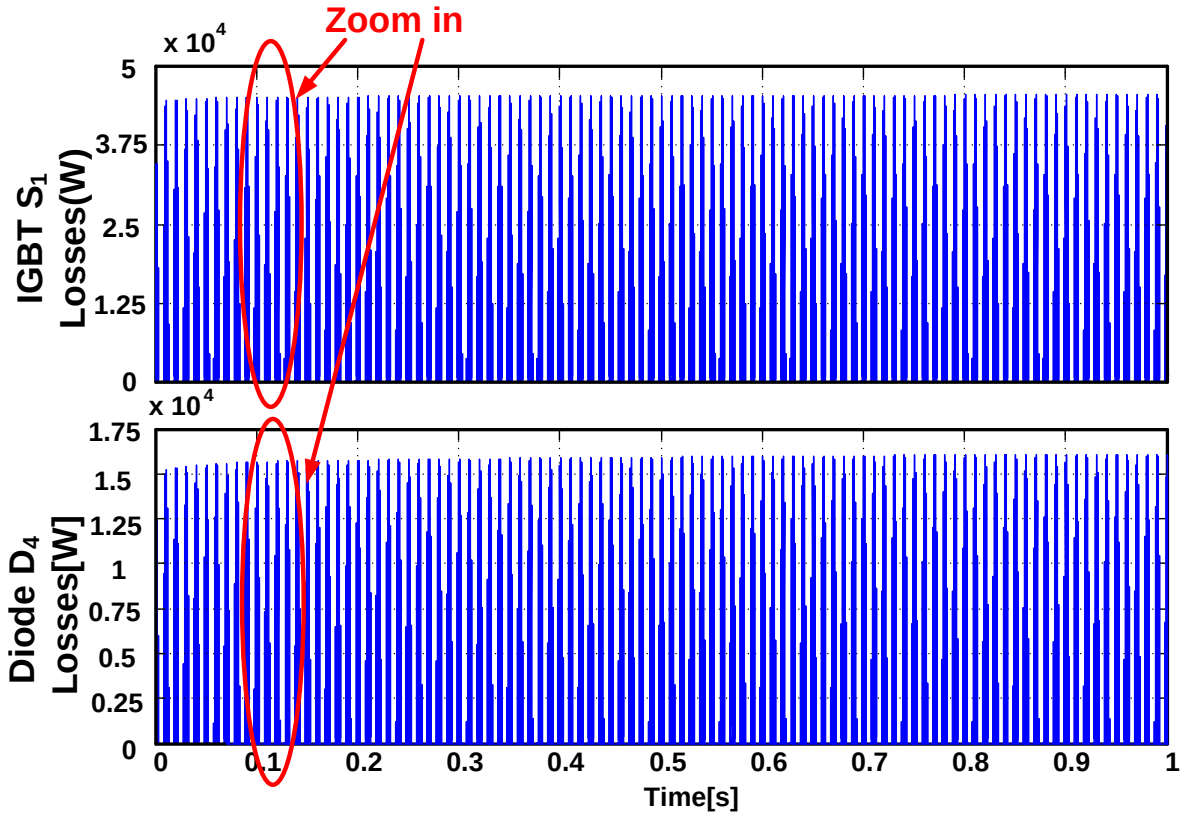


Fig. 4.8 Simulation results of the power losses in the electro-thermal model

In Fig. 4.9, the phase current is shown on the top as a reference, and as it has been mentioned, when the current of phase *A* is positive, the losses are added to IGBT S_1 and Diode D_4. The period of the sine wave current and thus period the power losses are 10ms, which corresponds to the modulation frequency.

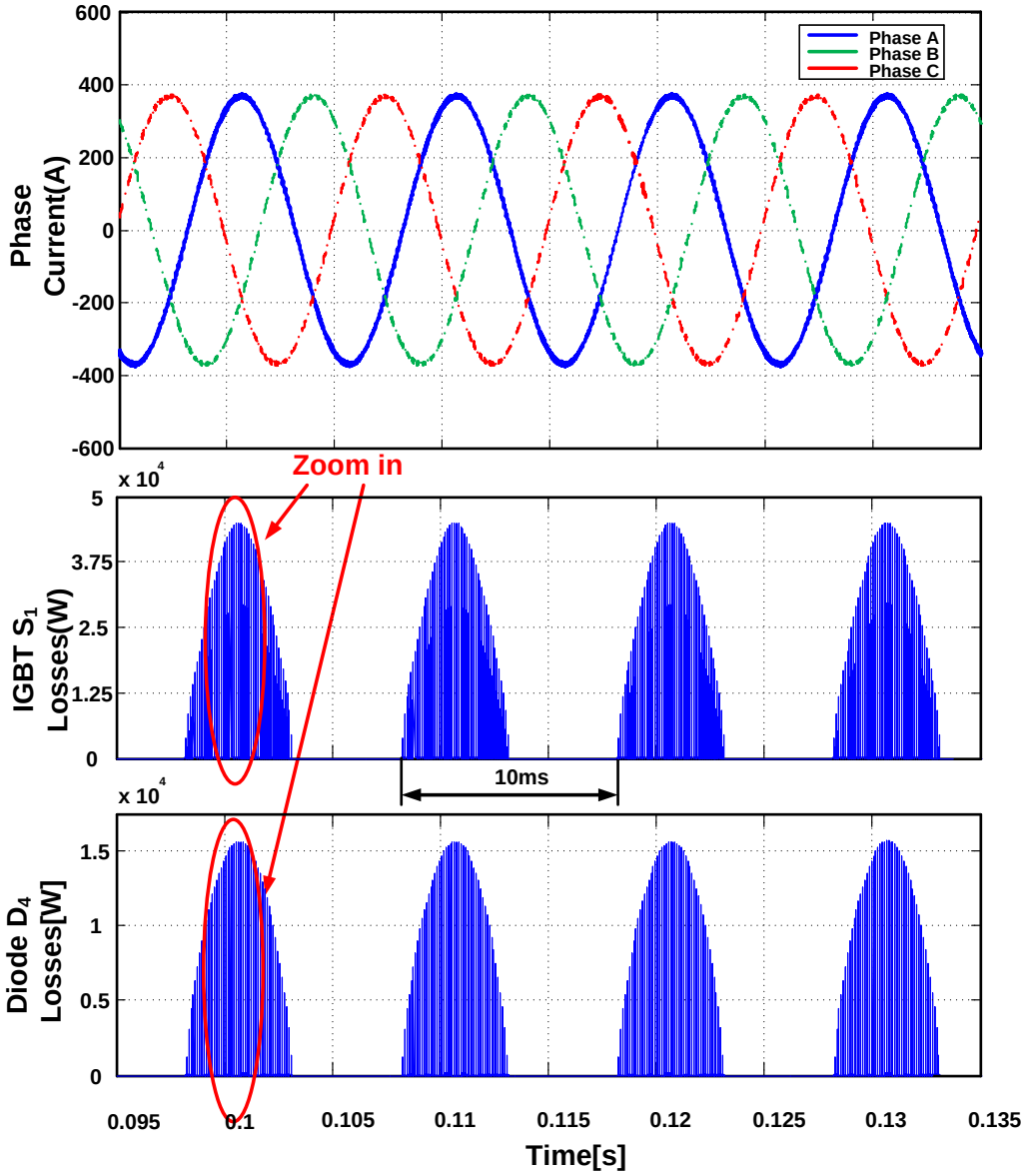


Fig. 4.9 Zooming in to the power losses in 40ms

The losses correspond to the switching frequency are shown in Fig. 4.10. The switching on and off time are set as 400 nanoseconds ($4*10^{-7}$s), which is a quite typical value. The amplitude of the switching losses in this case can be as large as 40kW.

The time behavior of the junction temperature in 40ms is shown in Fig. 4.11. It can be observed that the thermal inertia of the system was large enough so that the power loss variation within a switching cycle (the switching losses happened in 100μs in Fig.4.10) would not cause significant temperature fluctuation (red cycle in Fig. 4.11). However the junction temperature can still respond to the power loss oscillates at the fundamental frequency (the losses oscillate in 10ms in Fig. 4.9) and the instantaneous temperature fluctuation of the IGBT can be as large as 8 ℃.

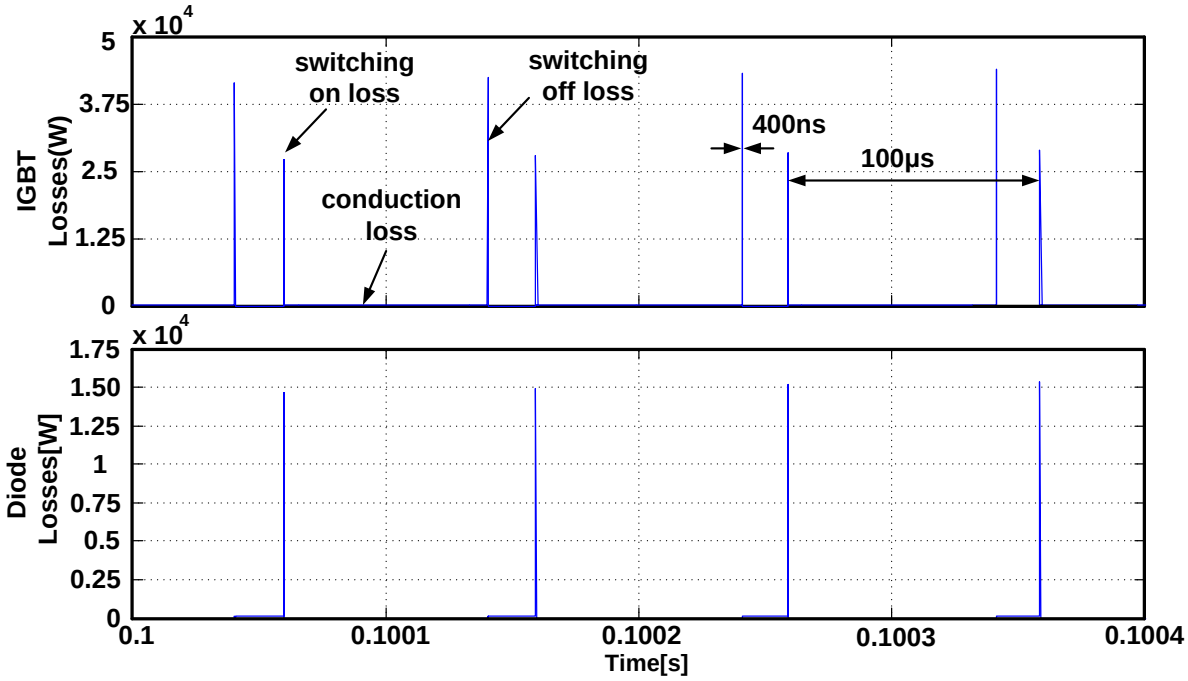


Fig. 4.10 Zooming in to the power losses in 400μs

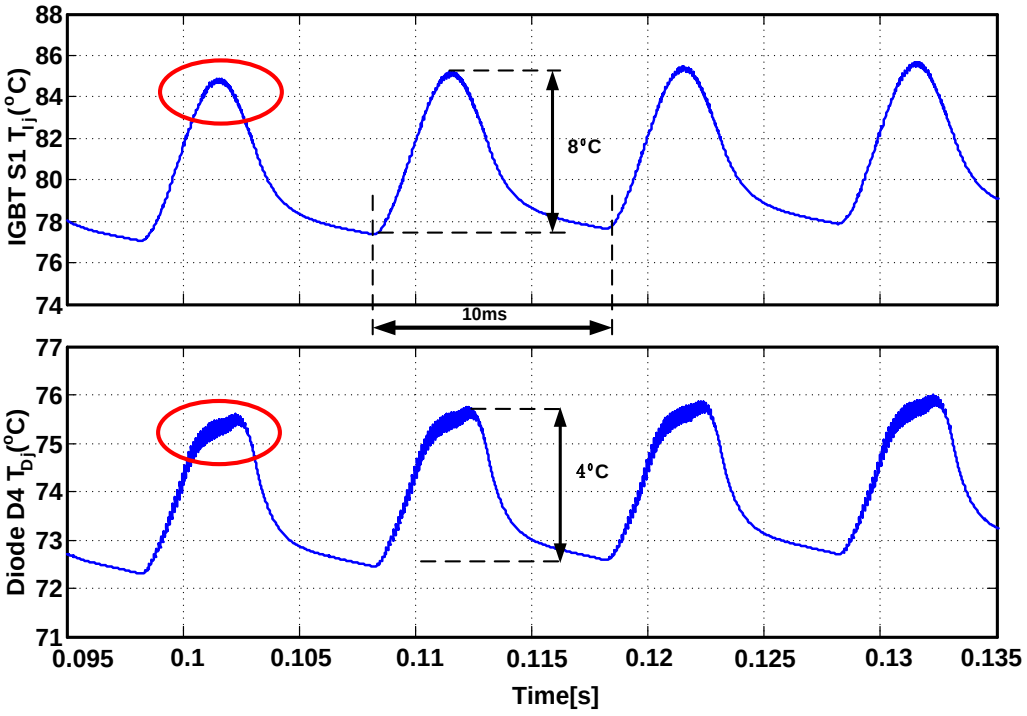


Fig. 4.11 Junction temperature waveforms in 40ms of S_1 and D_4

Since the junction temperature is mainly influenced by the power losses oscillate at the fundamental frequency, it is possible to average the switching losses to a larger time length and thus the time step can be also increased. Fig 4.12 shows this process, the switching energy are kept all the same and averaged to various time length including 400ns (the real switch on and of time length), 10^{-6}s, 10^{-5}s, and 10^{-4}s (corresponding to the 10 kHz switching frequency of the system). It can be observed that since the time length becomes larger, the power level of switching process becomes smaller and the temperature ripple also becomes smaller.

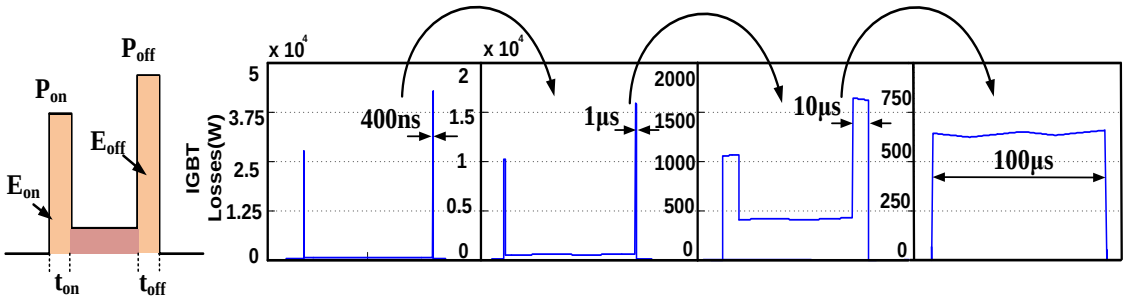


Fig. 4.12 Average the switching losses to different time length

The temperature waveforms when averaging the switching losses to a time length of 10^{-4}s is shown in Fig. 4.13. It can be seen that though the ripples disappear, the maximum junction temperature and temperature fluctuation, which are concerned most, are exactly the same as in Fig. 4.11.

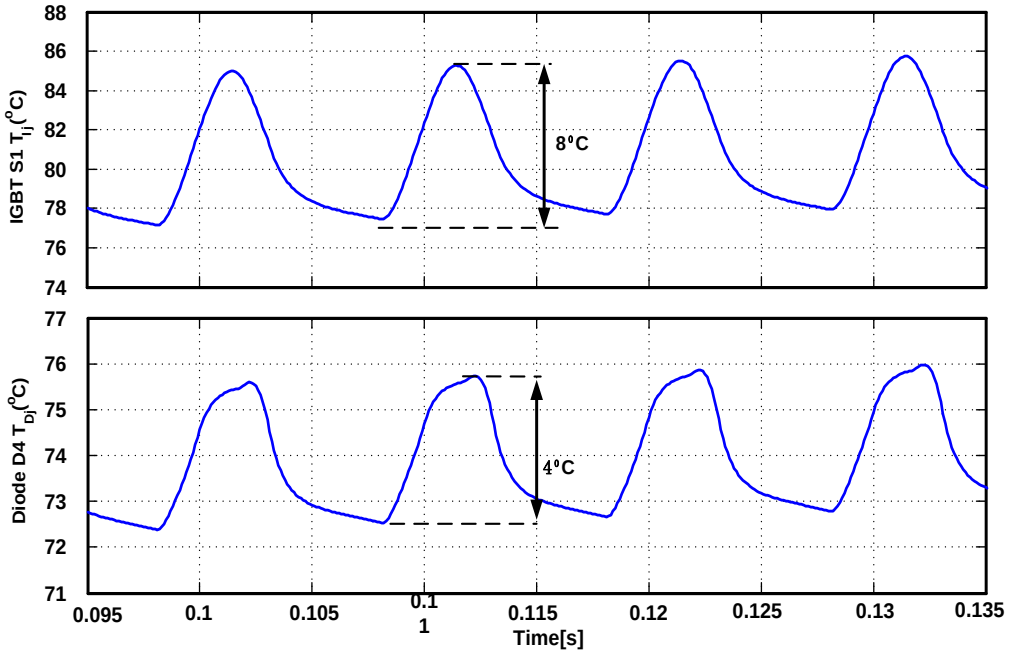


Fig. 4.13 Junction temperature waveforms in 40ms of S_1 and D_4 (with averaged switch losses)

Above analysis demonstrates that the time step can be increased to 10^{-4}s without losing any important temperature information in the simulation result, and in this case the whole simulation time can be set much longer to take into account the effects of both the small thermal inertia of the chips and the large thermal inertial of the heat sink. As already mentioned, it needs at least 40 seconds for the junction temperature to achieve its stable value, thus the simulation time is set as 100s.

The long term dynamic behavior of the junction temperature can be seen in Fig. 4.14, the sudden rise of the temperature at the very beginning and the temperature fluctuations during the whole simulation are mainly caused by the small thermal time inertial of the chips, and the slowly increasing of the junction temperature is caused by the large thermal inertia of the heat sink.

In addition, although the thermal impedance of the diode is larger than the IGBT due to its smaller area, the junction temperature of the diode is still much lower than the IGBT because the latter carries more current thus more power loss.

Details in power losses waveforms as well as a zoom in of junction temperature waveforms with duration of 40ms of all the IGBTs and diodes in Phase *A* at 90s are given in Fig. 4.15 and 4.16.

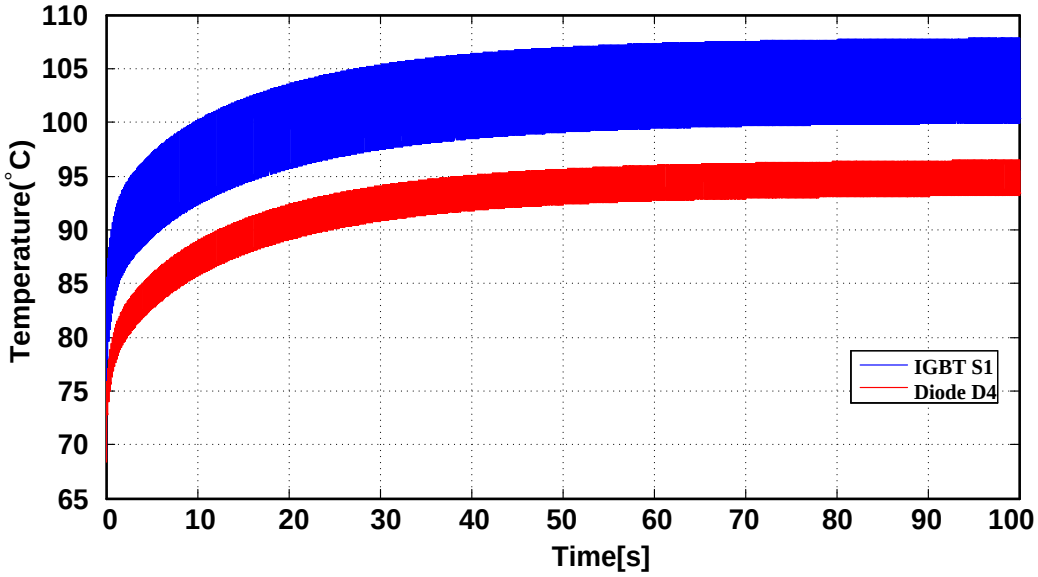


Fig. 4.14 Junction temperature waveforms for the entire simulation

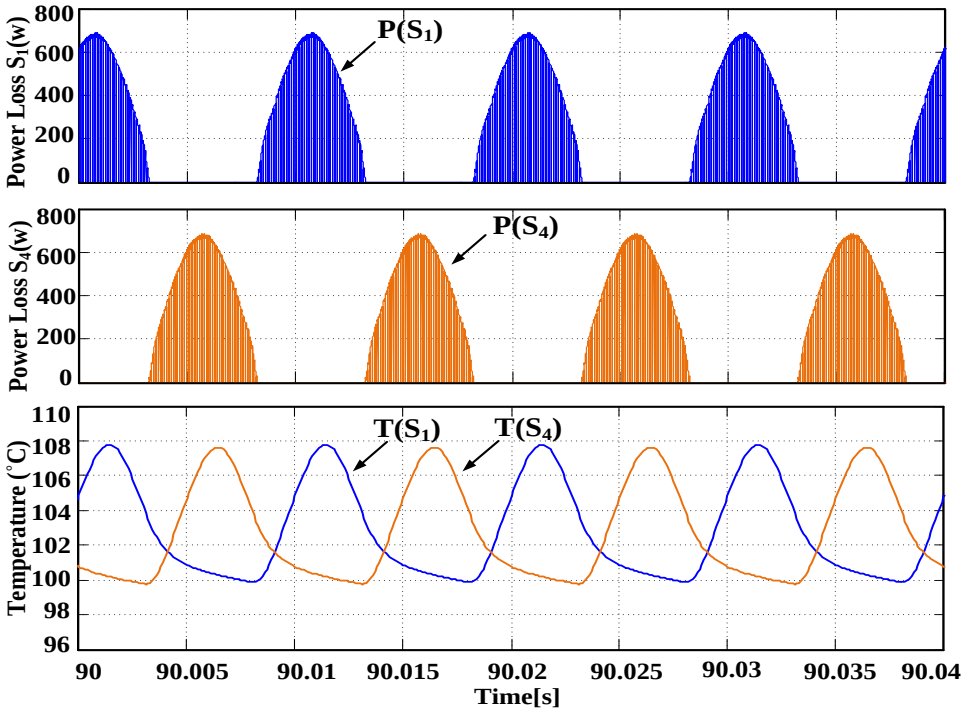


Fig. 4.15 Junction temperature waveforms of the IGBTs for the entire simulation

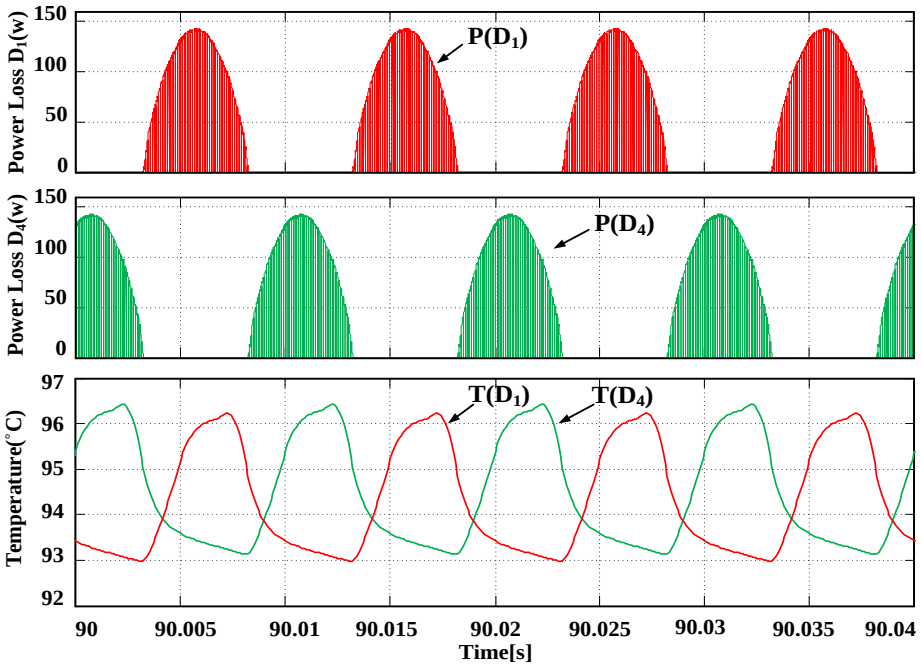


Fig. 4.16 Junction temperature waveforms of the diodes for the entire simulation

It can be clearly seen from Fig. 4.15 and Fig. 4.16 that the power losses of the high-side IGBT S_1 (diode D_1) and low-side IGBT S_4 (diode D_4) are complementary in the whole sinusoidal period. Meanwhile, the power losses of the high side IGBT S_1 (diode D_1) and the low-side diode D_4 (IGBT S_4) are complementary in the same half sinusoidal period.

The system has achieved its stationary state with a temperature rise in the IGBT of about 39℃, and as expected, the small temperature ripples corresponding to the switching loss disappeared due to the large time step (10^{-4}s). However, there is still significant temperature fluctuation caused by the power losses oscillate at the fundamental frequency. The amplitude of this fluctuation is 8℃, which is about 1/5 of the temperature rise.

These results demonstrate the importance of the transient electro-thermal analysis during the design stage of the inverter. Because the peak junction temperature could be much higher than the mean value due to the temperature fluctuation and as introduced in chapter 1.1, the device reliability is directly related to the the maximum junction temperature $T_{j,max}$ and the temperature fluctuations ΔT_j due to loading [83]. Exceeding the maximum permissible junction temperature $T_{j,max}$ will cause permanent damage of the components and the temperature cycling ΔT_j will lead to repetitive thermal stress and fatigue of the components. What makes it even worse is that this temperature fluctuation could be even larger if the fundamental frequency becomes lower or if the load changes become higher.

4.3 PREDICTION OF JUNCTION TEMPERATURE UNDER DIFFERENT OPERATING CONDITIONS

4.3.1 Temperature Fluctuation under Different Fundamental Frequency

Since the temperature fluctuation is caused by the power losses oscillate at the fundamental frequency, it is interesting to discuss in how much degree will the fundamental frequency influence the junction temperature waveform.

For the inverter studied in this thesis, the fundamental frequency is in the range 0-150 Hz. This is also a typical range for the traction inverters used in electric and hybrid vehicles and therefore three values (150Hz, 50Hz, 5Hz) are chosen as references. The load current is kept the same thus the power losses are equal to each other in these three simulations. The comparison of the junction temperature waveforms of the IGBT S_1 and S_4 under these fundamental frequencies is shown in Fig. 4.17.

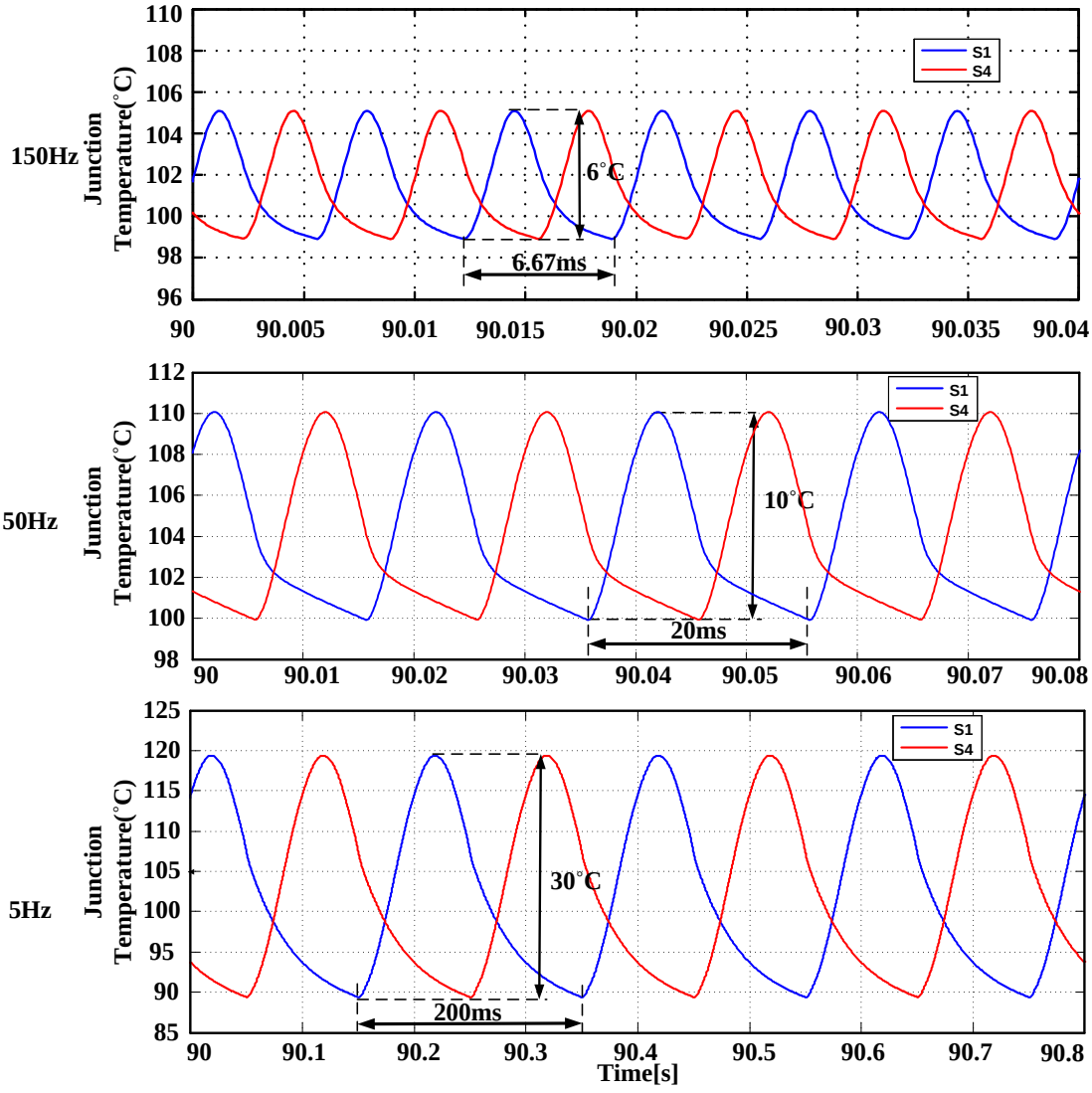


Fig. 4.17 Junction temperature waveforms under different fundamental frequencies

It can be seen that with the decrease of the fundamental frequency, the amplitude of the temperature fluctuation becomes larger. The temperature fluctuation can be as large as 30℃, which is nearly 75% of the whole temperature rise. And the peak junction temperature is 15℃ higher than the average junction temperature. These results indicate that without proper electro-thermal analysis, the junction temperature would not

be accurately predicted and design margin cannot be correctly determined. These results also highlight the importance of over-temperature protection of the silicon when the motor works at low speed, under heavy load or stall conditions.

4.3.2 Stall Torque Condition

It has been demonstrated that when fundamental frequency becomes smaller, the temperature fluctuation becomes larger and the peak junction temperature can be significantly higher than the average junction temperature which is normally predicted by the conventional steady state model. The worst-case is the stall torque condition when the fundamental frequency can be regarded as 0 and particular devices are loaded with DC like current.

When the rotor is rotating, six switches conduct alternatively to create the stator magnetic field rotating at the rotor speed. Under the stall torque condition, the rotor speed and, hence, the stator field speed are zero. Since the stator field is static, the six switches stop conducting alternatively. Instead, only one switch in each phase is operated continuously and there is no current in the other switches.

The three of the six switches work under stall torque condition are decided by the rotor field position. Fig.4.18 shows one worst case of the stall torque scenario where Phase-A carries the peak current. Under this condition, the current is kept at the peak value (375A as it shows in Fig. 4.9) and goes from the DC source to the motor winding through the high side switch S_1 in Phase *A* and returns back to the DC source through low side switches S_6 and S_2 in Phase *B* and Phase *C*. In addition, these switches are still controlled

by the switching signals and in order to regulate the DC current applied to the motor under stall torque condition, when the switches shown with red circles are off, diodes shown with blue circles conduct.

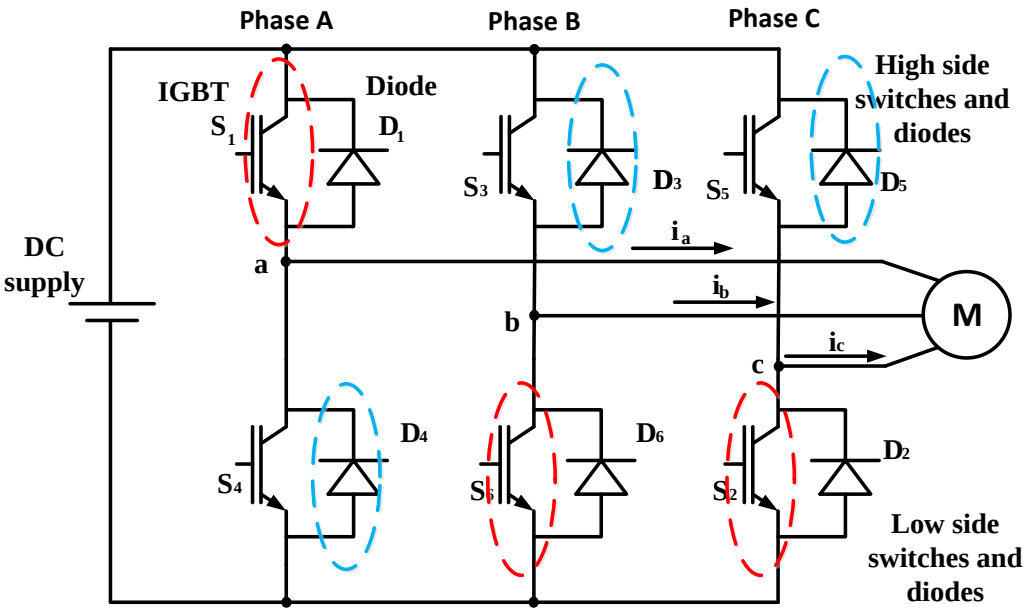


Fig. 4.18 Stall torque scenario

The junction temperature of IGBT S_1 in this case is shown in Fig. 4.19. Comparing to the junction temperature variation in Fig. 4.17 for rotating conditions, it can be seen that the temperature fluctuation disappears in the stall-torque condition. This is because the current passing through S_1 is kept at the peak value and the fundamental frequency can be regarded as 0Hz. However the junction temperature in this case (with a temperature rise of 80 ℃) is much higher than that in any condition in Fig. 4.17 (with an average temperature rise of 40 ℃ and a maximum temperature rise of 55 ℃) because the power dissipation in S_1 is much larger than any other condition and the junction temperature achieves the highest value under the giving load.

Another important issue is the big difference between the switch junction temperature and the cold plate temperature. Their temperature waveforms for the first few seconds are shown in Fig. 4.20. As illustrated in the figure, due to the small thermal time constant of the IGBT, the junction temperature of Phase-A high side switch jumps to 125 ℃ quickly (with a temperature rise of 60 ℃ in 2s). Meanwhile, the temperature of contact surface between the cold plate and the power module increases much slower (with a temperature rise of 8 ℃ in 2s). This problem emphasizes once again the importance of over-temperature protection of the silicon under stall-torque condition, because the thermistors used to protect the system are typically installed on the cold plate or the baseplate of the power module, and they cannot reflect the sudden rise of the junction temperature.

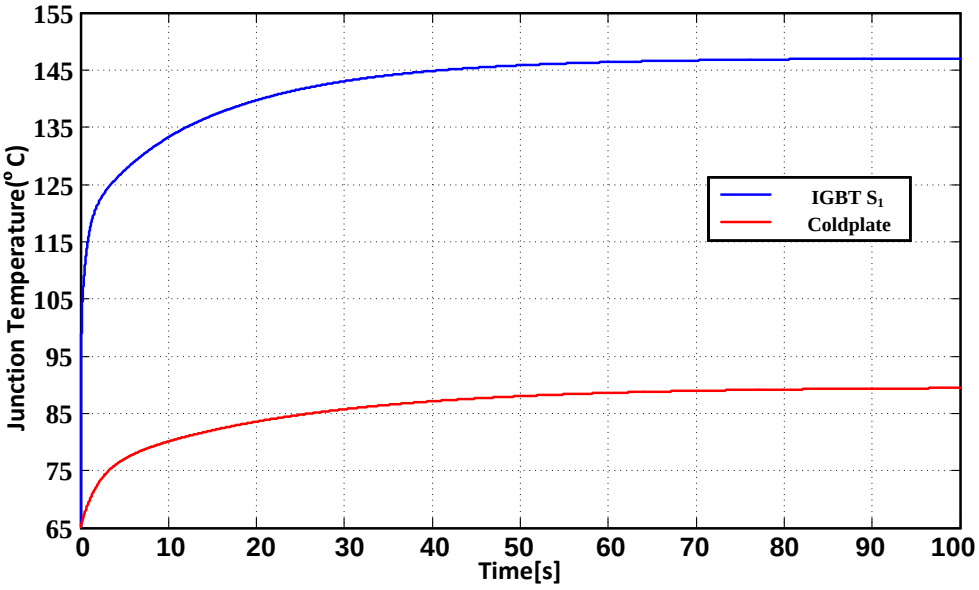


Fig. 4.19 Junction and cold plate temperature waveforms under stall torque condition

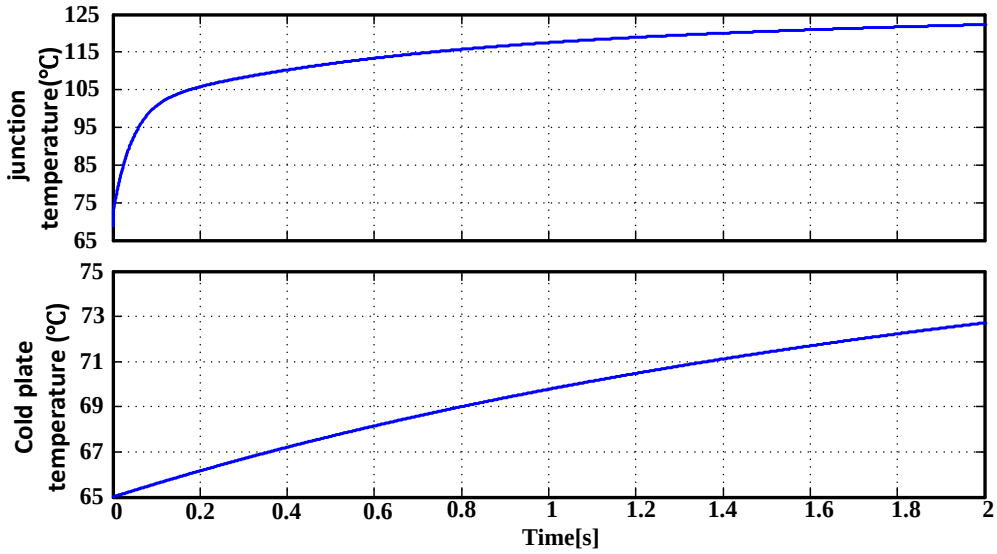


Fig. 4.20 Junction and cold plate temperature waveforms in the first 2 seconds

4.4 ERROR ANALYSIS OF THE TEMPERATURE PREDICTION WITH DIFFERENT MODEL SIMPLIFICATION METHODS

The electro-thermal model discussed in this thesis has considered both the temperature dependence of the power loss model and the thermal coupling effects in the thermal model. Since traditionally these factors are always ignored to simplify the thermal analysis process, it will be of good referential meaning to evaluate the errors caused by these kinds of simplification.

To eliminate the influence of the temperature dependence and the thermal coupling effects, simulations are carried out by fixing the junction temperature in at the ambient temperature and setting the cross-coupling impedance as zero respectively.

A comparison of these simulation results are illustrated in Fig 4. 21. It can be seen that the impact of the temperature dependence of the power loss to the junction temperature is

not significant, and comparing to the complete model the junction temperature is only 3℃ lower (about 8% of the temperature rise (38℃) of the IGBT). This result is reasonable because the impact of the temperature to the power losses in an IGBT is relatively small comparing to other switching component such as the MOSFET.

However, the thermal coupling effects have huge influence on the junction temperature, and it is noticed that failing to take into account of the mutual heating effects will result in an underestimation of the junction temperature rise of about 35%.

So it is very important to consider the influence of the thermal coupling between different chips in the power module when building the thermal model during the design stage of the inverter to help determine the correct level of the design margin.

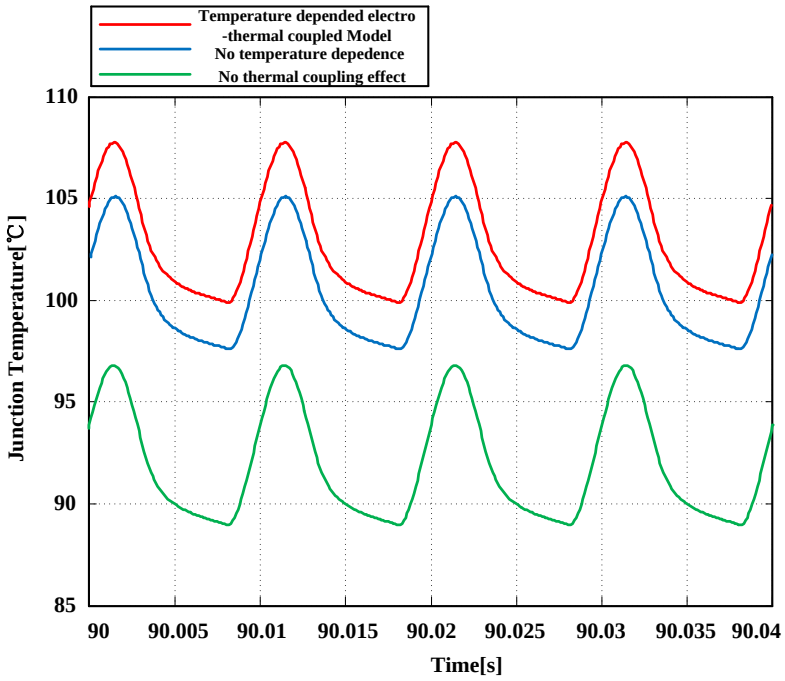


Fig. 4.21 Junction temperature waveforms for the entire simulation

4.5 CONCLUSION

In this chapter, the transient electro-thermal simulation of the inverter has been implemented in real time simulator. The simulation step size is carefully selected to solve the wide time scales separation problem when coupling the power loss model and thermal model. This electro-thermal model is then used to predict the junction temperatures of the inverter under various operation conditions. After that, the "worst-case" junction temperature under stall torque condition and the limitation of the traditional temperature protection methods is discussed. Finally, the importance of considering the temperature dependency of the power losses and the thermal cross-coupling effects in the thermal model at the design stage of the inverter is evaluated.

Chapter 5

EXPERIMENTAL VERIFICATION

5.1 INTRODUCTION

The accuracy of the transient electro-thermal simulation presented in Chapter.4 depends on both the accuracy of the power losses model proposed in Chapter.2, and the accuracy of the thermal model developed in Chapter.3. Actually, the power losses model should be accurate since it is based on the experimental results and the manufacturer's datasheet. However, the accuracy of the thermal model still need to be further verified, such as the transient thermal impedance, the linearity assumption and thermal cross-coupling effects of the entire system. This chapter describes the experimental verification of the thermal model.

5.2 PERVIOUS WORK

Methods for measuring the chip temperature can be classified into direct and indirect methods.

The direct methods are implemented by using fine geometry thermocouples [84] [85], optical fibers [86] [87] or infrared imaging [88] [89]. These methods can be really accurate however they typically require physical modification of the power module and the measurement time can hardly be lower than 1ms due to the electronic treatment and the thermal capacitance of thermo-sensible materials [90].

The indirect methods sense the junction temperature of the chips by measuring the temperature-sensitive electrical parameters (TSEP). Parameters that are commonly used as the TSEP of the IGBT module are the forward voltage under low current u_{CE} [91], the gate-emitter voltage u_{GE} [92] and the saturation current I_{CS} [93]. There is no need for physical modification of the package when using the TSEPs to measure the junction temperature. Also, fast measurements with times shorter than 100μs can be carried out [91]. However the accuracy of these methods is controversial because the chip temperature could be very inhomogeneous and the temperature given by a TSEP is only a "global" value between the maximum and minimum temperatures [94]. Several criteria such as the measurement accuracy, the temperature sensitivity, linearity and repeatability have been used to evaluate these methods. So far, the forward voltage under low current u_{CE} is regarded as the best solution [94] [95].

In this thesis, both the direct method and indirect method are used to verify the thermal model.

5.3 DIRECT MEASUREMENT OF THE CHIP TEMPERATURE

5.3.1 Principle of the Temperature Measurement

The measurement of the chips contains two stages as it is shown in Fig.5.1. During the first stage (heating stage), the IGBTs (three parallel dies in each switch) are heated by passing a high collector current (around 100-200A in our experiment), which will produced a huge amount of power loss and a significant temperature rise in the chips. During this stage, the gate emitter voltage u_{GE} is controlled at 15 V and the power losses

can be calculated by multiplying the collector current value i_C and the corresponding collector-emitter voltage value u_{CE} calculated from the datasheet. This stage will last several minutes until the thermal equilibrium was attained. Then the heating current is interrupted by means of external switch, and the temperature is measured by the thermocouples or the temperature TSEP during the following cooling stage. This result can be regard as the junction temperature step responses of the measured chips.

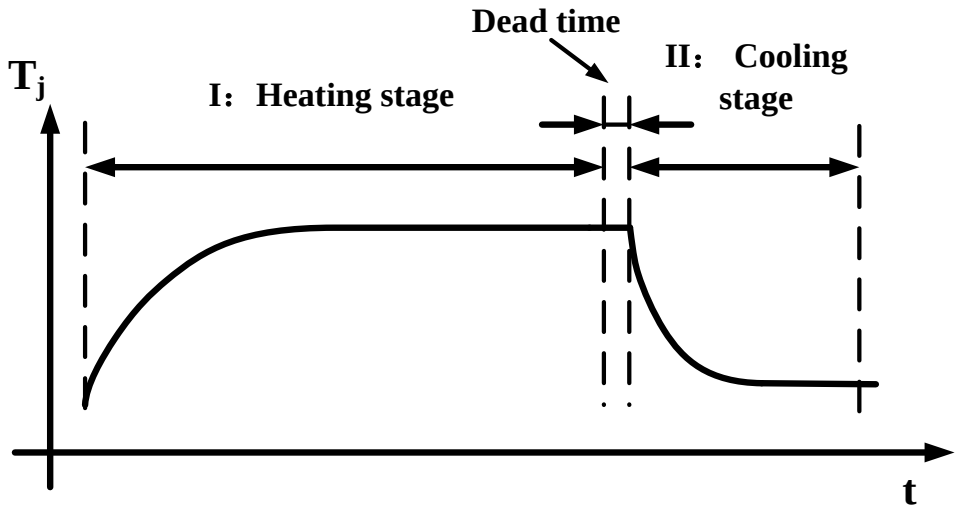


Fig. 5.1 Temperature profile during the measurement process

It is worth to mention that there will be a short dead time between these two stages due to the switching off process. However this process happens within several microseconds (which will be shown later) thus its impact to the temperature can be ignored.

Fig.5.2 shows the test circuit to realize the above measurement process. In this figure, the transient temperature of the high-side IGBT in half bridge 2 is measured, and the low-side IGBT is shorted. The switching from the heating stage to the cooling stages which is

mentioned in Fig.5.1 is realized by changing the gate signal from 1 to 0. The model of the power supply used in the experiment is Sorensen SGA from AMETEK whose maximum output current is 45A; however, a collector current of more than 100A is needed to generate enough temperature rise of the IGBT for further measurements. Thus a buck converter is involved in the test circuit to generate the required collector current through the measured IGBTs. This buck converter is composed of half bridge 1, capacitance *C* and inductance *L*. The real collector current i_C is measured by current sensors and compared to the reference current i_{ref} and it is controlled at the desired value by adjusting the DC voltage.

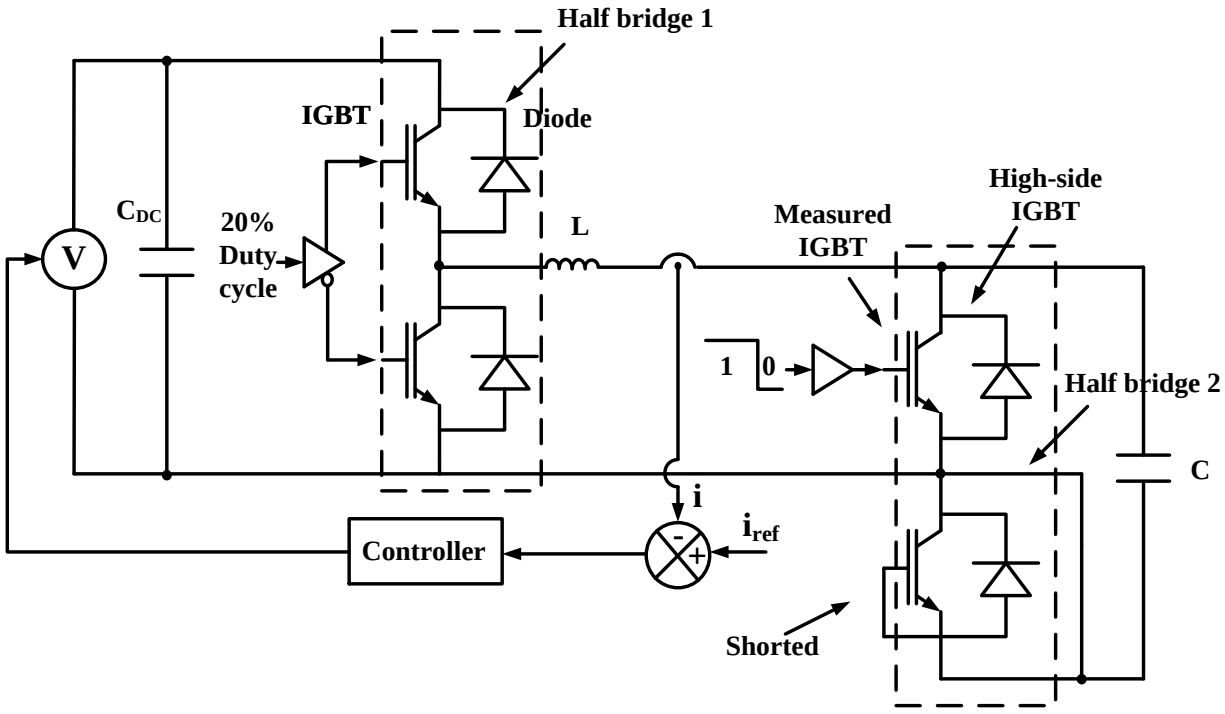


Fig. 5.2 Test circuit for the temperature measurement with thermocouples

5.3.2 Measurement Setup

The temperatures of the IGBTs and Diodes are measured with thermocouples. These thermocouples are attached to the surface of the silicon chips.

Since the transient temperature measurement of the chips requires extremely fast response time, the adopted thermocouples are type K the Cement-On style 2 (CO2-K) thermocouples from OMEGA. These thermocouples are made from 0.0005'' thermocouple alloy foil and they can achieve a response time of 2-5 milliseconds [96].

The installation processes of the thermocouples are described as follow:

Firstly, the gel is carefully removed from the power module to expose the measured surface and the location of the thermocouples placed on the IGBTs is demonstrated in Fig. 5.3 (the yellow circle).

Then, a thin layer of OB Epoxy from OMEGA is laid down on the chip surface for insulation (the black coating) [97].

After that, the thermocouples are directly bonded to the measured surface covered by the epoxy.

These procedures are also repeated for other chips, which are not shown in this Figure.

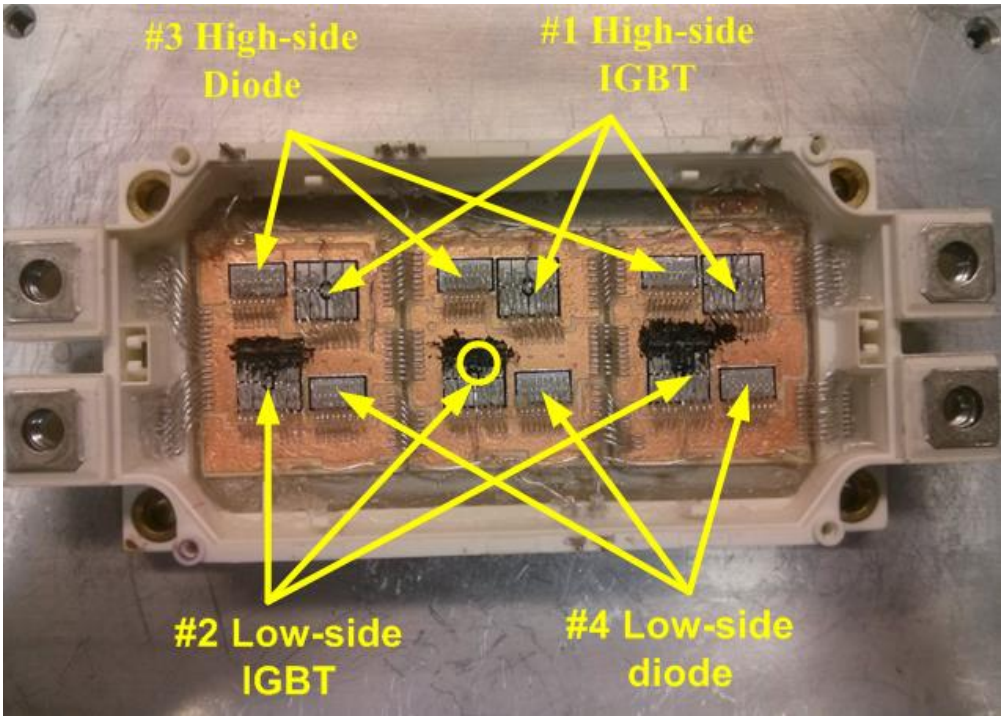


Fig. 5.3 Location of the thermocouples in the tested system

The whole temperature measurement system is shown in Fig. 5.4a. The circulation of the coolant is controlled by the pump, valve, and flow meter. The mass flow rate of the coolant is set at 2 LPM as it has been mentioned in chapter 3.6.1. Details of the test system can be seen in Fig. 5.4b, where the temperature is measured by the thermocouples and collected by an USB data acquisition module, which is also from OMEGA. The model of the DAQ module is OM-DAQ-2401 and it can provide a sampling rate of 1000 samples/sec.

Corresponds to Fig. 5.2, a buck converter is used to increase the collector current passing the measured chips, and the switching of the gate signals is controlled by the control board.

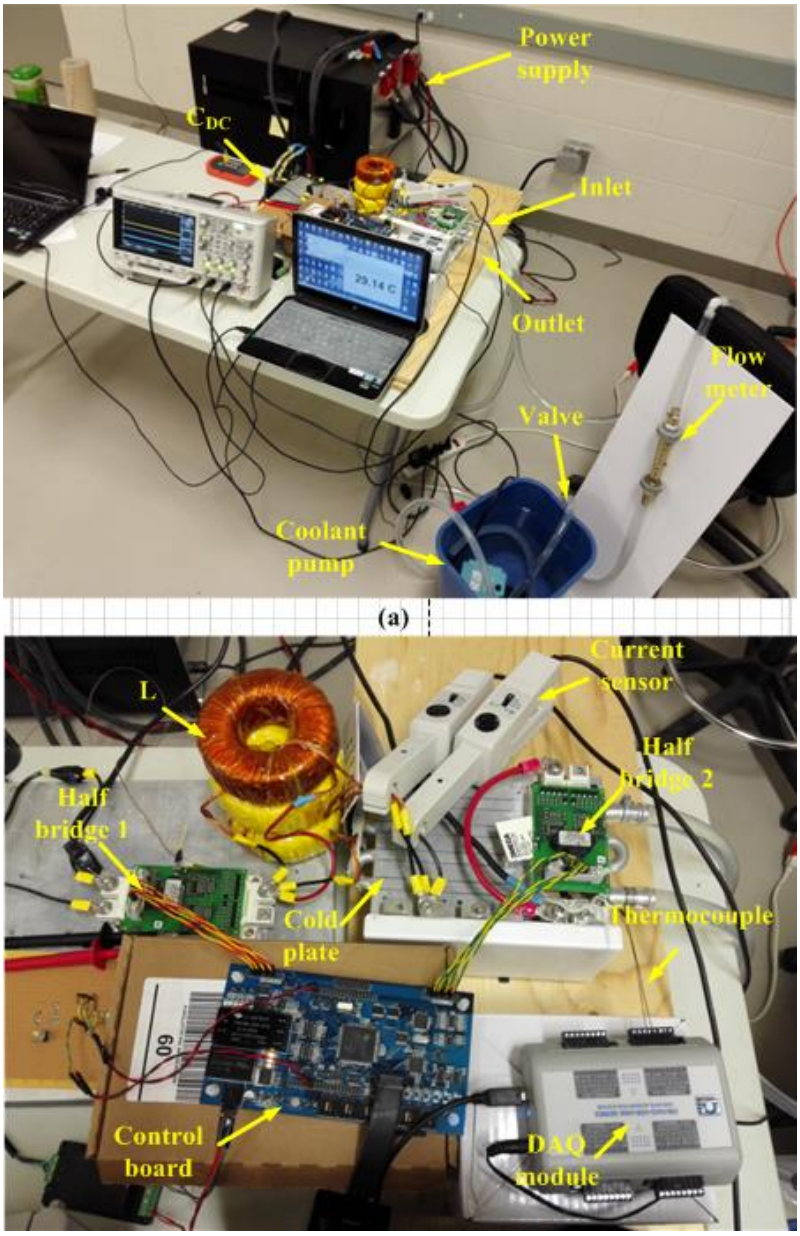


Fig. 5.4 Experimental setup for direct temperature measurement: (a) whole setup (b) test circuit and equipment for direct measurement

5.3.3 Calibration of the Thermocouples

In order to achieve accurate temperature measurement, it's important to calibrate the thermocouple accordingly. Thermocouple produces a voltage that increase with

temperature, thus it can be calibrated by plotting the thermocouple's voltage-temperature curve.

Fig. 5.5 shows the calibration setup for the thermocouples and DAQ module which will be used in our direct temperature measurement experiment. The calibration process is as follow: Firstly, the oil in the thermo bath container is heated to 25^{o} C. Then, the precision thermocouple and the calibrated thermocouple are both inserted to the thermo bath container and are kept very close to each other. After the values become stable, the temperature measured from the precision thermocouple and the voltage measured from the calibrated thermocouple are recorded. This process is repeated by increasing the temperature by 5^{o} C increments and recording the voltage until 100^{o} C is reached. In addition, the ice water mixture in the ice bath container is also used as a reference calibration point of 0^{o} C.

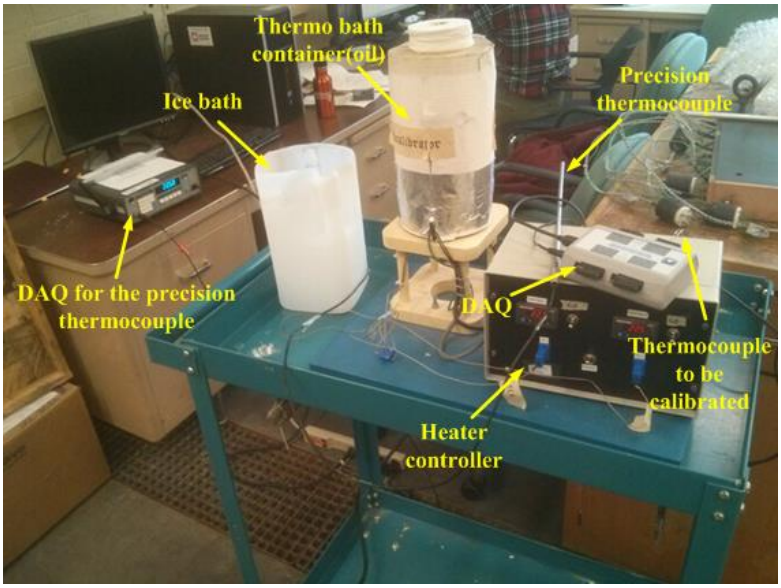


Fig. 5.5 Calibration setup for the thermocouples

The precision thermocouple is precisely calibrated by the manufacturer thus by performing the above steps the correspondence between the actual temperature and the voltage of the calibrated thermocouples can be obtained. These data is then fitted into a line as it shows in Fig. 5.6 and the relationship between the temperature (T_C) and the voltage (u_C) of the calibrated thermocouple can be expressed as:

$$T_C = 4.159e^{-5} \bullet u_C - 0.001275 \tag{5.1}$$

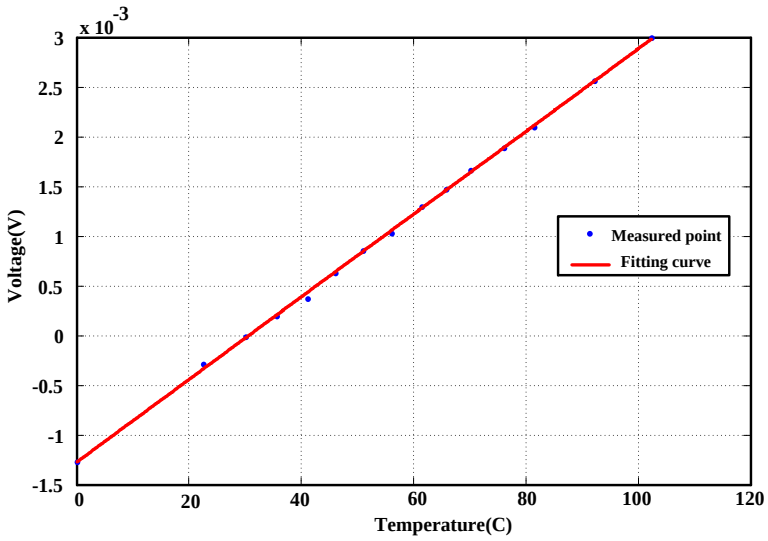


Fig. 5.6 Calibration curve of the thermocouples

5.3.4 Direct Measurement Results

It has been demonstrated that for a linear thermal system, the heating and cooling temperature responses are complementary [98], thus the transient thermal impedance can be measured during either the semiconductor's heating stage or the cooling stage. However it is much more complicated to measure the heating response than the cooling response and, therefore, the cooling response is used in this thesis to extract the transient thermal impedance.

As described in chapter 5.3.1, the chip under test was firstly heated by a high current to introduce a significant temperature rise. Then when the thermal equilibrium was attained, the heating current is interrupted and the junction temperature began to decrease and was measured by the thermocouples. There is a dead time between the heating and cooling stage for the interruption of the heating current as it shows in Fig.5.7. However, however this time is very short (around 0.3ms) in our set up, thus its impact on the measurement of the temperature response can be ignored.

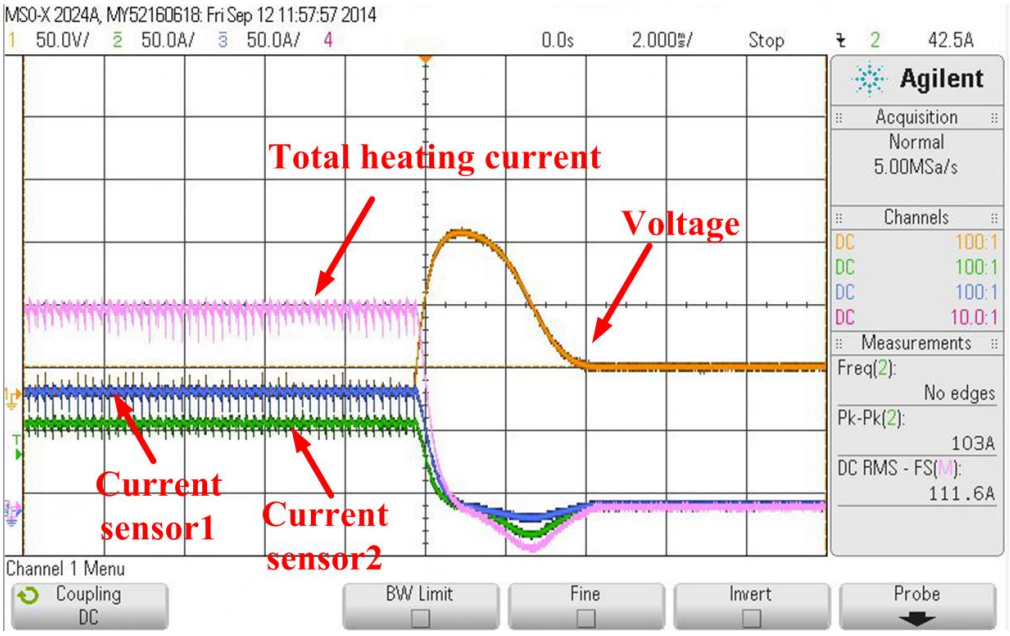


Fig. 5.7 Interruption of the heating current for the junction temperature measurement

(Range of each current is 100A)

The measured junction temperature waveform of the high-side IGBT (IGBT#1) during the cooling stage is shown in Fig. 5.8.

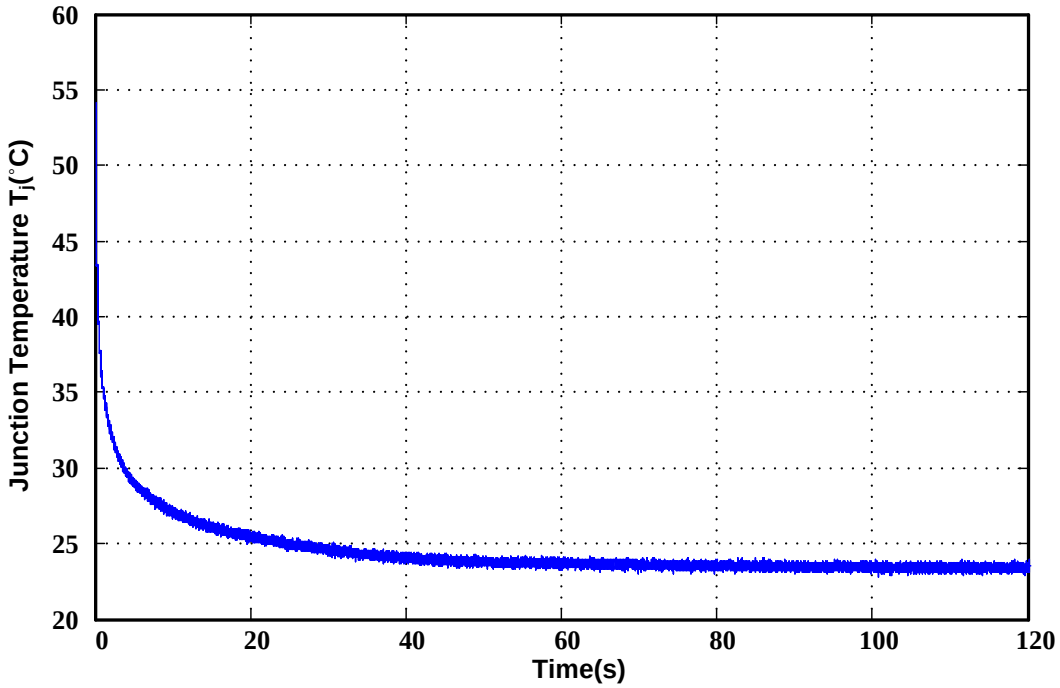


Fig. 5.8 Measured junction temperature of IGBT during the cooling stage (cooling curve)

Based on the measured temperature during the cooling stage, the transient thermal impedance of the high-side IGBT (IGBT#1) can be calculated by the following equation,

$$Z_{th}(t) = \frac{T_0 - T_j(t)}{P} \tag{5.2}$$

Meanwhile, the cross coupling thermal impedance can be calculated by measuring the temperature response of the corresponding chips when IGBT#1 is heated. A comparison between the experimental results and the simulation results in Chapter 3 are presented in Fig. 5.9.

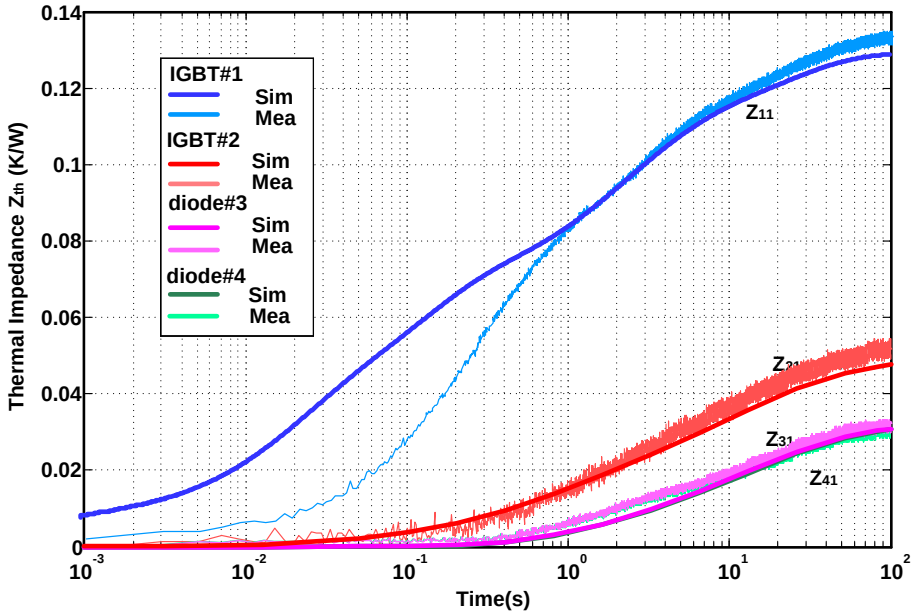


Fig. 5.9 Transient thermal impedance curves derived from the measured cooling curve (Sim-simulated result, Mea-measured result)

It can be seen that the measured and simulated self-heating thermal impedance of IGBT#1 are consistent with each other after 0.7 second, and the steady state error is only about 3.6%. Meanwhile the simulated and measured cross coupling thermal impedance also match extremely well. However, huge error (with a value of more than 100%) of the self-heating thermal impedance can be found in the first several hundred milliseconds.

The main source of this error is that there is a layer of epoxy painted on the surface of the measured chip surface and coated around the thermocouples for electric insulation. As a result, though the thermocouples can response to very fast temperature variation, there will still be a delay for them to detect the extremely rapid change of the junction temperature at the beginning of the cooling stage.

Thus the thermocouples are more suitable for long term or stable temperature measurement for the chips and can be only used to validate the steady-state simulation results and the thermal coupling effects.

5.4 INDIRECT TEMPERATURE MEASUREMENT BY USING TSEP

The steady-state thermal impedance value and thermal coupling effects were both verified in the direct measurement experiment. However, since the transient thermal impedance in the low time regime (10^{-3} to 0.7s) cannot be captured accurately, the TSEP which can provide a much faster response time is used to validate the transient thermal impedance of the chips.

The forward collector-emitter voltage under low current u_{CE} is chosen as the TESP in this thesis and two steps are necessary for the indirect temperature measurement. The first one is calibration, which is used to determine the relationship between u_{CE} and the junction temperature T_j. The second step is measurement, which is similar to the direct temperature measurement process using the thermocouples. However, a measurement current i_m is needed so that u_{CE} is measurable during the cooling stage, and this current is kept at a low level of 1 mA to ensure the self-heating of the device is negligible [99].

5.4.1 Calibration of the Thermocouples

Fig 5.10 shows the setup to calibrate the relationship between u_{CE} and T_j. The calibration method can be described as follow: Firstly, a thermocouple is pasted closely to the power

module to monitor its temperature. Then, this temperature is controlled to the reference value by a hotplate, and the corresponding u_{CE} is measured by the DAQ module.

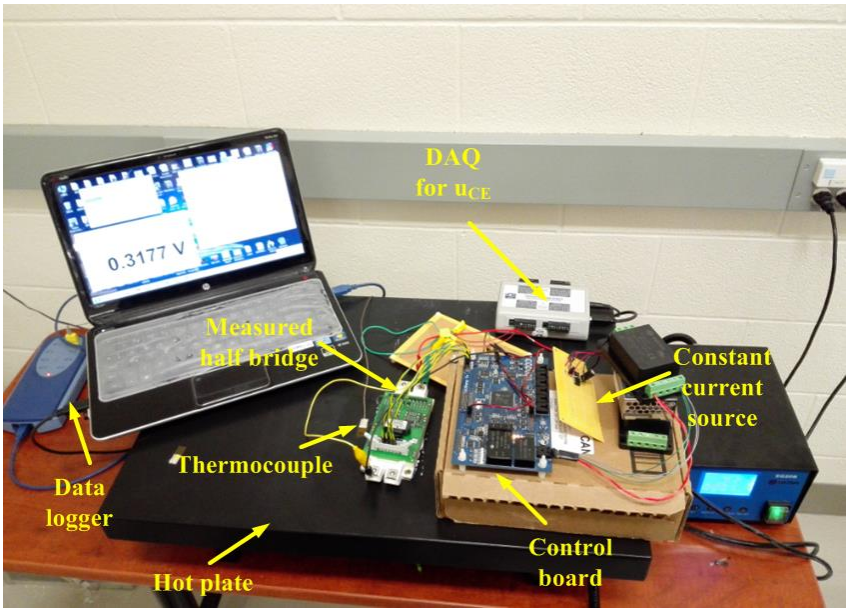


Fig. 5.10 Setup for the calibration of relationship between u_{CE} and temperature

17 reference temperatures is selected from 23.5˚C to 105˚C with an increment of 5^{o} C and the correspondence between u_{CE} and junction temperature of the high-side IGBT is shown in Fig.5. 11. It is clear that the variation of u_{CE} is almost linear with the junction temperature.

By applying least square curve fitting to the measured data, the relationship between u_{CE} and *Tj* can be expressed as:

$$T_j = 149.6 - 346.38u_{CE} \tag{5.3}$$

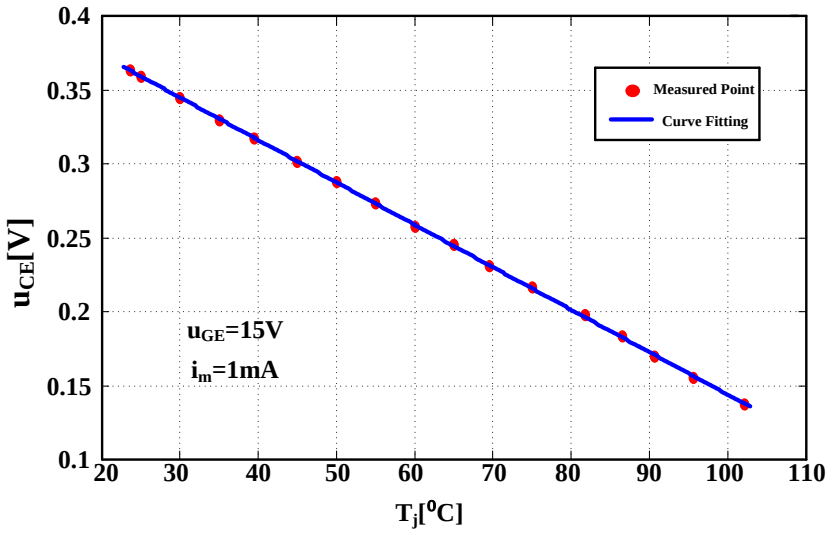


Fig. 5.11 The calibration curve of u_{CE} and the junction temperature of the high-side IGBT

5.4.2 Measurement setup

The test circuit for the indirect temperature measurement is given in Fig. 5.12.

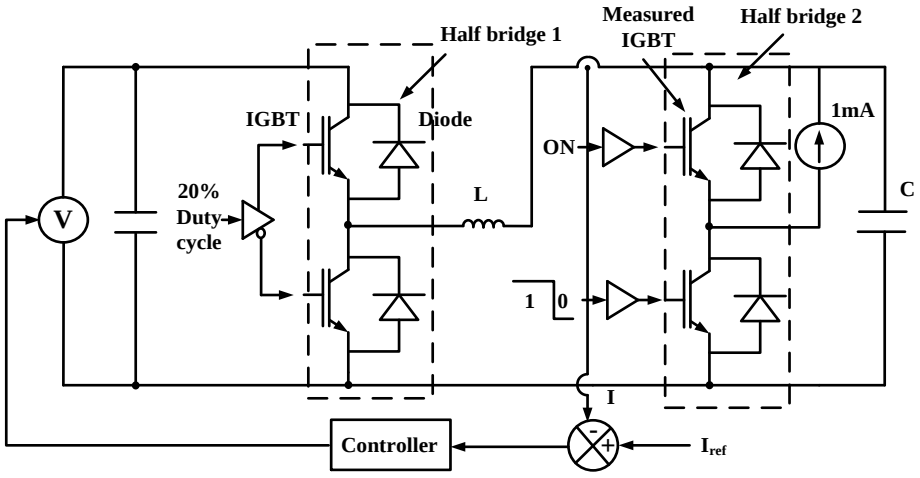
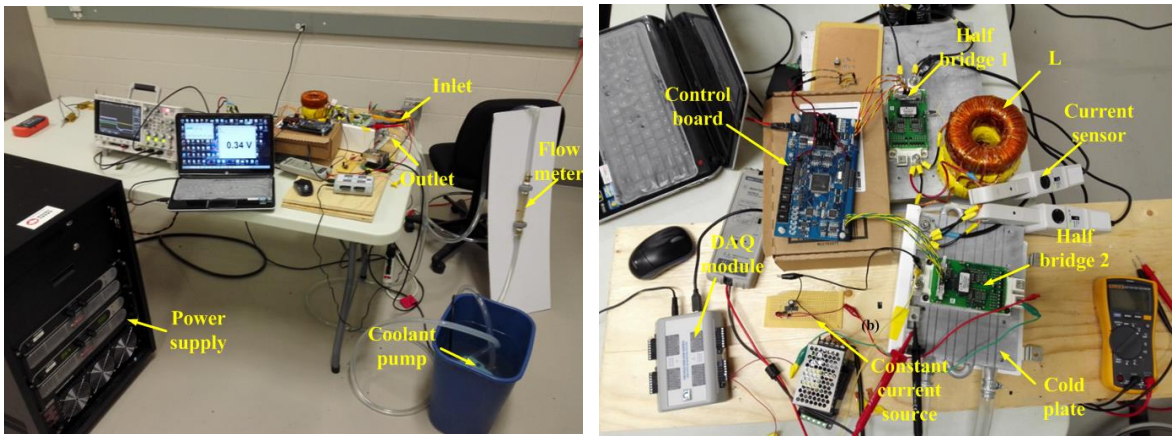


Fig. 5.12 Test circuit for the temperature measurement with u_{CE} as TSEP

Similar to the test circuit for the direct measurement, a buck converter is involved in the test circuit to introduce high enough collector current passing through the measured IGBT

during the heating stage. The only difference is that a measurement current i_m of 1mA is needed during the cooling stage so that u_{CE} is measurable, and this current is kept at a low level of 1 mA to ensure the self-heating of the device is negligible.

Fig 5.13 presents the whole setup for the indirect temperature measurement system. Again, the mass flow rate of coolant is controlled at 2LPM, however, the DAQ module is used to measure the instantaneous collector-emitter voltage u_{CE} during the cooling stage and a constant current source is connect to the measured IGBT module.



(a) (b)

Fig. 5.13 Experimental setup for indirect temperature measurement: (a) whole setup (b) test circuit and equipment for indirect measurement with u_{CE}

5.4.3 Indirect Measurement Results

The cross coupling thermal impedances have been verified by using the thermocouples thus only the self-heating thermal impedance of the IGBT need to be validated by using the indirect measurement method. Similar to process of the direct measurement, the junction temperature response during the cooling phase is measured to derive the transient

thermal impedance. However the temperature is measured by using the TSEP and the transient thermal impedance derived from the cooling response is shown in Fig. 5. 14.

In contrast to the direct measurement results, the experimental thermal impedance derived from the TSEP is in good accordance with the simulation result in the whole time range. There is still slight error of 3.4% for the steady-state value and 9.7% for the transient value because the measured dimensions of the chips in the power module could not be 100% accurate, and an ideal model is used to represent the thermal interface material between the power module and the cold plate while in reality the thermal grease cannot be uniformly distributed in the contact area. In addition, as mentioned at the beginning of this chapter, using u_{CE} as the TSEP to measure the temperature will also cause a tiny margin of error. But anyway the error is within an accepted level and the self-heating thermal impedance is also validated.

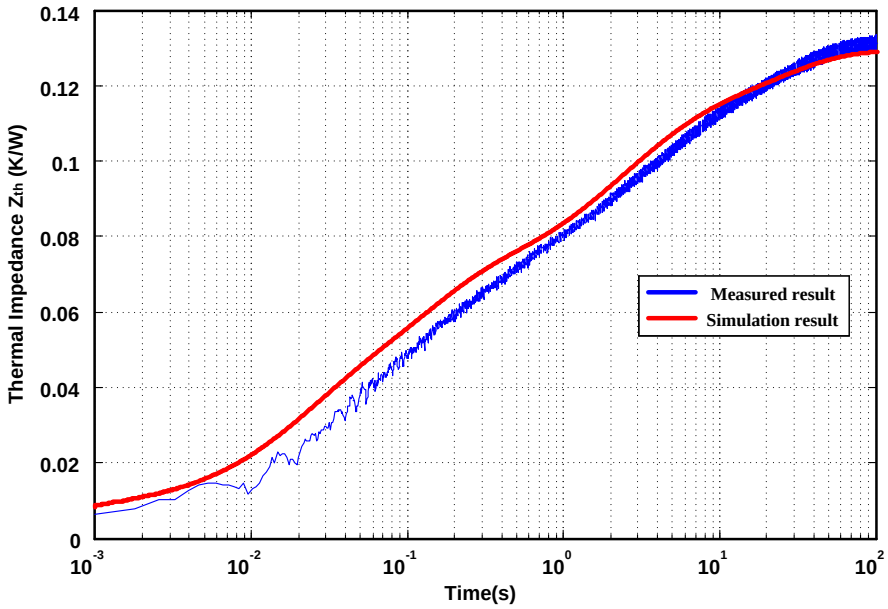


Fig. 5.14 Experimental results for indirect temperature measurement

5.5 CONCLUSION

The experimental validation of the thermal model is implemented in this chapter. Both the direct temperature measurement using the thermocouples and the indirect temperature measurement using u_{CE} as the TSEP are carried out. The self-heating and cross-coupling thermal impedance of the entire system tare verified thus the thermal model is accurate.

Chapter 6

CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSIONS

In this thesis, a state-of-art electro-thermal model of an IGBT based three-phase inverter is developed. Compare to the previous researches, the biggest advantage of the proposed electro-thermal model is its detail and completeness.

A fast and accurate temperature dependent power loss model was presented. The conduction losses were calculated based on the datasheet and the switching loss model was implemented by setting up a look-up table from the measured results of the practical traction inverter.

A comprehensive thermal model of the entire inverter considering the thermal cross coupling effect was developed. It is the first time that the feasibility and accuracy of using a behavior based thermal network model to represent an inverter containing both the power modules and the heat sink is validated and analyzed. Furthermore, two of the most controversial issues in this research field were discussed in this thesis, including the influence of the temperature dependency of the materials' thermal properties on the thermal model and the accuracy of combining thermal subsystems directly to form the thermal model of the entire inverter. These results will be of great reference significance for engineering practice.

Based on the power loss model and thermal model, the fully coupled transient electro-thermal simulation of the inverter was performed and the dynamic performances of the junction temperature under different operating conditions, especially the stall torque condition, were predicted. The importance of considering the temperature dependency of the power losses and the thermal cross-coupling effects in the thermal model at the design stage of the inverter was also evaluated.

Finally, the experimental validation of thermal model of the entire inverter is carried out with both direct measurement method with thermocouples and indirect method with the TSEP. Good agreement between model and measurement was obtained.

The developed electro-thermal model can predict the long-term temperature profile within a relatively short simulation time period and it can also guarantee the accuracy of the estimated temperature fluctuation in short-term transient. This simulation model will provide crucial information for the thermal system design, especially for the determination of the design margin and the reliability analysis of the inverter. This information can be applied for the thermal management system design, package optimization, analysis of the device long-term reliability, and maximum rating characterization of the inverters.

6.2 FUTURE WORK

As mentioned in Chapter. 1, the reliability of the inverters is strongly affected by both the maximum junction temperature T_j and the temperature variations ΔT_j. Since these

temperature characteristics have been successfully evaluated by applying the electro-thermal model proposed in this thesis, future work should include studying of the relationship between these temperature characteristics and the reliability of the device.

In addition, the electro-thermal simulations presented in this thesis mainly focus on the thermal analysis of the inverter under some specific operating conditions. However, since the feasibility of using this model for long term simulation has been verified, it will be of very great referential value if this model can be used to simulate the dynamic performances of the junction temperature under real drive cycles of the motors or the vehicles.

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