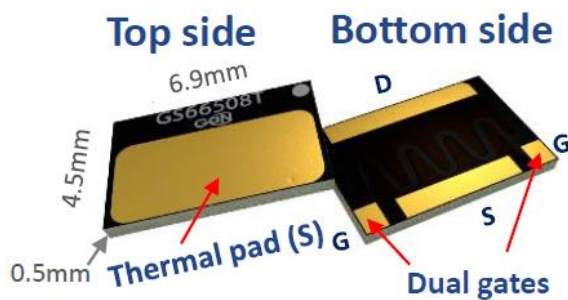


- In fact, the heat-sink that was installed in this inverter has not a known value of thermal resistance. Anyway, to resolve this problem, is possible to measure this parameter measuring at the same time the losses and the temperature of the heat-sink for different values of losses. Once this parameter is found it is possible to simulate the real working condition in the model and to compare correctly the results.

[1] FOSSATO, F. (2014). Loss estimation in a voltage source inverter for electrical drives.  
University of Padua.

### GS66508T (650V/30A, 50mΩ)



**Thermal pad internally connected to Source. However it is not designed for carrying current**

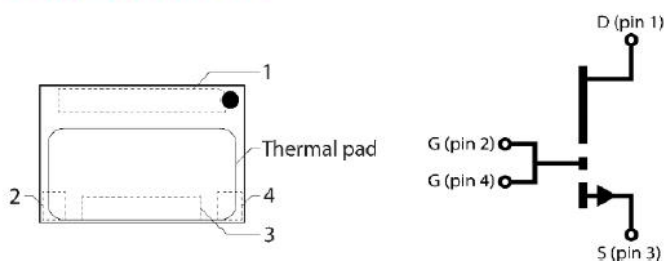


Figure: Top cooled

### GS61008P (100V/90A, 7.5mΩ)

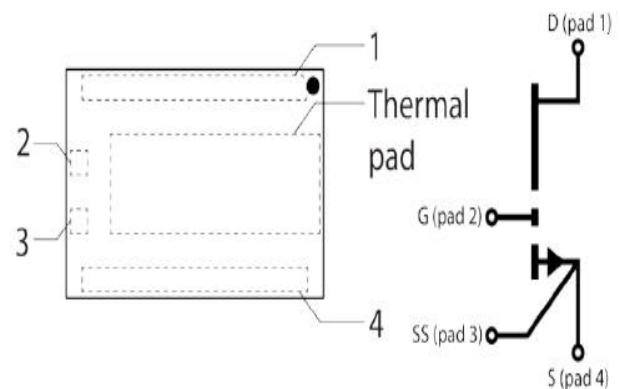
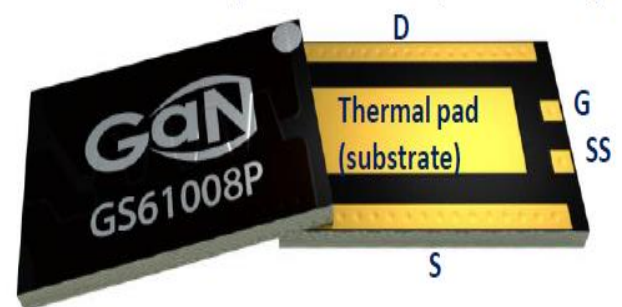
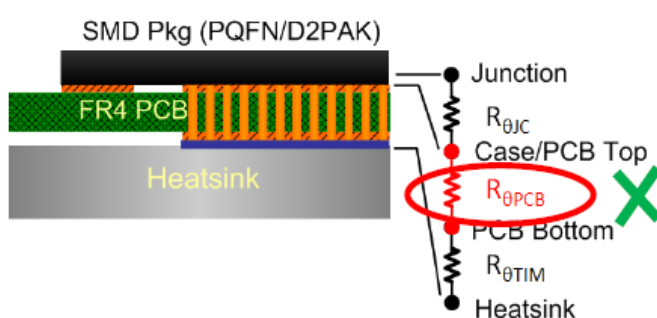
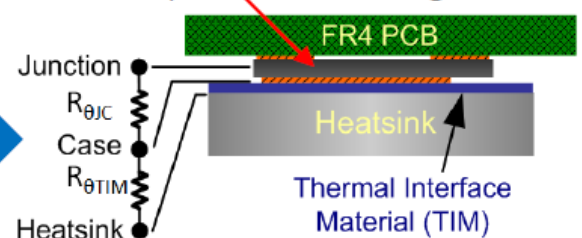


Figure: Bottom cooled



### GaNPX Top-cooled Package



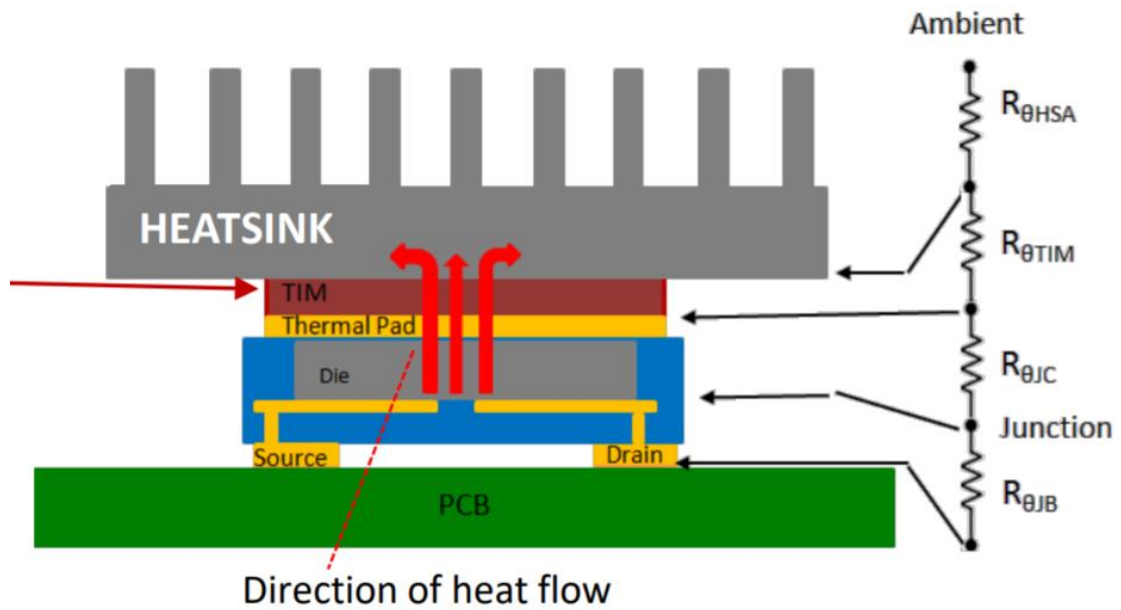


Figure: Top side cooling

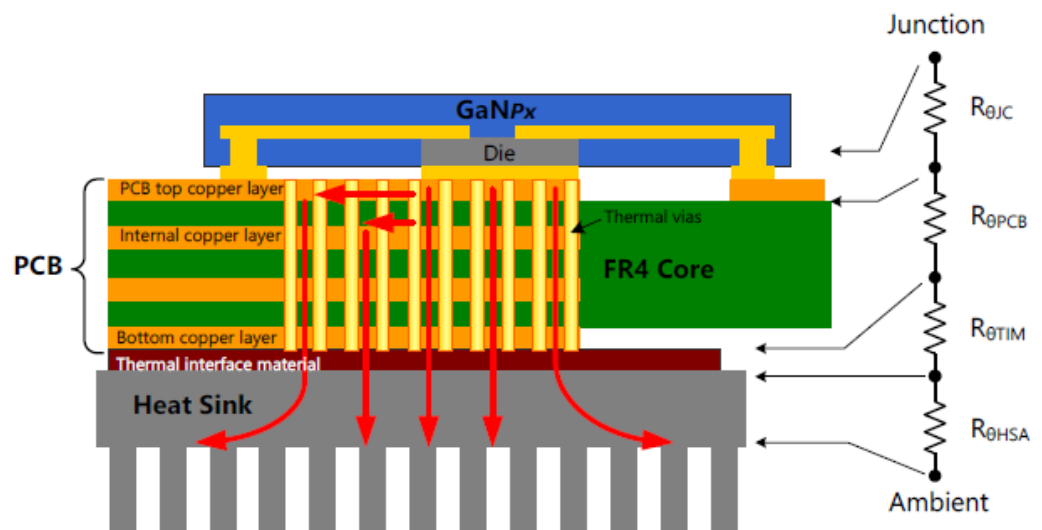
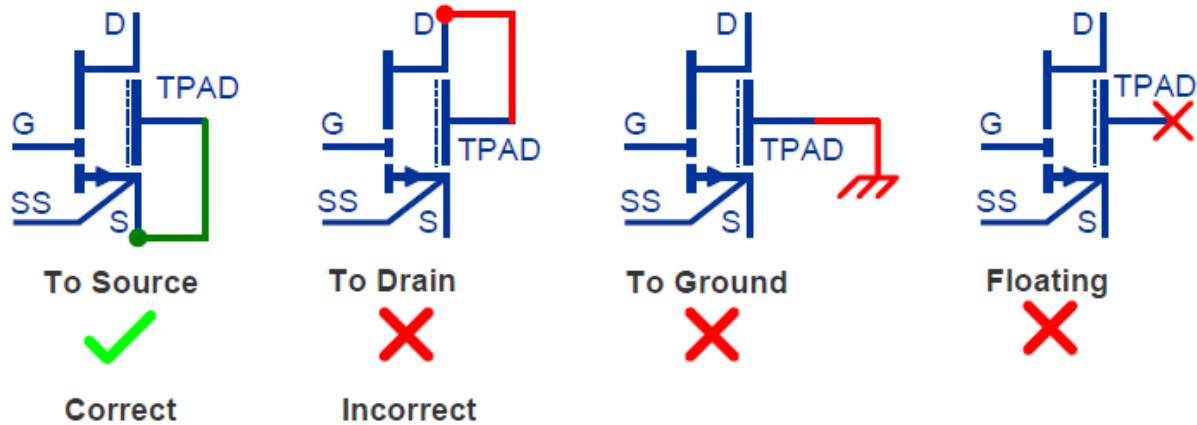


Figure 3 Cross section view of GaN<sub>pX</sub> package and thermal dissipation path

Figure:Bottom side cooling

The substrate or thermal pad must always be connected to Source on the PCB for optimum device performance (Figure 2). Any other substrate connections or connecting substrate to voltage potential other than Source affect the device parameters and reduce device performance. **DO NOT** connect thermal pad to Drain, keep floating or connect to ground (unless the source is also tied to ground).



**Figure 2 Substrate/Thermal Pad Connection**

## PCB thermal performance

### 1. Heat spreading copper pad

The top copper pad plays important role to conduct the heat from the small area under the device to larger area on the PCB. As such, the top copper layer must have sufficient thickness and area to provide enough heat spreading. **It is recommended to always use 2 oz (56.7 g) or thicker copper on all layers.** The internal and bottom layers also improve the heat spreading. The bottom copper pad serves as the contact surface to the heatsink or Thermal Interface Material (TIM) and it should have sufficient coverage to allow optimum heat transfer to the heatsink.

### 2. Thermal vias

The most effective way to improve vertical heat transfer for FR-4 PCB is to add plated through-hole thermal vias between conductive layers. **Since FR-4 material has very low thermal conductivity, thermal vias design is one of the dominating factors for total PCB thermal resistance.**

Below are some considerations for thermal vias design:

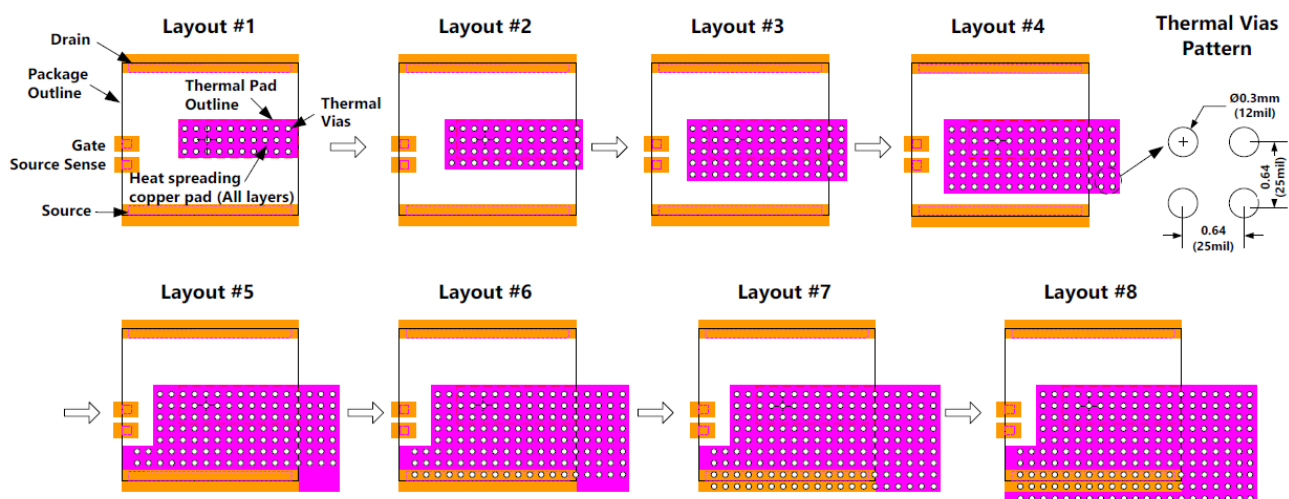
- Adding open plated through vias to the SMT pad (“Via In Pad”) is generally not a common practice as it may create the **solder-wicking issue**: the solder tends to be drained down into the vias during the reflow process and generates solder voids on the pad. Following steps can be taken to limit this problem:
  - o **Use small via diameter.** The surface tension of solder limits the amount of solder wicking on smaller vias. With 0.3 mm or smaller via diameter, the solder wicking can be reduced.

- o **Fill the vias with thermally conductive materials.** It eliminates the solder wicking but adds cost and extra manufacturing step.
- 8 mil (0.2 mm) is typical minimum mechanical drilling size. 12 mil (0.3 mm) is more common and lower cost.
- **IPC-6012 specifies minimum 0.8 mil (20  $\mu$ m) copper plating thickness for Class 2 PCB and 1 mil (25  $\mu$ m) is standard via plating thickness.**

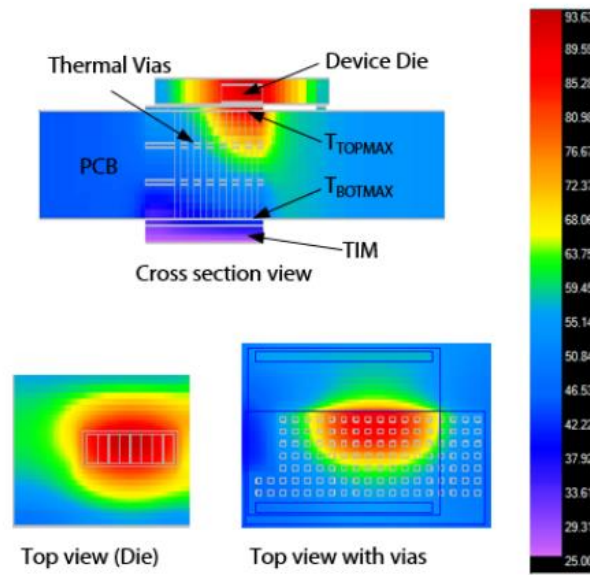
## GaN Systems Simulation

The first step is to determine the right size for the heat spreading copper pad and how many vias are needed under the thermal pad.

The design constraint rule is that no vias are added towards the drain side in order to maintain the same clearance between thermal and Drain pads. Also the left edge of the copper pad keeps minimum 0.5 mm distance from Gate and Source-sense pads. There will be no vias added on the left side the package as that area is typically used for gate driver circuit.



**Figure 4 PCB Layouts for copper area optimization**



**Figure 5 Example of thermal simulation results (Layout #5)**

The PCB thermal resistance  $R_{\theta PCB}$  is defined by:

$$R_{\theta PCB} = \frac{T_{TOPMAX} - T_{BOTMAX}}{P_{DISS}} \quad (\text{Eq.2})$$

where  $T_{TOPMAX}$  and  $T_{BOTMAX}$  are the maximum temperatures on the top and bottom copper layers, which are approximately located at the center of the die;  $P_{DISS}$  is power dissipation ( $P_{DISS} = 10 \text{ W}$ ).

**Figure: ElectroFlo® thermal analysis software was used for the thermal simulation**

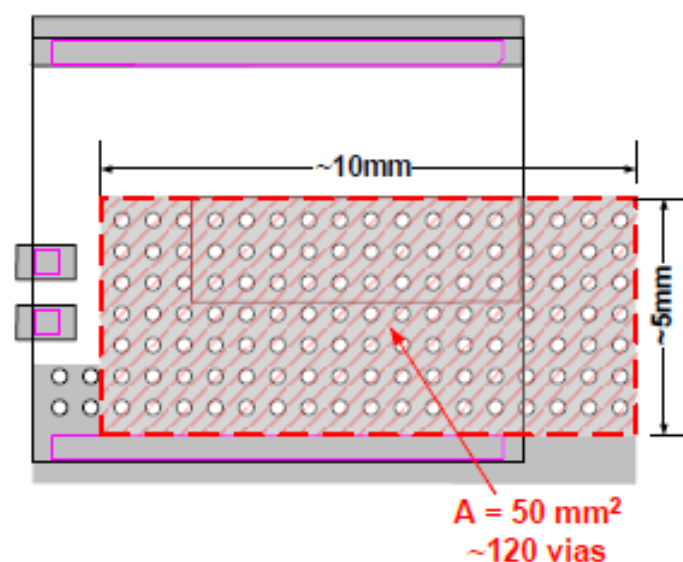
Both PCB and TIM thermal resistances decrease with the increasing of via numbers and copper area. **When number of thermal vias increase from 30 to 210 (Layout #1 to #8), the PCB thermal resistance  $R_{\theta PCB}$  drops almost 2.4 times from 11.5 °C/W to 4.8 °C/W. The TIM thermal resistance  $R_{\theta TIM}$  also reduces about 3 times as the contact area increases.**

**Table 1 Thermal resistance breakdown for 8 PCB layouts**

PCB Layout	Number of vias	$R_{\theta PCB}$ (°C/W)	$R_{\theta TM}$ (°C/W)	$R_{\theta JHS}$ (°C/W)
#1	30	11.54	5.25	17.29
#2	48	7.97	3.98	12.45
#3	70	6.46	2.83	9.79
#4	96	5.65	2.13	8.46

#5	123	5.13	1.95	7.58
#6	150	5.05	1.92	7.47
#7	179	4.91	1.85	7.29
#8	210	4.87	1.80	7.18

For optimum PCB thermal performance, it is recommended that the copper pad and thermal vias should cover at least 10x 5 mm area (50 mm<sup>2</sup>) under the thermal pad (or approximately 120 thermal vias), as shown in Figure 7.



**Figure 7 Recommended minimum copper area under thermal pad**

**Table 2 Thermal resistance with different number of copper layers and PCB thickness**

	1.6 mm PCB			1.0 mm PCB		
Layers	$R_{\theta PCB}$ (°C/W)	$R_{\theta TIM}$ (°C/W)	$R_{\theta JHS}$ (°C/W)	$R_{\theta PCB}$ (°C/W)	$R_{\theta TIM}$ (°C/W)	$R_{\theta JHS}$ (°C/W)
2	5.13	1.95	7.58	3.69	2.12	6.31
4	4.8	1.56	6.86	3.39	1.71	5.6
6	4.51	1.42	6.43	3.12	1.56	5.18

**PCB thickness has**

- less effect on TIM thermal performance and actually increases TIM thermal resistance by about 10 %.
- improvement on PCB thermal resistance