Design, Modeling, and Control of Multilevel Converter Motor Drive with Modular Design and Split Winding Machine

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***Abstract*—A multilevel converter utilizing machine windings to synthesize inverter outputs is proposed. The new multilevel converter overcomes the problems of classic multilevel converters, reduces the cost, size, and insulation requirement, and improves the performance of motor drives as well as electrical machines. The topology, advantages, modeling, control, and experimental results are presented in this paper.**

Keywords—multilevel converter; control; modeling; split winding; machine design

I. INTRODUCTION

In recent years, there has been increasing attention given to the efficiency of energy conversion. Electric motors utilize 45 per cent of global electricity. Increased energy efficiency in electric motors will provide the world with tremendous economic, environmental, human ecological, and security benefits.

An adjustable speed drive (ASD) is a power electronics device that controls the speed of machinery. ASDs also save energy for industry processes that require adjustable speed or control of flow from a fan or pump. ASDs have already replaced many conventional fixed speed drives in low-power and low-voltage applications such as air conditioners, washing machines, electric bicycles, and vehicles with stepless speed change, making up a large portion of the market. For high-power and medium-voltage (MV) applications including industrial air compressors, water pumping stations, cooling fans, railway traction systems, steel rolling mills, marine propulsion, and renewable energy systems, ASDs are even more attractive because the cost saving of electric power is even more significant than it is in low-voltage and low-power applications. MV products are generally considered to be in the voltage range of 2.3kV to 6.6kV and in the power range of 1-50MW [1]. At such voltage and power levels, the investment payback time for ASDs is only 1.0 to 2.5 years [2].

Multilevel converters are a preferred solution for adjustable-speed medium-voltage motor drives. Compared with conventional two-level converters or current source converters using high power semiconductor devices such as gate turn-off thyristors (GTOs), multilevel converters improve the output voltage waveforms and reduce the total harmonic distortion. At lower voltage levels, a large variety of less expensive, high performance semiconductor devices can be selected including insulated-gate bipolar transistors (IGBTs) and integrated gate-commutated thyristors (IGCTs). Using these mature medium-power semiconductor devices, multilevel converters improve performance, increase efficiency, and reduce semiconductor device cost up to 80% [3].

Since the first multilevel converter was invented in the late 1960s [1], multilevel converters have evolved over nearly a half-century. Some topologies have been successfully commercialized and have a wide range of applications in motor drives. However, multilevel converters now face new challenges in the 21st century including their efficiency, cost, size, and performance. In this paper, a new topology is presented which will change the way multilevel converters are designed. To make a comparison between the proposed multilevel converter and existing technologies, three classic topologies, and three other topologies, which have some similarities with the proposed design, are briefly reviewed.

Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-bridge (CHB) are considered as classic topologies because they have been commercialized for industrial products and widely used for decades [1]. Though there are a lot of multilevel topologies described in literature, most of them are variants of these three classical topologies. In this paper, these three classic multilevel converters are serving as benchmarks for comparison. Each of them has advantages and disadvantages depending on specific applications.

Fig. 1 shows a 3-phase, 3-level NPC with half of the dc-bus voltage on each of the capacitors. The voltage ratings of the diodes and switches in a 3-level NPC are also half of the dc-bus voltage. The diodes provide paths for ac current to flow and clamp the switch voltages. To avoid an over voltage on a switch, certain switching patterns should be followed. In general, an $n+1$ level NPC typically consists of n series capacitors with a voltage rating of V_{dc}/n, all switches and diodes are also rated at V_{dc}/n. To properly clamp the switch voltages, several diodes are connected in series between different levels. As a result, the number of diodes in an $n+1$ level, 3-phase NPC is $3n(n-1)$, yielding a quadratic growth as a function of n. The 3-level NPC is popular because of a simple front-end rectifier design and lower device count. When the number of levels is more than three, the unequal power provided by each level will cause unbalanced capacitor voltages. In theory NPC can only provide reactive power, so to supply real power and balance the capacitor voltages, NPC must be paired with another front-end AC-DC converter, which provides the exact amount of unequal real power [5]. Moreover, with more than three levels, the device stresses are also unequal and consequently, switching devices are overdesigned and incur extra losses and cost.

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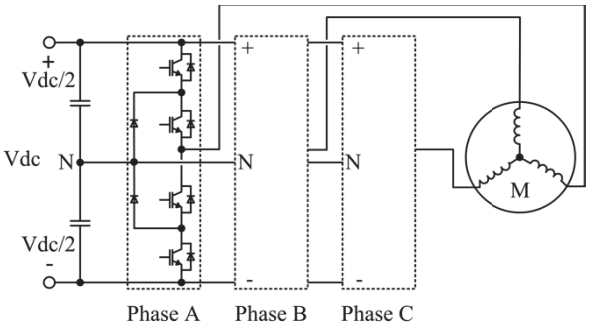


Fig. 1. 3-level 3-phase Neutral Point Clamped topology

The Flying Capacitor topology, as illustrated in Fig. 2, was introduced in the late 1960s. The capacitors between switches are floating and clamp the switch voltages. In general, an *n+1* level FC has *n* dc-bus capacitors and *3n(n-1)/2* auxiliary capacitors. Although FC can provide real power and has a simple front-end rectifier design, switching patterns are complicated and switching frequencies are higher in order to balance the capacitor voltages. It requires a combination of different output voltage levels in one fundamental cycle to balance the charge and discharge of each capacitor [6].

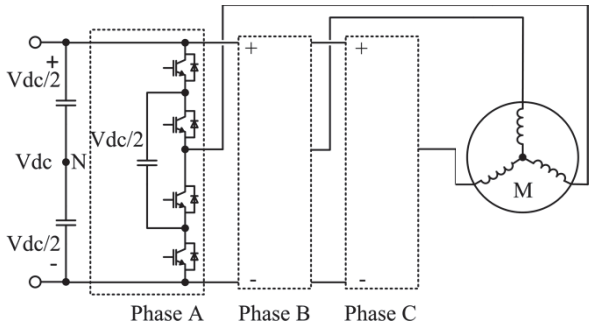


Fig. 2. 3-level 3-phase Flying Capacitor topology

Fig. 3 shows the Cascaded H-bridge topology. Different from the NPC and FC topologies, there are no extra clamping diodes or floating capacitors in CHB. Each H-Bridge can provide 3-level outputs: $-V_{dc}/n$, *0*, and V_{dc}/n. The output terminals of H-bridges are connected in series, leading to a superposition of the output voltages from each H-bridge. As a combination, a *2n+1* level CHB consists of *n* H-bridges in each phase, from which it is possible to generate an output of $\pm kV_{dc}/n$ (*k* from *0* to *n*). Since CHB does not have auxiliary capacitors or diodes that lead to a quadratic growth with the number of the level *n*, it is possible to construct a CHB with more output voltage levels (up to 17 [1]). CHB has drawn significant attention because of its modular structure. Compared to NPC and FC, CHB can reach higher voltage and power levels. However, there are apparent disadvantages associated with CHB. First, CHBs are supplied by isolated voltage sources or phase shift transformers for each bridge. The required number of individual voltage sources or transformer windings is *3n* for three phases as shown in Fig. 3. A 36-pulse rectifier system for CHB improves the power quality but it is complicated and more expensive. Second, each H-bridge only supplies a single-phase current, and the instantaneous power from the dc source is fluctuating, inevitably requiring extra power buffering capacitance and physically oversized dc capacitors.

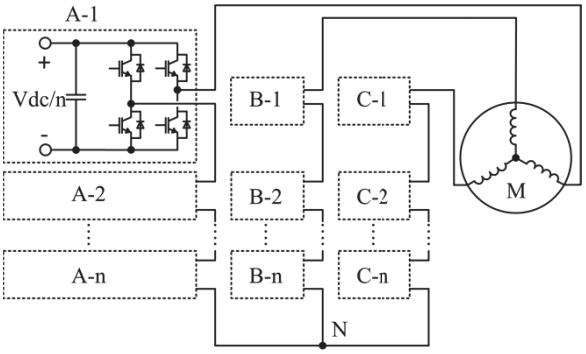


Fig. 3. *2n+1* level CHB topology

Fig. 4 shows a medium-voltage inverter topology that solves some problems of CHB [4]. Instead of having one individual dc source for each single-phase bridge, the topology shown in Fig. 4 only requires one individual dc source for each three-phase bridge. The capacitor size is reduced because the three-phase topology has little power fluctuation. However, extra transformers, which inevitably increase the cost, size, and loss, are needed in this topology to combine the output voltages from each bridge. The same authors proposed another multilevel converter topology without combining transformers [8]. The topology shown in Fig. 5 utilizes one of the machine winding properties: standard windings of medium voltage motor can be reconnected into several three-phase groups, where all the machine electrical and mechanical properties are maintained. Each group is driven from a separate three-phase inverter. The output voltages of the inverters are combined by the machine windings instead of transformers. However, each inverter still needs an isolated voltage source, and the front-end rectifier and input transformer are expensive and complex.

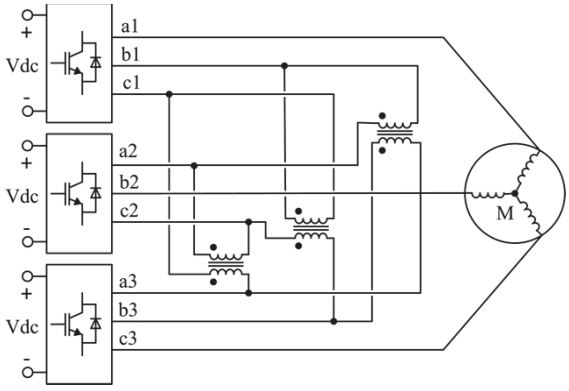


Fig. 4. New MV inverter topology

Proposed in [9] and shown in Fig. 6, a hexagram multilevel converter consists of six 3-phase inverter bridges interconnected through inductors. The six output terminals of the hexagram converter are connected to an open-winding, 6-lead machine. The voltage stresses on each inverter are further decreased and allow for the use of lower voltage semiconductor devices with better switching characteristics. The hexagram multilevel converter is a three phase modular design, which is easy to maintain and construct, and has a lower dc capacitance requirement than CHB. However, this

topology not only requires isolated voltage sources, but also needs extra inductors. Similar to multilevel converters in Figs. 4 and 5, the extra inductors increase the converter cost, size, and loss, and the front-end rectifier for the hexagram converter is more expensive and complicated. Moreover, certain switching patterns are prohibited to prevent circulating current between different inverters.

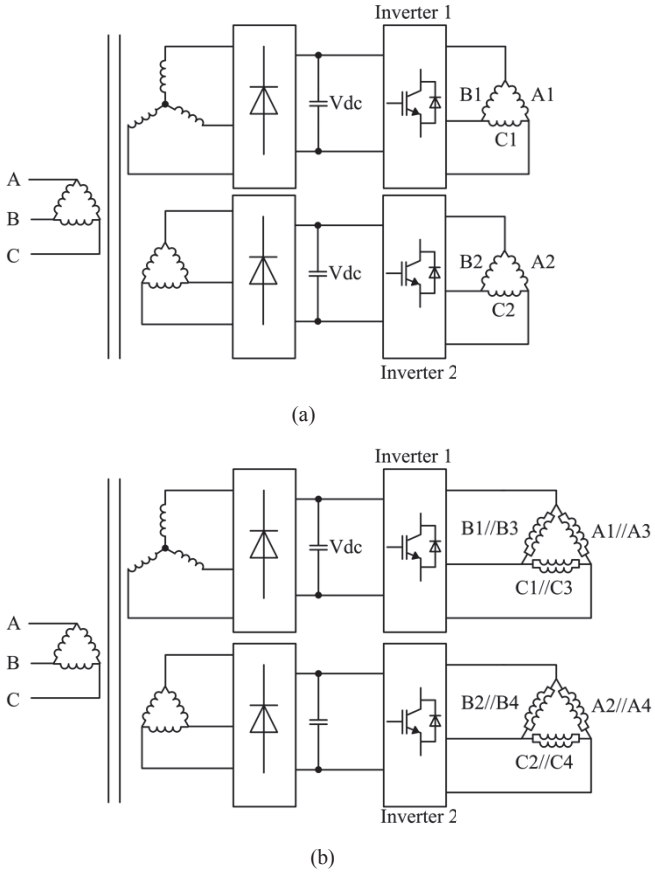


Fig. 5. (a) Multilevel topology for a machine with two pole-pairs (b) for a machine with four pole-pairs

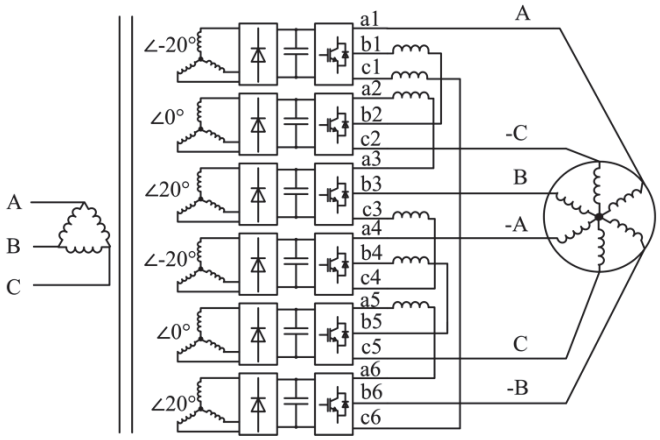


Fig. 6. Hexagram multilevel converter

Many of the multilevel converter topologies have been successfully commercialized successfully and proven to be feasible technologies. As stated above, there remain a number of challenges including efficiency, compactness, modularity, reliability, and cost. An ideal multilevel converter would have the following characteristics: 1) it would have a modular design that is reliable and easy to construct and maintain; 2) the output voltage levels are unlimited and easily expanded with few constraints; 3) the front-end rectifier or the input transformers should be simple and independent from the multilevel inverter; 4) the multilevel converter requires only one dc-input voltage source, if necessary, several multilevel converters can share the same front-end rectifier or a common dc bus; 5) the semiconductor devices would have even stress; 6) the input dc capacitors handle a balanced constant power instead of single phase pulsating power; 7) there is no voltage balance problem in dc capacitors; 8) allow the use of low voltage, better performance, less expensive devices instead of conventional high voltage, more expensive devices; 9) it would have no clamping diodes, clamping capacitors, extra transformers or inductors; 10) simple and flexible in switching patterns, design, and control.

In this paper, a new multilevel converter topology that is a compact, simple and flexible solution is proposed. The quantity of power components is minimized because there are no extra clamping capacitors, clamping diodes or isolated voltage sources. Only one dc source processing constant power is needed at the input. The number of voltage levels is easily expanded, independent of the front-end rectifier design. Through co-designing both the drive and machine, the proposed multilevel converter can also benefit electric machines.

In Section II, the proposed topology is illustrated and a comprehensive comparison between the proposed topology and existing multilevel topologies is presented. In Section III, key technologies for the proposed topology is introduced, including the interleaving technique and the voltage balancer technique. In Section IV, simulation and experimental results are presented to verify the proposed concept. Sections V concludes the paper.

II. PROPOSED MULTILEVEL CONVERTER TOPOLOGY

The component quantity in DCC and FC topologies is quadratic in growth for the number of voltage levels n. For this reason, the number of voltage levels in these topologies usually does not exceed five otherwise the system complexity and cost will be onerous [1]. The component quantity of a CHB topology is linear in growth for the number of levels, but it requires separate dc sources increasing the complexity of the front-end rectifier. Though these dc voltage sources only supply partial dc voltages (V_{dc}/n), they are floating and require extra insulation between bridges.

Figs. 5 and 6 show topologies that utilize machine windings to realize multilevel converters. These topologies indicate that the co-design of electrical machine and multilevel converter has the potential to increase the overall system performance, and reduce the size and cost. However, the inputs of these topologies still come from several separate isolated dc sources. As a result, these topologies have limited output voltage levels and complex front-end rectifier design.

A desirable topology is one that provides the advantages of each existing topology while minimizing the disadvantages. The topology should provide the flexibility to extend to higher levels like the CHB, but without the use of separate isolated dc sources. The component quantity should be minimized to reduce system complexity and cost.

Fig. 7 shows the proposed topology. Each module is a 3-phase inverter and handles only constant power unlike the pulsed power seen in the Cascaded H-bridge. All the inverter modules are connected in series and share the same dc input, but there are no clamping diodes or clamping capacitors as in the Flying Capacitor or Neutral Point Clamped topologies. The output ac terminals of the inverter modules power different groups of machine windings and the total output voltage is combined inside the machine without any extra components. Compared to the topologies in Figs. 4, 5 and 6, no extra inductors, extra transformers, or isolated input dc sources are needed to realize a multilevel output in the proposed topology. In [10], this topology is used in an integrated modular machine drive with low-voltage GaN semiconductor devices, and has been proved to be feasible.

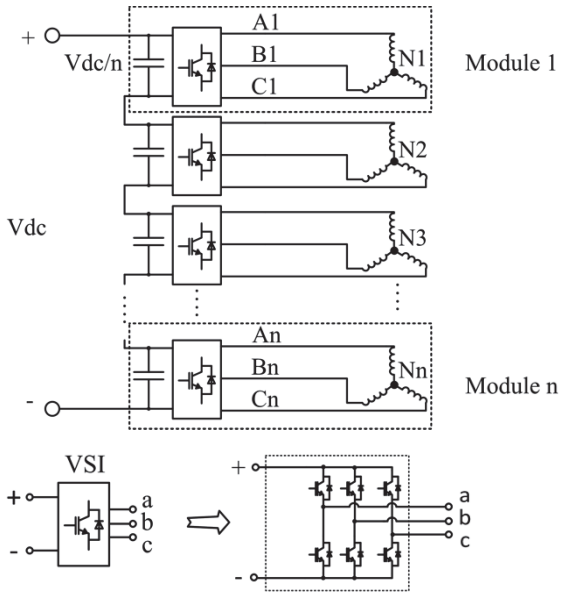


Fig. 7. Proposed topology with an *n+1* level

This topology benefits both the machine design and multilevel converter design. By recognizing that a machine itself is a large magnetic component and its windings are magnetically coupled with inherent electrical isolation, it allows for the design of a multilevel converter that takes advantage of these important properties. The multilevel can then utilize the machine windings, stator, or even rotor as coupling transformers, inductors, or filters to achieve a multilevel output. Machine manufacturers usually connect all the machine windings in series as shown in Figs. 8(a) and (b), but these machine windings can be disconnected and reconnected into several winding groups. In the proposed topology, individual machine winding groups have the same gauge, number of turns, and configuration as conventional ones. The only difference is that the interconnections between the windings are changed. As shown in Fig. 8(c), machine windings are connected to their local neutral points and the leads Ax, Bx and Cx are connected to their local three-phase input terminals. This kind of machine winding configuration maintains all the electrical and mechanical properties of the machine, but reduces the machine manufacture costs by eliminating the interconnection copper wires between different pole-pairs.

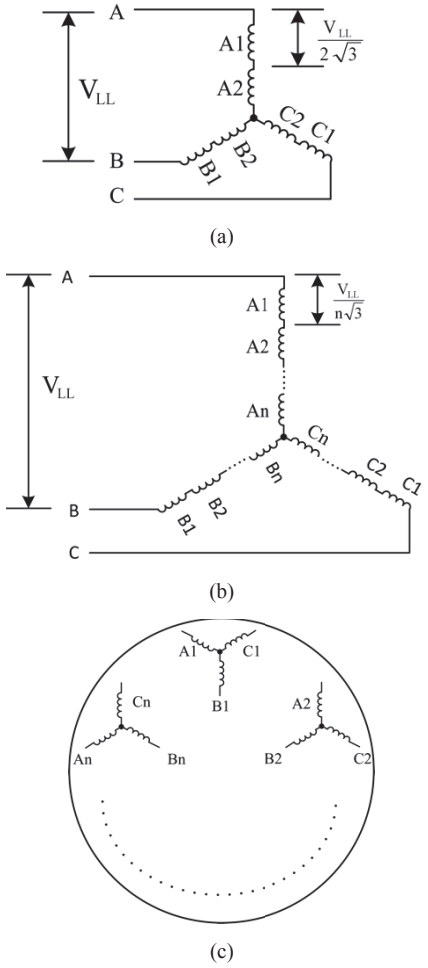


Fig. 8. (a) Conventional machine winding configuration of a two-pole-pair machine (b) Conventional machine winding configuration of a four-pole-pair machine (c) Proposed machine winding configuration

Compared with conventional multilevel converter topologies, the proposed topology has the following advantages, which make it very attractive for motor drive applications.

A. Significant Reduction in Component Quantity

Compared with topologies discussed in Section I, the proposed topology reduces the number of diodes, capacitors and separate DC sources and operates without extra transformers or inductors. Reduced component counts are made without degradation to the system performance. As a result, the proposed drive system has a compact size and lower cost. The component quantities in the proposed topology and classic multilevel topologies are summarized in Table I. It shows that the proposed topology has the same number of switches compared to NPC, FC and CHB. However, there are

no clamping diodes or balancing capacitors in the proposed topology compared to NPC, and FC. The proposed topology has the same number of dc input capacitors compared to NPC and FC but has less than CHB. Unlike CHB, the proposed topology only needs one separate dc source. Different from NPC and FC, the device stresses in the proposed topology are even, which means the proposed topology is easily extended to more output levels.

TABLE I. COMPONENT QUANTITIES IN DIFFERENT TOPOLOGIES TO REALIZE THREE PHASES N+1 LEVELS OUTPUTS

	Switch #	Diodes #	Balancing Caps. #	DC Bus Caps. #	Separate DC Sources #	Device Stress
NPC	*6n*	*3n(n-1)*	*0*	*n*	*1*	Uneven
FC	*6n*	*0*	*1.5n(n-1)*	*n*	*1*	Uneven
CHB	*6n*	*0*	*0*	*1.5n*	*1.5n*	Even
Proposed	***6n***	***0***	***0***	***n***	***1***	**Even**

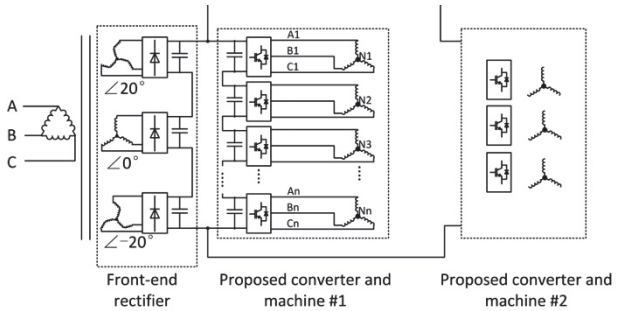
*The body diode of a switch is integrated and it is not counted in the table

B. Unlimited Flexibility and Performance Optimization

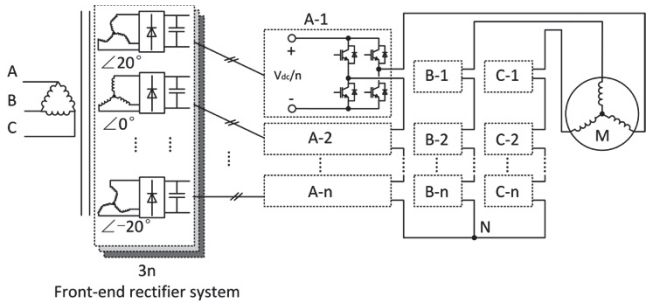
The proposed design is flexible and can accommodate a wide range of voltage levels and power ratings. Modules shown in Fig. 7 are connected in series to reduce the input voltage *Vdc* to V_{dc}/n. This also reduces the voltage stresses on the power devices allowing for the use of low-voltage, less-expensive devices such as MOSFETs instead of high-voltage, more-expensive devices such as IGBTs. For any system with a specific voltage and power rating, the proposed topology can utilize a wide variety of lower voltage semiconductor devices and different types of capacitors such as film or ceramics. As a result, the performance, size, and cost of the whole system can be optimized.

C. Compatibility with Different Systems

The proposed topology can be supplied by either a single dc source, or several dc sources to power each module. The front-end rectifier design is separated from the multilevel converter. Whether or not a single rectifier, multiple 12-pulse rectifier, dc grid, or batteries supply the dc sources, the proposed topology is always compatible. The voltage rating, power rating, and the number of front-end rectifiers can be different from the proposed multilevel converter. Several multilevel inverters can also share the same rectifier such as in an industrial dc bus system. Fig. 9(a) shows two proposed multilevel converters sharing the same input rectifier and driving two individual machines. In comparison, Fig. 9(b) shows the front-end rectifiers for a CHB converter.



(a)



(b)

Fig. 9. (a) Proposed converters drive two machines with the same input rectifier (b) CHB converter needs multiple separate input rectifiers

D. Modular Design

All inverter modules in the proposed topology are identical. The benefits of modular design include manufacturing cost reduction, faster product development, easy maintenance, and simple construction. In comparison, the NPC and FC topologies cannot be easily modularized because of uneven switching stresses. CHB is a modular design but it needs separated dc sources and its capacitors are oversized. Moreover, each module in CHB needs different gate signals, making control hardware complicated. The proposed topology has identical gate signal commands for each module (with a phase-shift for interleaving,) enabling a fully modular design. As shown in Fig. 10, each module in the proposed topology can also be NPC and FC too in order to further increase the output voltage levels and reduce the winding leads.

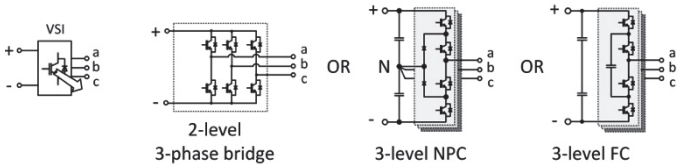


Fig. 10. The proposed topology is a flexible, compatible modular design

E. Release of Insulation Burden and Extended Service Life

In electrical machines, a critical factor that can shorten a product service life is the aging of insulation layers. In conventional multilevel converters, the thickness of insulation layers is proportional to the line-to-line output voltages. In the proposed topology, as inverter modules are connected in series, the common mode voltage and differential mode output voltages on insulation layers are reduced to to V_{dc}/n. As the number of dc levels increases, the voltages of each level decrease, further reducing the insulation burden between windings. With thinner insulation layers, the electrical machine is smaller and less expensive.

F. Reduction in Capacitor Size

In the proposed topology, all capacitors are connected to three-phase bridges with constant instantaneous power flow. Because there is no pulsating power, the capacitor size is only determined by the voltage or current ripples, which is related to the switching frequency and load current. In the CHB topology, every module is a single-phase full-bridge and the capacitance is oversized due to the instantaneous power fluctuation, which is related to the load current and the

fundamental frequency of the machine, not to the switching frequency of the converter. As a result, in the proposed topology, the capacitor sizes are smaller and can be further reduced by increasing the switching frequency. Increases in switching losses, due to higher switching frequency, are mitigated by the use of fast, low voltage, high performance devices in the proposed topology. Moreover, the capacitor size can be further reduced by the interleaving technique introduced in the next section.

G. Better Fault Tolerance and Fault Detection

The proposed topology has access to the voltage and current of each machine winding enabling detection of machine faults quickly and accurately through measurement of winding voltages. When one module is in a fault condition, the voltage of this module drops to zero and the voltage of other modules increases from V_{dc}/n to $V_{dc}/(n-1)$. In this way, the whole multilevel converter can operate without shutting down, despite the machine losing a winding group and possibly reducing the torque. Temporary operation with the increased voltage will not damage the inverter modules as modules are usually designed with 20 per cent to 30 per cent overvoltage redundancy.

The disadvantage of the proposed topology is the increased number of machine leads. However, this disadvantage is not a fatal problem because large machines usually have 6 leads for reconnection as discussed in [8]. Even for a normal 3-lead machine, a split-winding design can be applied to an integrated modular machine drive as illustrated in [10-12]. An integrated modular motor drive structure eliminates the interconnection wires between the proposed multilevel converter and the machine windings. It also increases fault tolerance and reduces the winding overvoltage due to the elimination of cable transmission effects. For a non-integrated machine drive, as long as the proposed multilevel converter is close to the machine, it can be easily installed. As there is only one dc bus between the front-end rectifier and the proposed multilevel converter, the place for the rectifier installment is flexible.

III. Design, Modeling, and Control

A. Machine Winding Configurations

The proposed topology requires the target machine to have multiple leads that match each other in electrical properties. A motor usually has multiple pole-pairs and multiple slots in each phase. Windings in these pole-pairs and slots can be split into several groups under certain rules: The different groups are located in different poles, or in different slots but in the same pole. These are the two fundamental winding configurations for the proposed design. In a real machine, these two configurations can both be implemented to create a more complex configuration. The two fundamental configurations are simplified as follows to identify the basic principles.

Fig. 11(a) illustrates winding configuration 1 for a 3-phase, 4-pole and 12-slot motor (1 slot per pole per phase). The windings in different pole-pairs are split into two groups. The two groups are connected in series or in parallel in the machine, sharing the same output terminals. For the proposed multilevel converter, the machine windings in different pole-pairs can be separated, each having their own neutral points N1 and N2, and output terminals A1 and A2. This kind of configuration does not change the motor electrical properties nor induce extra costs.

Winding configuration 2 is shown in Fig. 11(b). A 3-phase, 2-pole, 12-slot machine has distributed lap-winding coils. 2 slots per pole per phase are split into two groups. These groups are usually series connected in a conventional motor to form a lap-winding configuration. A machine split in this way is also called a six-phase machine. For the proposed multilevel converter, the machine windings in different slots can be separated each having their own neutral points N1 and N2, and output terminals A1 and A2.

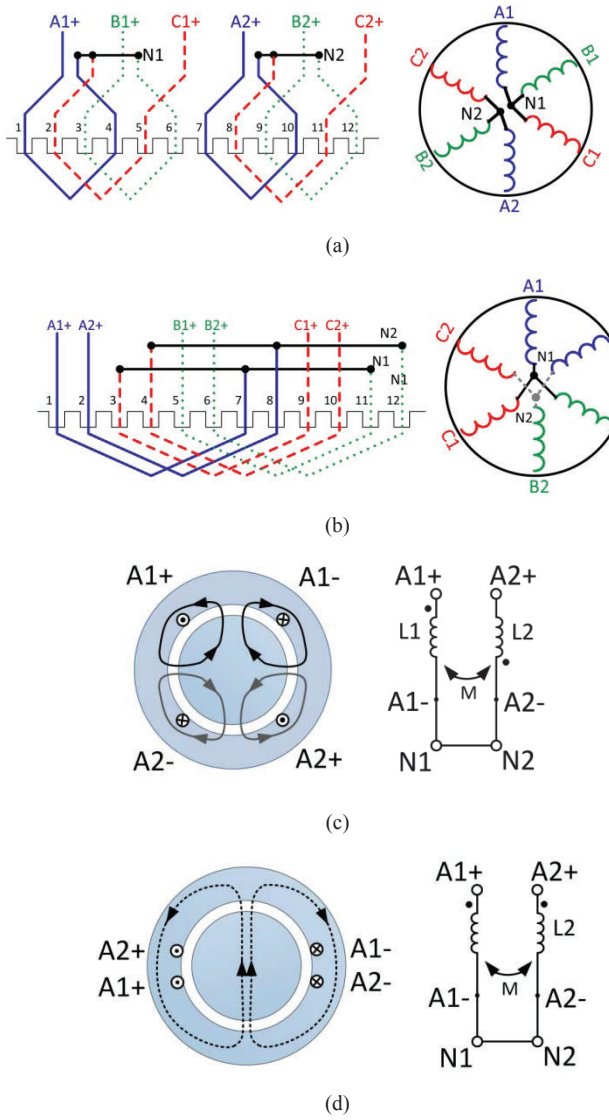


Fig. 11. (a) Winding configuration 1: windings in different pole-pairs (b) Winding configuration 2: windings in the same pole-pair but different slots (c) Coupling factor of configuration 1 (d) Coupling factor of configuration 2

Both winding configurations can be used for the proposed converter topology. Actual designs can be a combination of these two configurations. Machines with 2P poles with N slots per phase in each pole can be split into P·N segments.

However, when different winding configurations are applied, there will be different coupling effects as shown in Fig. 11 (c) and (d). These coupling effects will not change the proposed topology but will influence module interleaving as discussed below.

B. Module Interleaving Technique

In [13] and [15], researchers have built ASDs with smaller capacitor sizes by a gate signal interleaving technique to reduce the capacitor ripple current. Compared with non-interleaving cases, the input voltage and current ripple after interleaving has higher frequencies and smaller amplitudes. Thus interleaving allows for smaller dc-bus capacitors, which stabilize the dc-bus voltage and smooth the input current [15], while maintaining the same amount of voltage/current ripple at the dc input.

A similar idea can be applied to the proposed system to reduce the total capacitor voltage ripple and the capacitor size. The total dc-bus voltage, V_{dc}, is the summation of each module voltage. By shifting the gating signals of the series-connected inverter modules by 360°/*n* (*n* is the total number of modules), the module voltage ripple will be out of phase with each other and cancel out. The total voltage ripple amplitude is reduced and the equivalent frequency is *n* times the switching frequency. On the other hand, interleaving allows the use of smaller dc-bus capacitors to produce the same amount of voltage ripple on V_{dc} as a non-interleaving converter.

Fig. 12 illustrates an example for *n*=2. The duty ratio commands for two modules are identical, meaning that the output waveforms of two modules have the same fundamental frequency and amplitude. The triangular carrier waveforms of the two modules are shifted by 180 degrees. After the output voltage waveforms are added up, the second order harmonics and part of higher order harmonics are canceled.

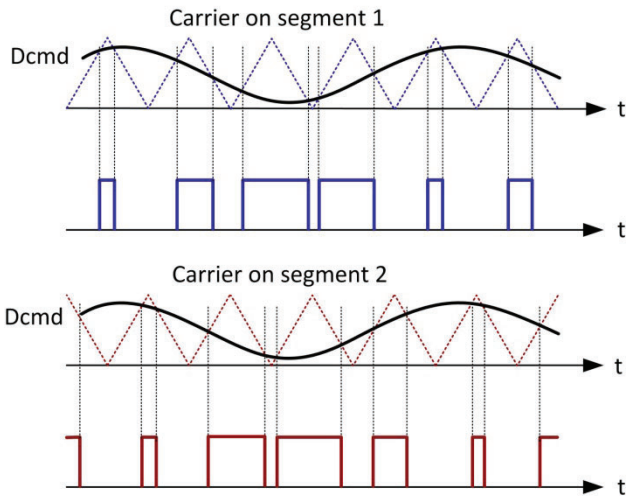


Fig. 12. Example of gating signal interleaving technique when the number of voltage levels is *n=2* and the gating signals are shifted by *180°*

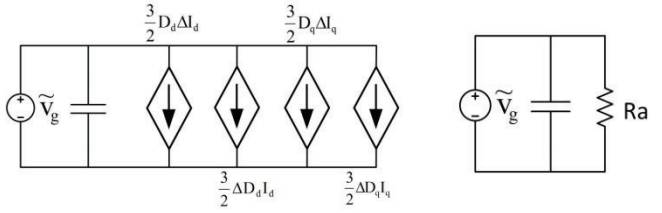
With the gating signal interleaving technique, the magnetic coupling between different groups will influence the current ripple of the converter output. According to [16], a negative or a small coupling factor results in a smaller current ripple if the interleaving technique is applied. For this reason, winding configuration 1 benefits from the interleaving technique because it has a negative coupling factor as shown in Fig. 11(c). When the coupling factor is positive and not negligible as shown in Fig. 11(d), interleaving needs to take special consideration of the leakage inductance otherwise the ripple current will be increased instead of decreased. However, the coupling factor value does not affect the inverter modules ability to be connected in series as shown in the proposed topology.

C. Active Voltage Balancers

Module inverters in the proposed topology are connected in series and drive machine windings independently. In a normal condition, all the windings are balanced and consume the same amount of real power. Any mismatches with the motor or inverter modules due to machine manufacture asymmetry, partial saturation, unbalanced magnetics, or even worse, a fault with any machine windings or inverter modules, the machine windings will have different electric properties and cause the dc input voltages of inverter modules to be unequal. Unbalanced machine windings degrade the fault tolerance and control stability of the converter. To prevent this from happening, an extra control algorithm needs to be applied to the proposed topology that balances the modules input voltages. Similar work has been done in input-series-output-parallel dc-dc converters. As shown in [14] and [17], in order to control series-connected module's input voltages, the controller adjusts the duty ratio commands for each module to have identical power outputs. In the proposed topology, the control algorithm is similar, but differs from dc-dc converters because both the d-axis and q-axis are involved in a three-phase ac system. Moreover, the leakage inductance of the machine needs to be considered in the d-q decoupling.

The voltages of series-connected capacitors may be balanced by passive resistors, which are in parallel with the capacitors. These passive resistors usually have large values in the range of 10kΩ to 200kΩ. The current balancing capability of these resistors is several milliamperes. This may be sufficient for balancing the capacitor leakage current since the leakage current is less than 1μA. However, in the proposed topology, the current difference is much larger than the capacitor leakage current. In order to realize voltage balancing, passive resistors have to be smaller than 10Ω in order to provide a 0.1A/V balancing current. It is unachievable to install such small resistors because the conduction loss of these resistors will be tremendous. In [18], a semi-active voltage balancer is proposed that has large balancing current and small steady state loss. In the proposed topology, an actively controlled virtual resistor is realized in the control algorithm to balance the module voltage. Fig. 13(a) shows the input small signal model for a three-phase inverter [19], where $\hat{v}_g$ is the unbalanced voltage error. To realize an active balance resistor, the duty ratio is manipulated to create a balancing current that is equivalent to the current consumed by a passive resistor as shown in Fig. 13(b). To achieve the same balancing results as a passive resistor, the following equation (1) must be satisfied. The small signal of current can be neglected because the current loop has much slower dynamic response than the voltage balance resistor.

$$\frac{\tilde{V}_g}{R_a} = \frac{3}{2}\Delta D_d I_d + \frac{3}{2}\Delta D_q I_q \quad (1)$$



(a) (b)

Fig. 13. (a) Small signal model of one module (b) The equivalent small signal model of active voltage balance resistor

An example of a 2-level converter controller is built as shown in Fig. 14. It implements active voltage balance control allowing it to perform like the active balance resistor shown in Fig. 13(b). The active resistor Ra can be programmed to a desired value. The balancer will generate amended values of ΔD_d and ΔD_q to realize the control algorithm.

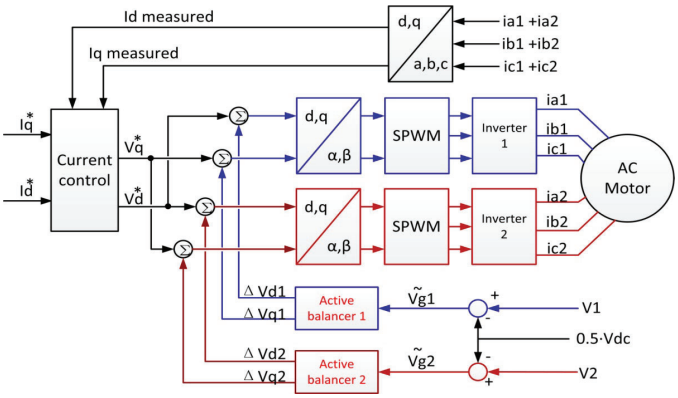


Fig. 14. Active balancer controller block diagram

IV. SIMULATION AND EXPERIMENT RESULTS

A. Simulation Results: Active Balancers

As shown in Fig. 15, the machine windings have an unbalanced load, which causes the module dc input voltages to be out of balanced. The results of simulations with and without active voltage balancers are illustrated in Fig. 16. Without an active balancer, the upper module has the same duty ratio as the lower module. Since the loads are different, the load current of the upper module is larger than that of the lower module. The dc input voltage of the upper module drops until the load current is as the same as the load current in the lower module. With an active balancer, the proposed topology is able to reject the load variation and imbalance, and maintain equal dc-bus voltages on two modules as shown in Fig. 16.

B. Simulation Results: SPM Machine Startup with a Constant Torque

In simulation, the balance virtual resistors Ra1 and Ra2 are programmed to 1Ω. Fig. 17 shows the simulation results of a SPM machine startup with constant torque. These simulation results prove that the proposed topology works properly for the standard closed loop current control and the dc input voltages are well balanced because of active balancers.

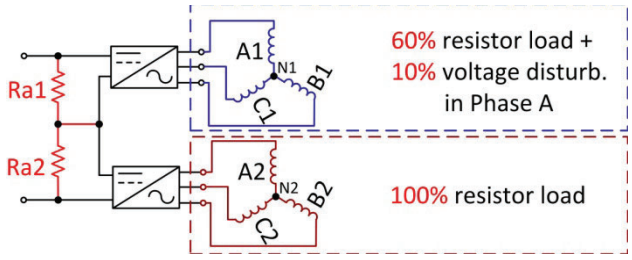


Fig. 15. Simulation of unbalanced load condition

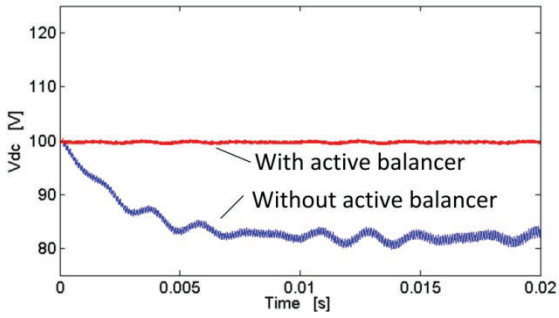
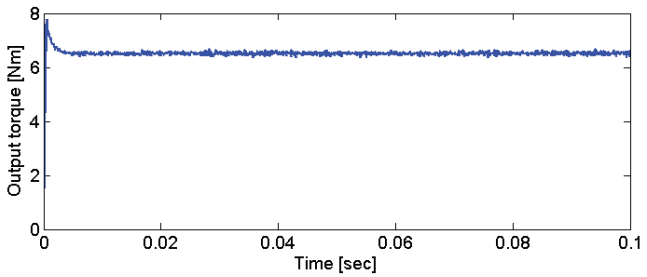
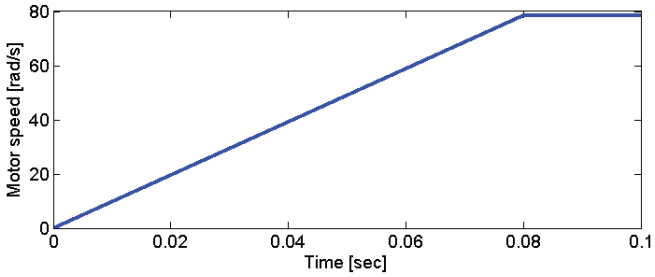


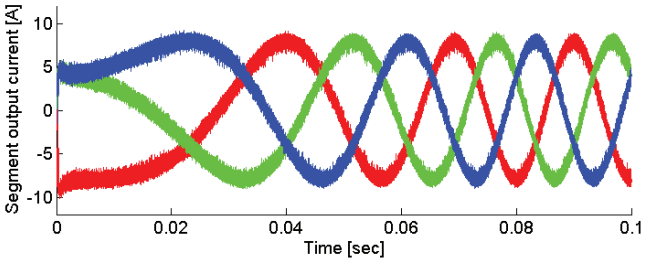
Fig. 16. The voltages of the upper module



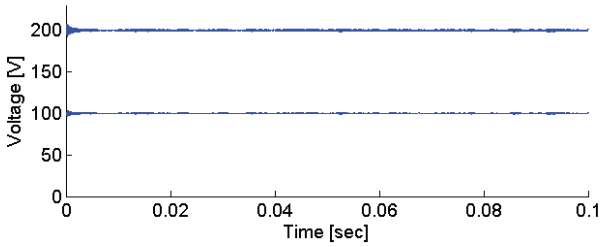
(a)



(b)



(c)



(d)

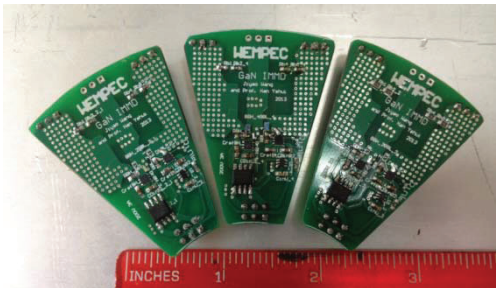
Fig. 17. Simulation results of the proposed converter during a startup (a) Output shaft torque of the machine (b) Motor speed (c) Three-phase output current waveforms (d) Voltages on dc-bus capacitors

C. Experiment Results: Test with RL loads

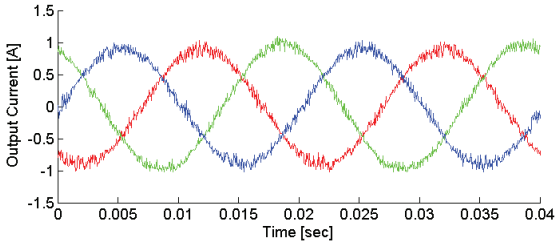
Two inverter modules are built, each rated at 150V, 3A as shown in TABLE II. The module driver is equipped with isolated digital voltage and three-phase current sensors. In Fig. 18(b), the three-phase 50Hz ac currents generated by the converter are shown. The voltages on each module are automatically balanced, as illustrated in Fig. 18(c). The benefit of interleaving is also validated, as experiment results in Fig. 18(d) shows at least 35% reduction in the dc-bus current ripple.

TABLE II. PARAMETERS OF THE PROPOSED CONVERTER UNDER TEST

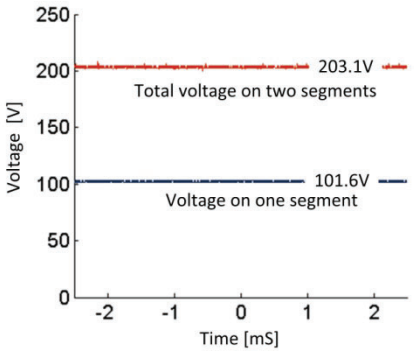
Vdc	150 [V]
Line Current	3 [Arms]
DC-Link Capacitance	36 [μF]
Converter Height	0.6 [inch]
Inverter radius	3 [inch]



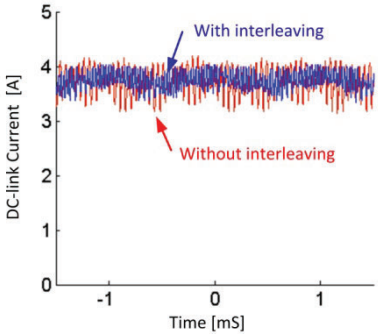
(a)



(b)



(c)

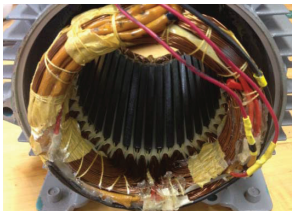


(d)

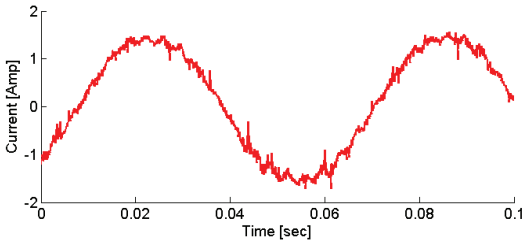
Fig. 18. (a) Photograph of the converter prototype (b) 3-phase output current waveforms (c) Voltage balances between two modules (d) Dc-bus input current

D. Experiment Results: Test an Induction Machine

A 3-lead induction machine has been rewound into 6-lead windings to match the proposed topology with 2-level inverters. Fig. 19 shows the machine and the input current of one phase. There is no load on the induction motor, but the converter is shown to have the ability to run the machine smoothly.



(a)



(b)

Fig. 19. (a) Photograph of the rewound induction machine (b) One phase output current waveform

V. CONCLUSION

In this paper, a new multilevel topology utilizing machine windings to synthesize inverter outputs is proposed. 2) Compared with the classic Cascaded H-bridge topology, each module in the proposed topology processes three-phase real power, reducing the number of power devices and dc capacitance; only one dc source is needed at the input of the proposed multilevel converter and the front-end rectifier design is simplified. 3) Compared with classic Neutral Point Clamped and Flying Capacitor topologies, no clamping diodes or clamping capacitors are required for the proposed topology; the proposed topology is modular and scalable, has even switch stresses, and can achieve more output voltage levels up to the number of machine slots. 4) In the proposed topology, the machine winding insulators only support the line-line voltage of each module, significantly reducing the insulation requirement. This also reduces the total copper for windings allowing smaller machine design. 5) Compared with classic multilevel converters, the proposed topology has improved fault tolerance for the machine and converter. 6) In the proposed topology, interleaving technologies are introduced to reduce the current or voltage ripple or the necessary size of dc capacitors, and an active virtual resistor technique is employed to balance the dc capacitor voltages without power loss.

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