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Electro-Thermal Simulation of a Three Phase Inverter with Cooling System♠

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Abstract—Power modules including IGBTs are widely used in the applications of motor drivers. The thermal behavior of these modules becomes more important to choose the optimum design of cooling system. In this paper, a RC thermal model enabling the calculation of the chip temperature of an IGBT module operating as a component of a frequency converter is presented. This model is used to estimate the maximum junction temperature of the module. A water cooling systems is used for the thermal protection of IGBTs. The electro-thermal model with cooling system is implemented and simulated with MATLAB simulator.

Keywords: Thermal model, IGBT, Cooling system, Inverter.

1. INTRODUCTION

The importance of reliability and lifetime of the integrated gate bipolar transistors (IGBT) modules has continuously increased due to the huge use in the field of traction applications. Today's the integrated IGBT can generate from 1 to 3 W/mm^2 of waste heat at the die level. With adequate cooling, heat fluxes of over 4 W/ mm^2 are possible (Wen et al.). Air cooling offers many benefits not for its low cost but also for its simplicity implementation. However, in order to achieve the required cooling, it is forced to increase heat sink airflow and consequently the use of larger heat sinks (Geng et al.). With heat fluxes of over 5 W/mm^2, forced liquid cooling is applied. The use of liquid cooling gives more advantages than air-cooling like higher specific heat capacity, density, and thermal conductivity (Schmidt et al.). The liquid cooling system is consisted of a pump, cold plates connected with the heat generation, and connections tubes.

In this paper, we present first a RC thermal model for electro-thermal simulation for an inverter module. The model takes into account the thermal influence between the different components. This simulation can predict the dynamic thermal behavior of an inverter device. A water cooling system is studied and implemented in MATLAB simulator.

2. ESTIMATION OF THE HOT SPOT TEMPERATURE IN THE IGBT

The studied module is the Semikron module SKM 75GB 123D (75A/1200V) which contains two IGBTs and two Diodes in antiparallels. The structure of the module contains primarily eight layers of different materials, each one of it is characterized by its thickness Li, its thermal conductivity Ki, density ρi and its heat capacity ρCpi. Table 1 shows the materials properties of the various layers of module as shown in Fig. 1. These values are given by the manufacturer and/or of the literatures (Dorkel et al., Khatir et al., Thomas et al., Masana et al., Cite web).

Table 1. Thermal parameters of a power module

Material	L (mm)	K (W/mK)	ρCp J/Kcm^3)
Silicon	0.5	140	1.7
Solder 1	0.053	35	1.3
Copper	0.35	360	3.5
Isolation	0.636	100	2.3
Copper	0.35	360	3.5
Solder 2	0.103	35	1.3
Base plate	3	280	3.6
Grease	0.1	1	2.1

♠ Sponsor and financial support acknowledgment goes here. Paper titles should be written in uppercase and lowercase letters, not all uppercase.

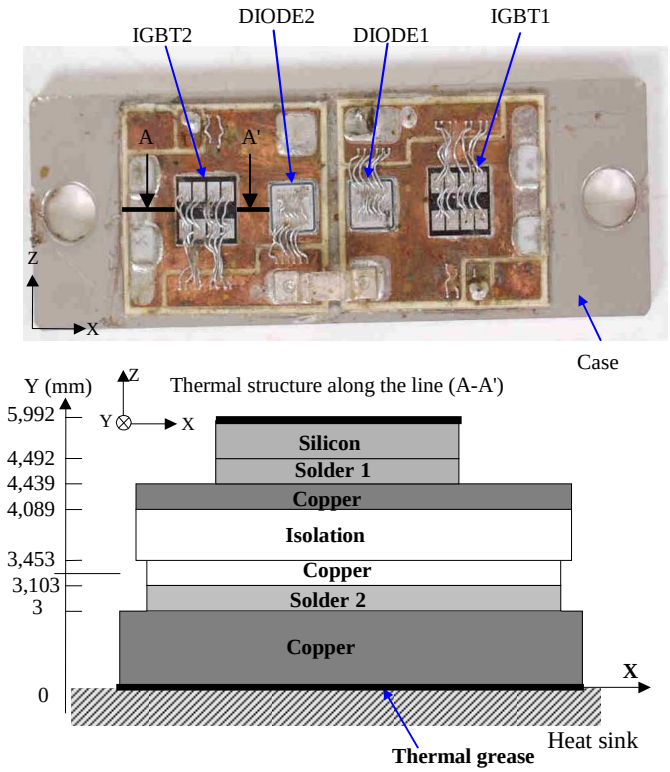


Fig. 1. Geometrical description of the studied IGBT module.

2.1 Experimental setup

The experimental estimation of the hottest area temperature inside an IGBT is based on suitable and measurable parameters. The hottest area that leads to the device destruction is located at the end of the channel region, where the current density is high.

Literature proposes the threshold voltage V_{th} as a parameter depending on the channel temperature. The measurement of the latter parameter is performed after a self-heating phase (by power losses inside the device) due to a non destructive short circuit. One mean problem of this technique is the small dependence on temperature, i.e., a small range of variation. Moreover, the measurement of V_{th} implies a fine control of the voltage V_{GS} in order to insure a low current density inside the device during the cooling phase.

Another method for the estimation of the channel temperature during a device self-heating phase is the measurement of the saturation current for a high gate-to-source voltage value. The results are not unique since they depend on circuit parameters, and the temperature calibration of the saturation current may not be performed without power losses that participate to the device self-heating.

2.2 Used method

It is considered to measure the saturation current during a cooling phase of the device, but for a low voltage V_{GS} (slightly larger than V_{th} at room temperature). These measurement methods are based on temperature calibration of saturation current I_{sat} without including self-heating in the device.

Fig. 4 shows the measurement setup for thermosensitive parameter I_{sat}. A heated flow generator controls the device temperature and the temperature in the IGBT is supposed to be homogeneous.

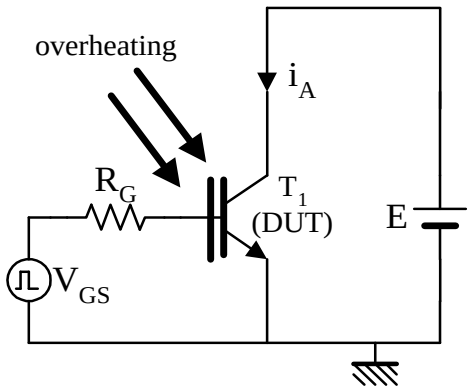


Fig. 2. Experimental circuit used for thermosensitive parameter calibration.

Fig. 3 shows the experimental temperature calibration curve for : $I_{sat} = i_A$ (E = 15V, V_{GS} = 6.2V). The device under test T_1 is submitted to a non-destructive short-circuit in order to induce an important channel temperature variation during a short time without inducing an elevation of the case temperature. The current I_{sat} is measured during the cooling phase that corresponds to the same heat generation.

Fig. 4 shows the experimental circuit used for the measurement of I_{sat} response. V_e and V_{in} (Fig. 5) are the driving signal of the device under test device under test (T_1) and the transistors T_2 driving signals, respectively. Until time t_1, the IGBT under (T_1) is short circuited to the 250V power supply. Thus, it is the place of a high saturation current in T_1. Transistor T_2 works in the linear region and is calibrated larger than T_1. For the I_{sat} measurement at $t = t_1$, T_1 is biased in the saturation region with a low V_{GS} (V_{GS} = 6.2V). It is then a cooling phase for the IGBT T_1, and the saturation current measurement is performed.

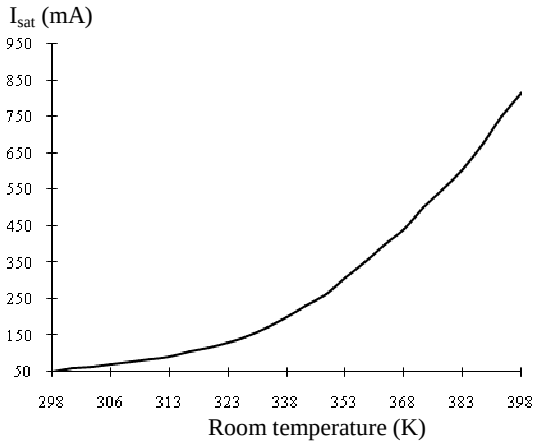


Fig. 3. Experimental calibration curve of saturation current (I_{sat}).

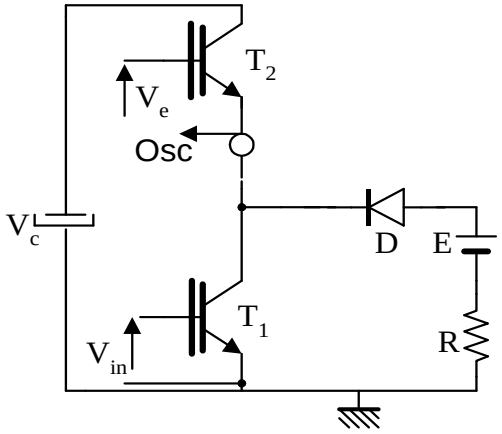


Fig. 4. Experimental circuit used for the measurement of the saturation current response during cooling phases.

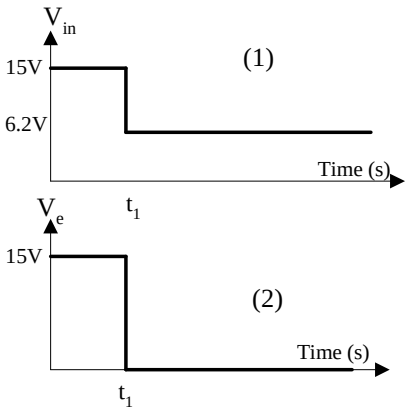


Fig. 5. Input waveforms for T_1 (1) and T_2 (2) switches used in the experimental circuit of Fig. 4.

Fig. 6 shows the evolution of the thermosensitive parameter (I_{sat}) versus time. From calibration characterization (Fig. 3) and I_{sat} response during cooling phase (Fig. 6) we can deduce the channel temperature (T_j) response after short circuit (Fig. 7).

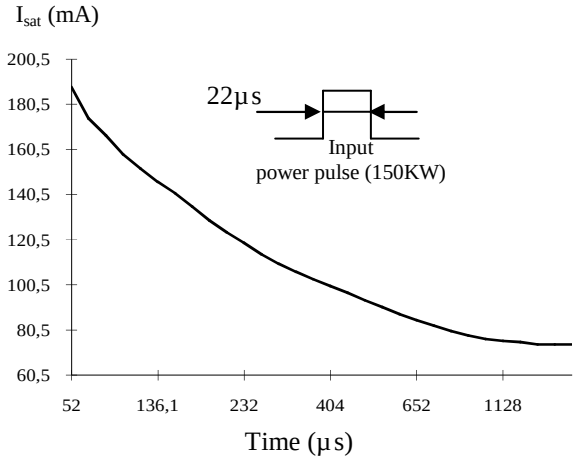


Fig. 6. Saturation current evolution during a cooling phase of the module.

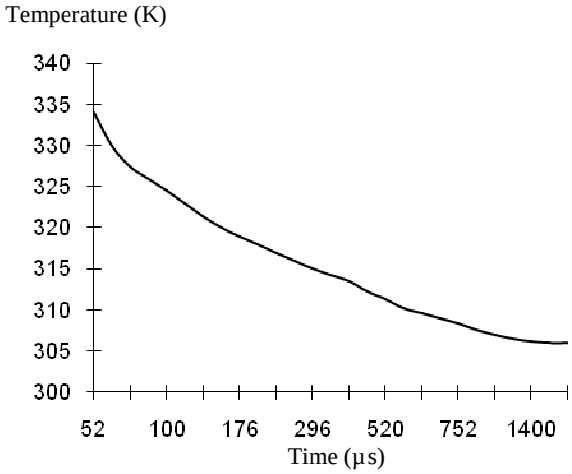


Fig. 7. Estimated temperature evolution during cooling phase.

2.3 Hot spot temperature evolution

In the case of a vertical power device, where the thickness L of the chip is small compared to other dimensions, heat is generated at the top surface of silicon and flows linearly along the axe perpendicular to the area (A). So, a one-dimensional (1D) heat flow may be considered (at the top of the structure).

Because most of the semiconductor device models are implemented in circuit simulators, thermal circuit networks are the practical models for electrothermal simulations. Literature proposes some approaches to construct thermal networks equivalent to a discretization of the heat equation. For example the finite difference method (FDM) and the finite element method (FEM) are proposed. In the case of vertical power devices, where the thickness L is small compared to other dimensions, it is commonly considered that heat is generated at the top surface of silicon and flows uniformly along the x-axis (perpendicular to the silicon surface). So, the top surface is considered to be a geometrical boundary of the device at x = 0, where the input power P is assumed to be uniformly dissipated. In our case we have chosen the (FEM) technique to develop the thermal model of the hybrid structure. Each material is represented by a simplified 1D thermal model. For the isolation and baseplate layer a modification have been introduced on the 1D model to take into account the thermal mutual between the different components. The thermal model of the silicon material can be represented by the equivalent electrical circuit (Trzer et al., Ammous et al.) shown in Fig. 8.

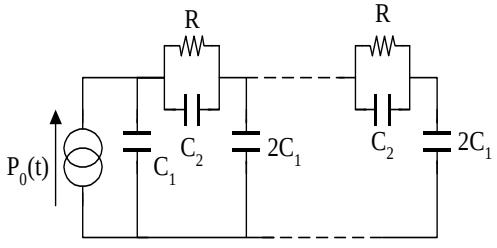


Fig. 8. The thermal model of the silicon material.

The thermal model is implemented in the MATLAB simulator. In order to estimate the channel temperature in the IGBT an identification procedure is used and so the effective thickness L and area A of the top material of the IGBT chip are deduced (Fig. 9 and Fig. 10).

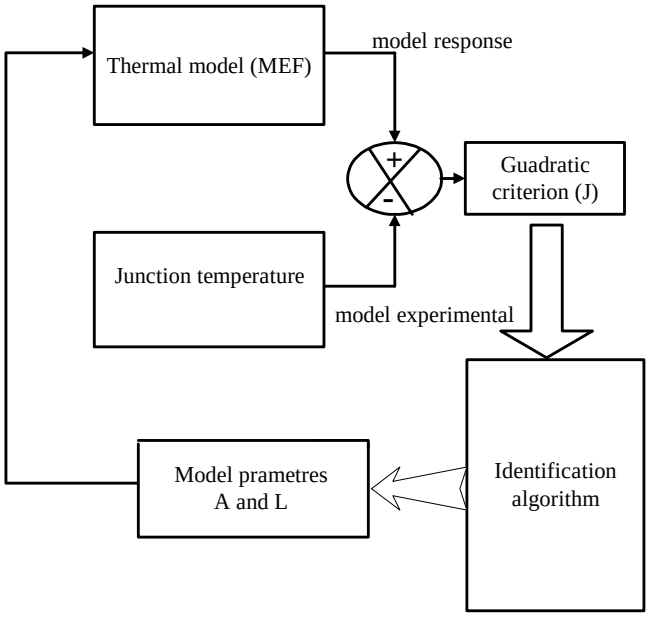


Fig. 9. Diagram showing the identification procedure

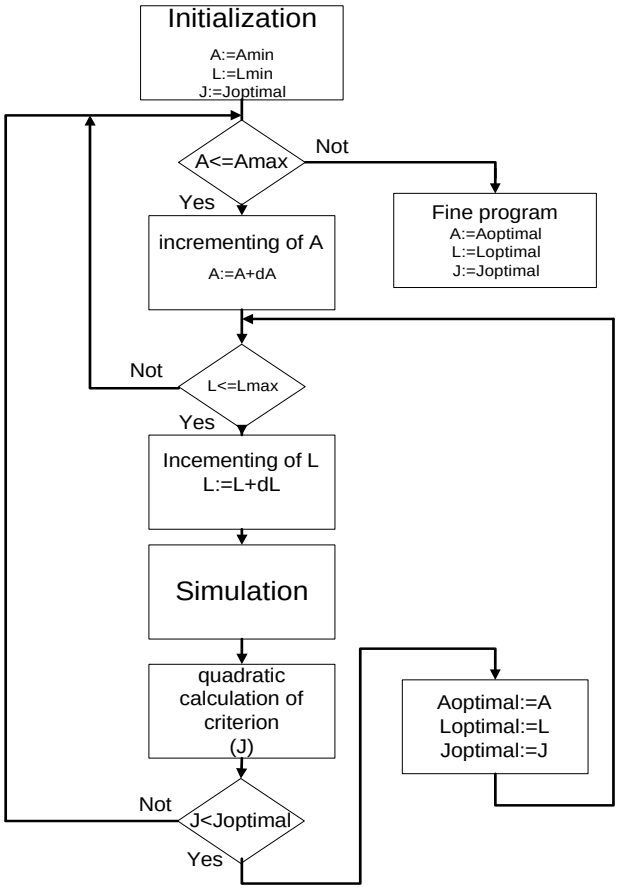


Fig. 10. Identification procedure of the thickness L and the area A.

The used technique leads a minimization of a quadratic error criterion J which is obtained by comparison between the experimental results and the simulation results (Fig. 11).

$$J(p)=\left[\frac{1}{t_2-t_1}\int_{t_1}^{t_2}\left(T_{ch\,0(P)}-\tilde{T}_{ch\,0}\right)^2 dt\right]^{\frac{1}{2}} \quad (1)$$

Where t_1 and t_2 are the boundary times of the experimental estimated temperature curve (t_1=52µs and t_2= 1780µs). The relaxation strategy with inequality constraints has been applied for model parameter identifications.

The obtained values of the thickness L and the area A of the IGBT are 0.05cm and 1cm^2 respectively. During short circuit the dissipated power is very high in the top surface of the device (silicon chip). Because short circuit duration is very small (22µs), channel temperature evolution don't depend on device thickness. In fact, temperatures inside and in the bottom of the device don't vary significantly. So, the identified area (A) and thickness (L) corresponds to an approximated parameters value of the active part of the device during and after the short circuit condition.

In the same way for the DIODE, the obtained values of the thickness L and the area A of are 0.05cm and 0.46cm^2 respectively.

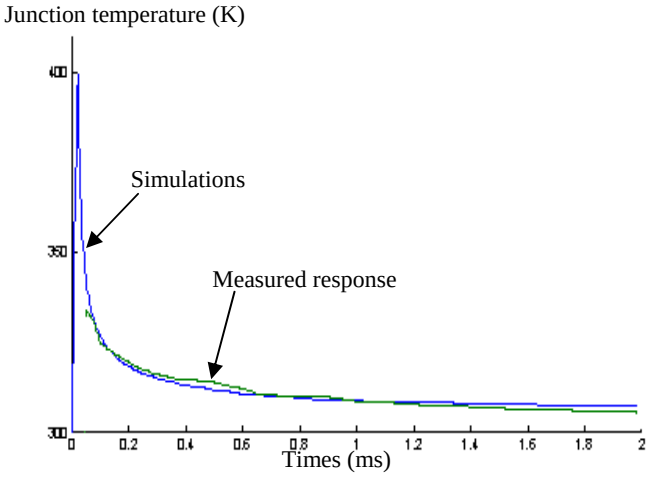


Fig. 11. Equivalent thermal circuit responses. (A=1cm^2; L = 0.05cm).

2.4 Experimental estimation of the thermal resistance of the IGBT

In order to estimate the thermal resistance of the IGBT, the electrical circuit of Fig. 12 is used. In fact, a gate-to-source voltage step is applied to the device and so a power step is dissipated on it. In this experience the bottom surface of the module is not fixed to a heat sink and the case temperature is measured by a ″thermal sensor″. In steady state condition a low gate-to-source voltage value (slightly larger than the threshold voltage V_{th}) is applied on the device during a small time (some microsecond) in order to measure the saturation current I_{sat} in the device. Using calibration characteristic

evolution shown in Fig. 3, the junction temperature in the IGBT is deduced.

The thermal resistance is given by

$$R_{th} = \frac{T_j - T_c}{P} \quad (2)$$

Where

T_j: Junction temperature (°C)

T_c: Case temperature (°C)

P: Power dissipated (W)

For P = 15W , T_j = 104°C and T_c = 100°C. The thermal resistance of the IGBT is equal to R_{th} = 0.266 °C/W. This value is in good agreement with the value deduced from manufacturer data sheet (0.27 °C/W). The obtained results show the accuracy of the proposed technique to estimate the channel temperature in the IGBT.

For P = 11,5W , T_j = 107°C and T_c = 100°C. The thermal resistance of the DIODE is equal to R_{th} = 0.598 °C/W. This value is in good agreement with the value deduced from manufacturer data sheet (0.6 °C/W). The obtained results show the accuracy of the proposed technique to estimate the channel temperature in the DIODE.

3. ELECTROTHERMAL MODEL OF IGBT

3.1 Electrical model of IGBT

The electric model used for IGBT is the model implemented in the Sim-Power library of MATLAB (V7.0). In its linear zone, the static characteristics of the IGBT can be modeled by a line of slope $1/R_0$ and X-coordinate in the V_0 threshold. We can, then, express the voltage drop at the boundaries of the IGBT in the linear zone by:

$$V_{ce}=V_0+R_0I_c \quad (3)$$

V_0 and R_0 can be expressed by the following equations:

$$V_0=V_{00}+a\ T_{j(IGBT)} \quad (4)$$

$$R_0=R_{00}+b\ T_{j(IGBT)} \quad (5)$$

Where V_{00} represents the voltage threshold at 0°C; R_{00} is the resistance at 0°C; a and b are the sensitivity coefficients of the temperature and $T_{j\ (IGBT)}$ is the junction temperature of the IGBT in °C.

Fig. 12 shows the static characteristics of the IGBT at various temperatures experimentally obtained. As Fig. 12 illustrates, the resistance R_0 and the voltage V_0 can be approximated by the following simple polynomial function:

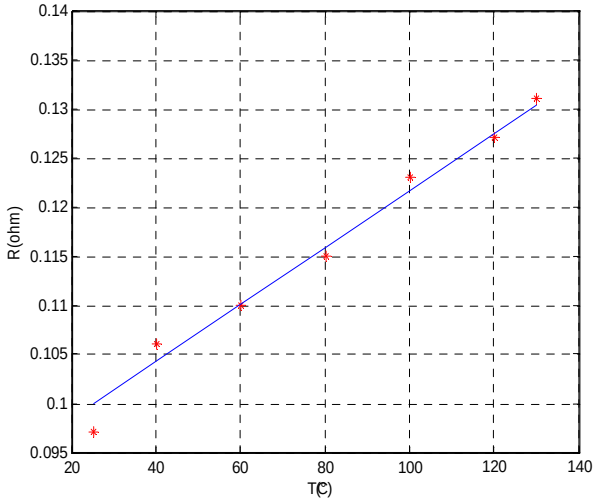
$$V_0=0{,}5-3.10^{-3}T_{j(IGBT)} \quad (6)$$

$$R_0=9.10^{-2}-3.10^{-4}T_{j(IGBT)} \quad (7)$$

3.2 Thermal model of IGBT

At power feeding into the chip the heating flow spreads out vertically to the module base plate and also laterally from the heating source. So, a mutual coupling of the different chip happens inside the module. This thermal interaction depends mainly on (Krummer et al.):

- The number of the devices under test.
- The boundary condition at the heat spreader.
- The dissipated power value in the different components.



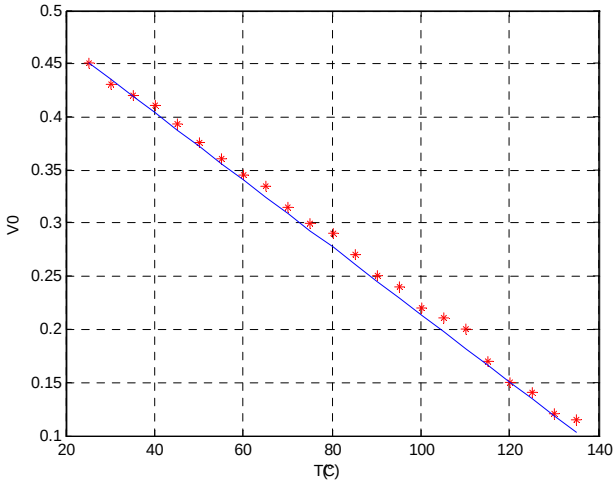


Fig. 12. Static characteristics of the IGBT obtained by experiments at various temperatures

The variations of side thermal resistances of influence, between the IGBT1 (for example) and the other components of the structure, according to the power dissipated in the IGBT, were traced on the Fig. 13.

The thermal resistance of coupling between the two IGBT for example is given by the following expression.

$$R_{IGBT1\text{-}IGBT2} = (T_{IGBT1}\text{-}T_{IGBT2})/P_{IGBT1} \quad (8)$$

The variations of side thermal resistances of influence, between the DIODE1 (for example) and the other components of the structure, according to equivalent thermal resistance between the case and the ambient air, were traced on the Fig. 14.

We notice that these thermal resistances of influences are a function of the amplitudes of the powers dissipated and the limiting conditions on the case of the module. Thus a study of the phenomenon of thermal mutual influence companies in the multichip structures cannot be carried out without the catch in consideration of these two parameters.

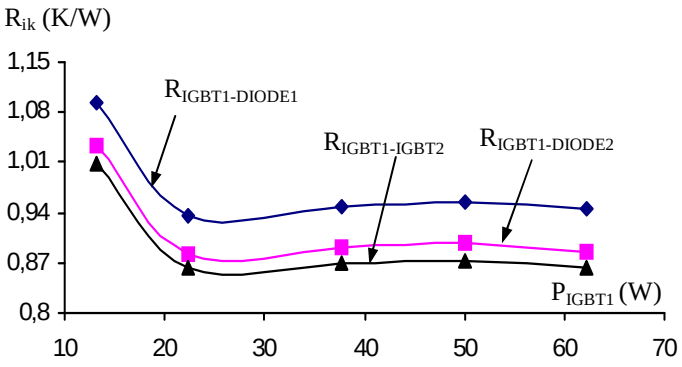


Fig. 13. Variation of the resistance of coupling according to the power dissipated in the IGBT1 ($R_{rad\text{-}IGBT1}$=1 K/W)

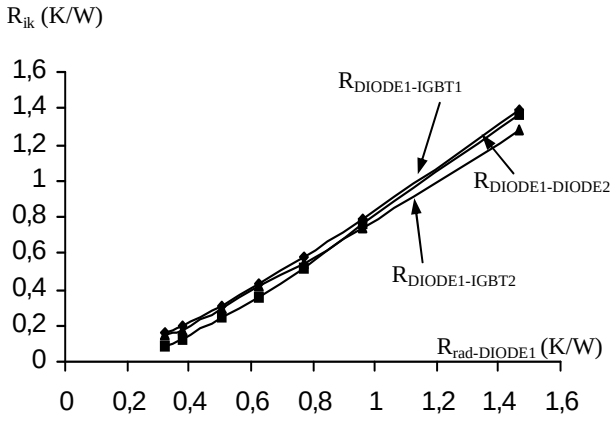


Fig. 14. Variation of the resistance of coupling according to the boundary conditions on the DIODE1 (P_{DIODE1}=37W)

The superposition technique is used to develop the simplified thermal model of the hybrid structure.

The used IGBT thermal model order is equal to 19 (10 for silicon, 3 for copper, 3 for isolation and 3 for base-plate) (Ayadi et al.).

4. COOLING SYSTEM

As cooling system for IGBT module we used a cold plate, whose channel design is critical to the thermal dissipation of the total system. In our study a linear type cold plate was employed. The structure of the water-cooling IGBT module is shown in Fig. 15.

For the tested IGBT modules, the maximum junction temperature was set by the manufacturer to 150 °C. So, for the IGBT thermal safety we fixed at 120°C the maximum junction temperature. The setting of temperature is ensured by the fluid flow in the cold plate (Hetsroni et al., Schmit et al., Chu et al.).

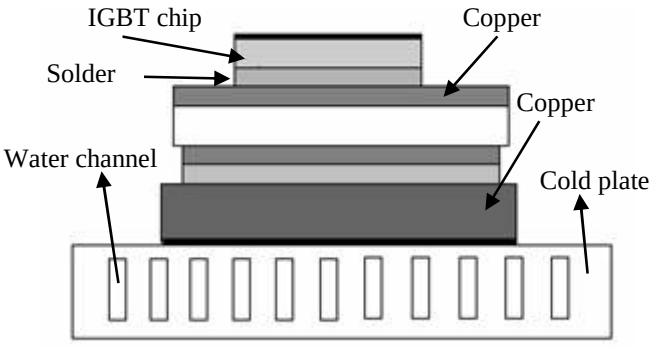


Fig. 15. Structure of IGBT module with cooling system

5. SIMULATIONS AND RESULTAS

For simulation, a three phase PWM inverter module was used. The inverter is coupled with a three phase motor. For the IGBT thermal module the ambient temperature is fixed at 33°C. Both the electro-thermal model of IGBT module and the water cooling system are implemented in MATLAB/simulink . Fig. 16 shows the circuit implemented and simulated in the MATLAB simulator

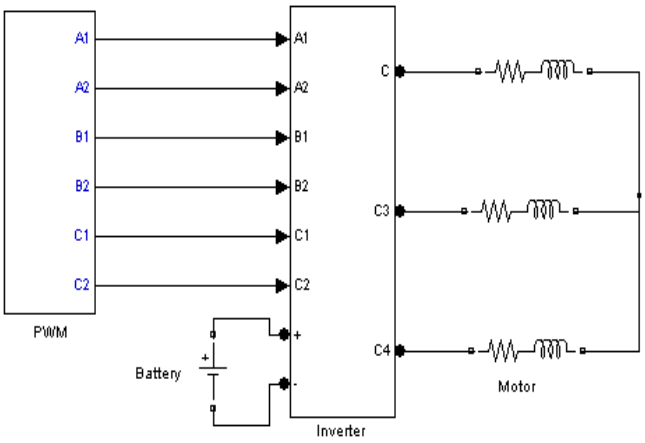


Fig. 16. Circuit used in simulation

From this simulation, the temperature of each part of IGBT module can be deduced. At t=1,1s an overload has been

applied until t=1.6s. The IGBT power loss is shown in Fig. 17.

Fig. 18 and Fig. 19 show respectively the IGBT junction temperature and the base plate temperature with and without cooling system. In our study we set the battery voltage at 120 V, the modulation index at 0.8, a modulation frequency at 100Hz, power factor at 0.8 and a switching frequency at 8 kHz.

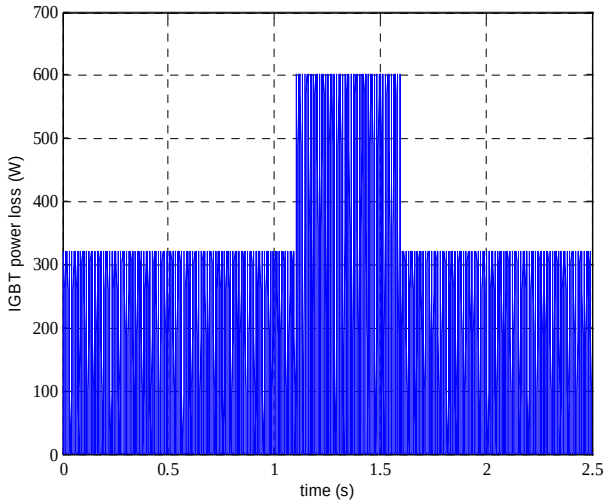


Fig. 17. Evolution of the base plate temperature (in the IGBT) (Operation inverter).

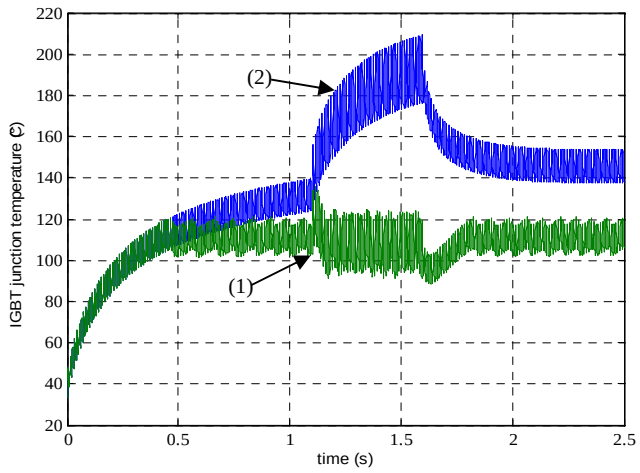


Fig. 18. Evolution of the junction temperature (in the IGBT) (Operation inverter; (1): with cooling system; (2): without cooling system).

6. CONCLUSION

A thermal investigation of a three phase inverter has been achieved. A simplified 1D thermal model has been used. This model takes into account the thermal influence between the different module chips based on the technique of superposition. A water cooling system has been developed. This system takes into account the junction temperature of IGBT to not exceed 120°C fixed by the book qualifications.

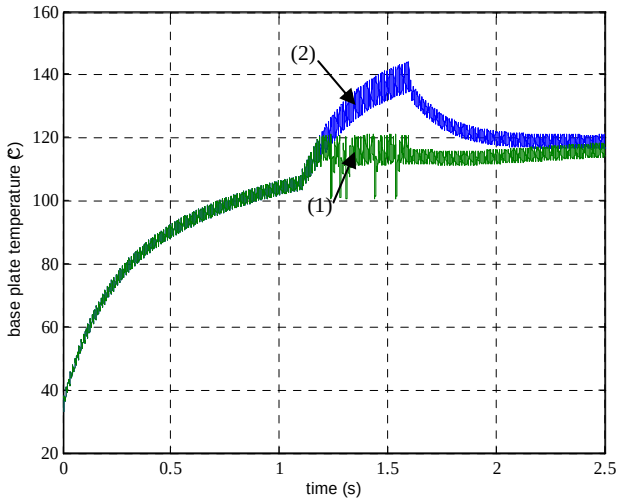


Fig. 19. Evolution of the base plate temperature (in the IGBT) (Operation inverter; (1): with cooling system; (2): without cooling system)

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