Homework 01

Due on March 17 12:00pm

1. Verilog simulation with NCVerilog and nWave:
   a. Modify the Verilog code of the majority circuit.
   b. Design a Verilog module to realize the following logic function:

$$f(x, y) = (x \vee y) \wedge \overline{(x \wedge y)}.$$

   c. Write a testbench to verify the operation of your design on all four combinations of x and y.
   d. What function does this circuit realize?
   e. Write a short report of a paragraph or two to summarize whether or not you encounter problems, and how you solve them. Also attach the simulation result and a screenshot of the waveform.

   Note: submit the source code and the electrical report based on TA's instructions.