Homework 04: Verilog Assignment

Due on April 14 11:59pm

1. Write a Verilog design for a circuit whose output is true if its four-bit decimal input is multiple-of-3. That is, the output is true if the input is 3, 6, or 9, where the input is between 0 to 9.
   a. The output is a don't care if the input is not between 0 to 9.
   b. Use Verilog `case` to implement the design.
   c. Also write a Verilog testbench to verify your design.
2. Write a Verilog design for a four-bit adder that adds two four-bit inputs, *A* and *B*, and a carry-in, producing the four-bit sum and carry-out.
   a. Design a single-bit full adder first. Then use four full adders to implement the four-bit adder.
   b. Write the full adder by using behavior description with Verilog `always` statement and arithmetic operator "+".
   c. How many test patterns do you need if you want to test the four-bit adder exhaustively? If the number of test patterns is limited, say, to 30 patterns, how do you pick them to test your design properly? Write a Verilog testbench to verify the adder with 30 test patterns. Explain your choice of patterns in the report.

Write a short report of a paragraph or two to summarize whether or not you encounter problems, and how you solve them. Also attach the simulation result and a screenshot of the waveform, for each Verilog design.

Note: submit the source code and the electrical report based on TA's instructions.