Homework 07: Verilog Assignment

Due on May 30 11:59pm

1. Write the Mealy model of FSM ***k*** (page 15 of Lecture 09 Finite State Machines and The Verilog Style) in Verilog HDL, with the template of design and stimulus given.
   a. Are the test patterns in the template enough to verify the FSM?
   b. Compare with the Moore model of Coding Example 2 (module `fsm2` in page 17), which is done in the template.
   Also note that we declare input/output and reg/wire at the same time when defining the port list, which is an elegant design style.
   Can you make your Mealy model behave the same as the Moore version cycle by cycle?
   c. Take a look at the template. We put the checking mechanism for you. The simulation will display "PASSED" if the two machines produces the same outputs, and "FAILED" when there is any mismatch. Can you explain what the signals `error` and `error_count` do in the Verilog template?
2. Write a Verilog design of GCD based on the specification in hw07-2_gcd.pdf.
   a. Add at least 4 more test patterns to test the GCD computation. Is it enough? If not, add more patterns.
   b. Try to learn the way we use shell script and Makefile.
   c. Optional: Can you improve the timing for consecutive GCD operations?

For each Verilog assignment, you should also design your own test patterns to verify the correctness, and write a short report of a paragraph or two to address any the followings:

a. Your design idea, whether or not you encounter problems, and how you solve them.
b. How you verify the design with the test patterns you used, and the reason you think the design is complete and correct. Also attach the simulation result, and a screenshot of the waveform result.
c. Any valuable discussion.

Note: Submit the source code and the electrical report based on TA's instructions. Otherwise you may fail to get the score.