Homework 05: Verilog Assignment

Due on May 5 11:59pm

1. Write a Verilog design for a 6:64 ***decoder*** by using smaller 3:8 decoders as the pre-decoding stage. Draw the logic diagram as well and explain how you can do it. Use behavioral description to design the 3:8 decoder as the basic block.
2. Write a Verilog design for a ***binary priority encoder*** with programmable priority. Assume the input data (**in**) is an 8-bit input vector. The priority selection (**pri**) is a 3-bit binary number to indicate the position of the highest priority. The priority rotates rightward from that bit position if the value is zero at the assigned position. Finally, the output (**out**) is a 3-bit binary number to indicate the actual bit position with the first priority. Add a 1-bit output "**zero**" to indicate if the input is zero or not (that is, zero=1 if in==0). Use behavioral (high-level) description when possible.
3. Try to use two 8-bit binary priority encoders in Problem (2) to form a larger 16-bit binary priority encoder. You may add additional logic (in behavioral way) outside the two blocks. (There can be different solutions. Try to have an elegant one.)

For each Verilog assignment, you should also design your own test patterns to verify the correctness, and write a short report of a paragraph or two to address any the followings:

a. Your design idea, whether or not you encounter problems, and how you solve them.
b. How you verify the design with the test patterns you used, and the reason you think the design is complete and correct. Also attach the simulation result, and a screenshot of the waveform result.
c. Any valuable discussion.

Note: Submit the source code and the electrical report based on TA's instructions. Otherwise you may fail to get the score.