Real-Time DSP Design & Applications

Assignment 2

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My matriculation number is G2203629G, so $d_0 = 9, d_1 = 2, d_2 = 6, d_3 = 3, d_4 = 0, d_5 = 2, d_6 = 2, A = G, B = G$

Q1

(i)

delay to compute $s_n = d_1 + c_{n-1}$ ns

delay to compute $c_n = d_0 + d_1 + c_{n-1}$ ns

If all adders are connected in sequence:

delay to compute $s_n = 11n + 2$ ns

delay to compute $c_n = (n + 1)(d_0 + d_1) = 11n + 11$ ns

(ii)

Delays are shown in the following figure.

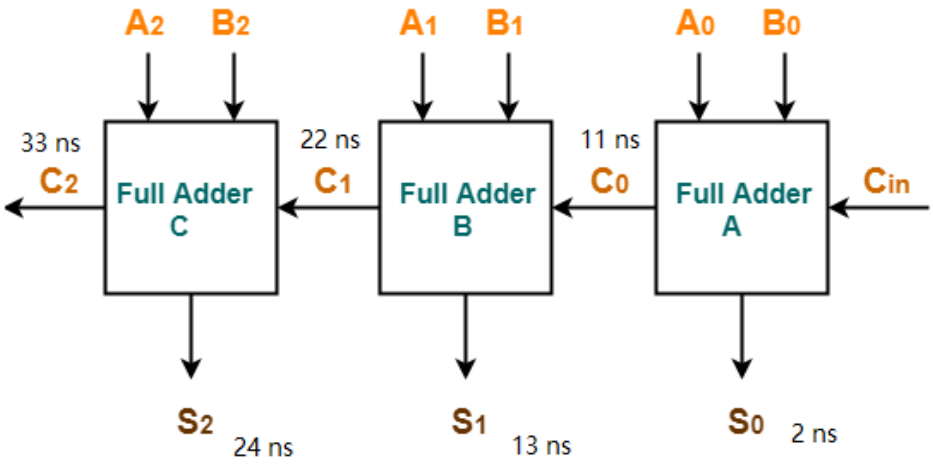

Figure 1: 3 bit Ripple Carry Adder

(iii)

delay to compute the carry bit of last full adder $= 11N$ ns

delay to compute the sum bit of last full adder $= 11(N-1)+2 = 11N-9$ ns

so, maximum delay $= 11N$ ns

Q2

(i)

$y(n) = \frac{2}{3}x(n) - \frac{5}{12}y(n-1)$

$y(n-1) = \frac{2}{3}x(n-1) - \frac{5}{12}y(n-2)$

$y(n) = \frac{2}{3}x(n) - \frac{10}{36}x(n-1) + \frac{25}{144}y(n-2)$

(ii)

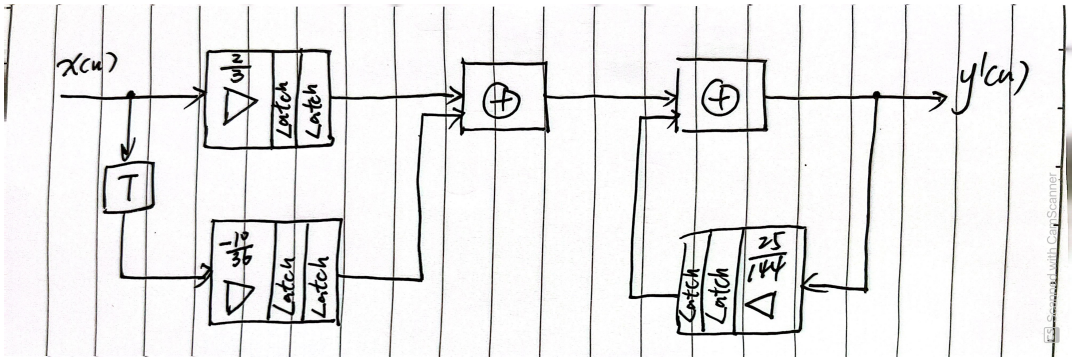

Figure 2: Pipelined Structure

$y'(n) = \frac{2}{3}x(n-2) - \frac{10}{36}x(n-3) + \frac{25}{144}y'(n-2)$

$y(n-2) = \frac{2}{3}x(n-2) - \frac{10}{36}x(n-3) + \frac{25}{144}y(n-4)$

$\text{output} = y'(n) = y(n-2)$

Q3

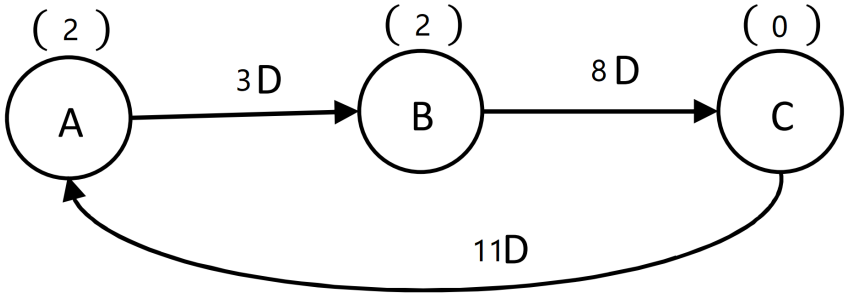

Figure 3: Data Flow Graph

(i)

Iteration bound = maximum loop bound

$$= \frac{\text{loop computation time}}{\text{no of delays in the loop}} = \frac{4}{22} = \frac{2}{11}$$

(ii)

$J = 2$

For $A_i \rightarrow B_{(i+3)\%2} = \lfloor \frac{i+m}{J} \rfloor = \lfloor \frac{i+3}{2} \rfloor = \begin{cases} 1 & i = 0 \\ 2 & i = 1 \end{cases}$

For $B_i \rightarrow C_{(i+8)\%2} = \lfloor \frac{i+m}{J} \rfloor = \lfloor \frac{i+8}{2} \rfloor = 4$

For $C_i \rightarrow A_{(i+11)\%2} = \lfloor \frac{i+m}{J} \rfloor = \lfloor \frac{i+11}{2} \rfloor = \begin{cases} 5 & i = 0 \\ 6 & i = 1 \end{cases}$

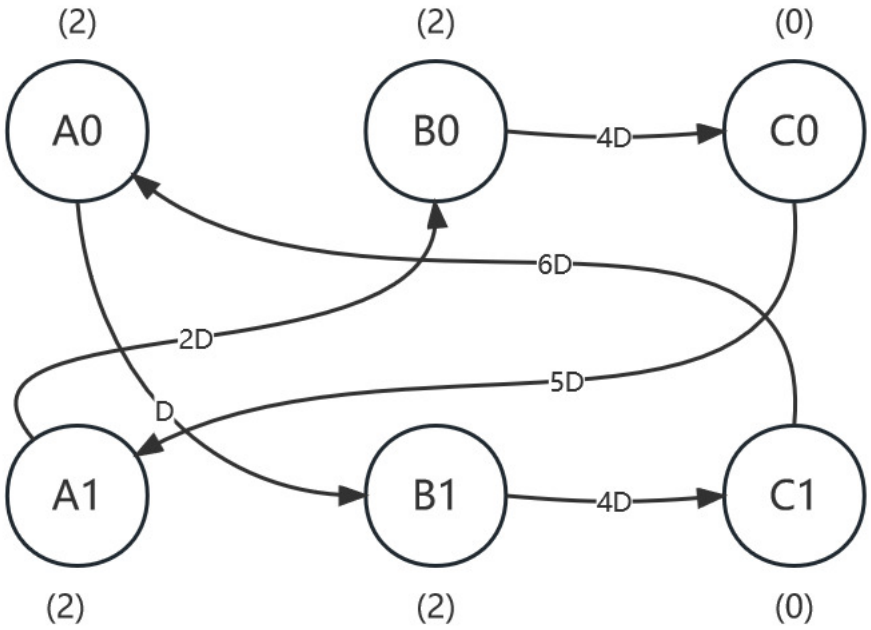

Figure 4: Unfolding Data Flow Graph

(iii)

Iteration bound = $JT_\infty = \frac{4}{11}$