

NANYANG TECHNOLOGICAL UNIVERSITY**SEMESTER 2 EXAMINATION 2021-2022****EE6402 – REAL-TIME DSP DESIGN AND APPLICATIONS**

April / May 2022

Time Allowed: 3 hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 4 pages.
 2. Answer all 5 questions.
 3. All questions carry equal marks.
 4. This is a closed book examination.
 5. Unless specifically stated, all symbols have their usual meanings.
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1. (a) Let $a = (3.75)_{10}$ be a decimal number.
 - (i) Express a in fixed point Q3.3 format. What is the largest (positive) number in Q3.3 format? What is the minimum possible (negative) number in Q3.3 format?
 - (ii) Express a in IEEE 754 single-precision floating point format $[S, Exp, D]$, where you may use either decimal or binary to express S, Exp , and D . What is the largest normalized number in IEEE 754 single precision format?

(10 Marks)
- (b) The input to a cascaded system has input noise $e(n)$ as a result of quantization with quantization step size Q . This input is filtered through a low pass filter with frequency response $|H(e^{j\omega})| = \begin{cases} 1 & 0 \leq \omega \leq 3\pi/4 \\ 0 & 3\pi/4 < \omega \leq \pi \end{cases}$, resulting in the first output noise $v(n)$. The first output is again filtered through a high pass filter with frequency response $|G(e^{j\omega})| = \begin{cases} 0 & 0 \leq \omega < \pi/2 \\ 1 & \pi/2 \leq \omega \leq \pi \end{cases}$, resulting in the second output noise $w(n)$. The output noises $v(n)$ and $w(n)$ are entirely due to the input noise (in this model, assume there is no rounding or truncation error in both filters).

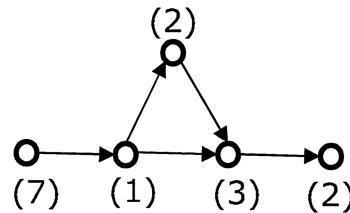
Note: Question No. 1 continues on page 2.

- (i) If truncation is used for input quantization, find the mean η_v and the variance σ_v^2 of the first output noise $v(n)$.
- (ii) If truncation is used for input quantization, find the mean η_w , and the variance σ_w^2 of the second output noise $w(n)$.
- (iii) If rounding is used for input quantization, find and sketch the power spectral densities $S_v(e^{j\omega})$ and $S_w(e^{j\omega})$ of the first and second output noises $v(n)$ and $w(n)$.
- (10 Marks)
2. (a) An analog signal $x_c(t)$ has some probability density function (pdf) from $-1V$ to $1V$, such that the mean for this pdf is 0 , and the variance is $\frac{1}{6}$.
- (i) $x_c(t)$ has to be digitized at its Nyquist sampling rate by an n -bit ADC (Analog to Digital Converter), such that the signal to quantization noise ratio (SQNR) is at least 23 dB. Find the minimum possible (integer) value of n .
- (ii) If $x_c(t)$ is instead oversampled by twice the Nyquist sampling rate, find the minimum possible (integer) value of n to obtain an SQNR of at least 23 dB. (You may assume that an appropriate lowpass filter is used after the ADC.)
- (8 Marks)
- (b) In each of the following requirements, choose the most appropriate ADC.
- (i) Low speed, high resolution, cost sensitive
- (ii) Low speed, high resolution, insensitive to ageing
- (iii) High speed, low resolution
- (6 Marks)
- (c) Explain the operation of a ladder DAC (digital to analog converter) in detail. What, if any, is the disadvantage of the ladder DAC?
- (6 Marks)

3. (a) Consider a full adder with two input bits a_n, b_n , an input carry bit c_{n-1} , an output sum bit s_n , and an output carry bit c_n . While s_n is computed 1 ns after all three inputs a_n, b_n, c_{n-1} are presented, c_n is computed 2 ns after all three inputs a_n, b_n, c_{n-1} are presented.
- (i) Draw a diagram of a 3-bit ripple carry adder using the above full adder.

Note: Question No. 3 continues on page 3.

- (ii) The input bits to this 3-bit ripple carry adder are not presented together. At time 0, two input bits c_{-1} and a_0 are presented to the adder. At 2 ns, two more input bits a_1 and b_0 are presented. At 4 ns, a_2 and b_1 become available. At 6 ns, b_2 is presented. Find the times when each of the output bits $s_0, s_1, s_2, c_0, c_1, c_2$ are computed by this 3-bit adder.
- (iii) For the scenario of part (ii) above, is there any way to reduce the carry propagation time?
- (11 Marks)
- (b) A data flow graph is shown in Figure 1. All nodes are labelled by their computation time. Since its critical path is too large, pipelining has to be used.

**Figure 1**

- (i) What is the critical path of this graph before pipelining?
- (ii) Draw all possible feed-forward cutsets for this graph. For each cutset, find the critical path after pipelining (by inserting latch/latches).
- (iii) From part (ii) above, choose the cutset to achieve the pipelining that results in the minimum critical path using the minimum number of latch/latches.
- (9 Marks)
4. (a) An FIR filter $y(n) = 0.8x(n) + 0.2x(n - 1)$ is implemented in a given hardware, which requires a clock cycle $T_c \geq 150\text{ns}$. This structure is not sufficient because the input signal to the filter is sampled at a sampling frequency $f_c = 10\text{MHz}$. Therefore, parallel processing has to be used.
- (i) Find the minimum block size L for the parallel structure of the filter, such that filtering the 10MHz sampled input may be achieved.
- (ii) For the L in part (i) above, draw the parallel structure of the above FIR filter. Clearly mark the inputs and the outputs. What is the maximum sampling frequency that is supported by your parallel structure?
- (iii) Your parallel structure with block size L should have $2L$ multipliers. Propose a low complexity parallel structure for this filter with the same block size that uses only 2 multipliers.
- (15 Marks)

Note: Question No. 4 continues on page 4.

- (b) Discuss the different aspects that should be considered while selecting a fixed point DSP processor versus a floating point DSP processor for some application.
- (5 Marks)
5. (a) In TMS320C55x assembly instruction **MOV** from a source to a destination, the number of bits moved may be different.
- (i) Give an example of a **MOV** that moves 40 bits.
 - (ii) Give an example of a **MOV** that moves 23 bits.
 - (iii) Give an example of a **MOV** that moves 16 bits.
 - (iv) Explain how the bits are moved in **MOV** when the source register has less bits than the destination register.

(8 Marks)

- (b) Some auxiliary registers (AR) and memory addresses in a TMS320C55x contain the following values:

XAR0	00_0100h
XAR1	00_0200h
XAR2	00_0300h
00_0100	0300h
00_0101	0301h
00_0102	0001h
00_0200	0100h
00_0201	0102h
00_0202	0002h
00_0300	0200h
00_0301	0003h

Using the operands rules for AR indirect addressing, find the values of **XAR0**, **XAR1** and **XAR2** after each of the following consecutive instructions:

```
MOV *AR0, AR1
MOV *AR1+, AR2
MOV *+AR2, AR0
```

(12 Marks)

END OF PAPER

EE6402 REAL-TIME DSP DESIGN & APPLICATIONS

Please read the following instructions carefully:

- 1. Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**
2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.
3. Please write your Matriculation Number on the front of the answer book.
4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.