NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 2 EXAMINATION 2020-2021

EE6402 – REAL-TIME DSP DESIGN AND APPLICATIONS

April / May 2021 Time Allowed: 3 hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 4 pages.
2. Answer all 5 questions.
3. All questions carry equal marks.
4. This is a closed book examination.
5. Unless specifically stated, all symbols have their usual meanings.

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1. (a) (i) Express $a = (1010.110)_{2's}$, a two's complement number, as a decimal number.

(ii) Express $b = (3)_{10}$ in the same format as a. Then add a and b in binary, and express the sum in the same format as a. Is there any overflow?

(iii) If b is subtracted from a in the same format, will there be any overflow?

(iv) Express a as a fixed-point number in the Q6.5 fixed point format.

(10 Marks)

(b) A signal x having a range of –5 volts to 5 volts, and variance $\sigma_x^2 = 3$, is quantized using a n-bit ADC (you may assume mid-rise quantizer) such that the signal to quantization noise ratio (SQNR) is at least 40 dB.

(i) Find the minimum possible n.

(ii) What is the SQNR and the quantization step size Q for your choice of n?

Note: Question No. 1 continues on page 2.

(iii) If a sinusoid $3\cos(200\pi t)$ is digitized using the above ADC, what will be the maximum possible amplitude of the signal after digitization?

(10 Marks)

2. (a) A continuous-time signal $x_c(t)$, whose spectrum is shown in Figure 1, consists of two frequencies, 500 Hz and 700 Hz.

Figure 1

(i) What is the Nyquist low-pass sampling frequency of $x_c(t)$?

(ii) If $x_c(t)$ is sampled at $f_s = 800$ Hz, will there be aliasing? Draw the spectrum of the sampled signal for $f_s = 800$ Hz.

(iii) After $x_c(t)$ is sampled at some sampling frequency of f_{s2} Hz, both frequencies of $x_c(t)$ map to the same frequency in the sampled signal. Find an example of such f_{s2}.

(10 Marks)

(b) Implement the FIR filter $y[n] = 4x[n] + 6x[n-1] + 10x[n-2] + 15x[n-3]$:

(i) Draw the conventional implementation using 4 multipliers and 3 adders.

(ii) Find an implementation using 4 multipliers and 2 adders. Does this implementation have any disadvantage compared to the conventional implementation?

(10 Marks)

3. (a) Consider a full adder with two input bits a_n, b_n, an input carry bit c_{n-1}, and an output carry bit c_n.

(i) Under what condition does the full adder generate a carry, that is, $c_n = 1$ regardless of c_{n-1}?

(ii) Under what condition does the full adder propagate a carry, that is, $c_n = c_{n-1}$?

Note: Question No. 3 continues on page 3.

(iii) Describe how the carry look-ahead adder (for individual bits) solves the problem of ripple carry of an adder.

(10 Marks)

(b) A camera has a maximum resolution of 3300 x 4200 pixels, and each pixel has 3 color components. The camera performs color demosaicing using a DSP processor. Demosaicing involves filtering each image with a 3 x 3 kernel, which requires 9 instructions per output pixel per color component. The time taken for demosaicing each image should not exceed 1 second. What is the minimum MIPS rating required for the DSP processor? In reality, there is always some overhead over and above the 3 x 3 filtering. If a 500 MIPS DSP processor is used, how many overhead instructions per output pixel per color component may be accommodated within the time of 1 second?

(6 Marks)

(c) TMS320C5515 DSP library function 'fir2' (FIR filtering) requires nx*(3+nh/2) core cycles, where nx is the number of input samples and nh is the number of coefficients of the filter. Normally, to compute each output sample of an FIR filter, we need nh operations. Explain how TMS320C5515 achieves nh/2 cycles instead.

(4 Marks)

4. (a) TMS320C5515 has four accumulators AC0-AC3. Each accumulator is how many bits long? Instead of accessing all these bits, some portions of these bits may be accessed individually. What are these portions called, and which bits are in each portion?

(7 Marks)

(b) Why is the anti-aliasing filter used before an ADC (analog to digital converter)? Explain if the anti-aliasing filter should be used or not for digitizing a band-limited signal.

(6 Marks)

(c) With the help of a block diagram, describe the operation of the counter ADC. What, if any, is the disadvantage of the counter ADC?

(7 Marks)

5. (a) Describe the multiple-line or multilevel interrupt system with the help of a diagram. What are the advantages of this interrupt system?

(7 Marks)

Note: Question No. 5 continues on page 4.

(b) The sequential system in Figure 2 is implemented where the multipliers have a delay of 26 ns and the adder has a delay of 5 ns. The sampling frequency of $x[n]$ is 50 MHz.

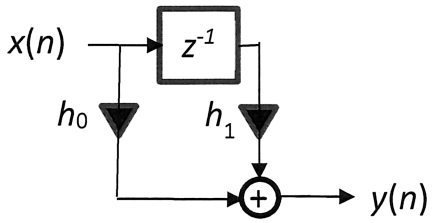

Figure 2

(i) Draw the data flow graph of Figure 2.

(ii) Is the sequential implementation adequate?

(iii) Design a parallel system to implement Figure 2. Find the minimum block size that achieves the above sampling frequency. Draw the architecture of the parallel system. What is the clock frequency of your implementation for the above sampling frequency?

(13 Marks)

END OF PAPER

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Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.