NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2019-2020

EE6402 – REAL-TIME DSP DESIGN AND APPLICATIONS

November / December 2019 Time Allowed: 3 hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 6 pages.
2. Answer all 5 questions.
3. All questions carry equal marks.
4. This is a closed book examination.

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1. (a) (i) In IEEE 754 single-precision (32 bit) floating point format, how many bits are used for the exponent? How many bits are used for the mantissa?

(ii) What is the dynamic range of IEEE 754 single-precision format?

(iii) Determine the decimal value of the following IEEE 754 single-precision (32 bit) floating point format (normalized) number, represented by three fields—sign, exponent, and mantissa—in that order.

0	$(133)_{10}$	$(0.5625)_{10}$

(iv) Add the above floating-point number to another floating-point number (in the same format) shown below. Show the intermediate steps, and express the sum in the same format.

0	$(131)_{10}$	$(0.25)_{10}$

(9 Marks)

Note : Question No. 1 continues on page 2.

(b) An input $x(n)$ passes through a length 100 FIR filter with frequency response

$$H(e^{j\omega}) = \begin{cases} 1, & \frac{\pi}{2} \leq |\omega| \leq \pi \\ 0, & otherwise \end{cases}$$

to give an output $y(n)$ (see Figure 1). The input $x(n)$ is rounded using a quantization step size of Q, which may be modelled as a noise injection $e_x(n)$ as shown in Figure 1. After each multiplication, each product is truncated to a word-length which is 5 bits longer than the input signal word-length. The truncations are modelled as noise injections $e_i(n)$, for $i = 0$ to 99. The output $y(n)$ is also rounded using the same quantization step size of Q, which is modelled as another noise injection $e_y(n)$.

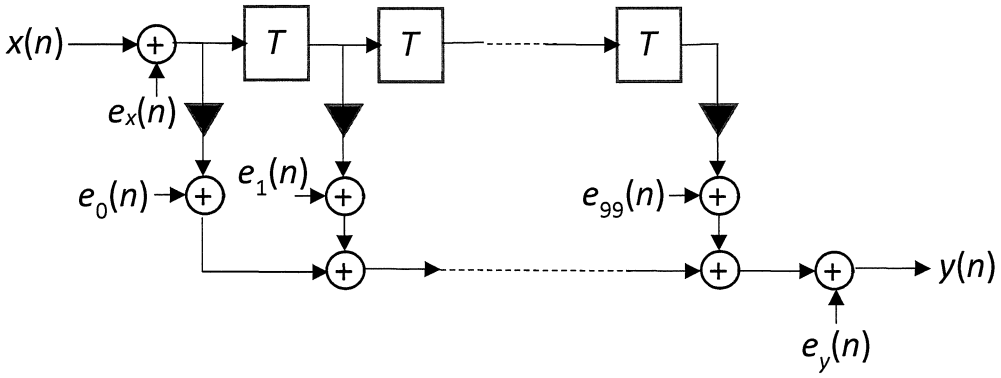

Figure 1

(i) Find the total noise mean (as a function of Q) at the output arising from $e_x(n)$, $e_i(n)$, and $e_y(n)$.

(ii) Find the total noise variance (as a function of Q) at the output arising from $e_x(n)$, $e_i(n)$, and $e_y(n)$.

(iii) It is further known that the input $x(n)$ is rounded to Qm.4 format (with 4 fractional bits after the point). In this case, find the quantization step size of Q. Using your answer, evaluate the total noise mean and the total noise variance you found in part b(i) and part b(ii).

(iv) If the input $x(n)$ is truncated instead of rounding (with the same quantization step size), what would be the total noise mean and the total noise variance?

(11 Marks)

2. (a) The reservation table for a pipelined circuit consisting of 2 stages is shown in Figure 2.

	time			
	0	1	2	3
stages 1	A			A
2		A	A	

Figure 2

(i) What is the minimum achievable throughput for this reservation table?

(ii) Determine the forbidden set of initiations (that causes a collision). Hence, suggest a scheduling strategy (a permissible sequence that does not cause any collision).

(iii) Find the latency and the average throughput for your scheduling strategy in part (a)(ii).

(10 Marks)

(b) A rounding adder is to be designed for rounding a 4-bit input $a_3a_2a_1a_0$ using the carry in bit $c_{-1} = a_{-1}$. The output is $s_3s_2s_1s_0$ and the carry out bit is c_3.

(i) Using the half adder (HA) shown in Figure 3, design the above rounding adder with ripple carry (carry propagates). Draw the block diagram of your design. Both outputs of the half adder need 1 gate delay as shown in the figure. Find the required gate delays for each of the output bits c_3, s_3, s_2, s_1, s_0.

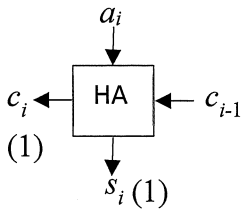

Figure 3

(ii) Describe how carry look-ahead may be used to reduce the gate delay for c_3 (you may ignore the gate delays for s_3, s_2, s_1, s_0). Draw the block diagram of the 4-bit carry look-ahead rounding adder, and find the required gate delay for c_3.

(10 Marks)

3. (a) The data flow graph of a filter of certain form is shown in Figure 4. Each node is labelled by its computation time. If any edge has a delay, it is labelled by D.

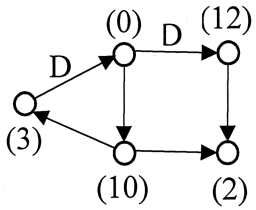

Figure 4

(i) Find a loop in the data flow graph. Find the loop bound for this loop.

(ii) Find the critical path and the computation time required.

(iii) Find a cutset such that the cutset retiming reduces the critical path. Draw the retimed data flow graph and show the new critical path.

(10 Marks)

(b) Figure 5 shows the received analog signal spectrum of a communication system.

(i) Show how a discrete signal can be obtained using inphase/quadrature (I/Q) sampling. Your answer should show spectra at different stages of the sampling system.

(ii) Show how the signal can be obtained using direct digital sampling. Assuming $f_0 = 18$ MHz and $B = 4$ MHz, find all possible sampling frequency ranges that avoid aliasing. Briefly compare direct digital sampling with I/Q sampling.

(10 Marks)

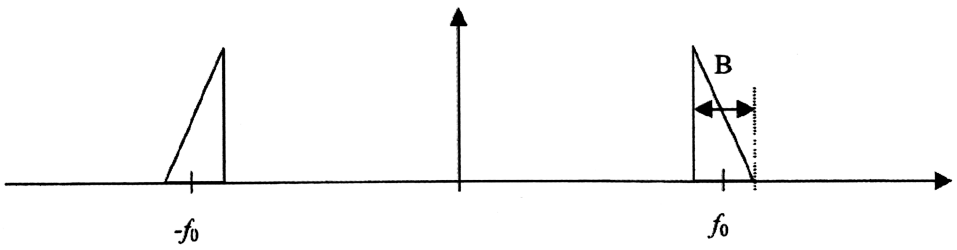

Figure 5

4. (a) Draw a block diagram of a discrete model to describe the operation of a 1st order $\Sigma - \Delta$ modulator. Using the input-output relationship of the discrete model, show that the output noise power of the modulator can be expressed as

$$\kappa\left(\frac{\pi}{M} - \sin\left(\frac{\pi}{M}\right)\right) \quad .$$

Show how symbols κ and M are related to the parameters in your block diagram.

(7 Marks)

(b) Figure 6 shows a vectored interrupt scheme. Explain the operation of this scheme in providing interrupt service to a processor.

(7 Marks)

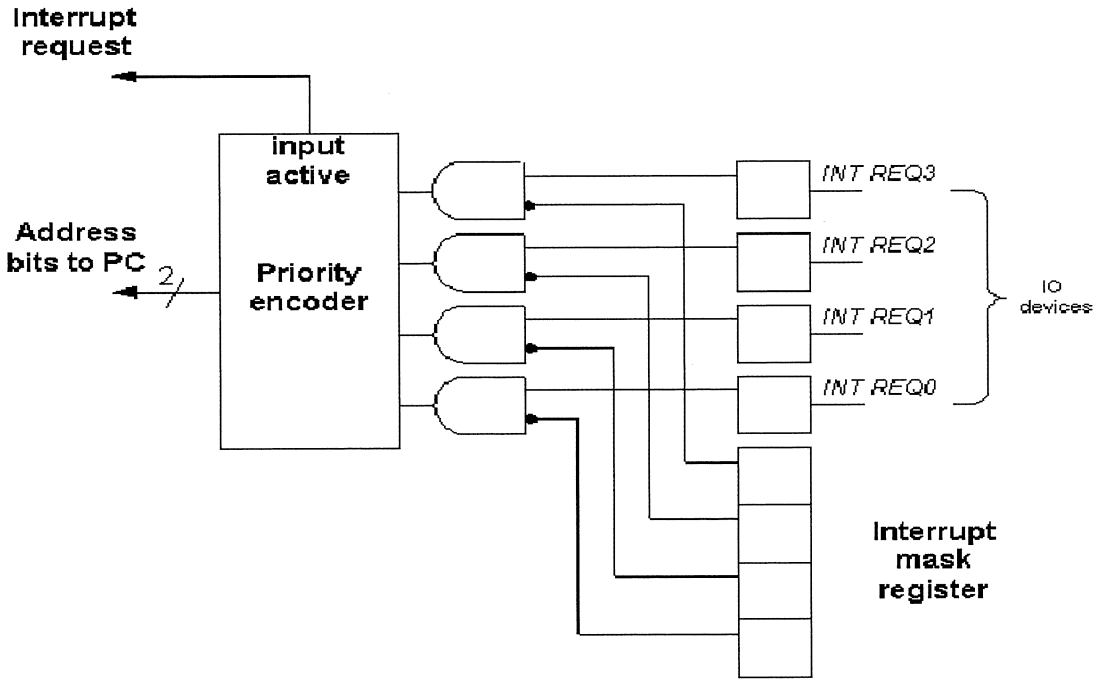

Figure 6

Note : Question No. 4 continues on page 6.

(c) Discrete Fourier transform (DFT) of an N-length sequence $x(n)$ is given by

$$X(k) = \sum_{n=0}^{N-1} x(n)e^{-j2\pi kn/N} \qquad \text{for} \quad (0 \leq k \leq N-1).$$

Express the above using 2 $(N/2)$–length DFTs. Hence explain how the following codes would be used in implementing a DFT in a digital signal processor.

```
STM     #addr1, AR3
STM     #addr2, AR2
STM     #64, AR0
RPT     #127
MVDD    *AR3+0B, *AR2+
```

(6 Marks)

5. (a) An L-length finite impulse response (FIR) filter was implemented on a C54x digital signal processor (DSP) in block processing mode. The DSP executes an instruction in 10 ns. The FIR filter routine requires $5 + B \times (5 + L)$ clocks to run where B is the block size. Determine the maximum possible sampling frequency for real-time implementation if the filter length is 32 and the block size is 128. Neglect the processing overheads.

(7 Marks)

(b) A part of a FIR filter program implemented on a C54x DSP is shown below. Explain the operation of the program. You need to initialize the BK and AR0 registers appropriately.

```
loop:   RPTZ    A, #30
        MAC     *AR3+0%, *AR2+0%, A
        MAC     *AR3+0%, *AR2, A
        STH     A, *AR4+
        PORTR   inport, *AR2
        B       loop
```

(7 Marks)

(c) A modification to the program in part (b) is shown below. Explain the modified program.

```
        STM     # 299, BRC
        RPTB    loop2-1
        RPTZ    A, #31
        MAC     *AR3+0%, *AR2+, A
        STH     A, *AR4+
        MAR     *+AR2(# -31)
loop2:
```

(6 Marks)

END OF PAPER

EE6402 REAL-TIME DSP DESIGN & APPLICATIONS

Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.