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# **kim-os Documentation**

***Release 1.0***

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## WHAT IS KIM-OS

KIM-OS (briefly, KIM) stands for “**Keep-It-Minimal Operating System**”. It is a state-machine based operating system targeted to Micro Controller Units. Its architecture is intended to be fully cross-platform, though the MCUs currently supported are all ARM Cortex-M core based.

The basic characteristic of KIM is that it can be compiled with simple, opensource, tools, like *gcc*-based toolchain, *make* and basic *bash* commands. A laptop with your favourite Linux distribution is all you need to compile it.

The idea of starting with this project, and most of its contents, came from my professional activities. I am a freelance firmware engineer, with a background in Linux Embedded. I started to work on MCUs a few years ago, and my first understanding about how to approach was provided by the [bathos](#) project, which was my first reference for experiments and tests, and is the model I adopted for KIM itself.

When having to release specific firmware for my clients, I began to collect some code snippets and conceptual ideas in a library that was growing over the time, and eventually ended up in KIM project. So, I can say KIM is the sum of all of my experience in microcontrollers, put together in a (hopefully) orderly form.

All of the source code is provided on MIT-style license, so that you can do whatever you want with it, as long as you declare that you are using it (see LICENSE for more information).



## SOURCE CODE ORGANIZATION

Directly going into the details of the code, this is the result of `ls` command run at KIM-OS root folder:

```
$ ls -l
total 60
drwxrwxr-x 4 colosimo colosimo 4096 mag 18 15:32 app
drwxrwxr-x 4 colosimo colosimo 4096 mag 18 15:32 arch
drwxrwxr-x 2 colosimo colosimo 4096 mag 18 15:32 cli
drwxrwxr-x 2 colosimo colosimo 4096 mag 18 15:32 config
-rw-rw-r-- 1 colosimo colosimo 768 mag 18 15:32 COPYING
-rw-rw-r-- 1 colosimo colosimo 176 mag 18 15:32 CREDITS
drwxrwxr-x 2 colosimo colosimo 4096 mag 18 15:32 doc
drwxrwxr-x 2 colosimo colosimo 4096 mag 19 15:32 drivers
drwxrwxr-x 2 colosimo colosimo 4096 mag 18 15:32 include
drwxrwxr-x 2 colosimo colosimo 4096 mag 18 15:32 kernel
drwxrwxr-x 2 colosimo colosimo 4096 mag 18 15:32 lib
-rw-rw-r-- 1 colosimo colosimo 1225 mag 18 15:32 LICENSE
-rw-rw-r-x 1 colosimo colosimo 146 mag 18 15:32 makeall.sh
-rw-rw-r-- 1 colosimo colosimo 3632 mag 18 15:32 Makefile
-rw-rw-r-- 1 colosimo colosimo 326 mag 18 15:32 README
drwxrwxr-x 2 colosimo colosimo 4096 mag 18 15:32 tasks
```

Here is a brief explanation for all of the most relevant files and subdirectories you can find:

- *arch*: contains all the MCU-specific code. At present, it contains two subfolders, *unix* and *arm*: the first is intended to make the firmware compile on Unix systems, simulating the presence of low-level hardware; the second one contains the code for all supported ARM chips;
- *app*: this is the place where your high-level application(s) will reside; any line of code inside this folder should be arch-independent, so that the same application can be compiled for different SoCs;
- *cli*: it is the **C**ommand **L**ine **I**nterface facility; both the programmer and the end user can have a (quite simple) shell-like user experience (e.g. on UART), to debug and interact with the firmware itself; a set of pre-defined commands is provided; in addition, it is easily extensible;
- *config*: contains all available configurations; a configuration file is a *.mk* file included by main Makefile, containing some variables which define the desired compile options;
- *drivers*: the code for peripherals and chips external to the SoC; the code here must be arch-independent, so that the same chip (e.g. a I2C temperature sensor) will be easily usable from whatever arch providing the needed bus (e.g. I2C);

- *kernel*: the core of KIM-OS; contains all the (hardware independent) functions needed to handle tasks and I/O;
- *include*: header files to be included when using the hardware independent code;
- *lib*: some useful generic functions; `k_printf`, a `printf`-like function, is one of the most important, providing a way of writing formatted strings;
- *tasks*: some generic arch-independent tasks, directly usable and intended as an example about how to write your tasks;



## QUICK START REFERENCE

The prerequisite to compile kim-os for ARM cores is to have basic tools for development in C language on ARM:

- ARM gcc toolchain, e.g. (in my Ubuntu 18.10 system) gcc-arm-none-eabi package; check and fix CROSS\_COMPILE variable in arch/arm/arm.mk if needed
- make
- git

If you want to compile the basic kim-os system from scratch, these are the steps:

- go to a suitable local path and download the up-to-date git version:

```
$ cd /your/local/path
$ git clone git@github.com:colosimo/kim-os.git
Cloning into 'kim-os'...
remote: Enumerating objects: 286, done.
remote: Counting objects: 100% (286/286), done.
remote: Compressing objects: 100% (137/137), done.
remote: Total 1537 (delta 157), reused 256 (delta 147), pack-reused 1251
Receiving objects: 100% (1537/1537), 203.59 KiB | 0 bytes/s, done.
Resolving deltas: 100% (851/851), done.
Checking connectivity... done.
```

- go into downloaded directory and compile your config (e.g. discovery\_f407vg is for STM32 F407 Discovery Board):

```
$ cd kim-os
$ make CONFIG=discovery_f407vg
```

The files cli.elf, cli.hex and cli.bin will be created; their name before prefix is given by the APP variable defined in the choosen config (cli in our example regarding Discovery Board).

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**Note:** The configuration chosen by make CONFIG=etc is saved in local .config file; for this reason, all subsequent compile operations on the same configuration do not need CONFIG= to be specified. Before changing from one configuration to another, it is recommended to perform a make clean operation.

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## CORTEX-M CORES: FROM POWER-ON TO RUNNING APPLICATION

I think that one of the most instructive subjects to be mastered by any computer programmer, especially if working in embedded scope, is the boot of a processor. However, most of software APIs and RTOSes (especially those released by hardware vendors) seem to have the goal of hiding that all; the reason is quite simple: chip vendors just need to sell their hardware, so they want to show *how easy* is to make them boot.

On the other side, KIM allows you to fully understand what happens in the low levels and be able to completely handle the boot process. I hope this will be useful, at least from an educational point of view.

Since Cortex-M is currently the only family of chips supported by KIM, I will refer to ARM Cortex-M core boot process. It is based on ISR vector: at each interrupt is assigned an address, which is automatically called when the interrupt happens. In KIM, the ISR vector is defined as a C array of pointers, defined in the files:

- arch/arm/cpu-cortex-m0/cpu.c for Cortex-M0
- arch/arm/cpu-cortex-m3/cpu.c for Cortex-M3
- arch/arm/cpu-cortex-m4/cpu.c for Cortex-M4

Let's have a look at Cortex-M0, which is the basic model:

```
static const void *attr_isr_v_sys _isrv_sys[] = {
    /* Cortex-M0 system interrupts */
    STACK_TOP,      /* Stack top */
    isr_reset,      /* Reset */
    isr_none,        /* NMI */
    isr_none,        /* Hard Fault */
    0,               /* Reserved */
    0,               /* Reserved */
    0,               /* Reserved */
    0,               /* Reserved */
    0,               /* Reserved */
    0,               /* Reserved */
    0,               /* Reserved */
    isr_none,        /* SVC */
    0,               /* Reserved */
    0,               /* Reserved */
    isr_none,        /* PendSV */
    isr_systick,     /* SysTick */
};
```

The boot is defined by the first two elements:

- the first one must contain the initial address of Stack Pointer; KIM sets it to the top of available RAM, so that all the RAM is available for the stack; this behaviour can be changed, since `STACK_TOP` is defined in the `reg.h` (register definition) file(s) (e.g. `arch/arm/cpu-cortex-m4/soc-stm32f407xx/include/reg.h`)
- the second element in the above ISR vector is the `isr_reset` function, that is pointer to the function executed at power on.

Actually, ARM expects the ISR vector to reside in the first part of the SoC flash; the definition of where each compiled object will be put is done by the so-called linker script. In KIM, the linker script has extension `.lds`. For instance, the file `arch/arm/cpu-cortex-m4/soc-stm32f407xx/kim.lds` contains the “map” of how we expect the compiled objects be put together in the final binary file.

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**Note:** An exhaustive description regarding the ARM system(s) is out of the scope of the present document: more information about the boot process, the Core registers, the interrupt routines, etc, can be found in the [Arm Information Center website](#).

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Let’s have a look at the linker script:

```
MEMORY
{
#ifdef SOC_VARIANT_stm32f407vg
    flash : o = 0x08000000, l = 1024k
    sram   : o = 0x20000000, l = 128k
#else
#error Unhandled SOC_VARIANT: $(SOC_VARIANT)
#endif
}
```

In the first part (here above), the `MEMORY` section, the address and size of RAM and Flash are declared; it is conditioned within C pre-processor `#ifdef` directories, because the KIM Makefile runs it in order to obtain a `lds` compliant with the specific SoC version (after make, you will find `kim.ldscpp` which is the output of C preprocessor).

```
SECTIONS
{
    .text 0x08000000: {
        *(isrv_sys); /* Interrupt Service Routine Vector - System */
        *(isrv_irq); /* Interrupt Service Routine Vector -
↳Peripherals IRQs */
        . = 0x0000240;
        *(.text)
    } > flash
```

The second part declares the “sections”: the first one is `text`, which contains the executable instructions. All ISRs (`isrv_sys` and `isrv_irq`) are located at the beginning of the flash, then all remaining compiled code `*(.text)` follows.

```

. = ALIGN(16);
.etext = .;

.rodata : {
    *(.rodata)
} > flash

. = ALIGN(16);
_erom = .;

.data : {
    __start_data_flash = LOADADDR(.data);
    __start_data_sram = .;
    *(.data);
    . = ALIGN(4);
    __start_tskts = .;
    *(tskts)
    __stop_tskts = .;
    __start_drvs = .;
    *(drvs);
    __stop_drvs = .;
    __start_devs = .;
    *(devs);
    __stop_devs = .;
} > sram AT > flash
__end_data_sram = .;

```

In the next part, the data (r/w and readonly), is declared. According to gcc definition, data contains all the initialized data. In KIM, some special sections are defined (see `include/linker.h` for more information). The goal of these sections is to provide a *declarative* approach for some relevant structs. In this way, if you want to add a task to the system, you will just have to declare, wherever you want, a `struct task_t` with `attr_tasks` attributes, and it will automatically be part of main task array.

```

.bss : {
    . = ALIGN(16);
    __start_bss = .;
    *(.bss);
    . = ALIGN(16);
    __end_bss = .;
} > sram
}

```

The final part just reminds the linker script to include the bss section, and to put it at the end of the RAM; bss is the uninitialized data, and is set to 0 at startup.

Coming back to our boot process, let's see what happens in `isr_reset` routine. Here follows the C code copied from `arch/arm/cpu-cortex-m-common.c` (shared by any Cortex-M SoC):

```

void isr_reset(void)
{
    unsigned char *src, *dest;

```

```
/* Load data to ram */
src = &__start_data_flash;
dest = &__start_data_sram;
while (dest != &__end_data_sram)
    *dest++ = *src++;

/* Set bss section to 0 */
dest = &__start_bss;
while (dest != &__end_bss)
    *dest++ = 0;

/* Skip to mach or board specific init */
init();
}
```

The `isr_reset` performs three main tasks:

- load data section into RAM;
- set to zero the bss section;
- call the `init` function, which is declared externally, and is specific for each SoC.

[TODO: Complete this Chapter]

## THE *ARCH* DIRECTORY

[TODO: Complete this Chapter]





## TASKS DEFINITION AND SCHEDULING

[TODO: Complete this Chapter]



## THE *LIB* LIBRARY

[TODO: Complete this Chapter]



## I/O SYSTEM: DEVICES AND DRIVERS

[TODO: Complete this Chapter]



## COMMAND LINE INTERFACE (CLI)

[TODO: Complete this Chapter]





## WRITING YOUR OWN APPLICATION

[TODO: Complete this Chapter]



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**CHAPTER  
TWELVE**

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**GLOSSARY**

**SoC** System on Chip

**MCU** Micro Controller Unit



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