1)

Case	Clock (ns)	Slack (ns)	Effective Clock (ns)	Total Area	Cost
2 ns Low	2	0.02	1.98	1781.91272	2481.91272
1.7 ns Low	1.7	0	1.7	2170.07373	1470.07373
1.5 ns Low	1.5	0	1.5	2293.552979	593.552979
1.4 ns Low	1.4	-0.07	1.47	2452.32251	602.32251
1	1.4	0.01	1.39	1940.684814	-309.315186
2	**1.38**	**0.01**	**1.37**	**2011.244873**	**-338.755127**
3	1.4	0	1.4	2028.872925	-171.127075
4	1.2	-0.17	1.37	2046.524902	-303.475098
5	1.3	-0.07	1.37	2134.715576	-215.284424
6	1.3	-0.07	1.37	2028.884888	-321.115112

Cases
Optimal case above is 2

Unless otherwise specified, all descriptions below have default settings when opening Design Analyzer. Design Analyzer was restarted for each case. Design Optimization was run multiple times with mapping effort changed – starting with the lowest setting and incrementally increased to indicated mapping effort for each case below.

All Low cases above were performed with low mapping effort

1) Medium mapping effort
Structure logic on (timing driven structuring on, boolean Optimization on)

2) (OPTIMIAL CASE)
High mapping effort
Structure logic off

3) High mapping effort
Structure logic off
Boundary Optimization on

4) High mapping effort
Structure logic on (timing driven structuring off, boolean Optimization on)

5) Medium mapping effort
Structure logic off
Flatten Logic on (high effort, multiple output, apply strategy)

6) High mapping effort
Structure logic on (timing driven structuring on, Boolean optimization on)
Flatten Logic on (high effort, multiple output, apply strategy)
Boundary Optimization on

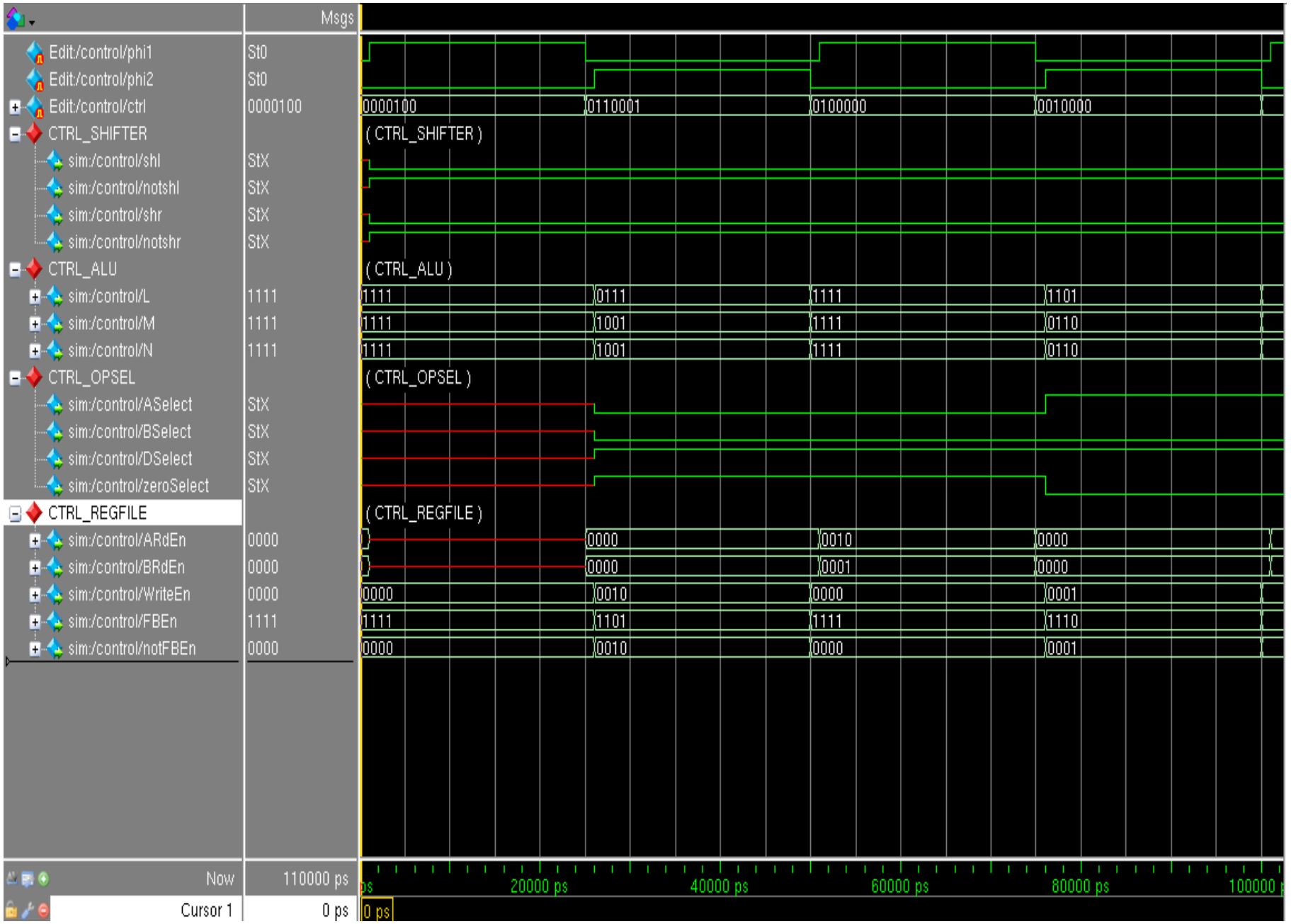
2)

```
 ****************************************
Report : area
Design : FA
Version: X-2005.09
Date   : Mon Mar 16 13:28:36 2015
****************************************

Library(s) Used:

    ece451_cells (File: /cad2/ece451/synopsys/ece451_cells.db)

Number of ports:              6
Number of nets:              20
Number of cells:             13
Number of references:         7

Combinational area:       617.399902
Noncombinational area:   1393.559937
Net Interconnect area:      0.284977

Total cell area:         2010.959961
Total area:              2011.244873
1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : FA
Version: X-2005.09
Date   : Mon Mar 16 13:28:36 2015
****************************************

Operating Conditions: nom_pvt   Library: ece451_cells
Wire Load Model Mode: top

  Startpoint: a_reg (rising edge-triggered flip-flop clocked by clk)
  Endpoint: sum_out_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  FA                 q35_27k               ece451_cells
```

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
a_reg/C (fdp2)	0.00	0.00 r
a_reg/Q (fdp2)	0.57	0.57 f
U38/Q (xo2p2)	0.40	0.97 r
U34/NQ (xn2p2)	0.31	1.28 r
sum_out_reg/D (fdp1)	0.00	1.28 r
data arrival time		1.28
clock clk (rise edge)	1.38	1.38
clock network delay (ideal)	0.00	1.38
sum_out_reg/C (fdp1)	0.00	1.38 r
library setup time	-0.09	1.29
data required time		1.29
data required time		1.29
data arrival time		-1.28
slack (MET)		0.01

3) Simulation

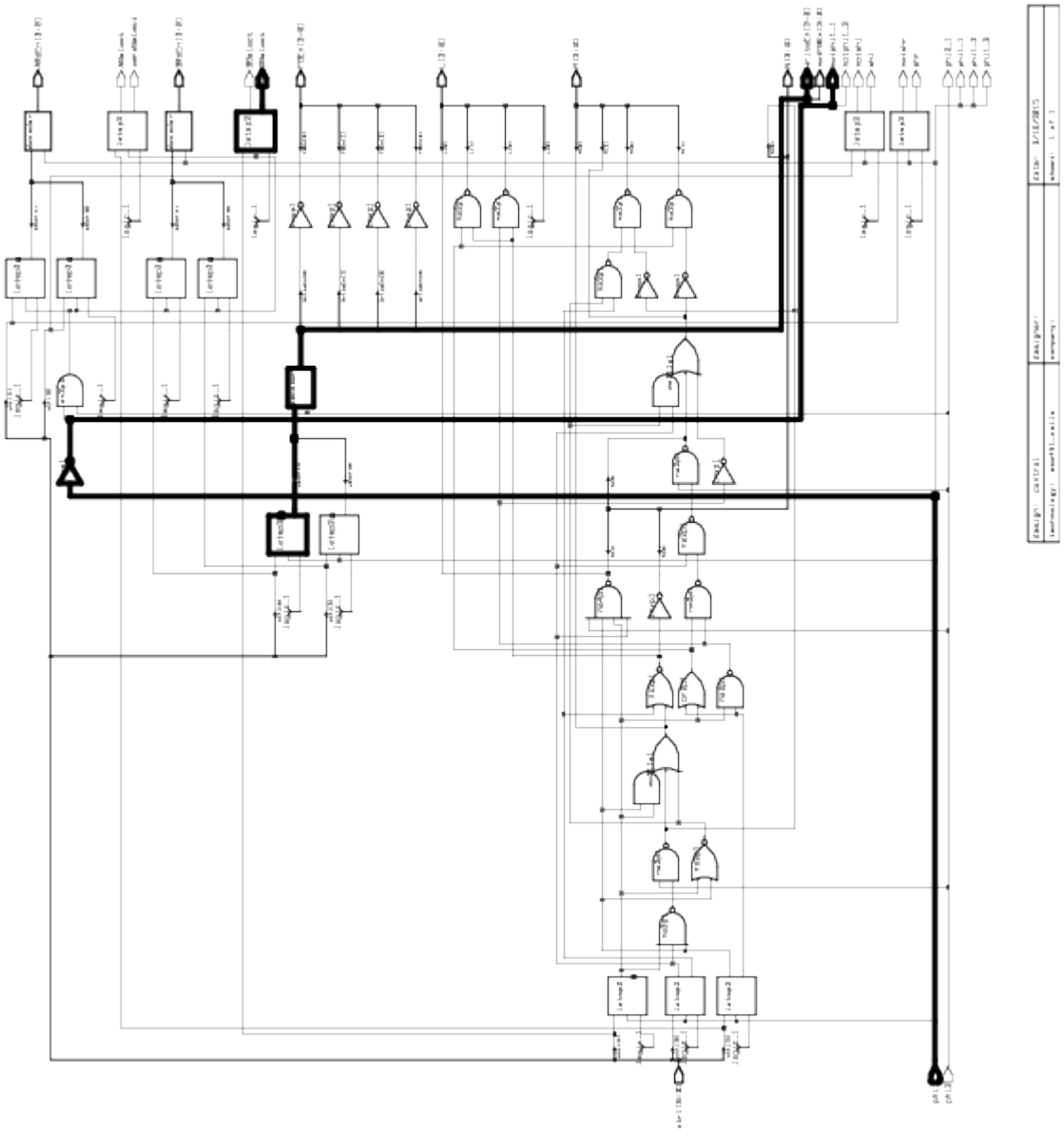
quartus.start was used to do the simulation. An R-S simulation was used. First we do an R+S with R=D and S=0, then we save it into memory location 1. On the next cycle we load the value from memory location 1 into A, which is then loaded into S, and we load the R value into D, where we do R-S and save it in memory location 0. The L, M, and N values can be read from the previous lab report. There is no shifting at all.


Msgs
Edit:/control/phi1
St0
Edit:/control/phi2
St0
Edit:/control/ctrl
0000100
0000100
0110001
0100000
0010000
CTRL_SHIFTER
(CTRL_SHIFTER)
sim:/control/shl
StX
sim:/control/notshl
StX
sim:/control/shr
StX
sim:/control/notshr
StX
CTRL_ALU
(CTRL_ALU)
sim:/control/L
1111
1111
0111
1111
1101
sim:/control/M
1111
1111
1001
1111
0110
sim:/control/N
1111
1111
1001
1111
0110
CTRL_OPSEL
(CTRL_OPSEL)
sim:/control/ASelect
StX
sim:/control/BSelect
StX
sim:/control/DSelect
StX
sim:/control/zeroSelect
StX
CTRL_REGFILE
(CTRL_REGFILE)
sim:/control/ARdEn
0000
0000
0010
0000
sim:/control/BRdEn
0000
0000
0001
0000
sim:/control/WriteEn
0000
0000
0010
0000
0001
sim:/control/FBEn
1111
1111
1101
1111
1110
sim:/control/notFBEn
0000
0000
0010
0000
0001
Now
110000 ps
Cursor 1
0 ps
0 ps
20000 ps
40000 ps
60000 ps
80000 ps
100000 p

4)

```
compile -map_effort low
create_clock -name "phi1" -period 19.1 -waveform {"0" "9.3"} {"phi1"}
create_clock -name "phi2" -period 19.1 -waveform {"9.55" "18.85"} {"phi2"}
set_max_delay 0.2 -from {"phi1"} -to {"phi1_1"}
set_max_delay 0.2 -from {"phi1"} -to {"phi1_2"}
set_max_delay 0.2 -from {"phi1"} -to {"phi1_3"}
set_max_delay 0.2 -from {"phi2"} -to {"phi2_1"}
set_max_delay 0.2 -from {"phi1"} -to {"notphi1_1"}
set_max_delay 0.2 -from {"phi1"} -to {"notphi1_1"}
set_output_delay -clock phi1 -max 0 "ARdEn"
set_output_delay -clock phi1 -max 0 "BRdEn"
set_output_delay -clock phi1 -max 2.2 "ASelect"
set_output_delay -clock phi1 -max 2.2 "zeroSelect"
set_output_delay -clock phi1 -max 2.2 "DSelect"
set_output_delay -clock phi1 -max 2.2 "BSelect"
set_output_delay -clock phi2 -max 0 "L"
set_output_delay -clock phi2 -max 0 "M"
set_output_delay -clock phi2 -max 3.5 "N"
set_output_delay -clock phi2 -max 6 "shr"
set_output_delay -clock phi2 -max 6 "shl"
set_output_delay -clock phi2 -max 6 "notshr"
set_output_delay -clock phi2 -max 6 "notshl"
set_output_delay -clock phi2 -max 7.5 "WriteEn"
```

5 Bottom up a)



5 bottom up b)
****
Report : area
Design : control
Version: X-2005.09
Date   : Mon Mar 16 21:05:12 2015
****

Library(s) Used:

    gtech (File: /CMC/tools/synopsys/syn_vX-2005.09/libraries/syn/gtech.db)
    ece451_cells (File: /cad2/ece451/synopsys/ece451_cells.db)

Number of ports: 55
Number of nets: 81
Number of cells: 43
Number of references: 10

Combinational area: 1517.040283
Noncombinational area: 2751.839355
Net Interconnect area: 2.386782

Total cell area: 4268.879883
Total area: 4271.266602

Information: This design contains unmapped logic. (RPT-7)
1
design_analyzer>
****
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : control
Version: X-2005.09
Date   : Mon Mar 16 21:05:12 2015
****

Operating Conditions: nom_pvt   Library: ece451_cells
Wire Load Model Mode: top

  Startpoint: opsel_reg[0]
              (positive level-sensitive latch clocked by phi2)
  Endpoint: DSelect (output port clocked by phi1)
  Path Group: phi1
  Path Type: max

  Des/Clust/Port   Wire Load Model   Library

```
control          q35_27k             ece451_cells

Point                              Incr       Path
-----------------------------------------------------------
clock phi2 (rise edge)                9.55       9.55
clock network delay (ideal)           0.00       9.55
opsel_reg[0]/G (latsp2)               0.00       9.55 r
opsel_reg[0]/Q (latsp2)               0.73      10.28 r
DSelect (out)                      0.00      10.28 r
data arrival time                            10.28

clock phi1 (rise edge)               19.10      19.10
clock network delay (ideal)           0.00      19.10
output external delay                -2.20      16.90
data required time                           16.90
-----------------------------------------------------------
data required time                           16.90
data arrival time                           -10.28
-----------------------------------------------------------
slack (MET)                                  6.62


Startpoint: waddr_reg[1]
          (positive level-sensitive latch clocked by phi1)
Endpoint: WriteEn[0] (output port clocked by phi2)
Path Group: phi2
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
control          q35_27k             ece451_cells

Point                              Incr       Path
-----------------------------------------------------------
clock phi1 (rise edge)                0.00       0.00
clock network delay (ideal)           0.00       0.00
waddr_reg[1]/G (latsp2)               0.00       0.00 r
waddr_reg[1]/Q (latsp2)               0.86       0.86 r
I3/a[1] (decoder)                  0.00       0.86 r
I3/C24/Z (GTECH_OR2)                  0.00       0.86 r
I3/I_2/Z (GTECH_NOT)                  0.00       0.86 f
I3/C16/Z_0 (*SELECT_OP_2.4_2.1_4)       0.00       0.86 f
I3/x[0] (decoder)                  0.00       0.86 f
WriteEn[0] (out)                   0.00       0.86 f
data arrival time                            0.86

clock phi2 (rise edge)                9.55       9.55
clock network delay (ideal)           0.00       9.55
output external delay                -7.50       2.05
```

```
  data required time                                 2.05
  ---------------------------------------------------------
  data required time                                 2.05
  data arrival time                                 -0.86
  ---------------------------------------------------------
  slack (MET)                                        1.19


  Startpoint: phi1 (clock source 'phi1')
  Endpoint: notphi1_1 (output port)
  Path Group: default
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  control            q35_27k               ece451_cells

  Point                              Incr       Path
  ---------------------------------------------------------
  phi1 (in)                        0.00       0.00 r
  U51/NQ (invp1)                     0.27       0.27 f
  notphi1_1 (out)                    0.00       0.27 f
  data arrival time                             0.27

  max_delay                        0.20       0.20
  output external delay              0.00       0.20
  data required time                            0.20
  ---------------------------------------------------------
  data required time                            0.20
  data arrival time                            -0.27
  ---------------------------------------------------------
  slack (VIOLATED)                              -0.07


1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : control
Version: X-2005.09
Date   : Mon Mar 16 21:09:59 2015
****************************************

Operating Conditions: nom_pvt   Library: ece451_cells
Wire Load Model Mode: top
```

```
Startpoint: opsel_reg[0]
          (positive level-sensitive latch clocked by phi2)
Endpoint: DSelect (output port clocked by phi1)
Path Group: phi1
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
control            q35_27k               ece451_cells

Point                                 Incr       Path
-------------------------------------------------------------
clock phi2 (rise edge)                9.55       9.55
clock network delay (ideal)           0.00       9.55
opsel_reg[0]/G (latsp2)               0.00       9.55 r
opsel_reg[0]/Q (latsp2)               0.73      10.28 r
DSelect (out)                         0.00      10.28 r
data arrival time                               10.28

clock phi1 (rise edge)               19.10      19.10
clock network delay (ideal)           0.00      19.10
output external delay                -2.20      16.90
data required time                              16.90
-------------------------------------------------------------
data required time                              16.90
data arrival time                              -10.28
-------------------------------------------------------------
slack (MET)                                     6.62


Startpoint: waddr_reg[1]
          (positive level-sensitive latch clocked by phi1)
Endpoint: WriteEn[0] (output port clocked by phi2)
Path Group: phi2
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
control            q35_27k               ece451_cells

Point                                 Incr       Path
-------------------------------------------------------------
clock phi1 (rise edge)                0.00       0.00
clock network delay (ideal)           0.00       0.00
waddr_reg[1]/G (latsp2)               0.00       0.00 r
waddr_reg[1]/Q (latsp2)               0.86       0.86 r
I3/a[1] (decoder)                     0.00       0.86 r
I3/C24/Z (GTECH_OR2)                  0.00       0.86 r
I3/I_2/Z (GTECH_NOT)                  0.00       0.86 f
```

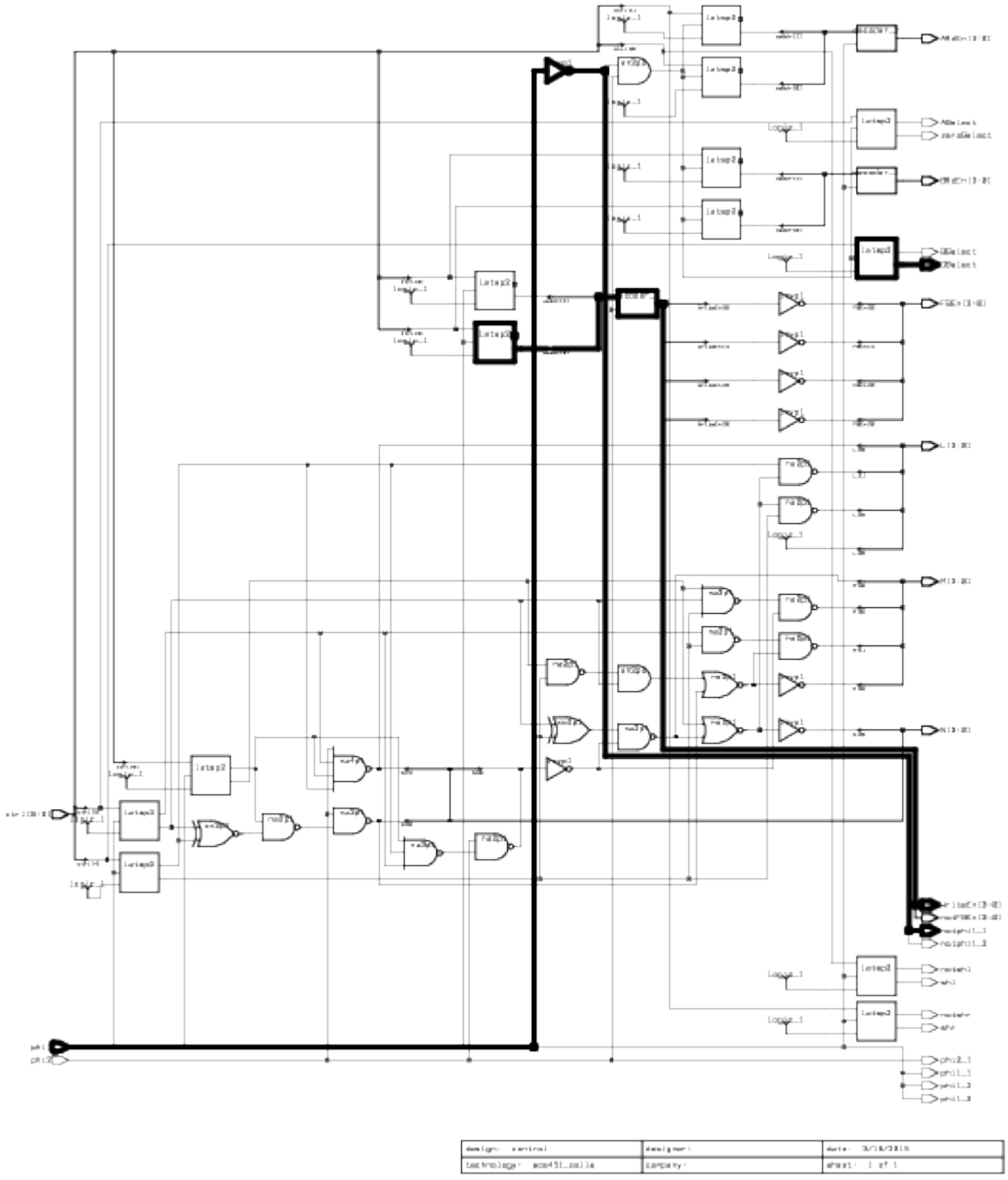
```
I3/C16/Z_0 (*SELECT_OP_2.4_2.1_4)        0.00       0.86 f
I3/x[0] (decoder)                        0.00       0.86 f
WriteEn[0] (out)                         0.00       0.86 f
data arrival time                                   0.86

clock phi2 (rise edge)                   9.55       9.55
clock network delay (ideal)              0.00       9.55
output external delay                   -7.50       2.05
data required time                                  2.05
-----------------------------------------------------------
data required time                                  2.05
data arrival time                                  -0.86
-----------------------------------------------------------
slack (MET)                                         1.19
```

5 bottom up c)

Signal	Max delay
phi1_1 (out)	0.00 f
phi1_2 (out)	0.00 f
phi1_3 (out)	0.00 f
notphi1_1 (out)	0.27 f
WriteEn[0] (out)	0.86 f
WriteEn[1] (out)	0.86 f
WriteEn[2] (out)	0.86 f
WriteEn[3] (out)	0.86 r
shl (out)	0.73 r
shr (out)	0.73 r
notshl (out)	0.59 f
notshr (out)	0.59 f
N[3] (out)	2.87 f
N[2] (out)	2.32 r
N[0] (out)	1.71 f
N[1] (out)	1.37 r
M[1] (out)	3.13 r
DSelect (out)	0.73 r
zeroSelect (out)	0.73 r
L[1] (out)	2.87 f
L[2] (out)	2.87 f

M[2] (out)	2.80 r
ASelect (out)	0.59 f
BSelect (out)	0.59 f
M[3] (out)	2.25 f
M[0] (out)	2.09 f
L[3] (out)	1.37 r
ARdEn[0] (out)	0.86 r
ARdEn[1] (out)	0.86 r
ARdEn[2] (out)	0.86 r
BRdEn[0] (out)	0.86 r
BRdEn[1] (out)	0.86 r
BRdEn[2] (out)	0.86 r
ARdEn[3] (out)	0.86 r
BRdEn[3] (out)	0.86 r

5 uniquify a)



5 uniquify b)

Library(s) Used:

ece451_cells (File: /cad2/ece451/synopsys/ece451_cells.db)

Number of ports: 55
Number of nets: 82
Number of cells: 43
Number of references: 12

Combinational area: 2875.319824
Noncombinational area: 2751.839355
Net Interconnect area: 2.141498

Total cell area: 5627.159668
Total area: 5629.300781
1
design_analyzer>
****
Report : timing
-path full
-delay max
-max_paths 1
Design : control
Version: X-2005.09
Date : Mon Mar 16 21:24:35 2015
****

Operating Conditions: nom_pvt Library: ece451_cells
Wire Load Model Mode: top

Startpoint: opsel_reg[0]
(positive level-sensitive latch clocked by phi2)
Endpoint: DSelect (output port clocked by phi1)
Path Group: phi1
Path Type: max

Des/Clust/Port	Wire Load Model	Library
control	q35_27k	ece451_cells

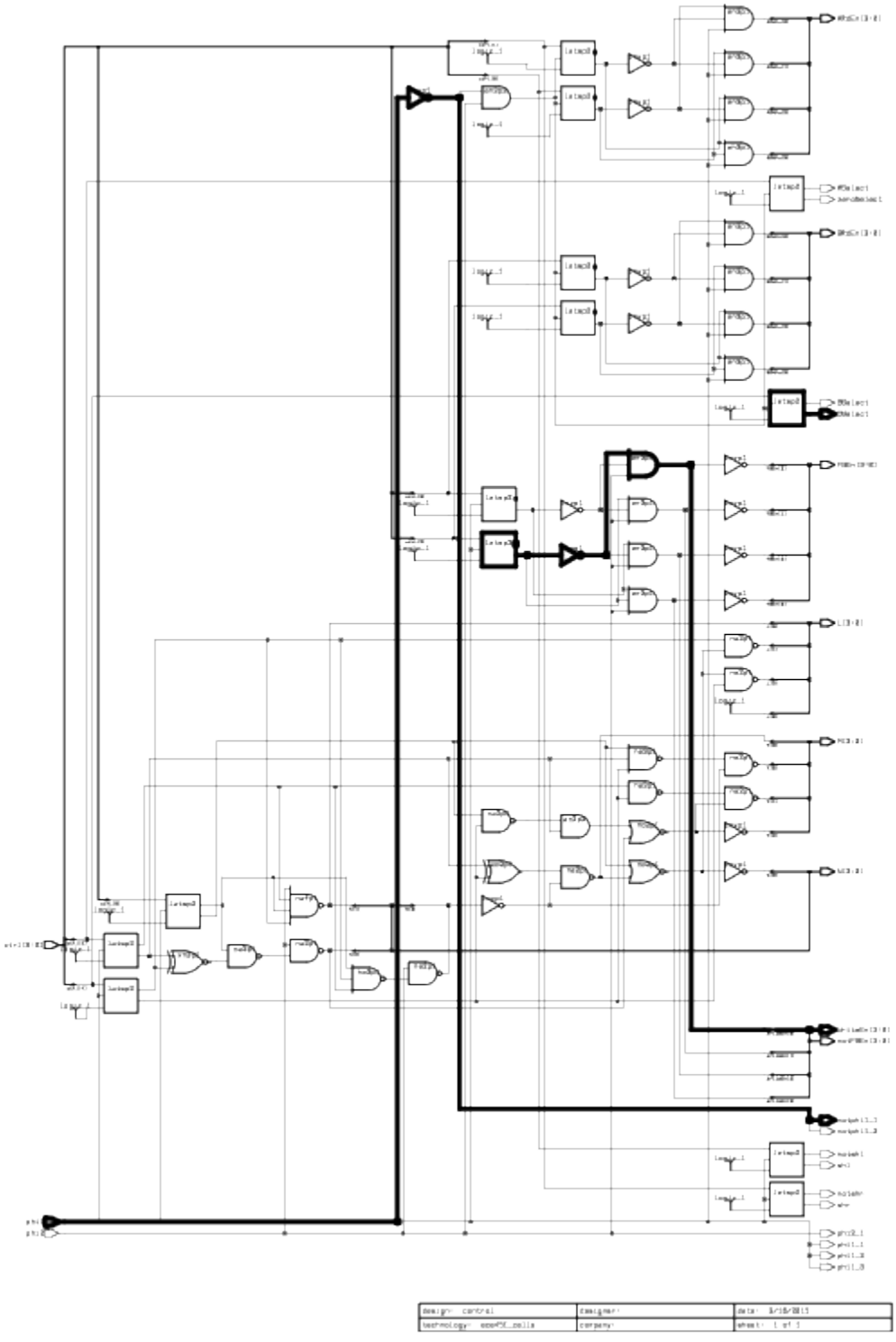
Point	Incr	Path
clock phi2 (rise edge)	9.55	9.55
clock network delay (ideal)	0.00	9.55
opsel_reg[0]/G (latsp2)	0.00	9.55 r
opsel_reg[0]/Q (latsp2)	0.73	10.28 r
DSelect (out)	0.00	10.28 r

```
data arrival time                                  10.28

clock phi1 (rise edge)                  19.10      19.10
clock network delay (ideal)              0.00      19.10
output external delay                   -2.20      16.90
data required time                                 16.90
-----------------------------------------------------------
data required time                                 16.90
data arrival time                                 -10.28
-----------------------------------------------------------
slack (MET)                                        6.62


Startpoint: waddr_reg[0]
            (positive level-sensitive latch clocked by phi1)
Endpoint: WriteEn[0] (output port clocked by phi2)
Path Group: phi2
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
control            q35_27k               ece451_cells

Point                                  Incr       Path
-----------------------------------------------------------
clock phi1 (rise edge)                 0.00       0.00
clock network delay (ideal)            0.00       0.00
waddr_reg[0]/G (latsp2)                0.00       0.00 r
waddr_reg[0]/Q (latsp2)                0.85       0.85 r
I3/a[0] (decoder_0)                    0.00       0.85 r
I3/U37/NQ (invp1)                      0.29       1.14 f
I3/U35/Q (an3p1)                       0.58       1.72 f
I3/x[0] (decoder_0)                    0.00       1.72 f
WriteEn[0] (out)                       0.00       1.72 f
data arrival time                                 1.72

clock phi2 (rise edge)                 9.55       9.55
clock network delay (ideal)            0.00       9.55
output external delay                  -7.50      2.05
data required time                                2.05
-----------------------------------------------------------
data required time                                2.05
data arrival time                                -1.72
-----------------------------------------------------------
slack (MET)                                       0.33
```

5 uniquify c)

Signal	Max Delay
notphi1_1 (out)	0.27 f
phi1_1 (out)	0.00 f
phi1_2 (out)	0.00 f
phi1_3 (out)	0.00 f
WriteEn[0] (out)	1.72 f
WriteEn[2] (out)	1.70 f
WriteEn[1] (out)	1.70 f
WriteEn[3] (out)	1.35 f
shl (out)	0.73 r
shr (out)	0.73 r
notshl (out)	0.59 f
notshr (out)	0.59 f
N[3] (out)	2.70 f
N[2] (out)	1.85 r
N[0] (out)	1.39 f
N[1] (out)	1.06 r
DSelect (out)	0.73 r
zeroSelect (out)	0.73 r
ASelect (out)	0.59 f
BSelect (out)	0.59 f
L[1] (out)	2.70 f
L[2] (out)	2.66 f

5 flatten a)



5 flatten b)

```
****************************************
Report : area
Design : control
Version: X-2005.09
Date   : Mon Mar 16 21:33:17 2015
****************************************

Library(s) Used:

    ece451_cells (File: /cad2/ece451/synopsys/ece451_cells.db)

Number of ports:              55
Number of nets:               88
Number of cells:              58
Number of references:         10

Combinational area:       2875.319824
Noncombinational area:    2751.839355
Net Interconnect area:       2.141498

Total cell area:          5627.159668
Total area:               5629.300781
1
design_analyzer>
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : control
Version: X-2005.09
Date   : Mon Mar 16 21:33:17 2015
****************************************

Operating Conditions: nom_pvt   Library: ece451_cells
Wire Load Model Mode: top

  Startpoint: opsel_reg[0]
              (positive level-sensitive latch clocked by phi2)
  Endpoint: DSelect (output port clocked by phi1)
  Path Group: phi1
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  control            q35_27k               ece451_cells
```

```
Point                                  Incr       Path
-----------------------------------------------------------
clock phi2 (rise edge)                 9.55       9.55
clock network delay (ideal)            0.00       9.55
opsel_reg[0]/G (latsp2)                0.00       9.55 r
opsel_reg[0]/Q (latsp2)                0.73      10.28 r
DSelect (out)                          0.00      10.28 r
data arrival time                                10.28

clock phi1 (rise edge)                19.10      19.10
clock network delay (ideal)            0.00      19.10
output external delay                 -2.20      16.90
data required time                               16.90
-----------------------------------------------------------
data required time                               16.90
data arrival time                               -10.28
-----------------------------------------------------------
slack (MET)                                      6.62


Startpoint: waddr_reg[0]
            (positive level-sensitive latch clocked by phi1)
Endpoint: WriteEn[0] (output port clocked by phi2)
Path Group: phi2
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
control            q35_27k               ece451_cells

Point                                  Incr       Path
-----------------------------------------------------------
clock phi1 (rise edge)                 0.00       0.00
clock network delay (ideal)            0.00       0.00
waddr_reg[0]/G (latsp2)                0.00       0.00 r
waddr_reg[0]/Q (latsp2)                0.85       0.85 r
I3/U37/NQ (invp1)                      0.29       1.14 f
I3/U35/Q (an3p1)                       0.58       1.72 f
WriteEn[0] (out)                       0.00       1.72 f
data arrival time                                 1.72

clock phi2 (rise edge)                 9.55       9.55
clock network delay (ideal)            0.00       9.55
output external delay                 -7.50       2.05
data required time                               2.05
-----------------------------------------------------------
data required time                               2.05
data arrival time                               -1.72
-----------------------------------------------------------
```

slack (MET) 0.33

5 flatten c)

Signal	Max Delay
notphi1_1 (out)	0.27 f
phi1_1 (out)	0.00 f
phi1_2 (out)	0.00 f
phi1_3 (out)	0.00 f
WriteEn[0] (out)	1.72 f
WriteEn[2] (out)	1.70 f
WriteEn[1] (out)	1.70 f
WriteEn[3] (out)	1.35 f
shl (out)	0.73 r
shr (out)	0.73 r
notshl (out)	0.59 f
notshr (out)	0.59 f
N[3] (out)	2.70 f
N[2] (out)	1.85 r
N[0] (out)	1.39 f
N[1] (out)	1.14 r
DSelect (out)	0.73 r
zeroSelect (out)	0.73 r
ASelect (out)	0.59 f
BSelect (out)	0.59 f
ASelect (out)	0.51 r
BSelect (out)	0.51 r
L[1] (out)	2.70 f
L[2] (out)	2.66 f

6) uniquify script

```
read -format verilog control.v
Current_design control
Uniquify
Characterize -cons {I1, I2, I3}
Write -o top.db

Current_design decoder_0
```

```
Write_script > decoder_0.scr
Write -o decoder_0.db

Current_design decoder_1
Write_script > decoder_1.scr
Write -o decoder_1.db

Current_design decoder_2
Write_script > decoder_2.scr
Write -o decoder_2.db

remove_design -designs

read decoder_0.db
include decoder_0.scr
compile -map_effort low
write -o decoder_0.db

read decoder_1.db
include decoder_1.scr
compile -map_effort low
write -o decoder_1.db

read decoder_2.db
include decoder_2.scr
compile -map_effort low
write -o decoder_2.db

read top.db
read decoder_0.db
read decoder_1.db
read decoder_2.db

Current_design control
compile -map_effort low
```

7) a)
Structural is easier because the behaviour is more intuitive compared to behavioural. Defining the structure of your circuit makes more sense for designers compared to using always blocks to define behaviour.

b)
Inaccuracies can be from extremely pessismtic or optimistic estimates, or can be from wires being placed slightly off due to lambda. You can reduce these by running a more accurate simulator for longer. Could also be from voltage problems or large amounts of noise, which might cause a problem with the capacitances.

c)
Bottom up is easy to implement, uniquify is harder, and flatten is the hardest. Uniquify also required writing a script, which was mildly annoying. Bottom up also has the smallest area, with flatten having the largest, and uniquify almost being the same size as flatten. However bottom up also has the worst timing, with uniquify having the best timing. Overall each method created pretty similar results, with area increasing by roughly 20% and timing decreasing by about 10% when comparing bottom up to flatten.