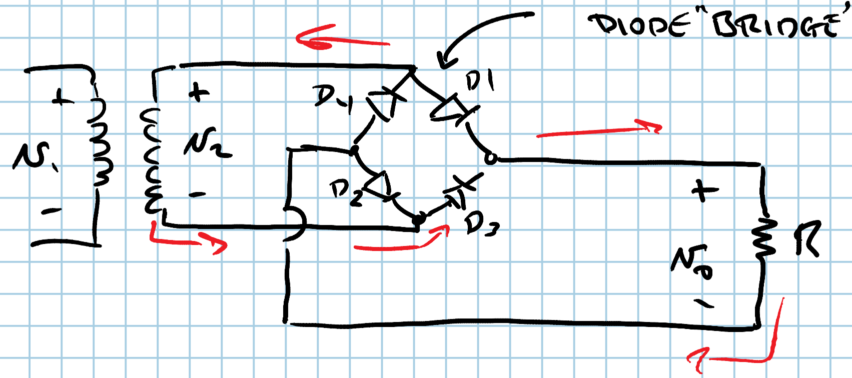
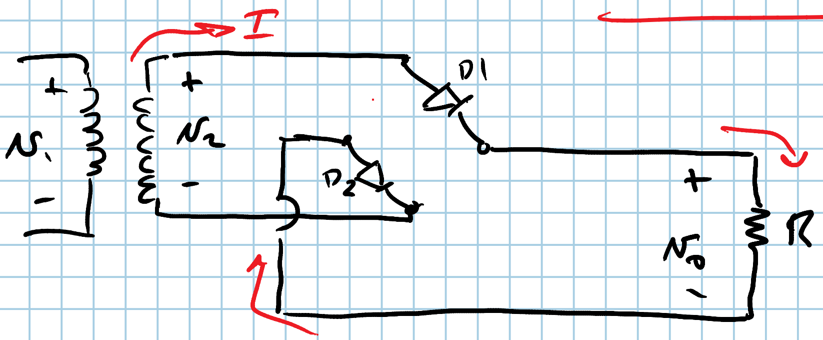
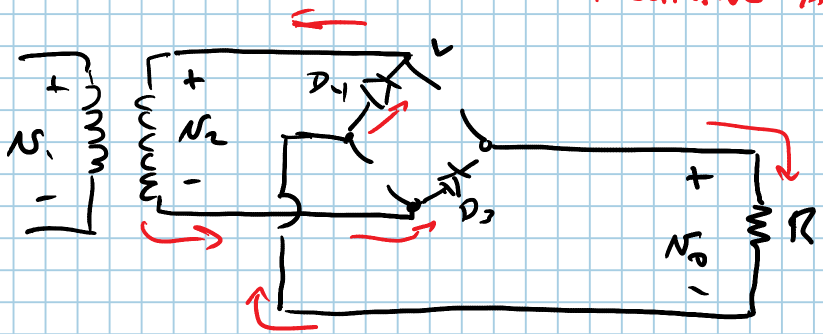
FULL-WAVE RECTIFICATION II

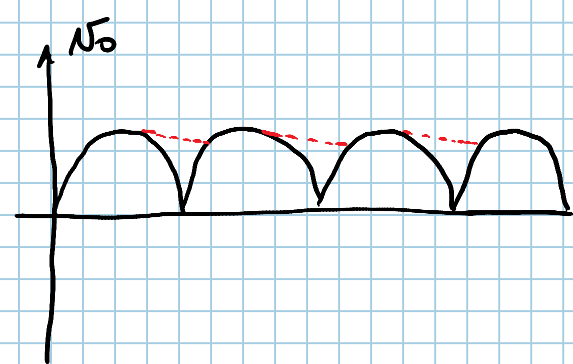


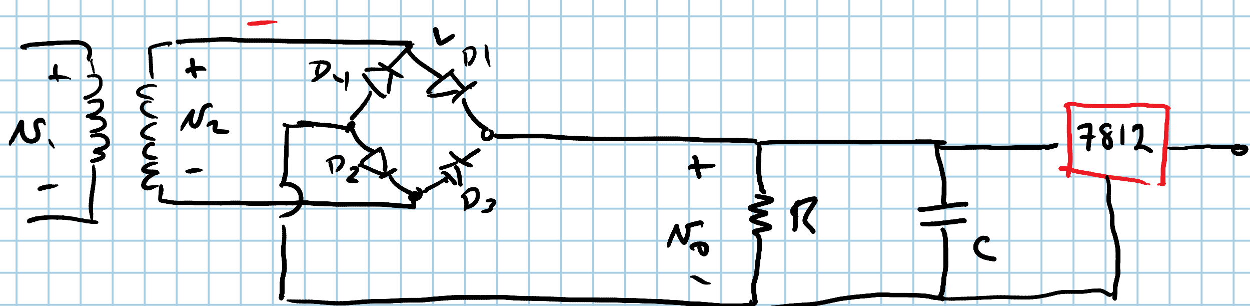
POSITIVE HALF-CYCLE



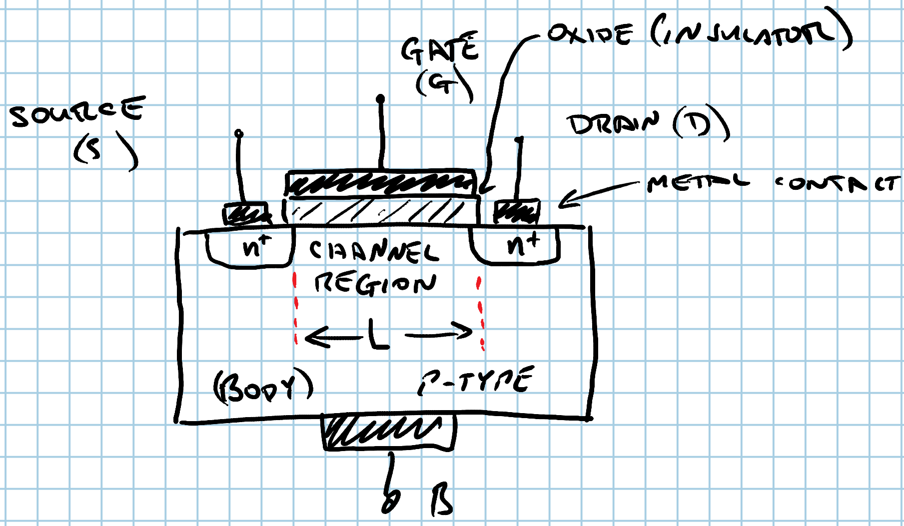
NEGATIVE HALF-CYCLE

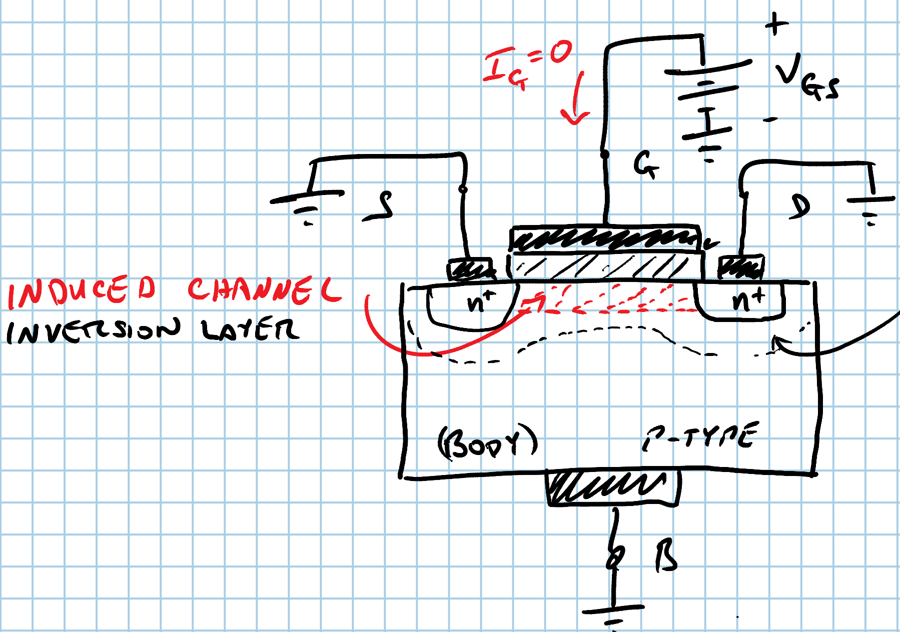






Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs)

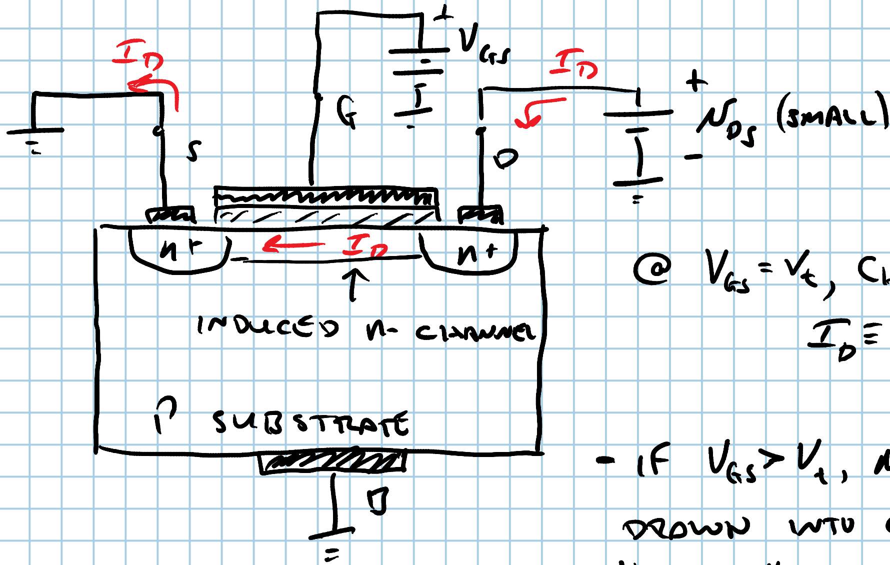




n-CHANNEL MOSFET
NMOS TRANSISTOR

$V_t \equiv$ THRESHOLD VOLTAGE, THE VALUE OF V_{GS} AT WHICH ENOUGH MOBILE ELECTRONS ACCUMULATE IN THE CHANNEL TO SUPPORT CONDUCTION.

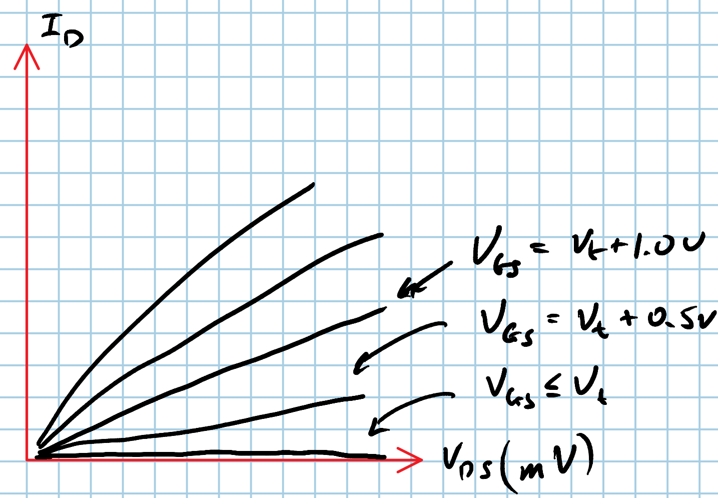
$V_t > 0$ FOR NMOS

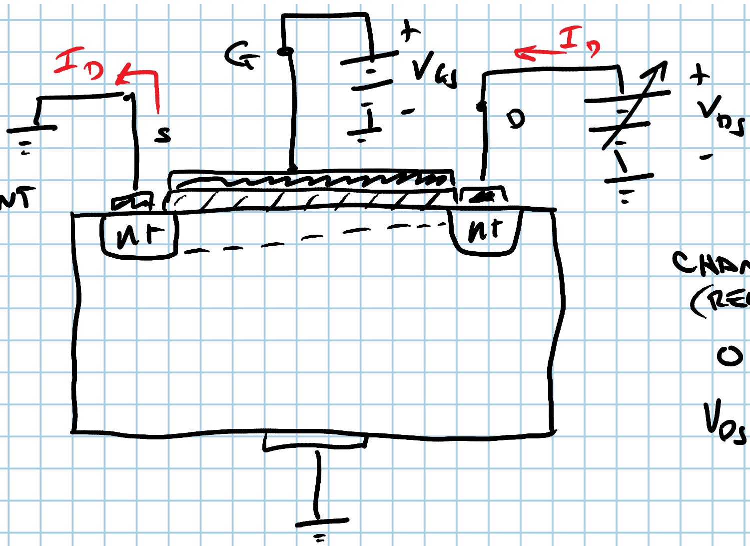


@ $V_{GS} = V_t$, CHANNEL IS JUST INDUCED,
$I_D \equiv$ NEGLIGIBLE

- IF $V_{GS} > V_t$, MORE ELECTRONS ARE DRAWN INTO CHANNEL, CHANNEL IS "DEEPER", INCREASED CONDUCTANCE, ⇒ REDUCED RESISTANCE.

- CHANNEL CONDUCTANCE IS PROPORTIONAL TO THE "EXCESS GATE VOLTAGE" = $V_{GS} - V_t$





$V_{GS} > V_t$, CONSTANT

CHANNEL VOLTAGE, (RELATIVE TO SOURCE)

0 V @ SOURCE END

V_{DS} @ DRAIN END

- VOLTAGE BETWEEN GATE & POINTS ALONG CHANNEL:

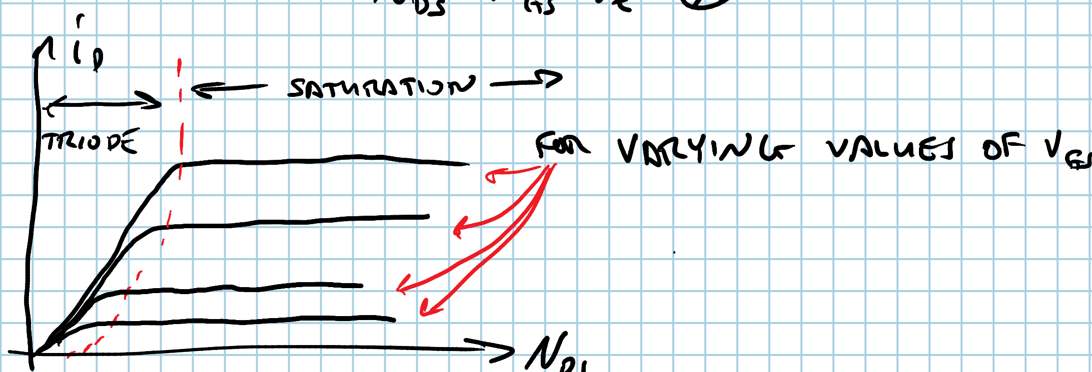
$V_{GS} - 0$ @ SOURCE

$V_{GS} - V_{DS}$ @ DRAIN

- WHEN V_{DS} INCREASES TO THE VALUE THAT REDUCES THE VOLTAGE BETWEEN GATE & CHANNEL @ THE DRAIN END TO V_t,

$V_{GD} = V_t$, OR $V_{GS} - V_{DS} = V_t$

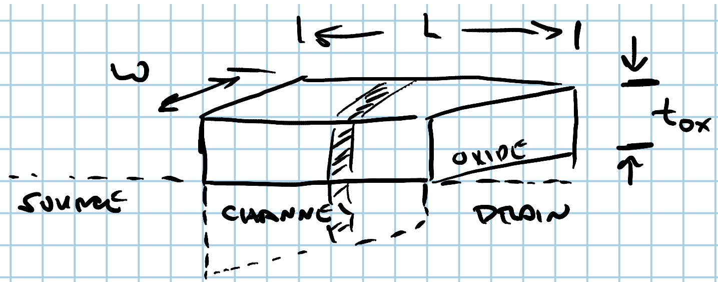
OR $V_{DS} = V_{GS} - V_t$ ⊗



@ $V_{DS} = V_{GS} - V_t$, - CHANNEL DEPTH (@ DRAIN END) IS ALMOST ZERO

- CHANNEL IS SAID TO BE "PINCHED-OFF".

$I_D \equiv$ SATURATED, $V_{DS} \equiv V_{DS_{SAT}} = V_{GS} - V_t$



$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$\varepsilon_{ox} \equiv$ PERMITTIVITY OF OXIDE LAYER

$t_{ox} \equiv$ THICKNESS OF OXIDE LAYER

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left[(v_{GS}-V_t)v_{DS} - \tfrac{1}{2}v_{DS}^2\right] \quad \text{(TRIODE REGION)}$$

IF $v_{DS} = v_{GS} - V_t \Rightarrow$ PINCHED-OFF, IN SATURATION RGN.

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\frac{1}{2}(v_{GS}-V_t)^2 \quad \text{(SATURATION RGN. OPERATION)}$$

($\mu_n \equiv$ ELECTRON MOBILITY)

$\mu_n C_{ox} = k_n' \left(A/V^2\right)$ PROCESS TRANSCONDUCTANCE PARAMETER

$$\therefore \quad i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS}-V_t)v_{DS} - \tfrac{1}{2}v_{DS}^2\right] \quad \text{(TRIODE REGION)}$$

$$i_D = \tfrac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS}-V_t)^2 \quad \text{(SATURATION REGION)}$$

EXAMPLE 5.1, pg 243

$L_{min} = 0.4\ \mu m$

$t_{ox} = 8\ nm$

$\mu_n = 450\ \frac{cm^2}{V \cdot s}$

$V_t = 0.7 V$

a) FIND C_{ox} & k_n'

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-11}\ F/m}{8 \times 10^{-9}\ m} = 4.31 \times 10^{-3}\ F/m^2$$

$$= 4.31\ fF/\mu m^2$$

$$k_n' = \mu_n C_{ox} = \left(450\ \frac{cm^2}{V \cdot s}\right)\left(4.31 \times 10^{-3}\ F/m^2\right)$$

$$k_n' = \left(450 \times 10^8\ \frac{\mu m^2}{V \cdot s}\right)\left(4.31\ \frac{fF}{\mu m^2}\right) = \boxed{194\ \frac{\mu A}{V^2}}$$

b) $\frac{W}{L} = \frac{8\ \mu m}{0.8\ \mu m}$ $\qquad V_{ov} = V_{GS} - V_t$

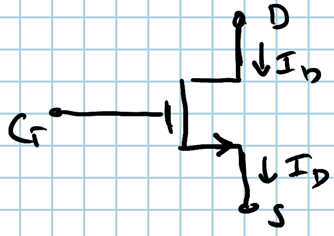
$$I_D = \frac{1}{2} \underbrace{\mu_n C_{ox}}_{k_n'} \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$100\ \mu A = \frac{1}{2}\left(194\ \frac{\mu A}{V^2}\right)\left(\frac{8}{0.8}\right)(V_{GS} - V_t)^2 \Rightarrow (V_{GS} - V_t)^2 = 103.09 \times 10^{-3}\ V^2$$

$$V_{GS} - V_t = 0.321\ V$$

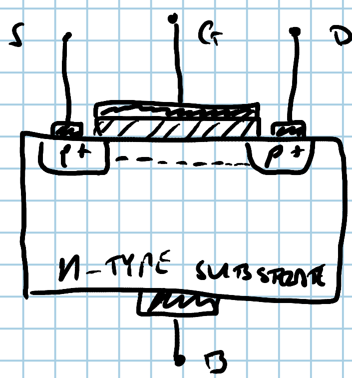
$$\boxed{V_{GS} = 1.021 V}$$

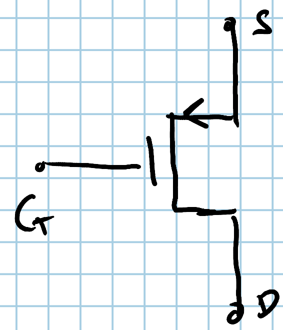
NMOS TRANSISTOR



p-CHANNEL MOSFET

- n-TYPE SUBSTRATE
- DRAIN & SOURCE ≡ p^+ MAT'L ⇒ HOLES ARE MAJORITY CHARGE CARRIERS.
- OPERATION IS SIMILAR TO NMOS EXCEPT: - V_{GS} & V_{DS} ARE NEG.
  - V_t IS NEG.





$i_D - v_{DS}$ characteristics (NMOS)