Design of an INS aided high dynamic GPS Receiver

Ma Xiaoyong
School of Instrument Science and Opto-electronics Engineering
Beihang University
Beijing, China
Maxiaoyong1985@yahoo.com.cn

Liu Baiqi
School of Instrument Science and Opto-electronics Engineering
Beihang University
Beijing, China

***Abstract*—GPS receiver tracking loop will loose lock easily in high dynamic environments. The velocity of INS (inertial navigation system) aided GPS receiver may advance the tracking loop in a high performance and improve anti-jamming capability. In this paper, the design of FPGA and DSPs based software receiver is described. In this system, The INS processor is embedded in the GPS receiver, so the velocity of INS would be used to aid the receiver in tracking loop. This system consists of two parts, a front-end circuit and a digital signal processor circuit. The GPS satellite's signal reaches the receivers through an antenna, and then is converted into IF signal (for intermediate frequency signal) by the front-end circuit, those signals enter the next stage of digital signal processing. Inertial signals shifts to signals processing stage through the serial port. Inertial navigation solution is finished in the receivers, and then loop aiding is achieved. The digital signal processer was composed of one FPGA and two DSPs, the FPGA was receiver's correlation channel, one DSPs is GPS navigation processor the other is INS processor, the two DSPs communicate by their HPI interface. The experiment indicates that this design has a high performance positioning result, and is significant for the realization of deep coupled SINS/GPS integration.**

Keywords- GPS receiver; INS aided; DSPs; front-end

I. INTRODUCTION

High dynamic GPS receivers as the important user equipment of Global Positioning System are wildly used in the key areas related to national defense such as Missile & Satellite and national economy. The design of tracking loop which would determine the receiver's dynamic performance is the core step of the receiver. The recent study indicated that INS velocity providing the GPS receiver tracking loops would improve the receivers' performance of high dynamic and high Signal-to-Noise ratio[1]. The Draper laboratory of United States of America proved that the deep integration of SINS/GPS system would advance 15dB of anti-jamming performance than ecumenical system in 2000, and applied for a patent in 2001. Some domestic institutes of our country such as Beijing University of Aeronautics and Astronautics have done the simulation studies. However, there are no reports about practical application.

In the high dynamic condition, the Doppler frequency would evidently augment. In order to track the signal, the bandwidth of the phase lock loop must enlarge corresponding, and simultaneity more noise appears in the loop. As a result, the measuring precision result will fall down. So the bandwidth of the PLL and the measuring precision are contrary. If the INS information could be introduced into the GPS receiver and eliminate frequency shifting caused by carrier's dynamic, the contradiction between the bandwidth of the PLL and SNR[2-4]. In this paper, the design of a dual-DSPs and FPGA based GPS receiver is described, and the inertial navigation system processing is completed in the receivers.

II. SYSTEM OVERVIEW

This project to build a GPS receiver using an FPGA for the base-band processing function was started with the aim of providing a general purpose GPS research platform with INS aided. In this paper we focus on the RF front end design, the interface of FPGA and DSPs and the dual DSPs function assigned.

In the project we selected the chip of TMS320c6416 of Texas Instruments as the main GPS receiver processor and another DSP chip TMS320C6747 of Texas Instruments for INS calculation and the FPGA chosen for this project was an EP3C120F484 in a 484 pin BGA package from the Altera Cyclone III family. FIGURE 1 shows the overall architecture of the receiver.

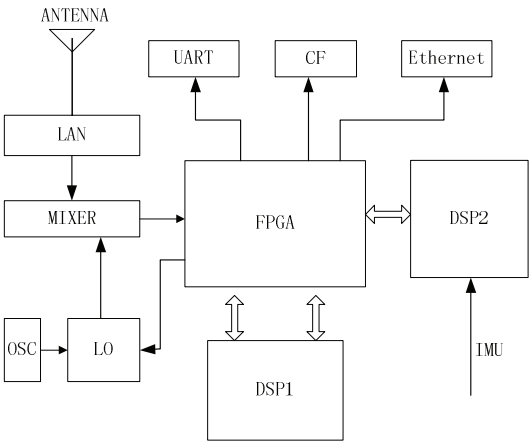

Figure 1. GPS receiver architecture

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A. The RF front end

The GPS signal received by the antenna is about -130dB and 1575.42MHz of L1 frequency, it is difficult to be sampled by a base-band processor. The RF front end is to down convert its frequency and amplify the signal. The RF front end composes of law noise amplifier (LNA), local oscillator (LO), and mixer, filters and AGC detector. The LNA is the first stage after the antenna, the main requirement in this area of a receiver is to have the highest gain with the lowest noise. The LO is used to create the local signal from a oscillator for the mixer, and the mixer multiply the received signal and the LO out signal. In order to down convert the GPS signal a low pass filter is needed. Take this process twice or three times the received GPS signal can be down to an Intermediate Frequency (IF), which could be disposed by a digital processor.

In this paper, we designed a two down conversions RF front end. We selected the SI4133 chip as the LO which creates two local signals for the mixer to down convert the received signal, selected the chip MAX2681 of MAXIM used for the first down conversion which converted the signal to 374MHz, and selected the chip ADL5350 for the second down conversions to get the final IF signal out of 12.92MHz. In order to avoid the A/D converter flood out or cannot detect signal an AGC used can control the power of the signal in a valuable range. See figure.2.

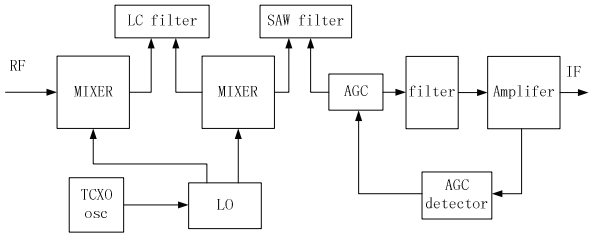

Figure 2. architecture of RF front end

B. Digital signal processor

The analog IF signals from the RF front end, being converted by A/D, are sent to digital correlator for related calculation. The correlator's functions operate in FPGA, GPS signal first multiply with the carrier wave where local generated, got two signals I and Q, after that the carrier signal has only Doppler frequency leave behind. In the base-band there are three local CA code generated: early, prevent and late signal, which all multiply with I and Q signal, get six signals: I_E, I_P, I_L, Q_E, Q_P, Q_L, these were the output of the correlator. The architecture of the correlator sees figure.3.

The output of the correlator entry the DSPs used for decode signal, get pseudorange and computed user position, control of the base-band (FPGA) in the DSPs as well. In this project, the DSPs chip TMS320C6416 we selected has 600MHz work frequency, can do floating-point, which can comfortably do the GPS signal procession. The interface of the DSPs and FPGA is DSP Extended Memory Interface (EMIF), which has a 64 width for the DSPs EMIFA, 32 bit was used to connect FPGA the address is 20 bit. A no flash of 64M was connected to DSPs EMIFB which carry the DSPs boot program and save the latest ephemeris data.

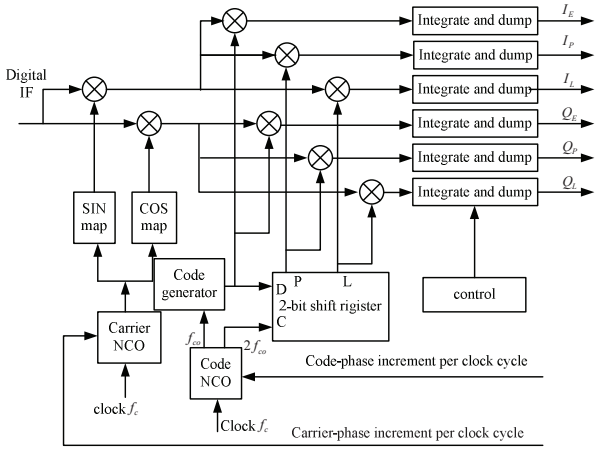

Figure 3. Correlator architecture

Another DSPs was used for aiding the tracking loop, which was designed to do SINS calculation. By its host post interface (HPI) connected to GPS processor, so its result can be read expeditious by the other DSP as the GPS processor. The connections see figure.4.

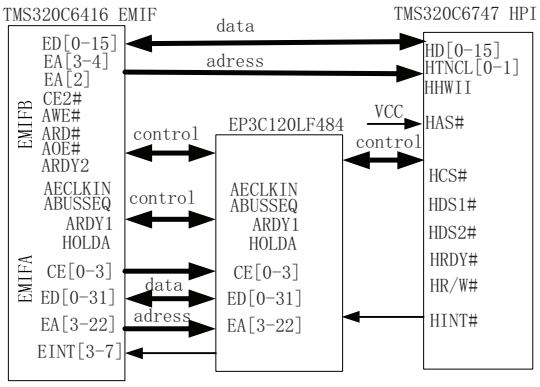

Figure 4. system connection

III. THEORY OF INS AIDED

A. Architecture of INS aided tracking loop

Inside the GPS receiver, delay lock loop (DLL) is used to track CA code, and it is Costas phase lock loop (PLL) that the carrier phase loop. And it is much easier for the PLL to lose lock than DLL. PLL is used to help DLL so that the DLL can be designed much simpleness. In the high dynamic condition, the Costas PLL will lose lock because the Doppler frequency is too much. So the INS velocity aiding is needed[5]. In that case the carrier loop can work at high SNR with a narrow bandwidth. The architecture of the loop sees figure.5.

In the figure, $\frac{k}{s+k}$ is the filter for INS, k is the parameter of the filter, the rank of the filter is two. $F(s)=\frac{s\tau_2+1}{s\tau_2}$, $\theta_i(s)$ is input, $w(s)$ is extend input phase noise, $e(s)$ is frequency aided error which come from INS velocity error and clock drift error[6].

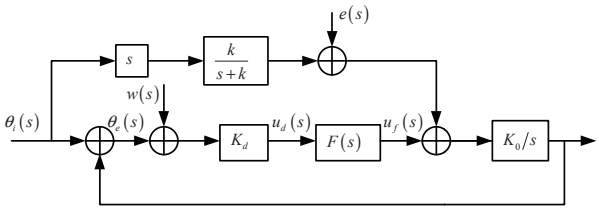

Figure 5. INS aided loop architecture

In this project the velocity used for aiding tracking loop comes from INS processor. Doppler frequency is direct proportion with the relativity velocity between GPS satellite and the receiver antennal, which has a relation as,

$$f_d = \frac{1}{\lambda}(V_{RS} - V_S)\, I_S \tag{1}$$

In the equation, λ is the wavelength of the GPS carrier wave, V_{RS} is the user speed, V_S is satellite speed, I_S is the unit vector from GPS satellite to user antennal.

B. Bandwidth and Tracking character

From fig.5 we can conclude the transfer function of the aided tracking loop[7],

$$H(s) = \frac{\left[(1+k)+K\tau\right]s^2 + (K+Ka\tau)s + Ka}{\tau s^3 + (1+K\tau)s^2 + (K+Ka\tau)s + Ka} \tag{2}$$

And the error equation,

$$H_e(s) = \frac{s^2}{s^2 + Ks + Ka}\,\frac{\tau s + k}{\tau s + 1} \tag{3}$$

Loop bandwidth,

$$B_L = \int_0^{\infty} \left|H(jw)\right|^2 df \tag{4}$$

When the parameter K and a are fixed, bandwidth is concluded by k and τ, See Table.1.

TABLE I. RELATIONSHIP BETWEEN B_L

B_L and k, τ ($=20$, $=10.1$)

τ =0.001		K =0.001	
k	B_L	τ	B_L
0.001	259.501	0.001	259.501
0.01	255.025	0.01	34.917
0.02	250.099	0.02	22.353
0.06	230.892	0.06	13.564
0.20	169.901	0.16	10.211
0.70	31.288	0.18	9.949
0.90	10.495	0.32	8.968
0.95	8.391	0.70	8.213
0.97	7.896	0.76	8.161
0.98	7.723	0.90	8.065
0.99	7.599	0.99	8.017

The conclusions from the table 1 are as follows: as k and τ are increasing, effective bandwidth of the loop will deceasing rapidly; the higher the precision of the INS velocity is, the better the aiding performance becomes.

IV. EXPRIMENTRESULT

The experiments include static and kinematic, we can get the positioning error from the static and test the dynamic performance from kinematic. Figure 6 is the positioning error and figure 7 is velocity error. the coordinate is local ENU.

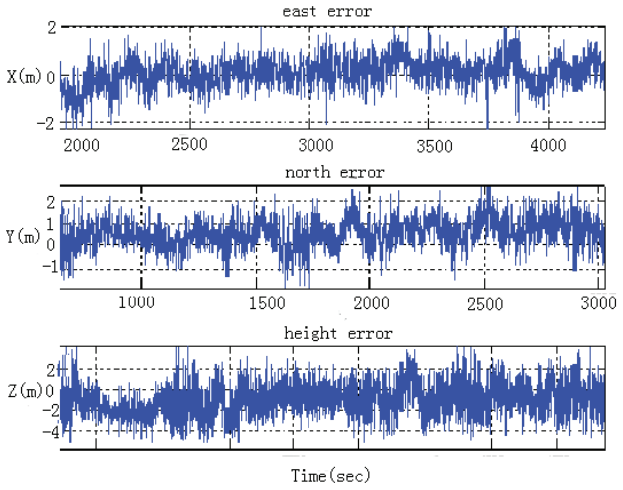

Figure 6. position error

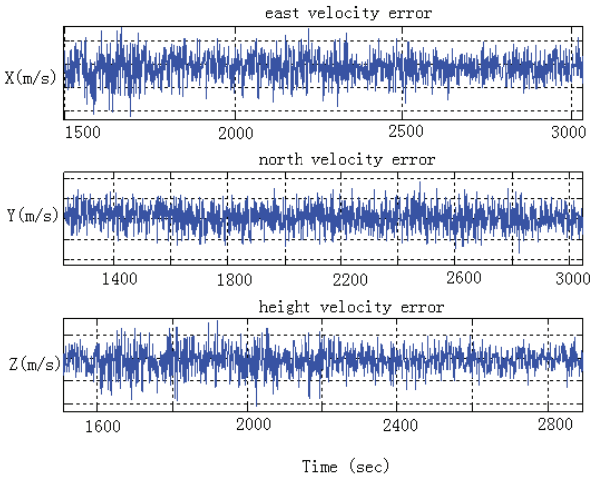

Figure 7. velocity error

CONCLUTION

In this paper, we developed an INS-aided GPS receiver use universal digital signal processor and FPGA, and realized GPS signal acquisition and track. In order to track high dynamic GPS signal, an INS processor was added in our receiver, and

the velocity is used to aid the tracking loop. The structure of the aided tracking loop was analyzed, and indicated the advantage of used INS to aided GPS. Some experiment was designed to test the performance of our design, and it indicated that the receiver can work successfully.

Because the vehicle-mounted experiment can't get a speed high enough, so the advantage of the INS aided loop didn't reflected. So in the future we must take new experimental method to accomplish the result.

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