

# **Mobile 5th Generation Intel® Core™ Processor Family I/O, Intel® Core™ M Processor Family I/O, Mobile Intel® Pentium® Processor Family I/O, and Mobile Intel® Celeron® Processor Family I/O**

**Datasheet**

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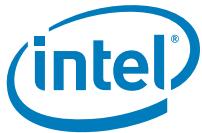
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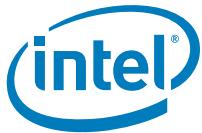
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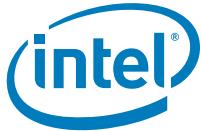
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# Revision History

Revision Number	Description	Revision Date
001	<ul style="list-style-type: none"><li>Initial Release</li></ul>	September 2014
002	<ul style="list-style-type: none"><li>Minor Updates throughout for clarity</li></ul> <p><b>Chapter 2</b></p> <ul style="list-style-type: none"><li>Table 2.9. Updated INTRUDER# description</li></ul> <p><b>Chapter 3</b></p> <ul style="list-style-type: none"><li>Table 3-2, "Power Plane and States for Output and I/O Signals for Configurations". Note 22 has been updated</li></ul> <p><b>Chapter 8</b></p> <ul style="list-style-type: none"><li>8.1.24.10.1. Updated Description for bits 14:8</li></ul> <p><b>Chapter 13</b></p> <ul style="list-style-type: none"><li>Table 13-3. Updated PORTSCNUUSB3 and PORTPMSCN Address Offset</li><li>13.2.1.3. Updated Bits 31:24 description</li><li>13.2.2.10. Updated Address offset</li><li>13.2.2.11. Updated Address offset</li><li>13.2.2.12. Updated Address offset</li><li>13.2.2.13. Updated Address offset</li><li>13.2.2.14. Added PORTLIX—USB 3.0 Port X Link Info Register</li></ul>	October 2014
003	<ul style="list-style-type: none"><li>Added U-Processor<ul style="list-style-type: none"><li>Mobile 5th Generation Intel® Core™ Processor Family I/O</li><li>Mobile Intel® Pentium® Family I/O</li><li>Mobile Intel® Celeron® Family I/O</li></ul></li><li>Replaced "Y-Processor Line" with "Intel® Core™ M processor"</li><li>Minor updates throughout for clarity.</li></ul>	January 2015
004	<p><b>Chapter 5</b></p> <ul style="list-style-type: none"><li>5.22.6. Updated paragraph</li><li>5.23.2. Added fourth bullet</li></ul> <p><b>Chapter 17</b></p> <ul style="list-style-type: none"><li>Table 17.1. Updated to add PEC2 Register</li><li>17.1.72. Added section - PEC2 Register</li></ul>	February 2015

§ §



# 1 *Introduction*

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This document is the Datasheet for the Mobile 5th Generation Intel® Core™ processor family I/O, Intel® Core™ M processor family I/O, Mobile Intel® Pentium® processor family I/O, and Mobile Intel® Celeron® processor family I/O Platform Controller Hub (PCH).

The 5th Generation Intel® Core™ processor family, Intel® Core™ M processor family, Mobile Intel® Pentium® processor family, and Mobile Intel® Celeron® processor family are designed for a one-chip platform. The processor includes this low-power PCH die that is in the same package as the processor die. For further details, refer to the processor Datasheet, Volume 1 of 2 (See [Table 1-1](#), document number 330834).

## 1.1 *About this Manual*

This document is intended for Original Equipment Manufacturers (OEMs) and BIOS vendors creating products based on the 5th Generation Intel® Core™ processor family, Intel® Core™ M processor family, Mobile Intel® Pentium® processor family, and Intel® Celeron® processor family (See [Section 1.3](#) for SKU definitions and supported features).

**Note:** Throughout this document the Platform Controller Hub (PCH) is used as a general term and refers to all Mobile 5th Generation Intel® Core™ processor family I/O, Intel® Core™ M processor family I/O, Mobile Intel® Pentium® processor family I/O, and Intel® Celeron® processor family I/O SKUs, unless specifically noted otherwise.

**Note:** Throughout this document, the Mobile 5th Generation Intel® Core™ processor family I/O, Mobile Intel® Pentium® processor family I/O, and Mobile Intel® Celeron® processor family I/O may be referred to as "**U-Processor Line**".

This manual assumes a working knowledge of the vocabulary and principles of interfaces and architectures such as Peripheral Component Interface Express\* (PCIe\*), Universal Serial Bus (USB), Advance Host Controller Interface (AHCI), Serial ATA (SATA), Intel® High Definition Audio (Intel® HD Audio), System Management Bus (SMBus), Advance Configuration Power Interface (ACPI), and Low Pin Count (LPC) Interface. Although some details of these features are described within this manual, refer to the individual industry specifications listed in [Table 1-1](#) for the complete details.

All PCI buses, devices and functions in this manual are abbreviated using the following nomenclature; Bus:Device:Function. This manual abbreviates buses as *Bn*, devices as *Dn* and functions as *Fn*. For example Device 31 Function 0 is abbreviated as D31:F0, Bus 1 Device 8 Function 0 is abbreviated as B1:D8:F0. Generally, the bus number will not be used, and can be considered to be Bus 0.

**Table 1-1. Related Documents**

Document	Location / Document Number
<b>Industry Standard Documents</b>	
<i>PCI Express* Base Specification, Revision 2.0</i>	<a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>
<i>Low Pin Count Interface Specification, Revision 1.1 (LPC)</i>	<a href="http://developer.intel.com/design/chipsets/industry/lpc.htm">http://developer.intel.com/design/chipsets/industry/lpc.htm</a>
<i>System Management Bus Specification, Version 2.0 (SMBus)</i>	<a href="http://www.smbus.org/specs/">http://www.smbus.org/specs/</a>
<i>PCI Local Bus Specification, Revision 2.3 (PCI)</i>	<a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>
<i>PCI Power Management Specification, Revision 1.2</i>	<a href="http://www.pcisig.com/specifications">http://www.pcisig.com/specifications</a>
<i>Universal Serial Bus Specification (USB), Revision 3.0</i>	<a href="http://www.usb.org/developers/docs">http://www.usb.org/developers/docs</a>
<i>Advanced Configuration and Power Interface, Version 4.0a (ACPI)</i>	<a href="http://www.acpi.info/spec.htm">http://www.acpi.info/spec.htm</a>
<i>Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0 (EHCI)</i>	<a href="http://developer.intel.com/technology/usb/ehcispec.htm">http://developer.intel.com/technology/usb/ehcispec.htm</a>
<i>eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.0</i>	<a href="http://www.intel.com/technology/usb/xhcispec.htm">http://www.intel.com/technology/usb/xhcispec.htm</a>
<i>Serial ATA Specification, Revision 3.10</i>	<a href="http://www.serialata.org/">http://www.serialata.org/</a>
<i>Serial ATA II: Extensions to Serial ATA 1.0, Revision 1.0</i>	<a href="http://www.serialata.org">http://www.serialata.org</a>
<i>Serial ATA II Cables and Connectors Volume 2 Gold</i>	<a href="http://www.serialata.org">http://www.serialata.org</a>
<i>Alert Standard Format Specification, Version 1.03</i>	<a href="http://www.dmtf.org/standards/asf">http://www.dmtf.org/standards/asf</a>
<i>IEEE 802.3 Fast Ethernet</i>	<a href="http://standards.ieee.org/getieee802/">http://standards.ieee.org/getieee802/</a>
<i>AT Attachment - 6 with Packet Interface (ATA/ATAPI - 6)</i>	<a href="http://T13.org">http://T13.org (T13 1410D)</a>
<i>IA-PC HPET (High Precision Event Timers) Specification, Revision 1.0a</i>	<a href="http://www.intel.com/content/www/us/en/software-developers/software-developers-hpet-spec-1-0a.html">http://www.intel.com/content/www/us/en/software-developers/software-developers-hpet-spec-1-0a.html</a>
<i>TPM Specification 1.3</i>	<a href="http://www.trustedcomputinggroup.org/specs/TPM">http://www.trustedcomputinggroup.org/specs/TPM</a>
<i>Intel® Virtualization Technology Transforms IT</i>	<a href="http://www.intel.com/technology/virtualization/index.htm">http://www.intel.com/technology/virtualization/index.htm</a>
<i>SFF-8485 Specification for Serial GPIO (SGPIO) Bus, Revision 0.7</i>	<a href="ftp://ftp.seagate.com/sff/SFF-8485.PDF">ftp://ftp.seagate.com/sff/SFF-8485.PDF</a>
<i>Serial ATA Advanced Host Controller Interface (AHCI) Revision 1.3</i>	<a href="http://www.intel.com/content/www/us/en/io/serial-ata/serial-ata-ahci-spec-rev1_3.html">http://www.intel.com/content/www/us/en/io/serial-ata/serial-ata-ahci-spec-rev1_3.html</a>
<i>Intel® High Definition Audio Specification, Revision 1.0</i>	<a href="http://www.intel.com/content/www/us/en/standards/standards-high-def-audio-specs-general-technology.html">http://www.intel.com/content/www/us/en/standards/standards-high-def-audio-specs-general-technology.html</a>
<b>Intel® Specific Documents</b>	
<i>5th Generation Intel® Core™ Processor Family, Intel® Core™ M Processor Family, Mobile Intel® Pentium® Processor Family, and Mobile Intel® Celeron® Processor Family Datasheet Volume 1 of 2</i>	330834
<i>5th Generation Intel® Core™ Processor Family, Intel® Core™ M Processor Family, Mobile Intel® Pentium® Processor Family, and Mobile Intel® Celeron® Processor Family Datasheet Volume 2 of</i>	330835



### 1.1.1 Chapter Descriptions

#### Chapter 1, "Introduction"

Chapter 1 introduces the Platform Controller Hub (PCH). This chapter provides information on the organization of the manual and gives a general overview of the PCH.

#### Chapter 2, "Signal Description"

Chapter 2 provides a block diagram of the PCH and a detailed description of each signal. Signals are arranged according to interface and details are provided as to the drive characteristics (Input/Output, Open Drain, and so on) of all signals.

#### Chapter 3, "Platform Controller Hub (PCH) Pin States"

Chapter 3 provides a complete list of signals, their associated power well, their logic level in each suspend state, and their logic level before and after reset.

#### Chapter 4, "PCH and System Clocks"

Chapter 4 provides a list of each clock domain associated with the PCH.

#### Chapter 5, "Functional Description"

Chapter 5 provides a detailed description of the functions in the PCH.

#### Chapter 6, "Electrical Characteristics"

Chapter 6 provides all AC and DC characteristics including detailed timing diagrams.

#### Chapter 7, "Register and Memory Mapping"

Chapter 7 provides an overview of the registers, fixed I/O ranges, variable I/O ranges and memory ranges decoded by the PCH.

#### Chapter 8, "Chipset Configuration Registers"

Chapter 8 provides a detailed description of registers and base functionality that is related to Chipset configuration. It contains the root complex register block, which describes the behavior of the upstream internal link.

#### Chapter 9, "Gigabit LAN Configuration Registers"

Chapter 9 provides a detailed description of registers that reside in the PCH's integrated LAN controller. The integrated LAN Controller resides at Device 25, Function 0 (D25:F0).

#### Chapter 10, "LPC Interface Bridge Registers (D31:F0)"

Chapter 10 provides a detailed description of registers that reside in the LPC bridge. This bridge resides at Device 31, Function 0 (D31:F0). This function contains registers for many different units within the PCH including DMA, Timers, Interrupts, Processor Interface, GPIO, Power Management, System Management and RTC.

#### Chapter 11, "SATA Controller Registers (D31:F2)"

Chapter 11 provides a detailed description of registers that reside in the SATA controller #1. This controller resides at Device 31, Function 2 (D31:F2).

#### Chapter 12, "EHCI Controller Registers (D29:F0)"

Chapter 12 provides a detailed description of registers that reside in the EHCI host controller. This controller resides at Device 29, Function 0 (D29:F0).

#### Chapter 13, "xHCI Controller Registers (D20:F0)"

Chapter 13 provides a detailed description of registers that reside in the xHCI. This controller resides at Device 20, Function 0 (D20:F0).



[Chapter 14, "Integrated Intel® High Definition Audio \(Intel® HD Audio\) Controller Registers"](#)

Chapter 14 provides a detailed description of registers that reside in the Intel® High Definition Audio controller. This controller resides at Device 27, Function 0 (D27:F0).

[Chapter 15, "SMBus Controller Registers \(D31:F3\)"](#)

Chapter 15 provides a detailed description of registers that reside in the SMBus controller. This controller resides at Device 31, Function 3 (D31:F3).

[Chapter 16, "High Precision Event Timer Registers"](#)

Chapter 16 provides a detailed description of registers that reside in the multi-media timer memory mapped register space.

[Chapter 17, "PCI Express\\* Configuration Registers"](#)

Chapter 17 provides a detailed description of registers that reside in the PCI Express controller. This controller resides at Device 28, Functions 0 to 7 (D28:F0-F7).

[Chapter 18, "Serial Peripheral Interface \(SPI\)"](#)

Chapter 18 provides a detailed description of registers that reside in the SPI memory mapped register space.

[Chapter 19, "Thermal Sensor Registers \(D31:F6\)"](#)

Chapter 19 provides a detailed description of registers that reside in the thermal sensors PCI configuration space. The registers reside at Device 31, Function 6 (D31:F6).

[Chapter 20, "Intel® Management Engine \(Intel® ME\) Subsystem Registers \(D22:F\[3:0\]\)"](#)

Chapter 20 provides a detailed description of registers that reside in the Intel® ME controller. The registers reside at Device 22, Functions 0 to 3 (D22:F0-F3).

[Chapter 21, "Intel® Serial I/O DMA Controller Registers \(D21:F0\)"](#)

Chapter 21 provides a detailed description of registers that reside in the Intel® Serial I/O DMA controller. The registers reside at Device 21, Function 0 (D21:F0).

[Chapter 22, "Intel® Serial I/O I2C\\* Controller Registers \(D21:F1/F2\)"](#)

Chapter 22 provides a detailed description of registers that reside in the Intel® Serial I/O I<sup>2</sup>C controller. The registers reside at Device 21, Function 1 and Function 2 (D21:F1-F2).

[Chapter 23, "Intel® Serial I/O Generic SPI \(GSPI\) Controller Registers \(D21:F3/F4\)"](#)

Chapter 23 provides a detailed description of registers that reside in the Intel® Serial I/O Generic SPI controller. The registers reside at Device 21, Function 3 and Function 4 (D21:F3-F4).

[Chapter 24, "Intel® Serial I/O SDIO Controller Registers \(D23:F0\)"](#)

Chapter 24 provides a detailed description of registers that reside in the Intel® Serial I/O Secure Digital I/O (SDIO) controller. The registers reside at Device 21, Function 5 and Function 6 (D21:F5-F6).

[Chapter 25, "Intel® Serial I/O UART Controller Registers \(D21:F5/F6\)"](#)

Chapter 25 provides a detailed description of registers that reside in the Intel® Serial I/O UART controller. The registers reside at Device 23, Function 0 (D23:F0).

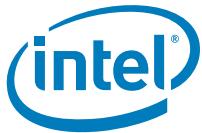


## 1.2 Overview

The PCH provides extensive I/O support. Functions and capabilities include:

- *PCI Express\* Base Specification*, Revision 2.0 support for up to six ports with transfers up to 5 GT/s
- ACPI Power Management Logic Support, Revision 4.0a
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controller with independent DMA operation on up to four ports
- xHCI USB controller provides support for up to 10-USB 2.0 ports and 4-USB 3.0 ports. New USB debug port support on xHCI controller.
- One legacy EHCI USB controller with USB debug port support.
- Flexible I/O—Allows some high speed I/O signals to be configured as PCIe\*, SATA or USB 3.0.
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- *System Management Bus (SMBus) Specification*, Version 2.0 with additional support for I<sup>2</sup>C devices
- Supports Intel® High Definition Audio (Intel® HD Audio)
- Supports Intel® Smart Sound Technology (Intel® SST)
- Supports Intel® Rapid Storage Technology (Intel® RST)
  - The PCH supports Intel RST for PCIe Storage that allows for PCIe SSDs to be used with Intel RST features. See [Section 1.3](#) for details on SKU feature availability.
- Supports Intel®Rapid Storage Technology for PCIe\* Storage
- Supports Intel® Active Management Technology (Intel® AMT)
- Supports Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Supports Intel® Trusted Execution Technology (Intel® TXT)
- Integrated Clock Controller
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- One Serial Peripheral Interface (SPI) support for flash
- Two general purpose Serial Peripheral Interface (SPI) controllers for various serial devices like sensors and TPM
- Intel® Anti-Theft Technology (Intel® AT)
- JTAG Boundary Scan support
- Two integrated Intel® Serial I/O I<sup>2</sup>S Host controllers
- Two integrated Intel® Serial I/O I<sup>2</sup>C Host controllers
- Two integrated Intel® Serial I/O UART Host controllers
- One Intel® Serial I/O Secure Digital I/O Host controller supporting Wireless LAN only
- One Intel® Serial I/O DMA Host controller

**Note:** Not all functions and capabilities may be available on all SKUs. See [Section 1.3](#) for details on SKU feature availability.



## 1.2.1 Capability Overview

The following sub-sections provide an overview of the PCH capabilities.

### PCI Express\* Interface

The PCH provides up to 6 PCI Express Root Ports, supporting the *PCI Express Base Specification*, Revision 2.0. Each Root Port x1 lane supports up to 5Gb/s bandwidth in each direction (10Gb/s concurrent). PCI Express Root Ports 1-4 can independently be configured to support multiple port width configurations (that is, 4x1, 2x1 and 1x2, 1x2 and 2x1, 1x4). PCI Express Root Ports 5 and 6 can each be configured as 1x1, 1x2, or 1x4 respectively. See [Section 1.3](#) for details on feature availability.

### Serial ATA (SATA) Controller

The PCH SATA controller has one integrated SATA host controller that supports independent DMA operation for up to four ports and supports data transfer rates of up to 6Gb/s on all ports. The PCH SATA controller contains one mode of operation—AHCI mode using memory space, and it also supports RAID mode. The PCH SATA controller no longer supports legacy mode using I/O space. Therefore, AHCI software is required. The PCH supports Serial ATA Specification, Revision 3.1.

See [Section 1.3](#) for details on feature availability.

### Advanced Host Controller Interface (AHCI)

The PCH SATA controller provides hardware support for Advanced Host Controller Interface (AHCI), a standardized programming interface for SATA host controllers. Platforms supporting AHCI may take advantage of performance features such as port independent DMA Engines—each device is treated as a master—and hardware-assisted native command queuing. AHCI also provides usability enhancements such as hot-plug and advanced power management. AHCI requires appropriate software support (such as an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware. Visit the Intel web site for current information on the AHCI specification.

### Intel® Rapid Storage Technology (Intel® RST)

The PCH SATA controller provides support for Intel® Rapid Storage Technology, providing both AHCI (see above for details on AHCI) and integrated RAID functionality. The RAID capability provides high-performance RAID 0, 1, 5, and 10 functionality on up to 4 SATA ports of the PCH SATA controller. Matrix RAID support is provided to allow multiple RAID levels to be combined on a single set of hard drives, such as RAID 0 and RAID 1 on two disks. Other RAID features include hot spare support, SMART alerting, and RAID 0 auto replace. Software components include an Option ROM for pre-boot configuration and boot functionality, a Microsoft® Windows® compatible driver, and a user interface for configuration and management of the RAID capability of PCH SATA controller. See [Section 1.3](#) for details on SKU feature availability.

### Intel® Rapid Storage Technology (Intel® RST) for PCI Express\* Storage

Intel® Rapid Storage Technology for PCIe Storage is supported on high-speed ports 11 and 12 (See [Section 5.20](#) for details on Flexible I/O). This capability allows the Intel RST driver to support a PCIe storage device connected to high speed ports 11 and 12 (PCIe x2 connection). The PCIe x1 devices are not supported.



### Intel® Smart Response Technology

Intel® Smart Response Technology is a disk caching solution that can provide improved computer system performance with improved power savings. It allows configuration of a computer system with the advantage of having HDDs for maximum storage capacity with system performance at or near SSD performance levels. See [Section 1.3](#) for details on SKU feature availability.

### Low Pin Count (LPC) Interface

The PCH implements an LPC Interface as described in the *LPC 1.1 Specification*. The Low Pin Count (LPC) bridge function of the PCH is mapped as PCI D31:F0 and supports a memory size up to 8MB, two master/DMA devices, interrupt controllers, timers, power management, system management, Super I/O, and RTC.

### Serial Peripheral Interface (SPI) for Flash

In addition to the standard Dual Output Fast Read mode, the SPI interface in the PCH supports Dual I/O Fast Read, Quad I/O Fast Read and Quad Output Fast Read. To enable the Quad I/O operation modes, all data transfer signals in the interface are bi-directional and two new signals (SPI\_IO2 and SPI\_IO3) have been added to the basic four-wire interface: Clock, Master Out Slave In (MOSI), Master In Slave Out (MISO) and active-low chip selects (CS#). The PCH supports three chip selects: SPI\_CS0# and SPI\_CS1# are used to access two separate SPI Flash components. SPI\_CS2# is dedicated only to support TPM on SPI (TPM can be configured through PCH soft straps to operate over LPC or SPI, but no more than 1 TPM is allowed in the system). SPI\_CS2# may not be used for any purpose other than TPM.

The SPI Flash Controller supports running instructions at 20 MHz, 33 MHz, and 50 MHz and can be used by the PCH for BIOS code, to provide Chipset configuration settings, integrated Gigabit Ethernet MAC/PHY configuration and Intel® Management Engine (Intel® ME) settings. The SPI Flash Controller supports the Serial Flash Discoverable Parameter (SFDP) JEDEC\* standard, which provides a consistent way of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. The SPI Flash Controller queries these parameter tables to discover the attributes to enable divergent features from multiple SPI part vendors, such as Quad I/O Fast Read capabilities or device storage capacity, among others.

### Intel Serial I/O General Purpose Serial Peripheral Interface (SPI)

Two general purpose SPI interfaces are implemented to support many devices which use serial protocols for transferring data such as sensors on the platform. These are full-duplex synchronous serial interfaces, which operate in master mode only, and supports up to 25Mb/s. Serial data formats may range from 4- to 32-bits in length. Each interface consists of 4 wires: a clock (CLK), a chip select (CS), and 2 data lines (MOSI and MISO). The signals are multiplexed with GPIO pins.

### Compatibility Modules (Timer/Counters, Interrupt Controller)

The timer/counter block contains three counters that are equivalent in function to those found in one 8254 programmable interval timer. These three counters are combined to provide the system timer function, and speaker tone. The 24 MHz xtal is used to generate the 14.318 MHz clock source for these three counters.

The PCH provides an ISA-compatible Programmable Interrupt Controller (PIC) that incorporates the functionality of two 8259 interrupt controllers. The two interrupt controllers are cascaded so that 14 external and two internal interrupts are possible. In addition, the PCH supports a serial interrupt scheme.

All of the registers in these modules can be read and restored. This is required to save and restore system state after power has been removed and restored to the platform.

### **Advanced Programmable Interrupt Controller (APIC)**

In addition to the standard ISA-compatible Programmable Interrupt controller (PIC) described in the previous section, the PCH incorporates the Advanced Programmable Interrupt Controller (APIC).

### **Universal Serial Bus (USB) Controllers**

The PCH contains one eXtensible Host Controller Interface (xHCI) controller and one Enhanced Host Controller Interface (EHCI) controller. The xHCI controller is mapped as PCI D20:F0 and it supports up to 10 (based on select SKU) USB 2.0 ports and 4-USB 3.0 ports.

EHCI controller 1 (EHCI1) is located at D29:F0 and it supports up to 8-USB 2.0 ports. USB 2.0 Ports 8 and 9 will only be routed to the xHCI controller and will not have the option of being routed to an EHCI controller. The Debug Port capability is available on the EHCI controller Port 1 and on all of the USB 3.0 ports.

**Note:** USB 2.0 differential pairs are numbered starting with 0. USB 3.0 differential pairs are numbered starting with 1.

See [Section 1.3](#) for details on feature availability.

**Note:** Regarding the optional USB Battery Charging Specification 1.x: Intel® does not have a topology for the Mobile 5th Generation Intel® Core™ processor family I/O, Intel® Core™ M processor family I/O, Mobile Intel® Pentium® processor family I/O, Mobile Intel® Celeron® processor family I/O based platforms that can accommodate USB battery charging circuits robustly across the large install base of USB cables and High Speed (HS) devices. As such, Intel does not recommend that platforms exceed native supply currents defined in the USB specification for USB 2.0 ports.

### **Flexible I/O**

Flexible I/O is an architecture that allows some high speed signals to be configured as SATA, USB 3.0, or PCIe\* signals. Through soft straps, the functionality on these multiplexed signals are selected to meet the I/O needs on the platform. See [Section 5.20](#) for details.

### **Gigabit Ethernet Controller**

The Gigabit Ethernet Controller provides a system interface using a PCI function. The controller provides a full memory-mapped or I/O mapped interface along with 64-bit address master support for systems using more than 4GB of physical memory. The Gigabit Ethernet Controller also provides DMA (Direct Memory Addressing) mechanisms for high performance data transfers. Its bus master capabilities enable the component to process high-level commands and perform multiple operations; this lowers processor utilization by off-loading communication tasks from the processor. Two large configurable transmit and receive FIFOs (up to 20KB each) help prevent data underruns and overruns while waiting for bus accesses. This enables the Gigabit Ethernet Controller to transmit data with minimum interframe spacing (IFS).



The Gigabit Ethernet Controller can operate at multiple speeds (10/100/1000MB/s) and in either full duplex or half duplex mode. In full duplex mode the Gigabit Ethernet Controller adheres with the *IEEE 802.3x Flow Control* Specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism. See [Section 5.3](#) for details.

### Intel® Serial I/O I<sup>2</sup>C\* Controllers

There are two I<sup>2</sup>C controllers for two independent I<sup>2</sup>C interfaces. Each interface is a two-wire I<sup>2</sup>C serial interface consisting of a serial data line and a serial clock. The interface supports standard mode (up to 100Kb/s), fast mode (up to 400Kb/s), and fast mode plus (up to 1MB/s). The interface operates in I<sup>2</sup>C master mode only and supports 7-bit or 10-bit addressing. All I<sup>2</sup>C signals are multiplexed with GPIOs.

### Intel® Serial I/O UART Controllers

The PCH integrates two UART controllers supporting up to 3.8MBit/s. The controllers are based on the 16550 industry standard providing the following supports:

- Programmable character properties, such as number of data bits per characters, optional parity bit and number of stop bits.
- Line break generation and detection.
- DMA signaling with two programmable mode.
- Prioritized interrupt identification.
- Programmable FIFO enable/disable.
- Programmable serial data baud rate.

All UART signals are multiplexed with GPIOs.

### Intel® Serial I/O Secure Digital I/O Controller

The PCH implements a single SDIO interface that is only intended for connection to an external Wireless LAN controller. The interface supports SDIO Default Speed (12.5MB/s) and SDR25 (25MB/s) modes of operation. The interface supports both DMA mode (32-bit only) and non-DMA mode, and can operate at either 1.8V or 3.3V. If the supported speed is 25MB/s or 50MB/s, the voltage must be at 1.8V. All SDIO signals are multiplexed with GPIOs.

For systems where the Wireless LAN is connected to another bus such as PCIe\* or USB, the SDIO interface is expected to be disabled. SDIO does not support Intel® AMT.

### Real-Time Clock (RTC)

The PCH contains a Motorola MC146818B-compatible real-time clock with 256 bytes of battery-backed RAM. The real-time clock performs two key functions—keeping track of the time of day and storing system data, even when the system is powered down. The RTC operates on a 32.768 KHz crystal and a 3V battery.

The RTC also supports two lockable memory ranges. By setting bits in the configuration space, two 8-byte ranges can be locked to read and write accesses. This prevents unauthorized reading of passwords or other system security information.

The RTC also supports a date alarm that allows for scheduling a wake up event up to 30 days in advance, rather than just 24 hours in advance.

## GPIO

Various general purpose inputs and outputs are provided for custom system design. The number of inputs and outputs varies depending on PCH configuration.

## Enhanced Power Management

The PCH's power management functions fully support the *Advanced Configuration and Power Interface (ACPI) Specification*, Revision 4.0a, and include enhanced clock control and various low-power (suspend) states (such as Suspend-to-RAM and Suspend-to-Disk). A hardware-based thermal management circuit permits software-independent entrance to low-power states.

## Intel® Active Management Technology (Intel® AMT)

Intel® AMT is a fundamental component of Intel® vPro™ technology. Intel® AMT is a set of advanced manageability features developed as a direct result of IT customer feedback gained through Intel® market research. With the advent of powerful tools like the Intel® System Defense Utility, the extensive feature set of Intel® AMT easily integrates into any network environment. See [Section 1.3](#) for details on SKU feature availability.

## Manageability

In addition to Intel® AMT, The PCH integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

- **TCO Timer**—The PCH's integrated programmable TCO timer is used to detect system locks. The first expiration of the timer generates an SMI# that the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.
- **Processor Present Indicator**—The PCH looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the PCH will reboot the system.
- **ECC Error Reporting**—When detecting an ECC error, the host controller has the ability to send one of several messages to the PCH. The host controller can instruct the PCH to generate either an SMI#, NMI, SERR#, or TCO interrupt.
- **Function Disable**—The PCH provides the ability to disable most integrated functions, including integrated LAN, USB, LPC, Intel® HD Audio, SATA, PCI Express and SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.
- **Intruder Detect**—The PCH provides an input signal (INTRUDER#) that can be used to inform the system in the event of the case being opened. The PCH can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

## System Management Bus (SMBus 2.0)

The PCH contains an SMBus Host interface that allows the processor to communicate with SMBus slaves. This interface is compatible with most I<sup>2</sup>C devices. Special I<sup>2</sup>C commands are implemented.



The PCH SMBus host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). Also, the PCH supports slave functionality, including the Host Notify protocol. Hence, the host controller supports eight command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification*, version 2.0): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify.

The PCH SMBus also implements hardware-based Packet Error Checking for data robustness and the Address Resolution Protocol (ARP) to dynamically provide addresses to all SMBus devices.

### **Intel® High Definition Audio (Intel® HD Audio) Controller**

The Intel® High Definition Audio controller is a PCI Express\* device, configured as D27:F0. The PCH Intel® HD Audio controller supports up to 4 codecs, such as audio and modem codecs. The link can operate at either 3.3V or 1.5V.

With the support of multi-channel audio stream, 32-bit sample depth, and sample rate up to 192 KHz, the Intel® HD Audio controller provides audio quality that can deliver Consumer Electronics (such as home audio components, portable audio devices, Bluetooth\* speakers, and so on) levels of audio experience. On the input side, the PCH adds support for an array of microphones.

### **Intel® Virtualization Technology for Directed I/O (Intel® VT-d)**

The PCH provides hardware support for implementation of Intel® Virtualization Technology with Directed I/O (Intel® VT-d). Intel® VT-d Technology consists of technology components that support the virtualization of platforms based on Intel® Architecture processors. Intel® VT-d Technology enables multiple operating systems and applications to run in independent partitions. A partition behaves like a virtual machine (VM) and provides isolation and protection across partitions. Each partition is allocated its own subset of host physical memory.

### **JTAG Boundary-Scan**

The PCH implements the industry standard Joint Test Action Group (JTAG) interface and enables Boundary-Scan. Boundary-Scan can be used to ensure device connectivity during the board manufacturing process. The JTAG interface allows system manufacturers to improve efficiency by using industry available tools to test the PCH on an assembled board. Since JTAG is a serial interface, it eliminates the need to create probe points for every pin in an XOR chain. This eases pin breakout and trace routing and simplifies the interface between the system and a bed-of-nails tester.

**Note:** The TRST# JTAG signal is an optional signal in the IEEE\* 1149 JTAG Specification and is not implemented in the PCH.

### **Integrated Clock Controller**

The PCH contains an Integrated Clock Controller (ICC) that generates various platform clocks from a 24 MHz crystal source. The ICC contains PLLs, Modulators and Dividers for generating various clocks suited to the platform needs. The ICC supplies up to six 100 MHz PCI Express 2.0 Specification compliant clocks, one 100 MHz PCI Express 2.0 Specification compliant clock to the processor core, one 24 MHz for the processor core, one 100 MHz PCI Express\* 2.0 Specification compliant clock for ITP, one 135 MHz differential output clock for Integrated Graphics Display on the processor, and two 24 MHz single-ended clocks for LPC devices.



### Serial Over LAN (SOL) Function

This function supports redirection of keyboard and text screens to a terminal window on a remote console. The keyboard and text redirection enables the control of the client machine through the network without the need to be physically near that machine. Text and keyboard redirection allows the remote machine to control and configure a client system. The SOL function emulates a standard PCI device and redirects the data from the serial port to the management console using the integrated LAN.

### Intel® KVM Technology

Intel® KVM technology provides enhanced capabilities to its predecessor—SOL. In addition to the features set provided by SOL, Intel® KVM technology provides mouse and graphic redirection across the integrated LAN. Unlike SOL, Intel® KVM technology does not appear as a host accessible PCI device but is instead almost completely performed by Intel® AMT Firmware with minimal BIOS interaction. The Intel® KVM technology feature is only available with internal graphics.

### IDE-R Function

The IDE-R function is an IDE Redirection interface that provides client connection to management console ATA/ATAPI devices such as hard disk drives and optical disk drives. A remote machine can setup a diagnostic software or OS installation image and direct the client to boot an IDE-R session. The IDE-R interface is the same as the IDE interface although the device is not physically connected to the system and supports the ATA/ATAPI-6 specification. IDE-R does not conflict with any other type of boot and can instead be implemented as a boot device option. The Intel® AMT solution will use IDE-R when remote boot is required. The device attached through IDE-R is only visible to software during a management boot session. During normal boot session, the IDE-R controller does not appear as a PCI present device.

## 1.3 SKU Definition

**Table 1-2. Mobile 5th Generation Intel® Core™ Processor Family I/O, Mobile Intel® Pentium® Processor Family I/O, and Intel® Celeron® Processor Family I/O SKUs (U-Processor Line) (Sheet 1 of 2)**

Feature Set	SKU Name	
	Premium	Base
Flexible I/O	Yes	Yes
Total Number of PCI Express* 2.0 Lanes	Up to 12 <sup>5</sup>	Up to 10 <sup>5</sup>
•PCI Express 2.0 Ports	Up to 6 <sup>5</sup>	Up to 6 <sup>5</sup>
Total number of USB ports	8	8
•USB 3.0 Capable Ports	Up to 4 <sup>6</sup>	Up to 4 <sup>6</sup>
Total number of SATA ports	Up to 4 <sup>7</sup>	2 <sup>8</sup>
Intel® Rapid Storage Technology	AHCI	Yes
	RAID 0/1/5/10 Support	Yes
	Intel® Smart Response Technology <sup>9</sup>	Yes
	Intel® Rapid Storage Technology for PCIe* Storage	Yes
Intel® Active Management Technology 10.0	Yes	No



**Table 1-2. Mobile 5th Generation Intel® Core™ Processor Family I/O, Mobile Intel® Pentium® Processor Family I/O, and Intel® Celeron® Processor Family I/O SKUs (U-Processor Line) (Sheet 2 of 2)**

Feature Set	SKU Name	
	Premium	Base
Intel® Small Business Advantage <sup>10</sup>	Yes	No
Intel® Rapid Start Technology <sup>11</sup>	Yes	No
Intel® Identity Protection Technology (Intel® IPT) <sup>12</sup>	Yes	Yes
Near Field Communication	Yes	Yes

**Notes:**

1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
2. Table 1-2 shows feature difference between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs.
3. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe\*-to-PCI bridge. See Section 5.1.2 for more details.
4. Flexible I/O is available on High Speed I/O ports 3 and 4 which are shared between USB 3.0 and PCI Express. Flexible I/O ports 11-14 are shared between SATA Gen 3 and PCI Express. See Table 1-3.
5. The total number of PCI Express lanes and ports available depends on the Flexible I/O configuration. See Table 1-3.
6. There are 2 dedicated USB 3.0 ports. Up to 4-USB 3.0 ports requires High Speed I/O ports 3 and 4 to be configured as USB 3.0. See Table 1-3.
7. Up to 4 SATA ports require Flexible I/O ports 11-14 to be configured as SATA. See Table 1-3.
8. High Speed I/O ports 13-14 will be dedicated as 2 SATA 6Gb/s ports. See Table 1-3.
9. Intel® Smart Response Technology requires an Intel® Core™ processor.
10. Intel® Small Business Advantage requires an Intel® Core™ processor.
11. Intel® Rapid Start Technology requires an Intel® Core™ processor.
12. Intel® Identity Protection Technology requires an Intel® Core™ processor.

**Table 1-3. Mobile 5th Generation Intel® Core™ Processor Family I/O, Mobile Intel® Pentium® Processor Family I/O, and Intel® Celeron® Processor Family I/O SKUs—Flexible I/O Map (U-Processor Line)**

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1	PCIe* Port 2							PCIe* Port 6 Lane 0 SSD <sup>1</sup>	PCIe* Port 6 Lane 1 SSD <sup>1</sup>	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD <sup>1</sup>	PCIe* Port 6 Lane 1 SSD <sup>1</sup>	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1	PCIe* Port 2										

**Note:**

1. Denotes support for Intel® Rapid Storage Technology for PCIe\* Storage. This feature can support up to x2 PCIe\* SSD. The PCH can support up to x4 PCIe\* SSD without the added benefit of the Intel® Rapid Storage Technology.

**Table 1-4. Intel® Core™ M Processor I/O Platform SKUs**

Feature Set	SKU Name
	Premium
Flexible I/O	Yes
Total Number of PCI Express* 2.0 Lanes	Up to 12 <sup>5</sup>
•PCI Express 2.0 Ports	Up to 6 <sup>5</sup>
Total number of USB ports	10 <sup>13</sup>
•USB 3.0 Capable Ports	Up to 4 <sup>6</sup>
Total number of SATA ports	Up to 4 <sup>7</sup>
Intel® Rapid Storage Technology	AHCI
	RAID 0/1/5/10 Support
	Intel® Smart Response Technology <sup>9</sup>
	Intel® Rapid Storage Technology for PCIe* Storage
Intel® Active Management Technology 10.0	Yes
Intel® Small Business Advantage <sup>10</sup>	Yes
Intel® Rapid Start Technology <sup>11</sup>	Yes
Intel® Identity Protection Technology (Intel® IPT) <sup>12</sup>	Yes
Near Field Communication	Yes

**Notes:**

1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
2. Table 1-4 shows feature difference between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs.
3. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe\*-to-PCI bridge. See Section 5.1.2 for more details.
4. Flexible I/O is available on High Speed I/O ports 3 and 4 which are shared between USB 3.0 and PCI Express. Flexible I/O ports 11-14 are shared between SATA Gen 3 and PCI Express. See Table 1-5.
5. The total number of PCI Express lanes and ports available depends on the Flexible I/O configuration. See Table 1-5.
6. There are 2 dedicated USB 3.0 ports. Up to 4-USB 3.0 ports requires High Speed I/O ports 3 and 4 to be configured as USB 3.0. See Table 1-5.
7. Up to 4 SATA ports require Flexible I/O ports 11-14 to be configured as SATA. See Table 1-5.
8. N/A
9. Intel® Smart Response Technology requires an Intel® Core™ processor.
10. Intel® Small Business Advantage requires an Intel® Core™ processor.
11. Intel® Rapid Start Technology requires an Intel® Core™ processor.
12. Intel® Identity Protection Technology requires an Intel® Core™ processor.
13. 10 USB2 port functionality is only available on xHCl. EHCI can support up to 8 USB2 ports.

**Table 1-5. Intel® Core™ M Processor I/O Platform SKUs—Flexible I/O Map**

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1	PCIe* Port 2							PCIe* Port 6 Lane 0 SSD <sup>1</sup>	PCIe* Port 6 Lane 1 SSD <sup>1</sup>	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3

**Note:**

1. Denotes support for Intel® Rapid Storage Technology for PCIe\* Storage. This feature can support x2 PCIe\* SSD only.

## 1.4

## Device and Revision ID Table

The Revision ID (RID) register is an 8-bit register located at offset 08h in the PCI header of every PCI/PCIe\* function. The RID register is used by software to identify a particular component stepping when a driver change or patch unique to that stepping is needed.

**Table 1-6. PCH Device and Revision ID Table (Sheet 1 of 2)**

Device Function	Description	Dev. ID	B2 SRID	Comments	
D31:F2	SATA (Note 1)	9C83h	03h	SATA Controller (AHCI)	
		9C85h	03h	SATA Controller (RAID Mode)	
		282Ah	03h	SATA Controller (RAID Mode) - Alternate ID	
		9C87h	03h	SATA Controller (RAID Mode) - Premium	
		282Ah	03h	SATA Controller (RAID Mode) - Premium- Alternate ID	
		9C8Fh	03h	SATA Controller (RAID 1/RRT Only)	
D28:F0	PCI Express* (Note 3)	9C90h	03h	PCI Express Port 1 (When D28:F0:ECh:bit 1 = 0)	
		2448h	03h	PCI Express Port 1 (When D28:F0:ECh:bit 1 = 1)	
D28:F1		9C92h	03h	PCI Express Port 2 (When D28:F0:ECh:bit 1 = 0)	
		2448h	03h	PCI Express Port 2 (When D28:F0:ECh:bit 1 = 1)	
D28:F2		9C94h	03h	PCI Express Port 3 (When D28:F0:ECh:bit 1 = 0)	
		2448h	03h	PCI Express Port 3 (When D28:F0:ECh:bit 1 = 1)	
D28:F3		9C96h	03h	PCI Express Port 4 (When D28:F0:ECh:bit 1 = 0)	
		2448h	03h	PCI Express Port 4 (When D28:F0:ECh:bit 1 = 1)	
D28:F4		9C98h	03h	PCI Express Port 5 (When D28:F0:ECh:bit 1 = 0)	
		2448h	03h	PCI Express Port 5 (When D28:F0:ECh:bit 1 = 1)	
D28:F5		9C9Ah	03h	PCI Express Port 6 (When D28:F0:ECh:bit 1 = 0)	
		2448h	03h	PCI Express Port 6 (When D28:F0:ECh:bit 1 = 1)	
D27:F0	Intel® High Definition Audio	9CA0h	03h	High Definition Audio Controller - All SKUs.	
D31:F3	SMBus	9CA2h	03h	SMBus Controller - All SKUs.	
D31:F6	Thermal	9CA4h	03h	Thermal Controller - All SKUs.	
D29:F0	USB EHCI	9CA6h	03h	USB EHCI Controller - All SKUs.	
D20:F0	USB xHCI	9CB1h	03h	USB xHCI Controller - All SKUs.	
D25:F0	LAN (Note 2)	155Ah	03h	LAN Controller - All SKUs.	
D23:F0	SDIO	9CB5h	03h	Intel® Serial I/O Secure Digital I/O Controller - All SKUs.	
D19:F0	Intel® Smart Sound Technology	9CB6h	03h	Smart Sound Technology Controller - All SKUs.	
D22:F0	Intel® ME Interface #1	9CBAh	03h	Intel® ME Interface #1 Controller - All SKUs.	
D22:F1	Intel® ME Interface #2	9CBBh	03h	Intel® ME Interface #2 Controller - All SKUs.	
D22:F2	IDE-R	9CBCh	03h	Intel® ME Interface IDE-R Controller - All SKUs.	

**Table 1-6. PCH Device and Revision ID Table (Sheet 2 of 2)**

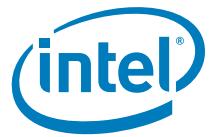
Device Function	Description	Dev. ID	B2 SRID	Comments	
D22:F3	KT	9CBDh	03h	Intel® ME Interface KT Controller - All SKUs.	
D31:F0	LPC	9CC1h	03h	LPC Controller (Full Featured Engineering Sample with U-Processor Line).	
		9CC2h	03h	LPC Controller (Full Featured Engineering Sample with U-Processor Line).	
		9CC3h	03h	LPC Controller (Premium SKU with U-Processor Line)	
		9CC5h	03h	LPC Controller (Base SKU with U-Processor Line)	
		9CC6	03h	LPC Controller (Full Featured Engineering Sample with the Intel® Core™ M processor).	
		9CC7h	03h	LPC Controller (Premium SKU with the Intel® Core™ M processor)	
		9CC9h	03h	LPC Controller (Base SKU with the Intel® Core™ M processor)	
D21:F0	Serial I/O	9CE0h	03h	Intel® Serial I/O DMA Controller	
D21:F1		9CE1h	03h	Intel® Serial I/O I <sup>2</sup> C Controller #0	
D21:F2		9CE2h	03h	Intel® Serial I/O I <sup>2</sup> C Controller #1	
D21:F3		9CE5h	03h	Intel® Serial I/O GSPI Controller #0	
D21:F4		9CE6h	03h	Intel® Serial I/O GSPI Controller #1	
D21:F5		9CE3h	03h	Intel® Serial I/O UART Controller #0	
D21:F6		9CE4h	03h	Intel® Serial I/O UART Controller #1	
<b>Notes:</b>					
1. The SATA RAID Controller Device ID is dependent upon the AIE bit setting (bit 7 of D31:F2:Offset 9Ch).					
2. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 1E33h is used. Refer to the appropriate Intel® GbE physical layer Transceiver (PHY) datasheet for LAN Device IDs.					
3. This table shows the default PCI Express Function Number-to-Root Port mapping. Function numbers for a given root port are assignable through the "Root Port Function Number and Hide for PCI Express Root Ports" register (RCBA+0404h).					
4. For a given stepping, not all SKUs may be available.					



## 1.5 Platform Controller Features

- NEW: Supports Intel® Rapid Storage Technology for PCIe\* Storage
- NEW: Windows\* InstantGo Power Save Mode (Windows\* InstantGo PSM)
- NEW (Intel® Core™ M processor): Ability to individually power gate the MPHY interfaces (PCIe\* SATA, USB 3.0)
- Intel® Smart Sound Technology (Intel® SST)
- Two integrated Intel® Serial I/O I<sup>2</sup>C\* Controllers
- Two integrated Intel® Serial I/O I<sup>2</sup>S Controllers
- Two integrated Intel® Serial I/O Universal Asynchronous Receive and Transmit (UART) Controllers
- One Intel® Serial I/O Secure Digital I/O (SDIO) Controller
- One Intel® Serial I/O DMA Controller
- Flexible I/O
  - An architecture that allows some high speed I/O signals to be configured as SATA, USB 3.0, or PCIe\*
- PCI Express\*
  - Up to six PCI Express root ports and up to twelve PCI Express Lanes
  - Supports PCI Express Rev 2.0 running at up to 5.0 GT/s
  - PCI Express root ports can independently be configured to support multiple port configurations (x1, x2, and x4 lanes)
  - Module-based hot-plug supported (that is, ExpressCard\*)
  - Latency Tolerance Reporting
  - Optimized Buffer Flush/Fill
- Integrated Serial ATA Host Controller
  - Up to four SATA ports
  - Data transfer rates supported: 6.0Gb/s, 3.0Gb/s, and 1.5Gb/s on all ports
  - Integrated AHCI controller
- External SATA support on all ports
  - 3.0Gb/s and 1.5Gb/s support
  - Port Disable Capability
- Intel® Rapid Storage Technology
  - Configures the PCH SATA controller as a RAID controller supporting RAID 0/1/5/10
- Intel® Smart Response Technology
- Intel® High Definition Audio Interface
  - PCI Express endpoint
  - Independent Bus Master logic for eight general purpose streams: four input and four output
  - Support four external Codecs
  - Supports variable length stream slots
  - Supports multichannel, 32-bit sample depth, 192 KHz sample rate output
  - Provides microphone array support
  - Allows for non-48 KHz sampling output
  - Support for ACPI Device States
  - Low Voltage
- USB
  - xHCI Host Controller, supports up to 10 USB 2.0 connections and up to 4 SuperSpeed USB 3.0 connections
  - One EHCI Host Controller, supporting up to eight external USB 2.0 ports
  - Support for dynamic power gating and Intel® Power Management Framework (PMF)
  - Per-Port-Disable Capability
  - Includes one EHCI and four xHCI Debug Ports
  - Supports wake-up from sleeping states S1 – S4
- Integrated Gigabit LAN Controller
  - Connection utilizes PCI Express pins
  - Integrated ASF Management Controller
  - Supports IEEE 802.3
  - 10/100/1000Mbps Ethernet Support
  - Jumbo Frame Support
- Intel® Active Management Technology with System Defense
  - Network Outbreak Containment Heuristics
- Intel® I/O Virtualization (Intel® VT-d) Support
- Intel® Trusted Execution Technology Support
- Intel® Anti-Theft Technology
- Power Management
  - Supports Intel Power Optimizer
  - Supports ACPI 4.0a
  - ACPI-defined power states (processor driven C states)
  - ACPI Power Management Timer
  - SMI# generation
  - All registers readable/restorable for proper resume from 0 V core well suspend states
  - Support for APM-based legacy power management for non-ACPI implementations
- Integrated Clock Controller
  - Full featured platform clocking without need for a discrete clock chip
  - 6 PCIe\* 2.0 specification compliant clocks, two 24 MHz LPC clocks and one 135 MHz clock for DisplayPort\*.

§ §



## 2 Signal Description

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This chapter provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. Refer to the *5th Generation Intel® Core™ Processor Family, Intel® Core™ M Processor Family, Mobile Intel® Pentium® Processor Family, and Mobile Intel® Celeron® Processor Family Datasheet – Volume 1 of 2* (Document # 330834) for the pin listing.

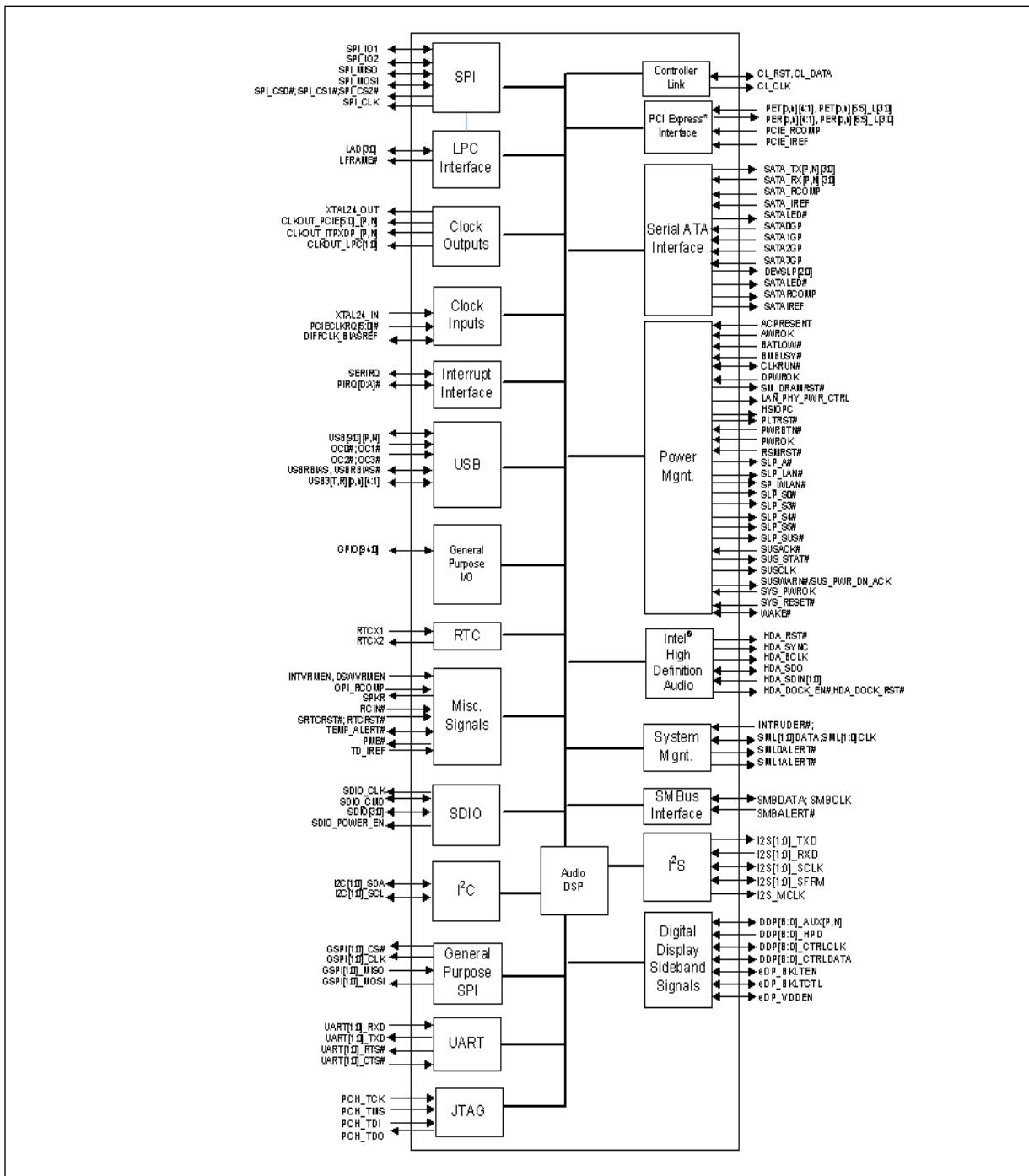
The “#” symbol at the end of the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when voltage level is high.

The following notations are used to describe the signal type:

<b>I</b>	Input Pin
<b>O</b>	Output Pin
<b>OD O</b>	Open Drain Output Pin
<b>I/OD</b>	Bi-directional Input/Open Drain Output Pin
<b>I/O</b>	Bi-directional Input/Output Pin
<b>CMOS</b>	CMOS buffers. 1.5V tolerant
<b>COD</b>	CMOS Open Drain buffers. 3.3V tolerant
<b>HVCMOS</b>	High Voltage CMOS buffers. 3.3V tolerant
<b>A</b>	Analog reference or output.

The “Type” for each signal is indicative of the functional operating mode of the signal. Unless otherwise noted in [Section 3.2](#) or [Section 3.3](#), a signal is considered to be in the functional operating mode after RTCRST# de-asserts for signals in the RTC well, after RSMRST# de-asserts for signals in the suspend well, after PCH\_PWROK asserts for signals in the core well, after DPWROK asserts for Signals in the Deep Sx well, after APWROK asserts for Signals in the Active Sleep well.

Core Well: Core well includes 1.05V, 1.5V and 3.3V rails. PCH logic on these rails may be shut off in S3, S4, S5, Deep Sx and G3 states.

**Figure 2-1. PCH Interface Signals Block Diagram (Not all Signals are on all SKUs)**


**Note:** Some of these signals may be multiplexed. Refer to the signal description tables for more details.

## 2.1 Flexible I/O

Flexible I/O, a new architecture to allow some high speed signals to be configured as PCIe\*, USB 3.0, or SATA signals. Through soft straps, the functionality on these multiplexed signals are selected to meet I/O needs on the platform. [Table 2-1](#) illustrates high speed I/O ports mapping to PCIe\*, USB 3.0, and SATA signals.

**Table 2-1. I/O Flexibility Signal Mapping**

High Speed I/O Ports	GbE Map	PCIe* Signals	USB 3.0 Signals	SATA Signals
1	—	—	USB3Tp1, USB3Tn1 USB3Rp1, USB3Rn1	—
2	—	—	USB3Tp2, USB3Tn2 USB3Rp2, USB3Rn2	—
3	—	PETp1, PETn1 PERp1, PERn1	USB3Tp3, USB3Tn3 USB3Rp3, USB3Rn3	—
4	—	PETp2, PETn2 PERp2, PERn2	USB3Tp4, USB3Tn4 USB3Rp4, USB3Rn4	—
5	000 (soft strap <sup>6</sup> )	PETp3, PETn3 PERp3, PERn3	—	—
6	001 (soft strap <sup>6</sup> )	PETp4, PETn4 PERp4, PERn4	—	—
7	010 (soft strap <sup>6</sup> )	PETp5_L0, PETn5_L0 PERp5_L0, PERn5_L0	—	—
8	011 (soft strap <sup>6</sup> )	PETp5_L1, PETn5_L1 PERp5_L1, PERn5_L1	—	—
9	100 (soft strap <sup>6</sup> )	PETp5_L2, PETn5_L2 PERp5_L2 PERn5_L2	—	—
10	101 (soft strap <sup>6</sup> )	PETp5_L3, PETn5_L3 PERp5_L3, PERn5_L3	—	—
11	—	PETp6_L0, PETn6_L0 PERp6_L0, PERn6_L0	—	SATA_TXP3, SATA_TXN3 SATA_RXP3, SATA_RXN3
12	—	PETp6_L1, PETn6_L1 PERp6_L1, PERn6_L1	—	SATA_TXP2, SATA_TXN2 SATA_RXP2, SATA_RXN2
13	—	PETp6_L2, PETn6_L2 PERp6_L2 PERn6_L2	—	SATA_TXP1, SATA_TXN1 SATA_RXP1, SATA_RXN1
14	—	PETp6_L3, PETn6_L3 PERp6_L3, PERn6_L3	—	SATA_TXP0, SATA_TXN0 SATA_RXP0, SATA_RXN0

**Notes:**

1. High speed I/O ports 3 and 4 can be configured as either PCIe\* port 1 and 2 or USB 3.0 ports 3 and 4.
2. High speed I/O ports 14 to 12 can be configured as either PCIe\* port 6 Lanes 3 to 1 or SATA ports 2 to 0.
3. Maximum of 6 PCIe\* ports, 4-USB 3.0 Ports or 4 SATA ports are possible.
4. GbE can only be used on PCIe\* ports 3, 4, or 5.
5. Refer to [Table 5-41](#) for more details.
6. Soft strap located at PCHSTRP9.GBE\_PCIEPORTSEL.

## 2.2 USB Interface

- Note:** No external pull-up/pull-down resistors are required for USB signals. USB ports not needed can be left floating as **No Connect**.
- Note:** See [Section 1.3](#) for details on SKU feature availability.
- Note:** All USB 2.0 register addresses throughout the EDS correspond to the external pin names. [Table 2-2](#) shows how the USB pins are mapped to the different internal ports within the xHCI and EHCI controllers.
- Note:** When USBr is enabled in the xHCI, USB port 10 will be the USBr port for both the U-Processor Line and Intel® Core™ M processor SKUs. USB port 10 address offset is +520h.

**Table 2-2. USB Interface Signals (Sheet 1 of 3)**

Name	xHCIPort	EHCI Port	Type	Description
USB2p0 USB2n0	0	0	I/O	<b>USB 2.0 Port 0 Transmit/Receive Differential Pair 0:</b> This USB 2.0 signal pair can be routed to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p1 USB2n1	1	1	I/O	<b>USB 2.0 Port 1 Transmit/Receive Differential Pair 1:</b> This USB 2.0 signal pair can be routed to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p2 USB2n2	2	2	I/O	<b>USB 2.0 Port 2 Transmit/Receive Differential Pair 2:</b> This USB 2.0 signal pair can be routed to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p3 USB2n3	3	3	I/O	<b>USB 2.0 Port 3 Transmit/Receive Differential Pair 3:</b> This USB 2.0 signal pair can be routed to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p4 USB2n4	4	4	I/O	<b>USB 2.0 Port 4 Transmit/Receive Differential Pair 4:</b> This USB 2.0 signal pair can be routed to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p5 USB2n5	5	5	I/O	<b>USB 2.0 Port 5 Transmit/Receive Differential Pair 5:</b> This USB 2.0 signal pair can be routed to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p6 USB2n6	6	6	I/O	<b>USB 2.0 Port 6 Transmit/Receive Differential Pair 6:</b> This USB 2.0 signal pair can be mapped to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p7 USB2n7	7	7	I/O	<b>USB 2.0 Port 7 Transmit/Receive Differential Pair 7:</b> This USB 2.0 signal pair can be mapped to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p8 USB2n8	8	-	I/O	<b>USB 2.0 Port 8 Transmit/Receive Differential Pair 8:</b> This USB 2.0 signal pair can be mapped to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2p9 USB2n9	9	-	I/O	<b>USB 2.0 Port 9 Transmit/Receive Differential Pair 9:</b> This USB 2.0 signal pair can be mapped to xHCI or EHCI Controller through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.

Table 2-2. USB Interface Signals (Sheet 2 of 3)

Name	xHCI Port	EHCI Port	Type	Description
USB3Tp1 USB3Tn1	1	-	O	<b>USB 3.0 Differential Transmit Pair 1:</b> These are USB 3.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #1 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 3.
USB3Rp1 USB3Rn1	1	-	I	<b>USB 3.0 Differential Receive Pair 1:</b> These are USB 3.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #1 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 3.
USB3Tp2 USB3Tn2	2	-	O	<b>USB 3.0 Differential Transmit Pair 2:</b> These are USB 3.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #2 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 3.
USB3Rp2 USB3Rn2	2	-	I	<b>USB 3.0 Differential Receive Pair 2:</b> These are USB 3.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #2 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 3.
USB3Tp3 USB3Tn3	3	-	O	<b>USB 3.0 Differential Transmit Pair 3:</b> These are USB 3.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #3 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 3.  <b>Note:</b> Use FITC to set the soft straps that select this port as USB 3.0 Port 3. Default configuration is PCIe*.
USB3Rp3 USB3Rn3	3	-	I	<b>USB 3.0 Differential Receive Pair 3:</b> These are USB 3.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #3 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 3.  <b>Note:</b> Use FITC to set the soft straps that select this port as USB 3.0 Port 3. Default configuration is PCIe*.
USB3Tp4 USB3Tn4	4	-	O	<b>USB 3.0 Differential Transmit Pair 4:</b> These are USB 3.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #4 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 3.  <b>Note:</b> Use FITC to set the soft straps that select this port as USB 3.0 Port 4. Default configuration is PCIe*.
USB3Rp4 USB3Rn4	4	-	I	<b>USB 3.0 Differential Receive Pair 4:</b> These are USB 3.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #4 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 3.  <b>Note:</b> Use FITC to set the soft straps that select this port as USB 3.0 Port 4. Default configuration is PCIe*.

**Table 2-2. USB Interface Signals (Sheet 3 of 3)**

Name	xHCI Port	EHCI Port	Type	Description
<b>OC0#/</b> GPIO40 <b>OC1#/</b> GPIO41 <b>OC2#/</b> GPIO42 <b>OC3#/</b> GPIO43	-	-	I	<p><b>Overcurrent Indicators:</b> These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred.</p> <p>OC[3:0]# pins may optionally be used as GPIOs.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. OC pins are 3.3V tolerant.</li> <li>2. Sharing of OC pins is required to cover all 10 USB connectors but no more than 1 OC line may be connected to a USB connector.</li> <li>3. OC[3:0]# should be connected with USB 2.0 ports 0–9 and any 4 of USB 3.0 ports 1–4.</li> </ol>
USBRBIAS	-	-	O	<b>USB Resistor Bias:</b> Analog connection point for an external resistor that is used to set transmit currents and internal load resistors. It is recommended that a $22.6 \Omega \pm 1\%$ resistor to ground be connected to this pin.
USBRBIAS#	-	-	I	<b>USB Resistor Bias Complement:</b> Analog connection point for an external resistor that is used to set transmit currents and internal load resistors. This signal should be connected directly to USBRBIAS.

## 2.3 PCI Express\*

**Table 2-3. PCI Express\* Signals (Sheet 1 of 2)**

Name	Type	Description
PETp1 PETn1	O	<p><b>PCI Express* Differential Transmit Pair 1:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #3.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as USB 3.0 Port 3. Default configuration is PCIe*.</p>
PERp1 PERn1	I	<p>PCI Express* Differential Receive Pair 1: These are PCI Express* 2.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #3.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as USB 3.0 Port 3. Default configuration is PCIe*.</p>
PETp2 PETn2	O	<p><b>PCI Express* Differential Transmit Pair 2:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #4.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as USB 3.0 Port 4. Default configuration is PCIe*.</p>
PERp2 PERn2	I	<p><b>PCI Express* Differential Receive Pair 2:</b> These are PCI Express* 2.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #4.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as USB 3.0 Port 4. Default configuration is PCIe*.</p>
PETp3 PETn3	O	<p><b>PCI Express* Differential Transmit Pair 3:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to HSIO Port #5.</p> <p><b>Note:</b> Use FITC to set the soft straps that map GbE to this PCIe* port.</p>

**Table 2-3. PCI Express\* Signals (Sheet 2 of 2)**

Name	Type	Description
PERp3 PERn3	I	<b>PCI Express* Differential Receive Pair 3:</b> These are PCI Express* 2.0-based inbound high-speed differential signals, mapped to HSIO Port #5.  <b>Note:</b> Use FITC to set the soft straps that map GbE to this PCIe* port.
PETp4 PETn4	O	<b>PCI Express* Differential Transmit Pair 4:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to HSIO Port #6.  <b>Note:</b> Use FITC to set the soft straps that map GbE to this PCIe* port.
PERp4 PERn4	I	<b>PCI Express* Differential Receive Pair 4:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to HSIO Port #6.  <b>Note:</b> Use FITC to set the soft straps that map GbE to this PCIe* port.
PETp5_L[3:0] PETn5_L[3:0]	O	<b>PCI Express* Differential Transmit Pair 5 Lane 3:0:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to HSIO ports #10-7.  <b>Note:</b> Use FITC to set the soft straps that map GbE to any of the lanes of this PCIe* port.
PERp5_L[3:0] PERn5_L[3:0]	I	<b>PCI Express* Differential Receive Pair 5 Lane 3:0:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to HSIO ports #10-7.  <b>Note:</b> Use FITC to set the soft straps that map GbE to any of the lanes of this PCIe* port.
PETp6_L[3:0] PETn6_L[3:0]	O	<b>PCI Express* Differential Transmit Pair 6 Lane 0:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to HSIO ports #14-11.  <b>Note:</b> Use FITC to set the soft straps that select the lanes of this port as SATA Ports [0:3]. Default configuration is SATA. <b>Note:</b> Use FITC to allow selection PCIe* versus SATA based on strapping of SATA[3:0]GP/GPIO[37:34].
PERp6_L[3:0] PERn6_L[3:0]	I	<b>PCI Express* Differential Receive Pair 6 Lane 0:</b> These are PCI Express* 2.0-based outbound high-speed differential signals, mapped to HSIO ports #14-11.  <b>Note:</b> Use FITC to set the soft straps that select the lanes of this port as SATA Ports [0:3]. Default configuration is SATA. <b>Note:</b> Use FITC to allow selection PCIe* versus SATA based on strapping of SATA[3:0]GP/GPIO[37:34].
PCIE_RCOMP	I	<b>Impedance Compensation Input:</b> Connected to a 3 KΩ (1%) precision external pull-up resistor to VCCUSB3PLL.
PCIE_IREF	I	<b>Internal Reference Voltage:</b> Connected to VCCUSB3PLL

## 2.4 Serial ATA (SATA) Interface

Table 2-4. Serial ATA Interface Signals (Sheet 1 of 3)

Name	Type	Description
<b>DEVSLP0/GPIO33</b>	OD O	<p><b>Serial ATA Device Sleep 0:</b> This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.</p> <p>Design Constraint: As per PDG, no external pull-up or pull-down termination required when used as DEVELP.</p> <p><b>Note:</b> This pin can be re-mapped from SATA port 0 to SATA port 3 by means of SCLKCG.P0P3_DEVSLP (D31:F2, offset 94h, bit 15) to support port 3.</p> <p><b>Note:</b> If SATA device is not present, the short window when pin is floating as GPI between power-on and BIOS programming of the pin to DEVSLP mode is negligible on this pin.</p>
<b>DEVSLP1/GPIO38</b>	OD O	<p><b>Serial ATA Device Sleep 1:</b> This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.</p> <p>Design Constraint: As per PDG, no external pull-up or pull-down termination required when used as DEVELP.</p> <p><b>Note:</b> This pin can only be mapped to SATA port 1.</p> <p><b>Note:</b> If SATA device is not present, the short window when pin is floating as GPI between power-on and BIOS programming of the pin to DEVSLP mode is negligible on this pin.</p>
<b>DEVSLP2/ GPIO39</b>	OD O	<p><b>Serial ATA Device Sleep 2:</b> This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.</p> <p>Design Constraint: As per PDG, no external pull-up or pull-down termination required when used as DEVELP.</p> <p><b>Note:</b> This pin can only be mapped to SATA port 2.</p> <p><b>Note:</b> If SATA device is not present, the short window when pin is floating as GPI between power-on and BIOS programming of the pin to DEVSLP mode is negligible on this pin.</p>
SATA_TXP0 SATA_TXN0	O	<p><b>Serial ATA Differential Transmit Pair 0:</b> These outbound SATA Port 0 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s, and are mapped to HSIO Port #14.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as PCIe* Port 6 Lane 3. Default configuration is SATA.</p> <p><b>Note:</b> Use FITC to allow selection of PCIe* versus SATA based on strapping of SATA0GP/GPIO34.</p>
SATA_RXP0 SATA_RXN0	I	<p><b>Serial ATA Differential Receive Pair 0:</b> These inbound SATA Port 0 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s, and are mapped to HSIO Port #14.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as PCIe* Port 6 Lane 3. Default configuration is SATA.</p> <p><b>Note:</b> Use FITC to allow selection of PCIe* versus SATA based on strapping of SATA0GP/GPIO34.</p>
SATA_TXP1 SATA_TXN1	O	<p><b>Serial ATA Differential Transmit Pair 1:</b> These outbound SATA Port 1 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s, and are mapped to HSIO Port #13.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as PCIe* Port 6 Lane 2. Default configuration is SATA.</p> <p><b>Note:</b> Use FITC to allow selection of PCIe* versus SATA based on strapping of SATA1GP/GPIO35.</p>

Table 2-4. Serial ATA Interface Signals (Sheet 2 of 3)

Name	Type	Description
SATA_RXP1 SATA_RXN1	I	<p>Serial ATA Differential Receive Pair 1: These inbound SATA Port 1 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s, and are mapped to HSIO Port #13.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as PCIe* Port 6 Lane 2. Default configuration is SATA.</p> <p><b>Note:</b> Use FITC to allow selection of PCIe* versus SATA based on strapping of SATA1GP/GPIO35.</p>
SATA_TXP2 SATA_TXN2	O	<p><b>Serial ATA Differential Transmit Pair 2:</b> These outbound SATA Port 2 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s, and are mapped to HSIO Port #12.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as PCIe* Port 6 Lane 1. Default configuration is SATA.</p> <p><b>Note:</b> Use FITC to allow selection of PCIe* versus SATA based on strapping of SATA2GP/GPIO36.</p>
SATA_RXP2 SATA_RXN2	I	<p><b>Serial ATA Differential Receive Pair 2:</b> These inbound SATA Port 2 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s, and are mapped to HSIO Port #12.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as PCIe* Port 6 Lane 1. Default configuration is SATA.</p> <p><b>Note:</b> Use FITC to allow selection of PCIe* versus SATA based on strapping of SATA2GP/GPIO36.</p>
SATA_TXP3 SATA_TXN3	O	<p><b>Serial ATA Differential Transmit Pair 3:</b> These outbound SATA Port 3 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s, and are mapped to HSIO Port #11.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as PCIe* Port 6 Lane 0. Default configuration is SATA.</p> <p><b>Note:</b> Use FITC to allow selection of PCIe* versus SATA based on strapping of SATA3GP/GPIO37.</p>
SATA_RXP3 SATA_RXN3	I	<p><b>Serial ATA Differential Receive Pair 3:</b> These inbound SATA Port 3 high-speed differential signals support 1.5Gb/s, 3Gb/s and 6Gb/s, and are mapped to HSIO Port #11.</p> <p><b>Note:</b> Use FITC to set the soft straps that select this port as PCIe* Port 6 Lane 0. Default configuration is SATA.</p> <p><b>Note:</b> Use FITC to allow selection of PCIe* versus SATA based on strapping of SATA3GP/GPIO37.</p>
SATA0GP/ GPIO34	I	<p><b>Serial ATA 0 General Purpose:</b> When configured as SATA0GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 0. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.</p> <p><b>Note:</b> The default use of this pin is GPIO34.</p>
SATA1GP/ SATAPHY_PC/ GPIO35	I	<p><b>Serial ATA 1 General Purpose:</b> When configured as SATA1GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 1. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.</p> <p><b>Note:</b> This pin defaults to native (out) SATAPHY_PC functionality.</p> <p><b>Note:</b> <b>(U-Processor Line)</b> SATAPHY_PC functionality should not be used. PCH Soft Strap 19 bit 31 must be programmed to '1' to change default to GPIO mode.</p>
SATA2GP/ GPIO36	I	<p><b>Serial ATA 2 General Purpose:</b> When configured as SATA2GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 2. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open.</p> <p><b>Note:</b> The default use of this pin is GPIO36.</p>

**Table 2-4. Serial ATA Interface Signals (Sheet 3 of 3)**

Name	Type	Description
SATA3GP/ GPIO37	I	<b>Serial ATA 3 General Purpose:</b> When configured as SATA3GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 3. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. <b>Note:</b> The default use of this pin is GPIO37.
SATALED#	OD O	<b>Serial ATA LED:</b> This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. <b>Note:</b> An external pull-up resistor to VCC3_3 is required.
SATA_RCOMP	I	<b>Impedance Compensation Input:</b> Connected to a 3 K $\Omega$ (1%) precision external pull-up resistor to VCCSATA3PLL through low impedance trace (<0.2 $\Omega$ ).
SATA_IREF	I	<b>Internal Reference Voltage:</b> Connected to VCCSATA3PLL

## 2.5 Low Pin Count (LPC) Interface

**Table 2-5. Low Pin Count (LPC) Interface Signals**

Name	Type	Description
LAD[3:0]	I/O	<b>LPC Multiplexed Command, Address, Data:</b> For LAD[3:0], internal pull-ups are provided.
LFRAME#	O	<b>LPC Frame:</b> LFRAME# indicates the start of an LPC cycle, or an abort.

## 2.6 Interrupt Interface

**Table 2-6. Interrupt Signals**

Name	Type	Description
SERIRQ	I/OD	<b>Serial Interrupt Request:</b> This pin implements the serial interrupt protocol. <b>Note:</b> An external pull-up required.
PIRQ[D:A]#/GPIO[80:77]	I/OD	<b>PCI Interrupt Requests:</b> In non-APIC mode, the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in <a href="#">Section 5.6.6</a> . Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts. <b>Note:</b> External pull-up of 8.2 K $\Omega$ resistor to VCC3_3 required.
<b>Note:</b> PIRQ Interrupts can only be shared if it is configured as level sensitive. They cannot be shared if configured as edge triggered.		

## 2.7 Power Management Interface

**Table 2-7. Power Management Interface Signals (Sheet 1 of 4)**

Name	Type	Description
<b>ACPRESENT/</b> GPIO31	I	<p><b>ACPRESENT:</b> This input pin indicates when the platform is plugged into AC power or not. In addition to the previous Intel® ME to EC communication, the PCH uses this information to implement the Deep Sx policies. For example, the platform may be configured to enter Deep Sx when in S4 or S5 and only when running on battery. This is powered by Deep Sx Well.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This signal is multiplexed with GPIO31 but GP31_CONFIG[0] is internally hardwired to a 1b, which means GPIO mode is permanently selected and cannot be changed.</li> <li>2. This GPIO is permanently appropriated by the Intel® ME as MGPIO2 for ACPRESENT function.</li> </ol>
APWROK	I	<b>Active Sleep Well (ASW) Power OK:</b> When asserted, indicates that power to the ASW sub-system is stable.
<b>BATLOW#/</b> GPIO72	I	<p><b>Battery Low:</b> This signal is available in Mobile package only. An input from the battery to indicate that there is insufficient power to boot the system. Assertion will prevent wake from S3-S5 state. This signal can also be enabled to cause an SMI# when asserted. For Mobile package, this signal is multiplexed with GPIO72. This signal must be tied high to the VCCDSW3_3, which will be tied to VCCSUS3_3 on Deep Sx disabled platforms.</p>
<b>BMBUSY#/</b> USB3PHY_PC/ GPIO76	I	<p><b>Bus Master Busy:</b> Generic bus master activity indication driven into the PCH. Can be configured to set the PM1_STS.BM_STS bit. Can also be configured to assert indications transmitted from the PCH to the processor using the PMSYNCH pin.</p> <p><b>Note:</b> This pin defaults to native (out) USB3PHY_PC functionality.</p> <p><b>Note:</b> <b>(U-Processor Line)</b> USB3PHY_PC functionality should not be used. PCH Soft Strap 19 bit 30 must be programmed to '1' to change default to GPI mode.</p>
CLKRUN#	I/O	<p><b>LPC Clock Run:</b> Used to support LPC CLKRUN protocol. Connects to peripherals that need to request clock restart or prevention of clock stopping.</p> <p><b>Note:</b> CLKRUN# is an optional feature for LPC TPM devices; implementation and support of this functionality with a LPC TPM device is vendor dependent</p>
DPWROK	I	<p><b>DPWROK:</b> Power OK Indication for the VCCDSW3_3 voltage rail. This input is tied together with RSMRST# on platforms that do not support Deep Sx.</p> <p><b>Note:</b> This signal is in the RTC well.</p>
(U-Processor Line): <b>HSIOPC/</b> GPIO71	O	<p><b>HSIO Power Control:</b> Used to control power to VCCHSIO, VCCUSB3PLL and VCCSATA3PLL in S0. PCH will drive HSIOPC low when all the high speed I/O controllers (xHCl, SATA, GbE and PCIe*) are idle or have no devices attached.</p> <p><b>Note:</b> This signal requires a 100 kΩ pull-up to VCC3_3 when used to control VCCHSIO, VCCUSB3PLL and VCCSATA3PLL.</p>
(Intel® Core™ M processor): <b>PCIEPHY_PC/</b> GPIO71	O	<p><b>PCIe* PHY Power Control:</b> Used to control power to VCCPCIEPHY in S0. PCH will drive PCIEPHY_PC low when PCIe* Root Ports 3-5 controllers are idle or have no devices attached.</p> <p><b>Note:</b> This signal requires a 100 kΩ pull-up to VCC3_3 when used as native functionality.</p>
<b>LAN_PHY_PWR_CTRL/</b> GPIO12	O	<p><b>LAN PHY Power Control:</b> LAN_PHY_PWR_CTRL should be connected to LAN_DISABLE_N on the PHY. PCH will drive LAN_PHY_PWR_CTRL low to put the PHY into a low power state when functionality is not needed.</p> <p><b>Note:</b> LAN_PHY_PWR_CTRL can only be driven low if SLP_LAN# is de-asserted.</p> <p><b>Note:</b> Signal can instead be used as GPIO12.</p>

**Table 2-7. Power Management Interface Signals (Sheet 2 of 4)**

Name	Type	Description
PCH_PWROK	I	<p><b>PCH Power OK:</b> When asserted, PCH_PWROK is an indication to the PCH that all of its core power rails have been stable for at least 5 ms. PCH_PWROK can be driven asynchronously. When PCH_PWROK is negated, the PCH asserts PLTRST#.</p> <p><b>Note:</b> PCH_PWROK must not glitch, even if RSMRST# is low.</p>
PLTRST#	O	<p><b>Platform Reset:</b> The PCH asserts PLTRST# to reset devices on the platform (such as SIO, FWH, LAN, processor, and so forth.). The PCH asserts PLTRST# during power-up and when software initiates a hard reset sequence through the Reset Control register (I/O port CF9h). The PCH drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O port CF9h).</p> <p><b>Note:</b> PLTRST# is in the VCCSUS3_3 well.</p> <p><b>Note:</b> PCI/PCIe* 2.0 specification requires that the power rails associated with PCI/PCIe* (typically the 3.3V, 5V, and 12V core well rails) have been valid for 100 ms prior to PLTRST# de-assertion. System designers must ensure the requirement is met on the platform.</p>
PWRBTN#	I	<p><b>Power Button:</b> The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1–S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.</p> <p><b>Note:</b> This signal is in the DSW well.</p> <p><b>Note:</b> Upon entry to S5 due to a power button override, if Deep Sx is enabled and conditions are met per <a href="#">Section 5.11.8.6</a>, the system will transition to Deep Sx.</p>
RSMRST#	I	<p><b>Resume Well Reset:</b> This signal is used for resetting the resume power plane logic. This signal must be asserted for at least t201 after the suspend power wells are valid. When de-asserted, this signal is an indication that the suspend power wells are stable.</p>
SATA1GP/ <b>SATAPHY_PC/</b> GPIO35	O	<p><b>SATA PHY Power Control:</b> Used to control power to VCCSATAPHY and VCCSATA3PLL in S0. PCH will drive SATAPHY_PC low when the SATA controller is idle or have no devices attached AND PCIe* Root Port 6 controller is idle or have no devices attached AND VCCSATA3PLL can be shutdown.</p> <p><b>Note:</b> This signal requires a 100 KΩ pull-up to VCC3_3 when used as SATAPHY_PC functionality.</p> <p><b>Note:</b> This pin defaults to native (out) SATAPHY_PC functionality.</p> <p><b>Note:</b> <b>(U-Processor Line)</b> SATAPHY_PC functionality should not be used. PCH Soft Strap 19 bit 31 must be programmed to '1' to change default to GPIO mode. Further configuration of the GPIO register can be used to change the pin to native (in) SATA1GP functionality.</p>
SLP_A#	O	<p><b>SLP_A#:</b> Used to control power to the active sleep well (ASW) of the PCH.</p>
SLP_LAN#	O	<p><b>LAN Sub-System Sleep Control:</b> When SLP_LAN# is de-asserted it indicates that the PHY device must be powered. When SLP_LAN# is asserted, power can be shut off to the PHY device. SLP_LAN# will always be de-asserted in S0 and anytime SLP_A# is de-asserted.</p>
SLP_WLAN#/ GPIO29	O	<p><b>WLAN Sub-System Sleep Control:</b> When SLP_WLAN# is asserted, power can be shut off to the external wireless LAN device. SLP_WLAN will always be de-asserted in S0.</p> <p><b>Note:</b> The selection between native and GPIO mode is based on a soft strap. The soft strap default is '0', slp_wlan# mode. Even though the pin is in the deep sleep well (DSW), the native and GPIO functionality is only available when the SUS well is powered. Set soft strap to '1' to use the GPIO mode.</p>

**Table 2-7. Power Management Interface Signals (Sheet 3 of 4)**

Name	Type	Description
SLP_S0#	O	<b>S0 Sleep Control:</b> When PCH is idle and processor is in C10 state, this pin will assert to indicate VR controller can go into a light load mode. This signal can also be connected to EC for other power management related optimizations.
SLP_S3#	O	<b>S3 Sleep Control:</b> SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	<b>S4 Sleep Control:</b> SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state.  <b>Note:</b> This pin must be used to control the DRAM power in order to use the PCH DRAM power-cycling feature.
SLP_S5#/GPIO63	O	<b>S5 Sleep Control:</b> SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.  <b>Note:</b> Pin may also be used as GPIO63.
SLP_SUS#	O	<b>Deep Sx Indication:</b> When asserted (driven low), this signal indicates PCH is in Deep Sx state where internal Sus power is shut off for enhanced power saving. When de-asserted (driven high), this signal indicates exit from Deep Sx state and Sus power can be applied to PCH. If Deep Sx is not supported, then this pin can be left unconnected.  <b>Note:</b> This pin is in the DSW power well.
SM_DRAMRST#	OD O	<b>System Memory DRAM Reset:</b> Active low reset signal to DRAM.  <b>Note:</b> An external pull-up to the DRAM power plane is required.
SUSACK#	I	<b>SUSACK#:</b> If Deep Sx is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin.  <b>Note:</b> SUSACK# is only required to change in response to SUSWARN# if Deep Sx is supported by the platform. <b>Note:</b> This pin is in the Sus power well.
SUS_STAT#/GPIO61	O	<b>Suspend Status:</b> This signal is asserted by the PCH to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes.  <b>Note:</b> Pin may also be used as GPIO61.
SUSCLK/GPIO62	O	<b>Suspend Clock:</b> This clock is an output of the RTC generator circuit to use by other chips for refresh clock.  <b>Note:</b> Pin may also be used as GPIO62.
SUSWARN#/SUSPWRDNACK/GPIO30	O	<b>SUSWARN#:</b> This pin asserts low when the PCH is planning to enter the Deep Sx power state and remove Suspend power (using SLP_SUS#). The EC/motherboard controlling logic must observe edges on this pin, preparing for SUS well power loss on a falling edge and preparing for SUS well related activity (host/Intel® ME wakes and runtime events) on a rising edge. SUSACK# must be driven to match SUSWARN# once the above preparation is complete. SUSACK# should be asserted within a minimal amount of time from SUSWARN# assertion as no wake events are supported if SUSWARN# is asserted but SUSACK# is not asserted. Platforms supporting Deep Sx, but not wishing to participate in the handshake during wake and Deep Sx entry may tie SUSACK# to SUSWARN#.  <b>Note:</b> This pin may be multiplexed with a GPIO for use in systems that do not support Deep Sx. This pin is multiplexed with SUSPWRDNACK since it is not needed in Deep Sx supported platforms. <b>Note:</b> This signal is multiplexed with GPIO30 and SUSPWRDNACK.

**Table 2-7. Power Management Interface Signals (Sheet 4 of 4)**

Name	Type	Description
<b>SUSPWRDNACK/ SUSWARN#/GPIO30</b>	O	<b>SUSPWRDNACK:</b> Active high. Asserted by the PCH on behalf of the Intel® ME when it does not require the PCH Suspend well to be powered. <b>Note:</b> Platforms are not expected to use this signal when the PCH Deep Sx feature is used. <b>Note:</b> This signal is multiplexed with GPIO30 and SUSWARN#.
<b>SYS_PWROK</b>	I	<b>System Power OK:</b> This generic power good input to the PCH is driven and utilized in a platform-specific manner. While PCH_PWROK always indicates that the core wells of the PCH are stable, SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset.
<b>SYS_RESET#</b>	I	<b>System Reset:</b> This pin forces an internal reset after being debounced. The PCH will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ±2 ms for the SMBus to idle before forcing a reset on the system.
<b>BMBUSY#/ USB3PHY_PC/ GPIO76</b>	O	<b>USB 3.0 PHY Power Control:</b> Used to control power to VCCUSB3PHY and VCCUSB3PLL in S0. PCH will drive USB3PHY_PC low when the xHCI controller is idle or have no devices attached AND PCIe* Root Ports 1-2 controllers are idle or have no devices attached AND VCCUSB3PLL can be shutdown. <b>Note:</b> This signal requires a 100 KΩ pull-up to VCC3_3 when used as USB3PHY_PC functionality. <b>Note:</b> This pin defaults to native (out) USB3PHY_PC functionality. <b>Note:</b> <b>(U-Processor Line)</b> USB3PHY_PC functionality should not be used. PCH Soft Strap 19 bit 30 must be programmed to '1' to change default to GPIO mode. Further configuration of the GPIO register can be used to change the pin to native (in) BMBUSY# functionality.
<b>WAKE#</b>	I	<b>PCI Express* Wake Event in Sx:</b> Input Pin in Sx. Sideband wake signal on PCI Express* asserted by components requesting wake up.

## 2.8 SMBus Interface

**Table 2-8. SMBus Interface Signals**

Name	Type	Description
<b>SMBDATA</b>	I/OD	<b>SMBus Data:</b> External pull-up resistor is required.
<b>SMBCLK</b>	I/OD	<b>SMBus Clock:</b> External pull-up resistor is required.
<b>SMBALERT#/ GPIO11</b>	I	<b>SMBus Alert:</b> This signal is used to wake the system or generate SMI#. <b>Note:</b> This signal may be used as GPIO11.

## 2.9 System Management Interface

**Table 2-9. System Management Interface Signals (Sheet 1 of 2)**

Name	Type	Description
<b>INTRUDER#</b>	I	<b>Intruder Detect:</b> This input signal can be used to inform the system in the event of the case being opened.
<b>SML0DATA</b>	I/OD	<b>System Management Link 0 Data:</b> SMBus link to external PHY. External pull-up is required.
<b>SML0CLK</b>	I/OD	<b>System Management Link 0 Clock:</b> SMBus link to external PHY. External pull-up is required.
<b>SML0ALERT#/ GPIO60</b>	OD O	<b>SMLLink Alert 0:</b> Output of the integrated LAN controller to external PHY. External pull-up resistor is required. <b>Note:</b> This signal can instead be used as GPIO60.

**Table 2-9. System Management Interface Signals (Sheet 2 of 2)**

Name	Type	Description
<b>SML1ALERT#/TEMP_ALERT#/GPIO73</b>	OD O	<p><b>SMLLink Alert 1:</b> Alert for the ME SMBus controller to optional Embedded Controller or BMC. A soft-strap determines the native function SML1ALERT# or TEMP_ALERT# usage. When soft-strap is 0, function is SML1ALERT#, when soft-strap is 1, function is TEMP_ALERT#.</p> <p><b>Note:</b> This pin can also be set to function as GPIO73.</p> <p><b>Note:</b> External pull-up resistor is required on this pin.</p>
<b>SML1CLK/GPIO75</b>	I/OD	<p><b>System Management Link 1 Clock:</b> SMBus link to optional Embedded Controller or BMC. External pull-up resistor is required.</p> <p><b>Note:</b> This signal can instead be used as GPIO75.</p>
<b>SML1DATA/GPIO74</b>	I/OD	<p><b>System Management Link 1 Data:</b> SMBus link to optional Embedded Controller or BMC. External pull-up resistor is required.</p> <p><b>Note:</b> This signal can instead be used as GPIO74.</p>

## 2.10 Real Time Clock (RTC) Interface

**Table 2-10. Real Time Clock (RTC) Interface**

Name	Type	Description
RTCX1	Special	<p><b>Crystal Input 1:</b> This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate. Maximum voltage allowed on this pin is 1.2V.</p>
RTCX2	Special	<p><b>Crystal Input 2:</b> This signal is connected to the 32.768 KHz crystal. If no external crystal is used, then RTCX2 must be left floating.</p>

## 2.11 Miscellaneous Signals

**Table 2-11. Miscellaneous Signals (Sheet 1 of 2)**

Name	Type	Description
DSWVRMEN	I	<p><b>Deep Sx Well Internal Voltage Regulator Enable:</b> This signal enables the internal DSW 1.05V regulators and must be always pulled-up to VCCRTC.</p>
INTVRMEN	I	<p><b>Internal Voltage Regulator Enable:</b> When pulled high, this signal enables the internal 1.05V regulators for the Suspend well in the PCH. This signal must remain asserted for the VRMs to behave properly (no glitches allowed).</p> <p>This signal must be pulled-up to VCCRTC on desktop platforms and may optionally be pulled low on mobile platforms if using an external VR for the 1.05V suspend rail (DcpSus1, DcpSus2, DcpSus3, and DcpSus4).</p>
PCH_OPI_RCOMP	I	<p><b>PCH On-Package Impedance (OPI) Compensation Input:</b> Connected to a 50 Ω (1%) precision resistor to Vss (Ground).</p> <p><b>Note:</b> This pin was called DMI_RCOMP on past platforms.</p>
PME#	I/OD	<p><b>PCI Power Management Event:</b> PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the PCH may drive PME# active due to an internal wake event. The PCH will not drive PME# high, but it will be pulled-up to VCCSUS3_3 by an internal pull-up resistor. PME# is still functional and can be used with PCI legacy mode on platforms using a PCIe*-to-PCI bridge. Downstream PCI devices would need to have PME# routed from the connector to the PCH PME# pin.</p>

Table 2-11. Miscellaneous Signals (Sheet 2 of 2)

Name	Type	Description
<b>RCIN#/GPIO82</b>	I	<p><b>Keyboard Controller Reset Processor:</b> The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the PCH's other sources of INIT#. When the PCH detects the assertion of this signal, INIT# is generated using a VLW message to the processor.</p> <p><b>Note:</b> The PCH will ignore RCIN# assertion during transitions to the S3, S4, and S5 states.</p>
<b>RTCRST#</b>	I	<p><b>RTC Reset:</b> When asserted, this signal resets register bits in the RTC well.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on.</li> <li>In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the DPWROK pin.</li> <li>RTCRST# must be routed to test pad or jumper pins, in case RTCRST# assertion is needed to address RTC well or platform boot problems typically observed during manufacturing.</li> </ol>
<b>SPKR</b>	O	<p><b>Speaker:</b> The SPKR signal is the output of counter 2 and is internally "ANDED" with Port 61h Bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST#, its output state is 0.</p> <p><b>Note:</b> SPKR is sampled as a functional strap. There is a weak integrated pull-down resistor on SPKR pin.</p>
<b>SRTC RST#</b>	I	<p><b>Secondary RTC Reset:</b> This signal resets the manageability register bits in the RTC well when the RTC battery is removed.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>The SRTC RST# input must always be high when all other RTC power planes are on.</li> <li>In the case where the RTC battery is dead or missing on the platform, the SRTC RST# pin must rise before the DPWROK pin.</li> </ol>
<b>SML1ALERT#/TEMP_ALERT#/GPIO73</b>	OD O	<p><b>TEMP_ALERT#:</b> This signal is used to indicate a PCH temperature out of bounds condition to an external EC, when PCH temperature is greater than value programmed by BIOS. An external pull-up resistor is required on this signal.</p> <p><b>Note:</b> A soft-strap determines the native function SML1ALERT# or TEMP_ALERT# usage. When soft-strap is 0, function is SML1ALERT#, when soft-strap is 1, function is TEMP_ALERT#.</p>
<b>TD_IREF</b>	I	<p><b>Thermal Diode Internal Reference Voltage:</b> Thermal sensor low-cap analog reference bias current. This should be connected to Vss (ground) using an external resistor of 8.25 KΩ.</p>

## 2.12 Intel® High Definition Audio (Intel® HD Audio) Link

Table 2-12. Intel® High Definition Audio (Intel® HD Audio) Link Signals (Sheet 1 of 2)

Name	Type	Description
<b>HDA_RST#/I2S_MCLK</b>	O	<p><b>Intel® High Definition Audio Reset:</b> Master hardware reset to external codec(s).</p> <p><b>Note:</b> This signal is multiplexed with I<sup>2</sup>S Master Clock.</p>
<b>HDA_SYNC/I2S0_SFRM</b>	O	<p><b>Intel High Definition Audio Sync:</b> 48 KHz fixed rate sample sync to the codec(s). Also used to encode the stream number.</p> <p><b>Note:</b> This signal is multiplexed with I<sup>2</sup>S 0 Serial Frame.</p>
<b>HDA_BCLK/I2S0_SCLK</b>	O	<p><b>Intel High Definition Audio Bit Clock Output:</b> 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the PCH).</p> <p><b>Note:</b> This signal is multiplexed with I<sup>2</sup>S 0 Serial Bit Clock.</p>

**Table 2-12. Intel® High Definition Audio (Intel® HD Audio) Link Signals (Sheet 2 of 2)**

Name	Type	Description
<b>HDA_SDO/ I2S0_TXD</b>	O	<p><b>Intel High Definition Audio Serial Data Out:</b> Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48MB/s for Intel High Definition Audio.</p> <p><b>Note:</b> This signal is multiplexed with I<sup>2</sup>S 0 Transmit Data (Serial Data Out).</p>
<b>HDA_SDI[1:0]/ I2S[1:0]_RXD</b>	I	<p><b>Intel High Definition Audio Serial Data In [1:0]:</b> Serial TDM data inputs from the codecs. The serial input is single-pumped for a bit rate of 24MB/s for Intel High Definition Audio. These signals have integrated pull-down resistors, which are always enabled.</p> <p><b>Note:</b> During enumeration, the PCH will drive this signal. During normal operation, the codec will drive it.</p> <p><b>Note:</b> This signal is multiplexed with I<sup>2</sup>S [1:0] Receive Data (Serial Data In).</p>
<b>HDA.Dock_EN#/ I2S1_TXD</b>	O	<p><b>Intel High Definition Audio Dock Enable:</b> This signal controls the external Intel® HD Audio docking isolation logic. This is an active low signal. When de-asserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel® HD Audio dock signals to the corresponding PCH signals.</p> <p><b>Note:</b> This signal is multiplexed with I<sup>2</sup>S 1 Transmit Data (Serial Data Out).</p>
<b>HDA.Dock_RST#/ I2S1_SFRM</b>	O	<p><b>Intel High Definition Audio Dock Reset:</b> This signal is a dedicated HDA_RST# signal for the codec(s) in the docking station. Aside from operating independently from the normal HDA_RST# signal, it otherwise works similarly to the HDA_RST# signal.</p> <p><b>Note:</b> This signal is multiplexed with I<sup>2</sup>S 1 Serial Frame.</p>

## 2.13 Intel® Serial I/O—I<sup>2</sup>S Interface

**Table 2-13. Intel® Serial I/O—I<sup>2</sup>S Interface Signals (Sheet 1 of 2)**

Name	Type	Description
<b>HDA_RST#/ I2S_MCLK</b>	O	<p><b>I<sup>2</sup>S Master Clock:</b></p> <p><b>Note:</b> This signal is multiplexed with Intel® High Definition Audio Reset.</p>
<b>HDA_SYNC/ I2S0_SFRM</b>	I/O	<p><b>I<sup>2</sup>S 0 Serial Frame:</b> Indicates the beginning and end of a serialized data word. Can be generated internally (master mode) or externally (slave mode).</p> <p><b>Note:</b> This signal is multiplexed with Intel High Definition Audio Sync.</p>
<b>HDA_BCLK/ I2S0_SCLK</b>	I/O	<p><b>I<sup>2</sup>S 0 Serial Bit Clock:</b> Used to control the timing of a transfer. Can be generated internally (master mode) or externally (slave mode).</p> <p><b>Note:</b> This signal is multiplexed with Intel High Definition Audio Bit Clock Output.</p>
<b>HDA_SDO/ I2S0_TXD</b>	O	<p><b>I<sup>2</sup>S 0 Transmit Data (Serial Data Out):</b> Serialized data line. Sample length is a function of the selected serial data sample size.</p> <p><b>Note:</b> This signal is multiplexed with Intel High Definition Audio Serial Data Out.</p>
<b>HDA_SDI[1:0]/ I2S[1:0]_RXD</b>	I	<p><b>I<sup>2</sup>S [1:0] Receive Data (Serial Data In):</b> Serialized data line. Sample length is a function of the selected serial data sample size.</p> <p><b>Note:</b> During enumeration, the PCH will drive this signal. During normal operation, the codec will drive it.</p> <p><b>Note:</b> This signal is multiplexed with Intel High Definition Audio Serial Data In [1:0].</p>

**Table 2-13. Intel® Serial I/O—I<sup>2</sup>S Interface Signals (Sheet 2 of 2)**

Name	Type	Description
HDA.Dock_EN#/ <b>I<sup>2</sup>S1_TxD</b>	O	<b>I<sup>2</sup>S 1 Transmit Data (Serial Data Out):</b> Serialized data line. Sample length is a function of the selected serial data sample size.  <b>Note:</b> This signal is multiplexed with Intel High Definition Audio Dock Enable.
HDA.Dock_RST#/ <b>I<sup>2</sup>S1_SFRM</b>	I/O	<b>I<sup>2</sup>S 1 Serial Frame:</b> Serialized data line. Sample length is a function of the selected serial data sample size.  <b>Note:</b> This signal is multiplexed with Intel High Definition Audio Dock Reset.
I <sup>2</sup> S1_SCLK	I/O	<b>I<sup>2</sup>S 1 Serial Bit Clock:</b> Used to control the timing of a transfer. Can be generated internally (master mode) or externally (slave mode).

## 2.14 Intel® Serial I/O—Secure Digital I/O (SDIO) Interface

**Table 2-14. Intel® Serial I/O—SDIO Signals**

Name	Type	Description
<b>SDIO_CLK/GPIO64</b>	O	<b>SDIO Clock</b>  <b>Note:</b> This signal is multiplexed with GPIO64. <b>Note:</b> 50 KΩ pull-down to GND required.
<b>SDIO_CMD/GPIO65</b>	I/O	<b>SDIO Command</b>  <b>Note:</b> This signal is multiplexed with GPIO65. <b>Note:</b> 50 KΩ pull-up to VCCSDIO required.
<b>SDIO_D0/GPIO66</b>	I/O	<b>SDIO Data Bit 0</b>  <b>Note:</b> This signal is multiplexed with GPIO66. <b>Note:</b> 150 KΩ pull-up to VCCSDIO required if the default functional strap (low) is desired. Or 4.7 KΩ pull-up resistor if the functional strap needs to be high.
<b>SDIO_D1/GPIO67</b>	I/O	<b>SDIO Data Bit 1</b>  <b>Note:</b> This signal is multiplexed with GPIO67. <b>Note:</b> 50 KΩ pull-up to VCCSDIO required.
<b>SDIO_D2/GPIO68</b>	I/O	<b>SDIO Data Bit 2</b>  <b>Note:</b> This signal is multiplexed with GPIO68. <b>Note:</b> 50 KΩ pull-up to VCCSDIO required.
<b>SDIO_D3/GPIO69</b>	I/O	<b>SDIO Data Bit 3</b>  <b>Note:</b> This signal is multiplexed with GPIO69. <b>Note:</b> 50 KΩ pull-up to VCCSDIO required.
<b>SDIO_POWER_EN/</b> GPIO70	O	<b>SDIO Power Enable</b>  <b>Note:</b> This signal is multiplexed with GPIO70.
<b>Note:</b> The SDIO interface is supported in Windows* 8 Connected Standby operation only; they are not supported for Windows* 8 Legacy or Windows* 7. Therefore, the SDIO interface should only be used on designs supporting Windows* 8 Connected Standby.		

## 2.15 Intel® Serial I/O—General Purpose SPI Interface

Table 2-15. Intel® Serial I/O—General Purpose SPI Signals

Name	Type	Description
<b>GSPI0_CS#/ GPIO83</b>	O	<b>General Purpose SPI 0 Chip Select</b>  <b>Note:</b> This signal is multiplexed with GPIO83. <b>Note:</b> External Pull-up required.
<b>GSPI0_CLK/ GPIO84</b>	O	<b>General Purpose SPI 0 Clock</b>  <b>Note:</b> This signal is multiplexed with GPIO84. <b>Note:</b> External Pull-up required.
<b>GSPI0_MISO/ GPIO85</b>	I	<b>General Purpose SPI 0 MISO</b>  <b>Note:</b> This signal is multiplexed with GPIO85. <b>Note:</b> External Pull-up required.
<b>GSPI0_MOSI/ GPIO86</b>	O	<b>General Purpose SPI 0 MOSI</b>  <b>Note:</b> This signal is multiplexed with GPIO86. <b>Note:</b> External Pull-up required.
<b>GSPI1_CS#/ GPIO87</b>	O	<b>General Purpose SPI 1 Chip Select</b>  <b>Note:</b> This signal is multiplexed with GPIO87.
<b>GSPI1_CLK/ GPIO88</b>	O	<b>General Purpose SPI 1 Clock</b>  <b>Note:</b> This signal is multiplexed with GPIO88. <b>Note:</b> External Pull-up required.
<b>GSPI1_MISO/ GPIO89</b>	I	<b>General Purpose SPI 1 MISO</b>  <b>Note:</b> This signal is multiplexed with GPIO89. <b>Note:</b> External Pull-up required.
<b>GSPI1_MOSI/ GPIO90</b>	O	<b>General Purpose SPI 1 MOSI</b>  <b>Note:</b> This signal is multiplexed with GPIO90. <b>Note:</b> External Pull-up required.

## 2.16 Serial Peripheral Interface (SPI)

Table 2-16. Serial Peripheral Interface (SPI) Signals

Name	Type	Description
SPI_CLK	O	<b>SPI Clock:</b> SPI clock signal, during idle the bus owner will drive the clock signal low. Supported frequencies are 20 MHz, 33 MHz, and 50 MHz.
SPI_CS0#	O	<b>SPI Chip Select 0:</b> Used to select the primary SPI Flash device.  <b>Note:</b> This signal cannot be used for any other type of device than SPI Flash.
SPI_CS1#	O	<b>SPI Chip Select 1:</b> Used to select an optional secondary SPI Flash device.  <b>Note:</b> This signal cannot be used for any other type of device than SPI Flash.
SPI_CS2#	O	<b>SPI Chip Select 2:</b> Used to select the TPM device if it is connected to the SPI interface; it cannot be used for any other type of device. <b>Note:</b> TPM can be configured through soft straps to operate over LPC or SPI, but no more than 1 TPM is allowed in the system.
SPI_MOSI	I/O	<b>SPI Master OUT Slave IN:</b> Defaults as a data output pin for PCH in Dual Output Fast Read mode. Can be configured with a soft strap as a bidirectional signal (SPI_I00) to support the new Dual I/O Fast Read, Quad I/O Fast Read and Quad Output Fast Read modes.

**Table 2-16. Serial Peripheral Interface (SPI) Signals**

Name	Type	Description
SPI_MISO	I/O	<b>SPI Master IN Slave OUT:</b> Defaults as a data input pin for PCH in Dual Output Fast Read mode. Can be configured with a soft strap as a bidirectional signal (SPI_IO1) to support the new Dual I/O Fast Read, Quad I/O Fast Read and Quad Output Fast Read modes.
SPI_IO2	I/O	<b>SPI Data I/O:</b> A bidirectional signal used to support the new Dual I/O Fast Read, Quad I/O Fast Read and Quad Output Fast Read modes. This signal is not used in Dual Output Fast Read mode.
SPI_IO3	I/O	<b>SPI Data I/O:</b> A bidirectional signal used to support the new Dual I/O Fast Read, Quad I/O Fast Read and Quad Output Fast Read modes. This signal is not used in Dual Output Fast Read mode.

## 2.17 Intel® Serial I/O—Universal Asynchronous Receiver Transmitter (UART) Interface

**Table 2-17. Intel® Serial I/O—UART Signals**

Name	Type	Description
<b>UART0_RXD/ GPIO91</b>	I	<b>High Speed UART 0 Receive Data Input</b>  <b>Note:</b> This signal is multiplexed with GPIO91. <b>Note:</b> External Pull-up required.
<b>UART0_TXD/ GPIO92</b>	O	<b>High Speed UART 0 Transmit Data Output</b>  <b>Note:</b> This signal is multiplexed with GPIO92. <b>Note:</b> External Pull-up required.
<b>UART0_RTS#/ GPIO93</b>	O	<b>High Speed UART 0 Request to Send</b>  <b>Note:</b> This signal is multiplexed with GPIO93. <b>Note:</b> External Pull-up required.
<b>UART0_CTS#/ GPIO94</b>	I	<b>High Speed UART 0 Clear to Send</b>  <b>Note:</b> This signal is multiplexed with GPIO94.
<b>UART1_RXD/ GPIO00</b>	I	<b>High Speed UART 1 Receive Data Input</b>  <b>Note:</b> This signal is multiplexed with GPIO00. <b>Note:</b> External Pull-up required.
<b>UART1_TXD/ GPIO01</b>	O	<b>High Speed UART 1 Transmit Data Output</b>  <b>Note:</b> This signal is multiplexed with GPIO01. <b>Note:</b> External Pull-up required.
<b>UART1_RTS#/ GPIO02</b>	O	<b>High Speed UART 1 Request to Send</b>  <b>Note:</b> This signal is multiplexed with GPIO02. <b>Note:</b> External Pull-up required.
<b>UART1_CTS#/ GPIO03</b>	I	<b>High Speed UART 1 Clear to Send</b>  <b>Note:</b> This signal is multiplexed with GPIO03. <b>Note:</b> External Pull-up required.

## 2.18 Intel® Serial I/O—I<sup>2</sup>C\* Interface

**Table 2-18. Intel® Serial I/O I<sup>2</sup>C Signals**

Name	Type	Description
<b>I2C0_SDA/</b> GPIO4	I/OD	<b>I<sup>2</sup>C 0 Data</b>  <b>Note:</b> This signal is multiplexed with GPIO4. <b>Note:</b> External Pull-up required.
<b>I2C0_SCL/</b> GPIO5	I/OD	<b>I<sup>2</sup>C 0 Clock</b>  <b>Note:</b> This signal is multiplexed with GPIO5. <b>Note:</b> External Pull-up required.
<b>I2C1_SDA/</b> GPIO6	I/OD	<b>I<sup>2</sup>C 1 Data</b>  <b>Note:</b> This signal is multiplexed with GPIO6. <b>Note:</b> External Pull-up required.
<b>I2C1_SCL/</b> GPIO7	I/OD	<b>I<sup>2</sup>C 1 Clock</b>  <b>Note:</b> This signal is multiplexed with GPIO7. <b>Note:</b> External Pull-up required.

## 2.19 Controller Link

**Table 2-19. Controller Link Signals**

Signal Name	Type	Description
CL_RST#	O	<b>Controller Link Reset:</b> Controller Link reset that connects to a Wireless LAN Device supporting Intel Active Management Technology. This signal is in the Suspend power well.
CL_CLK	I/O	<b>Controller Link Clock:</b> Bi-directional clock that connects to a Wireless LAN Device supporting Intel Active Management Technology. This signal is in the Suspend power well.
CL_DATA	I/O	<b>Controller Link Data:</b> Bi-directional data that connects to a Wireless LAN Device supporting Intel Active Management Technology. This signal is in the Suspend power well.

## 2.20 Testability Signals

**Table 2-20. Testability Signals**

Name	Type	Description
PCH_TCK	I/O	<b>Test Clock Input (TCK):</b> The test clock input provides the clock for the JTAG test logic.
PCH_TMS	I/O D	<b>Test Mode Select (TMS):</b> The signal is decoded by the Test Access Port (TAP) controller to control test operations.
PCH_TDI	I/O D	<b>Test Data Input (TDI):</b> Serial test instructions and data are received by the test logic at TDI.
PCH_TDO	I/O D	<b>Test Data Output (TDO):</b> TDO is the serial output for test instructions and data from the test logic defined in this standard.
JTAGX	I/O	<b>JTAGX:</b> This is DFX pin used to support debug port topologies.
<b>Note:</b> JTAG Pin definitions are from IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Std. 1149.1-2001)		

## 2.21 Clock Signals

**Table 2-21. Clock Interface Signals**

Name	Type	Description
CLKOUT_ITPXDP_P CLKOUT_ITPXDP_N	O	100 MHz PCIe* 2.0 specification compliant differential output to processor XDP/ITP connector on platform This Clock can be used for 3rd PEG slot. Platform Over clocking will not be supported when this clock is used for 3rd PEG slot.
XTAL24_IN	I	Connection for 24 MHz crystal to PCH oscillator circuit
XTAL24_OUT	O	Connection for 24 MHz crystal to PCH oscillator circuit
CLKOUT_PCIE_P[5:0], CLKOUT_PCIE_N[5:0]	O	100 MHz PCIe* 2.0 specification compliant differential output to PCI Express* devices. <b>Note:</b> CLKOUT_PCIEn can be mapped to any PCIe* Root Portn using PMSRCCLK register in the FITC tool. See <a href="#">Section 4.5.1.8</a> . <b>Note:</b> Non-Common Clock mode is NOT supported.
PCIECLKRQ0#/GPIO18, PCIECLKRQ1#/GPIO19, PCIECLKRQ2#/GPIO20, PCIECLKRQ3#/GPIO21, PCIECLKRQ4#/GPIO22, PCIECLKRQ5#/GPIO23	I/O	Clock Request Signals for PCI Express* 100 MHz Clocks Can instead be used as GPIOs <b>Note:</b> External pull-up resistor required if used for CLKREQ# functionality. <b>Note:</b> PCIECLKRQn# assignment is fixed to the PCIe* Root Port (n+1), it cannot be remapped.
CLKOUT_LPC[1:0]	O	Single-Ended, 24 MHz outputs to various connectors/devices.
DIFFCLK_BIASREF	I/O	<b>Differential Clock Bias Reference:</b> Connected to an external precision resistor (3 KΩ ±1%) to 1.05V

## 2.22 Digital Display Signals

**Table 2-22. Digital Display Signals**

Name	Type	Description
DDPB_AUXP	I/O	<b>Port B:</b> DisplayPort* Aux
DDPB_AUXN	I/O	<b>Port B:</b> DisplayPort* Aux Complement
DDPB_HPD	I	<b>Port B:</b> HPD Hot-Plug Detect
DDPB_CTRLCLK	I/O	<b>Port B:</b> HDMI* Port B Control Clock.
DDPB_CTRLDATA	I/O	<b>Port B:</b> HDMI* Port B Control Data.
DDPC_AUXP	I/O	<b>Port C:</b> DisplayPort* Aux
DDPC_AUXN	I/O	<b>Port C:</b> DisplayPort* Aux Complement
DDPC_HPD	I	<b>Port C:</b> HPD Hot-Plug Detect
DDPC_CTRLCLK	I/O	<b>Port C:</b> HDMI* Port C Control Clock
DDPC_CTRLDATA	I/O	<b>Port C:</b> HDMI* Port C Control Data

## 2.23 embedded DisplayPort\* (eDP\*) Backlight Control Signals

**Table 2-23. embedded DisplayPort\* (eDP\*) Backlight Control Signals**

Name	Type	Description
eDP_VDDEN	I/O	<b>eDP Panel power Enable:</b> Panel power control enable. This signal is also called VDD_DBL in the CPIS specification and is used to control the VDC source of the panel logic.
eDP_BKLTN	I/O	<b>eDP Backlight Enable:</b> Panel backlight enable control for eDP. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry.
eDP_BKLTCTL	I/O	<b>eDP Panel Backlight Brightness control:</b> Panel brightness control for eDP. This signal also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal
eDP_HPD	I	<b>eDP Port:</b> Hot-Plug Detect <b>Note:</b> The polarity of this signal is active high.
<b>Note:</b> eDP_VDDEN, eDP_BKLTN, eDP_BKLTCTL can be left as no connect if eDP* is not used.		

## 2.24 General Purpose I/O Signals

**Table 2-24** summarizes the GPIOs in the PCH. The control for the GPIO signals is handled through an independent 128-byte I/O space. The base offset for this space is selected by the GPIO\_BAR register in D31:F0 configuration space.

**Note:**

Unused GPIOs should be individually tied to power in order to ensure the input buffer is stable and not dissipating needless power. However, additional power savings (up to 5  $\mu$ W per unused GPIO in some corner and high temperature cases) can be achieved if these unused GPIOs are pulled down to ground instead of pulled up to power. In either case, the value of the resistor used should be in the range of 4.7 K $\Omega$  to 50 K $\Omega$ . The unused GPIOs should remain configured in default GPIO state and input sensing should be disabled by setting the corresponding GPIO's GPnConfigB.GPINDIS = 1.

### Highlights of GPIO Features

1. All GPIO are powered from 3.3V rail but some are 1.8V input tolerant.
2. Only GPIO[31:0] are blink-capable.
3. When the default of a multiplexed GPIO is Native but the desired functionality is GPIO, care should be taken to ensure the signal is stable until it is initialized to GPIO functionality.
4. In **Table 2-24**, Glitch-less Output means the signal is guaranteed to be stable (no glitch) during power on and when switching mode of operation. Glitch-less Input means the signal has built-in de-glitch protection.
5. All GPIO are capable of generating IRQ interrupt based on software-configured level or edge-triggered event.
6. All GPIO are capable of generating SCI.
7. Only GPIO[47:32] are capable of NMI generation.
8. Only GPIO[47:32] are capable of SMI# generation.
9. All Suspend Well (SUS) and Deep Sleep Well (DSW) GPIO are capable of generating wake event.

10. GPIO Configuration registers within the Core Well are reset whenever PCH\_PWROK is de-asserted.
11. GPIO Configuration registers within the Suspend Well are reset when RSMRST# is asserted, CF9h reset (06h or 0Eh), or SYS\_RESET# is asserted. However, CF9h reset and SYS\_RESET# events can be masked from resetting the Suspend well GPIO by programming appropriate GPIO Reset Select (GPIO\_RST\_SEL) registers.
12. GPIO24 is an exception to the other GPIO signals in the Suspend Well and is not reset by CF9h reset (06h or 0Eh). Refer to offset 60h-63h: GP\_RST\_SEL[31:0] register description.
13. All GPIO pins can be configured to have internal weak pull-up, weak pull-down or none, as described in [Section 10.9.25, "GPnCONFIGB—GPIO Configuration B Register \(Where n = GPIO Pin Number\)" on page 480](#).

**Table 2-24. General Purpose I/O Signals (Sheet 1 of 5)**

Name	Type	Power Well	Default	Internal Pull-Up/Pull-Down	Glitch-less		Description
					Input	Output	
GPIO0	I/O	Core	GPIO		No	Yes	Multiplexed with UART1_RXD
GPIO1	I/O	Core	GPIO		No	Yes	Multiplexed with UART1_TXD
GPIO2	I/O	Core	GPIO		No	Yes	Multiplexed with UART1_RTS#
GPIO3	I/O	Core	GPIO		No	Yes	Multiplexed with UART1_CTS#
GPIO4	I/O	Core	GPIO		Yes	Yes	Multiplexed with I2C0_SDA (Note 2)
GPIO5	I/O	Core	GPIO		Yes	Yes	Multiplexed with I2C0_SCL (Note 2)
GPIO6	I/O	Core	GPIO		Yes	Yes	Multiplexed with I2C1_SDA (Note 2)
GPIO7	I/O	Core	GPIO		Yes	Yes	Multiplexed with I2C1_SCL (Note 2)
GPIO8	I/O	Sus	GPIO		No	Yes	Unmultiplexed.
GPIO9	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO10	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO11	I/O	Sus	GPIO		Yes	Yes	Multiplexed with SMBALERT#
GPIO12	I/O	DSW	Native		No	Yes	Multiplexed with LAN_PHY_PWR_CTRL. GPIO/Native functionality is controlled using soft strap. When configured as GPIO, default direction is Output (GPO). (Note 4)
GPIO13	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO14	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO15	I/O	Sus	GPO	Pull-down (Disabled after RSMRST# de-asserts)	No	Yes	Unmultiplexed This pin is a functional boot strap, see <a href="#">Section 2.27</a> .
GPIO16	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO17	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO18	I/O	Core	GPIO		No	Yes	Multiplexed with PCIECLKRQ0# External pull-up resistor required for Native function.
GPIO19	I/O	Core	GPIO		No	Yes	Multiplexed with PCIECLKRQ1# External pull-up resistor required for Native function.

Table 2-24. General Purpose I/O Signals (Sheet 2 of 5)

Name	Type	Power Well	Default	Internal Pull-Up/Pull-Down	Glitch-less		Description
					Input	Output	
GPIO20	I/O	Core	GPIO		No	Yes	Multiplexed with PCIECLKRQ2# External pull-up resistor required for Native function.
GPIO21	I/O	Core	GPIO		No	Yes	Multiplexed with PCIECLKRQ3# External pull-up resistor required for Native function.
GPIO22	I/O	Core	GPIO		No	Yes	Multiplexed with PCIECLKRQ4#. External pull-up resistor required for Native function.
GPIO23	I/O	Core	GPIO		No	Yes	Multiplexed with PCIECLKRQ5#. External pull-up resistor required for Native function.
GPIO24	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO25	I/O	DSW	GPIO		No	Yes	Unmultiplexed
GPIO26	I/O	Sus	GPIO		No	Yes	Unmultiplexed (Note 1)
GPIO27	I/O	DSW	GPIO	(Note 3)	No	Yes	Unmultiplexed. Can be configured as wake input to allow wakes from Deep Sx, but since this pin is shared, the PCH counts on this pin remaining asserted until PLTRST# de-asserts or the PCH may latch the pin assertion as a LAN wake request. <ul style="list-style-type: none"> <li>Intel LAN Present: This pin is connected to the LANWAKE# pin on the LAN PHY, and used to signal a ME or host wake to the PCH. The pin may also be driven by the platform to cause a host wake, but it must be de-asserted whenever PLTRST# is de-asserted and may only be used to wake the host (GP27 wake enable must always be set).</li> <li>No Intel LAN Present: This pin does not have a specific usage model for connection on the board, but allows the OEM/ODM customers a custom method to wake from Deep Sx.</li> </ul>
GPIO28	I/O	Sus	GPIO		No	Yes	Unmultiplexed (Note 1)
GPIO29	I/O	DSW	Native		No	Yes	Multiplexed with SLP_WLAN#.           GPIO/Native functionality is controlled using soft strap. When configured as GPIO, default direction is Output (GPO).           Even though the pin is in the deep sleep well (DSW), the Native and GPIO/MGPIO functionality is only available when the SUS well is powered.
GPIO30	I/O	Sus	Native		No	Yes	Multiplexed with SUSPWRDNACK, SUSWARN#.           SUSPWRDNACK mode is the default mode of operation. If the system supports Deep Sx, then subsequent boots will default to SUSWARN# mode.

**Table 2-24. General Purpose I/O Signals (Sheet 3 of 5)**

Name	Type	Power Well	Default	Internal Pull-Up/Pull-Down	Glitch-less		Description
					Input	Output	
GPIO31	I/O	DSW	GPIO	(Note 3)	No	Yes	<b>Notes:</b> <ol style="list-style-type: none"> <li>Toggling this pin at a frequency higher than 10 Hz is not supported.</li> <li>GP31_CONFIG[0] is internally hardwired to a 1b, which means GPIO mode is permanently selected and cannot be changed.</li> <li>This GPIO is permanently appropriated by the Intel® ME as MGPIO2 for ACPRESENT function.</li> </ol>
GPIO32	I/O	Core	GPIO		No	Yes	Multiplexed with CLKRUN#.
GPIO33	I/O	Core	GPIO		No	Yes	Multiplexed with DEVSLP0
GPIO34	I/O	Core	GPIO (Note 5)	(Note 8)	No	Yes	Multiplexed with SATA0GP
GPIO35	I/O	Core	Native (Note 6, 7)	(Note 8)	No	Yes	Multiplexed with SATAPHY_PC and SATA1GP <b>Note:</b> This pin defaults to native (out) SATAPHY_PC functionality. <b>Note:</b> <b>(U-Processor Line)</b> SATAPHY_PC functionality should not be used. PCH Soft Strap 19 bit 31 must be programmed to '1' to change default to GPIO mode.
GPIO36	I/O	Core	GPIO (Note 5)	(Note 8)	No	Yes	Multiplexed with SATA2GP
GPIO37	I/O	Core	GPIO (Note 5)	(Note 8)	No	Yes	Multiplexed with SATA3GP
GPIO38	I/O	Core	GPIO		No	Yes	Multiplexed with DEVSLP1
GPIO39	I/O	Core	GPIO		No	Yes	Multiplexed with DEVSLP2
GPIO40	I/O	Sus	GPIO		No	Yes	Multiplexed with OC0#
GPIO41	I/O	Sus	GPIO		No	Yes	Multiplexed with OC1#
GPIO42	I/O	Sus	GPIO		No	Yes	Multiplexed with OC2#
GPIO43	I/O	Sus	GPIO		No	Yes	Multiplexed with OC3#
GPIO44	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO45	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO46	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO47	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO48	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO49	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO50	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO51	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO52	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO53	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO54	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO55	I/O	Core	GPIO		No	Yes	Unmultiplexed
GPIO56	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO57	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO58	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO59	I/O	Sus	GPIO		No	Yes	Unmultiplexed
GPIO60	I/O	Sus	GPIO		Yes	Yes	Multiplexed with SML0ALERT#

Table 2-24. General Purpose I/O Signals (Sheet 4 of 5)

Name	Type	Power Well	Default	Internal Pull-Up/Pull-Down	Glitch-less		Description
					Input	Output	
GPIO61	I/O	Sus	Native		No	Yes	Multiplexed with SUS_STAT#. GPIO/Native functionality is controlled using soft strap. When configured as GPIO, default direction is Output (GPO)
GPIO62	I/O	Sus	Native		No	Yes	Multiplexed with SUSCLK. GPIO/Native functionality is controlled using soft strap. When configured as GPIO, default direction is Output (GPO).
GPIO63	I/O	DSW	Native		No	Yes	Multiplexed with SLP_S5#. GPIO/Native functionality is controlled using soft strap. When configured as GPIO, default direction is Output (GPO). Even though the pin is in the deep sleep well (DSW), the GPIO functionality is only available when the SUS well is powered.
GPIO64	I/O	Core	GPIO		No	Yes	Multiplexed with SDIO_CLK (Note 10)
GPIO65	I/O	Core	GPIO		No	Yes	Multiplexed with SDIO_CMD (Note 10)
GPIO66	I/O	Core	GPO	Pull-down (Disabled after PLTRST#)	No	Yes	Multiplexed with SDIO_D0 This pin is a functional boot strap, see Section 2.27. (Note 10)
GPIO67	I/O	Core	GPIO		No	Yes	Multiplexed with SDIO_D1 (Note 10)
GPIO68	I/O	Core	GPIO		No	Yes	Multiplexed with SDIO_D2 (Note 10)
GPIO69	I/O	Core	GPIO		No	Yes	Multiplexed with SDIO_D3 (Note 10)
GPIO70	I/O	Core	GPIO		No	Yes	Multiplexed with SDIO_POWER_EN (Note 10)
GPIO71	I/O	Core	Native		No	No	(Intel® Core™ M processor): Multiplexed with PCIEPHY_PC  <b>(U-Processor Line):</b> Multiplexed with HSIO PC
GPIO72	I/O	DSW	Native		No	Yes	Multiplexed with BATLOW#
GPIO73	I/O	Sus	GPIO		Yes	Yes	Multiplexed with SML1ALERT#/TEMP_ALERT# After selecting Native mode by updating GPIO_USE_SEL, the choice of SML1ALERT# and TEMP_ALERT# is determined by a soft strap.
GPIO74	I/O	Sus	GPIO		Yes	Yes	Multiplexed with SML1DATA
GPIO75	I/O	Sus	GPIO		Yes	Yes	Multiplexed with SML1CLK
GPIO76	I/O	Core	Native		No	Yes	Multiplexed with USB3PHY_PC and BMBUSY#  <b>Note:</b> This pin defaults to native (out) USB3PHY_PC functionality. <b>Note:</b> <b>(U-Processor Line)</b> USB3PHY_PC functionality should not be used. PCH Soft Strap 19 bit 30 must be programmed to '1' to change default to GPIO mode.
GPIO77	I/O	Core	GPIO		No	Yes	Multiplexed with PIRQA#
GPIO78	I/O	Core	GPIO		No	Yes	Multiplexed with PIRQB#

**Table 2-24. General Purpose I/O Signals (Sheet 5 of 5)**

Name	Type	Power Well	Default	Internal Pull-Up/Pull-Down	Glitch-less		Description
					Input	Output	
GPIO79	I/O	Core	GPIO		No	Yes	Multiplexed with PIRQC#
GPIO80	I/O	Core	GPIO		No	Yes	Multiplexed with PIRQD#
GPIO81	I/O	Core	GPO	Pull-down (disabled after PLTRST#)	No	Yes	Multiplexed with SPKR This pin is a functional boot strap, see <a href="#">Section 2.27</a> .
GPIO82	I/O	Core	GPIO		No	Yes	Multiplexed with RCIN#
GPIO83	I/O	Core	GPIO		No	Yes	Multiplexed with GSPI0_CS#
GPIO84	I/O	Core	GPIO		No	Yes	Multiplexed with GSPI0_CLK
GPIO85	I/O	Core	GPIO	(Note 9)	No	Yes	Multiplexed with GSPI0_MISO
GPIO86	I/O	Core	GPO	Pull-down (disabled after PLTRST#)	No	Yes	Multiplexed with GSPI0_MOSI This pin is a functional boot strap, see <a href="#">Section 2.27</a> .
GPIO87	I/O	Core	GPIO		No	Yes	Multiplexed with GSPI1_CS#
GPIO88	I/O	Core	GPIO		No	Yes	Multiplexed with GSPI1_CLK
GPIO89	I/O	Core	GPIO	(Note 9)	No	Yes	Multiplexed with GSPI1_MISO
GPIO90	I/O	Core	GPIO		No	Yes	Multiplexed with GSPI1_MOSI
GPIO91	I/O	Core	GPIO		No	Yes	Multiplexed with UART0_RXD
GPIO92	I/O	Core	GPIO		No	Yes	Multiplexed with UART0_TXD
GPIO93	I/O	Core	GPIO		No	Yes	Multiplexed with UART0_RTS#
GPIO94	I/O	Core	GPIO		No	Yes	Multiplexed with UART0_CTS#

**Notes:**

1. GPIO26 and GPIO28 can be re-purposed as NFC input interface. If so, both are required (instead of one or the other). The NFC option can be set through FITC in Intel® ME configuration settings.
2. 1.8V input tolerant.
3. Internal pull-down resistor may be enabled in Deep Sx mode based on DSX\_CFG configuration bit, as follows: '1' (pin will be driven by platform in Deep Sx) -> Z; - '0' (pin will NOT be driven by the platform in Deep Sx) -> Internal pull-down. Refer to DSX\_CFG register (RCBA+3334h) for more details.
4. Soft-Strap configuration even though GPIO Lockdown Enable (GLE) bit is set. LAN\_PHY\_PWR\_CTRL and SLP\_S5# are backed up in DSW by the PMC.
5. Pin will default to SATAxGP (native input mode) if associated PCH soft strap 14 SATAPx\_PCIEP6Lx\_MODE is set to 11b.
6. PCH soft strap 14 SATAP1\_PCIEP6L2\_MODE set to 11b will have no effect if PCH soft strap 19 bit 31 is programmed to '0' (default SATAPHY\_PC functionality).
7. **(U-Processor Line)** SATAPHY\_PC functionality should not be used. PCH Soft Strap 19 bit 31 must be programmed to '1' to change default to GPIO mode. Pin will default to SATA1GP (native input mode) if associated PCH Soft Strap 14 SATAP1\_PCIEP6L2\_MODE is set to 11b.
8. When PCH soft strap 14 SATAPx\_PCIE6Lx\_MODE is set to 11b and pin is used as SATAxGP (native input mode), an internal pull-up is present.
9. In native mode usage, an internal pull-down is present.
10. SDIO/GPIO signal group will support 1.8V signaling levels and is only 1.8V voltage tolerant when VCCSDIO = 1.8V; SDIO/GPIO signal group will support 3.3V signaling levels and is 3.3V voltage tolerant when VCCSDIO = 3.3V.

## 2.25 Manageability Signals

The following signals can be optionally used by Intel® Management Engine supported applications and appropriately configured by Intel® Management Engine firmware. When configured and used as a manageability function, the associated host GPIO functionality is no longer available. If the manageability function is not used in a platform, the signal can be used as a host General Purpose I/O or a native function.

The manageability signals are referred to as Management Engine GPIO pins (MGPIO pins), which are GPIO pins that can be controlled through Intel® ME firmware.

**Table 2-25. Management Engine GPIO (MGPIO) Conversion Table**

MGPIO	GPIO	Well	Recommended Usage
0	24	SUS	RTD3 Support: Mini PCIe* Wake
1	30	SUS	<b>SUSWARN# or SUSPWRDNACK</b>
2	31	DSW	ACPRESENT
3	29	DSW	SLP_WLAN#
4	60	SUS	SML0ALERT#
5	26	SUS	NFC Interrupt (If used, assumes GPIO73 is not setup for NFC)
6	27	DSW	ME Wake Input (see <a href="#">Table 2-26</a> )
7	28	SUS	NFC Reset (required for NFC)
8	73	SUS	<b>SML1ALERT#/TEMP_ALERT# or NFC Interrupt</b> (If used as NFC, assumes GPIO26 is not setup for NFC)
9	16	MAIN	RTD3 Support: Gated Reset to on-board LAN PHY
10	17	MAIN	Critical temperature reporting between PCH and EC
11	75	SUS	SML1CLK
12	74	SUS	SML1DATA

**Table 2-26. Manageability Signals**

Name	Type	Power Well	Description
MGPIO 6	I/O	DSW	Can be configured as a wake input for the Intel® ME. This pin is implemented in the DSW in order to allow wakes from the DeepSx state. This pin does not have a specific usage model for connection on the board, but allows the OEM/ODM customers a custom method to wake from DeepSx.

## 2.26 Power and Ground Signals

**Table 2-27. Power and Ground Signals (Sheet 1 of 3)**

Name	Description
DCPRTC	<b>Decoupling:</b> This signal is for RTC decoupling only. This signal requires decoupling.
DCPSUS1	1.05V Suspend well power. If INTVRMEN is strapped high then power to this well is supplied internally and this pin should be left as no connect. If INTVRMEN is strapped low then power to this well must be supplied by an external 1.05V suspend rail.
DCPSUS2	1.05V Suspend well power for USB 2.0 core logic and HD Audio. If INTVRMEN is strapped high then power to this well is supplied internally and this pin should be left as no connect. If INTVRMEN is strapped low then power to this well must be supplied by an external 1.05V suspend rail.
DCPSUS3	1.05V Suspend well power for USB 3.0. If INTVRMEN is strapped high then power to this well is supplied internally and these pins should be left as no connect. If INTVRMEN is strapped low then power to this well must be supplied by an external 1.05V suspend rail.
DCPSUS4	1.05V Suspend well Oscillator power. If INTVRMEN is strapped high then power to this well is supplied internally and these pins should be left as no connect. If INTVRMEN is strapped low then power to this well must be supplied by an external 1.05V suspend rail.
DCPSUSBYP	<b>Decoupling:</b> This signal is for decoupling internally generated 1.05V Deep Sx only.
VCC1_05	1.05V supply for core well logic. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.  <b>Note:</b> In external suspend VR mode (INTVRMEN sampled low), the voltage level of VCC1_05 may be indeterminate while DcpSus (1.05V suspend well power) supply ramps and prior to PCH_PWROK assertion. <b>Note:</b> If VCC1_05 ramps prior to VCC3_3, leakage may be seen on VCC3_3. If VCC3_3 ramps prior to VCC1_05, leakage may be seen on VCC1_05. This will not result in any functional issue.
(Intel® Core™ M processor: Multiplexed with PCIEPHY_PC): VCC1_05_PHY	1.05V supply for PCIe* and SATA core well logic. This power is NOT gated and remains on in S0. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
(Intel® Core™ M processor: Multiplexed with PCIEPHY_PC): VCC1_05_USB2	1.05V supply for USB 2.0 core well logic. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
(Intel® Core™ M processor: Multiplexed with PCIEPHY_PC): VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6, VCCCLK7  (U-Processor Line): VCCCLK	1.05V supply for clock buffers. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
(U-Processor Line) VCCHSIO	1.05V supply for High Speed I/O core well logic.  <b>Note:</b> This power can be shut off when PCH drives HSIOPC low during S0 idle condition. This power may be shut off in S3, S4, S5, Deep Sx or G3 states.



Table 2-27. Power and Ground Signals (Sheet 2 of 3)

Name	Description
(Intel® Core™ M processor: Multiplexed with PCIEPHY_PC) VCCPCIEPHY	1.05V supply for PCIe* Root Ports 3, 4, and 5 core well logic.  <b>Note:</b> This power can be shut off when PCH drives PCIEPHY_PC low during S0 idle condition. This power may be shut off in S3, S4, S5, Deep Sx or G3 states.
(Intel® Core™ M processor: Multiplexed with PCIEPHY_PC) VCCSATAPHY	1.05V supply for SATA core well logic AND PCIe* Root Port 6 core well logic.  <b>Note:</b> This power can be shut off when PCH drives SATAPHY_PC low during S0 idle condition. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
(Intel® Core™ M processor: Multiplexed with PCIEPHY_PC) VCCUSB3PHY	1.05V supply for xHCI core well logic AND PCIe* Root Ports 1 and 2 core well logic.  <b>Note:</b> This power can be shut off when PCH drives USB3PHY_PC low during S0 idle condition. This power may be shut off in S3, S4, S5, Deep Sx or G3 states.
VCCUSB3PLL	1.05V supply for USB 3.0, PCI Express* and GbE PLL.  <b>Note:</b> <b>(U-Processor Line):</b> This power can be shut off when PCH drives HSIOPC low during S0 idle condition. <b>(Intel® Core™ M processor):</b> (Multiplexed with PCIEPHY_PC) This power can be shut off when PCH drives USB3PHY_PC low during S0 idle condition. <b>Note:</b> This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
VCCSATA3PLL	1.05V supply for SATA3 PLL.  <b>Note:</b> <b>(U-Processor Line):</b> This power can be shut off when PCH drives HSIOPC low during S0 idle condition. <b>(Intel® Core™ M processor):</b> (Multiplexed with PCIEPHY_PC) This power can be shut off when PCH drives SATAPHY_PC low during S0 idle condition. <b>Note:</b> This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
VCCAPLL	<b>Note:</b> 1.05V supply for USB 2.0 and Audio, PLL. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
VCCACLKPLL	<b>Note:</b> 1.05V supply for Clock PLL. This power may be shut off in S3, S4, S5, Deep Sx or G3 states.
VCCHDAPLL	<b>Note:</b> 1.05V supply for Audio PLL. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
VCCUSB2PLL	<b>Note:</b> 1.05V supply for USB2 PLL. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
VCCOPIPLL	<b>Note:</b> 1.05V supply for On Package DMI PLL. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
VCCTS1_5	1.5V supply for Thermal Sensor and Diodes. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
VCCTS3_3	3.3V supply for Thermal Sensor and Diodes. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.
VCCSDIO	1.8V/3.3V supply for SDIO. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states. <b>Note:</b> VCCSDIO still needs to be supplied 1.8V/3.3V even when SDIO interface is not used. <b>Note:</b> SDIO/GPIO signal group will support 1.8V signaling levels and is only 1.8V voltage tolerant when VCCSDIO = 1.8V; SDIO/GPIO signal group will support 3.3V signaling levels and is 3.3V voltage tolerant when VCCSDIO = 3.3V
VCC3_3	3.3V supply for core well I/O buffers. This power may be shut off in S3, S4, S5, Deep Sx, or G3 states.  <b>Note:</b> If VCC1_05 ramps prior to VCC3_3, leakage may be seen on VCC3_3. If VCC3_3 ramps prior to VCC1_05, leakage may be seen on VCC1_05. This will not result in any functional issue.
VCCASW	1.05V supply for the Active Sleep Well. Provides power to the Intel® ME and integrated LAN. This plane must be on in S0 and other times the Intel® ME or integrated LAN is used.

**Table 2-27. Power and Ground Signals (Sheet 3 of 3)**

Name	Description
VCCHDA	1.5V or 3.3V supply for Intel® HD Audio. When function as I <sup>2</sup> S interface, this power can be supplied with 1.8V or 3.3V. This power can be supplied with suspend or core well.
VCCSUS3_3	3.3V supply for suspend well I/O buffers. This power may be shut off in Deep Sx or G3 states.
VCCSUS3_3_RTC	3.3V supply for RTC suspend well I/O buffers. This power may be shut off in Deep Sx or G3 states.
VCCSPI	3.3V supply for SPI I/O buffers. This rail must be powered when VCCASW is powered. <b>Note:</b> This rail can be optionally powered on 3.3V Suspend power (VCCSUS3_3) based on platform needs.
VCCDSW3_3	3.3V supply for Deep Sx wells. If platform does not support Deep Sx then tie to VCCSUS3_3.
VCCRRTC	3.3V (can drop to 2.0V minimum in the G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. <b>Note:</b> Implementations should not attempt to clear CMOS by using a jumper to pull VCCRRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI. <b>Note:</b> VCCRRTC is expected to only ramp during RTC coin cell battery insertion. It is not intended for repetitive power cycling.
VSS	Ground

## 2.27 Pin Straps

The following signals are used for static configuration. They are sampled at the rising edge of PCH\_PWROK to select configurations (except as noted), and then revert later to their normal usage. To invoke the associated mode, the signal should be driven at least four 24-MHz clocks prior to the time it is sampled.

The PCH implements soft straps, which are used to configure specific functions within the PCH and processor very early in the boot process before BIOS or software intervention. When Descriptor Mode is enabled, the PCH will read soft strap data out of the SPI device prior to the de-assertion of reset to both the Intel® Management Engine and the Host system. Refer to [Section 5.26.2](#) for information on Descriptor Mode.

**Table 2-28. Functional Strap Definitions (Sheet 1 of 3)**

Signal	Usage	When Sampled	Comment
HDA_SDO/ I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.            0 = <b>Enable</b> security measures defined in the Flash Descriptor.            1 = <b>Disable</b> Flash Descriptor Security (<b>override</b>). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>2. Asserting HDA_SDO high on the rising edge of PWROK will also halt Intel® Management Engine after Chipset bring up and disable runtime Intel® ME features. This is a debug mode and must not be asserted after manufacturing/debug.</li> <li>3. This signal is in the Suspend well.</li> </ol>

Table 2-28. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
INTVRMEN	Integrated VRM Enable	Always	<p>This signal does not have an internal resistor; an <b>external</b> resistor is <b>required</b>.</p> <p>0 = DCPSUS1, DCPSUS2, DCPSUS3 and DCPSUS4 are powered from an external power source (should be connected to an external VRM).</p> <p>1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2, and DCPSUS3 can be left as No Connect.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This signal is always sampled.</li> <li>2. This signal is in the RTC well.</li> </ol>
DSWVRMEN	DeepSx Well On-Die Voltage Regulator Enable	Always	<p>This signal does not have an internal resistor; an <b>external</b> resistor is <b>required</b>.</p> <p>0 = <b>Disable</b> Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments.</p> <p>1 = <b>Enable</b> DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This signal is always sampled.</li> <li>2. This signal is in the RTC well.</li> </ol>
GPIO15	TLS Confidentiality	Rising edge of RSMRST#	<p>This signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> Intel® ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).</p> <p>1 = <b>Enable</b> Intel® ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel® SBA (Small Business Advantage) with TLS.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The internal pull-down is disabled after RSMRST# de-asserts.</li> <li>2. This signal is in the Suspend well.</li> </ol>
SPKR/GPIO81	No Reboot	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "No Reboot" mode.</p> <p>1 = <b>Enable</b> "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5).</li> <li>3. See <a href="#">Section 8.1.50</a> for additional information.</li> <li>4. This signal is in the Core well.</li> </ol>

**Table 2-28. Functional Strap Definitions (Sheet 3 of 3)**

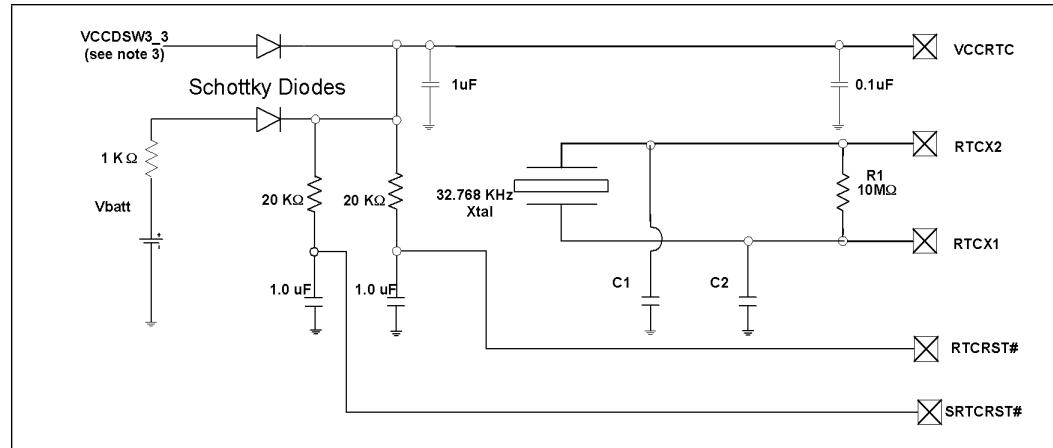
Signal	Usage	When Sampled	Comment						
GPIO0_MOSI/GPIO86	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	<p>This Signal has a weak internal pull-down.</p> <p>This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.</p> <table> <thead> <tr> <th>Bit 10</th> <th>Boot BIOS Destination</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SPI</td> </tr> <tr> <td>1</td> <td>LPC</td> </tr> </tbody> </table> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.</li> <li>3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel® ME or Integrated GbE LAN.</li> <li>4. This signal is in the Core well.</li> </ol>	Bit 10	Boot BIOS Destination	0	SPI	1	LPC
Bit 10	Boot BIOS Destination								
0	SPI								
1	LPC								
SDIO_D0/GPIO66	Top Swap Override	Rising edge of PCH_PWROK	<p>The signal has a weak internal pull-down.</p> <p>0 = <b>Disable</b> "Top Swap" mode. (Default)</p> <p>1 = <b>Enable</b> "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC).</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>2. Software will not be able to clear the Top Swap bit until the system is rebooted.</li> <li>3. The status of this strap is readable using the Top Swap bit (Chipset Configuration Registers: RCBA + Offset 3414h:Bit 0).</li> <li>4. This signal is in the Core well.</li> </ol>						
DDPB_CTRLDATA	Port B Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port B is not detected.</p> <p>1 = Port B is detected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>2. This signal is in the Core well.</li> </ol>						
DDPC_CTRLDATA	Port C Detected	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down.</p> <p>0 = Port C is not detected.</p> <p>1 = Port C is detected.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The internal pull-down is disabled after PLTRST# de-asserts.</li> <li>2. This signal is in the Core well.</li> </ol>						

**Note:** See Section 3.1 for full details on pull-up/pull-down resistors.

## 2.28 External RTC Circuitry

The PCH implements an internal oscillator circuit that is sensitive to step voltage changes in VCCRTC. Figure 2-2 shows an example schematic recommended to ensure correct operation of the PCH RTC.

**Figure 2-2. Example External RTC Circuit**



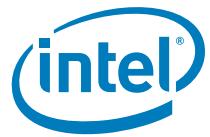
**Notes:**

1. The Reference Designators used in this example are arbitrarily assigned.
2. The exact capacitor values and tolerances for C1 and C2 must be based on the crystal maker recommendations.
3. For platforms not supporting Deep Sx, the VCCDSW3\_3 pins must be connected to the VCCSUS3\_3 pins.
4. Vbatt is voltage provided by the RTC battery (such as coin cell).
5. VCCRTC, RTCX1, RTCX2, RTCRST#, and SRTCRST# are PCH pins.
6. VCCRTC powers PCH RTC well.
7. RTCX1 is the input to the internal oscillator.
8. RTCX2 is the amplified feedback (output) for the external crystal. Important: If a single-ended clock source, such as an oscillator, is used instead of the crystal to generate the RTC frequency, **pin RTCX2 must be left floating** (no connect).
9. Capacitors on RTCRST# and SRTCRST# must be type X5R type or better

**Table 2-1. Real Time Clock (RTC) Crystal Requirements**

Parameter	Specification
Frequency	32.768 KHz
Tolerance	20 PPM or better
ESR	$\leq 50 \text{ k}\Omega$

§ §



***Signal Description***

# 3 Platform Controller Hub (PCH) Pin States

## 3.1 Integrated Pull-Ups and Pull-Downs

Table 3-1. Integrated Pull-Up and Pull-Down Resistors

Signal	Resistor Type	Nominal	Notes
CL_CLK	Pull-up/Pull-down	32/100 KΩ	8, 13
CL_DATA	Pull-up/Pull-down	32/100 KΩ	8, 13
HDA_SDI[1:0]/I2S[1:0]_RXD	Pull-down	20 KΩ	2
HDA_SYNC/I2S0_SCLK	Pull-down	20 KΩ	2, 5, 9
HDA_SD0/I2S0_TXD	Pull-down	20 KΩ	2, 5, 9
GPIO15	Pull-down	20 KΩ	2, 5, 12
LAD[3:0]#	Pull-up	20 KΩ	3
PME#	Pull-up	20 KΩ	3
PWRBTN#	Pull-up	20 KΩ	3
SPI_MOSI	Pull-up/Pull-down	20 KΩ	3, 16
SPI_MISO	Pull-up	20 KΩ	3
SPI_CS[2:0]#	Pull-up	20 KΩ	3
SPI_IO[3:2]	Pull-up	20 KΩ	3
SPI_CLK	Pull-up	20 KΩ	3
SPKR/GPIO81	Pull-down	20 KΩ	2, 9
USB[7:0] [P,N]	Pull-down	15 KΩ	4, 17
DDP[B:C]_CTRLDATA	Pull-down	20 KΩ	3, 9
CLKOUT_LPC[1:0]	Pull-down	20 KΩ	1, 10
JTAG_TDI, JTAG_TMS	Pull-up	20 KΩ	6, 11
JTAG_TCK	Pull-down	20 KΩ	7, 11
WAKE#	Pull-down	20 KΩ	3, 14, 19
ACPRESENT_GPI31	Pull-down	20 KΩ	3, 14
GPIO27	Pull-down	20 KΩ	3, 14, 20
SUSACK#	Pull-up	20 KΩ	3
SATA[3:0]GP/GPIO[37:34]	Pull-up	20 KΩ	3, 15
SDIO_D0/GPIO66	Pull-down	20 KΩ	2, 9
GPIO_MISO/GPIO85	Pull-down	20 KΩ	2, 18
GPIO_MOSI/GPIO86	Pull-down	20 KΩ	2, 9
GSPI1_MISO/GPIO89	Pull-down	20 KΩ	2, 18

**Notes:**

1. Simulation data shows that these resistor values can range from 10 – 40 K $\Omega$ .
2. Simulation data shows that these resistor values can range from 9 – 50 K $\Omega$ .
3. Simulation data shows that these resistor values can range from 15 – 40 K $\Omega$ .
4. Simulation data shows that these resistor values can range from 14.25 – 24.8 K $\Omega$ .
5. This signal is a PCH functional strap. The pull-up or pull-down on this signal is disabled after it is sampled as a PCH functional strap.
6. Simulation data shows that these resistor values can range from 5 – 15 K $\Omega$ .
7. Simulation data shows that these resistor values can range from 10 – 25 K $\Omega$ .
8. Simulation data shows that these resistor values can range from 15 – 31 K $\Omega$ .
9. The pull-up or pull-down is disabled when PLTRST# is de-asserted.
10. The pull-down is enabled when PCH\_PWROK is low.
11. External termination is also required on these signals for JTAG enabling.
12. The pull-up/pull-down is disabled after RSMRST# is de-asserted.
13. The Controller Link Clock and Data buffers use internal pull-up or pull-down resistors to drive a logical 1 or 0.
14. Pull-down is configurable and can be enabled in Deep Sx state; refer to DSX\_CFG register (RCBA+3334h) for more details.
15. SATA[3:0]GP/GPIO[37:34] has two native functions – the first native function (SATAPx\_PCIEPx\_SELECT) is selected if the Flex I/O soft strap SATAPx\_PCIEPx\_MODE = 11b and takes precedence over any other assignments to this pin (that is, if this is selected, writes to GPIO\_USE\_SEL are ignored). If SATAPx\_PCIEPx\_MODE is not set to 11b, the GPIO\_USE\_SEL register can be used to select the 2nd native function (SATAxGP) or GPIO functionality. Setting SATAPx\_PCIEPx\_MODE = 11b also enables an internal pull-up resistor in this pin to allow Flexible I/O selection of SATA Port x or PCIe\* Port x to be done based on the type of card installed (If sampled value = 1, select SATA; if sampled value = 0, select PCIe\*). Soft straps are handled through FITC
16. Weak internal pull-up resistor is enabled when APWROK is de-asserted and is switched to a weak internal pull-down resistor when APWROK and PLTRST# are both asserted.
17. The integrated pull-down resistor is turned off when the connected port is in L1 or L2.
18. The internal pull-down is valid in native mode only.
19. Regardless of internal pull-up or pull-down, an external pull-up resistor is still required.
20. External pull-up if Intel wired LAN is present (pull-up to SUS/DSW based on deepest wake on LAN support desired).

## 3.2 Output and I/O Signals Planes and States

Table 3-2 shows the power plane associated with the output and I/O signals, as well as the state at various times. Within the table, the following terms are used:

"DL"	PCH drives low
"DH"	PCH drives high
"IPU"	Internal pull-up
"IPD"	Internal pull-down
"T"	Toggling or signal is transitioning because function is not stopping.
"High-Z"	Tri-state—PCH not driving the signal high or low
"Defined"	Driven to a level that is defined by the function or external pull-up/pull-down resistor (will be high or low).
"Off"	The power plane is off; PCH is not driving when configured as an output or sampling when configured as an input.

**Note:** Pin state within table assumes interfaces are idle and default pin configuration for different power states.

Signal levels are the same in S3, S4, and S5, except as noted.

PCH suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# de-assertion. Some signals are determinate and defined prior to RSMRST# de-assertion; refer to signals with Note 21 references.

PCH core well signal states are indeterminate and undefined and may glitch prior to PCH\_PWROK assertion.

DSW indicates PCH Deep Sx Well. This state provides a few wake events and critical context to allow system to draw minimal power in S3, S4, or S5 states. PCH DSW well signal states are indeterminate and undefined and may glitch prior to DPWROK assertion. Some signals are determinate and defined prior to DPWROK assertion; refer to signals with Note 21 references.

ASW indicates PCH Active Sleep Well. This power well contains functionality associated with active usage models while the host system is in Sx. These are signals on VCCSPI.

**Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 1 of 5)**

Signal Name	Power Plane	During Reset <sup>1</sup>	Immediately After Reset <sup>1</sup>	S3/S4/S5	Deep Sx
<b>USB Interface</b>					
USB2n[7:0], USB2p[7:0]	DSW	IPD	IPD	IPD	IPD
USB3Tn[2:1], USB3Tp[2:1]	Suspend	IPD	IPD <sup>27</sup>	S3 IPD <sup>27</sup> S4/S5 Off	Off
USB3Tn[4:3], USB3Tp[4:3] <sup>19</sup>	Suspend	IPD	IPD <sup>27</sup>	S3 IPD <sup>27</sup> S4/S5 Off	Off
USBRBIAS	Core	High-Z	High-Z	Off	Off

Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 2 of 5)

Signal Name	Power Plane	During Reset <sup>1</sup>	Immediately After Reset <sup>1</sup>	S3/S4/S5	Deep Sx
<b>PCI Express*</b>					
PETp[2:1], PETn[2:1] <sup>19</sup>	Suspend	IPD <sup>27</sup>	IPD <sup>27</sup>	Off	Off
PETp[4:3], PETn[4:3]	Core	IPD <sup>27</sup>	IPD <sup>27</sup>	Off	Off
PETp5_L[3:0], PETn5_L[3:0]	Core	IPD <sup>27</sup>	IPD <sup>27</sup>	Off	Off
PETp6_L[3:0], PETn6_L[3:0]	Core	IPU	IPU	Off	Off
<b>SATA Interface</b>					
SATA_TXP[3:0], SATA_TXN[3:0]	Core	IPU	IPU	Off	Off
SATALED#	Core	High-Z	High-Z	Off	Off
<b>DEVSLP0</b> /GPIO33 <sup>22</sup>	Core	High-Z	High-Z	Off	Off
<b>DEVSLP1</b> /GPIO38 <sup>22</sup>	Core	High-Z	High-Z	Off	Off
<b>DEVSLP2</b> /GPIO39 <sup>22</sup>	Core	High-Z	High-Z	Off	Off
<b>Clocking Signals</b>					
CLKOUT_ITPXD_P, CLKOUT_ITPXD_N	Core	T	T	Off	Off
XTAL24_OUT	Core	High-Z	High-Z	Off	Off
DIFFCLK_BIASREF	Core	High-Z	High-Z	Off	Off
CLKOUT_PCIE[5:0] P, CLKOUT_PCIE[5:0] N	Core	T	T	Off	Off
CLKOUT_LPC[1:0] P <sup>10</sup> CLKOUT_LPC[1:0] N <sup>10</sup>	Core	T	T	Off	Off
PCIECLKRQ[5:0]#/ GPIO[23:18] <sup>22</sup>	Core	High-Z	High-Z	Off	Off
<b>Interrupts</b>					
<b>PIRQ[A:D]#</b> /GPIO[80:77] <sup>22</sup>	Core	High-Z	High-Z	Off	Off
SERIRQ	Core	High-Z	High-Z	Off	Off
<b>Backlight Control Signals</b>					
eDP_VDD_EN <sup>15</sup>	Core	DL	DL/High-Z <sup>18</sup>	Off	Off
eDP_BKL滕 <sup>15</sup>	Core	DL	DL/High-Z <sup>18</sup>	Off	Off
eDP_BKLTCTL <sup>15</sup>	Core	DL	DL/High-Z <sup>18</sup>	Off	Off
<b>Digital Display Interface</b>					
DDP[C:B]_AUXP, DDP[C:B]_AUXN	Core	IPD	IPD	Off	Off
eDP_AUXP, eDP_AUXN	Core	IPD	IPD	Off	Off
DDPB_CTRLCLK, DDPC_CTRLCLK	Core	High-Z	High-Z	Off	Off
DDPB_CTRLDATA <sup>6</sup> DDPC_CTRLDATA <sup>6</sup>	Core	IPD <sup>12</sup>	High-Z	Off	Off
<b>LPC/FWH Interface</b>					
LAD[3:0]	Core	IPU	IPU	Off	Off
LFRAME#	Core	DH	DH	Off	Off



**Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 3 of 5)**

Signal Name	Power Plane	During Reset <sup>1</sup>	Immediately After Reset <sup>1</sup>	S3/S4/S5	Deep Sx
<b>SMBus Interface</b>					
SMBCLK, SMBDATA	Suspend	High-Z	High-Z	High-Z	Off
<b>System Management Interface</b>					
<b>SMBALERT#/ GPIO11<sup>22</sup></b>	Suspend	High-Z	High-Z	High-Z	Off
SML0DATA	Suspend	High-Z	High-Z	High-Z	Off
SML0CLK	Suspend	High-Z	High-Z	High-Z	Off
<b>SML0ALERT#/ GPIO60<sup>22</sup></b>	Suspend	High-Z	High-Z	High-Z	Off
<b>SML1CLK/GPIO75<sup>22</sup></b>	Suspend	High-Z	High-Z	High-Z	Off
<b>SML1ALERT#/TEMP_ALERT#/ GPIO73<sup>22</sup></b>	Suspend	High-Z	High-Z	High-Z	Off
<b>SML1DATA/GPIO74<sup>22</sup></b>	Suspend	High-Z	High-Z	High-Z	Off
<b>Controller Link</b>					
CL_CLK <sup>7</sup>	Suspend	IPD <sup>8</sup>	IPD <sup>8</sup>	IPU/IPD	Off
CL_DATA <sup>7</sup>	Suspend	IPD <sup>8</sup>	IPD <sup>8</sup>	IPU/IPD	Off
CL_RST# <sup>7</sup>	Suspend	DL	DH	DH	Off
<b>SPI Interface</b>					
SPI_CLK	ASW	High-Z <sup>23</sup>	DL	DL	Off
SPI_CS0#	ASW	High-Z <sup>23</sup>	DH	DH	Off
SPI_CS1#	ASW	High-Z <sup>23</sup>	DH	DH	Off
SPI_CS2#	ASW	High-Z <sup>23</sup>	DH	DH	Off
SPI_MOSI	ASW	High-Z <sup>23</sup>	DL	DL	Off
SPI_MISO	ASW	High-Z <sup>23</sup>	IPU	IPU	Off
SPI_IO2	ASW	High-Z <sup>23</sup>	IPU	IPU	Off
SPI_IO3	ASW	High-Z <sup>23</sup>	IPU	IPU	Off
<b>Power Management</b>					
<b>CLKRUN#/GPIO32<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>HSIOPC/GPIO71<sup>28</sup></b>	Core	DH	DH	Off	Off
SM_DRAMRST# <sup>21</sup>	DSW	DL	High-Z	High-Z	High-Z
WAKE#	DSW	High-Z	High-Z	High-Z	High-Z/ IPD <sup>34</sup>
PME#	Suspend	IPU	IPU	IPU	Off
PLTRST#	Suspend	DL	DH	DL	Off
SLP_S0# <sup>21</sup>	Suspend	DH	DH	DH	Off
SLP_A# <sup>21</sup>	DSW	DL	DH	DH <sup>13</sup>	DL
SLP_S3# <sup>21</sup>	DSW	DL	DH	DL	DL
SLP_S4# <sup>21</sup>	DSW	DL	DH	DL/DH <sup>20</sup>	DL/DH <sup>30</sup>
<b>SLP_S5#/GPIO63<sup>11,21,28</sup></b>	DSW	DL	DH	DL/DH <sup>2</sup>	DL/DH <sup>30</sup>
<b>SUS_STAT#/GPIO61<sup>21,28,32</sup></b>	Suspend	DL	DH <sup>17</sup>	DL	Off
<b>SUSCLK/GPIO62<sup>21,28</sup></b>	Suspend	DL	T		Off
SLP_SUS# <sup>21</sup>	DSW	DL	DH	DH	DL

Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 4 of 5)

Signal Name	Power Plane	During Reset <sup>1</sup>	Immediately After Reset <sup>1</sup>	S3/S4/S5	Deep Sx
<b>SUSWARN#/SUSPWRDNACK/</b> GPIO30 <sup>21,24,26,28</sup>	Suspend	DL	DL	DL <sup>5</sup>	N/A
<b>SUSWARN#/SUSPWRDNACK/</b> GPIO30 <sup>21,25,26,28</sup>	Suspend	DL	DL	DL	Off
<b>LAN_PHY_PWR_CTRL/</b> GPIO12 <sup>11,21,28</sup>	DSW	DL	DL	DL	DL
SLP_LAN# <sup>21</sup>	DSW	DL	DL	DL/DH <sup>33</sup>	DL/DH <sup>33</sup>
<b>SLP_WLAN#/</b> GPIO29 <sup>11,14,21,28</sup>	DSW	DL	DL <sup>33</sup>	DL/DH <sup>33</sup>	DL <sup>33</sup>
<b>Miscellaneous Signals</b>					
<b>SPKR</b> /GPIO81 <sup>6,22</sup>	Core	IPD	DL	Off	Off
<b>Intel® High Definition Audio (Intel® HD Audio) Interface</b>					
<b>HDA_RST#/I2S_MCLK</b>	Suspend/Core	DL	DL <sup>3</sup>	DL <sup>29</sup>	Off
<b>HDA_SDO<sup>4,6</sup>/I2S0_TXD</b>	Suspend/Core	IPD	IPD	IPD <sup>29</sup>	Off
<b>HDA_SYNC<sup>6</sup>/I2S0_SFRM</b>	Suspend/Core	IPD	IPD	IPD <sup>29</sup>	Off
<b>HDA_BCLK/I2S0_SCLK</b>	Suspend/Core	DL	DL <sup>3</sup>	DL <sup>29</sup>	Off
<b>HDA.Dock_EN#/I2S1_TXD</b>	Suspend/Core	DH	DH <sup>16</sup>	DH <sup>16,29</sup>	Off
<b>HDA.Dock_RST#/I2S1_SFRM</b>	Suspend/Core	DL	DL <sup>9</sup>	DL <sup>9,29</sup>	Off
<b>I<sup>2</sup>S Interface</b>					
<b>HDA_RST#/I2S_MCLK</b>	Suspend/Core	DL	DL	DL <sup>29</sup>	Off
<b>HDA_SDO/I2S0_TXD<sup>7</sup></b>	Suspend/Core	IPD	IPD	IPD <sup>29</sup>	Off
<b>HDA_SYNC/I2S0_SFRM</b>	Suspend/Core	IPD	IPD	IPD <sup>29</sup>	Off
<b>HDA_BCLK/I2S0_SCLK</b>	Suspend/Core	DL	DL <sup>3</sup>	DL <sup>29</sup>	Off
<b>HDA.Dock_EN#/I2S1_TXD</b>	Suspend/Core	DH	DH	DH <sup>29</sup>	Off
<b>HDA.Dock_RST#/I2S1_SFRM</b>	Suspend/Core	DL	DL	DL <sup>29</sup>	Off
I2S1_SCLK	Suspend/Core	DL	DL	DL <sup>29</sup>	Off
<b>General Purpose SPI Interface</b>					
<b>GSPI0_CS#/GPIO83<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>GSPI0_CLK#/GPIO84<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>GSPI0_MOSI/GPIO86<sup>6,22</sup></b>	Core	IPD	DL	Off	Off
<b>GSPI1_CS#/GPIO87<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>GSPI1_CLK#/GPIO88<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>GSPI1_MOSI/GPIO90<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>UART Interface</b>					
<b>UART0_TXD/GPIO92<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>UART0_RST#/GPIO93<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>UART1_TXD/GPIO1<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>UART1_RST#/GPIO2<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off

**Table 3-2. Power Plane and States for Output and I/O Signals for Configurations (Sheet 5 of 5)**

Signal Name	Power Plane	During Reset <sup>1</sup>	Immediately After Reset <sup>1</sup>	S3/S4/S5	Deep Sx
<b>I<sup>2</sup>C Interface</b>					
<b>I2C0_SDA/GPIO4<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>I2C0_SCL/GPIO5<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>I2C1_SDA/GPIO6<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>I2C1_SCL/GPIO7<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>SDIO Interface</b>					
<b>SDIO_CLK/GPIO64<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>SDIO_CMD/GPIO65<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
SDIO_D0/GPIO66 <sup>6,22</sup>	Core	IPD	DL	Off	Off
<b>SDIO_D[3:1]/GPIO[69:67]<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>SDIO_POWER_EN/GPIO70<sup>22</sup></b>	Core	High-Z	High-Z	Off	Off
<b>Multiplexed GPIO Signals (Defaults to Native Mode) Used as GPIO</b>					
HSIOPC/ <b>GPIO71<sup>32</sup></b>	Core	DH	DH	Off	Off
SLP_S5#/ <b>GPIO63<sup>11,21,32</sup></b>	DSW	DL	DH	High-Z	High-Z
SUS_STAT#/ <b>GPIO61<sup>21,32</sup></b>	Suspend	DL	DH <sup>17</sup>	High-Z	Off
SUSCLK/ <b>GPIO62<sup>21,32</sup></b>	Suspend	DL	T	High-Z	Off
SUSWARN#/SUSPWRDNACK/ <b>GPIO30<sup>21,26,32</sup></b>	Suspend	DL	DL	High-Z	N/A
LAN_PHY_PWR_CTRL/ <b>GPIO12<sup>11,21,32</sup></b>	DSW	DL	DL	High-Z	High-Z
SLP_WLAN#/ <b>GPIO29<sup>11,14,21,32</sup></b>	DSW	DL	DL	High-Z	High-Z
BATLOW#/ <b>GPIO72<sup>32</sup></b>	DSW	High-Z	High-Z	High-Z	High-Z
<b>Multiplexed GPIO Signals (Defaults to GPO)</b>					
SDIO_D0/ <b>GPIO66<sup>6,32</sup></b>	Core	IPD	DL	Off	Off
SPKR/ <b>GPIO81<sup>6,32</sup></b>	Core	IPD	DL	Off	Off
GSPI0_MOSI/ <b>GPIO86<sup>6,32</sup></b>	Core	IPD	DL	Off	Off
<b>UnMultiplexed GPIO Signals (Defaults to GPO)</b>					
GPIO15 <sup>6,32</sup>	Suspend	IPD	DL	DL	Off
<b>Testability</b>					
PCH_TDO	Suspend	High-Z	High-Z	High-Z	Off
PCH_TDI	Suspend	IPU	IPU	IPU	Off
PCH_TMS	Suspend	IPU	IPU	IPU	Off
PCH_TCK	Suspend	IPD	IPD	IPD	Off

**Notes:**

1. The states of signals on Core power planes are evaluated at the times during PLTRST# and immediately after PLTRST#. The states of the Controller Link signals are taken at the times during CL\_RST# and immediately after CL\_RST#. The states of the Suspend signals are evaluated at the times during RSMRST# and immediately after RSMRST#, with an exception to GPIO signals; refer to [Section 2.24](#) for more details on GPIO state after reset. The states of the HDA signals are evaluated at the times during HDA\_RST# and immediately after HDA\_RST#. The states of signals on DSW power planes are evaluated at times during DPWROK and immediately after DPWROK assertion.
2. SLP\_S5# signal will be driven high in the S3 and S4 state and driven low in the S5 state.



3. Internal pull-down enabled when PCH\_PWROK de-asserts until Intel® High Definition Audio Controller Reset bit is set (D27:F0:Offset HDBAR+08h:bit 0), at which time HDA\_RST# will be High and HDA\_BCLK will start to toggle.
4. Internal pull-down on HDA\_SDO enabled during reset.
5. Pin state always driven low during S0 or Sx/M3. In Sx/M-Off, pin may be driven low or high based on Intel® ME policy.
6. This signal is sampled as a functional strap During Reset. Refer to Functional straps definition table for usage.
7. Controller Link Clock and Data buffers use internal pull-up and pull-down resistors to drive a logical 1 or 0.
8. I/O buffer pull-down is enabled.
9. This pin will be driven to high when Dock Attach bit is set (Docking Control Register D27:F0 Offset 4Ch).
10. The pull-down is disabled after the pins are driven strongly to 0 when PCH\_PWROK is asserted.
11. Native/GPIO functionality controlled using soft straps. Default to Native functionality until soft straps are loaded.
12. External 2.2 kΩ pull-up when used.
13. The SLP\_A# state will be determined by Intel® ME policies.
14. SLP\_WLAN# behavior after reset is dependent on value of SLP\_WLAN# default value bit. A soft strap is used to select between SLP\_WLAN# and GPIO usage. When strap is set to 0 (default), pin is used as SLP\_WLAN#, when soft strap is set to 1, pin is used as GPIO29.
15. Glitch free power sequencing.
16. This pin will be driven low when Dock Attach bit is set (Docking Control Register D27:F0 Offset 4Ch).
17. Driven high after PCH\_PWROK rises.
18. Pins are tri-stated when eDP is disabled.
19. USB 3.0 or PCIe\* mode selection is based on soft strap.
20. SLP\_S4# signal will be driven high in the S3 state and driven low in the S4 and S5 state.
21. The pin requires glitch-free output power sequence. The pull-down is momentarily when the corresponding buffer power supply is not stable.
22. Pin defaults to GPIO mode. The pin state during and immediately after reset follows default GPIO mode pin state. The pin state for S0 to Deep Sx reflects assumption that GPIO Use Select register was programmed to native mode functionality. If GPIO Use Select register is programmed to GPIO mode, refer to Multiplexed GPIO (Defaults to GPIO Mode) section for the respective pin states in S0 to Deep Sx. For SML1CLK/GPIO75 and SML1DATA/GPIO74, during Sx/Moff, the pins revert to GPIO.
23. Pins are tri-stated prior to RSMRST# de-assertion.
24. Pin-state indicates SUSPWRDNACK in Non-Deep Sx, Deep Sx after RTC power failure.
25. Pin-state indicates SUSWARN# in Deep Sx supported platforms.
26. SUSPWRDNACK is the default mode of operation. If system supports Deep Sx, subsequent boots will default to SUSWARN#
27. This is a strong pull low.
28. Pin defaults to native mode. The pin state during and immediately after reset follows default native mode pin state. The pin state for S0 to Deep Sx reflects assumption that GPIO Use Select register was kept at native mode functionality. If GPIO Use Select register is programmed to GPIO mode, refer to Multiplexed GPIO (Defaults to Native Mode) section for the respective pin states in S0 to Deep Sx.
29. Buffer is off if connected to Core power.
30. When platform enters Deep Sx, pin will retain the value held prior to Deep Sx entry. If platform was in S5 prior to Deep Sx, SLP\_S3#, SLP\_S4#, SLP\_S5# will be asserted. If platform was in S4 prior to Deep Sx, SLP\_S3# and SLP\_S4# will be asserted while SLP\_S5# will be de-asserted.
31. N/A
32. Internal weak pull resistor is default off but configurable (pull-up/pull-down/none) after boot. The pin may be IPD or IPU depending on configuration by means of the GPIO register settings.
33. Pin may toggle from RSMRST# de-assertion to PLTRST# de-assertion due to Intel® ME. Based on wake events and Intel® ME state/policy.
34. Based on configuration, pin maybe High-Z or IPD.
35. Not all signals or pin functionalities may be available on a given SKU. See [Section 2.3](#) and [Chapter 2](#) for details.



### 3.3

## Power Planes for Input Signals

Table 3-3 shows the power plane associated with each input signal, as well as the state at various times. Within the table, the following terms are used:

"IPU"	Internal pull-up
"IPD"	Internal pull-down
"T"	Toggling or signal is transitioning because function is not stopping.
"High-Z"	Tri-state—PCH not driving the signal high or low
"Defined"	Driven to a level that is defined by the function or external pull-up/pull-down resistor (will be high or low).
"Off"	The power plane is off; PCH is not driving when configured as an output or sampling when configured as an input.

**Note:** Pin state within table assumes interfaces are idle and default pin configuration for different power states.

Signal levels are the same in S3, S4, and S5, except as noted.

PCH suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# de-assertion.

PCH core well signal states are indeterminate and undefined and may glitch prior to PCH\_PWROK assertion.

DSW indicates PCH Deep Sx Well. This state provides a few wake events and critical context to allow system to draw minimal power in S3, S4, or S5 states. PCH DSW well signal states are indeterminate and undefined and may glitch prior to DPWROK assertion.

ASW indicates PCH Active Sleep Well. This power well contains functionality associated with active usage models while the host system is in Sx.

**Table 3-3. Power Plane for Input Signals for Mobile Configurations (Sheet 1 of 3)**

Signal Name	Power Plane	During Reset	Immediately After Reset	S3/S4/S5	Deep Sx
<b>USB Interface</b>					
USB2n[7:0], USB2p[7:0]	DSW	IPD	IPD	IPD	IPD
USB3Rn[2:1], USB3Rp[2:1]	Suspend	IPD <sup>2</sup>	IPD <sup>1</sup>	S3 IPD <sup>1</sup> S4/S5 Off	Off
USB3Rn[4:3], USB3Rp[4:3] <sup>3</sup>	Suspend	IPD <sup>2</sup>	IPD <sup>1</sup>	S3 IPD <sup>1</sup> S4/S5 Off	Off
USBRBIAS#	Core	High-Z	High-Z	Off	Off
<b>PCI Express*</b>					
PERp[2:1], PERn[2:1] <sup>3</sup>	Suspend	IPD <sup>5</sup>	IPD	Off	Off
PERp[4:3], PERn[4:3]	Core	IPD <sup>5</sup>	IPD	Off	Off

Table 3-3. Power Plane for Input Signals for Mobile Configurations (Sheet 2 of 3)

Signal Name	Power Plane	During Reset	Immediately After Reset	S3/S4/S5	Deep Sx
PERp5_L[3:0], PERn5_L[3:0]	Core	IPD <sup>5</sup>	IPD	Off	Off
PERp6_L[3:0], PERn6_L[3:0]	Core	IPD <sup>5</sup>	IPD	Off	Off
PCIe_RCOMP	Core	High-Z	High-Z	Off	Off
PCIe_IREF	Core	High-Z	High-Z	Off	Off
<b>SATA Interface</b>					
SATA_RXP[3:0], SATA_RXN[3:0]	Core	IPD	IPD	Off	Off
SATA_IREF	Core	High-Z	High-Z	Off	Off
SATA_RCOMP	Core	High-Z	High-Z	Off	Off
<b>Multiplexed GPIO Signals (Defaults to GPI Mode) Used as GPIO</b>					
PCIECLKRQ[5:0]#/GPIO[23:18] <sup>4</sup>	Core	High-Z	High-Z	Off	Off
ACPRESENT/GPIO31 <sup>4</sup>	DSW	High-Z	High-Z	High-Z	High-Z/ IPD <sup>8</sup>
CLKRUN#/GPIO32 <sup>4</sup>	Core	High-Z	High-Z	Off	Off
DEVSLP0/GPIO33 <sup>4</sup>	Core	High-Z	High-Z	Off	Off
DEVSLP1/GPIO38 <sup>4</sup>	Core	High-Z	High-Z	Off	Off
DEVSLP2/GPIO39 <sup>4</sup>	Core	High-Z	High-Z	Off	Off
SATA[3:0]GP/GPIO[37:34] <sup>4,6</sup>	Core	High-Z	High-Z	Off	Off
OC[3:0]#/GPIO[43:40] <sup>4</sup>	Suspend	High-Z	High-Z	High-Z	Off
BMBUSY#/GPIO76 <sup>4</sup>	Core	High-Z	High-Z	Off	Off
GPIO[94:87,85:83,70:67,65:64,7:0] <sup>4</sup>	Core	High-Z	High-Z	Off	Off
SMBALERT#/GPIO11 <sup>4</sup>	Suspend	High-Z	High-Z	High-Z	Off
SML0ALERT#/GPIO60 <sup>4</sup>	Suspend	High-Z	High-Z	High-Z	Off
SML1CLK/GPIO75 <sup>4</sup>	Suspend	High-Z	High-Z	High-Z	Off
SML1ALERT#/TEMP_ALERT#/GPIO73 <sup>4</sup>	Suspend	High-Z	High-Z	High-Z	Off
SML1DATA/GPIO74 <sup>4</sup>	Suspend	High-Z	High-Z	High-Z	Off
PIRQ[A:D]#/GPIO[80:77] <sup>4</sup>	Core	High-Z	High-Z	Off	Off
RCIN#/GPIO82 <sup>4</sup>	Core	High-Z	High-Z	Off	Off
<b>Non-Multiplexed GPIO Signals (Defaults to GPI)</b>					
GPIO[59:56,47:44,28,26,24,14:13,10:8] <sup>4</sup>	Suspend	High-Z	High-Z	High-Z	Off
GPIO[55:48,17:16] <sup>4</sup>	Core	High-Z	High-Z	Off	Off
GPIO25 <sup>4</sup>	DSW	High-Z	High-Z	High-Z	High-Z
GPIO27 <sup>4</sup>	DSW	High-Z	High-Z	High-Z	High-Z/ IPD <sup>8</sup>

**Table 3-3. Power Plane for Input Signals for Mobile Configurations (Sheet 3 of 3)**

Signal Name	Power Plane	During Reset	Immediately After Reset	S3/S4/S5	Deep Sx
<b>Clock Interface</b>					
XTAL24_IN	Core	High-Z	High-Z	Off	Off
<b>Digital Display Interface</b>					
DDP[B:C:]_HPD	Core	High-Z	High-Z	Off	Off
eDP_HPD	Core	High-Z	High-Z	Off	Off
<b>Power Management</b>					
<b>BATLOW#/GPIO72<sup>1</sup></b>	DSW	High-Z	High-Z	High-Z	High-Z
APWROK	Suspend	High-Z	High-Z	High-Z	Off
PWRBTN#	DSW	IPU	IPU	IPU	IPU
PCH_PWROK	RTC	High-Z	High-Z	High-Z	High-Z
SYS_PWROK	Suspend	High-Z	High-Z	High-Z	Off
DPWROK	RTC	High-Z	High-Z	High-Z	High-Z
RSMRST#	RTC	High-Z	High-Z	High-Z	High-Z
SYS_RESET#	Core	High-Z	High-Z	Off	Off
BMBUSY#	Core	High-Z	High-Z	Off	Off
<b>System Management Interface</b>					
INTRUDER#	RTC	High-Z	High-Z	High-Z	High-Z
<b>Miscellaneous Signals</b>					
INTVRMEN <sup>7</sup>	RTC	High-Z	High-Z	High-Z	High-Z
DSWVRMEN <sup>7</sup>	RTC	High-Z	High-Z	High-Z	High-Z
RTCRST#	RTC	High-Z	High-Z	High-Z	High-Z
SRTCST#	RTC	High-Z	High-Z	High-Z	High-Z
OPI_RCOMP	Core	High-Z	High-Z	Off	Off
<b>RCIN#/GPIO82<sup>1</sup></b>	Core	High-Z	High-Z	Off	Off
<b>General Purpose SPI Interface</b>					
<b>GSPI0_MISO/GPIO85<sup>1</sup></b>	Core	High-Z	High-Z	Off	Off
<b>GSPI1_MISO/GPIO89<sup>1</sup></b>	Core	High-Z	High-Z	Off	Off
<b>UART Interface</b>					
<b>UART0_RXD/GPIO91<sup>10</sup></b>	Core	High-Z	High-Z	Off	Off
<b>UART0_CTS#/GPIO94<sup>10</sup></b>	Core	High-Z	High-Z	Off	Off
<b>UART1_RXD/GPIO0<sup>10</sup></b>	Core	High-Z	High-Z	Off	Off
<b>UART1_CTS#/GPIO3<sup>10</sup></b>	Core	High-Z	High-Z	Off	Off
<b>I<sup>2</sup>S Interface</b>					
HDA_SDI[1:0]/ <b>I<sup>2</sup>S[1:0]_RXD</b>	Suspend	High-Z	High-Z	High-Z <sup>9</sup>	Off

**Notes:**

1. This is a strong pull low.
2. USB 3.0 Rx pins transition from Z to L during Reset.
3. USB 3.0 or PCIe\* mode selection is based on soft strap.

4. Internal weak pull resistor is default off but configurable (pull-up/pull-down/none) after boot. The pin may be IPD or IPU depending on configuration by means of the GPIO register settings.
5. PCIe\* Rx pins transition from Z to L during Reset.
6. Pin may default to native mode, if soft strap corresponding to this pin is assigning PCIe\*/SATA multiplexing selection to be based on the input value of this pin (Flex I/O soft strap SATAPx\_PCIEPx\_MODE = 11b)
7. This signal is sampled as a functional strap during Reset. Refer to [Table 2-28, "Functional Strap Definitions" on page 98](#) for usage.
8. Configurable, pin maybe High-Z or IPD.
9. Buffer is off if connected to core power.
10. Pin defaults to GPI but can be used as GPO or as native functionality.
11. Not all signals or pin functionalities may be available on a given SKU. See [Section 2.3](#) and [Chapter 2](#) for details.

§ §



## 4 PCH and System Clocks

The PCH provides a complete system clocking solution through Integrated Clocking.

PCH based platforms require several single-ended and differential clocks to synchronize signal operation and data propagation system-wide between interfaces and across clock domains. In Integrated Clock mode, all the system clocks will be provided by PCH from a 24 MHz crystal generated clock input.

The output signals from PCH are:

- Six, 100 MHz differential sources for PCI Express\* 2.0 devices
- One, 100 MHz differential clock for XDP/ITP
- Two, 24 MHz single-ended sources for other LPC devices.

### 4.1 Platform Clocking Requirements

Providing a platform-level clocking solution uses multiple system components including:

- The PCH
- 24 MHz crystal source

Table 4-1 shows the system clock input to PCH. Table 4-2 shows system clock outputs generated by PCH.

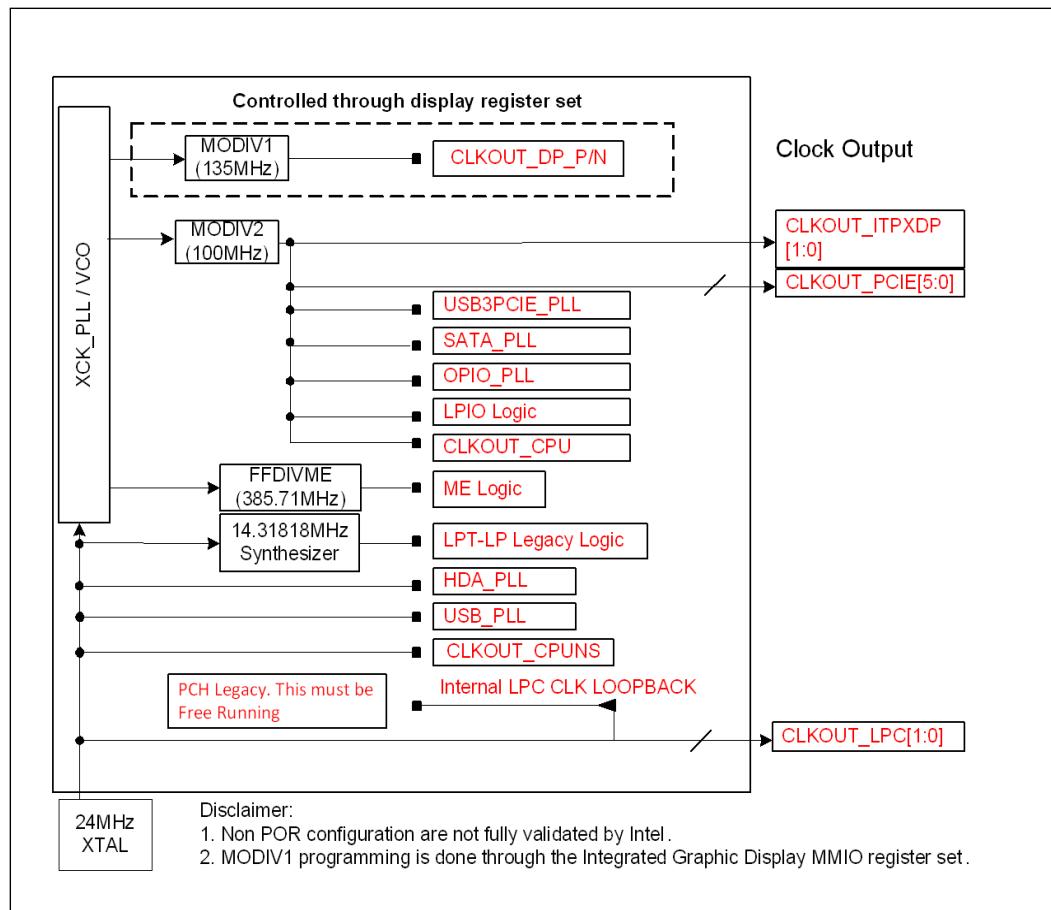
**Table 4-1. PCH Clock Inputs**

Clock Domain	Frequency	Usage Description
XTAL24_IN	24 MHz	Crystal input source used by PCH.

**Table 4-2. Clock Outputs**

Clock Domain	Frequency	Spread Spectrum	Usage
CLKOUT_LPC[1:0]	24 MHz	No	Single Ended 24 MHz outputs to LPC devices.
CLKOUT_PCIE[5:0]_P, CLKOUT_PCIE[5:0]_N	100 MHz	Yes	100 MHz PCIe* 2.0 specification compliant differential output to PCI Express* devices.
CLKOUT_ITPXPDP_P, CLKOUT_ITPXPDP_N	100 MHz	Yes	Primarily used as 100 MHz Clock to processor XDP/ITP on the platform.
SPI_CLK	17.86 MHz/ 20.83 MHz 31.25 MHz	No	Drive SPI devices connected to the PCH. Generated by the PCH.

Figure 4-1. PCH Internal Clock Diagram



## 4.2 Functional Blocks

The PCH has one main PLL in which its output is divided down through Modulators and Dividers to provide great flexibility in clock source selection, configuration, and better power management.

Table 4-3, describes the PLLs on the PCH and the clock domains that are driven from the PLLs.

Table 4-3. PCH PLLs

PLL	Outputs <sup>1</sup>	Description/Usage
XCK_PLL	Four 2.7 GHz outputs 90° apart. Outputs are routed to each of the Spread Modulator blocks before hitting the various dividers and the other PLLs to provide clocks to all of the I/O interface logic. Also provides 5.4 GHz and 2.7 GHz CMOS outputs for use by various dividers to create non-spread output clocks.	Main Reference PLL—always enabled, but is subject to dynamic power management based on system idle condition.

**Note:**

1. Indicates the source clock frequencies driven to other internal logic for delivering functionality needed. Does not indicate external outputs.



**Table 4-4**, provides a basic description of the available spread modulators. The spread modulators each operate on the XCK PLL's 2.7 GHz outputs. Spread Spectrum tuning and adjustment can be made on the fly without a platform reboot using specific programming sequence to the clock registers.

**Table 4-4. Modulator Blocks**

Modulator	Description
MOD1	Used for spread modulation, or bending, on 135 MHz clock to integrated graphics display. Typical display usage model is 0.5% down spread. In certain usage case, can be shut off for 0% spread with or without clock bending. Used by the display driver only.
MOD2	Used for spread modulation and fine grain frequency synthesis on nominal 100 MHz clock to processor, ITP, PCIe*, USB 3.0, SATA, and misc internal I/O. Also subject to adaptive clocking adjustment (for RFI reduction) when left on at nominal 100 MHz frequency.

## 4.3 Straps Related to Clock Configuration

There are no functional (pin) straps required for clock configuration.

The following soft-straps are implemented on the PCH for Clock Configuration:  
Integrated Clocking Profile Select: 4 Profile select bits allow up to 16 different clock profiles to be specified in the SPI flash device. In addition, 4 RTC well backed host register bits are also defined for Integrated Clocking Profile Selection through BIOS.

## 4.4 Clock Configuration Access Overview

The PCH provides increased flexibility of host equivalent configurability of clocks, using Intel® ME firmware.

In the Intel® ME firmware assisted configuration mode, Control settings for PLLs, Spread Modulators and other clock configuration registers will be handled by the Intel® ME engine. The parameters to be loaded will reside in the Intel® ME data region of the SPI Flash device. BIOS would only have access to the register set through a set of Intel® MEI commands to the Intel® ME.

## 4.5 Integrated Clock Controller (ICC) Registers

This section describes all registers and base functionality that is related to the Integrated Clock Controller. The ICC registers are not visible by means of PCI Configuration access and they are not mapped to I/O memory as other devices within the PCH. The control settings for the ICC clock structure is located in registers directly under the control of the Intel® Management Engine (Intel® ME).

ICC register access is only accessible by means of Intel® ME firmware and must be programmed by means of available firmware access tools. The ICC registers in this chapter cover user adjustable features within the ICC subsystem programmable through available firmware access tools.

## 4.5.1 ICC Registers Under Intel® Management Engine (Intel® ME) Control

Mnemonic	Register Name	Default
SSCDIVINPHASE_CPU100	100 MHz SSC Divider Integer Phase Direction	00000032h
SSCTRIPARAM_CPU100	100 MHz SSC Triangle Parameter	12404038
OCKEN	Output Clock Enables	713F0003h
TMCPCIECLK	Timing Control PCIe* Clock	00000000h
ENPCIECLKREQ	Enable Control PCIe* CLKREQ	00000000h
SEOBP	Single Ended Buffer Parameters	00000099h
PM	Power Management Clock	00000000h
PMPCIECLK	Power Management PCIe* Clock	0002C688h

### 4.5.1.1 **SSCDIVINPHASE\_CPU100—100 MHz Clock SSC Divider Integer Phase Direction Register**

**FCIM Hardware Default:** 0000\_0032h

**Description:** This register is used for tuning PCIe\* Adaptive Clocking frequency.

Bit	Description
31:0	<b>SSCDIVINPHASE_CPU100 Field 1</b> —R/W. Firmware may program this field with various values to tune PCIe* adaptive clocking frequency.

### 4.5.1.2 **SSCTRIPARAM\_CPU100—100 MHz Clock SSC Triangle Direction Register**

**FCIM Hardware Default:** 1240\_4038h

**Description:** This register is used for SSC spread control of the 100 MHz clock output.

Bit	Description
31:0	<b>SSCTRIPARAM_CPU100 Field 1</b> —R/W. Firmware may program this field with various values when SSC is enabled.

### 4.5.1.3 OCKEN—Output Clock Enable Register

**FCIM Hardware Default:** 713F\_0003h

**Description:** This register controls the clock enables for all clock outputs.

Bit	Description
31:25	Reserved
24	<b>CLKOUT_ITPXD Clock Output Clock Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)
23:22	Reserved
21	<b>CLKOUT_PCIE5 Output Clock Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)
20	<b>CLKOUT_PCIE4 Output Clock Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)
19	<b>CLKOUT_PCIE3 Output Clock Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)
18	<b>CLKOUT_PCIE2 Output Clock Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)
17	<b>CLKOUT_PCIE1 Output Clock Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)
16	<b>CLKOUT_PCIE0 Output Clock Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)
15:2	Reserved
1	<b>24 MHz CLKOUT_LPC1 Output Clock 1 Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)
0	<b>24 MHz CLKOUT_LPC0 Output Clock 0 Enable</b> —R/W 0 = Output is gated to a low state. 1 = Output is enabled to toggle (Default)

### 4.5.1.4 TMCPCECLK—Timing Control PCIe\* Clock Register

**FCIM Hardware Default:** 0000\_0000h

**Description:** This register controls minimum timing of PCIe\* Clocks for L1Off using CLKREQ#.

Bit	Description
31:0	<b>TMCPCECLK Field 1</b> —R/W. Firmware may program this field with various values for L1Off.

#### 4.5.1.5 ENPCIECLKRQ—Enable Control PCIe\* CLKREQ Register

**FCIM Hardware Default:** 0000\_0000h

**Description:** This register controls the enabling of CLKREQs for PCIe\* clocks.

Bit	Description
31:6	Reserved
5	<b>Enable CLKREQ# for CLKOUT_PCIE5</b> —R/W. This field enables the CLKOUT_PCIE5 by the mapped CLKREQ. 0 = Disable dynamic control of CLKOUT_PCIE5 (Default) 1 = Enable dynamic control of CLKOUT_PCIE5
4	<b>Enable CLKREQ# for CLKOUT_PCIE4</b> —R/W. This field enables the CLKOUT_PCIE4 by the mapped CLKREQ. 0 = Disable dynamic control of CLKOUT_PCIE4 (Default) 1 = Enable dynamic control of CLKOUT_PCIE4
3	<b>Enable CLKREQ# for CLKOUT_PCIE3</b> —R/W. This field enables the CLKOUT_PCIE3 by the mapped CLKREQ. 0 = Disable dynamic control of CLKOUT_PCIE3 (Default) 1 = Enable dynamic control of CLKOUT_PCIE3
2	<b>Enable CLKREQ# for CLKOUT_PCIE2</b> —R/W. This field enables the CLKOUT_PCIE2 by the mapped CLKREQ. 0 = Disable dynamic control of CLKOUT_PCIE2 (Default) 1 = Enable dynamic control of CLKOUT_PCIE2
1	<b>Enable CLKREQ# for CLKOUT_PCIE1</b> —R/W. This field enables the CLKOUT_PCIE1 by the mapped CLKREQ. 0 = Disable dynamic control of CLKOUT_PCIE1 (Default) 1 = Enable dynamic control of CLKOUT_PCIE1
0	<b>Enable CLKREQ# for CLKOUT_PCIE0</b> —R/W. This field enables the CLKOUT_PCIE0 by the mapped CLKREQ. 0 = Disable dynamic control of CLKOUT_PCIE0 (Default) 1 = Enable dynamic control of CLKOUT_PCIE0

#### 4.5.1.6 SEOBP—Single-Ended Output Buffer Parameters Register

**FCIM Hardware Default:** 0000\_0099h

**Description:** This register controls the buffer parameters of the single ended LPC clocks.

Bit	Description
31:8	Reserved
7:4	<p><b>CLKOUT_LPC1 Buffer Parameters</b>—R/W. These settings control the parameter of the CLKOUT_LPC1 output Buffer.</p> <p>Bit 4 is for single or dual loading. 1 = 17 Ohm double-load usage 0 = 25 Ohm single-load usage</p> <p>Bits 7:5 is for slew rate control. Each bit step change corresponds to ~0.2V/ns. 000 = 0.6V/ns minimum 100 = 1.4V/ns (Default) 111 = 2.0V/ns maximum</p> <p><b>Note:</b> Register Default is '1001b'. Firmware will override bit 4 to '0'.</p>
3:0	<p><b>CLKOUT_LPC0 Buffer Parameters</b>—R/W. These settings control the parameter of the CLKOUT_LPC0 output Buffer.</p> <p>Bit 0 is for single or dual loading. 1 = 17 Ohm double-load usage 0 = 25 Ohm single-load usage</p> <p>Bits 3:1 is for slew rate control. Each bit step change corresponds to ~0.2V/ns. 000 = 0.6V/ns minimum 100 = 1.4V/ns (Default) 111 = 2.0V/ns maximum</p> <p><b>Note:</b> Register Default is '1001b'. Firmware will override these bits to '0'.</p>

#### 4.5.1.7 PM—Power Management Clock

**FCIM Hardware Default:** 0000\_0000h

**Description:** This register controls the power management features of LPC clock outputs.

Bit	Description
31:2	Reserved
1	<p><b>CLKRUN Control Enable for CLKOUT_LPC1 output</b>—R/W</p> <p>This field Controls the enabling of support for CLKRUN protocol on the 24 MHz clock outputs. 0 = CLKRUN Control is disabled and clocks are free running (Default) 1 = CLKRUN Control is enabled and clocks outputs can be turned off</p>
0	<p><b>CLKRUN Control Enable for CLKOUT_LPC2 output</b>—R/W</p> <p>This field Controls the enabling of support for CLKRUN protocol on the 24 MHz clock outputs. 0 = CLKRUN Control is disabled and clocks are free running (Default) 1 = CLKRUN Control is enabled and clocks outputs can be turned off</p>

#### 4.5.1.8 PMSRCCLK—Power Management PCIe\* Clock Register

**FCIM Hardware Default:** 0002\_C688h

**Description:** This register controls the power management features for PCIe\* clocks.

Bit	Description
31:18	Reserved
17:15	<p><b>CLKRQ# Select for CLKOUT_PCIE5—R/W</b>            Select version of external input CLKRQ# for dynamic control of the output CLKOUT_PCIE5.            000 = PCIECLKRQ0# (GPIO 18) controls CLKOUT_PCIE5            001 = PCIECLKRQ1# (GPIO 19) controls CLKOUT_PCIE5            010 = PCIECLKRQ2# (GPIO 20) controls CLKOUT_PCIE5            011 = PCIECLKRQ3# (GPIO 21) controls CLKOUT_PCIE5            100 = PCIECLKRQ4# (GPIO 22) controls CLKOUT_PCIE5            101 = PCIECLKRQ5# (GPIO 23) controls CLKOUT_PCIE5            110 - 111 = RSVD</p> <p>Default setting is '101b' enabling PCIECLKRQ5# to control CLKOUT_PCIE5 output.</p> <p><b>Note:</b> PCIECLKRQn# assignment is fixed to the PCIE Root Port (n+1); it cannot be remapped. CLKOUT_PCIEn can be mapped to any PCIE Root Portn using FITC tool.</p>
14:12	<p><b>CLKRQ# Select for CLKOUT_PCIE4—R/W</b>            Select version of external input CLKRQ# for dynamic control of the output CLKOUT_PCIE4.            000 = PCIECLKRQ0# (GPIO 18) controls CLKOUT_PCIE4            001 = PCIECLKRQ1# (GPIO 19) controls CLKOUT_PCIE4            010 = PCIECLKRQ2# (GPIO 20) controls CLKOUT_PCIE4            011 = PCIECLKRQ3# (GPIO 21) controls CLKOUT_PCIE4            100 = PCIECLKRQ4# (GPIO 22) controls CLKOUT_PCIE4            101 = PCIECLKRQ5# (GPIO 23) controls CLKOUT_PCIE4            110 - 111 = RSVD</p> <p>Default setting is '100b' enabling PCIECLKRQ4# to control CLKOUT_PCIE4 output.</p> <p><b>Note:</b> PCIECLKRQn# assignment is fixed to the PCIE Root Port (n+1); it cannot be remapped. CLKOUT_PCIEn can be mapped to any PCIE Root Portn using FITC tool.</p>
11:9	<p><b>CLKRQ# Select for CLKOUT_PCIE3—R/W</b>            Select version of external input CLKRQ# for dynamic control of the output CLKOUT_PCIE3.            000 = PCIECLKRQ0# (GPIO 18) controls CLKOUT_PCIE3            001 = PCIECLKRQ1# (GPIO 19) controls CLKOUT_PCIE3            010 = PCIECLKRQ2# (GPIO 20) controls CLKOUT_PCIE3            011 = PCIECLKRQ3# (GPIO 21) controls CLKOUT_PCIE3            100 = PCIECLKRQ4# (GPIO 22) controls CLKOUT_PCIE3            101 = PCIECLKRQ5# (GPIO 23) controls CLKOUT_PCIE3            110 - 111 = RSVD</p> <p>Default setting is '011b' enabling PCIECLKRQ3# to control CLKOUT_PCIE3 output.</p> <p><b>Note:</b> PCIECLKRQn# assignment is fixed to the PCIE Root Port (n+1); it cannot be remapped. CLKOUT_PCIEn can be mapped to any PCIE Root Portn using FITC tool.</p>

Bit	Description
8:6	<p><b>CLKRQ# Select for CLKOUT_PCIE2</b>—R/W</p> <p>Select version of external input CLKRQ# for dynamic control of the output CLKOUT_PCIE2.</p> <p>000 = PCIECLKRQ0# (GPIO 18) controls CLKOUT_PCIE2      001 = PCIECLKRQ1# (GPIO 19) controls CLKOUT_PCIE2      010 = PCIECLKRQ2# (GPIO 20) controls CLKOUT_PCIE2      011 = PCIECLKRQ3# (GPIO 21) controls CLKOUT_PCIE2      100 = PCIECLKRQ4# (GPIO 22) controls CLKOUT_PCIE2      101 = PCIECLKRQ5# (GPIO 23) controls CLKOUT_PCIE2      110 – 111 = RSVD</p> <p>Default setting is '010b' enabling PCIECLKRQ2# to control CLKOUT_PCIE2 output.</p> <p><b>Note:</b> PCIECLKRQn# assignment is fixed to the PCIE Root Port (n+1); it cannot be remapped. CLKOUT_PCIEn can be mapped to any PCIE Root Portn using FITC tool.</p>
5:3	<p><b>CLKRQ# Select for CLKOUT_PCIE1</b>—R/W</p> <p>Select version of external input CLKRQ# for dynamic control of the output CLKOUT_PCIE1.</p> <p>000 = PCIECLKRQ0# (GPIO 18) controls CLKOUT_PCIE1      001 = PCIECLKRQ1# (GPIO 19) controls CLKOUT_PCIE1      010 = PCIECLKRQ2# (GPIO 20) controls CLKOUT_PCIE1      011 = PCIECLKRQ3# (GPIO 21) controls CLKOUT_PCIE1      100 = PCIECLKRQ4# (GPIO 22) controls CLKOUT_PCIE1      101 = PCIECLKRQ5# (GPIO 23) controls CLKOUT_PCIE1      110 – 111 = RSVD</p> <p>Default setting is '001b' enabling PCIECLKRQ1# to control CLKOUT_PCIE1 output.</p> <p><b>Note:</b> PCIECLKRQn# assignment is fixed to the PCIE Root Port (n+1); it cannot be remapped. CLKOUT_PCIEn can be mapped to any PCIE Root Portn using FITC tool.</p>
2:0	<p><b>CLKRQ# Select for CLKOUT_PCIE0</b>—R/W.</p> <p>Select version of external input CLKRQ# for dynamic control of the output CLKOUT_PCIE0.</p> <p>000 = PCIECLKRQ0# (GPIO 18) controls CLKOUT_PCIE0      001 = PCIECLKRQ1# (GPIO 19) controls CLKOUT_PCIE0      010 = PCIECLKRQ2# (GPIO 20) controls CLKOUT_PCIE0      011 = PCIECLKRQ3# (GPIO 21) controls CLKOUT_PCIE0      100 = PCIECLKRQ4# (GPIO 22) controls CLKOUT_PCIE0      101 = PCIECLKRQ5# (GPIO 23) controls CLKOUT_PCIE0      110 – 111 = RSVD</p> <p>Default setting is '000b' enabling PCIECLKRQ0# to control CLKOUT_PCIE0 output.</p> <p><b>Note:</b> PCIECLKRQn# assignment is fixed to the PCIE Root Port (n+1); it cannot be remapped. CLKOUT_PCIEn can be mapped to any PCIE Root Portn using FITC tool.</p>

## 4.5.2 Miscellaneous ICC Register

### 4.5.2.1 OC\_WDT\_CTL—Overclocking Watchdog Timer Control Register

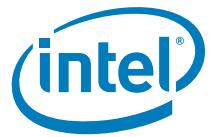
Address Offset 54h - 57h Attribute: WO, RO, RWC, RW,  
 Default Value: 00002000h Size: 32-bit RW/L, RW/L/V

Bit	Description
31	<p><b>Over-Clocking WDT Reload (OC_WDT_RLD)</b>—WO. Software can write a '1' to this bit to reload ("ping") the PCH over-clocking watchdog timer while it is running. A write of '0' to this bit has no effect. A write of „1“ to this bit while OC_WDT_EN=0, or with the clearing of OC_WDT_EN, does not start or reload the WDT (i.e. OC_WDT_EN takes precedence).</p> <p>The value in OC_WDT_TOV may be changed by software along with its setting of this bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value.</p> <p><b>Note:</b> This bit is on the Resume power well.</p>
30:26	<b>Reserved.</b>
25	<p><b>Over-Clocking WDT ICC Survive Mode Timeout Status (OC_WDT_ICCSURV_STS)</b>—RWC. This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that has ICC survivability impact (OC_WDT_ICCSURV=1). It is cleared by a software write of '1' or by the RSMRST# pin.</p> <p><b>Note:</b> This bit is on the Resume power well.</p>
24	<p><b>Over-Clocking WDT Non-ICC Survive Mode Timeout Status (OC_WDT_NO_ICCSURV_STS)</b>—RWC. This bit is set to '1' if the over-clocking WDT has timed out and triggered a global reset while running in a mode that does not have ICC survivability impact (OC_WDT_ICCSURV=0). It is cleared by a software write of '1' or by the RSMRST# pin.</p> <p><b>Note:</b> This bit is on the Resume power well.</p>
23:16	<p><b>Over-Clocking WDT Scratch pad (OC_WDT_SCRATCH)</b>—RW. This field is available as scratch pad space for software and has no effect on PCH hardware operation.</p> <p><b>Note:</b> This bit is on the Resume power well.</p>
15	<p><b>Over-Clocking WDT Force All (OC_WDT_FORCE_ALL)</b>—RW/L. GATE_BIT:OC_WDT_CTL.OC_WDT_CTL_LCK.HIGH When this bit is set to 1b and the OC_WDT is running, any included global reset source will behave as though the OC_WDT expired.</p> <p><b>Note:</b> This bit is on the Resume power well.</p>
14	<p><b>Over-Clocking WDT Enable (OC_WDT_EN)</b>—RW/L. Software sets this bit to '1' to enable the PCH over-clocking watchdog timer. While the counter is running, if it expires before being reloaded by software by means of the OC_WDT_RLD bit or halted by software clearing this bit, then one of the status bits will be set (which one depends on the WDT operating mode at the time - see the OC_WDT_ICCSURV bit description), and a global reset will be triggered.</p> <p>This bit is also set by the hardware when conditions allow the OC_WDT to self-start at power-cycle reboot (effectively changes the default of this bit as seen by software).</p> <p><b>Note:</b> This bit is on the Resume power well.</p>
13	<p><b>Over-Clocking WDT ICC Survive Impact (OC_WDT_ICCSURV)</b>—RW/L. This bit determines whether OC_WDT expiration will have an impact on ICC (Integrated Clock Controller) bootstrap survivability.</p> <p>OC_WDT_ICCSURV=1 (default): An OC_WDT timeout while operating in this mode causes certain ICC hardware auto-recovery actions to take place. A timeout in this mode will set OC_WDT_ICCSURV_STS.</p> <p>OC_WDT_ICCSURV=0: Software should configure the OC_WDT to this mode if no ICC hardware auto-recovery actions are desired in the event of a timeout. A timeout in this mode will set OC_WDT_NO_ICCSURV_STS.</p> <p><b>Note:</b> This bit is on the Resume power well.</p>



Bit	Description
12	<p><b>OC_WDT_CTL Register Lock (OC_WDT_CTL_LCK)</b>—RW/L. This bit controls write-ability to this register.</p> <p>0 = All fields of register OC_WDT_CTL operate as normal and can be updated by software. Reads to the register operate as normal.</p> <p>1 = All RW/L fields of register OC_WDT_CTL, including this lock control bit, are locked. Writes to these register fields have no effect and the register fields retain their current states. Reads to the register operate as normal. Once this bit is set, it can only be cleared by CORE well power loss.</p> <p><b>Note:</b> This bit is on the Core power well.</p>
11:10	<b>Reserved.</b>
9:0	<p><b>Over-Clocking WDT Timeout Value (OC_WDT_TOV)</b>—RW/L. Software programs the desired over-clocking WDT timeout value into this register. This timer is zero-based and has a granularity of 1 second. Example timeout values:</p> <p>000h = 1 second 001h = 2 seconds ... 3FFh = ~17 minutes (1024 seconds)</p> <p>The value of OC_WDT_TOV may be changed by software along with its setting of the OC_WDT_RLD bit. On a WDT reload, the current (potentially new) value in OC_WDT_TOV is loaded into the WDT as the new timeout value.</p> <p>This field is also updated by the hardware when conditions allow the OC_WDT to self-start at power-cycle reboot (effectively changes the default of this field as seen by software).</p> <p><b>Note:</b> This bit is on the Resume power well.</p>

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# 5 Functional Description

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This chapter describes the functions and interfaces of the PCH.

## 5.1 PCI-to-PCI Bridge

The PCI-to-PCI bridge resides in PCI configuration space. This portion of the PCH implements the buffering and control logic between PCI and On Package DMI (OPI). The PCI decoder in this device must decode the ranges for the OPI. All register contents are lost when core well power is removed.

### 5.1.1 PCI Bus Interface

PCI Bus Interface is not available on the PCH.

### 5.1.2 PCI Legacy Mode

PCI functionality is not supported on new generation of PCH requiring methods such as using PCIe\*-to-PCI bridges to enable external PCI I/O devices. To be able to use PCIe\*-to-PCI bridges and attached legacy PCI devices, the PCH provides PCI Legacy Mode. PCI Legacy Mode allows both the PCI Express\* root port and PCIe\*-to-PCI bridge to look like subtractive PCI-to-PCI bridges. This allows the PCI Express\* root port to subtractively decode and forward legacy cycles to the bridge, and the PCIe\*-to-PCI bridge continues forwarding legacy cycles to downstream PCI devices.

**Note:** Software must ensure that only one PCH device is enabled for Subtractive decode at a time.

## 5.2 PCI Express\* Root Ports (D28:F0,F1,F2,F3,F4,F5)

There are six root ports available in the PCH. The root ports are compliant to the PCI Express\* 2.0 specification running at 5.0 GT/s. The ports all reside in Device 28 and take Function 0 – 5. Port 1 is Function 0, Port 2 is Function 1, Port 3 is Function 2, Port 4 is Function 3, Port 5 is Function 4, and Port 6 is Function 5.

**Note:** This section assumes the default PCI Express\* Function Number-to-Root Port mapping is used. Function numbers for a given root port are assignable through the Root Port Function Number and Hide for PCI Express\* Root Ports register (RCBA+238h).

**Note:** Non-Common Clock *without* Spread Spectrum Clocking (also known as, PCIe\* SRNS mode, with 600 ppm jitter tolerance) is **not** supported.

**Note:** Non-Common Clock *with* Spread Spectrum Clocking (also known as, PCIe SRIS mode, with 5600 ppm jitter tolerance) is **not** supported.

## 5.2.1 Supported PCI Express\* Port Configurations

- The maximum number of PCI Express\* root ports supported is 6.
- PCI Express\* Port 5 and 6 can each support up to 4 lanes.
- The possible PCI Express\* port configurations are:
  - PCI Express\* ports 1-4: 1x4, 2x2, 1x2+2x1, 4x1
  - PCI Express\* port 5: 1x4, 1x2, 1x1
  - PCI Express\* port 6: 1x4, 1x2, 1x1

**Note:** Integrated GbE can only be mapped to PCI Express\* ports 3, 4, or 5.

**Figure 5-1. PCI Express\* Supported Port Configurations**

1	2	3	4	5-L0	5-L1	5-L2	5-L3	6-L0	6-L1	6-L2	6-L3
x4				x4				x4			
x2		x2		x2				x2			
x2		x1	x1	x2				x2			
x2		x1	x1	x1	x1			x1			
x1	x1	x1	x1	x1				x1			

## 5.2.2 Interrupt Generation

The root port generates interrupts on behalf of hot-plug and power management events, when enabled. These interrupts can either be pin based, or can be MSIs, when enabled.

When an interrupt is generated using the legacy pin, the pin is internally routed to the PCH interrupt controllers. The pin that is driven is based upon the setting of the Chipset configuration registers. Specifically, the Chipset configuration registers used are the D28IP (Base address + 310Ch) and D28IR (Base address + 3146h) registers.

Table 5-1 summarizes interrupt behavior for MSI and wire-modes. In the table “bits” refers to the hot-plug and PME interrupt bits.

**Table 5-1. Message Signal Interrupt (MSI) Versus PCI IRQ Actions**

Interrupt Register	Wire-Mode Action	MSI Action
All bits 0	Wire inactive	No action
One or more bits set to 1	Wire active	Send message
One or more bits set to 1, new bit gets set to 1	Wire active	Send message
One or more bits set to 1, software clears some (but not all) bits	Wire active	Send message
One or more bits set to 1, software clears all bits	Wire inactive	No action
Software clears one or more bits, and one or more bits are set on the same clock	Wire active	Send message



## 5.2.3 Power Management

### 5.2.3.1 S3/S4/S5 Support

Software initiates the transition to S3/S4/S5 by performing an I/O write to the Power Management Control register in the PCH. After the I/O write completion has been returned to the processor, each root port will send a PME\_Turn\_Off TLP (Transaction Layer Packet) message on its downstream link. The device attached to the link will eventually respond with a PME\_TO\_Ack TLP message followed by sending a PM\_Enter\_L23 DLLP (Data Link Layer Packet) request to enter the L2/L3 Ready state. When all of the PCH root ports links are in the L2/L3 Ready state, the PCH power management control logic will proceed with the entry into S3/S4/S5.

Prior to entering S3, software is required to put each device into D3<sub>HOT</sub>. When a device is put into D3<sub>HOT</sub>, it will initiate entry into a L1 link state by sending a PM\_Enter\_L1 DLLP. Under normal operating conditions when the root ports send the PME\_Turn\_Off message, the link will be in state L1. However, when the root port is instructed to send the PME\_Turn\_Off message, it will send it whether or not the link was in L1. Endpoints attached to the PCH can make no assumptions about the state of the link prior to receiving a PME\_Turn\_Off message.

**Note:** The PME\_Turn\_Off TLP messaging flow is also issued during a host reset with and without power-cycle. Refer to [Table 5-34](#) for a list of host reset sources.

### 5.2.3.2 Resuming from Suspended State

The root port contains enough circuitry in the suspend well to detect a wake event through the WAKE# signal and to wake the system. When WAKE# is detected asserted, an internal signal is sent to the power management controller of the PCH to cause the system to wake up. This internal message is not logged in any register, nor is an interrupt/GPE generated due to it.

### 5.2.3.3 Device Initiated PM\_PME Message

When the system has returned to a working state from a previous low power state, a device requesting service will send a PM\_PME message continuously, until acknowledged by the root port. The root port will take different actions depending upon whether this is the first PM\_PME that has been received, or whether a previous message has been received but not yet serviced by the operating system.

If this is the first message received (RSTS.PS - D28:F0/F1/F2/F3/F4/F5:Offset 60h:bit 16 is cleared), the root port will set RSTS.PS, and log the PME Requester ID into RSTS.RID (D28:F0/F1/F2/F3/F4/F5:Offset 60h:bits 15:0). If an interrupt is enabled using RCTL.PIE (D28:F0/F1/F2/F3/F4/F5:Offset 5Ch:bit 3), an interrupt will be generated. This interrupt can be either a pin or an Message Signal Interrupt if MSI is enabled using MC.MSIE (D28:F0/F1/F2/F3/F4/F5:Offset 82h:Bit 0). See [Section 5.2.3.4](#) for SMI/SCI generation.

If this is a subsequent message received (RSTS.PS is already set), the root port will set RSTS.PP (D28:F0/F1/F2/F3/F4/F5:Offset 60h:Bit 17) and log the PME Requester ID from the message in a hidden register. No other action will be taken.

When the first PME event is cleared by software clearing RSTS.PS, the root port will set RSTS.PS, clear RSTS.PP, and move the requester ID from the hidden register into RSTS.RID.

If RCTL.PIE is set, an interrupt will be generated. If RCTL.PIE is not set, a message will be sent to the power management controller so that a GPE can be set. If messages have been logged (RSTS.PS is set), and RCTL.PIE is later written from a 0 to a 1, an interrupt will be generated. This last condition handles the case where the message was received prior to the operating system re-enabling interrupts after resuming from a low power state.

#### 5.2.3.4 SMI/SCI Generation

Interrupts for power management events are not supported on legacy operating systems. To support power management on non-PCI Express\* aware operating systems, PM events can be routed to generate SCI. To generate SCI, MPC.PMCE must be set. When set, a power management event will cause SMSCS.PMCS (D28:F0/F1/F2/F3/F4/F5:Offset DCh:Bit 31) to be set.

Additionally, BIOS workarounds for power management can be supported by setting MPC.PMME (D28:F0/F1/F2/F3/F4/F5:Offset D8h:Bit 0). When this bit is set, power management events will set SMSCS.PMMS (D28:F0/F1/F2/F3/F4/F5:Offset DCh:Bit 0), and SMI will be generated. This bit will be set regardless of whether interrupts or SCI is enabled. The SMI may occur concurrently with an interrupt or SCI.

#### 5.2.3.5 Latency Tolerance Reporting (LTR)

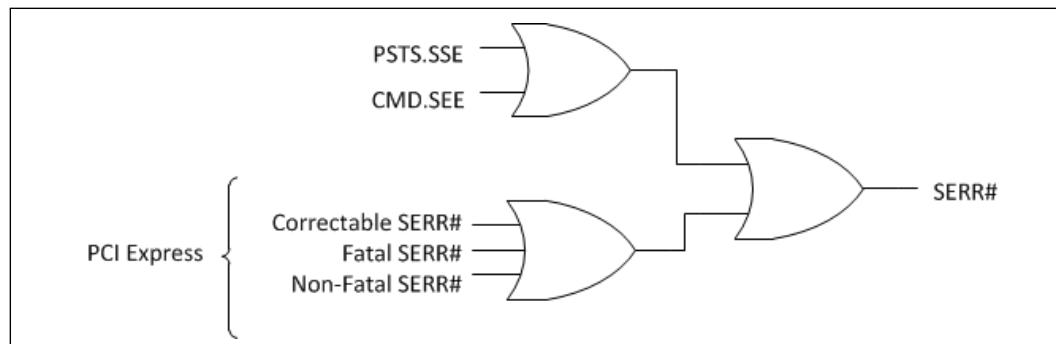
The root port supports the extended Latency Tolerance Reporting (LTR) capability. LTR provides a means for device endpoints to dynamically report their service latency requirements for memory access to the root port. Endpoint devices should transmit a new LTR message to the root port each time its latency tolerance changes (and initially during boot). The PCH uses the information to make better power management decisions. The processor uses the worst case tolerance value communicated by the PCH to optimize C-State transitions. This results in better platform power management without impacting endpoint functionality.

**Note:** Endpoint devices that support LTR must implement the reporting and enable mechanism detailed in the PCIe\* Latency Tolerance Reporting Engineering Change Notice.

#### 5.2.4 SERR# Generation

SERR# may be generated using two paths—through PCI mechanisms involving bits in the PCI header, or through PCI Express\* mechanisms involving bits in the PCI Express\* capability structure.

**Figure 5-2. Generation of SERR# to Platform**



## 5.2.5 Hot-Plug

All PCIe\* Root Ports support Express Card 1.0 based hot-plug that performs the following:

- Presence Detect and Link Active Changed Support
- Interrupt generation

### 5.2.5.1 Presence Detection

When a module is plugged in and power is supplied, the physical layer will detect the presence of the device, and the root port sets SLSTS.PDS (D28:F0/F1/F2/F3/F4/F5:Offset 5Ah:Bit 6) and SLSTS.PDC (D28:F0/F1/F2/F3:Offset 6h:Bit 3). If SLCTL.PDE (D28:F0/F1/F2/F3/F4/F5:Offset 58h:Bit 3) and SLCTL.HPE (D28:F0/F1/F2/F3/F4/F5:Offset 58h:Bit 5) are both set, the root port will also generate an interrupt.

When a module is removed (using the physical layer detection), the root port clears SLSTS.PDS and sets SLSTS.PDC. If SLCTL.PDE and SLCTL.HPE are both set, the root port will also generate an interrupt.

### 5.2.5.2 SMI/SCI Generation

Interrupts for power-management events are not supported on legacy operating systems. To support power-management on non-PCI Express\* aware operating systems, power-management events can be routed to generate SCI. To generate SCI, MPC.HPCE (D28:F0/F1/F2/F3/F4/F5:Offset D8h:Bit 30) must be set. When set, enabled hot-plug events will cause SMSCS.HPCS (D28:F0/F1/F2/F3/F4/F5:Offset DCh:Bit 30) to be set.

Additionally, BIOS workarounds for hot-plug can be supported by setting MPC.HPME (D28:F0/F1/F2/F3/F4/F5:Offset D8h:Bit 1). When this bit is set, hot-plug events can cause SMI status bits in SMSCS to be set. Supported hot-plug events and their corresponding SMSCS bit are:

- Presence Detect Changed – SMSCS.HPPDM (D28:F0/F1/F2/F3/F4/F5:Offset DCh:Bit 1)
- Link Active State Changed – SMSCS.HPLAS (D28:F0/F1/F2/F3/F4/F5:Offset DCh:Bit 4)

When any of these bits are set, SMI# will be generated. These bits are set regardless of whether interrupts or SCI is enabled for hot-plug events. The SMI# may occur concurrently with an interrupt or SCI.

## 5.2.6 Non-Common Clock Mode

Non-Common Clock mode is not supported.

## 5.3

## Gigabit Ethernet Controller (B0:D25:F0)

The PCH integrates a Gigabit Ethernet (GbE) controller. The integrated GbE controller is compatible with the Intel® Ethernet Network Connection I218LM/V Platform LAN Connect Device. The integrated GbE controller provides two interfaces for 10/100/1000MB/s and manageability operation:

- Based on PCI Express\* – A high-speed SerDes interface using PCI Express\* electrical signaling at half speed while keeping the custom logical protocol for active state operation mode.
- System Management Bus (SMBus) SMLink0 – A low speed connection for low power state mode for manageability communication only. The frequency of this connection can be configured to one of three different speeds (100 KHz, 400 KHz, or 1 MHz). At this low power state mode the Ethernet link speed is reduced to 10MB/s.

**Note:**

The SMBus Specification Version 2.0 defines a maximum bus frequency of 100 KHz. Speeds faster than this are not SMBus compliant and are used by Intel to support higher bandwidth manageability communication in the Sx states.

The Intel® Ethernet Network Connection I218LM/V Platform LAN Connect Device can be connected to any non-multiplexed (fixed) PCI Express\* port on the PCH.

**Figure 5-3. Valid PCI Express\* Ports for Platform LAN Connect Device (GbE) Use**

Fixed Signals		Muxed Signals		Fixed Signals						Muxed Signals			
USB3 1	USB3 2	PCIe* 1	PCIe* 2	PCIe 3	PCIe 4	PCIe 5 Lane 0	PCIe 5 Lane 1	PCIe 5 Lane 2	PCIe 5 Lane 3	SATA 3	SATA 2	SATA 1	SATA 0
		USB3 3	USB3 4							PCIe 6 Lane 0	PCIe 6 Lane 1	PCIe 6 Lane 2	PCIe 6 Lane 3
GbE can be used						GbE can be used							

The Intel® Ethernet Network Connection I218LM/V only runs at a speed of 1250MB/s, which is 1/2 of the 2.5GB/s PCI Express\* frequency. Each of the PCI Express\* root ports in the PCH have the ability to run at the 1250MB/s rate. There is no need to implement a mechanism to detect that the Platform LAN Device is connected. The port configuration (if any), attached to the Platform LAN device, is pre-loaded from the NVM. The selected port adjusts the transmitter to run at the 1250MB/s rate and does not need to be PCI Express\* compliant.

**Note:**

PCIe\* validation tools cannot be used for electrical validation of this interface—however, PCIe\* layout rules apply for on-board routing.

The integrated GbE controller operates at full-duplex at all supported speeds or half-duplex at 10/100MB/s. It also adheres to the *IEEE 802.3x Flow Control Specification*.

**Note:**

GbE operation (1000MB/s) is only supported in S0 mode. In Sx modes, SMBus is the only active bus and is used to support manageability/remote wake-up functionality.

The integrated GbE controller provides a system interface using a PCI Express\* function. A full memory-mapped or I/O-mapped interface is provided to the software, along with DMA mechanisms for high performance data transfer.

The integrated GbE controller features are:

- Network Features
  - Compliant with the 1GB/s Ethernet 802.3, 802.3u, 802.3z, 802.3ab specifications
  - Multi-speed operation: 10/100/1000MB/s
  - Full-duplex operation at 10/100/1000MB/s: Half-duplex at 10/100MB/s
  - Flow control support compliant with the 802.3X specification as well as the specific operation of asymmetrical flow control defined by 802.3z
  - VLAN support compliant with the 802.3q specification
  - MAC address filters: perfect match unicast filters; multicast hash filtering, broadcast filter, and promiscuous mode
  - PCI Express\*/SMBus interface to GbE PHYs
- Host Interface Features
  - 64-bit address master support for systems using more than 4GB of physical memory
  - Programmable host memory receive buffers (256 Bytes to 16KB)
  - Intelligent interrupt generation features to enhance driver performance
  - Descriptor ring management hardware for transmit and receive
  - Software controlled reset (resets everything except the configuration space)
  - Message Signaled Interrupts
- Performance Features
  - Configurable receive and transmit data FIFO, programmable in 1KB increments
  - TCP segmentation capability compatible with Windows\* NT 5.x off-loading features
  - Fragmented UDP checksum offload for packet reassembly
  - IPv4 and IPv6 checksum offload support (receive, transmit, and TCP segmentation offload)
  - Split header support to eliminate payload copy from user space to host space
  - Receive Side Scaling (RSS) with two hardware receive queues
  - Supports 9018 bytes of jumbo packets
  - Packet buffer size
  - LinkSec offload compliant with 802.3ae specification
  - TimeSync offload compliant with 802.1as specification
- Virtualization Technology Features
  - Warm function reset – function level reset (FLR)
  - VMDq1
- Power Management Features
  - Magic Packet wake-up enable with unique MAC address
  - ACPI register set and power down functionality supporting D0 and D3 states
  - Full wake up support (APM, ACPI)
  - MAC power down at Sx, DM-Off with and without WoL
  - Auto connect battery saver at S0 no link and Sx no link
  - Energy Efficient Ethernet (EEE) support
  - Latency Tolerance Reporting (LTR)
  - ARP and ND proxy support through LAN Connected Device proxy
  - Wake on LAN (WoL) from Deep Sx

## 5.3.1 GbE PCI Express\* Bus Interface

The GbE controller has a PCI Express\* interface to the host processor and host memory. The following sections detail the bus transactions.

### 5.3.1.1 Transaction Layer

The upper layer of the host architecture is the transaction layer. The transaction layer connects to the device GbE controller using an implementation specific protocol. Through this GbE controller-to-transaction-layer protocol, the application-specific parts of the device interact with the subsystem and transmit and receive requests to or from the remote agent, respectively.

### 5.3.1.2 Data Alignment

#### 5.3.1.2.1 4KB Boundary

PCI requests must never specify an address/length combination that causes a memory space access to cross a 4KB boundary. It is the responsibility of hardware to break requests into 4KB-aligned requests (if needed). This does not pose any requirement on software. However, if software allocates a buffer across a 4KB boundary, hardware issues multiple requests for the buffer. Software should consider aligning buffers to a 4KB boundary in cases where it improves performance.

The alignment to the 4KB boundaries is done by the GbE controller. The transaction layer does not do any alignment according to these boundaries.

#### 5.3.1.2.2 64 Bytes

PCI requests are 128 bytes or less and are aligned to make better use of memory controller resources. Writes, however, can be on any boundary and can cross a 64-byte alignment boundary.

### 5.3.1.3 Configuration Request Retry Status

The integrated GbE controller might have a delay in initialization due to an NVM read. If the NVM configuration read operation is not completed and the device receives a configuration request, the device responds with a configuration request retry completion status to terminate the request, and thus effectively stalls the configuration request until such time that the sub-system has completed local initialization and is ready to communicate with the host.

## 5.3.2 Error Events and Error Reporting

### 5.3.2.1 Data Parity Error

The PCI host bus does not provide parity protection, but it does forward parity errors from bridges. The integrated GbE controller recognizes parity errors through the internal bus interface and sets the *Parity Error* bit in PCI configuration space. If parity errors are enabled in configuration space, a system error is indicated on the PCI host bus. The offending cycle with a parity error is dropped and not processed by the integrated GbE controller.



### 5.3.2.2 Completion with Unsuccessful Completion Status

A completion with unsuccessful completion status (any status other than 000) is dropped and not processed by the integrated GbE controller. Furthermore, the request that corresponds to the unsuccessful completion is not retried. When this unsuccessful completion status is received, the *System Error* bit in the PCI configuration space is set. If the system errors are enabled in configuration space, a system error is indicated on the PCI host bus.

### 5.3.3 Ethernet Interface

The integrated GbE controller provides a complete CSMA/CD function supporting IEEE 802.3 (10MB/s), 802.3u (100MB/s) implementations. It also supports the IEEE 802.3z and 802.3ab (1000MB/s) implementations. The device performs all of the functions required for transmission, reception, and collision handling called out in the standards.

The mode used to communicate between the PCH and the Intel® Ethernet Network Connection I218LM/V Platform LAN Connect Device supports 10/100/1000MB/s operation, with both half- and full-duplex operation at 10/100MB/s, and full-duplex operation at 1000MB/s.

#### 5.3.3.1 Intel® Ethernet Network Connection I218LM/V Platform LAN Connect Device Interface

The integrated GbE controller and the Intel® Ethernet Network Connection I218LM/V Platform LAN Connect Device communicate through the PCIe\* and SMLink0 interfaces. All integrated GbE controller configuration is performed using device control registers mapped into system memory or I/O space. The Platform LAN Connect Device is configured using the PCI Express\* or SMLink0 interface.

The integrated GbE controller supports various modes as listed in [Table 5-2](#).

**Table 5-2. LAN Mode Support**

Mode	System State	Interface Active	Connections
Normal 10/100/1000MB/s	S0	PCI Express* or SMLink0 <sup>1</sup>	Intel® Ethernet Network Connection I218LM/V
Manageability and Remote Wake-up	Sx	SMLink0	Intel® Ethernet Network Connection I218LM/V

**Note:**

1. GbE operation is not supported in Sx state.

### 5.3.4 PCI Power Management

The integrated GbE controller supports the Advanced Configuration and Power Interface (ACPI) specification as well as Advanced Power Management (APM). This enables the network-related activity (using an internal host wake signal) to wake up the host. For example, from Sx (S3 – S5) and Deep Sx to S0.

**Note:**

The Intel® Ethernet Network Connection I218LM/V Platform LAN Connect Device must be powered during the Deep Sx state in order to support host wake up from Deep Sx. GPIO27 on the PCH must be configured to support wake from Deep Sx and must be connected to LANWAKE\_N on the Platform LAN Connect Device. The SLP\_LAN# signal must be driven high (de-asserted) in the Deep Sx state to maintain power to the Platform LAN Connect Device.

The integrated GbE controller contains power management registers for PCI and supports D0 and D3 states. PCIe\* transactions are only allowed in the D0 state, except for host accesses to the integrated GbE controller's PCI configuration registers.

#### 5.3.4.1 Wake Up

The integrated GbE controller supports two types of wake-up mechanisms:

1. Advanced Power Management (APM) Wake Up
2. ACPI Power Management Wake Up

Both mechanisms use an internal logic signal to wake the system up. The wake-up steps are as follows:

1. Host wake event occurs

**Note:**

Packet is not delivered to host

2. The Platform LAN Connect Device receives a WoL packet/link status change.
3. The Platform LAN Connect Device sends a wake indication to the PCH. This requires the LANWAKE\_N pin from the Intel Ethernet Network Connection I218LM/V Platform LAN Connect Device to be connected to the PCH GPIO27 pin. GPIO27 must also be configured to support wake from Deep Sx.
4. If the system is in Deep Sx, the wake will cause the system to wake from the Deep Sx state to the Sx state.
5. The Platform LAN Connect Device wakes up the integrated GbE controller using an SMBus message on SMLink0.
6. The integrated GbE controller sets the *PME\_STATUS* bit.
7. System wakes from Sx state to S0 state.
8. The host LAN function is transitioned to D0.
9. The host clears the *PME\_STATUS* bit.

##### 5.3.4.1.1 Advanced Power Management Wake Up

Advanced Power Management Wake Up or APM Wake Up was previously known as Wake on LAN (WoL). It is a feature that has existed in the 10/100MB/s NICs for several generations. The basic premise is to receive a broadcast or unicast packet with an explicit data pattern and then to assert a signal to wake up the system. In earlier generations, this was accomplished by using a special signal that ran across a cable to a defined connector on the motherboard. The NIC would assert the signal for approximately 50 ms to signal a wake up. The integrated GbE controller uses (if configured) an in-band PM\_PME message for this.

At power up, the integrated GbE controller reads the *APM Enable* bits from the NVM PCI INIT Control Word into the *APM Enable* (APME) bits of the Wake Up Control (WUC) register. These bits control enabling of APM wake up.

When APM wake up is enabled, the integrated GbE controller checks all incoming packets for Magic Packets.

Once the integrated GbE controller receives a matching Magic Packet, it:

- Sets the *Magic Packet Received* bit in the Wake Up Status (WUS) register.
- Sets the *PME\_Status* bit in the Power Management Control/Status Register (PMCSR).



APM wake up is supported in all power states and only disabled if a subsequent NVM read results in the *APM Wake Up* bit being cleared or the software explicitly writes a 0b to the *APM Wake Up* (APM) bit of the WUC register.

**Note:** APM wake up settings will be restored to NVM default by the PCH when the LAN connected Device (PHY) power is turned off and subsequently restored. Some example host WoL flows are:

- When system transitions to G3 after WoL is disabled from the BIOS, APM host WoL would get enabled.
- Anytime power to the LAN Connected Device (PHY) is cycled while in S4/S5 after WoL is disabled from the BIOS, APM host WoL would get enabled. Anytime power to the LAN Connected Device (PHY) is cycled while in S3, APM host WoL configuration is lost.

#### 5.3.4.1.2 ACPI Power Management Wake Up

The integrated GbE controller supports ACPI Power Management based wake ups. It can generate system wake-up events from three sources:

- Receiving a Magic Packet.
- Receiving a Network Wake Up Packet.
- Detecting a link change of state.

Activating ACPI Power Management Wake Up requires the following steps:

- The software device driver programs the Wake Up Filter Control (WUFC) register to indicate the packets it needs to wake up from and supplies the necessary data to the IPv4 Address Table (IP4AT) and the Flexible Filter Mask Table (FFMT), Flexible Filter Length Table (FFLT), and the Flexible Filter Value Table (FFVT). It can also set the *Link Status Change Wake Up Enable* (LNKC) bit in the Wake Up Filter Control (WUFC) register to cause wake up when the link changes state.
- The operating system (at configuration time) writes a 1b to the *PME\_EN* bit of the Power Management Control/Status Register (PMCSR.8).

Normally, after enabling wake up, the operating system writes a 11b to the lower two bits of the PMCSR to put the integrated GbE controller into low-power mode.

Once wake up is enabled, the integrated GbE controller monitors incoming packets, first filtering them according to its standard address filtering method, then filtering them with all of the enabled wake-up filters. If a packet passes both the standard address filtering and at least one of the enabled wake-up filters, the integrated GbE controller:

- Sets the *PME\_Status* bit in the PMCSR
- Sets one or more of the *received* bits in the Wake Up Status (WUS) register. (More than one bit is set if a packet matches more than one filter.)

If enabled, a link state change wake up causes similar results, setting the *Link Status Changed* (LNKC) bit in the Wake Up Status (WUS) register when the link goes up or down.

After receiving a wake-up packet, the integrated GbE controller ignores any subsequent wake-up packets until the software device driver clears all of the *Received* bits in the Wake Up Status (WUS) register. It also ignores link change events until the software device driver clears the *Link Status Changed* (LNKC) bit in the Wake Up Status (WUS) register.

**Note:** ACPI wake-up settings are not preserved when the LAN Connected Device (PHY) power is turned off and subsequently restored. Some example host WoL flows are:

- Anytime power to the LAN Connected Device (PHY) is cycled while in S3 or S4, ACPI host WoL configuration is lost.

### 5.3.5 Configurable LEDs

The integrated GbE controller supports three controllable and configurable LEDs that are driven from the Intel Ethernet Network Connection I218LM/V Platform LAN Connect Device. Each of the three LED outputs can be individually configured to select the particular event, state, or activity that is indicated on that output. In addition, each LED can be individually configured for output polarity as well as for blinking versus non-blinking (steady-state) indication.

The configuration for LED outputs is specified using the LEDCTL register. Furthermore, the hardware-default configuration for all the LED outputs, can be specified using NVM fields; thereby, supporting LED displays configurable to a particular OEM preference.

Each of the three LEDs might be configured to use one of a variety of sources for output indication. The MODE bits control the LED source:

- LINK\_100/1000 is asserted when link is established at either 100 or 1000MB/s.
- LINK\_10/1000 is asserted when link is established at either 10 or 1000MB/s.
- LINK\_UP is asserted when any speed link is established and maintained.
- ACTIVITY is asserted when link is established and packets are being transmitted or received.
- LINK/ACTIVITY is asserted when link is established AND there is NO transmit or receive activity.
- LINK\_10 is asserted when a 10MB/s link is established and maintained.
- LINK\_100 is asserted when a 100MB/s link is established and maintained.
- LINK\_1000 is asserted when a 1000MB/s link is established and maintained.
- FULL\_DUPLEX is asserted when the link is configured for full duplex operation.
- COLLISION is asserted when a collision is observed.
- PAUSED is asserted when the device's transmitter is flow controlled.
- LED\_ON is always asserted; LED\_OFF is always de-asserted.

The IVRT bits enable the LED source to be inverted before being output or observed by the blink-control logic. LED outputs are assumed to normally be connected to the negative side (cathode) of an external LED.



The *BLINK* bits control whether the LED should be blinked while the LED source is asserted, and the blinking frequency (either 200 ms on and 200 ms off or 83 ms on and 83 ms off). The blink control can be especially useful for ensuring that certain events, such as ACTIVITY indication, cause LED transitions that are sufficiently visible to a human eye. The same blinking rate is shared by all LEDs.

## 5.3.6 Function Level Reset Support (FLR)

The integrated GbE controller supports FLR capability. FLR capability can be used in conjunction with Intel Virtualization Technology (Intel VT). FLR allows an operating system in a Virtual Machine to have complete control over a device, including its initialization, without interfering with the rest of the platform. The device provides a software interface that enables the operating system to reset the entire device as if a PCI reset was asserted.

### 5.3.6.1 FLR Steps

#### 5.3.6.1.1 FLR Initialization

1. FLR is initiated by software by writing a 1b to the *Initiate FLR* bit.
2. All subsequent requests targeting the function are not claimed and will be master aborted immediately on the bus. This includes any configuration, I/O or memory cycles. However, the function will continue to accept completions targeting the function.

#### 5.3.6.1.2 FLR Operation

Function resets all configuration, I/O, and memory registers of the function except those indicated otherwise and resets all internal states of the function to the default or initial condition.

#### 5.3.6.1.3 FLR Completion

The *Initiate FLR* bit is reset (cleared) when the FLR reset completes. This bit can be used to indicate to the software that the FLR reset completed.

**Note:** From the time the *Initiate FLR* bit is written to 1b, software must wait at least 100 ms before accessing the function.

## 5.4 Low Pin Count (LPC) Bridge (with System and Management Functions) (D31:F0)

The LPC bridge function of the PCH resides in PCI D31:F0. In addition to the LPC bridge function, D31:F0 contains other functional units including Interrupt controllers, Timers, Power Management, System Management, GPIO, and RTC. In this chapter, registers and functions associated with other functional units (power management, GPIO, USB, and so forth.) are described in their respective sections.

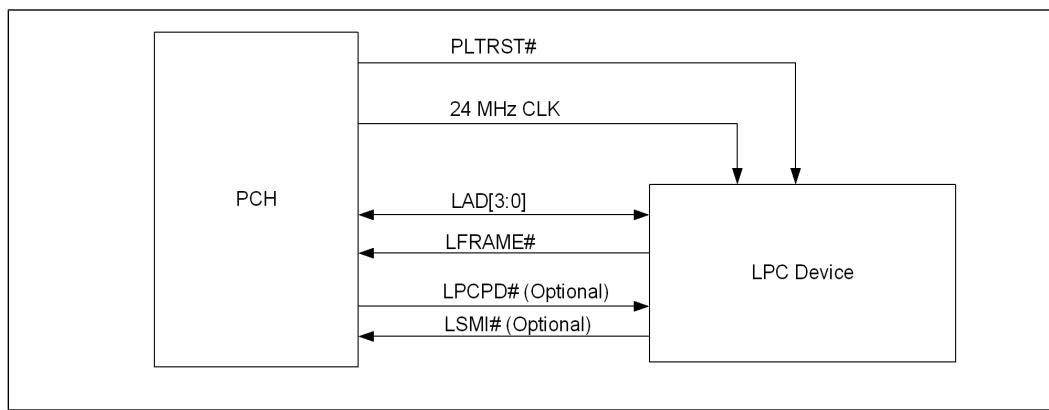
**Note:** The LPC bridge cannot be configured as a subtractive decode agent.

### 5.4.1 Low Pin Count (LPC) Interface

The PCH implements an LPC interface as described in the *Low Pin Count Interface Specification*, Revision 1.1. The LPC interface to the PCH is shown in [Figure 5-4](#).

**Note:** The PCH implements all of the signals that are shown as optional, but peripherals are not required to do so.

**Figure 5-4.** **Low Pin Count (LPC) Interface Diagram**



#### 5.4.1.1 **LPC Cycle Types**

The PCH implements all of the cycle types described in the *Low Pin Count Interface Specification*, Revision 1.1. [Table 5-3](#) shows the cycle types supported by the PCH.

**Table 5-3.** **Low Pin Count (LPC) Cycle Types Supported (Sheet 1 of 2)**

Cycle Type	Comment
Memory Read	1 byte only—(See Note 1 below)
Memory Write	1 byte only—(See Note 1 below)
I/O Read	1 byte only—The PCH breaks up 16-bit and 32-bit processor cycles into multiple 8-bit transfers.
I/O Write	1 byte only—The PCH breaks up 16-bit and 32-bit processor cycles into multiple 8-bit transfers.

**Table 5-3. Low Pin Count (LPC) Cycle Types Supported (Sheet 2 of 2)**

Cycle Type	Comment
Bus Master Read	Can be 1, 2 or 4 bytes—(See Note 2 below)
Bus Master Write	Can be 1, 2 or 4 bytes—(See Note 2 below)
<b>Notes:</b>	
1.	The PCH provides a single generic memory range (LGMR) for decoding memory cycles and forwarding them as LPC Memory cycles on the LPC bus. The LGMR memory decode range is 64KB in size and can be defined as being anywhere in the 4GB memory space. This range needs to be configured by BIOS during POST to provide the necessary memory resources. BIOS should advertise the LPC Generic Memory Range as Reserved to the operating system in order to avoid resource conflict. For larger transfers, the PCH performs multiple 8-bit transfers. If the cycle is not claimed by any peripheral, it is subsequently aborted, and the PCH returns a value of all 1s to the processor. This is done to maintain compatibility with ISA memory cycles where pull-up resistors would keep the bus high if no device responds.
2.	Bus Master Read or Write cycles must be naturally aligned. For example, a 1-byte transfer can be to any address. However, the 2-byte transfer must be word-aligned (that is, with an address where A0=0). A DWord transfer must be DWord-aligned (that is, with an address where A1 and A0 are both 0).

#### 5.4.1.2 Start Field Definition

**Table 5-4. Start Field Bit Definitions**

Bits[3:0] Encoding	Definition
0000	Start of cycle for a generic target.
1111	Stop/Abort: End of a cycle for a target.
<b>Note:</b> All other encodings are RESERVED.	

#### 5.4.1.3 Cycle Type/Direction (CYCTYPE + DIR)

The PCH always drives Bit 0 of this field to 0. [Table 5-5](#) shows the valid bit encodings.

**Table 5-5. Cycle Type Bit Definitions**

Bits[3:2]	Bit[1]	Definition
00	0	I/O Read
00	1	I/O Write
01	0	Memory Read
01	1	Memory Read
11	x	Reserved. If a peripheral performing a bus master cycle generates this value, the PCH aborts the cycle.
<b>Note:</b> All other encodings are RESERVED.		

#### 5.4.1.4 Size

Bits 3:2 are reserved. The PCH always drives them to 00. Bits 1:0 are encoded as listed in [Table 5-6](#).

**Table 5-6. Transfer Size Bit Definition**

Bits[1:0]	Size
00	8-bit transfer (1 byte)
01	16-bit transfer (2 bytes)
10	Reserved—The PCH never drives this combination.
11	32-bit transfer (4 bytes)
<b>Note:</b> All other combinations are RESERVED.	

### 5.4.1.5 SYNC

Valid values for the SYNC field are shown in Table 5-7.

**Table 5-7. SYNC Bit Definition**

Bits[3:0]	Indication
0000	<b>Ready:</b> SYNC achieved with no error.
0101	<b>Short Wait:</b> Part indicating wait-states. For bus master cycles, the PCH does not use this encoding. Instead, the PCH uses the Long Wait encoding (see next encoding below).
0110	<b>Long Wait:</b> Part indicating wait-states, and many wait-states will be added. This encoding driven by the PCH for bus master cycles, rather than the Short Wait (0101).
1010	<b>Error:</b> Sync achieved with error. This is generally used to replace the SERR# or IOCHK# signal on the PCI/ISA bus. It indicates that the data is to be transferred, but there is a serious error in this transfer.
<b>Notes:</b>	
1. All other combinations are RESERVED.	
2. If the LPC controller receives any SYNC returned from the device other than short (0101), long wait (0110), or ready (0000) when running a FWH cycle, indeterminate results may occur. A FWH device is not allowed to assert an Error SYNC.	

### 5.4.1.6 SYNC Timeout

There are several error cases that can occur on the LPC interface. The PCH responds as defined in Section 4.2.1.9 of the *Low Pin Count Interface Specification*, Revision 1.1 to the stimuli described therein. There may be other peripheral failure conditions; however, these are not handled by the PCH.

### 5.4.1.7 SYNC Error Indication

The PCH responds as defined in Section 4.2.1.10 of the *Low Pin Count Interface Specification*, Revision 1.1.

Upon recognizing the SYNC field indicating an error, the PCH treats this as a SERR by reporting this into the Device 31 Error Reporting Logic.

### 5.4.1.8 LFRAME# Usage

The PCH follows the usage of LFRAME# as defined in the *Low Pin Count Interface Specification*, Revision 1.1.

The PCH performs an abort for the following cases (possible failure cases):

- The PCH starts a Memory or I/O cycle, but no device drives a valid SYNC after four consecutive clocks.
- The PCH starts a Memory or I/O and the peripheral drives an invalid SYNC pattern.
- A peripheral drives an invalid value.

### 5.4.1.9 I/O Cycles

For I/O cycles targeting registers specified in the PCH decode ranges, the PCH performs I/O cycles as defined in the *Low Pin Count Interface Specification*, Revision 1.1. These are 8-bit transfers. If the processor attempts a 16-bit or 32-bit transfer, the PCH breaks the cycle up into multiple 8-bit transfers to consecutive I/O addresses.

**Note:**

If the cycle is not claimed by any peripheral (and subsequently aborted), the PCH returns a value of all 1s (FFh) to the processor. This is to maintain compatibility with ISA I/O cycles where pull-up resistors would keep the bus high if no device responds.

### 5.4.1.10 LPC Power Management

#### LPCPD# Protocol

Same timings as SUS\_STAT#. Upon driving SUS\_STAT# low, the PCH drives LFRAME# low, and tri-states (or drives low) LAD[3:0].

**Note:**

The *Low Pin Count Interface Specification*, Revision 1.1 defines the LPCPD# protocol where there is at least 30  $\mu$ s from LPCPD# assertion to LRST# assertion. This specification explicitly states that this protocol only applies to entry/exit of low power states that do not include asynchronous reset events. The PCH asserts both SUS\_STAT# (connects to LPCPD#) and PLTRST# (connects to LRST#) at the same time during a global reset. This is not inconsistent with the LPC LPCPD# protocol.

### 5.4.1.11 Configuration and PCH Implications

#### LPC I/F Decoders

To allow the I/O cycles and memory-mapped cycles to go to the LPC interface, the PCH includes several decoders. During configuration, the PCH must be programmed with the same decode ranges as the peripheral. The decoders are programmed using the D 31:F0 configuration space.

**Note:**

The PCH cannot accept PCI write cycles from PCI-to-PCI bridges or devices with similar characteristics (specifically those with a "Retry Read" feature which is enabled) to an LPC device if there is an outstanding LPC read cycle towards the same PCI device or bridge. These cycles are not part of normal system operation, but may be encountered as part of platform validation testing using custom test fixtures.

## 5.5 8254 Timers (D31:F0)

The PCH contains three counters that have fixed uses. All registers and functions associated with the 8254 timers are in the core well. The 8254 unit is clocked by a 14.318 MHz clock derived from 24 MHz xtal clock.

#### Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value 1 counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

#### Counter 1, Refresh Request Signal

This counter provides the refresh request signal and is typically programmed for Mode 2 operation and only impacts the period of the REF\_TOGGLE bit in Port 61. The initial count value is loaded one counter period after being written to the counter I/O address. The REF\_TOGGLE bit will have a square wave behavior (alternate between 0 and 1) and will toggle at a rate based on the value in the counter. Programming the counter to anything other than Mode 2 will result in undefined behavior for the REF\_TOGGLE bit.

### Counter 2, Speaker Tone

This counter provides the speaker tone and is typically programmed for Mode 3 operation. The counter provides a speaker frequency equal to the counter clock frequency (1.193 MHz) divided by the initial count value. The speaker must be enabled by a write to port 061h (see NMI Status and Control ports).

## 5.5.1 Timer Programming

The counter/timers are programmed in the following fashion:

1. Write a control word to select a counter.
2. Write an initial count for that counter.
3. Load the least and/or most significant bytes (as required by Control Word Bits 5, 4) of the 16-bit counter.
4. Repeat with other counters.

Only two conventions need to be observed when programming the counters. First, for each counter, the control word must be written before the initial count is written. Second, the initial count must follow the count format specified in the control word (least significant byte only, most significant byte only, or least significant byte, and then most significant byte).

A new initial count may be written to a counter at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

If a counter is programmed to read/write two-byte counts, the following precaution applies – a program must not transfer control between writing the first and second byte to another routine which also writes into that same counter. Otherwise, the counter will be loaded with an incorrect count.

The Control Word Register at port 43h controls the operation of all three counters. Several commands are available:

- **Control Word Command.** Specifies which counter to read or write, the operating mode, and the count format (binary or BCD).
- **Counter Latch Command.** Latches the current count so that it can be read by the system. The countdown process continues.
- **Read Back Command.** Reads the count value, programmed mode, the current state of the OUT pins, and the state of the Null Count Flag of the selected counter.

Table 5-8 lists the six operating modes for the interval counters.

**Table 5-8. Counter Operating Modes (Sheet 1 of 2)**

Mode	Function	Description
0	Out signal on end of count (=0)	Output is 0. When count goes to 0, output goes to 1 and stays at 1 until counter is reprogrammed.
1	Hardware retriggerable one-shot	Output is 0. When count goes to 0, output goes to 1 for one clock time.
2	Rate generator (divide by n counter)	Output is 1. Output goes to 0 for one clock time, then back to 1 and counter is reloaded.
3	Square wave output	Output is 1. Output goes to 0 when counter rolls over, and counter is reloaded. Output goes to 1 when counter rolls over, and counter is reloaded, and so on

**Table 5-8. Counter Operating Modes (Sheet 2 of 2)**

Mode	Function	Description
4	Software triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.
5	Hardware triggered strobe	Output is 1. Output goes to 0 when count expires for one clock time.

## 5.5.2 Reading from the Interval Timer

It is often desirable to read the value of a counter without disturbing the count in progress. There are three methods for reading the counters—a simple read operation, counter Latch command, and the Read-Back command. Each is explained below.

With the simple read and counter latch command methods, the count must be read according to the programmed format; specifically, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other. Read, write, or programming operations for other counters may be inserted between them.

### 5.5.2.1 Simple Read

The first method is to perform a simple read operation. The counter is selected through Port 40h (Counter 0), 41h (Counter 1), or 42h (Counter 2).

**Note:**

Performing a direct read from the counter does not return a determinate value, because the counting process is asynchronous to read operations. However, in the case of Counter 2, the count can be stopped by writing to the GATE bit in Port 61h.

### 5.5.2.2 Counter Latch Command

The Counter Latch command, written to Port 43h, latches the count of a specific counter at the time the command is received. This command is used to ensure that the count read from the counter is accurate, particularly when reading a two-byte count. The count value is then read from each counter's Count register as was programmed by the Control register.

The count is held in the latch until it is read or the counter is reprogrammed. The count is then unlatched. This allows reading the contents of the counters on the fly without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one counter. Counter Latch commands do not affect the programmed mode of the counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch command is ignored. The count read is the count at the time the first Counter Latch command was issued.

### 5.5.2.3 Read Back Command

The Read Back command, written to Port 43h, latches the count value, programmed mode, and current states of the OUT pin and Null Count flag of the selected counter or counters. The value of the counter and its status may then be read by I/O access to the counter address.

The Read Back command may be used to latch multiple counter outputs at one time. This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read or

reprogrammed. Once read, a counter is unlatched. The other counters remain latched until they are read. If multiple count Read Back commands are issued to the same counter without reading the count, all but the first are ignored.

The Read Back command may additionally be used to latch status information of selected counters. The status of a counter is accessed by a read from that counter's I/O port address. If multiple counter status latch operations are performed without reading the status, all but the first are ignored.

Both count and status of the selected counters may be latched simultaneously. This is functionally the same as issuing two consecutive, separate Read Back commands. If multiple count and/or status Read Back commands are issued to the same counters without any intervening reads, all but the first are ignored.

If both count and status of a counter are latched, the first read operation from that counter returns the latched status, regardless of which was latched first. The next one or two reads, depending on whether the counter is programmed for one or two type counts, returns the latched count. Subsequent reads return unlatched count.

## 5.6 8259 Programmable Interrupt Controllers (PIC) (D31:F0)

The PCH incorporates the functionality of two 8259 interrupt controllers that provide system interrupts for the ISA compatible interrupts. These interrupts can include; system timer, keyboard controller, serial ports, parallel ports, floppy disk, mouse, and DMA channels. In addition, this interrupt controller can support the PCI-based interrupts, by mapping the PCI interrupt onto the compatible ISA interrupt line. Each 8259 controller supports eight interrupts, numbered 0–7. [Table 5-9](#) shows how the controllers are connected.

**Table 5-9. Interrupt Controller Connections**

8259	8259 Input	Typical Interrupt Source	Connected Pin/Function
Master	0	Internal	Internal Timer/Counter 0 output/HPET #0
	1	Keyboard	IRQ1 using SERIRQ
	2	Internal	Slave controller INTR output
	3	Serial Port A	IRQ3 using PIRQ#, Intel® SST
	4	Serial Port B	IRQ4 using PIRQ#, Intel® SST
	5	Parallel Port/Generic	IRQ5 using SERIRQ, PIRQ#, GSPI, UART, I <sup>2</sup> C, SDIO
	6	Floppy Disk	IRQ6 using SERIRQ, PIRQ#, GSPI, UART, I <sup>2</sup> C, SDIO
	7	Parallel Port/Generic	IRQ7 using SERIRQ, PIRQ#, GSPI, UART, I <sup>2</sup> C, SDIO
Slave	0	Internal Real Time Clock	Internal RTC/HPET #1
	1	Generic	IRQ9 using SERIRQ, SCI, TCO, or PIRQ#
	2	Generic	IRQ10 using SERIRQ, SCI, TCO, or PIRQ#
	3	Generic	IRQ11 using SERIRQ, SCI, TCO, or PIRQ#, or HPET #2
	4	PS/2 Mouse	IRQ12 using PIRQ# or HPET #3
	5	Internal	GSPI, UART, I <sup>2</sup> C, SDIO
	6	Generic	GPIO, PIRQ#
	7	Generic	GPIO, PIRQ#



The PCH cascades the slave controller onto the master controller through master controller interrupt input 2. This means there are only 15 possible interrupts for the PCH PIC.

Interrupts can individually be programmed to be edge or level, except for IRQ0, IRQ2, IRQ8#, and IRQ13.

**Note:** Active-low interrupt sources (such as, the PIRQ#s) are inverted inside the PCH. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term "high" indicates "active," which means "low" on an originating PIRQ#.

## 5.6.1 Interrupt Handling

### 5.6.1.1 Generating Interrupts

The PIC interrupt sequence involves three bits, from the IRR, ISR, and IMR, for each interrupt level. These bits are used to determine the interrupt vector returned, and status of any other pending interrupts. [Table 5-10](#) defines the IRR, ISR, and IMR.

**Table 5-10. Interrupt Status Registers**

Bit	Description
IRR	<b>Interrupt Request Register.</b> This bit is set on a low-to-high transition of the interrupt line in edge mode, and by an active high level in level mode. This bit is set whether or not the interrupt is masked. However, a masked interrupt will not generate INTR.
ISR	<b>Interrupt Service Register.</b> This bit is set, and the corresponding IRR bit cleared, when an interrupt acknowledge cycle is seen, and the vector returned is for that interrupt.
IMR	<b>Interrupt Mask Register.</b> This bit determines whether an interrupt is masked. Masked interrupts will not generate INTR.

### 5.6.1.2 Acknowledging Interrupts

The processor generates an interrupt acknowledge cycle that is translated by the host bridge into a PCI Interrupt Acknowledge Cycle to the PCH. The PIC translates this command into two internal INTA# pulses expected by the 8259 cores. The PIC uses the first internal INTA# pulse to freeze the state of the interrupts for priority resolution. On the second INTA# pulse, the master or slave sends the interrupt vector to the processor with the acknowledged interrupt code. This code is based upon Bits [7:3] of the corresponding ICW2 register, combined with three bits representing the interrupt within that controller.

**Table 5-11. Content of Interrupt Vector Byte**

Master, Slave Interrupt	Bits[7:3]	Bits[2:0]
IRQ7,15	ICW2[7:3]	111
IRQ6,14		110
IRQ5,13		101
IRQ4,12		100
IRQ3,11		011
IRQ2,10		010
IRQ1,9		001
IRQ0,8		000

### 5.6.1.3

#### Hardware/Software Interrupt Sequence

1. One or more of the Interrupt Request lines (IRQ) are raised high in edge mode, or seen high in level mode, setting the corresponding IRR bit.
2. The PIC sends INTR active to the processor if an asserted interrupt is not masked.
3. The processor acknowledges the INTR and responds with an interrupt acknowledge cycle. The cycle is translated into a PCI interrupt acknowledge cycle by the host bridge. This command is broadcast over PCI by the PCH.
4. Upon observing its own interrupt acknowledge cycle on PCI, the PCH converts it into the two cycles that the internal 8259 pair can respond to. Each cycle appears as an interrupt acknowledge pulse on the internal INTA# pin of the cascaded interrupt controllers.
5. Upon receiving the first internally generated INTA# pulse, the highest priority ISR bit is set and the corresponding IRR bit is reset. On the trailing edge of the first pulse, a slave identification code is broadcast by the master to the slave on a private, internal three bit wide bus. The slave controller uses these bits to determine if it must respond with an interrupt vector during the second INTA# pulse.
6. Upon receiving the second internally generated INTA# pulse, the PIC returns the interrupt vector. If no interrupt request is present because the request was too short in duration, the PIC returns vector 7 from the master controller.
7. This completes the interrupt cycle. In AEOI mode the ISR bit is reset at the end of the second INTA# pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

## 5.6.2 Initialization Command Words (ICWx)

Before operation can begin, each 8259 must be initialized. In the PCH, this is a four-byte sequence. The four initialization command words are referred to by their acronyms: ICW1, ICW2, ICW3, and ICW4.

The base address for each 8259 initialization command word is a fixed location in the I/O memory space: 20h for the master controller, and A0h for the slave controller.

### 5.6.2.1 ICW1

An I/O write to the master or slave controller base address with data bit 4 equal to 1 is interpreted as a write to ICW1. Upon sensing this write, the PCH PIC expects three more byte writes to 21h for the master controller, or A1h for the slave controller, to complete the ICW sequence.

A write to ICW1 starts the initialization sequence during which the following automatically occur:

1. Following initialization, an interrupt request (IRQ) input must make a low-to-high transition to generate an interrupt.
2. The Interrupt Mask Register is cleared.
3. IRQ7 input is assigned priority 7.
4. The slave mode address is set to 7.
5. Special mask mode is cleared and Status Read is set to IRR.

### 5.6.2.2 ICW2

The second write in the sequence (ICW2) is programmed to provide Bits [7:3] of the interrupt vector that will be released during an interrupt acknowledge. A different base is selected for each interrupt controller.

### 5.6.2.3 ICW3

The third write in the sequence (ICW3) has a different meaning for each controller.

- For the master controller, ICW3 is used to indicate which IRQ input line is used to cascade the slave controller. Within the PCH, IRQ2 is used. Therefore, Bit 2 of ICW3 on the master controller is set to a 1, and the other bits are set to 0s.
- For the slave controller, ICW3 is the slave identification code used during an interrupt acknowledge cycle. On interrupt acknowledge cycles, the master controller broadcasts a code to the slave controller if the cascaded interrupt won arbitration on the master controller. The slave controller compares this identification code to the value stored in its ICW3, and if it matches, the slave controller assumes responsibility for broadcasting the interrupt vector.

### 5.6.2.4 ICW4

The final write in the sequence (ICW4) must be programmed for both controllers. At the very least, Bit 0 must be set to a 1 to indicate that the controllers are operating in an Intel Architecture-based system.

### 5.6.3 Operation Command Words (OCW)

These command words reprogram the Interrupt controller to operate in various interrupt modes.

- OCW1 masks and unmasks interrupt lines.
- OCW2 controls the rotation of interrupt priorities when in rotating priority mode, and controls the EOI function.
- OCW3 sets up ISR/IRR reads, enables/disables the special mask mode (SMM), and enables/disables polled interrupt mode.

### 5.6.4 Modes of Operation

#### 5.6.4.1 Fully-Nested Mode

In this mode, interrupt requests are ordered in priority from 0 through 7, with 0 being the highest. When an interrupt is acknowledged, the highest priority request is determined and its vector placed on the bus. Additionally, the ISR for the interrupt is set. This ISR bit remains set until: the processor issues an EOI command immediately before returning from the service routine; or if in AEOI mode, on the trailing edge of the second INTA#. While the ISR bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels generate another interrupt. Interrupt priorities can be changed in the rotating priority mode.

#### 5.6.4.2 Special Fully-Nested Mode

This mode is used in the case of a system where cascading is used, and the priority has to be conserved within each slave. In this case, the special fully-nested mode is programmed to the master controller. This mode is similar to the fully-nested mode with the following exceptions:

- When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority interrupts within the slave are recognized by the master and initiate interrupts to the processor. In the normal-nested mode, a slave is masked out when its request is in service.
- When exiting the Interrupt Service routine, software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a Non-Specific EOI command to the slave and then reading its ISR. If it is 0, a non-specific EOI can also be sent to the master.

#### 5.6.4.3 Automatic Rotation Mode (Equal Priority Devices)

In some applications, there are a number of interrupting devices of equal priority. Automatic rotation mode provides for a sequential 8-way rotation. In this mode, a device receives the lowest priority after being serviced. In the worst case, a device requesting an interrupt has to wait until each of seven other devices are serviced at most once.

There are two ways to accomplish automatic rotation using OCW2 – the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the rotate in automatic EOI mode that is set by (R=1, SL=0, EOI=0).



#### 5.6.4.4 Specific Rotation Mode (Specific Priority)

Software can change interrupt priorities by programming the bottom priority. For example, if IRQ5 is programmed as the bottom priority device, then IRQ6 is the highest priority device. The Set Priority Command is issued in OCW2 to accomplish this, where: R=1, SL=1, and LO-L2 is the binary priority level code of the bottom priority device.

In this mode, internal status is updated by software control during OCW2. However, it is independent of the EOI command. Priority changes can be executed during an EOI command by using the Rotate on Specific EOI Command in OCW2 (R=1, SL=1, EOI=0) and LO-L2=IRQ level to receive bottom priority.

#### 5.6.4.5 Poll Mode

Poll mode can be used to conserve space in the interrupt vector table. Multiple interrupts that can be serviced by one interrupt service routine do not need separate vectors if the service routine uses the poll command. Poll mode can also be used to expand the number of interrupts. The polling interrupt service routine can call the appropriate service routine, instead of providing the interrupt vectors in the vector table. In this mode, the INTR output is not used and the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=1 in OCW3. The PIC treats its next I/O read as an interrupt acknowledge, sets the appropriate ISR bit if there is a request, and reads the priority level. Interrupts are frozen from the OCW3 write to the I/O read. The byte returned during the I/O read contains a 1 in Bit 7 if there is an interrupt, and the binary code of the highest priority level in Bits 2:0.

#### 5.6.4.6 Edge and Level Triggered Mode

In ISA systems this mode is programmed using Bit 3 in ICW1, which sets level or edge for the entire controller. In the PCH, this bit is disabled and a register for edge and level triggered mode selection, per interrupt input, is included. This is the Edge/Level control registers ELCR1 and ELCR2.

If an ELCR bit is 0, an interrupt request will be recognized by a low-to-high transition on the corresponding IRQ input. The IRQ input can remain high without generating another interrupt. If an ELCR bit is 1, an interrupt request will be recognized by a high level on the corresponding IRQ input and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued to prevent a second interrupt from occurring.

In both the edge and level triggered modes, the IRQ inputs must remain active until after the falling edge of the first internal INTA#. If the IRQ input goes inactive before this time, a default IRQ7 vector is returned.

#### 5.6.4.7 End Of Interrupt (EOI) Operations

An EOI can occur in one of two fashions: by a command word write issued to the PIC before returning from a service routine, the EOI command; or automatically when AEOI bit in ICW4 is set to 1.

#### 5.6.4.8

#### Normal End of Interrupt

In normal EOI, software writes an EOI command before leaving the interrupt service routine to mark the interrupt as completed. There are two forms of EOI commands: Specific and Non-Specific. When a Non-Specific EOI command is issued, the PIC clears the highest ISR bit of those that are set to 1. Non-Specific EOI is the normal mode of operation of the PIC within the PCH, as the interrupt being serviced currently is the interrupt entered with the interrupt acknowledge. When the PIC is operated in modes that preserve the fully nested structure, software can determine which ISR bit to clear by issuing a Specific EOI. An ISR bit that is masked is not cleared by a Non-Specific EOI if the PIC is in the special mask mode. An EOI command must be issued for both the master and slave controller.

#### 5.6.4.9

#### Automatic End of Interrupt Mode

In this mode, the PIC automatically performs a Non-Specific EOI operation at the trailing edge of the last interrupt acknowledge pulse. From a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single PIC. The AEOI mode can only be used in the master controller and not the slave controller.

### 5.6.5

### Masking Interrupts

#### 5.6.5.1

#### Masking on an Individual Interrupt Request

Each interrupt request can be masked individually by the Interrupt Mask Register (IMR). This register is programmed through OCW1. Each bit in the IMR masks one interrupt channel. Masking IRQ2 on the master controller masks all requests for service from the slave controller.

#### 5.6.5.2

#### Special Mask Mode

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enables some of them for another portion.

The special mask mode enables all interrupts not masked by a bit set in the Mask register. Normally, when an interrupt service routine acknowledges an interrupt without issuing an EOI to clear the ISR bit, the interrupt controller inhibits all lower priority requests. In the special mask mode, any interrupts may be selectively enabled by loading the Mask Register with the appropriate pattern. The special mask mode is set by OCW3 where: SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

### 5.6.6

### Steering PCI Interrupts

The PCH can be programmed to allow PIRQA#–PIRQD# to be routed internally to interrupts 3–7, 9–12, 14, or 15. The assignment is programmable through the PIRQx Route Control registers, located at 60–63h and 68–6Bh in D31:F0. One or more PIRQx# lines can be routed to the same IRQx input. If interrupt steering is not required, the Route registers can be programmed to disable steering.

The PIRQx# lines are defined as active low, level sensitive to allow multiple interrupts on a PCI board to share a single line across the connector. When a PIRQx# is routed to specified IRQ line, software must change the IRQ's corresponding ELCR bit to level



sensitive mode. The PCH internally inverts the PIRQx# line to send an active high level to the PIC. When a PCI interrupt is routed onto the PIC, the selected IRQ can no longer be used by an active high device (through SERIRQ). However, active low interrupts can share their interrupt with PCI interrupts.

Internal sources of the PIRQs, including SCI and TCO interrupts, cause the external PIRQ to be asserted. The PCH receives the PIRQ input, like all of the other external sources, and routes it accordingly.

## 5.7 Advanced Programmable Interrupt Controller (APIC) (D31:F0)

In addition to the standard ISA-compatible PIC described in the previous section, the PCH incorporates the APIC. While the standard interrupt controller is intended for use in a uni-processor system, APIC can be used in either a uni-processor or multi-processor systems.

### 5.7.1 Interrupt Handling

The I/O APIC handles interrupts very differently than the 8259. Briefly, these differences are:

- **Method of Interrupt Transmission.** The I/O APIC transmits interrupts through memory writes on the normal data path to the processor. Interrupts are handled without the need for the processor to run an interrupt acknowledge cycle.
- **Interrupt Priority.** The priority of interrupts in the I/O APIC is independent of the interrupt number. For example, interrupt 10 can be given a higher priority than interrupt 3.
- **More Interrupts.** The I/O APIC in the PCH supports a total of 24 interrupts.
- **Multiple Interrupt Controllers.** The I/O APIC architecture allows for multiple I/O APIC devices in the system with their own interrupt vectors.

### 5.7.2 Interrupt Mapping

The I/O APIC within the PCH supports 40 APIC interrupts. Each interrupt has its own unique vector assigned by software. The interrupt vectors are mapped as indicated in the following table.

**Table 5-12. APIC Interrupt Mapping<sup>1</sup> (Sheet 1 of 2)**

IRQ #	Using SERIRQ	Direct from Pin	Using PCI Message	Internal Modules
0	No	No	No	Cascade from 8259 #1
1	Yes	No	Yes	
2	No	No	No	8254 Counter 0, HPET #0 (legacy mode)
3	Yes	No	Yes	
4	Yes	No	Yes	
5	Yes	No	Yes	GSPI, UART, I <sup>2</sup> C, SDIO
6	Yes	No	Yes	GSPI, UART, I <sup>2</sup> C, SDIO
7	Yes	No	Yes	GSPI, UART, I <sup>2</sup> C, SDIO
8	No	No	No	RTC, HPET #1 (legacy mode)

**Table 5-12. APIC Interrupt Mapping<sup>1</sup> (Sheet 2 of 2)**

IRQ #	Using SERIRQ	Direct from Pin	Using PCI Message	Internal Modules
9	Yes	No	Yes	Option for SCI, TCO
10	Yes	No	Yes	Option for SCI, TCO
11	Yes	No	Yes	HPET #2, Option for SCI, TCO (Note 2)
12	Yes	No	Yes	HPET #3 (Note 3)
13	No	No	No	GSPI, UART, I <sup>2</sup> C, SDIO
14	Yes	No	Yes	GPIO
15	Yes	No	Yes	GPIO
16	PIRQA#	PIRQA# <sup>5</sup>	Yes	Internal devices are routable.
17	PIRQB#	PIRQB# <sup>5</sup>		
18	PIRQC#	PIRQC# <sup>5</sup>		
19	PIRQD#	PIRQD# <sup>5</sup>		
20	N/A	PIRQE# <sup>4</sup>	Yes	Option for SCI, TCO, HPET #0, 1, 2, 3. Other internal devices are routable.
21	N/A	PIRQF# <sup>4</sup>		
22	N/A	PIRQG# <sup>4</sup>		
23	N/A	PIRQH# <sup>4</sup>		
24	No	PIRQI	No	
25	No	PIRQJ	No	
26	No	PIRQK	No	
27	No	PIRQL	No	
28	No	PIRQM	No	
29	No	PIRQN	No	
30	No	PIRQO	No	
31	No	PIRQP	No	
32	No	PIRQQ	No	
33	No	PIRQR	No	
34	No	PIRQS	No	
35	No	PIRQT	No	
36	No	PIRQU	No	
37	No	PIRQV	No	
38	No	PIRQW	No	
39	No	PIRQX	No	

**Notes:**

1. When programming the polarity of internal interrupt sources on the APIC, interrupts 0 through 15 receive active-high internal interrupt sources, while interrupts 16 through 23 receive active-low internal interrupt sources.
2. If IRQ 11 is used for HPET 2, software should ensure IRQ 11 is not shared with any other devices to ensure the proper operation of HPET 2. The PCH hardware does not prevent sharing of IRQ 11.
3. If IRQ 12 is used for HPET 3, software should ensure IRQ 12 is not shared with any other devices to ensure the proper operation of HPET 3. The PCH hardware does not prevent sharing of IRQ 12.
4. PIRQ[E:H] physical pins are not supported. The internal PIRQ[E:H]# are delivered internally to the internal interrupt controller.
5. PIRQ[A:D] are multiplexed with GPIO pins. Interrupts PIRQ[A:D] will not be exposed if they are configured as GPIOs. When configured as GPIO pins, the internal PIRQ[A:D]# are delivered internally to internal interrupt controller.



### 5.7.3 PCI/PCI Express\* Message-Based Interrupts

When external devices through PCI/PCI Express\* wish to generate an interrupt, they will send the message defined in the *PCI Express\* Base Specification*, Revision 2.0 for generating INTA# – INTD#. These will be translated to internal assertions/de-assertions of INTA# – INTD#.

### 5.7.4 IOxAPIC Address Remapping

To support Intel® Virtualization Technology (Intel® VT), interrupt messages are required to go through similar address remapping as any other memory request. Address remapping allows for domain isolation for interrupts; thus, a device assigned in one domain is not allowed to generate an interrupt to another domain.

The address remapping is based on the Bus: Device: Function field associated with the requests. The internal APIC is required to initiate the interrupt message using a unique Bus: Device: Function.

The PCH allows BIOS to program the unique Bus: Device: Function address for the internal APIC. This address field does not change the APIC functionality and the APIC is not promoted as a stand-alone PCI device. See Device 31: Function 0 Offset 6Ch for additional information.

### 5.7.5 External Interrupt Controller Support

The PCH supports external APICs off of PCI Express\* ports but does not support APICs on the PCI bus. The EOI special cycle is only forwarded to PCI Express\* ports.

## 5.8 Serial Interrupt (D31:F0)

The PCH supports a serial IRQ scheme. This allows a single signal to be used to report interrupt requests. The signal used to transmit this information is shared between the PCH and all participating peripherals. The signal line, SERIRQ, is synchronous to 24 MHz CLKOUT\_LPC, and follows the sustained tri-state protocol that is used by all PCI signals. This means that if a device has driven SERIRQ low, it will first drive it high synchronous to the 24-MHz clock and release it on the following 24-MHz clock. The serial IRQ protocol defines this sustained tri-state signaling in the following fashion:

- **S – Sample Phase**, Signal driven low
- **R – Recovery Phase**, Signal driven high
- **T – Turn-around Phase**, Signal released

The PCH supports a message for 21 serial interrupts. These represent the 15 ISA interrupts (IRQ0–1, 3–15), the four PCI interrupts, and the control signals SMI# and IOCHK#. The serial IRQ protocol does not support the additional APIC interrupts (20–23).

**Note:**

IRQ14 and IRQ15 are special interrupts and can be used by the GPIO controller when it is running GPIO driver mode. When the GPIO controller operates in GPIO driver mode, IRQ14 and IRQ15 shall not be utilized by the SERIRQ stream nor mapped to other interrupt sources, and instead come from the GPIO controller. If the GPIO controller is entirely in ACPI mode, these interrupts can be mapped to other devices accordingly.

## 5.8.1 Start Frame

The serial IRQ protocol has two modes of operation that affect the start frame. These two modes are: Continuous, where the PCH is solely responsible for generating the start frame; and Quiet, where a serial IRQ peripheral is responsible for beginning the start frame.

The mode that must first be entered when enabling the serial IRQ protocol is Continuous mode. In this mode, the PCH asserts the start frame. This start frame is 4, 6, or 8 24-MHz clocks wide based upon the Serial IRQ Control register, bits 1:0 at 64h in D31:F0 configuration space. This is a polling mode.

When the serial IRQ stream enters Quiet mode (signaled in the Stop Frame), the SERIRQ line remains inactive and pulled up between the Stop and Start Frame until a peripheral drives the SERIRQ signal low. The PCH senses the line low and continues to drive it low for the remainder of the Start Frame. Since the first 24-MHz clock of the start frame was driven by the peripheral in this mode, the PCH drives the SERIRQ line low for one 24-MHz clock less than in continuous mode. This mode of operation allows for a quiet, and therefore lower power, operation.

## 5.8.2 Data Frames

Once the Start frame has been initiated, all of the SERIRQ peripherals must start counting frames based on the rising edge of SERIRQ. Each of the IRQ/DATA frames has exactly 3 phases of 1 clock each:

- **Sample Phase**—During this phase, the SERIRQ device drives SERIRQ low if the corresponding interrupt signal is low. If the corresponding interrupt is high, the SERIRQ devices tri-state the SERIRQ signal. The SERIRQ line remains high due to pull-up resistors (there is no internal pull-up resistor on this signal; an external pull-up resistor is required). A low level during the IRQ0-1 and IRQ2-15 frames indicates that an active-high ISA interrupt is not being requested; however, a low level during the PCI INT[A:D], SMI#, and IOCHK# frame indicates that an active-low interrupt is being requested.
- **Recovery Phase**—During this phase, the device drives the SERIRQ line high if in the Sample Phase, it was driven low. If it was not driven in the sample phase, it is tri-stated in this phase.
- **Turn-around Phase**—The device tri-states the SERIRQ line.

## 5.8.3 Stop Frame

After all data frames, a Stop Frame is driven by the PCH. The SERIRQ signal is driven low by the PCH for two or three 24-MHz clocks. The number of clocks is determined by the SERIRQ configuration register. The number of clocks determines the next mode.

Table 5-13. Stop Frame Explanation

Stop Frame Width	Next Mode
two 24-MHz clocks	<b>Quiet Mode</b> —Any SERIRQ device may initiate a Start Frame.
three 24-MHz clocks	<b>Continuous Mode</b> —Only the host (the PCH) may initiate a Start Frame.

## 5.8.4 Specific Interrupts Not Supported Using SERIRQ

There are three interrupts seen through the serial stream that are not supported by the PCH. These interrupts are generated internally, and are not sharable with other devices within the system. These interrupts are:

- IRQ0. Heartbeat interrupt generated off of the internal 8254 counter 0.
- IRQ8#. RTC interrupt can only be generated internally.
- IRQ13. Reserved internally.

The PCH ignores the state of these interrupts in the serial stream, and does not adjust their level based on the level seen in the serial stream.

## 5.8.5 Data Frame Format

Table 5-14 shows the format of the data frames. For the PCI interrupts (A-D), the output from the PCH is AND'd with the PCI input signal. This way, the interrupt can be signaled using both the PCI interrupt input signal and using the SERIRQ signal (they are shared).

**Table 5-14. Data Frame Format**

Data Frame #	Interrupt	Clocks Past Start Frame	Comment
1	IRQ0	2	Ignored. IRQ0 can only be generated using the internal 8524
2	IRQ1	5	Before port 60h latch
3	SMI#	8	Causes SMI# if low. Will set the SERIRQ_SMI_STS bit.
4	IRQ3	11	
5	IRQ4	14	
6	IRQ5	17	
7	IRQ6	20	
8	IRQ7	23	
9	IRQ8	26	Ignored. IRQ8# can only be generated internally.
10	IRQ9	29	
11	IRQ10	32	
12	IRQ11	35	
13	IRQ12	38	Before port 60h latch
14	IRQ13	41	Ignored.
15	IRQ14	44	Not attached to GPIO logic
16	IRQ15	47	Not attached to GPIO logic
17	IOCHCK#	50	Same as ISA IOCHCK# going active
18	PCI INTA#	53	Drive PIRQA#
19	PCI INTB#	56	Drive PIRQB#
20	PCI INTC#	59	Drive PIRQC#
21	PCI INTD#	62	Drive PIRQD#

## 5.9 Real Time Clock (D31:F0)

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device with two banks of static RAM with 128 bytes each, although the first bank has 114 bytes for general purpose usage. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122 – 500 ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. Daylight savings compensation is no longer supported. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768 KHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block has very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers that configure and report RTC functions.

The time and calendar data should match the data mode (BCD or binary) and hour mode (12 or 24 hour) as selected in Register B. It is up to the programmer to make sure that data stored in these locations is within the reasonable values ranges and represents a possible date and time. The exception to these ranges is to store a value of C0-FFh in the Alarm bytes to indicate a don't care situation. All Alarm conditions must match to trigger an Alarm Flag that could trigger an Alarm Interrupt, if enabled. The SET bit must be 1 while programming these locations to avoid clashes with an update cycle. Access to time and date information is done through the RAM locations. If a RAM read from the ten time and date bytes is attempted during an update cycle, the value read do not necessarily represent the true contents of those locations. Any RAM writes under the same conditions are ignored.

**Note:** The leap year determination for adding a 29th day to February does not take into account the end-of-the-century exceptions. The logic simply assumes that all years divisible by 4 are leap years. According to the Royal Observatory Greenwich, years that are divisible by 100 are typically not leap years. In every fourth century (years divisible by 400, like 2000), the 100-year exception is over-ridden and a leap year occurs.

**Note:** The year 2100 will be the first time in which the current RTC implementation would incorrectly calculate the leap year.

The PCH does not implement month/year alarms.

### 5.9.1 Update Cycles

An update cycle occurs once a second, if the SET bit of Register B is not asserted and the divide chain is properly configured. During this procedure, the stored time and date are incremented, overflow is checked, a matching alarm condition is checked, and the time and date are rewritten to the RAM locations. The update cycle will start at least 488  $\mu$ s after the UIP bit of Register A is asserted, and the entire cycle does not take more than 1984  $\mu$ s to complete. The time and date RAM locations (0-9) are disconnected from the external bus during this time.

To avoid update and data corruption conditions, external RAM access to these locations can safely occur at two times. When an updated-ended interrupt is detected, almost 999 ms is available to read and write the valid time and date data. If the UIP bit of Register A is detected to be low, there is at least 488  $\mu$ s before the update cycle begins.

**Warning:** The overflow conditions for leap years adjustments are based on more than one date or time item. To ensure proper operation when adjusting the time, the new time and data values should be set at least two seconds before leap year occurs.



## 5.9.2 Interrupts

The real-time clock interrupt is internally routed within the PCH; both to the I/O APIC and the 8259. It is mapped to interrupt vector 8. This interrupt does not leave the PCH, nor is it shared with any other interrupt. IRQ8# from the SERIRQ stream is ignored. However, the High Performance Event Timers can also be mapped to IRQ8#; in this case, the RTC interrupt is blocked.

## 5.9.3 Lockable RAM Ranges

The RTC battery-backed RAM supports two 8-byte ranges that can be locked using the configuration space. If the locking bits are set, the corresponding range in the RAM will not be readable or writable. A write cycle to those locations will have no effect. A read cycle to those locations will not return the location's actual value (resultant value is undefined).

Once a range is locked, the range can be unlocked only by a hard reset, which will invoke the BIOS and allow it to relock the RAM range.

## 5.9.4 Century Rollover

The PCH detects a rollover when the Year byte (RTC I/O space, index Offset 09h) transitions from 99 to 00. Upon detecting the rollover, the PCH sets the NEWCENTURY\_STS bit (TCOBASE + 04h, Bit 7). If the system is in an S0 state, this causes an SMI#. The SMI# handler can update registers in the RTC RAM that are associated with century value. If the system is in a sleep state (S1 – S5) when the century rollover occurs, the PCH also sets the NEWCENTURY\_STS bit, but no SMI# is generated. When the system resumes from the sleep state, BIOS should check the NEWCENTURY\_STS bit and update the century value in the RTC RAM.

## 5.9.5 Clearing Battery-Backed RTC RAM

Clearing CMOS RAM in a PCH-based platform can be done by using a jumper on RTCRST# or GPI. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.

### Using RTCRST# to Clear CMOS

A jumper on RTCRST# can be used to clear CMOS values, as well as reset to default, the state of those configuration bits that reside in the RTC power well. When the RTCRST# is strapped to ground, the RTC\_PWR\_STS bit (D31:F0:A4h Bit 2) will be set and those configuration bits in the RTC power well will be set to their default state. BIOS can monitor the state of this Bit, and manually clear the RTC CMOS array once the system is booted. The normal position would cause RTCRST# to be pulled up through a weak pull-up resistor. [Table 5-15](#) shows which bits are set to their default state when RTCRST# is asserted. This RTCRST# jumper technique allows the jumper to be moved and then replaced; all while the system is powered off. Then, once booted, the RTC\_PWR\_STS can be detected in the set state.

Table 5-15. Configuration Bits Reset by RTCRST# Assertion

Bit Name	Register	Location	Bit(s)	Default State
Alarm Interrupt Enable (AIE)	Register B (General Configuration) (RTC_REGB)	I/O space (RTC Index + 0Bh)	5	X
Alarm Flag (AF)	Register C (Flag Register) (RTC_REGC)	I/O space (RTC Index + 0Ch)	5	X
SWSMI_RATE_SEL	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	7:6	0
SLP_S4# Minimum Assertion Width	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	5:4	0
SLP_S4# Assertion Stretch Enable	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	3	0
RTC Power Status (RTC_PWR_STS)	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	2	0
Power Failure (PWR_FLR)	General PM Configuration 3 Register (GEN_PMCON_3)	D31:F0:A4h	1	0
AFTERG3_EN	General PM Configuration 3 Register GEN_PMCON_3	D31:F0:A4h	0	0
Power Button Override Status (PRBTNOR_STS)	Power Management 1 Status Register (PM1_STS)	PMBase + 00h	11	0
RTC Event Enable (RTC_EN)	Power Management 1 Enable Register (PM1_EN)	PMBase + 02h	10	0
Sleep Type (SLP_TYP)	Power Management 1 Control (PM1_CNT)	PMBase + 04h	12:10	0
PME_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	11	0
BATLOW_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	10	0
RI_EN	General Purpose Event 0 Enables Register (GPE0_EN)	PMBase + 2Ch	8	0
NEWCENTURY_STS	TCO1 Status Register (TCO1_STS)	TCOBase + 04h	7	0
Intruder Detect (INTRD_DET)	TCO2 Status Register (TCO2_STS)	TCOBase + 06h	0	0
Top Swap (TS)	Backed Up Control Register (BUC)	Chipset Configuration Registers:Offset 3414h	0	X

### Using a GPI to Clear CMOS

A jumper on a GPI can also be used to clear CMOS values. BIOS would detect the setting of this GPI on system boot-up, and manually clear the CMOS array.

**Note:** The GPI strap technique to clear CMOS requires multiple steps to implement. The system is booted with the jumper in new position; then powered back down. The jumper is replaced back to the normal position; then the system is rebooted again.

**Warning:** Do not implement a jumper on VccRTC to clear CMOS.



## 5.10 Processor Interface (D31:F0)

The PCH interfaces to the processor with following pin-based signals other than OPI:

- Standard Outputs to processor: PROCPWRGD, PMSYNCH, PECI
- Standard Input from processor: THRMTRIP#

Most PCH outputs to the processor use standard buffers.

The following processor interface legacy pins were removed from the PCH:

- A20M#, SMI#, NMI, INIT#, INTR, FERR#: Functionality has been replaced by in-band Virtual Legacy Wire (VLW) messages. See [Section 5.10.3](#).

### 5.10.1 Processor Interface Signals and VLW Messages

This section describes each of the signals that interface between the PCH and the processor(s). The behavior of some signals may vary during processor reset, as the signals are used for frequency strapping.

#### 5.10.1.1 INIT (Initialization)

The INIT# VLW Message is asserted based on any one of several events described in [Table 5-16](#). When any of these events occur, INIT# is asserted for sixteen 24-MHz clocks, then driven high.

**Table 5-16. INIT# Going Active**

Cause of INIT# Going Active	Comment
Shutdown special cycle from processor observed on PCH-processor interconnect.	INIT assertion based on value of Shutdown Policy Select register (SPS)
PORT92 write, where INIT_NOW (Bit 0) transitions from a 0 to a 1.	
PORTCF9 write, where SYS_RST (Bit 1) was a 0 and RST_CPU (Bit 2) transitions from 0 to 1.	
RCIN# input signal goes low for at least twenty-five 24-MHz clocks. RCIN# is expected to be driven by the external microcontroller (KBC).	0-to-1 transition on RCIN# must occur before the PCH will arm INIT# to be generated again. In the case when INIT# causes a reset, RCIN#/GPIO82 will reset to the default GPI mode and cause INIT# to internally transition from 0-to-1. <b>Note:</b> To prevent a 2nd reset due to the same RCIN# assertion, RCIN# must de-assert prior to PLTRST# de-assertion. <b>Note:</b> RCIN# signal is expected to be low during S3, S4, and S5 states. Transition on the RCIN# signal in those states (or the transition to those states) may not necessarily cause the INIT# signal to be generated to the processor.
Processor BIST	To enter BIST, software sets CPU_BIST_EN bit and then does a full processor reset using the CF9 register.

### 5.10.1.2 FERR# (Numeric Coprocessor Error)

The PCH supports the coprocessor error function with the FERR# message. The function is enabled using the CEN bit. If FERR# is driven active by the processor, IRQ13 goes active (internally). When it detects a write to the COPROC\_ERR register (I/O Register F0h), the PCH negates the internal IRQ13 and IGNNE# will be active. IGNNE# remains active until FERR# is driven inactive. IGNNE# is never driven active unless FERR# is active.

**Note:** IGNNE# (Ignore Numeric Error) is now internally generated by the processor.

### 5.10.1.3 NMI (Non-Maskable Interrupt)

Non-Maskable Interrupts (NMIs) can be generated by several sources, as described in Table 5-17.

**Table 5-17. NMI Sources**

Cause of NMI	Comment
SERR# goes active (either internally, externally using SERR# signal, or using message from processor)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (D31:F0, TCO Base + 08h, Bit 11).
IOCHK# goes active using SERIRQ# stream (ISA system Error)	Can instead be routed to generate an SCI, through the NMI2SCI_EN bit (D31:F0, TCO Base + 08h, Bit 11).
SECSTS register D31:F0 Offset 1Eh, bit 8.	This is enabled by the Parity Error Response Bit (PER).
DEV_STS register D31:F0 Offset 06h, bit 8	This is enabled by the Parity Error Response Bit (PER).
GPIO[15:0] when configured as a General Purpose input and routed as NMI (by GPIO_ROUT at D31:F0 Offset B8)	This is enabled by GPI NMI Enable (GPI_NMI_EN) bits at D31:F0 Offset: GPIOBASE + 28h bits 15:0

### 5.10.1.4 Processor Power Good (PROCPWRGD)

This signal is connected to the processor's UNCOREPWRGOOD input to indicate when the processor power is valid.

## 5.10.2 Dual-Processor Issues

### 5.10.2.1 Usage Differences

In dual-processor designs, some of the processor signals are unused or used differently than for uniprocessor designs.

- FERR# are generally not used, but still supported.
- I/O APIC and SMI# are assumed to be used.



### 5.10.3 Virtual Legacy Wire (VLW) Messages

The PCH supports VLW messages as alternative method of conveying the status of the following legacy sideband interface signals to the processor:

- A20M#, INTR, SMI#, INIT#, NMI

**Note:** IGNNE# VLW message is not required to be generated by the PCH as it is internally emulated by the processor.

VLW are inbound messages to the processor. They are communicated using Vendor Defined Message over the DMI link.

Legacy processor signals can only be delivered using VLW in the PCH. Delivery of legacy processor signals (A20M#, INTR, SMI#, INIT#, or NMI) using I/O APIC controller is not supported.

## 5.11 Power Management

### 5.11.1 Features

- Support for *Advanced Configuration and Power Interface, Version 4.0a (ACPI)* providing power and thermal management
  - ACPI 24-Bit Timer SCI and SMI# Generation
- PCI PME# signal for Wake Up from low-power states
- System Sleep State Control
  - ACPI S3 state – Suspend to RAM (STR)
  - ACPI S4 state – Suspend-to-Disk (STD)
  - ACPI G2/S5 state – Soft Off (SOFF)
  - Power Failure Detection and Recovery
  - Deep Sx
- Intel® Management Engine Power Management Support
  - Wake events from the Intel® Management Engine (enabled from all S-states including Catastrophic S5 conditions)
- SLP\_S0# signal for external platform VR power gating or EC power management handling during lower-power condition
- NEW: **(U-Processor Line)** HSIOPC signal for power gating VCCHSIO, VCCSATA3PLL and VCCUSB3PLL supply rails during port idle condition. **(Intel® Core™ M processor)** Ability to individually power gate VCCPCIEPHY, VCCSATAPHY and VCCUSB3PHY supply rail during port idle condition.
- NEW: Windows\* InstantGo Power Save Mode (Windows\* InstantGo PSM)

### 5.11.2 Power Management Controller (PMC)

The Power Management Controller (PMC) is the PCH unit that handles all PCH power management related activities. This unit administers power management functions of the PCH including interfacing with other logic and controllers on the platform to perform

power state transitions (such as SLP\_S3# and PLTRST#); configure, manage and respond to wake events; aggregate and report latency tolerance information for devices and peripherals connected to and integrated into the PCH.

### 5.11.3 PCH and System Power States

Table 5-18 shows the power states defined for PCH-based platforms. The state names generally match the corresponding ACPI states.

**Table 5-18. General Power States for Systems Using the PCH**

State/ Substates	Legacy Name/Description
G0/S0/C0	<b>Full On:</b> Processor operating. Individual devices may be shut down or be placed into lower power states to save power.
G0/S0/Cx	<b>Cx State:</b> Cx states are processor power states within the S0 system state that provide for various levels of power savings. The processor initiates C-State entry and exit while interacting with the PCH. The PCH will base its behavior on the processor state.
G1/S1	<b>S1:</b> The PCH provides the S1 messages and the S0 messages on a wake event. It is preferred for systems to use C-States than S1.
G1/S3	<b>Suspend-To-RAM (STR):</b> The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained and refreshes continue. All external clocks stop except RTC.
G1/S4	<b>Suspend-To-Disk (STD):</b> The context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
G2/S5	<b>Soft Off (SOFF):</b> System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.
Deep Sx	<b>Deep Sx:</b> An optional low power state where system context may or may not be maintained depending upon entry condition. All power is shut off except for minimal logic that allows exiting Deep Sx. If Deep Sx state was entered from S3 state, then the resume path will place system back into S3. If Deep Sx state was entered from S4 state, then the resume path will place system back into S4. If Deep Sx state was entered from S5 state, then the resume path will place system back into S5.
G3	<b>Mechanical OFF (M-Off):</b> System context not maintained. All power is shut off except for the RTC. No "Wake" events are possible. This state occurs if the user removes the main system batteries in a mobile system, turns off a mechanical switch, or if the system power supply is at a level that is insufficient to power the "waking" logic. When system power returns, transition will depend on the state just prior to the entry to G3 and the AFTERG3_EN bit in the GEN_PMCN_3 register (D31:F0, offset A4). Refer to Table 5-25 for more details.

Table 5-19 shows the transitions rules among the various states.

**Note:**

Transitions among the various states may appear to temporarily transition through intermediate states. For example, in going from S0 to S3, it may appear to pass through the G1/S1 states. These intermediate transitions and states are not listed in the Table 5-19.

**Table 5-19. State Transition Rules for the PCH**

Present State	Transition Trigger	Next State
G0/S0/C0	<ul style="list-style-type: none"> <li>• OPI Msg</li> <li>• SLP_EN bit set</li> <li>• Power Button Override<sup>3,5</sup></li> <li>• Mechanical Off/Power Failure</li> </ul>	<ul style="list-style-type: none"> <li>• G0/S0/Cx</li> <li>• G1/Sx or G2/S5 state</li> <li>• G2/S5</li> <li>• G3</li> </ul>
G0/S0/Cx	<ul style="list-style-type: none"> <li>• OPI Msg</li> <li>• Power Button Override<sup>3,5</sup></li> <li>• Mechanical Off/Power Failure</li> </ul>	<ul style="list-style-type: none"> <li>• G0/S0/C0</li> <li>• S5</li> <li>• G3</li> </ul>
G1/S1 or G1/S3	<ul style="list-style-type: none"> <li>• Any Enabled Wake Event</li> <li>• Power Button Override<sup>3,5</sup></li> <li>• Conditions met as described in <a href="#">Section 5.11.8.6.1</a> and <a href="#">Section 5.11.8.6.2</a></li> <li>• Mechanical Off/Power Failure</li> </ul>	<ul style="list-style-type: none"> <li>• G0/S0/C0<sup>2</sup></li> <li>• G2/S5</li> <li>• Deep Sx</li> <li>• G3</li> </ul>
G1/S4	<ul style="list-style-type: none"> <li>• Any Enabled Wake Event</li> <li>• Power Button Override<sup>3,5</sup></li> <li>• Conditions met as described in <a href="#">Section 5.11.8.6.1</a> and <a href="#">Section 5.11.8.6.2</a></li> <li>• Mechanical Off/Power Failure</li> </ul>	<ul style="list-style-type: none"> <li>• G0/S0/C0<sup>2</sup></li> <li>• G2/S5</li> <li>• Deep Sx</li> <li>• G3</li> </ul>
G2/S5	<ul style="list-style-type: none"> <li>• Any Enabled Wake Event</li> <li>• Conditions met as described in <a href="#">Section 5.11.8.6.1</a> and <a href="#">Section 5.11.8.6.2</a></li> <li>• Mechanical Off/Power Failure</li> </ul>	<ul style="list-style-type: none"> <li>• G0/S0/C0<sup>2</sup></li> <li>• Deep Sx</li> <li>• G3</li> </ul>
G2/Deep Sx	<ul style="list-style-type: none"> <li>• Any Enabled Wake Event</li> <li>• ACPRESENT Assertion</li> <li>• Mechanical Off/Power Failure</li> </ul>	<ul style="list-style-type: none"> <li>• G0/S0/C0<sup>2</sup></li> <li>• G1/S3, G1/S4 or G2/S5 (see <a href="#">Section 5.11.8.6.2</a>)</li> <li>• G3</li> </ul>
G3	<ul style="list-style-type: none"> <li>• Power Returns</li> </ul>	<ul style="list-style-type: none"> <li>• S0/C0 (reboot) or G2/S5<sup>4</sup> (stay off until power button pressed or other wake event)<sup>1,2</sup></li> </ul>

**Notes:**

1. Some wake events can be preserved through power failure.
2. Transitions from the S1 – S5 or G3 states to the S0 state are deferred until BATLOW# is inactive in mobile configurations.
3. Includes all other applicable types of events that force the host into and stay in G2/S5.
4. If the system was in G1/S4 before G3 entry, then the system will go to S0/C0 or G1/S4.
5. Upon entry to S5 due to a power button override, if Deep Sx is enabled and conditions are met per [Section 5.11.8.6](#), the system will transition to Deep Sx.

## 5.11.4 System Power Planes

The system has several independent power planes, as described in Table 5-20.

**Note:** When a particular power plane is shut off, it should go to a 0V level.

**Table 5-20. System Power Plane**

Plane	Controlled By	Description
Processor	SLP_S3# signal	The SLP_S3# signal can be used to cut the power to the processor completely.
Main	SLP_S3# signal	When SLP_S3# goes active, power can be shut off to any circuit not required to wake the system from the S3 state. Since the S3 state requires that the memory context be preserved, power must be retained to the main memory. The processor, devices on the PCI bus, LPC I/F, and graphics will typically be shut off when the Main power plane is off; although, there may be small subsections powered.
Memory	SLP_S4# signal SLP_S5# signal	When SLP_S4# goes active, power can be shut off to any circuit not required to wake the system from the S4. Since the memory context does not need to be preserved in the S4 state, the power to the memory can also be shut down. When SLP_S5# goes active, power can be shut off to any circuit not required to wake the system from the S5 state. Since the memory context does not need to be preserved in the S5 state, the power to the memory can also be shut.
Intel® ME	SLP_A#	This signal is asserted when the manageability platform goes to M-Off. Depending on the platform, this pin may be used to control the Intel® Management Engine power planes, LAN subsystem power, and the SPI flash power.
LAN	SLP_LAN#	This signal is asserted in Sx/M-Off when both host and Intel® ME WoL are not supported. This signal can be used to control power to the Intel GbE PHY.
Suspend Well	SLP_SUS#	This signal is asserted when the Sus rails can be externally shut off for enhanced power saving.
DEVICE[n]	Implementation Specific	Individual subsystems may have their own power plane. For example, GPIO signals may be used to control the power to disk drives, audio amplifiers, or the display screen.

## 5.11.5 SMI#/SCI Generation

Upon any enabled SMI event taking place while the End of SMI (EOS) bit is set, the PCH will clear the EOS bit and assert SMI to the processor, which will cause it to enter SMM space. SMI assertion is performed using a Virtual Legacy Wire (VLW) message. Prior system generations (those based upon legacy processors) used an actual SMI# pin.

Once the SMI VLW has been delivered, the PCH takes no action on behalf of active SMI events until Host software sets the End of SMI (EOS) bit. At that point, if any SMI events are still active, the PCH will send another SMI VLW message.

The SCI is a level-mode interrupt that is typically handled by an ACPI-aware operating system. In non-APIC systems (which is the default), the SCI IRQ is routed to one of the 8259 interrupts (IRQ 9, 10, or 11). The 8259 interrupt controller must be programmed to level mode for that interrupt.

In systems using the APIC, the SCI can be routed to interrupts 9, 10, 11, 20, 21, 22, or 23. The interrupt polarity changes depending on whether it is on an interrupt shareable with a PIRQ or not. The interrupt remains asserted until all SCI sources are removed.



Table 5-21 shows which events can cause an SMI and SCI.

- Note:** Some events can be programmed to cause either an SMI or SCI. The usage of the event for SCI (instead of SMI) is typically associated with an ACPI-based system. Each SMI or SCI source has a corresponding enable and status bit.
- Note:** All GPIO[94:0] are capable of SCI generation, but only GPIO[47:32] are capable of NMI generation and SMI generation. See D31:F0 for details on GPIO configuration.

**Table 5-21. Causes of SMI and SCI (Sheet 1 of 2)**

Cause	SCI	SMI	Additional Enables	Where Reported
PME#	Yes	Yes	PME_EN=1	PME_STS
PME_B0 (Internal, Bus 0, PME-Capable Agents)	Yes	Yes	PME_B0_EN=1	PME_B0_STS
PCI Express* PME Messages	Yes	Yes	PCI_EXP_EN=1 (Not enabled for SMI)	PCI_EXP_STS
PCI Express* Hot-Plug Message	Yes	Yes	HOT_PLUG_EN=1 (Not enabled for SMI)	HOT_PLUG_STS
Power Button Press	Yes	Yes	PWRBTN_EN=1	PWRBTN_STS
Power Button Override (Note 7)	Yes	No	None	PRBTNOR_STS
RTC Alarm	Yes	Yes	RTC_EN=1	RTC_STS
Ring Indicate	Yes	Yes	RI_EN=1	RI_STS
ACPI Timer overflow (2.34 seconds)	Yes	Yes	TMROF_EN=1	TMROF_STS
TCO SCI Logic	Yes	No	TCOSCI_EN=1	TCOSCI_STS
GPIO[94:48]	Yes	No	GPI_ROUTE[94:48] 0 = SCI 1 = NMI or SMI (dependant on respective NMI_EN or ALT_GPI_SMI_EN) GPE0_EN[94:64], GPE0_EN[63:32]	GPE0_STS[94:64], GPE0_STS[63:32]
GPIO[47:32]	Yes	Yes	GPI_ROUTE[47:32] 0 = SCI 1 = NMI or SMI (dependant on respective NMI_EN or ALT_GPI_SMI_EN) GPE0_EN[63:32] GPI_NMI_EN[47:32] ALT_GPI_SMI_EN[47:32]	GPE0_STS[63:32] GPI_NMI_STS[47:32] ALT_GPI_SMI_STS[47:32]
GPIO[31:0]	Yes	No	GPI_ROUTE[31:0] 0 = SCI 1 = NMI or SMI (dependant on respective NMI_EN or ALT_GPI_SMI_EN) GPE0_EN[31:0]	GPE0_STS[31:0]
TCO SCI message from processor	Yes	No	None	OPISCI_STS
TCO SMI Logic	No	Yes	TCO_EN=1	TCO_STS
TCO SMI - Century Rollover	No	Yes	None	NEWCENTURY_STS
TCO SMI - TCO TIMEROUT	No	Yes	None	TIMEOUT
TCO SMI - OS writes to TCO_DAT_IN register	No	Yes	None	SW_TCO_SMI
TCO SMI - Message from processor	No	Yes	None	OPISMI_STS
TCO SMI - NMI occurred (and NMIs mapped to SMI)	No	Yes	NMI2SMI_EN=1	NMI2SMI_STS

Table 5-21. Causes of SMI and SCI (Sheet 2 of 2)

Cause	SCI	SMI	Additional Enables	Where Reported
TCO SMI – INTRUDER# signal goes active	No	Yes	INTRD_SEL=10	INTRD_STS
TCO SMI – Change of the BIOSWE (D31:F0:DCh, Bit 0) bit from 0 to 1	No	Yes	BLE=1	BIOSWR_STS
TCO SMI – Write attempted to BIOS	No	Yes	BIOSWE=1	BIOSWR_STS
BIOS_RLS written to	Yes	No	GBL_EN=1	GBL_STS
GBL_RLS written to	No	Yes	BIOS_EN=1	BIOS_STS
Write to B2h register	No	Yes	APMC_EN = 1	APM_STS
Periodic timer expires	No	Yes	PERIODIC_EN=1	PERIODIC_STS
64 ms timer expires	No	Yes	SWSMI_TMR_EN=1	SWSMI_TMR_STS
Enhanced USB Legacy Support Event	No	Yes	LEGACY_USB2_EN = 1	LEGACY_USB2_STS
Enhanced USB Intel Specific Event	No	Yes	INTEL_USB2_EN = 1	INTEL_USB2_STS
Serial IRQ SMI reported	No	Yes	None	SERIRQ_SMI_STS
Device monitors match address in its range	No	Yes	None	DEVTRAP_STS
SMBus Host Controller	No	Yes	SMB_SMI_EN Host Controller Enabled	SMBus host status register
SMBus Slave SMI message	No	Yes	None	SMBUS_SMI_STS
SMBus SMBALERT# signal active	No	Yes	None	SMBUS_SMI_STS
SMBus Host Notify message received	No	Yes	HOST_NOTIFY_INTREN	SMBUS_SMI_STS HOST_NOTIFY_STS
(Mobile Only) BATLOW# assertion	Yes	Yes	BATLOW_EN=1	BATLOW_STS
Access microcontroller 62h/66h	No	Yes	MCSMI_EN	MCSMI_STS
SLP_EN bit written to 1	No	Yes	SLP_SMI_EN=1	SLP_SMI_STS
SPI Command Completed	No	Yes	None	SPI_STS
Software Generated GPE	Yes	Yes	SWGPE_EN=1	SWGPE_STS
USB Per-Port Registers Write Enable bit changes to 1	No	Yes	INTEL_USB2_EN=1, Write_Enable_SMI_Enable=1	INTEL_USB2_STS, Write Enable Status
GPIO Lockdown Enable bit changes from '1' to '0'	No	Yes	GPIO_UNLOCK_SMI_EN=1	GPIO_UNLOCK_SMI_STS
Wake Alarm Device Timer	Yes	Yes	WADT_EN	WADT_STS

**Notes:**

1. SCI\_EN must be 1 to enable SCI, except for BIOS\_RLS. SCI\_EN must be 0 to enable SMI.
2. SCI can be routed to cause interrupt 9:11 or 20:23 (20:23 only available in APIC mode).
3. GBL\_SMI\_EN must be 1 to enable SMI.
4. EOS must be written to 1 to re-enable SMI for the next 1.
5. The PCH must have SMI fully enabled when the PCH is also enabled to trap cycles. If SMI is not enabled in conjunction with the trap enabling, then hardware behavior is undefined.
6. Only GPI[15:0] may generate an SMI or SCI.
7. When a power button override first occurs, the system will transition immediately to S5. The SCI will only occur after the next wake to S0 if the residual status bit (PRBTNOR\_STS) is not cleared prior to setting SCI\_EN.
8. GBL\_STS being set will cause an SCI, even if the SCI\_EN bit is not set. Software must take great care not to set the BIOS\_RLS bit (which causes GBL\_STS to be set) if the SCI handler is not in place.

### 5.11.5.1 PCI Express\* SCI

PCI Express\* ports and the processor have the ability to cause PME using messages. When a PME message is received, the PCH will set the PCI\_EXP\_STS bit. If the PCI\_EXP\_EN bit is also set, the PCH can cause an SCI using the GPE1\_STS register.



### 5.11.5.2 PCI Express\* Hot-Plug

PCI Express\* has a hot-plug mechanism and is capable of generating a SCI using the GPE1 register. It is also capable of generating an SMI. However, it is not capable of generating a wake event.

### 5.11.6 C-States

PCH-based systems implement C-States by having the processor control the states. The Chipset exchanges messages with the processor as part of the C-State flow, but the Chipset does not directly control any of the processor impacts of C-States, such as voltage levels or processor clocking. In addition to the messages, the PCH also provides additional information to the processor using a sideband pin (PMSYNCH). All of the legacy C-State related pins (STPCLK#, STP\_CPU#, DPRSLP#, DPRSLPVR#, and so on) do not exist on the PCH.

### 5.11.7 Dynamic 24 MHz Clock Control

The 24 MHz clock can be dynamically controlled independent of any other low-power state.

The Dynamic 24 MHz Clock control is handled using the following signal:

- CLKRUN#: Used by LPC peripherals or other legacy devices to request the system 24 MHz clock to run.

#### 5.11.7.1 Conditions for Checking the 24 MHz Clock

When there is a lack of activity, the PCH has the capability to stop the 24 MHz clocks to conserve power. “Clock activity” is defined as any activity that would require the 24 MHz clock to be running.

Any of the following conditions will indicate that it is **not okay** to stop the 24 MHz clock:

- Cycles on LPC
- Cycles of any internal source that would need to go on the LPC bus
- Cycles using internal DMA
- SERIRQ activity

#### Behavioral Description

When there is a lack of activity (as defined above) for twenty nine to thirty 24 MHz clock cycles, the PCH de-asserts (drive high) CLKRUN# for 1 clock and then tri-states the signal.

### 5.11.7.2 Conditions for Maintaining the 24 MHz Clock

LPC or any other devices that wish to maintain the 24 MHz clock running will observe the CLKRUN# signal de-asserted, and then must re-assert it (drive it low) within two to three 24-MHz clocks.

- When the PCH has tri-stated the CLKRUN# signal after de-asserting it, the PCH then checks to see if the signal has been re-asserted (externally).
- After observing the CLKRUN# signal asserted for 1 clock, the PCH again starts asserting the signal.
- If an internal device needs the LPC bus, the PCH asserts the CLKRUN# signal.

### 5.11.7.3 Conditions for Stopping the 24 MHz Clock

- If no device drives CLKRUN# low within six 24-MHz clock cycles after it has been de-asserted, the PCH will stop the 24 MHz clocks.

### 5.11.7.4 Conditions for Re-starting the 24 MHz Clock

- Observing the CLKRUN# signal asserted externally for 1 (free running) 24-MHz clock, the PCH again starts driving CLKRUN# asserted.

If an internal source requests the clock to be re-started, the PCH re-asserts CLKRUN#; then, the PCH will start the 24 MHz clocks.

### 5.11.7.5 LPC Devices and CLKRUN#

If an LPC device (of any type) needs the 24 MHz clock, such as for LPC DMA or LPC serial interrupt, then it can assert CLKRUN#.

**Note:** LPC devices running DMA or bus master cycles will not need to assert CLKRUN#, since the PCH asserts it on their behalf.

The LDRQ# inputs are ignored by the PCH when the 24-MHz clock is stopped to the LPC devices in order to avoid misinterpreting the request.

## 5.11.8 Sleep States

### 5.11.8.1 Sleep State Overview

The PCH directly supports different sleep states (S1 – S5), which are entered by methods such as setting the SLP\_EN bit or due to a Power Button press. The entry to the Sleep states is based on several assumptions:

- The G3 state cannot be entered using any software mechanism. The G3 state indicates a complete loss of power.

### 5.11.8.2 Initiating Sleep State

Sleep states (S1 – S5) are initiated by:

- Masking interrupts, turning off all bus master enable bits, setting the desired type in the SLP\_TYP field, and then setting the SLP\_EN bit. The hardware then attempts to gracefully put the system into the corresponding Sleep state.
- Pressing the PWRBTN# Signal for more than 4 seconds to cause a Power Button Override event. In this case the transition to the S5 state is less graceful, since there are no dependencies on OPI messages from the processor or on clocks other than the RTC clock.
- Assertion of the THRMTRIP# signal will cause a transition to the S5 state. This can occur when the system is in S0 or S1 state.
- Shutdown by integrated manageability functions (ASF/Intel AMT)
- Internal watchdog timer Timeout events

**Table 5-22. Sleep Types**

Sleep Type	Comment
S1	System lowers the processor's power consumption. No snooping is possible in this state.
S3	The PCH asserts SLP_S3#. The SLP_S3# signal controls the power to non-critical circuits. Power is only retained to devices needed to wake from this sleeping state, as well as to the memory.
S4	The PCH asserts SLP_S3# and SLP_S4#. The SLP_S4# signal shuts off the power to the memory subsystem. Only devices needed to wake from this state should be powered.
S5	The PCH asserts SLP_S3#, SLP_S4# and SLP_S5#.

### 5.11.8.3 Exiting Sleep States

Sleep states (S1 – S5) are exited based on Wake events. The Wake events forces the system to a full on state (S0); although, some non-critical subsystems might still be shut off and have to be brought back manually. For example, the hard disk may be shut off during a sleep state and have to be enabled using a GPIO pin before it can be used.

Upon exit from the PCH-controlled Sleep states, the WAK\_STS bit is set. The possible causes of Wake Events (and their restrictions) are shown in [Table 5-23](#).

**Note:**

(Mobile Only) If the BATLOW# signal is asserted, the PCH does not attempt to wake from an S3 – S5 state, nor will it exit from Deep Sx state, even if the power button is pressed. This prevents the system from waking when the battery power is insufficient to wake the system. Wake events that occur while BATLOW# is asserted are latched by the PCH, and the system wakes after BATLOW# is de-asserted.

Table 5-23. Causes of Wake Events (Sheet 1 of 2)

Cause	How Enabled	Wake from S1, Sx	Wake from Deep Sx	Wake from S1, Sx After Power Loss (Note 1)	Wake from "Reset" Types (Note 2)
RTC Alarm	Set RTC_EN bit in PM1_EN register.	Yes	Yes	Yes	No
Power Button	Always enabled as Wake event.	Yes	Yes	Yes	Yes
GPI[95:0]	GPE0_EN[31:0], GPE0_EN[63:32], GPE0_EN[94:64] registers  <b>Note:</b> GPIOs that are in the core well are not capable of waking the system from sleep states when the core well is not powered.	Yes	No	No	No
GPIO27 (Intel LAN solution uses GPIO27 for PHY Wake)	Set GP27_EN (bit 16) in GPE0[127:96]  <b>Note:</b> GPE0_EN[31:0], bit 27 already covered above and that bit cannot cause a wake from Deep Sx.	Yes	Yes (Note 6)	Yes	Yes
LAN	Will use PME#. Wake enable set with LAN logic.	Yes	No	Yes	No
Intel® High Definition Audio	Event sets PME_B0_STS bit; PM_B0_EN must be enabled. Can not wake from S5 state if it was entered due to power failure or power button override.	Yes	No	Yes	No
Primary PME#	PME_B0_EN bit in GPE0_EN[127:96] register.	Yes	No	Yes	No
Secondary PME#	Set PME_EN bit in GPE0_EN[127:96] register.	Yes	No	Yes	No
PCI_EXP_WAKE#	PCI_EXP_WAKE bit. (Note 3)	Yes	Yes	Yes	No
PCI_EXP PME Message	Must use the PCI Express* WAKE# pin rather than messages for wake from S3, S4, or S5.	Yes (S1 only)	No	Yes (S1 only)	No
SATA	Set PME_EN bit in GPE0_EN[127:96] register. (Note 4)	Yes (S1 only)	No	Yes (S1 only)	No
SMBALERT#	Always enabled as Wake event.	Yes	No	Yes	Yes
SMBus Slave Wake Message (01h)	Wake/SMI# command always enabled as a Wake event.  <b>Note:</b> SMBus Slave Message can wake the system from S1 – S5, as well as from S5 due to Power Button Override.	Yes	No	Yes	Yes
SMBus Host Notify message received	HOST_NOTIFY_WKEN bit SMBus Slave Command register. Reported in the SMB_WAK_STS bit in the GPE0_STS register.	Yes	No	Yes	Yes
Intel® ME Non-Maskable Wake	Always enabled as a wake event.	Yes	No	Yes	Yes

**Table 5-23. Causes of Wake Events (Sheet 2 of 2)**

Cause	How Enabled	Wake from S1, Sx	Wake from Deep Sx	Wake from S1, Sx After Power Loss (Note 1)	Wake from "Reset" Types (Note 2)
Integrated WoL Enable Override	WoL Enable Override bit (in Configuration Space).	Yes	No	Yes	Yes
Wake Alarm Device	WADT_EN in GPE0_EN[127:96]	Yes	Yes	No	No
<b>Notes:</b>					
<ol style="list-style-type: none"> <li>1. This column represents what the PCH would honor as wake events but there may be enabling dependencies on the device side which are not enabled after a power loss.</li> <li>2. Reset Types include: Power Button override, Intel® ME initiated power button override, Intel® ME initiated host partition reset with power down, Intel® ME Watchdog Timer, SMBus unconditional power down, processor thermal trip, PCH catastrophic temperature event.</li> <li>3. When the WAKE# pin is active and the PCI Express* device is enabled to wake the system, the PCH will wake the platform.</li> <li>4. SATA can only trigger a wake event in S1; however, if PME is asserted prior to S3/S4/S5 entry and software does not clear the PME_BO_STS, a wake event would still result.</li> <li>5. Normal Sx wakes caused by USB device connection is routed through PME_B0. The USB_CON_DSX_EN applies only to connection wakes while in Deep Sx</li> <li>6. Only GPE0_EN[127:96], bit 16 (GP27_EN) is capable of generating a wake from Deep Sx. DSX_CFG.GP27_PIN_DSX_EN also needs to be set.</li> </ol>					

It is important to understand that the various GPIOs have different levels of functionality when used as wake events. The GPIOs that reside in the core power well can only generate wake events from sleep states where the core well is powered. Also, only certain GPIOs are "ACPI Compliant," meaning that their Status and Enable bits reside in ACPI I/O space. [Table 5-24](#) summarizes the use of GPIOs as wake events.

**Table 5-24. GPIO Wake Events**

GPIO	Power Well	Wake From	Notes
GPIO[7:0]	Core	S1	ACPI Compliant
GPIO[15:8]	Suspend	S1 – S5	ACPI Compliant

The latency to exit the various Sleep states varies greatly and is heavily dependent on power supply design; so much so that the exit latencies due to the PCH are insignificant.

#### 5.11.8.4 PCI Express\* WAKE# Signal and PME Event Message

PCI Express\* ports can wake the platform from any sleep state (S1, S3, S4, S5, or Deep Sx) using the WAKE# pin. WAKE# is treated as a wake event, but does not cause any bits to go active in the GPE\_STS register.

PCI Express\* ports and the processor have the ability to cause PME using messages. When a PME message is received, the PCH will set the PCI\_EXP\_STS bit.

#### 5.11.8.5 Sx-G3-Sx, Handling Power Failures

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTERG3\_EN bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). There are only two possible events that will wake the system after a power failure.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN\_STS bit is reset. When the PCH exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because V<sub>CC</sub>-standby goes high before RSMRST# goes high) and the PWRBTN\_STS bit is 0.
2. **RTC Alarm:** The RTC\_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN\_STS the RTC\_STS bit is cleared when RSMRST# goes low.

The PCH monitors both PCH\_PWROK and RSMRST# to detect for power failures. If PCH\_PWROK goes low, the PWROK\_FLR bit is set. If RSMRST# goes low, PWR\_FLR is set.

**Note:** Although PME\_EN is in the RTC well, this signal cannot wake the system after a power loss. PME\_EN is cleared by RTCRST#, and PME\_STS is cleared by RSMRST#.

**Table 5-25. Transitions Due to Power Failure**

State at Power Failure	AFTERG3_EN Bit	Transition when Power Returns
S0, S1, S3	1 0	S5 S0
S4	1 0	S4 S0
S5	1 0	S5 S0
Deep Sx	1 0	Deep Sx <sup>1</sup> S0

**Note:**

1. Entry state to Deep Sx is preserved through G3 allowing resume from Deep Sx to take appropriate path (that is, return to S3, S4, or S5).

### 5.11.8.6 Deep Sx

To minimize power consumption while in S3/S4/S5, the PCH supports a lower power, lower featured version of these power states known as Deep Sx. In the Deep Sx state, the Suspend wells are powered off, while the Deep Sx Well (DSW) remains powered. A limited set of wake events are supported by the logic located in the DSW.

The Deep Sx capability and the SUSPWRDNACK pin functionality are mutually exclusive.

#### 5.11.8.6.1 Entry Into Deep Sx

A combination of conditions is required for entry into Deep Sx.

All of the following must be met:

1. Intel® ME in M-Off AND
2. Either a or b as defined below:
  - a. ((DPS3\_EN\_AC AND S3) OR (DPS4\_EN\_AC AND S4) OR (DPS5\_EN\_AC AND S5))
  - b. ((ACPRESENT = 0) AND ((DPS3\_EN\_DC AND S3) OR (DPS4\_EN\_DC AND S4) OR (DPS5\_EN\_DC AND S5)))

**Table 5-26. Supported Deep Sx Policy Configurations**

Configuration	DPS3_EN_DC	DPS3_EN_AC	DPS4_EN_DC	DPS4_EN_AC	DPS5_EN_DC	DPS5_EN_AC
1: Enabled in S5 when on Battery (ACPRESENT = 0)	0	0	0	0	1	0
2: Enabled in S5 (ACPRESENT not considered)	0	0	0	0	1	1
3: Enabled in S4 and S5 when on Battery (ACPRESENT = 0)	0	0	1	0	1	0
4: Enabled in S4 and S5 (ACPRESENT not considered)	0	0	1	1	1	1
5: Enabled in S3, S4 and S5 when on Battery (ACPRESENT = 0)	1	0	1	0	1	0
6: Enabled in S3, S4 and S5 (ACPRESENT not considered)	1	1	1	1	1	1
7: Deep S3/S4/S5 disabled	0	0	0	0	0	0

**Note:** All other configurations are RESERVED.

The PCH also performs a SUSWARN#/SUSACK# handshake to ensure the platform is ready to enter Deep Sx. The PCH asserts SUSWARN# as notification that it is about to enter Deep Sx. Before the PCH proceeds and asserts SLP\_SUS#, the PCH waits for SUSACK# to assert.

#### 5.11.8.6.2 Exit from Deep Sx

While in Deep Sx, the PCH monitors and responds to a limited set of wake events (RTC Alarm, Power Button, WAKE#, and GPIO27). Upon sensing an enabled Deep Sx wake event, the PCH brings up the Suspend well by de-asserting SLP\_SUS#.

**Table 5-27. Deep Sx Wake Events**

Event	Enable
RTC Alarm	RTC_DS_WAKE_DIS (RCBA+3318h:Bit 21)
Power Button	Always enabled
GPIO27	GPE0_EN [127:96] (PMBASE+9Ch:Bit 16)  <b>Note:</b> GPI_IE27 (GPIOBASE+90h:Bit 27) will not generate a wake event from Deep Sx; this bit is only capable of generating an interrupt and wake event from Sx.
PCIe* WAKE# pin	PCIEXP_WAK_DIS
Wake Alarm Device	WADT_EN

**Note:**

ACPRESENT has some behaviors that are different from the other Deep Sx wake events. If the Intel® ME has enabled ACPRESENT as a wake event, then it behaves just like any other Intel® ME Deep Sx wake event. However, even if ACPRESENT wakes are not enabled, if the Host policies indicate that Deep Sx is only supported when on battery, then ACPRESENT going high will cause the PCH to exit Deep Sx. In this case, the Suspend wells gets powered up and the platform remains in S3/M-Off, S4/M-Off, or S5/M-Off. If ACPRESENT subsequently drops (before any Host or Intel® ME wake events are detected), the PCH will re-enter Deep Sx.

## 5.11.9 Event Input Signals and Their Usage

The PCH has various input signals that trigger specific events. This section describes those signals and how they should be used.

### 5.11.9.1 PWRBTN# (Power Button)

The PCH PWRBTN# signal operates as a "Fixed Power Button" as described in the *Advanced Configuration and Power Interface, Version 2.0b*. The PWRBTN# signal has a 16 ms de-bounce on the input. The state transition descriptions are included in [Table 5-28](#).

**Note:** The transitions start as soon as the PWRBTN# is pressed (but after the debounce logic), and does not depend on when the Power Button is released.

**Note:** During the time that the SLP\_S4# signal is stretched for the minimum assertion width (if enabled), the Power Button is not a wake event. Refer to the following Power Button Override Function section for further details.

**Table 5-28. Transitions Due to the Power Button**

Present State	Event	Transition/Action	Comment
S0/Cx	PWRBTN# goes low	SMI or SCI generated (depending on SCI_EN, PWRBTN_EN and GLB_SMI_EN)	Software typically initiates a Sleep state
S1 – S5	PWRBTN# goes low	Wake Event. Transitions to S0 state	Standard wakeup
G3	PWRBTN# pressed	None	No effect since no power Not latched nor detected <b>Note:</b> During G3 exit, PWRBTN# must be asserted at least until SLP_SUS# de-asserts to be registered by PCH as a valid wake event.
S0 – S4	PWRBTN# held low for at least 4 consecutive seconds	Unconditional transition to S5 state and if Deep Sx is enabled and conditions are met per <a href="#">Section 5.11.8.6</a> , the system will then transition to Deep Sx.	No dependence on processor or any other subsystem

#### Power Button Override Function

If PWRBTN# is observed active for at least four consecutive seconds, the state machine should unconditionally transition to the G2/S5 state or Deep Sx, regardless of present state (S0 – S4), even if the PCH\_PWROK is not active. In this case, the transition to the G2/S5 state or Deep Sx does not depend on any particular response from the processor, nor any similar dependency from any other subsystem.

The PWRBTN# status is readable to check if the button is currently being pressed or has been released. The status is taken after the de-bounce, and is readable using the PWRBTN\_LVL bit.

**Note:** The 4-second PWRBTN# assertion should only be used if a system lock-up has occurred. The 4-second timer starts counting when the PCH is in a S0 state. If the PWRBTN# signal is asserted and held active when the system is in a suspend state (S1 – S5), the assertion causes a wake event. Once the system has resumed to the S0 state, the 4-second timer starts.



**Note:** During the time that the SLP\_S4# signal is stretched for the minimum assertion width (if enabled by D31:F0:A4h Bit 3), the Power Button is not a wake event. As a result, it is conceivable that the user will press and continue to hold the Power Button waiting for the system to awake. Since a 4-second press of the Power Button is already defined as an Unconditional Power-down, the power button timer will be forced to inactive while the power-cycle timer is in progress. Once the power-cycle timer has expired, the Power Button wakes the system. Once the minimum SLP\_S4# power-cycle expires, the Power Button must be pressed for another 4 to 5 seconds to create the Override condition to S5.

### Sleep Button

The *Advanced Configuration and Power Interface, Version 2.0b* defines an optional Sleep button. It differs from the power button in that it only is a request to go from S0 to S1 – S4 (not S5). Also, in an S5 state, the Power Button can wake the system, but the Sleep Button cannot.

Although the PCH does not include a specific signal designated as a Sleep Button, one of the GPIO signals can be used to create a “Control Method” Sleep Button. See the *Advanced Configuration and Power Interface, Version 2.0b* for implementation details.

## 5.11.9.2 PME# (PCI Power Management Event)

The PME# signal comes from a PCI Express\* device to request that the system be restarted. The PME# signal can generate an SMI#, SCI, or optionally a Wake event. The event occurs when the PME# signal goes from high to low. No event is caused when it goes from low to high.

There is also an internal PME\_B0 bit. This is separate from the external PME# signal and can cause the same effect.

## 5.11.9.3 SYS\_RESET# Signal

When the SYS\_RESET# pin is detected as active after the 16 ms debounce logic, the PCH attempts to perform a “graceful” reset by entering a host partition reset entry sequence.

Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the SYS\_RESET# input remains asserted or not. It cannot occur again until SYS\_RESET# has been detected inactive after the debounce logic, and the system is back to a full S0 state with PLTRST# inactive.

**Note:** If bit 3 of the CF9h I/O register is set, then SYS\_RESET# will result in a full power-cycle reset.

## 5.11.9.4 THRMTRIP# Signal

If THRMTRIP# goes active, the processor is indicating an overheat condition, and the PCH immediately transitions to an S5 state, driving SLP\_S3#, SLP\_S4#, SLP\_S5# low, and setting the CTS bit. The transition looks like a power button override.

When a THRMTRIP# event occurs, the PCH will power down immediately without following the normal S0 -> S5 path. The PCH will immediately drive SLP\_S3#, SLP\_S4#, and SLP\_S5# low after sampling THRMTRIP# active.

If the processor is running extremely hot and is heating up, it is possible (although very unlikely) that components around it, such as the PCH, are no longer executing cycles properly. Therefore, if THRMTRIP# goes active, and the PCH is relying on state machine logic to perform the power down, the state machine may not be working, and the system will not power down.

The PCH provides filtering for short low glitches on the THRMTRIP# signal in order to prevent erroneous system shut downs from noise. Glitches shorter than 25 nsec are ignored.

During boot, THRMTRIP# is ignored until SLP\_S3#, PCH\_PWROK, and PLTRST# are all '1'. During entry into a powered-down state (due to S3, S4, S5 entry, power-cycle reset, and so on) THRMTRIP# is ignored until either SLP\_S3# = 0, or PCH\_PWROK = 0, or SYS\_PWROK = 0.

**Note:** A thermal trip event will:

- Clear the PWRBTN\_STS bit
- Clear all the GPE0\_EN register bits
- Clear the SMB\_WAK\_STS bit only if SMB\_SAK\_STS was set due to SMBus slave receiving message and not set due to SMBAlert

### 5.11.10 ALT Access Mode

Before entering a low power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the PCH implements an ALT access mode.

If the ALT access mode is entered and exited after reading the registers of the PCH timer (8254), the timer starts counting faster (13.5 ms). The following steps listed below can cause problems:

1. BIOS enters ALT access mode for reading the PCH timer related registers.
2. BIOS exits ALT access mode.
3. BIOS continues through the execution of other needed steps and passes control to the operating system.

After getting control in step #3, if the operating system does not reprogram the system timer again, the timer ticks may be happening faster than expected. For example, Microsoft\* MS-DOS and its associated software assume that the system timer is running at 54.6 ms and as a result the Timeouts in the software may be happening faster than expected.

Operating systems (such as Microsoft\* Windows\* 98 and Windows\* 2000) reprogram the system timer and, therefore, do not encounter this problem.

For other operating systems (such as Microsoft\* MS-DOS) the BIOS should restore the timer back to 54.6 ms before passing control to the operating system. If the BIOS is entering ALT access mode before entering the suspend state, it is not necessary to restore the timer contents after the exit from ALT access mode.

### 5.11.10.1 Write Only Registers with Read Paths in ALT Access Mode

The registers described in Table 5-29 have read paths in ALT access mode. The access number field in the table indicates which register will be returned per access to that port.

**Table 5-29. Write Only Registers with Read Paths in ALT Access Mode (Sheet 1 of 2)**

Restore Data				Restore Data			
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data
00h	2	1	DMA Chan 0 base address low byte	40h	7	1	Timer Counter 0 status, bits [5:0]
		2	DMA Chan 0 base address high byte			2	Timer Counter 0 base count low byte
01h	2	1	DMA Chan 0 base count low byte			3	Timer Counter 0 base count high byte
		2	DMA Chan 0 base count high byte			4	Timer Counter 1 base count low byte
02h	2	1	DMA Chan 1 base address low byte			5	Timer Counter 1 base count high byte
		2	DMA Chan 1 base address high byte			6	Timer Counter 2 base count low byte
03h	2	1	DMA Chan 1 base count low byte			7	Timer Counter 2 base count high byte
		2	DMA Chan 1 base count high byte	41h	1		Timer Counter 1 status, bits [5:0]
04h	2	1	DMA Chan 2 base address low byte	42h	1		Timer Counter 2 status, bits [5:0]
		2	DMA Chan 2 base address high byte	70h	1		Bit 7 = NMI Enable, Bits [6:0] = RTC Address
05h	2	1	DMA Chan 2 base count low byte	C4h	2	1	DMA Chan 5 base address low byte
		2	DMA Chan 2 base count high byte			2	DMA Chan 5 base address high byte
06h	2	1	DMA Chan 3 base address low byte	C6h	2	1	DMA Chan 5 base count low byte
		2	DMA Chan 3 base address high byte			2	DMA Chan 5 base count high byte
07h	2	1	DMA Chan 3 base count low byte	C8h	2	1	DMA Chan 6 base address low byte
		2	DMA Chan 3 base count high byte			2	DMA Chan 6 base address high byte

**Table 5-29. Write Only Registers with Read Paths in ALT Access Mode (Sheet 2 of 2)**

Restore Data				Restore Data				
I/O Addr	# of Rds	Access	Data	I/O Addr	# of Rds	Access	Data	
08h	6	1	DMA Chan 0-3 Command <sup>2</sup>	CAh	2	1	DMA Chan 6 base count low byte	
		2	DMA Chan 0-3 Request			2	DMA Chan 6 base count high byte	
		3	DMA Chan 0 Mode: Bits(1:0) = 00	CCh	2	1	DMA Chan 7 base address low byte	
		4	DMA Chan 1 Mode: Bits(1:0) = 01			2	DMA Chan 7 base address high byte	
		5	DMA Chan 2 Mode: Bits(1:0) = 10	CEh	2	1	DMA Chan 7 base count low byte	
		6	DMA Chan 3 Mode: Bits(1:0) = 11.			2	DMA Chan 7 base count high byte	
20h	12	1	PIC ICW2 of Master controller	D0h	6	1	DMA Chan 4-7 Command <sup>2</sup>	
		2	PIC ICW3 of Master controller			2	DMA Chan 4-7 Request	
		3	PIC ICW4 of Master controller			3	DMA Chan 4 Mode: Bits(1:0) = 00	
		4	PIC OCW1 of Master controller <sup>1</sup>			4	DMA Chan 5 Mode: Bits(1:0) = 01	
		5	PIC OCW2 of Master controller			5	DMA Chan 6 Mode: Bits(1:0) = 10	
		6	PIC OCW3 of Master controller			6	DMA Chan 7 Mode: Bits(1:0) = 11.	
		7	PIC ICW2 of Slave controller					
		8	PIC ICW3 of Slave controller					
		9	PIC ICW4 of Slave controller					
		10	PIC OCW1 of Slave controller <sup>1</sup>					
		11	PIC OCW2 of Slave controller					
		12	PIC OCW3 of Slave controller					

**Notes:**

1. The OCW1 register must be read before entering ALT access mode.
2. Bits 5, 3, 1, and 0 return 0.



### 5.11.10.2 PIC Reserved Bits

Many bits within the PIC are reserved, and must have certain values written in order for the PIC to operate properly. Therefore, there is no need to return these values in ALT access mode. When reading PIC registers from 20h and A0h, the reserved bits shall return the values listed in [Table 5-30](#).

**Table 5-30. PIC Reserved Bits Return Values**

PIC Reserved Bits	Value Returned
ICW2(2:0)	000
ICW4(7:5)	000
ICW4(3:2)	00
ICW4(0)	0
OCW2(4:3)	00
OCW3(7)	0
OCW3(5)	Reflects bit 6
OCW3(4:3)	01

### 5.11.10.3 Read Only Registers with Write Paths in ALT Access Mode

The registers described in [Table 5-31](#) have write paths to them in ALT access mode. Software restores these values after returning from a powered down state. These registers must be handled special by software. When in normal mode, writing to the base address/count register also writes to the current address/count register. Therefore, the base address/count must be written first, then the part is put into ALT access mode and the current address/count register is written.

**Table 5-31. Register Write Accesses in ALT Access Mode**

I/O Address	Register Write Value
08h	DMA Status Register for Channels 0–3
D0h	DMA Status Register for Channels 4–7

## 5.11.11 System Power Supplies, Planes, and Signals

### 5.11.11.1 Power Plane Control with SLP\_S3#, SLP\_S4#, SLP\_S5#, SLP\_A# and SLP\_LAN#

The SLP\_S3# output signal can be used to cut power to the system core supply, since it only goes active for the Suspend-to-RAM state (typically mapped to ACPI S3). Power must be maintained to the PCH suspend well, and to any other circuits that need to generate Wake signals from the Suspend-to-RAM state. During S3 (Suspend-to-RAM) all signals attached to powered down plans will be tri-stated or driven low, unless they are pulled using a pull-up resistor.

Cutting power to the core may be done using the power supply, or by external FETs on the motherboard.

The SLP\_S4# or SLP\_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done using the power supply, or by external FETs on the motherboard.

The SLP\_S4# output signal is used to remove power to additional subsystems that are powered during SLP\_S3#.

SLP\_S5# output signal can be used to cut power to the system core supply, as well as power to the system memory, since the context of the system is saved on the disk. Cutting power to the memory may be done using the power supply, or by external FETs on the motherboard.

SLP\_A# output signal can be used to cut power to the Intel® Management Engine and SPI flash on a platform that supports the M3 state (for example, certain power policies in Intel AMT).

SLP\_LAN# output signal can be used to cut power to the external Intel 82579 GbE PHY device.

#### 5.11.11.2 SLP\_S4# and Suspend-to-RAM Sequencing

The system memory suspend voltage regulator is controlled by the Glue logic. The SLP\_S4# signal should be used to remove power to system memory rather than the SLP\_S5# signal. The SLP\_S4# logic in the PCH provides a mechanism to fully cycle the power to the DRAM and/or detect if the power is not cycled for a minimum time.

**Note:** To use the minimum DRAM power-down feature that is enabled by the SLP\_S4# Assertion Stretch Enable bit (D31:F0:A4h Bit 3), the DRAM power must be controlled by the SLP\_S4# signal.

#### 5.11.11.3 PCH\_PWROK Signal

When asserted, PCH\_PWROK is an indication to the PCH that its core well power rails are powered and stable. PCH\_PWROK can be driven asynchronously. When PCH\_PWROK is low, the PCH asynchronously asserts PLTRST#. PCH\_PWROK must not glitch, even if RSMRST# is low.

**Note:** SYS\_RESET# is recommended for implementing the system reset button. This saves external logic that is needed if the PCH\_PWROK input is used. Additionally, it allows for better handling of the SMBus and processor resets and avoids improperly reporting power failures.

#### 5.11.11.4 BATLOW# (Battery Low)

The BATLOW# input can inhibit waking from S3, S4, S5, and Deep Sx states if there is not sufficient power. It also causes an SMI if the system is already in an S0 state.

#### 5.11.11.5 SLP\_LAN# Pin Behavior

The PCH controls the voltage rails into the external LAN PHY using the SLP\_LAN# pin.

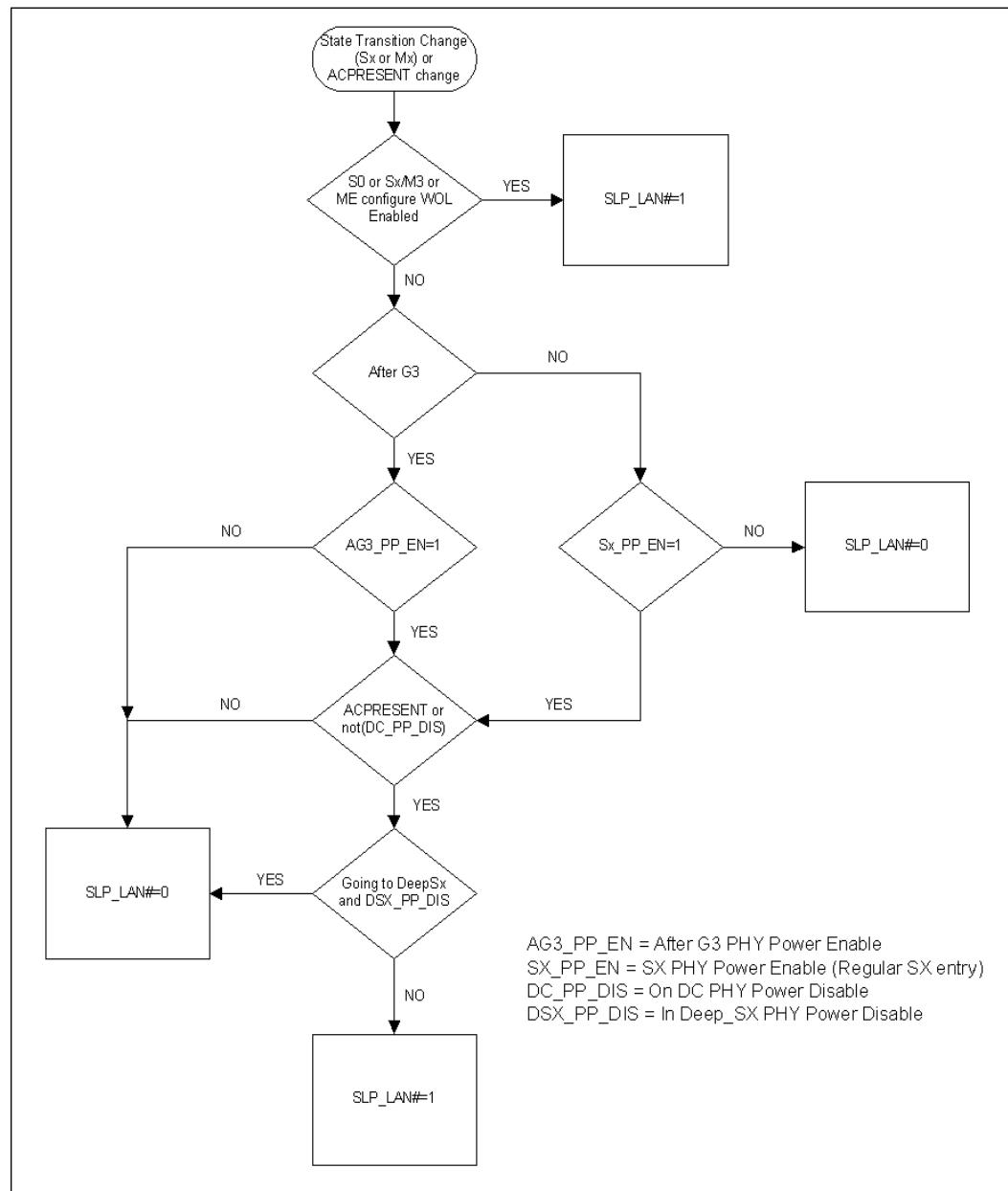
- The LAN PHY is always powered when the Host and Intel® ME systems are running.
  - SLP\_LAN#='1' whenever SLP\_S3#='1' or SLP\_A#='1'.
- If the LAN PHY is required by Intel® ME in Sx/M-Off or Deep Sx, Intel® ME must configure SLP\_LAN#='1' irrespective of the power source and the destination power state. Intel® ME must be powered at least once after G3 to configure this.
- If the LAN PHY is required after a G3 transition, the host BIOS must set AG3\_PP\_EN (B0:D31:F0:A2h bit 12).
- If the LAN PHY is required in Sx/M-Off, the host BIOS must set SX\_PP\_EN (B0:D31:F0:A2h bit 11).

- If the LAN PHY is required in Deep Sx, the host BIOS must keep DSX\_PP\_DIS (B0:D31:F0:A2h bit 13) cleared.
- If the LAN PHY is not required if the source of power is battery, the host BIOS must set DC\_PP\_DIS (B0:D31:F0:A2h bit 14).

**Note:** Intel® ME configuration of SLP\_LAN# in Sx/M-Off and Deep Sx is dependant on Intel® ME power policy configuration.

Figure 5-5 (flow chart) shows how a decision is made to drive SLP\_LAN# every time its policy needs to be evaluated.

**Figure 5-5. Conceptual Diagram of SLP\_LAN#**



### 5.11.11.6 SLP\_WLAN# Pin Behavior

The PCH controls the voltage rails into the external wireless LAN PHY using the SLP\_WLAN# pin.

- The wireless LAN PHY is always powered when the Host is running.
  - SLP\_WLAN#=‘1’ whenever SLP\_S3#=‘1’.
- If Wake on Wireless LAN (WoWLAN) is required from S3/S4/S5 states, the host BIOS must set CIR33E0.HOST\_WLAN\_PP\_EN (RCBA+33E0h bit 17).
- If Wake on Wireless LAN (WoWLAN) is desired from Deep Sx, CIR33E0.HOST\_WLAN\_PP\_EN.DSX\_WLAN\_PP\_EN must be set.
- If Intel® ME has access to the Wireless LAN device
  - The Wireless LAN device must always be powered as long as Intel® ME is powered. SLP\_WLAN#=‘1’ whenever SLP\_A#=‘1’.
  - If Wake on Wireless LAN (WoWLAN) is required from M-Off state, Intel® ME will configure SLP\_WLAN#=‘1’ in Sx/M-Off.

Intel® ME configuration of SLP\_WLAN# in Sx/M-Off is dependant on Intel® ME power policy configuration.

### 5.11.11.7 SUSPWRDNACK/SUSWARN#/GPIO30 Steady State Pin Behavior

Table 5-32 summarizes SUSPWRDNACK/SUSWARN#/GPIO30 Pin Behavior.

**Table 5-32. SUSPWRDNACK/SUSWARN#/GPIO30 Pin Behavior**

Pin	Deep Sx (Supported/ Not- Supported)	GPIO30 Input/ Output (Determine by GP_IO_SEL bit)	Pin Value in S0	Pin Value in Sx/M-Off	Pin Value in Sx/M3	Pin Value in Deep Sx
SUSPWRDNACK	Not Supported	Native	0	Depends on Intel® ME power package and power source (Note 1)	0	Off
SUSWARN#	Supported	Native	1	1 (Note 2)	1	Off
GPIO30	Don't Care	IN	High-Z	High-Z	High-Z	Off
	Don't Care	OUT	Depends on GPIO30 output data value	Depends on GPIO30 output data value	Depends on GPIO30 output data value	Off

**Notes:**

1. PCH will drive SPDA pin based on ME power policy configuration.
2. If entering Deep Sx, pin will assert and become undriven (“Off”) when suspend well drops upon Deep Sx entry.

**Table 5-33. SUSPWRDNACK During Reset**

Reset Type (Note)	SPDA Value
Power-cycle Reset	0
Global Reset	0
Straight to S5	PCH initially drive ‘0’ and then drive per ME power policy configuration.
<b>Note:</b> See Table 5-34.	



### 5.11.11.8 RTCRST# and SRTCST#

RTCRST# is used to reset PCH registers in the RTC Well to their default value. If a jumper is used on this pin, it should only be pulled low when system is in the G3 state and then replaced to the default jumper position. Upon booting, BIOS should recognize that RTCRST# was asserted and clear internal PCH registers accordingly. It is imperative that this signal not be pulled low in the S0 to S5 states.

SRTCST# is used to reset portions of the Intel® Management Engine and should not be connected to a jumper or button on the platform. The only time this signal gets asserted (driven low in combination with RTCRST#) should be when the coin cell battery is removed or not installed and the platform is in the G3 state. Pulling this signal low independently (without RTCRST# also being driven low) may cause the platform to enter an indeterminate state. Similar to RTCRST#, it is imperative that SRTCST# not be pulled low in the S0 to S5 states.

See Figure 2-2 which demonstrates the proper circuit connection of these pins.

### 5.11.12 Legacy Power Management Theory of Operation

Instead of relying on ACPI software, legacy power management uses BIOS and various hardware mechanisms. The scheme relies on the concept of detecting when individual subsystems are idle, detecting when the whole system is idle, and detecting when accesses are attempted to idle subsystems.

However, the operating system is assumed to be at least APM enabled. Without APM calls, there is no quick way to know when the system is idle between keystrokes. The PCH does not support burst modes.

#### 5.11.12.1 Mobile APM Power Management

In mobile systems, there are additional requirements associated with device power management. To handle this, the PCH has specific SMI traps available. The following algorithm is used:

1. The periodic SMI timer checks if a device is idle for the required time. If so, it puts the device into a low-power state and sets the associated SMI trap.
2. When software (not the SMI handler) attempts to access the device, a trap occurs (the cycle does not really go to the device and an SMI is generated).
3. The SMI handler turns on the device and turns off the trap.
4. The SMI handler exits with an I/O restart. This allows the original software to continue.

### 5.11.13 Reset Behavior

When a reset is triggered, the PCH will send a warning message to the processor to allow the processor to attempt to complete any outstanding memory cycles and put memory into a safe state before the platform is reset. When the processor is ready, it will send an acknowledge message to the PCH. Once the message is received, the PCH asserts PLTRST#.

The PCH does not require an acknowledge message from the processor to trigger PLTRST#. A global reset will occur after 4 seconds if an acknowledge from the processor is not received.

When the PCH causes a reset by asserting PLTRST#, its output signals will go to their reset states as defined in [Chapter 3](#).

A reset in which the host platform is reset and PLTRST# is asserted is called a Host Reset or Host Partition Reset. Depending on the trigger, a host reset may also result in power cycling; see [Table 5-34](#) for details. If a host reset is triggered and the PCH times out before receiving an acknowledge message from the processor, a Global Reset with power-cycle will occur.

A reset in which the host and Intel® ME partitions of the platform are reset is called a Global Reset. During a Global Reset, all PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. Intel® ME and Host power back up after the power-cycle period.

Straight to S5 is another reset type where all power wells that are controlled by the SLP\_S3#, SLP\_S4#, and SLP\_A# pins, as well as SLP\_S5# and SLP\_LAN# (if pins are not configured as GPIOs), are turned off. All PCH functionality is reset except RTC Power Well backed information and Suspend well status, configuration, and functional logic for controlling and reporting the reset. The host stays there until a valid wake event occurs.

[Table 5-34](#) shows the various reset triggers.

**Table 5-34. Causes of Host and Global Resets (Sheet 1 of 2)**

Trigger	Host Reset Without Power-cycle <sup>1</sup>	Host Reset With Power-cycle <sup>2</sup>	Global Reset With Power-cycle <sup>3</sup>	Straight to S5 <sup>6</sup> (Host Stays There)
Write of 0Eh to CF9h (RST_CNT Register)	No	Yes	No (Note 4)	
Write of 06h to CF9h (RST_CNT Register)	Yes	No	No (Note 4)	
SYS_RESET# Asserted and CF9h (RST_CNT Register) Bit 3 = 0	Yes	No	No (Note 4)	
SYS_RESET# Asserted and CF9h (RST_CNT Register) Bit 3 = 1	No	Yes	No (Note 4)	
SMBus Slave Message received for Reset with Power-Cycle	No	Yes	No (Note 4)	
SMBus Slave Message received for Reset without Power-Cycle	Yes	No	No (Note 4)	
SMBus Slave Message received for unconditional Power Down	No	No	No	Yes
TCO Watchdog Timer reaches zero two times	Yes	No	No (Note 4)	
Power Failure: PCH_PWROK signal goes inactive in S0/S1 or DPWROK drops	No	No	Yes	
SYS_PWROK Failure: SYS_PWROK signal goes inactive in S0/S1	No	No	Yes	
Processor Thermal Trip (THRMTRIP#) causes transition to S5 and reset asserts	No	No	No	Yes
PCH internal thermal sensors signals a catastrophic temperature condition	No	No	No	Yes
Power Button 4 second override causes transition to S5 and reset asserts	No	No	No	Yes
Special shutdown cycle from processor causes CF9h-like PLTRST# and CF9h (RST_CNT Register) Bit 3 = 1	No	Yes	No (Note 4)	

**Table 5-34. Causes of Host and Global Resets (Sheet 2 of 2)**

Trigger	Host Reset Without Power-cycle <sup>1</sup>	Host Reset With Power-cycle <sup>2</sup>	Global Reset With Power-cycle <sup>3</sup>	Straight to S5 <sup>6</sup> (Host Stays There)
Special shutdown cycle from processor causes CF9h-like PLTRST# and CF9h (RST_CNT Register) Bit 3 = 0	Yes	No	No (Note 4)	
Intel® Management Engine Triggered Host Reset without Power-Cycle	Yes	No	No (Note 4)	
Intel® Management Engine Triggered Host Reset with Power-Cycle	No	Yes	No (Note 4)	
Intel® Management Engine Triggered Power Button Override	No	No	No	Yes
Intel® Management Engine Watchdog Timer Timeout	No	No	No	Yes
Intel® Management Engine Triggered Global Reset	No	No	Yes	
Intel® Management Engine Triggered Host Reset with power down (host stays there)	No	Yes (Note 5)	No (Note 4)	
PLTRST# Entry Timeout (Note 7)	No	No	Yes	
PROCPWRGD Stuck Low	No	No	Yes	
Power Management Watchdog Timer	No	No	No	Yes
Intel® Management Engine Hardware Uncorrectable Error	No	No	No	Yes
<b>Notes:</b>				
<ol style="list-style-type: none"> <li>1. The PCH drops this type of reset request if received while the system is in S3/S4/S5.</li> <li>2. PCH does not drop this type of reset request if received while system is in a software-entered S3/S4/S5 state. However, the PCH will perform the reset without executing the RESET_WARN protocol in these states.</li> <li>3. The PCH does not send warning message to processor, reset occurs without delay.</li> <li>4. Trigger will result in Global Reset with Power-Cycle if the acknowledge message is not received by the PCH.</li> <li>5. The PCH waits for enabled wake event to complete reset.</li> <li>6. Upon entry to S5, if Deep Sx is enabled and conditions are met per <a href="#">Section 5.11.8.6</a>, the system will transition to Deep Sx.</li> <li>7. PLTRST# Entry Timeout is automatically initiated if the hardware detects that the PLTRST# sequence has not been completed within 4 seconds of being started.</li> </ol>				

### 5.11.14 Windows\* InstantGo Power Save Mode (Windows\* InstantGo PSM)

The PCH supports a new feature, 0.95 V Windows\* InstantGo Power Save Mode (Windows\* InstantGo PSM). During S0 when the processor is in its lowest idle power state and SLP\_S0# is asserted, all of the processor's 1.05V rails (including core, suspend and active sleep well) can be lowered to 0.95 V voltage level. This capability is already available on the platforms using Power Management Integrated Circuit (PMIC).

**Note:** This feature is only supported on platforms that are configured for External Suspend VR Mode. This means that INTVRMEN strap is pulled down and DCPSUS1, DCPSUS2, DCPSUS3, and DCPSUS4 are powered from an external power source.

## 5.12 System Management (D31:F0)

The PCH provides various functions to make a system easier to manage and to lower the Total Cost of Ownership (TCO) of the system. Features and functions can be augmented using external A/D converters and GPIO, as well as an external microcontroller.

The following features and functions are supported by the PCH:

- Processor present detection
  - Detects if processor fails to fetch the first instruction after reset
- Various Error detection (such as ECC Errors) indicated by host controller
  - Can generate SMI#, SCI, SERR, NMI, or TCO interrupt
- Intruder Detect input
  - Can generate TCO interrupt or SMI# when the system cover is removed
  - INTRUDER# allowed to go active in any power state, including G3
- Detection of bad BIOS Flash (FWH or Flash on SPI) programming
  - Detects if data on first read is FFh (indicates that BIOS flash is not programmed)

**Note:** Voltage ID from the processor can be read using GPI signals.

### 5.12.1 Theory of Operation

The System Management functions are designed to allow the system to diagnose failing subsystems. The intent of this logic is that some of the system management functionality can be provided without the aid of an external microcontroller.

#### 5.12.1.1 Detecting a System Lockup

When the processor is reset, it is expected to fetch its first instruction. If the processor fails to fetch the first instruction after reset, the TCO timer times out twice and the PCH asserts PLTRST#.

#### 5.12.1.2 Handling an Intruder

The PCH has an input signal, INTRUDER#, that can be attached to a switch that is activated by the system's case being open. This input has a two RTC clock debounce. If INTRUDER# goes active (after the debouncer), this will set the INTRD\_DET bit in the TCO2\_STS register. The INTRD\_SEL bits in the TCO\_CNT register can enable the PCH to cause an SMI# or interrupt. The BIOS or interrupt handler can then cause a transition to the S5 state by writing to the SLP\_EN bit.

The software can also directly read the status of the INTRUDER# signal (high or low) by clearing and then reading the INTRD\_DET bit.

If the INTRUDER# signal goes inactive some point after the INTRD\_DET bit is written as a 1, then the INTRD\_DET bit will go to a 0 when INTRUDER# input signal goes inactive.

**Note:** This is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.



**Note:** The INTRD\_DET bit resides in the PCH's RTC well, and is set and cleared synchronously with the RTC clock. Thus, when software attempts to clear INTRD\_DET (by writing a 1 to the bit location), there may be as much as two RTC clocks (about 65  $\mu$ s) delay before the bit is actually cleared. Also, the INTRUDER# signal should be asserted for a minimum of 1 ms to ensure that the INTRD\_DET bit will be set.

**Note:** If the INTRUDER# signal is still active when software attempts to clear the INTRD\_DET bit, the bit remains set and the SMI is generated again immediately. The SMI handler can clear the INTRD\_SEL bits to avoid further SMIs. However, if the INTRUDER# signal goes inactive and then active again, there will not be further SMIs, since the INTRD\_SEL bits would select that no SMI# be generated.

### 5.12.1.3 Detecting Improper Flash Programming

The PCH can detect the case where the BIOS flash is not programmed. This results in the first instruction fetched to have a value of FFh. If this occurs, the PCH sets the BAD\_BIOS bit. The BIOS flash may reside in FWH or flash on the SPI bus.

### 5.12.1.4 Heartbeat and Event Reporting Using SMLink/SMBus

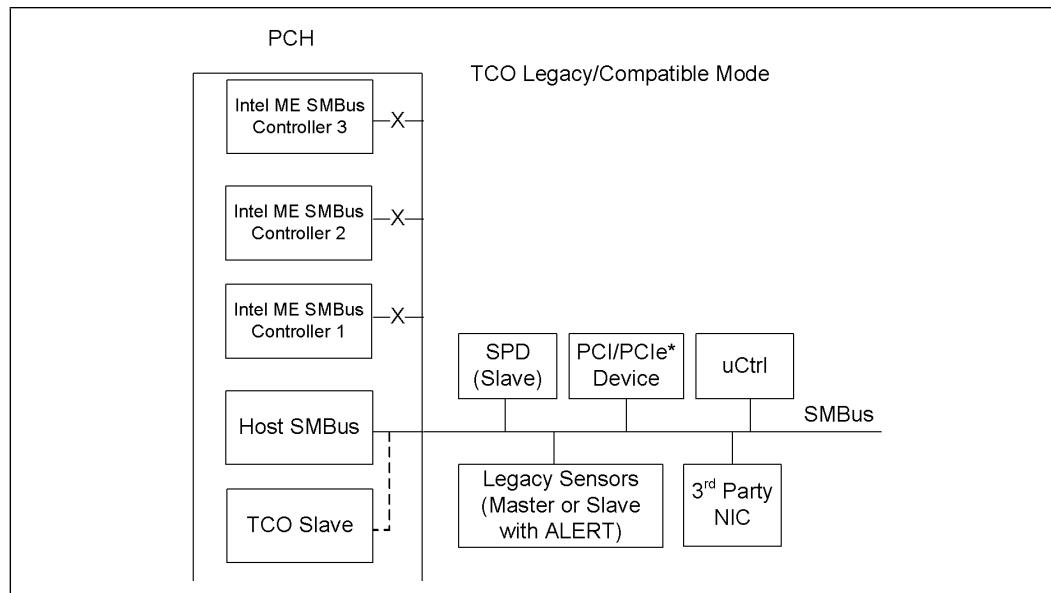
Heartbeat and event reporting using SMLink/SMBus is no longer supported. The Intel® AMT logic in the PCH can be programmed to generate an interrupt to the Intel® Management Engine when an event occurs. The Intel® Management Engine will poll the TCO registers to gather appropriate bits to send the event message to the Gigabit Ethernet controller, if Intel® Management Engine is programmed to do so.

## 5.12.2 Total Cost of Ownership (TCO) Modes

### 5.12.2.1 TCO Legacy/Compatible Mode

In TCO Legacy/Compatible mode, only the host SMBus is utilized. The TCO Slave is connected to the host SMBus internally by default. In this mode, the Intel® Management Engine SMBus controllers are not used and should be disabled by soft strap.

**Figure 5-6. Total Cost of Ownership (TCO) Legacy/Compatible Mode SMBus Configuration**



In TCO Legacy/Compatible mode the PCH can function directly with an external LAN controller or equivalent external LAN controller to report messages to a network management console without the aid of the system processor. This is crucial in cases where the processor is malfunctioning or cannot function due to being in a low-power state. [Table 5-35](#) includes a list of events that will report messages to the network management console.

**Table 5-35. Event Transitions that Cause Messages**

Event	Assertion?	De-assertion?	Comments
INTRUDER# pin	Yes	No	Must be in "S1 or hung S0" state
THRM# pin	Yes	Yes	Must be in "S1 or hung S0" state. <b>Note:</b> The THRM# pin is isolated when the core power is off, thus preventing this event in S3 – S5.
Watchdog Timer Expired	Yes	No (N/A)	"S1 or hung S0" state entered
GPIO11/SMBALERT# pin	Yes	Yes	Must be in "S1 or hung S0" state
BATLOW#	Yes	Yes	Must be in "S1 or hung S0" state
<b>Note:</b> The GPIO11/SMBALERT# pin will trigger an event message (when enabled by the GPIO11_ALERT_DISABLE bit), regardless of whether it is configured as a GPI or not.			

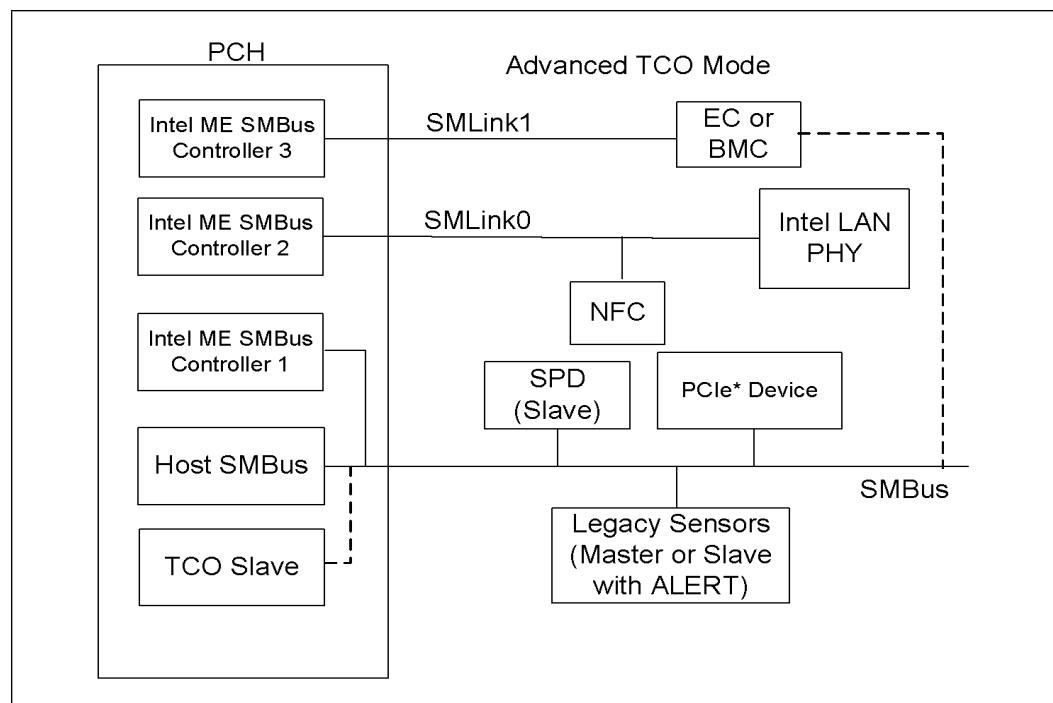
### 5.12.2.2 Advanced TCO Mode

The PCH supports the Advanced TCO mode in which SMLink0 and SMLink1 are used in addition to the host SMBus. See [Figure 5-7](#) for more details. In this mode, the Intel® ME SMBus controllers must be enabled by a soft strap in the flash descriptor.

SMLink0 is dedicated to integrated LAN and NFC use. When an Intel LAN PHY is connected to SMLink0, a soft strap must be set to indicate that the PHY is connected to SMLink0. The interface will be running at the frequency of up to 1 MHz depending on different factors such as board routing or bus loading when the Fast Mode is enabled using a soft strap.

SMLink1 is dedicated to Embedded Controller (EC) or Baseboard Management Controller (BMC) use. In the case where a BMC is connected to SMLink1, the BMC communicates with the Intel® Management Engine through the Intel® ME SMBus connected to SMLink1. The host and TCO slave communicate with BMC through SMBus.

**Figure 5-7. Advanced Total Cost of Ownership (TCO) Mode**



## 5.13 General Purpose I/O (D31:F0)

The PCH contains up to 94 General Purpose Input/Output (GPIO) signals. Each GPIO can be configured as an input or output signal. The number of inputs and outputs varies depending on the configuration. Following is a brief summary of GPIO features.

- Capability to mask Suspend well GPIOs from CF9h events (configured using GP\_RST\_SEL registers)
- Added capability to program GPIO prior to switching to output

### 5.13.1 Power Wells

Some GPIOs exist in the suspend power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some PCH GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PCH\_PWROK low) or a Power Button Override event results in the PCH driving a pin to a logic 1 to another device that is powered down.

### 5.13.2 SMI# SCI and NMI Routing

The routing bits for GPIO[47:32] allow an input to be routed to SMI#, SCI, NMI or none of these.

**Note:** A bit can be routed to either an SMI# or an SCI, but not both.

### 5.13.3 Triggering

GPIO[94:0] have "sticky" bits on the input. Refer to the GPE0\_STS register and the ALT\_GPI\_SMI\_STS register. As long as the signal goes active for at least 2 clock cycles, the PCH keeps the sticky status bit active. The active level can be selected in the GP\_INV register. This does not apply to GPI\_NMI\_STS residing in GPIO I/O space.

If the system is in an S0 or an S1 state, the GPI inputs are sampled at 24 MHz; thus, the signal only needs to be active for about 83.33 ns to be latched. In the S3 – S5 states, the GPI inputs are sampled at 32.768 KHz, and thus must be active for at least 61 microseconds to be latched.

**Note:** GPIOs that are in the core well are not capable of waking the system from sleep states where the core well is not powered.

If the input signal is still active when the latch is cleared, it will again be set. Another edge trigger is not required. This makes these signals "level" triggered inputs.

### 5.13.4 GPIO Registers Lockdown

The following GPIO registers are locked down when the GPIO Lockdown Enable (GLE) bit is set. The GLE bit resides in D31:F0:GPIO Control (GC) register.

- Offset 00h: GPIO\_OWN[31:0]
- Offset 04h: GPIO\_OWN[63:32]
- Offset 08h: GPIO\_OWN[94:64]
- Offset 28h: GPI\_NMI\_EN[15:0]
- Offset 60h: GP\_RST\_SEL[31:0]
- Offset 64h: GP\_RST\_SEL2[63:32]
- Offset 68h: GP\_RST\_SEL3[95:64]

**Note:** All other GPIO registers not listed here are not to be locked by GLE.

Once these registers are locked down, they become read-only registers and any software writes to these registers will have no effect. To unlock the registers, the GPIO Lockdown Enable (GLE) bit is required to be cleared to '0'. When the GLE bit changes from a '1' to a '0', a System Management Interrupt (SMI#) is generated, if enabled. Once the GPIO\_UNLOCK\_SMI bit is set, it can not be changed until a PLTRST# occurs. This ensures that only BIOS can change the GPIO configuration. If the GLE bit is cleared by unauthorized software, BIOS will set the GLE bit again when the SMI# is triggered and these registers will continue to be locked down.

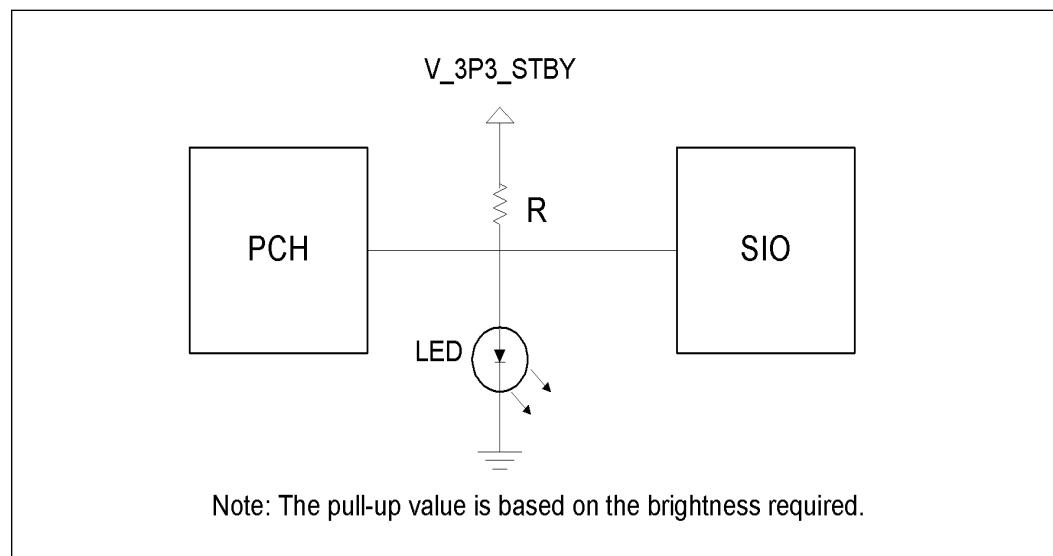
### 5.13.5 Serial POST Codes Over GPIO

The PCH adds the extended capability allowing system software to serialize POST or other messages on GPIO. This capability negates the requirement for dedicated diagnostic LEDs on the platform.

#### 5.13.5.1 Theory of Operation

For the PCH generation POST code serialization logic will be shared with GPIO. These GPIOs will likely be shared with LED control offered by the Super I/O (SIO) component. Figure 5-8 shows a likely configuration.

**Figure 5-8. Serial POST Over GPIO Reference Circuit**



The anticipated usage model is that either the PCH or the SIO can drive a pin low to turn off an LED. In the case of the power LED, the SIO would normally leave its corresponding pin in a high-Z state to allow the LED to turn on. In this state, the PCH can blink the LED by driving its corresponding pin low and subsequently tri-stating the buffer. The I/O buffer should not drive a '1' when configured for this functionality and should be capable of sinking 24mA of current.

An external optical sensing device can detect the on/off state of the LED. By externally post-processing the information from the optical device, the serial bit stream can be recovered. The hardware will supply a 'sync' byte before the actual data transmission to allow external detection of the transmit frequency. The frequency of transmission should be limited to 1 transition every 1  $\mu$ s to ensure the detector can reliably sample

the on/off state of the LED. To allow flexibility in pull-up resistor values for power optimization, the frequency of the transmission is programmable using the DRS field in the GP\_GB\_CMDSTS register.

The serial bit stream is Manchester encoded. This choice of transmission ensures that a transition will be seen on every clock. The 1 or 0 data is based on the transmission happening during the high or low phase of the clock.

As the clock will be encoded within the data stream, hardware must ensure that the Z-0 and 0-Z transitions are glitch-free. Driving the pin directly from a flip-flop or through glitch-free logic are possible methods to meet the glitch-free requirement.

A simplified hardware/software register interface provides control and status information to track the activity of this block. Software enabling the serial blink capability should implement an algorithm referenced below to send the serialized message on the enabled GPIO.

1. Read the Go/Busy status bit in the GP\_GB\_CMDSTS register and verify it is cleared. This will ensure that the GPIO is idled and a previously requested message is still not in progress.
2. Write the data to serialize into the GP\_GB\_DATA register.
3. Write the DLS and DRS values into the GP\_GB\_CMDSTS register and set the Go bit. This may be accomplished using a single write.

[Figure 5-8](#) shows the LEDs being powered from the suspend supply. By providing a generic capability that can be used both in the main and the suspend power planes, maximum flexibility can be achieved. A key point to make is that the PCH will not unintentionally drive the LED control pin low unless a serialization is in progress. System board connections using this serialization capability are required to use the same power plane controlling the LED as the PCH GPIO pin. Otherwise, the PCH GPIO may float low during the message and prevent the LED from being controlled from the SIO. The hardware will only be serializing messages when the core power well is powered and the processor is operational.

Care should be taken to prevent the PCH from driving an active '1' on a pin sharing the serial LED capability. Since the SIO could be driving the line to 0, having the PCH drive a 1 would create a high-current path. A recommendation to avoid this condition involves choosing a GPIO defaulting to an input. The GP\_SER\_BLINK register should be set first before changing the direction of the pin to an output. This sequence ensures the open-drain capability of the buffer is properly configured before enabling the pin as an output.

### 5.13.5.2

#### Serial Message Format

To serialize the data onto the GPIO, an initial state of high-Z is assumed. The SIO is required to have its LED control pin in a high-Z state as well to allow the PCH to blink the LED (refer to [Figure 5-8](#)).

The three components of the serial message include the sync, data, and idle fields. The sync field is 7 bits of '1' data followed by 1 bit of '0' data. Starting from the high-Z state (LED on) provides external hardware a known initial condition and a known pattern. In case one or more of the leading 1 sync bits are lost, the 1s followed by 0 provide a clear indication of 'end of sync'. This pattern will be used to 'lock' external sampling logic to the encoded clock.

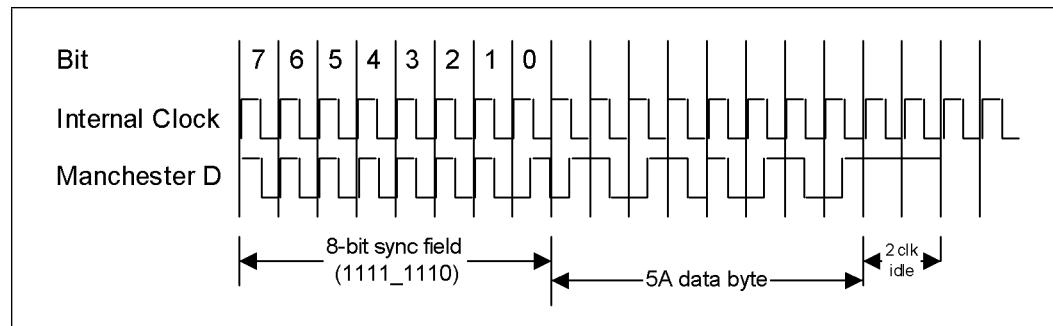
The data field is shifted out with the highest byte first (MSB). Within each byte, the most significant bit is shifted first (MSb).

The idle field is enforced by the hardware and is at least 2-bit times long. The hardware will not clear the Busy and Go bits until this idle time is met. Supporting the idle time in hardware prevents time-based counting in BIOS as the hardware is immediately ready for the next serial code when the Go bit is cleared.

**Note:** The idle state is represented as a high-Z condition on the pin. If the last transmitted bit is a 1, returning to the idle state will result in a final 0-1 transition on the output Manchester data. Two full bit times of idle correspond to a count of 4 time intervals; the width of the time interval is controlled by the DRS field.

The following waveform shows a 1-byte serial write with a data byte of 5Ah. The internal clock and bit position are for reference purposes only. The Manchester D is the resultant data generated and serialized onto the GPIO. Since the buffer is operating in open-drain mode, the transitions are from high-Z to 0 and back.

**Figure 5-9. One-Byte Serial Write with Data Byte of 5Ah**



## 5.13.6 Peripheral IRQ

Eight suspend well GPIOs and eight core well GPIOs are mapped to the new peripheral IRQ pins that are routed to dedicated entries of IOxAPIC. To be used as peripheral IRQ, a GPIO pin needs to be configured to GPIO mode input direction (GPIO\_USE\_SEL=1 and GPIO\_IO\_SEL=1). For PIRQ mapping to APIC interrupt, refer to [Table 5-12](#).

**Table 5-36. GPIO Mode Input to PIRQ Mapping (Sheet 1 of 2)**

GPIO #	PIRQ Mapping	GPIO Mode Power Well
8	PIRQI	Suspend
9	PIRQJ	Suspend
10	PIRQK	Suspend
13	PIRQL	Suspend
14	PIRQM	Suspend
45	PIRQN	Suspend
46	PIRQO	Suspend
47	PIRQP	Suspend
48	PIRQQ	Core
49	PIRQR	Core
50	PIRQS	Core

**Table 5-36. GPIO Mode Input to PIRQ Mapping (Sheet 2 of 2)**

GPIO #	PIRQ Mapping	GPIO Mode Power Well
51	PIRQT	Core
52	PIRQU	Core
53	PIRQV	Core
54	PIRQW	Core
55	PIRQX	Core

## 5.14 SATA Host Controller (D31:F2)

The SATA function supports AHCI or RAID mode.

The PCH SATA controller does not support legacy IDE mode or combination mode.

The PCH SATA controller features four sets of interface signals (ports) that can be independently enabled or disabled (they cannot be tri-stated or driven low). Each interface is supported by an independent DMA controller.

The PCH SATA controller interacts with an attached mass storage device through a register interface that is compatible with an SATA AHCI/RAID host adapter. The host software follows existing standards and conventions when accessing the register interface and follows standard command protocol conventions.

### 5.14.1 SATA 6Gb/s Support

The PCH SATA controller is SATA 6Gb/s capable and supports 6Gb/s transfers with all capable SATA devices. The PCH SATA controller also supports SATA 3Gb/s and 1.5Gb/s transfer capabilities.

### 5.14.2 SATA Feature Support

The PCH SATA controller is capable of supporting all AHCI 1.3 and AHCI 1.3.1 expanded capabilities for DEVSLP.

PCH SATA register details are in the [Chapter 11, "SATA Controller Registers \(D31:F2\)"](#).

Also, refer to the Intel web site on Advanced Host Controller Interface Specification for current specification status: <http://www.intel.com/content/www/us/en/io/serial-ata/ahci.html>.

For capability details, refer to PCH SATA controller register (D31:F2:Offset 00h CAP, D31:F2:Offset 04h CAP2, and AHCI BAR PxCMD Offset 18h).

The PCH SATA controller does **not** support:

- Port Multiplier
- FIS Based Switching
- Command Based Switching
- IDE mode or combination mode
- Cold Presence Detect
- Function Level Reset (FLR)



### 5.14.3 Hot-Plug Operation

The PCH SATA controller supports Hot-Plug Surprise removal and Insertion Notification. An internal SATA port with a Mechanical Presence Switch can support PARTIAL and SLUMBER with hot-plug Enabled. Software can take advantage of power savings in the low-power states while enabling hot-plug operation. Refer to Chapter 7 of the AHCI specification for details.

## 5.15 Intel® Rapid Storage Technology (Intel® RST) Configuration

Intel® RST offers several diverse options for RAID (redundant array of independent disks) to meet the needs of the end user. AHCI support provides higher performance and alleviates disk bottlenecks by taking advantage of the independent DMA engines that each SATA port offers in the PCH SATA controller.

- RAID Level 0 performance scaling up to 6 drives, enabling higher throughput for data intensive applications, such as video editing.
- Data redundancy is offered through RAID Level 1 that performs mirroring.
- RAID Level 10 provides high levels of storage performance with data protection, combining the fault-tolerance of RAID Level 1 with the performance of RAID Level 0. By striping RAID Level 1 segments, high I/O rates can be achieved on systems that require both performance and fault-tolerance. RAID Level 10 requires 4 hard drives, and provides the capacity of two drives.
- RAID Level 5 provides highly efficient storage while maintaining fault-tolerance on 3 or more drives. By striping parity, and rotating it across all disks, fault tolerance of any single drive is achieved while only consuming 1 drive worth of capacity. That is, a 3 drive RAID 5 has the capacity of 2 drives, or a 4 drive RAID 5 has the capacity of 3 drives. RAID 5 has high read transaction rates, with a medium write rate. RAID 5 is well suited for applications that require high amounts of storage while maintaining fault tolerance.

By using the PCH built-in Intel® Rapid Storage Technology, there is no loss of additional PCIe\*/system resources or add-in card slot/motherboard space footprint used, compared to when a discrete RAID controller is implemented. Intel® Rapid Storage Technology functionality requires the following:

- PCH SKU enabled for Intel® Rapid Storage Technology (see [Section 2.3](#))
- Intel® Rapid Storage Technology RAID Option ROM must be on the platform
- Intel® Rapid Storage Technology drivers, most recent revision.
- At least two SATA hard disk drives (minimum depends on RAID configuration).

Intel® Rapid Storage Technology is not available in the following configurations:

- The SATA controller is programmed in RAID mode, but the AIE bit (D31:F2:Offset 9Ch bit 7) is set to 1.

### 5.15.0.1 Intel® Rapid Storage Technology (Intel® RST) RAID Option ROM

The Intel® Rapid Storage Technology RAID Option ROM is a standard PnP Option ROM that is easily integrated into any System BIOS. When in place, it provides the following three primary functions:

- Provides a text mode user interface that allows the user to manage the RAID configuration on the system in a pre-operating system environment. Its feature set is kept simple to keep size to a minimum, but allows the user to create and delete RAID volumes and select recovery options when problems occur.
- Provides boot support when using a RAID volume as a boot disk. It does this by providing Int13 services when a RAID volume needs to be accessed by MS-DOS applications (such as NTLDR) and by exporting the RAID volumes to the System BIOS for selection in the boot order.
- At each boot up, provides the user with a status of the RAID volumes and the option to enter the user interface by pressing CTRL-I.

### 5.15.1 Intel® Smart Response Technology (Intel® RST)

Part of the Intel® RST storage class driver feature set, Intel® Smart Response Technology implements storage I/O caching to provide users with faster response times for things like system boot and application startup. On a traditional system, performance of these operations is limited by the hard drive, particularly when there may be other I/O intensive background activities running simultaneously, such as system updates or virus scans. Intel® Smart Response Technology accelerates the system response experience by putting frequently-used blocks of disk data on an SSD, providing dramatically faster access to user data than the hard disk alone can provide. The user sees the full capacity of the hard drive with the traditional single drive letter with overall system responsiveness similar to what an SSD-only system provides.

See Section 1.3 for SKUs enabled for Intel® Smart Response Technology.

### 5.15.2 Power Management Operation

Power management of the PCH SATA controller and ports will cover operations of the host controller and the SATA link.

#### 5.15.2.1 Power State Mappings

The D0 PCI power management (PM) state for a device is supported by the PCH SATA controller.

SATA devices may also have multiple power states. SATA adopted three main power states from parallel ATA. The three device states are supported through ACPI. They are:

- **D0** – Device is working and instantly available.
- **D1** – Device enters when it receives a STANDBY IMMEDIATE command. Exit latency from this state is in seconds
- **D3** – From the SATA device's perspective, no different than a D1 state, in that it is entered using the STANDBY IMMEDIATE command. However, an ACPI method is also called that will reset the device and then cut its power.

Each of these device states are subsets of the host controller's D0 state.



Finally, the SATA specification defines three PHY layer power states that have no equivalent mappings to parallel ATA. They are:

- **PHY READY** – PHY logic and PLL are both on and in active state
- **Partial** – PHY logic is powered up, and in a reduced power state. The link PM exit latency to active state maximum is 10 ns.
- **Slumber** – PHY logic is powered up, and in a reduced power state. The link PM exit latency to active state maximum is 10 ms.
- **Devslp** – PHY logic is powered down. The link PM exit latency from this state to active state maximum is 20 ms, unless otherwise specified by DETO in Identify Device Data Log page 08h (see 13.7.9.4 of the SATA Revision 3.2 Gold specification).

Since these states have much lower exit latency than the ACPI D1 and D3 states, the SATA controller specification defines these states as sub-states of the device D0 state.

## 5.15.2.2 Power State Transitions

### 5.15.2.2.1 Partial and Slumber State Entry/Exit

The partial and slumber states save interface power when the interface is idle. It would be most analogous to CLKRUN# (in power savings, not in mechanism), where the interface can have power saved while no commands are pending. The SATA controller defines PHY layer power management (as performed using primitives) as a driver operation from the host side, and a device proprietary mechanism on the device side. The SATA controller accepts device transition types, but does not issue any transitions as a host. All received requests from a SATA device will be ACKed.

When an operation is performed to the SATA controller such that it needs to use the SATA cable, the controller must check whether the link is in the Partial or Slumber states, and if so, must issue a COMWAKE to bring the link back online. Similarly, the SATA device must perform the same COMWAKE action.

### 5.15.2.2.2 Devslp State Entry/Exit

Devslp is a host-controlled hardware signal that enables a SATA host and device to enter an ultra-low interface power state, including the possibility of completely powering down the host and device PHYs.

### 5.15.2.2.3 Device D1 and D3 States

These states are entered after some period of time when software has determined that no commands will be sent to this device for some time. The mechanism for putting a device in these states does not involve any work on the host controller, other than sending commands over the interface to the device. The command most likely to be used in ATA/ATAPI is the "STANDBY IMMEDIATE" command.

### 5.15.2.2.4 Host Controller D3<sub>HOT</sub> State

After the interface and device have been put into a low-power state, the SATA host controller may be put into a low-power state. This is performed using the PCI power management registers in configuration space. There are two very important aspects to Note when using PCI power management.

1. When the power state is D3, only accesses to configuration space are allowed. Any attempt to access the memory or I/O spaces will result in master abort.

- When the power state is D3, no interrupts may be generated, even if they are enabled. If an interrupt status bit is pending when the controller transitions to D0, an interrupt may be generated.

When the controller is put into D3, it is assumed that software has properly shut down the device and disabled the ports. Therefore, there is no need to sustain any values on the port wires. The interface will be treated as if no device is present on the cable, and power will be minimized.

When returning from a D3 state, an internal reset will not be performed.

### 5.15.2.3 Low Power Platform Consideration

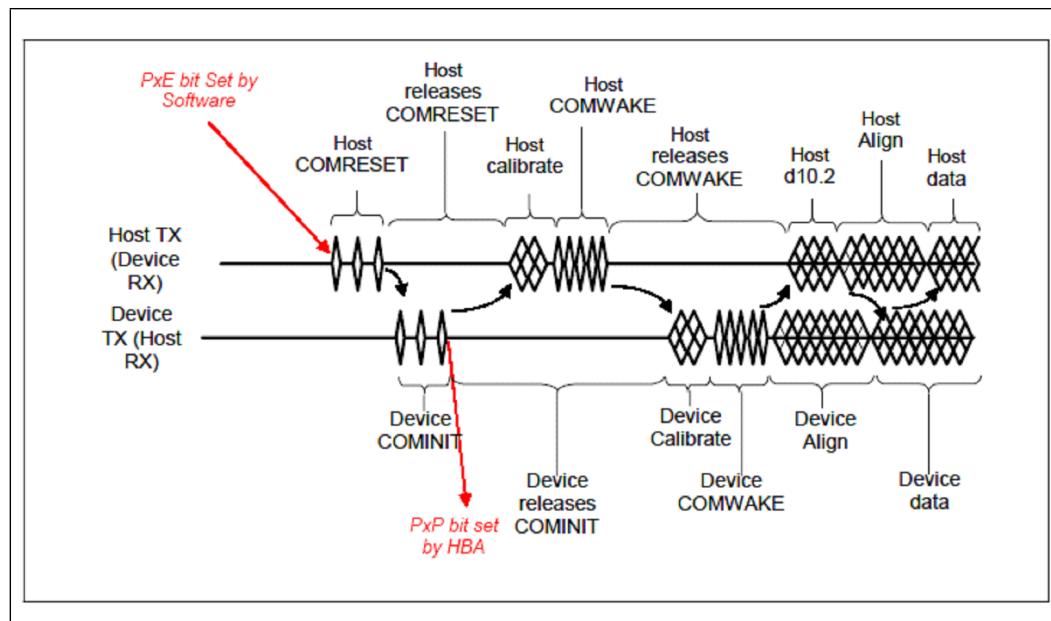
When the low power feature is enabled, the Intel SATA controller may power off PLLs or OOB detection circuitry while in the Slumber link power state. As a result, a device initiated wake may not be recognized by the host. For example, when the low power feature is enabled it can prevent a Zero Power ODD (ZPODD) device from successfully communicating with the host on media insertion.

**Note:** Refer to PHYDPGE of the SCLKGC2 register for details.

## 5.15.3 SATA Device Presence

The flow used to indicate SATA device presence is shown in [Figure 5-10](#). The 'PxE' bit refers to PCS.P[3:0]E bits, depending on the port being checked and the 'PxP' bits refer to the PCS.P[3:0]P bits, depending on the port being checked. If the PCS/PxP bit is set, a device is present; if the bit is cleared, a device is not present. If a port is disabled, software can check to see if a new device is connected by periodically re-enabling the port and observing if a device is present. If a device is not present, it can disable the port and check again later. If a port remains enabled, software can periodically poll PCS.PxP to see if a new device is connected.

**Figure 5-10. Flow for Port Enable/Device Present Bits**





## 5.15.4 SATA LED

The SATALED# output is driven whenever the BSY bit is set in any SATA port. SATALED# is an active-low open-drain output. When SATALED# is low, the LED should be active. When SATALED# is high, the LED should be inactive.

## 5.15.5 Advanced Host Controller Interface (AHCI) Operation

The PCH SATA controller provides hardware support for the Advanced Host Controller Interface (AHCI)—a programming interface for SATA host controllers developed through a joint industry effort. AHCI defines transactions between the SATA controller and software and enables advanced performance and usability with SATA. Platforms supporting AHCI may take advantage of performance features such as no master/slave designation for SATA devices—each device is treated as a master—and hardware assisted native command queuing. AHCI also provides usability enhancements, such as hot-plug. AHCI requires appropriate software support (such as, an AHCI driver) and for some features, hardware support in the SATA device or additional platform hardware.

The PCH SATA controller supports all of the mandatory features of the *Serial ATA Advanced Host Controller Interface Specification*, Revision 1.3 and many optional features, such as hardware assisted native command queuing, aggressive power management, LED indicator support, and hot-plug through the use of interlock switch support. Additional platform hardware and software may be required depending on the implementation.

**Note:**

For reliable device removal notification while in AHCI operation without the use of interlock switches (surprise removal), interface power management should be disabled for the associated port. See Section 7.3.1 of the *AHCI Specification* for more information.

## 5.15.6 External SATA

The PCH SATA controller supports external SATA. External SATA uses the SATA interface outside of the system box. The usage model for this feature must comply with the *Serial ATA II (SATA Gen 2, 3Gb/s) Cables and Connectors Volume 2 Gold specification* at:

[www.sata-io.org](http://www.sata-io.org). Intel® validates one configuration:

- The back-panel solution involves running a trace to the I/O back panel and connecting a device using an external SATA connector on the board.

## 5.16 High Precision Event Timers (HPET)

This function provides a set of timers that can be used by the operating system. The timers are defined such that the operating system may be able to assign specific timers to be used directly by specific applications. Each timer can be configured to cause a separate interrupt.

The PCH provides eight timers. The timers are implemented as a single counter, and each timer has its own comparator and value register. The counter increases monotonically. Each individual timer can generate an interrupt when the value in its value register matches the value in the main counter.

The registers associated with these timers are mapped to a memory space (much like the I/O APIC). However, it is not implemented as a standard PCI function. The BIOS reports to the operating system the location of the register space. The hardware can support an assignable decode space; however, BIOS sets this space prior to handing it over to the operating system. It is not expected that the operating system will move the location of these timers once it is set by BIOS.

## 5.16.1 Timer Accuracy

The timers are accurate over any 1 ms period to within 0.05% of the time specified in the timer resolution fields.

Within any 100 microsecond period, the timer reports a time that is up to two ticks too early or too late. Each tick is less than or equal to 100 ns—thus, this represents an error of less than 0.2%.

The timer is monotonic. It does not return the same value on two consecutive reads (unless the counter has rolled over and reached the same value).

The main counter is clocked by the 14.31818 MHz clock derived from 24 MHz xtal clock. The accuracy of the main counter is as accurate as the 14.31818 MHz clock.

## 5.16.2 Interrupt Mapping

### Mapping Option #1 (Legacy Replacement Option)

In this case, the Legacy Replacement Rout bit (LEG\_RT\_CNF) is set. This forces the mapping found in [Table 5-37](#).

**Table 5-37. Legacy Replacement Routing**

Timer	8259 Mapping	APIC Mapping	Comment
0	IRQ0	IRQ2	In this case, the 8254 timer will not cause any interrupts
1	IRQ8	IRQ8	In this case, the RTC will not cause any interrupts.
2 and 3	Per IRQ Routing Field.	Per IRQ Routing Field	
4, 5, 6, 7	not available	not available	

**Note:** The Legacy Option does not preclude delivery of IRQ0/IRQ8 using processor interrupts messages.

### Mapping Option #2 (Standard Option)

In this case, the Legacy Replacement Rout bit (LEG\_RT\_CNF) is 0. Each timer has its own routing control. The interrupts can be routed to various interrupts in the 8259 or I/O APIC. A capabilities field indicates which interrupts are valid options for routing. If a timer is set for edge-triggered mode, the timers should not be shared with any legacy interrupts.

For the PCH, the only supported interrupt values are as follows:

Timer 0 and 1: IRQ20, 21, 22, and 23 (I/O APIC only).

Timer 2: IRQ11 (8259 or I/O APIC) and IRQ20, 21, 22, and 23 (I/O APIC only).

Timer 3: IRQ12 (8259 or I/O APIC) and IRQ 20, 21, 22, and 23 (I/O APIC only).



Interrupts from Timer 4, 5, 6, 7 can only be delivered using processor message interrupts.

#### Mapping Option #3 (Processor Message Option)

In this case, the interrupts are mapped directly to processor messages without going to the 8259 or I/O (x) APIC. To use this mode, the interrupt must be configured to edge-triggered mode. The Tn\_PROCMMSG\_EN\_CNF bit must be set to enable this mode.

When the interrupt is delivered to the processor, the message is delivered to the address indicated in the Tn\_PROCMMSG\_INT\_ADDR field. The data value for the write cycle is specified in the Tn\_PROCMMSG\_INT\_VAL field.

**Note:**

The processor message interrupt delivery option has HIGHER priority and is mutually exclusive to the standard interrupt delivery option. Thus, if the Tn\_PROCMMSG\_EN\_CNF bit is set, the interrupts will be delivered directly to the processor, rather than by means of the APIC or 8259.

The processor message interrupt delivery can be used even when the legacy mapping is used.

### 5.16.3 Periodic Versus Non-Periodic Modes

#### Non-Periodic Mode

Timer 0 is configurable to 32 (default) or 64-bit mode, whereas Timers 1:7 only support 32-bit mode.

**Warning:**

Software must be careful when programming the comparator registers. If the value written to the register is not sufficiently far in the future, then the counter may pass the value before it reaches the register and the interrupt will be missed. The BIOS should pass a data structure to the operating system to indicate that the operating system should not attempt to program the periodic timer to a rate faster than 5 microseconds.

All of the timers support non-periodic mode.

Refer to Section 2.3.9.2.1 of the *IA-PC HPET Specification* for more details of this mode.

#### Periodic Mode

Timer 0 is the only timer that supports periodic mode. Refer to Section 2.3.9.2.2 of the *IA-PC HPET Specification* for more details of this mode.

If the software resets the main counter, the value in the comparator's value register needs to reset as well. This can be done by setting the TIMERn\_VAL\_SET\_CNF bit. Again, to avoid race conditions, this should be done with the main counter halted. The following usage model is expected:

1. Software clears the ENABLE\_CNF bit to prevent any interrupts.
2. Software Clears the main counter by writing a value of 00h to it.
3. Software sets the TIMER0\_VAL\_SET\_CNF bit.
4. Software writes the new value in the TIMER0\_COMPARATOR\_VAL register.
5. Software sets the ENABLE\_CNF bit to enable interrupts.

The Timer 0 Comparator Value register cannot be programmed reliably by a single 64-bit write in a 32-bit environment, except if only the periodic rate is being changed during run-time. If the actual Timer 0 Comparator Value needs to be reinitialized, then the following software solution will always work, regardless of the environment:

1. Set TIMER0\_VAL\_SET\_CNF bit.
2. Set the lower 32 bits of the Timer0 Comparator Value register.
3. Set TIMER0\_VAL\_SET\_CNF bit.
4. Set the upper 32 bits of the Timer0 Comparator Value register.

#### 5.16.4 Enabling the Timers

The BIOS or operating system PnP code should route the interrupts. This includes the Legacy Rout bit, Interrupt Rout bit (for each timer), and interrupt type (to select the edge or level type for each timer).

The Device Driver code should do the following for an available timer:

1. Set the Overall Enable bit (Offset 10h, bit 0).
2. Set the timer type field (selects one-shot or periodic).
3. Set the interrupt enable.
4. Set the comparator value.

#### 5.16.5 Interrupt Levels

Interrupts directed to the internal 8259s are active high. See [Section 5.7](#) for information regarding the polarity programming of the I/O APIC for detecting internal interrupts.

If the interrupts are mapped to the 8259 or I/O APIC and set for level-triggered mode, they can be shared with legacy interrupts. They may be shared although it is unlikely for the operating system to attempt to do this.

If more than one timer is configured to share the same IRQ (using the TIMERn\_INT\_ROUT\_CNF fields), then the software must configure the timers to level-triggered mode. Edge-triggered interrupts cannot be shared.

#### 5.16.6 Handling Interrupts

Section 2.4.6 of the *IA-PC HPET Specification* describes handling interrupts.

#### 5.16.7 Issues Related to 64-Bit Timers with 32-Bit Processors

Section 2.4.7 of the *IA-PC HPET Specification* describes issues related to 64-Bit timers with 32-Bit processors.



## 5.17 USB Enhanced Host Controller Interface (EHCI) Host Controller (D29:F0)

The PCH contains one Enhanced Host Controller Interface (EHCI) host controller that support up to eight USB 2.0 high-speed root ports. USB 2.0 allows data transfers up to 480Mb/s. A USB 2.0-based Debug Port is also implemented in the PCH.

### 5.17.1 Enhanced Host Controller (EHC) Initialization

The following descriptions step through the expected PCH Enhanced Host Controller (EHC) initialization sequence in chronological order, beginning with a complete power-cycle in which the suspend well and core well have been off.

#### 5.17.1.1 BIOS Initialization

BIOS performs a number of platform customization steps after the core well has powered up. Contact your Intel Field Representative for additional PCH BIOS information.

#### 5.17.1.2 Driver Initialization

See Chapter 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 1.0.

#### 5.17.1.3 Enhance Host Controller (EHC) Resets

In addition to the standard PCH hardware resets, portions of the EHC are reset by the HCRESET bit and the transition from the D3<sub>HOT</sub> device power management state to the D0 state. The effects of each of these resets are shown in the following table.

**Table 5-38. Enhance Host Controller (EHC) Resets**

Reset	Does Reset	Does Not Reset	Comments
HCRESET bit set.	Memory space registers except Structural Parameters (which is written by BIOS).	Configuration registers.	The HCRESET must only affect registers that the EHCI driver controls. PCI Configuration space and BIOS-programmed parameters cannot be reset.
Software writes the Device Power State from D3 <sub>HOT</sub> (11b) to D0 (00b).	Core well registers (except BIOS-programmed registers).	Suspend well registers; BIOS-programmed core well registers.	The D3-to-D0 transition must not cause wake information (suspend well) to be lost. It also must not clear BIOS-programmed registers because BIOS may not be invoked following the D3-to-D0 transition.

If the detailed register descriptions provide exceptions to these rules, those exceptions override these rules. This summary is provided to help explain the reasons for the reset policies.

### 5.17.2 Data Structures in Main Memory

See Section 3 and Appendix B of the *Enhanced Host Controller Interface Specification for Universal Serial Bus*, Revision 1.0 for details.

### 5.17.3 USB 2.0 Enhanced Host Controller (EHC) DMA

The PCH USB 2.0 EHC implements three sources of USB packets. They are, in order of priority on USB during each microframe:

1. The USB 2.0 Debug Port,
2. The Periodic DMA engine, and
3. The Asynchronous DMA engine.

The PCH always performs any currently-pending debug port transaction at the beginning of a microframe, followed by any pending periodic traffic for the current microframe. If there is time left in the microframe, then the EHC performs any pending asynchronous traffic until the end of the microframe (EOF1).

**Note:**

The debug port traffic is only presented on Port 1, while the other ports are idle during this time.

### 5.17.4 Data Encoding and Bit Stuffing

See Chapter 8 of the *Universal Serial Bus Specification, Revision 2.0*.

### 5.17.5 Packet Formats

See Chapter 8 of the *Universal Serial Bus Specification, Revision 2.0*.

The PCH EHCI allows entrance to USB test modes, as defined in the USB 2.0 specification, including Test J, Test Packet, and so on. However, the PCH Test Packet test mode interpacket gap timing may not meet the USB 2.0 specification.

### 5.17.6 USB 2.0 Interrupts and Error Conditions

Section 4 of the *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0* goes into detail on the EHC interrupts and the error conditions that cause them. All error conditions that the EHC detects can be reported through the EHCI Interrupt status bits. Only PCH-specific interrupt and error-reporting behavior is documented in this section. The EHCI Interrupts Section must be read first, followed by this section of the datasheet to fully comprehend the EHC interrupt and error-reporting functionality.

- Based on the EHC Buffer sizes and buffer management policies, the Data Buffer Error can never occur on the PCH.
- Master Abort and Target Abort responses from hub interface on EHC-initiated read packets will be treated as Fatal Host Errors. The EHC halts when these conditions are encountered.
- The PCH may assert the interrupts that are based on the interrupt threshold as soon as the status for the last complete transaction in the interrupt interval has been posted in the internal write buffers. The requirement in the *Enhanced Host Controller Interface Specification for Universal Serial Bus, Revision 1.0* (that the status is written to memory) is met internally.
- Since the PCH supports the 1024-element Frame List size, the Frame List Rollover interrupt occurs every 1024 milliseconds.
- The PCH delivers interrupts using PIRQH#.
- The PCH does not modify the CERR count on an Interrupt IN when the "Do Complete-Split" execution criteria are not met.

- For complete-split transactions in the Periodic list, the “Missed Microframe” bit does not get set on a control-structure-fetch that fails the late-start test. If subsequent accesses to that control structure do not fail the late-start test, then the “Missed Microframe” bit will get set and written back.

### 5.17.6.1 Aborts on USB 2.0 Initiated Memory Reads

If a read initiated by the EHC is aborted, the EHC treats it as a fatal host error. The following actions are taken when this occurs:

- The Host System Error status bit is set.
- The DMA engines are halted after completing up to one more transaction on the USB interface.
- If enabled (by the Host System Error Enable), then an interrupt is generated.
- If the status is Master Abort, then the Received Master Abort bit in configuration space is set.
- If the status is Target Abort, then the Received Target Abort bit in configuration space is set.
- If enabled (by the SERR Enable bit in the function’s configuration space), then the Signaled System Error bit in configuration bit is set.

## 5.17.7 USB 2.0 Power Management

### 5.17.7.1 Pause Feature

This feature allows platforms to dynamically enter low-power states during brief periods when the system is idle (that is, between keystrokes). This is useful for enabling power management features in the PCH. The policies for entering these states typically are based on the recent history of system bus activity to incrementally enter deeper power management states. Normally, when the EHC is enabled, it regularly accesses main memory while traversing the DMA schedules looking for work to do; this activity is viewed by the power management software as a non-idle system; thus, preventing the power managed states to be entered. Suspending all of the enabled ports can prevent the memory accesses from occurring, but there is an inherent latency overhead with entering and exiting the suspended state on the USB ports that makes this unacceptable for the purpose of dynamic power management. As a result, the EHCI software drivers are allowed to pause the EHC DMA engines when it knows that the traffic patterns of the attached devices can afford the delay. The pause only prevents the EHC from generating memory accesses; the SOF packets continue to be generated on the USB ports (unlike the suspended state).

### 5.17.7.2 Suspend Feature

The *Enhanced Host Controller Interface (EHCI) For Universal Serial Bus Specification*, Section 4.3 describes the details of Port Suspend and Resume.

### 5.17.7.3 ACPI Device States

The USB 2.0 function only supports the D0 and D3 PCI Power Management states.

The PCH implementation of the Device States:

- The EHC hardware does not inherently consume any more power when it is in the D0 state than it does in the D3 state. However, software is required to suspend or disable all ports prior to entering the D3 state such that the maximum power consumption is reduced.
- In the D0 state, all implemented EHC features are enabled.
- In the D3 state, accesses to the EHC memory-mapped I/O range will master abort.

**Note:** Since the Debug Port uses the same memory range, the Debug Port is only operational when the EHC is in the D0 state.

4. In the D3 state, the EHC interrupt must never assert for any reason. The internal PME# signal is used to signal wake events, and so on.
5. When the Device Power State field is written to D0 from D3, an internal reset is generated. See section EHC Resets for general rules on the effects of this reset.
6. Attempts to write any other value into the Device Power State field other than 00b (D0 state) and 11b (D3 state) will complete normally without changing the current value in this field.

#### 5.17.7.4 ACPI System States

The EHC behavior as it relates to other power management states in the system is summarized in the following list:

- The System is always in the S0 state when the EHC is in the D0 state. However, when the EHC is in the D3 state, the system may be in any power management state (including S0).
- When in D0, the Pause feature enables dynamic processor low-power states to be entered.
- The PLL in the EHC is disabled when entering the S3/S4/S5 states (core power turns off).
- All core well logic is reset in the S3/S4/S5 states.

#### 5.17.8 USB 2.0 Legacy Keyboard Operation

The PCH must support the possibility of a keyboard downstream from either a full-speed/low-speed or a high-speed port. The description of the legacy keyboard support is unchanged from USB 1.1.

The EHC provides the basic ability to generate SMIs on an interrupt event, along with more sophisticated control of the generation of SMIs.

#### 5.17.9 USB 2.0 Based Debug Port

The PCH supports the elimination of the legacy COM ports by providing the ability for debugger software to interact with devices on a USB 2.0 port.

High-level restrictions and features are:

- Operational before USB 2.0 drivers are loaded.
- Functions even when the port is disabled.
- Allows normal system USB 2.0 traffic in a system that may only have one USB port.
- Debug Port device (DPD) must be high-speed capable and connect directly to Port 1 on PCH-based systems (such as, the DPD cannot be connected to Port 1 through a hub. When a DPD is detected, the PCH EHCI will bypass the integrated Rate Matching Hub and connect directly to the port and the DPD.).
- Debug Port FIFO always makes forward progress (a bad status on USB is simply presented back to software).
- The Debug Port FIFO is only given one USB access per microframe.



The Debug port facilitates operating system and device driver debug. It allows the software to communicate with an external console using a USB 2.0 connection. Because the interface to this link does not go through the normal USB 2.0 stack, it allows communication with the external console during cases where the operating system is not loaded, the USB 2.0 software is broken, or where the USB 2.0 software is being debugged. Specific features of this implementation of a debug port are:

- Only works with an external USB 2.0 debug device (console)
- Implemented for a specific port on the host controller
- Operational anytime the port is not suspended AND the host controller is in D0 power state.
- Capability is interrupted when port is driving USB RESET

### 5.17.9.1 Theory of Operation

There are two operational modes for the USB debug port:

1. Mode 1 is when the USB port is in a disabled state from the viewpoint of a standard host controller driver. In Mode 1, the Debug Port controller is required to generate a "keepalive" packets less than 2 ms apart to keep the attached debug device from suspending. The keepalive packet should be a standalone 32-bit SYNC field.
2. Mode 2 is when the host controller is running (that is, host controller's *Run/Stop*# bit is 1). In Mode 2, the normal transmission of SOF packets will keep the debug device from suspending.

#### Behavioral Rules

1. In both modes 1 and 2, the Debug Port controller must check for software requested debug transactions at least every 125 microseconds.
2. If the debug port is enabled by the debug driver, and the standard host controller driver resets the USB port, USB debug transactions are held off for the duration of the reset and until after the first SOF is sent.
3. If the standard host controller driver suspends the USB port, then USB debug transactions are held off for the duration of the suspend/resume sequence and until after the first SOF is sent.
4. The ENABLED\_CNT bit in the debug register space is independent of the similar port control bit in the associated Port Status and Control register.

Table 5-39 shows the debug port behavior related to the state of bits in the debug registers as well as bits in the associated Port Status and Control register.

**Table 5-39. Debug Port Behavior (Sheet 1 of 2)**

OWNER_CNT	ENABLED_CT	Port Enable	Run/Stop	Suspend	Debug Port Behavior
0	X	X	X	X	Debug port is not being used. Normal operation.
1	0	X	X	X	Debug port is not being used. Normal operation.
1	1	0	0	X	Debug port in Mode 1. SYNC keepalives sent plus debug traffic
1	1	0	1	X	Debug port in Mode 2. SOF (and only SOF) is sent as keepalive. Debug traffic is also sent. <b>Note:</b> No other normal traffic is sent out this port, because the port is not enabled.

**Table 5-39. Debug Port Behavior (Sheet 2 of 2)**

OWNER_CNT	ENABLED_CNT	Port Enable	Run/Stop	Suspend	Debug Port Behavior
1	1	1	0	0	Invalid. Host controller driver should never put controller into this state (enabled, not running and not suspended).
1	1	1	0	1	Port is suspended. No debug traffic sent.
1	1	1	1	0	Debug port in Mode 2. Debug traffic is interspersed with normal traffic.
1	1	1	1	1	Port is suspended. No debug traffic sent.

#### 5.17.9.1.1 OUT Transactions

An OUT transaction sends data to the debug device. It can occur only when the following are true:

- The debug port is enabled
- The debug software sets the GO\_CNT bit
- The WRITE\_READ#\_CNT bit is set

The sequence of the transaction is:

1. Software sets the appropriate values in the following bits:
  - USB\_ADDRESS\_CNF
  - USB\_ENDPOINT\_CNF
  - DATA\_BUFFER[63:0]
  - TOKEN\_PID\_CNT[7:0]
  - SEND\_PID\_CNT[15:8]
  - DATA\_LEN\_CNT
  - WRITE\_READ#\_CNT:

**Note:** This will always be 1 for OUT transactions  
 — GO\_CNT:

**Note:** This will always be 1 to initiate the transaction

2. The debug port controller sends a token packet consisting of:
  - SYNC
  - TOKEN\_PID\_CNT field
  - USB\_ADDRESS\_CNT field
  - USB\_ENDPOINT\_CNT field
  - 5-bit CRC field
3. After sending the token packet, the debug port controller sends a data packet consisting of:
  - SYNC
  - SEND\_PID\_CNT field
  - The number of data bytes indicated in DATA\_LEN\_CNT from the DATA\_BUFFER
  - 16-bit CRC

**Note:** A DATA\_LEN\_CNT value of 0 is valid in which case no data bytes would be included in the packet.



4. After sending the data packet, the controller waits for a handshake response from the debug device.
  - If a handshake is received, the debug port controller:
    - a. Places the received PID in the RECEIVED\_PID\_STS field
    - b. Resets the ERROR\_GOOD#\_STS bit
    - c. Sets the DONE\_STS bit
  - If no handshake PID is received, the debug port controller:
    - a. Sets the EXCEPTION\_STS field to 001b
    - b. Sets the ERROR\_GOOD#\_STS bit
    - c. Sets the DONE\_STS bit

#### 5.17.9.1.2 IN Transactions

An IN transaction receives data from the debug device. It can occur only when the following are true:

- The debug port is enabled
- The debug software sets the GO\_CNT bit
- The WRITE\_READ#\_CNT bit is reset

The sequence of the transaction is:

1. Software sets the appropriate values in the following bits:
  - USB\_ADDRESS\_CNF
  - USB\_ENDPOINT\_CNF
  - TOKEN\_PID\_CNT[7:0]
  - DATA\_LEN\_CNT
  - WRITE\_READ#\_CNT:
- Note:** This will always be 0 for IN transactions
  - GO\_CNT:
- Note:** This will always be 1 to initiate the transaction
2. The debug port controller sends a token packet consisting of:
  - SYNC
  - TOKEN\_PID\_CNT field
  - USB\_ADDRESS\_CNF field
  - USB\_ENDPOINT\_CNF field
  - 5-bit CRC field.
3. After sending the token packet, the debug port controller waits for a response from the debug device.
 

If a response is received:

  - The received PID is placed into the RECEIVED\_PID\_STS field
  - Any subsequent bytes are placed into the DATA\_BUFFER
  - The DATA\_LEN\_CNT field is updated to show the number of bytes that were received after the PID.

4. If a valid packet was received from the device that was one byte in length (indicating it was a handshake packet), then the debug port controller:
  - Resets the ERROR\_GOOD#\_STS bit
  - Sets the DONE\_STS bit
5. If a valid packet was received from the device that was more than one byte in length (indicating it was a data packet), then the debug port controller:
  - Transmits an ACK handshake packet
  - Resets the ERROR\_GOOD#\_STS bit
  - Sets the DONE\_STS bit
6. If no valid packet is received, then the debug port controller:
  - Sets the EXCEPTION\_STS field to 001b
  - Sets the ERROR\_GOOD#\_STS bit
  - Sets the DONE\_STS bit.

#### 5.17.9.1.3 Debug Software

##### Enabling the Debug Port

There are two mutually exclusive conditions that debug software must address as part of its startup processing:

- The EHCI has been initialized by system software
- The EHCI has not been initialized by system software

Debug software can determine the current 'initialized' state of the EHCI by examining the Configure Flag in the EHCI USB 2.0 Command Register. If this flag is set, then system software has initialized the EHCI. Otherwise, the EHCI should not be considered initialized. Debug software will initialize the debug port registers depending on the state of the EHCI. However, before this can be accomplished, debug software must determine which root USB port is designated as the debug port.

##### Determining the Debug Port

Debug software can easily determine which USB root port has been designated as the debug port by examining bits 20:23 of the EHCI Host Controller Structural Parameters register. This 4-bit field represents the numeric value assigned to the debug port (that is, 0001=port 1).

##### Debug Software Startup with Non-Initialized EHCI

Debug software can attempt to use the debug port if after setting the OWNER\_CNT bit, the Current Connect Status bit in the appropriate (See *Determining the Debug Port Presence*) PORTSC register is set. If the Current Connect Status bit is not set, then debug software may choose to terminate or it may choose to wait until a device is connected.

If a device is connected to the port, then debug software must reset/enable the port. Debug software does this by setting and then clearing the Port Reset bit the PORTSC register. To ensure a successful reset, debug software should wait at least 50 ms before clearing the Port Reset bit. Due to possible delays, this bit may not change to 0 immediately; reset is complete when this bit reads as 0. Software must not continue until this bit reads 0.



If a high-speed device is attached, the EHCI will automatically set the Port Enabled/Disabled bit in the PORTSC register and the debug software can proceed. Debug software should set the ENABLED\_CNT bit in the Debug Port Control/Status register, and then reset (clear) the Port Enabled/Disabled bit in the PORTSC register (so that the system host controller driver does not see an enabled port when it is first loaded).

#### **Debug Software Startup with Initialized EHCI**

Debug software can attempt to use the debug port if the Current Connect Status bit in the appropriate (See Determining the Debug Port) PORTSC register is set. If the Current Connect Status bit is not set, then debug software may choose to terminate or it may choose to wait until a device is connected.

If a device is connected, then debug software must set the OWNER\_CNT bit and then the ENABLED\_CNT bit in the Debug Port Control/Status register.

#### **Determining Debug Peripheral Presence**

After enabling the debug port functionality, debug software can determine if a debug peripheral is attached by attempting to send data to the debug peripheral. If all attempts result in an error (Exception bits in the Debug Port Control/Status register indicates a Transaction Error), then the attached device is not a debug peripheral. If the debug port peripheral is not present, then debug software may choose to terminate or it may choose to wait until a debug peripheral is connected.

### **5.17.10 EHCI Caching**

EHCI Caching is a power management feature in the USB (EHCI) host controllers that enables the controller to execute the schedules entirely in cache and eliminates the need for the DMA engine to access memory when the schedule is idle. EHCI caching allows the processor to maintain longer C-State residency times and provides substantial system power savings.

### **5.17.11 Intel® USB Pre-Fetch Based Pause**

The Intel® USB Pre-Fetch Based Pause is a power management feature in USB (EHCI) host controllers to ensure maximum C3/C4 processor power state time with C2 popup. This feature applies to the period schedule, and works by allowing the DMA engine to identify periods of idleness and preventing the DMA engine from accessing memory when the periodic schedule is idle. Typically in the presence of periodic devices with multiple millisecond poll periods, the periodic schedule will be idle for several frames between polls.

The Intel® USB Pre-Fetch Based Pause feature is disabled by setting bit 4 of EHCI Configuration Register.

### **5.17.12 Function Level Reset Support (FLR)**

The USB EHCI Controllers support the Function Level Reset (FLR) capability. The FLR capability can be used in conjunction with Intel Virtualization Technology. FLR allows an operating system in a Virtual Machine to have complete control over a device, including its initialization, without interfering with the rest of the platform. The device provides a software interface that enables the operating system to reset the whole device as if a platform reset was asserted.

### 5.17.12.1 FLR Steps

#### 5.17.12.1.1 FLR Initialization

1. A FLR is initiated by software writing a '1' to the Initiate FLR bit.
2. All subsequent requests targeting the Function will not be claimed and will be Master Abort Immediate on the bus. This includes any configuration, I/O or memory cycles; however, the Function shall continue to accept completions targeting the Function.

#### 5.17.12.1.2 FLR Operation

The Function will Reset all configuration, I/O and memory registers of the Function except those indicated otherwise and reset all internal states of the Function to the default or initial condition.

#### 5.17.12.1.3 FLR Completion

The Initiate FLR bit is reset (cleared) when the FLR reset is completed. This bit can be used to indicate to the software that the FLR reset is completed.

**Note:** From the time Initiate FLR bit is written to 1, software must wait at least 100 ms before accessing the function.

### 5.17.13 USB Overcurrent Protection

The PCH has implemented programmable USB Overcurrent signals. The PCH provides a total of 4 overcurrent pins to be shared across the 8 ports.

Four overcurrent signals have been allocated to the ports in each USB Device:

- OC[3:0]# for Device 29 (Ports 0-7)

Each pin is mapped to one or more ports by setting bits in the USBOCM1 and USBOCM2 registers. It is the responsibility of system BIOS to ensure that each port is mapped to only one over current pin. Operation with more than one overcurrent pin mapped to a port is undefined. It is expected that multiple ports are mapped to a single overcurrent pin; however, they should be connected at the port and not at the PCH pin. Shorting these pins together may lead to reduced test capabilities.

**Note:** All USB ports routed out of the package must have Overcurrent protection. It is system BIOS responsibility to ensure all used ports have Overcurrent protection.

**Note:** USB Ports that are unused on the system (not routed out from the package) should not have Overcurrent pins assigned to them.

### 5.18 Integrated USB 2.0 Rate Matching Hub

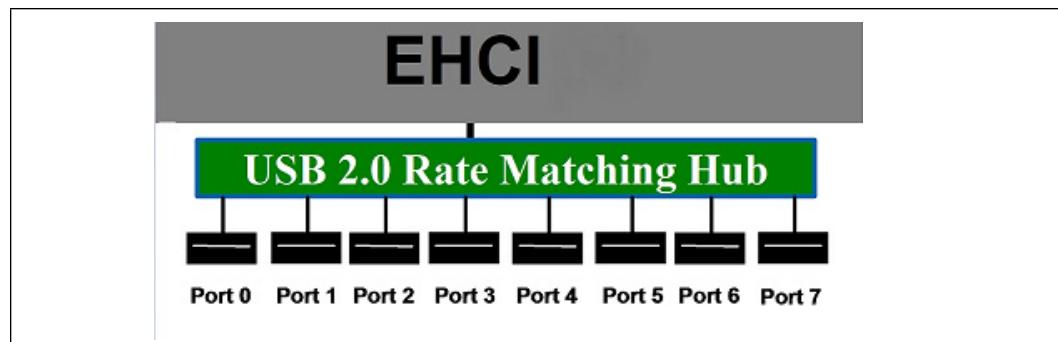
#### 5.18.1 Overview

The PCH has an integrated USB 2.0 Rate Matching Hubs (RMH). The hub is connected to the EHCI controllers as shown in [Figure 5-11](#). The hub converts low- and full-speed traffic into high-speed traffic. The RMH will appear to software like an external hub is

connected to Port 0 of the EHCI controller. In addition, port 1 of the RMH is multiplexed with Port 1 of the EHCI controller and is able to bypass the RMH for use as the Debug Port.

The hub operates like any USB 2.0 Discrete Hub and will consume one tier of hubs allowed by the USB 2.0 Specification, section 4.1.1. A maximum of four additional non-root hubs can be supported on any of the PCH USB Ports. The RMH will report the following Vendor ID = 8087h and Product ID = 8000h.

**Figure 5-11. EHCI with USB 2.0 with Rate Matching Hub**



## 5.18.2 Architecture

A hub consists of three components: the Hub Repeater, the Hub Controller, and the Transaction Translator.

1. The Hub Repeater is responsible for connectivity setup and tear-down. It also supports exception handling, such as bus fault detection and recovery and connect/disconnect detect.
2. The Hub Controller provides the mechanism for host-to-hub communication. Hub-specific status and control commands permit the host to configure a hub and to monitor and control its individual downstream facing ports.
3. The Transaction Translator (TT) responds to high-speed split transactions and translates them to full/low-speed transactions with full/low-speed devices attached on downstream facing ports. There is 1 TT per RMH in the PCH.

See Chapter 11 of the USB 2.0 Specification for more details on the architecture of the hubs.

## 5.19 eXtensible Host Controller Interface (xHCI) Controller (D20:F0)

The PCH contains an eXtensible Host Controller Interface (xHCI) host controller that supports up to 10, (based on select SKU) USB 2.0 ports of which up to 4 can be used as USB 3.0 ports with board routing, ACPI table and BIOS considerations. This controller allows data transfers of up to 5Gb/s. The controller supports SuperSpeed (SS), High-Speed (HS), Full-Speed (FS) and Low-Speed (LS) traffic on the bus.

The xHCI controller supports USB Debug port on all USB 3.0 capable ports.

USB Attached SCSI Protocol (UASP) is supported.

**Note:** Some USB 3.0 motherboard down devices do not require support for a USB 2.0 speed and it is possible to route only the SuperSpeed signals, as allowed by the USB 3.0 specification. In this special case, USB 2.0 and USB 3.0 signals will not need to be paired together; thereby, allowing support for more than 10, USB connections.

## 5.20 Flexible I/O

Flexible I/O is an architecture to allow some high-speed signals to be configured as PCIe\*, USB 3.0 or SATA signals per I/O needs on a platform. There are 14, differential pairs that are split between the three interfaces. Among them, 6 differential pairs are multiplexed: 2 multiplexed differential pairs can be configured to be used as PCIe\* port 1, 2, or USB 3.0 port 3, 4 and the other 4 differential pairs can be configured to be used as PCIe\* port 6 lane 3 to 0 or SATA port 3 to 0. [Figure 5-40](#) illustrates how the signals are used for Flexible I/O.

The Flexible I/O is configured through soft straps. These Flexible I/O ports can be configured in any way as allowed by the soft strap, provided that the maximum number of PCIe\* ports does not exceed 6.

**Note:** Specifically for the multiplexed differential signal pairs between SATA and PCIe\*, the corresponding soft straps provide an option to select desired ports by means of GPIO34 – GPIO37. If a GPIO is chosen to select the desired port, the GPIO value needs to be valid at PLTRST# de-assertion and must be maintained without change while PCH\_PLTRST# remains de-asserted.

**Table 5-40. Flexible I/O—High Speed Signal Mapping with PCIe\*, USB 3.0, and SATA Ports**

HSIO Port	1	2	3	4	5	6	7	8	9	10	11	12	13	14
USB3.0	1	2	3	4										
PCIe			1	2	3	4	5-L0	5-L1	5-L2	5-L3	6-L0	6-L1	6-L2	6-L3
SATA											3	2	1	0
GbE	soft strap values -->				000	001	010	011	100	101				

**Notes:**

1. USB3Tp3/USB3Tn3 and USB3Rp3/USB3Rn3 signals are multiplexed with PETp1/PETn1 and PERp1/PERn1 signals respectively.
2. USB3Tp4/USB3Tn4 and USB3Rp4/USB3Rn4 signals are multiplexed with PETp2/PETn2 and PERp2/PERn2 signals respectively.
3. SATA\_TXP3/SATA\_TXN3 and SATA\_RXP3/SATA\_RXN3 signals are multiplexed with PETp6\_L0/PETn6\_L0 and PERp6\_L0/PERn6\_L0 signals respectively.
4. SATA\_TXP2/SATA\_TXN2 and SATA\_RXP2/SATA\_RXN2 signals are multiplexed with PETp6\_L1/PETn6\_L1 and PERp6\_L1/PERn6\_L1 signals respectively.
5. SATA\_TXP1/SATA\_TXN1 and SATA\_RXP1/SATA\_RXN1 signals are multiplexed with PETp6\_L2/PETn6\_L2 and PERp6\_L2/PERn6\_L2 signals respectively.
6. SATA\_TXP0/SATA\_TXN0 and SATA\_RXP0/SATA\_RXN0 signals are multiplexed with PETp6\_L3/PETn6\_L3 and PERp6\_L3/PERn6\_L3 signals respectively.
7. The total number of PCIe\* ports on the platform must not exceed 6. System designer needs to take this into account when configuring the flexible I/O on the platform.
8. The Intel® Ethernet Network Connection I218LM/V Platform LAN Connect Device can be connected to any non-multiplexed (fixed) PCI Express\* port on the PCH.



## 5.21 SMBus Controller (D31:F3)

The PCH provides an System Management Bus (SMBus) 2.0 host controller as well as an SMBus Slave Interface. The host controller provides a mechanism for the processor to initiate communications with SMBus peripherals (slaves). The PCH is also capable of operating in a mode in which it can communicate with I<sup>2</sup>C compatible devices. The host SMBus controller supports up to 100 KHz clock speed.

The PCH can perform SMBus messages with either packet error checking (PEC) enabled or disabled. The actual PEC calculation and checking is performed in hardware by the PCH.

The Slave Interface allows an external master to read from or write to the PCH. Write cycles can be used to cause certain events or pass messages, and the read cycles can be used to determine the state of various status bits. The PCH's internal host controller cannot access the PCH's internal Slave Interface.

The PCH SMBus logic exists in D31:F3 configuration space, and consists of a transmit data path and host controller. The transmit data path provides the data flow logic needed to implement the seven different SMBus command protocols and is controlled by the host controller. The PCH's SMBus controller logic is clocked by the RTC clock.

The SMBus Address Resolution Protocol (ARP) is supported by using the existing host controller commands through software, except for the Host Notify command (which is actually a received message).

The programming model of the host controller is combined into two portions: a PCI configuration portion, and a system I/O mapped portion. All static configuration, such as the I/O base address, is accomplished using the PCI configuration space. Real-time programming of the Host interface is accomplished in system I/O space.

The PCH SMBus host controller checks for parity errors as a target. If an error is detected, the detected parity error bit in the PCI Status register (D31:F3:Offset 06h:Bit 15) is set. If Bit 6 and Bit 8 of the PCI Command register (D31:F3:Offset 04h) are set, an SERR# is generated and the signaled SERR# bit in the PCI Status register (bit 14) is set.

### 5.21.1 Host Controller

The SMBus host controller is used to send commands to other SMBus slave devices. Software sets up the host controller with an address, command, and, for writes, data and optional PEC; and then tells the controller to start. When the controller has finished transmitting data on writes, or receiving data on reads, it generates an SMI# or interrupt, if enabled.

The host controller supports 8 command protocols of the SMBus interface (see *System Management Bus (SMBus) Specification*, Version 2.0): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, Block Write-Block Read Process Call, and Host Notify.

The SMBus host controller requires that the various data and command fields be setup for the type of command to be sent. When software sets the START bit, the SMBus Host controller performs the requested transaction, and interrupts the processor (or generates an SMI#) when the transaction is completed. Once a START command has been issued, the values of the "active registers" (Host Control, Host Command, Transmit Slave Address, Data 0, Data 1) should not be changed or read until the

interrupt status message (INTR) has been set (indicating the completion of the command). Any register values needed for computation purposes should be saved prior to issuing of a new command, as the SMBus host controller updates all registers while completing the new command.

The PCH supports the *System Management Bus (SMBus) Specification, Version 2.0*. Slave functionality, including the Host Notify protocol, is available on the SMBus pins. The SMLink and SMBus signals can be tied together externally, depending on TCO mode used. Refer to [Section 5.12.2](#) for more details.

Using the SMBus host controller to send commands to the PCH SMBus slave port is not supported.

### 5.21.1.1 Command Protocols

In all of the following commands, the Host Status register (offset 00h) is used to determine the progress of the command. While the command is in operation, the HOST\_BUSY bit is set. If the command completes successfully, the INTR bit will be set in the Host Status register. If the device does not respond with an acknowledge, and the transaction times out, the DEV\_ERR bit is set. If software sets the KILL bit in the Host Control register while the command is running, the transaction will stop and the FAILED bit will be set.

#### Quick Command

When programmed for a Quick Command, the Transmit Slave Address register is sent. The PEC byte is never appended to the Quick Protocol. Software should force the PEC\_EN bit to 0 when performing the Quick Command. Software must force the I2C\_EN bit to 0 when running this command. See section 5.5.1 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

#### Send Byte/Receive Byte

For the Send Byte command, the Transmit Slave Address and Device Command registers are sent. For the Receive Byte command, the Transmit Slave Address register is sent. The data received is stored in the DATA0 register. Software must force the I2C\_EN bit to 0 when running this command.

The Receive Byte is similar to a Send Byte; the only difference is the direction of data transfer. See sections 5.5.2 and 5.5.3 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

#### Write Byte/Word

The first byte of a Write Byte/Word access is the command code. The next 1 or 2 bytes are the data to be written. When programmed for a Write Byte/Word command, the Transmit Slave Address, Device Command, and Data0 registers are sent. In addition, the Data1 register is sent on a Write Word command. Software must force the I2C\_EN bit to 0 when running this command. See section 5.5.4 of the *System Management Bus (SMBus) Specification, Version 2.0* for the format of the protocol.

#### Read Byte/Word

Reading data is slightly more complicated than writing data. First the PCH must write a command to the slave device. Then it must follow that command with a repeated start condition to denote a read from that device's address. The slave then returns 1 or 2 bytes of data. Software must force the I2C\_EN bit to 0 when running this command.

When programmed for the read byte/word command, the Transmit Slave Address and Device Command registers are sent. Data is received into the DATA0 on the read byte, and the DATA0 and DATA1 registers on the read word. See section 5.5.5 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

### Process Call

The process call is so named because a command sends data and waits for the slave to return a value dependent on that data. The protocol is simply a Write Word followed by a Read Word, but without a second command or stop condition.

When programmed for the Process Call command, the PCH transmits the Transmit Slave Address, Host Command, DATA0 and DATA1 registers. Data received from the device is stored in the DATA0 and DATA1 registers. The Process Call command with I2C\_EN set and the PEC\_EN bit set produces undefined results. Software must force either I2C\_EN or PEC\_EN to 0 when running this command. See section 5.5.6 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

**Note:** For the process call command, the value written into bit 0 of the Transmit Slave Address register (SMBus I/O register, Offset 04h) needs to be 0.

**Note:** If the I2C\_EN bit is set, the protocol sequence changes slightly: the Command Code (Bits 18:11 in the bit sequence) are not sent; as a result, the slave will not acknowledge (Bit 19 in the sequence).

### Block Read/Write

The PCH contains a 32-byte buffer for read and write data that can be enabled by setting bit 1 of the Auxiliary Control register at offset 0Dh in I/O space, as opposed to a single byte of buffering. This 32-byte buffer is filled with write data before transmission, and filled with read data on reception. In the PCH, the interrupt is generated only after a transmission or reception of 32 bytes, or when the entire byte count has been transmitted/received.

**Note:** When operating in I<sup>2</sup>C mode (I2C\_EN bit is set), the PCH will never use the 32-byte buffer for any block commands.

The byte count field is transmitted but ignored by the PCH as software will end the transfer after all bytes it cares about have been sent or received.

For a Block Write, software must either force the I2C\_EN bit or both the PEC\_EN and AAC bits to 0 when running this command.

The block write begins with a slave address and a write condition. After the command code, the PCH issues a byte count describing how many more bytes will follow in the message. If a slave had 20 bytes to send, the first byte would be the number 20 (14h), followed by 20 bytes of data. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

When programmed for a block write command, the Transmit Slave Address, Device Command, and Data0 (count) registers are sent. Data is then sent from the Block Data Byte register; the total data sent being the value stored in the Data0 register. On block read commands, the first byte received is stored in the Data0 register, and the remaining bytes are stored in the Block Data Byte register. See section 5.5.7 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

**Note:** For Block Write, if the I2C\_EN bit is set, the format of the command changes slightly. The PCH will still send the number of bytes (on writes) or receive the number of bytes (on reads) indicated in the DATA0 register. However, it will not send the contents of the DATA0 register as part of the message. Also, the Block Write protocol sequence changes slightly. The Byte Count (bits 27:20 in the bit sequence) are not sent; as a result, the slave will not acknowledge (bit 28 in the sequence).

### I<sup>2</sup>C\* Read

This command allows the PCH to perform block reads to certain I<sup>2</sup>C devices, such as serial E<sup>2</sup>PROMs. The SMBus Block Read supports the 7-bit addressing mode only.

However, this does not allow access to devices using the I<sup>2</sup>C "Combined Format" that has data bytes after the address. Typically, these data bytes correspond to an offset (address) within the serial memory chips.

**Note:** This command is supported independent of the setting of the I2C\_EN bit. The I<sup>2</sup>C Read command with the PEC\_EN bit set produces undefined results. Software must force both the PEC\_EN and AAC bit to 0 when running this command.

For the I<sup>2</sup>C Read command, the value written into bit 0 of the Transmit Slave Address register (SMBus I/O register, offset 04h) needs to be 0.

The format that is used for the command is shown in Table 5-41.

**Table 5-41. I<sup>2</sup>C\* Block Read**

Bit	Description
1	Start
8:2	Slave Address – 7 bits
9	Write
10	Acknowledge from slave
18:11	Send DATA1 register
19	Acknowledge from slave
20	Repeated Start
27:21	Slave Address – 7 bits
28	Read
29	Acknowledge from slave
37:30	Data byte 1 from slave – 8 bits
38	Acknowledge
46:39	Data byte 2 from slave – 8 bits
47	Acknowledge
–	Data bytes from slave/Acknowledge
–	Data byte N from slave – 8 bits
–	NOT Acknowledge
–	Stop

The PCH will continue reading data from the peripheral until the NAK is received.



### Block Write–Block Read Process Call

The block write-block read process call is a two-part message. The call begins with a slave address and a write condition. After the command code the host issues a write byte count (M) that describes how many more bytes will be written in the first part of the message. If a master has 6 bytes to send, the byte count field will have the value 6 (0000 0110b), followed by the 6 bytes of data. The write byte count (M) cannot be 0.

The second part of the message is a block of read data beginning with a repeated start condition followed by the slave address and a Read bit. The next byte is the read byte count (N), which may differ from the write byte count (M). The read byte count (N) cannot be 0.

The combined data payload must not exceed 32 bytes. The byte length restrictions of this process call are summarized as follows:

- $M \geq 1$  byte
- $N \geq 1$  byte
- $M + N \leq 32$  bytes

The read byte count does not include the PEC byte. The PEC is computed on the total message beginning with the first slave address and using the normal PEC computational rules. It is highly recommended that a PEC byte be used with the Block Write-Block Read Process Call. Software must do a read to the command register (offset 2h) to reset the 32-byte buffer pointer prior to reading the block data register.

**Note:** There is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

**Note:** E32B bit in the Auxiliary Control register must be set when using this protocol.

See section 5.5.8 of the *System Management Bus (SMBus) Specification*, Version 2.0 for the format of the protocol.

## 5.21.2 Bus Arbitration

Several masters may attempt to get on the bus at the same time by driving the SMBDATA line low to signal a start condition. The PCH continuously monitors the SMBDATA line. When the PCH is attempting to drive the bus to a 1 by letting go of the SMBDATA line, and it samples SMBDATA low, then some other master is driving the bus and the PCH will stop transferring data.

If the PCH sees that it has lost arbitration, the condition is called a collision. The PCH will set the BUS\_ERR bit in the Host Status register, and if enabled, generate an interrupt or SMI#. The processor is responsible for restarting the transaction.

When the PCH is a SMBus master, it drives the clock. When the PCH is sending address or command as an SMBus master, or data bytes as a master on writes, it drives data relative to the clock it is also driving. It will not start toggling the clock until the start or stop condition meets proper setup and hold time. The PCH will also ensure minimum time between SMBus transactions as a master.

**Note:** The PCH supports the same arbitration protocol for both the SMBus and the System Management (SMLink) interfaces.

## 5.21.3 Bus Timing

### 5.21.3.1 Clock Stretching

Some devices may not be able to handle their clock toggling at the rate that the PCH as an SMBus master would like. They have the capability of stretching the low time of the clock. When the PCH attempts to release the clock (allowing the clock to go high), the clock will remain low for an extended period of time.

The PCH monitors the SMBus clock line after it releases the bus to determine whether to enable the counter for the high time of the clock. While the bus is still low, the high time counter must not be enabled. Similarly, the low period of the clock can be stretched by an SMBus master if it is not ready to send or receive data.

### 5.21.3.2 Bus Timeout (PCH as SMBus Master)

If there is an error in the transaction, such that an SMBus device does not signal an acknowledge, or holds the clock lower than the allowed Timeout time, the transaction will time out. The PCH will discard the cycle and set the DEV\_ERR bit. The timeout minimum is 25 ms (800 RTC clocks). The Timeout counter inside the PCH will start after the last bit of data is transferred by the PCH and it is waiting for a response.

The 25-ms Timeout counter will not count under the following conditions:

1. BYTE\_DONE\_STATUS bit (SMBus I/O Offset 00h, Bit 7) is set
2. The SECOND\_TO\_STS bit (TCO I/O Offset 06h, Bit 1) is not set (this indicates that the system has not locked up).

## 5.21.4 Interrupts/SMI#

The PCH SMBus controller uses PIRQB# as its interrupt pin. However, the system can alternatively be set up to generate SMI# instead of an interrupt, by setting the SMBUS\_SMI\_EN bit (D31:F0:Offset 40h:Bit 1).

Table 5-42, Table 5-43 and Table 5-44 specify how the various enable bits in the SMBus function control the generation of the interrupt, Host and Slave SMI, and Wake internal signals. The rows in the tables are additive, which means that if more than one row is true for a particular scenario, then the Results for all of the activated rows will occur.

**Table 5-42. Enable for SMBALERT#**

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit 1)	SMBALERT_DIS (Slave Command I/O Register, Offset 11h, Bit 2)	Result
SMBALERT# asserted low (always reported in Host Status Register, Bit 5)	X	X	X	Wake generated
	X	1	0	Slave SMI# generated (SMBUS_SMI_STS)
	1	0	0	Interrupt generated

**Table 5-43. Enables for SMBus Slave Write and SMBus Host Events**

Event	INTREN (Host Control I/O Register, Offset 02h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Offset 40h, Bit 1)	Event
Slave Write to Wake/SMI# Command	X	X	Wake generated when asleep. Slave SMI# generated when awake (SMBUS_SMI_STS).
Slave Write to SMLINK_SLAVE_SMI Command	X	X	Slave SMI# generated when in the S0 state (SMBUS_SMI_STS)
Any combination of Host Status Register [4:1] asserted	0	X	None
	1	0	Interrupt generated
	1	1	Host SMI# generated

**Table 5-44. Enables for the Host Notify Command**

HOST_NOTIFY_INTREN (Slave Control I/O Register, Offset 11h, Bit 0)	SMB_SMI_EN (Host Configuration Register, D31:F3:Off40h, Bit 1)	HOST_NOTIFY_WKEN (Slave Control I/O Register, Offset 11h, Bit 1)	Result
0	X	0	None
X	X	1	Wake generated
1	0	X	Interrupt generated
1	1	X	Slave SMI# generated (SMBUS_SMI_STS)

## 5.21.5 SMBALERT#

SMBALERT# is multiplexed with GPIO11. When enable and the signal is asserted, the PCH can generate an interrupt, an SMI#, or a wake event from S1 – S5.

## 5.21.6 SMBus CRC Generation and Checking

If the AAC bit is set in the Auxiliary Control register, the PCH automatically calculates and drives CRC at the end of the transmitted packet for write cycles, and will check the CRC for read cycles. It will not transmit the contents of the PEC register for CRC. The PEC bit must not be set in the Host Control register. If this bit is set, unspecified behavior will result.

If the read cycle results in a CRC error, the DEV\_ERR bit and the CRCE bit in the Auxiliary Status register at Offset 0Ch will be set.

## 5.21.7 SMBus Slave Interface

The PCH SMBus Slave interface is accessed using the SMBus. The SMBus slave logic will not generate or handle receiving the PEC byte and will only act as a Legacy Alerting Protocol device. The slave interface allows the PCH to decode cycles, and allows an external microcontroller to perform specific actions. Key features and capabilities include:

- Supports decode of three types of messages: Byte Write, Byte Read, and Host Notify.
- Receive Slave Address register: This is the address that the PCH decodes. A default value is provided so that the slave interface can be used without the processor having to program this register.
- Receive Slave Data register in the SMBus I/O space that includes the data written by the external microcontroller.
- Registers that the external microcontroller can read to get the state of the PCH.
- Status bits to indicate that the SMBus slave logic caused an interrupt or SMI# due to the reception of a message that matched the slave address.
  - Bit 0 of the Slave Status Register for the Host Notify command
  - Bit 16 of the SMI Status Register for all others

**Note:**

The external microcontroller should not attempt to access the PCH SMBus slave logic until either:

- 800 milliseconds after both: RTCRST# is high and RSMRST# is high, OR
- The PLTRST# de-asserts

If a master leaves the clock and data bits of the SMBus interface at 1 for 50  $\mu$ s or more in the middle of a cycle, the PCH slave logic's behavior is undefined. This is interpreted as an unexpected idle and should be avoided when performing management activities to the slave logic.

**Note:**

When an external microcontroller accesses the SMBus Slave Interface over the SMBus a translation in the address is needed to accommodate the least significant bit used for read/write control. For example, if the PCH slave address (RCV\_SLVA) is left at 44h (default), the external micro-controller would use an address of 88h/89h (write/read).

### 5.21.7.1 Format of Slave Write Cycle

The external master performs Byte Write commands to the PCH SMBus Slave interface. The "Command" field (bits 11:18) indicates which register is being accessed. The Data field (bits 20:27) indicates the value that should be written to that register.



Table 5-45 has the values associated with the registers.

**Table 5-45. Slave Write Registers**

Register	Function
0	Command Register. See <a href="#">Table 5-46</a> for valid values written to this register.
1–3	Reserved
4	Data Message Byte 0
5	Data Message Byte 1
6–7	Reserved
8	Reserved
9–FFh	Reserved
<b>Note:</b> The external microcontroller is responsible to make sure that it does not update the contents of the data byte registers until they have been read by the system processor. The PCH overwrites the old value with any new value received. A race condition is possible where the new value is being written to the register just at the time it is being read. The PCH will not attempt to cover this race condition (that is, unpredictable results in this case).	

**Table 5-46. Command Types**

Command Type	Description
0	Reserved
1	<b>WAKE/SMI#.</b> This command wakes the system if it is not already awake. If system is already awake, an SMI# is generated. <b>Note:</b> The SMB_WAK_STS bit will be set by this command, even if the system is already awake. The SMI handler should then clear this bit.
2	<b>Unconditional Powerdown.</b> This command sets the PWRBTNOR_STS bit, and has the same effect as the Powerbutton Override occurring.
3	<b>HARD RESET WITHOUT CYCLING:</b> This command causes a hard reset of the system (does not include cycling of the power supply). This is equivalent to a write to the CF9h register with Bits 2:1 set to 1; but Bit 3 set to 0.
4	<b>HARD RESET SYSTEM.</b> This command causes a hard reset of the system (including cycling of the power supply). This is equivalent to a write to the CF9h register with Bits 3:1 set to 1.
5	<b>Disable the TCO Messages.</b> This command will disable the PCH from sending Heartbeat and Event messages (as described in <a href="#">Section 5.11.14</a> ). Once this command has been executed, Heartbeat and Event message reporting can only be re-enabled by assertion and de-assertion of the RSMRST# signal.
6	<b>WD RELOAD:</b> Reload watchdog timer.
7	Reserved
8	<b>SMLINK_SLV_SMI.</b> When the PCH detects this command type while in the S0 state, it sets the SMLINK_SLV_SMI_STS bit. This command should only be used if the system is in an S0 state. If the message is received during S1 – S5 states, the PCH acknowledges it, but the SMLINK_SLV_SMI_STS bit does not get set. <b>Note:</b> It is possible that the system transitions out of the S0 state at the same time that the SMLINK_SLV_SMI command is received. In this case, the SMLINK_SLV_SMI_STS bit may get set but not serviced before the system goes to sleep. Once the system returns to S0, the SMI associated with this bit would then be generated. Software must be able to handle this scenario.
9–FFh	Reserved.

### 5.21.7.2 Format of Read Command

The external master performs Byte Read commands to the PCH SMBus Slave interface. The "Command" field (bits 18:11) indicates which register is being accessed. The Data field (bits 30:37) contains the value that should be read from that register.

**Table 5-47. Slave Read Cycle Format**

Bit	Description	Driven By	Comment
1	Start	External Microcontroller	
2-8	Slave Address - 7 bits	External Microcontroller	Must match value in Receive Slave Address register
9	Write	External Microcontroller	Always 0
10	ACK	PCH	
11-18	Command code – 8 bits	External Microcontroller	Indicates which register is being accessed. See <a href="#">Table 5-48</a> for a list of implemented registers.
19	ACK	PCH	
20	Repeated Start	External Microcontroller	
21-27	Slave Address - 7 bits	External Microcontroller	Must match value in Receive Slave Address register
28	Read	External Microcontroller	Always 1
29	ACK	PCH	
30-37	Data Byte	PCH	Value depends on register being accessed. See <a href="#">Table 5-48</a> for a list of implemented registers.
38	NOT ACK	External Microcontroller	
39	Stop	External Microcontroller	

**Table 5-48. Data Values for Slave Read Registers**

Register	Bits	Description
0	7:0	Reserved for capabilities indication. Should always return 00h. Future chips may return another value to indicate different capabilities.
1	2:0	System Power State 000 = S0 001 = S1 010 = Reserved 011 = S3 100 = S4 101 = S5 110 = Reserved 111 = Reserved
	7:3	Reserved
2	3:0	Reserved
	7:4	Reserved
3	5:0	<b>Watchdog Timer current value</b> <b>Note:</b> The Watchdog Timer has 10 bits; however, this field is only 6 bits. If the current value is greater than 3Fh, the PCH will always report 3Fh in this field.
	7:6	Reserved
4	0	1 = The <b>Intruder Detect</b> (INTRD_DET) bit is set. This indicates that the system cover has probably been opened.
	1	1 = BTI <b>Temperature Event</b> occurred. This bit will be set if the PCH's THRM# input signal is active. Otherwise, this bit will read "0."
	2	<b>DOA Processor Status.</b> This bit will be 1 to indicate that the processor is dead
	3	1 = <b>SECOND_TO_STS</b> bit set. This bit will be set after the second Timeout (SECOND_TO_STS bit) of the Watchdog Timer occurs.
	6:4	Reserved. Will always be 0, but software should ignore.
	7	Reflects the value of the GPIO11/SMBALERT# pin (and is dependent upon the value of the GPI_INV[11] bit). If the GPI_INV[11] bit is 1, the value in this bit equals the level of the GPI[11]/SMBALERT# pin (high = 1, low = 0). If the GPI_INV[11] bit is 0, the value of this bit will equal the inverse of the level of the GPIO11/SMBALERT# pin (high = 0, low = 1).
5	0	<b>FWH bad bit.</b> This bit will be 1 to indicate that the FWH read returned FFh, which indicates that it is probably blank.
	1	Reserved
	2	<b>SYS_PWROK Failure Status:</b> This bit will be 1 if the SYSPWR_FLR bit in the GEN_PMCN_2 register is set.
	3	Reserved
	4	Reserved
	5	POWER_OK_BAD: Indicates the failure core power well ramp during boot/resume. This bit will be active if the SLP_S3# pin is de-asserted and PCH_PWROK pin is not asserted.
	6	Thermal Trip: This bit will shadow the state of processor Thermal Trip status bit (CTS) (16.2.1.2, GEN_PMCN_2, bit 3). Events on signal will not create a event message
	7	Reserved: Default value is "X" <b>Note:</b> Software should not expect a consistent value when this bit is read through SMBUS/SMLink
6	7:0	Contents of the Message 1 register.
7	7:0	Contents of the Message 2 register.
8	7:0	Contents of the TCO_WDCNT register.
9	7:0	Seconds of the RTC
A	7:0	Minutes of the RTC
B	7:0	Hours of the RTC
C	7:0	"Day of Week" of the RTC
D	7:0	"Day of Month" of the RTC
E	7:0	Month of the RTC
F	7:0	Year of the RTC
10h-FFh	7:0	Reserved

#### 5.21.7.2.1 Behavioral Notes

According to SMBus protocol, Read and Write messages always begin with a Start bit—Address—Write bit sequence. When the PCH detects that the address matches the value in the Receive Slave Address register, it will assume that the protocol is always followed and ignore the Write bit, (bit 9) and signal an Acknowledge during bit 10. In other words, if a Start—Address—Read occurs (which is invalid for SMBus Read or Write protocol), and the address matches the PCH’s Slave Address, the PCH will still grab the cycle.

Also according to SMBus protocol, a Read cycle contains a Repeated Start—Address—Read sequence beginning at Bit 20. Once again, if the Address matches the PCH’s Receive Slave Address, it will assume that the protocol is followed, ignore bit 28, and proceed with the Slave Read cycle.

**Note:**

An external microcontroller must not attempt to access the PCH’s SMBus Slave logic until at least 1 second after both RTCRST# and RSMRST# are de-asserted (high).

#### 5.21.7.3 Slave Read of RTC Time Bytes

The PCH SMBus slave interface allows external SMBus master to read the internal RTC’s time byte registers.

The RTC time bytes are internally latched by the PCH’s hardware whenever RTC time is not changing and SMBus is idle. This ensures that the time byte delivered to the slave read is always valid and it does not change when the read is still in progress on the bus. The RTC time will change whenever a hardware update is in progress, or there is a software write to the RTC time bytes.

The PCH SMBus slave interface only supports Byte Read operation. The external SMBus master will read the RTC time bytes, one after another. It is the responsibility of software to check and manage the possible time rollover when subsequent time bytes are read.

For example, assuming the RTC time is 11 hours: 59 minutes: 59 seconds. When the external SMBus master reads the hour as 11, then proceeds to read the minute, it is possible that the rollover happens between the reads and the minute is read as 0. This results in 11 hours: 0 minute instead of the correct time of 12 hours: 0 minutes. Unless it is certain that rollover will not occur, software is required to detect the possible time rollover by reading multiple times such that the read time bytes can be adjusted accordingly if needed.

#### 5.21.7.4 Format of Host Notify Command

The PCH tracks and responds to the standard Host Notify command as specified in the *System Management Bus (SMBus) Specification*, Version 2.0. The host address for this command is fixed to 0001000b. If the PCH already has data for a previously-received host notify command that has not been serviced yet by the host software (as indicated by the HOST\_NOTIFY\_STS bit), then it will NACK following the host address byte of the protocol. This allows the host to communicate non-acceptance to the master and retain the host notify address and data values for the previous cycle until host software completely services the interrupt.

**Note:**

Host software must always clear the HOST\_NOTIFY\_STS bit after completing any necessary reads of the address and data registers.

Table 5-49 shows the Host Notify format.

**Table 5-49. Host Notify Format**

Bit	Description	Driven By	Comment
1	Start	External Master	
8:2	SMBus Host Address – 7 bits	External Master	Always 0001_000
9	Write	External Master	Always 0
10	ACK (or NACK)	PCH	PCH NACKs if HOST_NOTIFY_STS is 1
17:11	Device Address – 7 bits	External Master	Indicates the address of the master; loaded into the Notify Device Address Register
18	Unused – Always 0	External Master	7-bit-only address; this bit is inserted to complete the byte
19	ACK	PCH	
27:20	Data Byte Low – 8 bits	External Master	Loaded into the Notify Data Low Byte Register
28	ACK	PCH	
36:29	Data Byte High – 8 bits	External Master	Loaded into the Notify Data High Byte Register
37	ACK	PCH	
38	Stop	External Master	

## 5.22 Intel® Serial I/O I<sup>2</sup>C\* Controllers (D21:F1,F2)

### 5.22.1 Overview and Features

There are two I<sup>2</sup>C controllers for two independent I<sup>2</sup>C interfaces. Each interface is a two-wire I<sup>2</sup>C serial interface consisting of a serial data line (SDA) and a serial clock (SCL).

The I<sup>2</sup>C interfaces support the following features:

- Speed: standard mode (up to 100Kb/s), fast mode (up to 400Kb/s), and fast mode plus (up to 1MB/s).
- 1.8V or 3.3V support (configured by means of the BIOS)
- Master I<sup>2</sup>C operation only. I<sup>2</sup>C slave not supported.
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers
- Bulk transmit mode
- Ignoring CBUS addresses
- Interrupt or polled-mode operation
- Bit and Byte waiting at all bus speed
- Component parameters for configurable software driver support
- Programmable SDA hold time ( $t_{HD}$ ; DAT)

**Note:** High speed mode (up to 3.4MB/s) not supported.

**Note:** For details on supported OS, refer to the Intel® Serial IO Bus Drivers Product Requirements Document (PRD). Refer to IBL/CDI document 526515.

## 5.22.2 Protocols

The I<sup>2</sup>C controllers are designed to be compliant with I<sup>2</sup>C protocols specified in the industry I<sup>2</sup>C specification, version 2.1. Refer the I<sup>2</sup>C specification for more information on the protocols and command formats.

Below is a simplified description of I<sup>2</sup>C bus operation:

- The master generates a START condition, signaling all devices on the bus to listen for data.
- The master writes a 7-bit address, followed by a read/write bit to select the target device and to define whether it is a transmitter or a receiver.
- The target device sends an acknowledge bit over the bus. The master must read this bit to determine whether the addressed target device is on the bus.
- Depending on the value of the read/write bit, any number of 8-bit messages can be transmitted or received by the master. These messages are specific to the I<sup>2</sup>C device used. After 8 message bits are written to the bus, the transmitter will receive an acknowledge bit. This message and acknowledge transfer continues until the entire message is transmitted.
- The message is terminated by the master with a STOP condition. This frees the bus for the next master to begin communications.

### 5.22.2.1 Combined Formats

The PCH controllers support mixed read and write combined format transactions in both 7-bit and 10-bit addressing modes.

The PCH controllers do not support mixed address and mixed address format (which means a 7-bit address transaction followed by a 10-bit address transaction or vice versa) combined format transaction.

to initiate combined format transfers, IC\_CON.IC\_RESTSTART\_EN should be set to 1. With this value set and operating as a master, when the controller completes an I<sup>2</sup>C transfer, it checks the transmit FIFO and executes the next transfer. If the direction of this transfer differs from the previous transfer, the combined format is used to issue the transfer. If the transmit FIFO is empty when the current I<sup>2</sup>C transfer completes, a STOP is issued and the next transfer is issued following a START condition.

## 5.22.3 DMA Controller Interface

The I<sup>2</sup>C Controller has an optional built-in DMA handshaking interface to an internal DMA Controller. The interface can be used to request and control transfers.

To enable the DMA Controller interface on the I<sup>2</sup>C controller, software must write to the DMA Control register (D21:F1/2:Offset 88h). Writing a 1 into the Transmit DMA Enable bit field of Control register enables the controller transmit handshaking interface. Writing a 1 into the Receive DMA Enable bit field enables the controller receive handshaking interface.



## 5.22.4 Device Power Down Support

To power down peripherals connected to PCH I<sup>2</sup>C bus, the PCH will drive the I<sup>2</sup>C output signal to tri-state and ignore the inputs. I/O isolation logic is implemented to condition the I/O as platform connected devices move between D3<sub>HOT</sub> and D3<sub>COLD</sub> (power off) states. The control of the power isolation is through the Peripherals Private register.

## 5.22.5 Power Management

Each I<sup>2</sup>C interface will support hardware managed clock gating and Runtime D3 functional clock gating mechanism. Power gating of the I<sup>2</sup>C interface is not supported.

### 5.22.5.1 Hardware Managed

The I<sup>2</sup>C controller hardware provides Idle Detection logic that will be used to locally gate the controller's clocks.

### 5.22.5.2 Runtime D3

The I<sup>2</sup>C controller supports Runtime D3.

**Note:** The I<sup>2</sup>C controller will not be placed into the D3<sub>HOT</sub> state until the I<sup>2</sup>C controller is fully idle.

### 5.22.5.3 Latency Tolerance Reporting (LTR)

To support Intel Power Optimization, the PCH I<sup>2</sup>C controller supports the LTR mechanism by means of an LTR register.

Latency Tolerance Reporting is used to allow the system to make better choices on which power state to choose. For example, the system should not enter a power state that has an exit latency that is longer than the latency tolerance of an I/O stream. Each interface module supports this by reporting the latency tolerance.

There are two options for how LTR will be handled:

1. In the standard mode, the software will write to the host controllers software LTR register. It is the responsibility of software to update the LTR with the appropriate value based on the bus data rate.
2. In the auto mode, the BIOS will write to the "host controllers Auto LTR Active Value" register and software LTR register.
  - a. When the host controller goes active, the reported LTR value will be the value in the Auto LTR register.
  - b. When the host controller goes inactive (idle), the reported LTR value will be taken from the software LTR register.

## 5.22.6 Interrupts

Each I<sup>2</sup>C interface has an interrupt line that is used to notify the driver that service is required. Each interrupt line is assigned to interrupt PCI INT [A-D] or ACPI IRQ[5-7,13].

## 5.22.7 Error Handling

Errors that might occur on the external I<sup>2</sup>C signals are comprehended by the I<sup>2</sup>C host controller and reported to the I<sup>2</sup>C bus driver through the MMIO registers.

## 5.22.8 Programmable SDA Hold Time

The I<sup>2</sup>C specification requires 300 ns of hold time on the SDA (data line) signal ( $t_{HD;DAT}$ ) in standard and fast speed modes, and a hold time long enough to bridge the undefined part between logic 1 and logic 0 of the falling edge of SCL (clock) in high speed mode.

Board delays on the SCL and SDA signals can mean that the hold time requirement is met at the I<sup>2</sup>C master, but not at the I<sup>2</sup>C slave (or vice versa). As each application will encounter different board delays, the I<sup>2</sup>C controller contains a software programmable register (IC\_SDA\_HOLD, TDB bit) to enable dynamic adjustment of the SDA hold time.

# 5.23 Thermal Management

## 5.23.1 Thermal Sensor

The PCH incorporates one on-die Digital Thermal Sensor (DTS) for thermal management. The thermal sensor can provide PCH temperature information to an EC or SIO device that can be used to determine how to control the fans.

**Note:** Some parts can read down to 43 °C but this is part to part dependent.

This thermal sensor is located near the OPI interface. The on-die thermal sensor is placed as close as possible to the hottest on-die location to reduce thermal gradients and to reduce the error on the sensor trip thresholds. The thermal sensor trip points may be programmed to generate various interrupts including SCI, SMI, and other General Purpose events.

### 5.23.1.1 Internal Thermal Sensor Operation

The internal thermal sensor reports four trip points: Aux2, Aux, Hot, and Catastrophic trip points in the order of increasing temperature.

#### Aux, Aux2 Temperature Trip Points

These trip points may be set dynamically if desired and provides an interrupt to ACPI (or other software) when it is crossed in either direction. These auxiliary temperature trip points do not automatically cause any hardware throttling but may be used by software to trigger interrupts. This trip point is set below the Hot temperature trip point and responses are separately programmable from the hot temperature settings, in order to provide incrementally more aggressive actions. Aux and Aux2 trip points are fully software programmable during system runtime. Aux2 trip point is set below the Aux temperature trip point.



### Hot Temperature Trip Point

This trip point may be set dynamically if desired and provides an interrupt to ACPI (or other software) when it is crossed in either direction. Software could optionally set this as an Interrupt when the temperature exceeds this level setting. Hot trip does not provide any default hardware-based thermal throttling, and is available only as a customer configurable interrupt when  $T_{j,max}$  has been reached.

### Catastrophic Trip Point

This trip point is set at the temperature at which the PCH must be shut down immediately without any software support. The catastrophic trip point must correspond to a temperature ensured to be functional in order for the interrupt generation and Hardware response. Hardware response using THRMTRIP# would be an unconditional transition to S5. The catastrophic transition to the S5 state does not enforce a minimum time in the S5 state. It is assumed that the S5 residence and the reboot sequence cools down the system. If the catastrophic condition remains when the catastrophic power down enable bit is set by BIOS, then the system will re-enter S5.

### Thermometer Mode

The thermometer is implemented using a counter that starts at 0 and increments during each sample point until the comparator indicates the temperature is above the current value. The value of the counter is loaded into a read-only register (Thermal Sensor Thermometer Read) when the comparator first trips.

#### 5.23.1.1.1 Recommended Programming for Available Trip Points

There may be a  $\pm 2$  °C offset due to thermal gradient between the hot-spot and the location of the thermal sensor. Trip points should be programmed to account for this temperature offset between the hot-spot  $T_{j,max}$  and the thermal sensor.

**Aux Trip Points** should be programmed for software and firmware control using interrupts.

**Hot Trip Point** should be set to throttle at 108 °C ( $T_{j,max}$ ) due to DTS trim accuracy adjustments. Hot trip points should also be programmed for a software response.

Catastrophic Trip Point should be set to halt operation to avoid maximum  $T_j$  of about 120 °C.

**Note:**

Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register that can be programmed to select the type of interrupt to be generated. Crossing a trip point is implemented as edge detection on each trip point to generate the interrupts.

$T_{accuracy}$  for the PCH is  $\pm 5$  °C in the temperature range 90 – 120 °C.  $T_{accuracy}$  is  $\pm 10$  °C for temperatures from 45 – 90 °C. The PCH may not operate above +108 °C. This value is based on product characterization and is not ensured by manufacturing test.

Software has the ability to program the Tcat, Thot, and Taux trip points, but these trip points should be selected with consideration for the thermal sensor accuracy and the quality of the platform thermal solution. Overly conservative (unnecessarily low) temperature settings may unnecessarily degrade performance due to frequent throttling, while overly aggressive (dangerously high) temperature settings may fail to protect the part against permanent thermal damage.

## 5.23.2 PCH Thermal Throttling

Occasionally the PCH may operate in conditions that exceed its maximum operating temperature. To protect itself and the system from thermal failure, the PCH is capable of reducing its overall power consumption and as a result, lower its temperature. This is achieved by:

- Forcing the SATA device and interface into a lower power state
- Reducing the number of active lanes on the OPI interface
- Reducing the Intel® Management Engine (Intel® ME) clock frequency
- Forcing the PCIe device and interface into a low power state with the enabling of dynamic Rx and Tx link throttling

The severity of the throttling response is defined by four global PCH throttling states referred to as T-states. In each T-state, the throttling response will differ per interface, but will operate concurrently when a global T-state is activated. A T-state corresponds to a temperature range. The T-states are defined in [Table 5-50](#).

**Table 5-50. PCH Thermal Throttle States (T-States)**

State	Description
T0	Normal operation, temperature is less than the T1 trip point temperature
T1	Temperature is greater than or equal to the T1 trip point temperature, but less than the T2 trip point temperature. The default temperature is $T_{j,max}$ at 108 °C
T2	Temperature is greater than or equal to the T2 trip point temperature, but less than the T3 trip point temperature. The default temperature is 112 °C
T3	Temperature is greater than or equal to the T3 trip point temperature. The default temperature is 116 °C

Enabling of this feature requires appropriate Intel® Management Engine firmware and configuration of the following registers shown in [Table 5-51](#).

**Table 5-51. PCH Thermal Throttling Configuration Registers**

Register Name	Register Location
TL—Throttle Level	TBARB+40h

### 5.23.3 Thermal Reporting Over System Management Link 1 Interface (SMLink1)

SMLink1 interface in the PCH is the SMBus link to an optional external controller. A SMBus protocol is defined on the PCH to allow compatible devices such as Embedded Controller (EC) or SIO to obtain system thermal data from PCH sensors using the SMLink1 interface. The sensors that can be monitored using the SMLink1 include those in the processor, PCH, and DIMMs with sensors implemented. This solution allows an external device or controller to use the system thermal data for system thermal management.

**Note:** To enable Thermal Reporting, Enable TS (see [Section 19.2.4](#)) and Enable SMBus Temperature Reporting (see [Section 19.2.5](#)) bits need to be enabled.

There are two uses for PCH thermal reporting capability:

1. To provide system thermal data to an external controller. The controller can manage the fans and other cooling elements based on this data. In addition, the PCH can be programmed by setting appropriate bits in the Catastrophic Trip Point register (see [Section 19.2.7](#)), Thermal Alert high Value register (see [Section 19.2.8](#)) or the Thermal Alert Low Value register (see [Section 19.2.9](#)) to alert the controller when a device has gone outside of its temperature limits. The alert causes the assertion of the PCH TEMP\_ALERT# (SML1ALERT#/TEMP\_ALERT#/GPIO73) signal. See [Section 5.23.3.5](#) for more details.
2. To provide an interface between the external controller and host software. This software interface has no direct affect on the PCH's thermal collection. It is strictly a software interface to pass information or data.

The PCH responds to thermal requests only when the system is in S0 or S1. Once the PCH has been programmed, it will start responding to a request while the system is in S0 or S1.

To implement this thermal reporting capability, the platform is required to have appropriate BIOS support and compatible devices that support the SMBus protocol.

#### 5.23.3.1 Block Read Address

The PCH supports the Block Read Address for reads. This address is used for reads from the PCH.

- The address is set by soft straps or BIOS. It can be set to any value the platform requires.
- This address only supports SMBus Block Read command and not Byte or Word Read.
- The Block Read command is supported as defined in the SMBus 2.0 specification, with the command being 40h, and the byte count being provided by the PCH following the block read format in the SMBus specification.
- Writes are not allowed to this address, and result in indeterminate behavior.
- Packet Error Code (PEC) may be enabled or not, which is set up by BIOS.

### 5.23.3.2 Block Read Command

The external controller may read thermal information from the PCH using the SMBus Block Read Command. Byte-read and Word-read SMBus commands are not supported.

**Note:** The reads use a different address than the writes.

The command format follows the Block Read format of the SMBus specification.

The PCH returns a single byte of data, indicating the temperature between 0 °C (0x00) and 254 °C (0xFE). A read of 0xFF indicates that the sensor is not yet enabled. For more information, see [Section 5.23.3.1](#).

### 5.23.3.3 Read Data Format

For each of the data fields, an ERROR Code is listed below. This code indicates that the PCH failed in its access to the device. This would be for the case where the read returned no data, or some invalid value. In general that would mean the device is broken. The EC can treat the device that failed the read as broken or with some fail-safe mechanism.

#### 5.23.3.1 PCH Temperature

The temperature readings for the PCH are 8-bit unsigned values from 0 – 255. The minimum granularity supported by the internal thermal sensor is 1 °C. Thus, there are no fractional values for the PCH temperatures. The device returns a temperature between 0 °C (0x00) and 254 °C (0xFE). Devices that are not yet enabled, return the value 0xFF.

**Note:** Sensors used within the components do not support values below 0 °C; thus, this field is treated as 8-bits (0 – 255) absolute.

#### 5.23.3.4 Thermal Data Update Rate

The temperature values are updated every 1 ms in the PCH; thus, reading more often than that simply returns the same data multiple times. Also, the data may be up to 1 ms old if the external controller reads the data right before the next update window.

#### 5.23.3.5 Temperature Comparator and Alert

The PCH has the ability to alert the external controller when temperatures are out of range. This is accomplished using the PCH TEMP\_ALERT# signal. The alert is a simple comparator. If any device's temperature is outside the limit range for that device, the signal is asserted (electrical low).

**Note:** This alert does not use the SML1ALERT#.

The PCH supports 2 ranges: an upper and lower limit (8-bits each, in °C) for the PCH temperature.

The comparator checks if the device is within the specified range, including the limits. For example, a device that is at 100 °C when the upper limit is 100 °C will not trigger the alert. Likewise, a device that is at 70 °C when the lower limit is 70 °C will not trigger the alert.

The compares are done only on devices that have been enabled by BIOS for checking.



The compares are done in firmware, so all the compares are executed in one software loop and at the end, if there is any out of bound temperature, the PCH TEMP\_ALERT# signal is asserted.

When the external controller sees the TEMP\_ALERT# signal low, it knows the device is out of range. It can read the temperature and then change the limit for the device.

**Note:**

It may take up to 250 ms before the actual writes cause the signal to change state. For instance, if the PCH is at 105 °C and the limit is 100 °C, the alert is triggered. If the controller changes the limits to 110 °C, the TEMP\_ALERT# signal may remain low until the next thermal sampling window (every 1 ms) occurs and only then go high, assuming the PCH was still within its limits.

At boot, the controller can monitor the TEMP\_ALERT# signal state. When BIOS has finished all the initialization and enabled the temperature comparators, the TEMP\_ALERT# signal will be asserted since the default state of the limit registers is 0h; hence, when the PCH first reads temperatures, they will be out of range. This is the positive indication that the external controller may now read thermal information and get valid data. If the TEMP\_ALERT# signal is enabled and not asserted within 30 seconds after PLTRST#, the external controller should assume there is a fatal error and handle accordingly. In general the TEMP\_ALERT# signal will assert within 1 – 4 seconds, depending on the actual BIOS implementation and flow.

**Note:**

The TEMP\_ALERT# assertion is only valid when PLTRST# is de-asserted. The controller should mask the state of this signal when PLTRST# is asserted. Since the controller may be powered even when the PCH and the rest of the platform are not, the signal may glitch as power is being asserted; thus, the controller should wait until PLTRST# has de-asserted before monitoring the signal.

#### 5.23.3.5.1 Special Conditions

The external controller should have a graceful means of handling when TEMP\_ALERT# asserts, and the controller reads PCH, but all temperature values are within limits. In this case, the controller should assume that by the time the controller could read the data, it had changed and moved back within the limits.

#### 5.23.3.6 BIOS Set Up

For the PCH to properly report temperature and enable alerts, the BIOS must configure the PCH at boot or from suspend/resume state by writing the following information to the PCH MMIO space. This information is NOT configurable using the external controller.

- Enables for PCH thermal alerts.
- Enables for reading PCH temperatures.
- Setting up the temperature calculation equations.

#### 5.23.3.7 SMBus Rules

The PCH may NACK an incoming SMBus transaction. In certain cases the PCH will NACK the address, and in other cases it will NACK the command depending on internal conditions (such as errors, busy conditions). Given that most of the cases are due to internal conditions, the external controller must alias a NACK of the command and a NACK of the address to the same behavior. The controller must not try to make any determination of the reason for the NACK, based on the type of NACK (command versus address).

The PCH will NACK when it is enabled but busy. The external controller is required to retry up to 3 times when they are NACK'ed. In reality if there is a NACK because of the PCH being busy, in almost all cases the next read will succeed since the update internally takes very little time. In the case of a long delay, the external controller must assume that the PCH will never return good data.

#### 5.23.3.7.1 During Block Read

On the Block Read, the PCH will respect the NACK and Stop indications from the external controller, but will consider this an error case. It will recover from this case and correctly handle the next SMBus request.

The PCH will honor STOP during the block read command and cease providing data. On the next Block Read, the data will start with byte 0 again. However, this is not a recommended usage except for 'emergency cases'. In general the external controller should read the entire length of data that was originally programmed.

#### 5.23.3.7.2 Power On

On the Block Read, the PCH will respect the NACK and Stop indications from the external controller, but will consider this an error case. It will recover from this case and correctly handle the next SMBus request.

The PCH will honor STOP during the block read command and cease providing data. On the next Block Read, the data will start with byte 0 again. However, this is not a recommended usage except for 'emergency cases'. In general, the external controller should read the entire length of data that was originally programmed.

### 5.23.3.8 Case for Considerations

Below are some corner cases and some possible actions that the external controller could take.

**Note:** A 1-byte sequence number is available to the data read by the external controller. Each time the PCH updates the thermal information it will increment the sequence number. The external controller can use this value as an indication that the thermal firmware is actually operating.

**Note:** The sequence number will roll over to 00h when it reaches FFh.

#### 1. Power on:

The PCH will not respond to any SMBus activity (on SMLink1 interface) until it has loaded the thermal firmware, which in general would take 1 – 4 ms. During this period, the PCH will NACK any SMBus transaction from the external controller.

The load should take 1 - 4 ms, but the external controller should design for 30 seconds based on long delays for S4 resume that takes longer than normal power up. This would be an extreme case, but for larger memory footprints and non-optimized recovery times, 30 seconds is a safe number to use for the timeout.

Recover/Failsafe: if the PCH has not responded within 30 seconds, the external controller can assume that the system has had a major error and the external controller should ramp the fans to some reasonably high value. The only recover from this is an internal reset on the PCH that is not visible to the external controller. Therefore the external controller might choose to poll every 10 – 60 seconds (some fairly long period) hereafter to see if the PCH's thermal reporting has come alive.

2. The PCH Thermal firmware hangs and requires an internal reset that is not visible to the external controller.

The PCH will NACK any SMBus transaction from the external controller. The PCH may not be able to respond for up to 30 seconds while the firmware is being reset and reconfigured. The external controller could choose to poll every 1 – 10 seconds to see if the thermal firmware has been successfully reset and is now providing data.

General recovery for this case is about 1 second, but 30 seconds should be used by the external controller at the Timeout.

Recovery/Failsafe: same as in case #1.

3. Fatal PCH error, causes a global reset of all components.

When there is a fatal PCH error, a global reset may occur, and then case #1 applies. The external controller can observe, if desired, PLTRST# assertion as an indication of this event.

4. The PCH thermal firmware fails or is hung, but no reset occurs

The sequence number will not be updated, so the external controller knows to go to failsafe after some number of reads (8 or so) return the same sequence number. The external controller could choose to poll every 1 – 10 seconds to see if the thermal firmware has been successfully reset and working again.

In the absence of other errors, the updates for the sequence number should never be longer than 400 ms, so the number of reads needed to indicate that there is a hang should be at around 2 seconds. But when there is an error, the sequence number may not get updated for seconds. In the case that the external controller sees a NACK from the PCH, then it should restart its sequence counter, or otherwise be aware that the NACK condition needs to be factored into the sequence number usage.

The use of sequence numbers is not required, but is provided as a means to ensure correct PCH firmware operation.

5. When the PCH updates the Block Read data structure, the external controller gets a NACK during this period.

To ensure atomicity of the SMBus data read with respect to the data itself, when the data buffer is being updated, the PCH will NACK the Block Read transaction.

The update is only a few microseconds, so very short in terms of SMBus polling time; therefore, the next read should be successful. The external controller should attempt 3 reads to handle this condition before moving on.

If the Block read has started (that is, the address is ACK'ed) then the entire read will complete successfully, and the PCH will update the data only after the SMBus read has completed.

6. System is going from S0 to S3/4/5. The thermal monitoring firmware is fully operational if the system is in S0/S1, so the following only applies to S3/4/5.

When the PCH detects the operating system request to go to S3/4/5, it will take the SMLink1 controller offline as part of the system preparation. The external controller will see a period where its transactions are getting NACK'ed, and then see SLP\_S3# assert. This period is relatively short (a couple of seconds depending on how long all the devices take to place themselves into the D3 state), and would be far less than the 30 second limit mentioned above.

7. TEMP\_ALERT# – Since there can be an internal reset, the TEMP\_ALERT# may get asserted after the reset. The external controller must accept this assertion and handle it.

### 5.23.3.8.1 Example Algorithm for Handling Transaction

One algorithm for the transaction handling could be summarized as follows. This is just an example to illustrate the above rules. There could be other algorithms that can achieve the same results.

1. Perform SMBus transaction.
2. If ACK, then continue
3. If NACK
  - a. Try again for 2 more times, in case the PCH is busy updating data.
  - b. If 3 successive transactions receive NACK, then
    - Ramp fans, assuming some general long reset or failure
    - Try every 1 – 10 seconds to see if SMBus transactions are now working
    - If they start then return to step 1
    - If they continue to fail, then stay in this step and poll, but keep the fans ramped up or implement some other failure recovery mechanism.

## 5.24

### Intel® High Definition Audio (Intel® HD Audio) Overview (D27:F0)

The PCH High Definition Audio (HDA) controller communicates with the external codec(s) over the Intel® High Definition Audio serial link. The controller consists of a set of DMA engines that are used to move samples of digitally encoded data between system memory and an external codec(s). The PCH implements four output DMA engines and four input DMA engines. The output DMA engines move digital data from system memory to a D-A converter in a codec. The PCH implements a single Serial Data Output signal (HDA\_SDO) that is connected to all external codecs. The input DMA engines move digital data from the A-D converter in the codec to system memory. The PCH implements four Serial Digital Input signals (HDA\_SDI[1:0]) supporting up to four codecs.

Audio software renders outbound and processes inbound data to/from buffers in system memory. The location of individual buffers is described by a Buffer Descriptor List (BDL) that is fetched and processed by the controller. The data in the buffers is arranged in a predefined format. The output DMA engines fetch the digital data from memory and reformat it based on the programmed sample rate, bit/sample, and number of channels. The data from the output DMA engines is then combined and serially sent to the external codecs over the Intel High Definition Audio link. The input DMA engines receive data from the codecs over the Intel High Definition Audio link and format the data based on the programmable attributes for that stream. The data is then written to memory in the predefined format for software to process. Each DMA engine moves one stream of data. A single codec can accept or generate multiple streams of data, one for each A-D or D-A converter in the codec. Multiple codecs can accept the same output stream processed by a single DMA engine.

Codec commands and responses are also transported to and from the codecs using DMA engines.

The PCH Intel® HD Audio controller supports the Function Level Reset (FLR).



## 5.24.1 Intel® High Definition Audio (Intel® HD Audio) Docking

### 5.24.1.1 Dock Sequence

**Note:** This sequence is followed when the system is running and a docking event occurs.

1. Since the PCH supports docking, the Docking Supported (DCKSTS.DS) bit defaults to a 1. POST BIOS and ACPI BIOS software uses this bit to determine if the Intel® HD Audio controller supports docking. BIOS may write a 0 to this R/WO bit during POST to effectively turn off the docking feature.
2. After reset in the undocked quiescent state, the Dock Attach (DCKCTL.DA) bit and the Dock Mate (DCKSTS.DM) bit are both de-asserted. The HDA\_DOCK\_EN# signal is de-asserted and HDA\_DOCK\_RST# is asserted. Bit Clock, SYNC, and SDO signals may or may no be running at the point in time that the docking event occurs.
3. The physical docking event is signaled to ACPI BIOS software using ACPI control methods. This is normally done through a GPIO signal on the PCH and is outside the scope of this section of the specification.
4. ACPI BIOS software first checks that the docking is supported using DCKSTS.DS=1 and that the DCKSTS.DM=0 and then initiates the docking sequence by writing a 1 to the DCKCTL.DA bit.
5. The Intel® HD Audio controller then asserts the HDA\_DOCK\_EN# signal so that the Bit Clock signal begins toggling to the dock codec. HDA\_DOCK\_EN# shall be asserted synchronously to Bit Clock and timed such that Bit Clock is low, SYNC is low, and SDO is low. Pull-down resistors on these signals in the docking station discharge the signals low so that when the state of the signal on both sides of the switch is the same when the switch is turned on. This reduces the potential for charge coupling glitches on these signals.

**Note:** In the PCH the first 8 bits of the Command field are “reserved” and always driven to 0s. This creates a predictable point in time to always assert HDA\_DOCK\_EN#.

**Note:** The HD Audio link reset exit specification that requires that SYNC and SDO be driven low during Bit Clock startup is not ensured. The SDO and Bit Clock signals may not be low while HDA\_DOCK\_RST# is asserted which also violates the specification.

6. After the controller asserts HDA\_DOCK\_EN#, it waits for a minimum of 2400 Bit Clocks (100  $\mu$ s) and then de-asserts HDA\_DOCK\_RST#. This is done in such a way to meet the HD Audio link reset exit specification. HDA\_DOCK\_RST# de-assertion should be synchronous to Bit Clock and timed such that there are least 4 full Bit Clocks from the de-assertion of HDA\_DOCK\_RST# to the first frame SYNC assertion.
7. The Connect/Turnaround/Address Frame hardware initialization sequence will now occur on the dock codecs' SDI signals. A dock codec is detected when SDI is high on the last Bit Clock cycle of the Frame Sync of a Connect Frame. The appropriate bit(s) in the State Change Status (STATESTS) register will be set. The Turnaround and Address Frame initialization sequence then occurs on the dock codecs' SDI(s).
8. After this hardware initialization sequence is complete (approximately 32 frames), the controller hardware sets the DCKSTS.DM bit to 1 indicating that the dock is now mated. ACPI BIOS polls the DCKSTS.DM bit and when it detects it is set to 1, conveys this to the operating system through a plug-N-play IRP. This eventually invokes the HD Audio Bus Driver, which then begins its codec discovery, enumeration, and configuration process.

9. Alternatively to step #8, the HD Audio Bus Driver may choose to enable an interrupt by setting the WAKEEN bits for SDINs that did not originally have codecs attached to them. When a corresponding STATESTS bit gets set, an interrupt will be generated. In this case the HD Audio Bus Driver is called directly by this interrupt instead of being notified by the plug-N-play IRP.
10. Intel® HD Audio Bus Driver software “discovers” the dock codecs by comparing the bits now set in the STATESTS register with the bits that were set prior to the docking event.

#### 5.24.1.2 Exiting D3/CRST# When Docked

1. In D3/CRST#, CRST# is asserted by the HD Audio Bus Driver. CRST# asserted resets the dock state machines, but does not reset the DCKCTL.DA bit. Because the dock state machines are reset, the dock is electrically isolated (HDA.Dock\_EN# de-asserted) and DOCK\_RST# is asserted.
2. The Bus Driver clears the STATESTS bits, then de-asserts CRST#, waits approximately 7 ms, then checks the STATESTS bits to see which codecs are present.
3. When CRST# is de-asserted, the dock state machine detects that DCKCTL.DA is still set and the controller hardware sequences through steps to electrically connect the dock by asserting HDA.Dock\_EN# and then eventually de-asserts DOCK\_RST#. This completes within the 7 ms mentioned in step 2).
4. The Bus Driver enumerates the codecs present as indicated using the STATESTS bits.

**Note:** This process does not require BIOS or ACPI BIOS to set the DCKCTL.DA bit.

#### 5.24.1.3 Cold Boot/Resume From S3 When Docked

1. When booting and resuming from S3, PLTRST# switches from asserted to de-asserted. This clears the DCKCTL.DA bit and the dock state machines. Because the dock state machines are reset, the dock is electrically isolated (HDA.Dock\_EN# de-asserted) and DOCK\_RST# is asserted.
2. POST BIOS detects that the dock is attached and sets the DCKCTL.DA bit to 1.

**Note:** At this point, CRST# is still asserted—thus, the dock state machine will remain in its reset state.

3. The Bus Driver clears the STATESTS bits, then de-asserts CRST#, waits approximately 7 ms, then checks the STATESTS bits to see which codecs are present.
4. When CRST# is de-asserted, the dock state machine detects that DCKCTL.DA is still set and the controller hardware sequences through steps to electrically connect the dock by asserting HDA.Dock\_EN# and then eventually de-asserts DOCK\_RST#. This completes within the 7 ms mentioned in step 3).
5. The Bus Driver enumerates the codecs present as indicated using the STATESTS bits.

#### 5.24.1.4 Undock Sequence

There are two possible undocking scenarios. The first is the one that is initiated by the user that invokes software and gracefully shuts down the dock codecs before they are undocked. The second is referred to as the “surprise undock” where the user undocks



while the dock codec is running. Both of these situations appear the same to the controller as it is not cognizant of the “surprise removal”. Both sequences will be discussed here.

#### 5.24.1.5 Normal Undock

1. In the docked quiescent state, the Dock Attach (DCKCTL.DA) bit and the Dock Mate (DCKSTS.DM) bit are both asserted. The HDA\_DOCK\_EN# signal is asserted and HDA\_DOCK\_RST# is de-asserted.
2. The user initiates an undock event through the GUI interface or by pushing a button. This mechanism is outside the scope of this section of the document. Either way ACPI BIOS software will be invoked to manage the undock process.
3. ACPI BIOS will call the HD Audio Bus Driver software in order to halt the stream to the dock codec(s) prior to electrical undocking. If the HD Audio Bus Driver is not capable of halting the stream to the docked codec, ACPI BIOS will initiate the hardware undocking sequence as described in the next step while the dock stream is still running. From this standpoint, the result is similar to the “surprise undock” scenario where an audio glitch may occur to the docked codec(s) during the undock process.
4. The ACPI BIOS initiates the hardware undocking sequence by writing a 0 to the DCKCTL.DA bit.
5. The HD Audio controller asserts HDA\_DOCK\_RST#. HDA\_DOCK\_RST# assertion shall be synchronous to Bit Clock. There are no other timing requirements for HDA\_DOCK\_RST# assertion. The HD Audio link reset specification requirement that the last Frame sync be skipped will not be met.
6. A minimum of 4 Bit Clocks after HDA\_DOCK\_RST# the controller will de-assert HDA\_DOCK\_EN# to isolate the dock codec signals from the PCH HD Audio link signals. HDA\_DOCK\_EN# is de-asserted synchronously to Bit Clock and timed such that Bit Clock, SYNC, and SDO are low.
7. After this hardware undocking sequence is complete, the controller hardware clears the DCKSTS.DM bit to 0 indicating that the dock is now un-mated. ACPI BIOS software polls DCKSTS.DM and when it sees DM set, conveys to the end user that physical undocking can proceed. The controller is now ready for a subsequent docking event.

#### 5.24.1.6 Surprise Undock

1. In the surprise undock case the user undocks before software has had the opportunity to gracefully halt the stream to the dock codec and initiate the hardware undock sequence.
2. A signal on the docking connector is connected to the switch that isolates the dock codec signals from the PCH HD Audio link signals (DOCK\_DET#). When the undock event begins to occur, the switch will be put into isolate mode.
3. The undock event is communicated to the ACPI BIOS using ACPI control methods that are outside the scope of this section of the document.
4. ACPI BIOS software writes a 0 to the DCKCTL.DA bit. ACPI BIOS then calls the HD Audio Bus Driver using plug-N-play IRP. The Bus Driver then posthumously cleans up the dock codec stream.
5. The HD Audio controller hardware is oblivious to the fact that a surprise undock occurred. The flow from this point on is identical to the normal undocking sequence described in [Section 5.24.1.5](#) starting at step 3). It finishes with the hardware

clearing the DCKSTS.DM bit set to 0 indicating that the dock is now un-mated. The controller is now ready for a subsequent docking event.

#### 5.24.1.7 Interaction Between Dock/Undock and Power Management States

When exiting from S3, PLTRST# will be asserted. The POST BIOS is responsible for initiating the docking sequence if the dock is already attached when PLTRST# is de-asserted. POST BIOS writes a 1 to the DCKCTL.DA bit prior to the HD Audio driver de-asserting CRST# and detecting and enumerating the codecs attached to the HDA.Dock\_Rst# signal. The HD Audio controller does not directly monitor a hardware signal indicating that a dock is attached. Therefore, a method outside the scope of this document must be used to cause the POST BIOS to initiate the docking sequence.

When exiting from D3, CRST# will be asserted. When CRST# bit is 0 (asserted), the DCKCTL.DA bit is not cleared. The dock state machine will be reset such that HDA.Dock\_En# will be de-asserted, HDA.Dock\_Rst# will be asserted, and the DCKSTS.DM bit will be cleared to reflect this state. When the CRST# bit is de-asserted, the dock state machine will detect that DCKCTL.DA is set to 1 and will begin sequencing through the dock process.

**Note:** This does not require any software intervention.

#### 5.24.1.8 Relationship Between HDA.Dock\_Rst# and HDA.Rst#

HDA.Rst# will be asserted when a PLTRST# occurs or when the CRST# bit is 0. As long as HDA.Rst# is asserted, the DOCK.Rst# signal will also be asserted.

When PLTRST# is asserted, the DCKCTL.DA and DCKSTS.DM bits will be get cleared to their default state (0s), and the dock state machine will be reset such that HDA.Dock\_En# will be de-asserted, and HDA.Dock\_Rst# will be asserted. After any PLTRST#, POST BIOS software is responsible for detecting that a dock is attached and then writing a 1 to the DCKCTL.DA bit prior to the HD Audio Bus Driver de-asserting CRST#.

When CRST# bit is 0 (asserted), the DCKCTL.DA bit is not cleared. The dock state machine will be reset such that HDA.Dock\_En# will be de-asserted, HDA.Dock\_Rst# will be asserted, and the DCKSTS.DM bit will be cleared to reflect this state. When the CRST# bit is de-asserted, the dock state machine will detect that DCKCTL.DA is set to 1 and will begin sequencing through the dock process.

**Note:** This does not require any software intervention

### 5.25 Intel® Management Engine (Intel® ME) and Intel® ME Firmware 9.5

This embedded operating environment is called the Intel® Management Engine (Intel® ME). The key properties of Intel® ME:

- Connectivity
  - Integration into I/O subsystem of PCH
  - Delivery of advanced I/O functions
- Security
  - More secure (Intel root of trust) and isolated execution
  - Increased security of flash file system

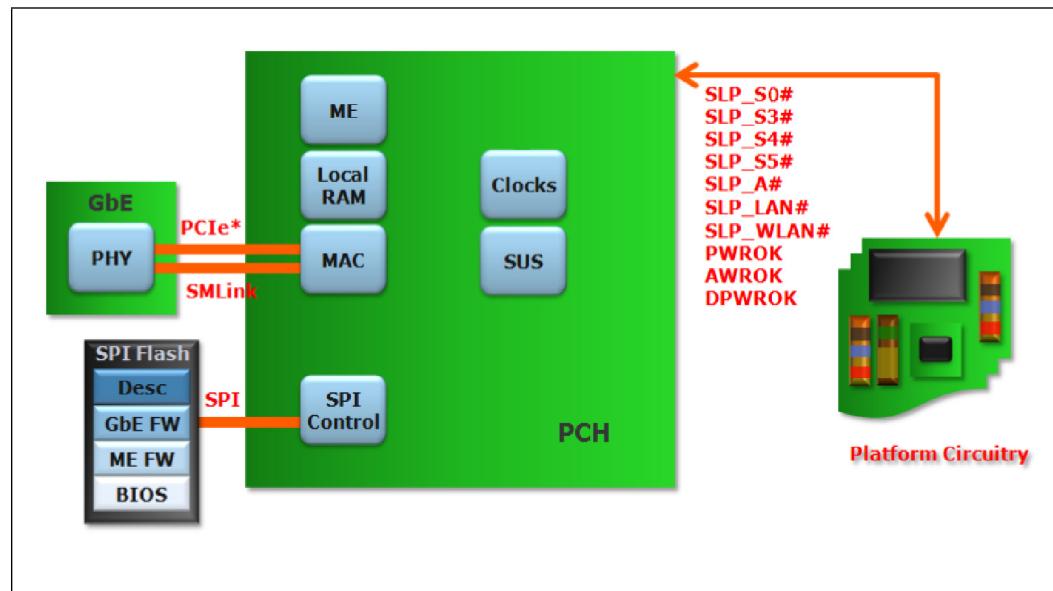
- Modularity and Partitioning
  - OSV, VMM, and software Independence
  - Rapid response to competitive changes
- Power
  - Always-On, Always Connected
  - Advanced functions in low power S3-S4-S5 operation
  - OS independent PM and thermal heuristics

Intel® ME firmware provides a variety of services that range from low-level hardware initialization and provisioning to high-level end-user software based IT manageability services. One of Intel® ME firmware's most established and recognizable features is Intel® Active Management Technology (Intel® AMT).

Intel® Active Management Technology (Intel® AMT) is a set of advanced manageability features developed to meet the evolving demands placed on IT to manage a network infrastructure. Intel® AMT reduces the Total Cost of Ownership (TCO) for IT management through features such as asset tracking, remote manageability, and robust policy-based security, resulting in fewer desk-side visits and reduced incident support durations. Intel® AMT extends the manageability capability for IT through Out Of Band (OOB), allowing asset information, remote diagnostics, recovery, and contain capabilities to be available on client systems even when they are in a low-power, or "off" state, or in situations when the operating system is hung.

For more details on various Intel® ME firmware features supported by Intel® ME firmware, such as Intel Active Management Technology, refer to the relevant firmware feature Product Requirements Document (PRD).

**Figure 5-12. PCH Intel® Management Engine (Intel® ME)—High Level Block Diagram**



## 5.25.1 Intel® Management Engine (Intel® ME) Requirements

The following list of components compose the Intel® ME hardware infrastructure:

- The Intel® ME is the general purpose controller that resides in the PCH. It operates in parallel to, and is resource-isolated from, the host processor.
- The SPI flash device stores Intel® ME Firmware code that is executed by the Intel® ME for its operations. The PCH controls the flash device through the SPI interface and internal logic.
- In the M0 power state, the Intel® ME Firmware code is loaded from SPI flash into DRAM and cached in secure and isolated SRAM. In order to interface with DRAM, the Intel® ME uses the integrated memory controller (IMC) present in the processor. In the lower Intel® ME power state, M3, code is executed exclusively from secure and isolated Intel® ME local RAM.
- The LAN controller embedded in the PCH, as well as the Intel Gigabit Platform LAN Connect Device, are required for Intel® ME and Intel AMT network connectivity.
- BIOS provides asset detection and POST diagnostics (BIOS and Intel® AMT can optionally share the same flash memory device)
- An ISV software package, such as LANDesk\*, Altiris\*, or Microsoft\* SMS, can be used to take advantage of the platform manageability capabilities of Intel® AMT.

## 5.26 Serial Peripheral Interface (SPI) for Flash

The Serial Peripheral Interface (SPI) is a 4-pin interface that provides a lower-cost alternative for system flash versus the Firmware Hub on the LPC bus.

The 4-pin SPI interface consists of clock (CLK), master data out (Master Out Slave In (MOSI)), master data in (Master In Slave Out (MISO)) and an active low chip select (SPI\_CS[1:0]#). SPI also adds two extra pins, SPI\_IO2 and SPI\_IO3, for Quad I/O operation.

The PCH supports up to two SPI flash devices using two separate Chip Select pins. Each SPI flash device can be up to 16MB. The PCH SPI interface supports 20 MHz, 33 MHz, and 50 MHz SPI devices. A SPI Flash device on Chip Select 0 with a valid descriptor MUST be attached directly to the PCH.

The PCH supports fast read that consist of:

1. Dual Output Fast Read (Single Input Dual Output)
2. Dual I/O Fast Read (Dual Input Dual Output)
3. Quad Output Fast Read (Single Input Quad Output)
4. Quad I/O Fast Read (Quad Input Quad Output)

Fast Read function will be enabled if the particular SPI part supports one of the functions mentioned above, along with support for SFDP (Serial Flash Discoverable Parameter).

The PCH adds support for SFDP. SFDP is a JEDEC\* standard that provides a consistent method for describing functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. The PCH SPI controller reads the internal parameter table and enables divergent features of multiple SPI vendor parts.

The PCH adds a third chip select, SPI\_CS2#, for TPM support over SPI. The TPM Bus will use SPI\_CLK, SPI\_MISO, SPI\_MOSI, and SPI\_CS2# SPI signals.



**Note:** Communication on the SPI bus is accomplished with a Master – Slave protocol. The Slave is connected to the PCH and is implemented as a tri-state bus. If Boot BIOS Strap = '00', then the LPC is selected as the location for BIOS. The BIOS may still be placed on LPC, but all platforms with the PCH require a SPI flash connected directly to the PCH's SPI bus with a valid descriptor connected to Chip Select 0 in order to boot.

**Note:** When SPI is selected by the Boot BIOS Destination Strap and a SPI device is detected by the PCH, LPC-based BIOS flash is disabled.

## 5.26.1 SPI Supported Feature Overview

SPI Flash on the PCH has two operational modes—descriptor and non-descriptor.

### 5.26.1.1 Non-Descriptor Mode

Non-Descriptor Mode is not supported as a valid flash descriptor is required for all PCH platforms.

### 5.26.1.2 Descriptor Mode

Descriptor Mode is required for all SKUs of the PCH. It enables many features of the Chipset:

- Integrated Gigabit Ethernet and Host processor for Gigabit Ethernet Software
- Intel® Active Management Technology
- Intel® Management Engine Firmware
- PCI Express\* root port configuration
- Supports up to two SPI components using two separate chip select pins
- Hardware enforced security restricting master accesses to different regions
- Chipset soft strap regions provides the ability to use Flash NVM as an alternative to hardware pull-up/pull-down resistors for the PCH and processor
- Supports the SPI Fast Read instruction and frequencies of up to 50 MHz
- Support Single Input, Dual Output Fast read
- Uses standardized Flash Instruction Set

#### 5.26.1.2.1 SPI Flash Regions

In Descriptor Mode the Flash is divided into five separate regions as indicated in the following table.

**Table 5-52. SPI Flash Regions**

Region	Content
0	Flash Descriptor
1	BIOS
2	Intel® Management Engine
3	Gigabit Ethernet
4	Platform Data

Only three masters can access the four regions; Host processor running BIOS code, Integrated Gigabit Ethernet, and Host processor running Gigabit Ethernet Software, and the Intel® Management Engine. The Flash Descriptor and Intel® ME regions are the only required regions. The Flash Descriptor has to be in region 0 and region 0 must be located in the first sector of Device 0 (Offset 0).

Regions can extend across multiple components, but must be contiguous.

### Flash Region Sizes

SPI flash space requirements differ by platform and configuration. The Flash Descriptor requires one 4KB or larger block. GbE requires two 4KB or larger blocks. The amount of flash space consumed is dependent on the erase granularity of the flash part and the platform requirements for the Intel® ME and BIOS regions. The Intel® ME region contains firmware to support Intel Active Management Technology and other Intel® ME capabilities.

**Table 5-53. Region Size Versus Erase Granularity of Flash Components**

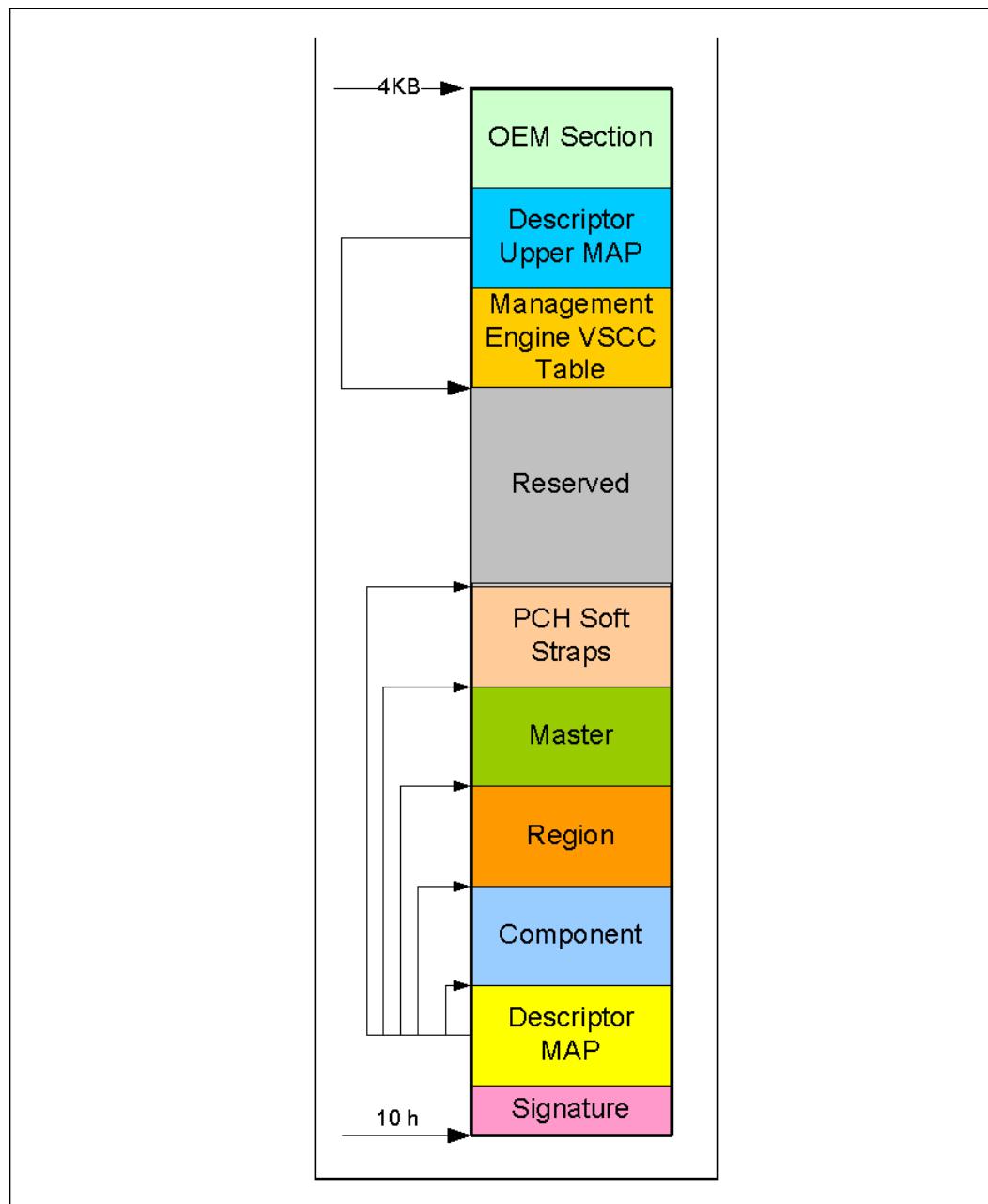
Region	Size with 4KB Blocks	Size with 8KB Blocks	Size with 64KB Blocks
Descriptor	4KB	8KB	64KB
GbE	8KB	16KB	128KB
BIOS	Varies by Platform	Varies by Platform	Varies by Platform
Intel® ME	Varies by Platform	Varies by Platform	Varies by Platform

## 5.26.2 Flash Descriptor

The maximum size of the Flash Descriptor is 4KB. If the block/sector size of the SPI flash device is greater than 4KB, the flash descriptor will only use the first 4KB of the first block. The flash descriptor requires its own block at the bottom of memory (00h). The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to read-only when the computer leaves the manufacturing floor.

The Flash Descriptor is made up of eleven sections (see Figure 5-13).

Figure 5-13. Flash Descriptor Sections



1. The Flash signature selects Descriptor Mode as well as verifies if the flash is programmed and functioning. The data at the bottom of the flash (offset 10h) must be OFF0A55Ah in order to be in Descriptor mode.
2. The Descriptor map has pointers to the other five descriptor sections as well as the size of each.

3. The component section has information about the SPI flash in the system including: the number of components, density of each, invalid instructions (such as chip erase), and frequencies for read, fast read and write/erase instructions.
4. The Region section points to the three other regions as well as the size of each region.
5. The master region contains the security settings for the flash, granting read/write permissions for each region and identifying each master by a requestor ID. See [Section 5.26.2.1](#) for more information.
6. and 7. The processor and PCH soft strap sections contain processor and PCH configurable parameters.
8. The Reserved region between the top of the processor strap section and the bottom of the OEM Section is reserved for future Chipset usages.
9. The Descriptor Upper MAP determines the length and base address of the Management Engine VSCC Table.
10. The Management Engine VSCC Table holds the JEDEC\* ID and the VSCC information of the entire SPI Flash supported by the NVM image.
11. OEM Section is 256 Bytes, reserved at the top of the Flash Descriptor for use by the OEM.

### 5.26.2.1 Descriptor Master Region

The master region defines read and write access setting for each region of the SPI device. The master region recognizes three masters: BIOS, Gigabit Ethernet, and Management Engine. Each master is only allowed to do direct reads of its primary regions.

**Table 5-54. Region Access Control Table**

Master Read/Write Access			
Region	Processor and BIOS	Intel® ME	GbE Controller
Descriptor	N/A	N/A	N/A
BIOS	Processor and BIOS can always read from and write to BIOS Region	Read/Write	Read/Write
Management Engine	Read/Write	Intel® ME can always read from and write to Intel® ME Region	Read/Write
Gigabit Ethernet	Read/Write	Read/Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A



### 5.26.3 Flash Access

There are two types of flash accesses:

#### Direct Access:

- Masters are allowed to do direct read-only of their primary region
  - Gigabit Ethernet region can only be directly accessed by the Gigabit Ethernet controller. Gigabit Ethernet software must use Program registers to access the Gigabit Ethernet region.
- Master's Host or Management Engine virtual read address is converted into the SPI Flash Linear Address (FLA) using the Flash Descriptor Region Base/Limit registers

#### Program Register Access:

- Program Register accesses are not allowed to cross a 4KB boundary and can not issue a command that might extend across two components
- Software programs the FLA corresponding to the region desired
  - Software must read the devices Primary Region Base/Limit address to create a FLA.

#### 5.26.3.1 Direct Access Security

- Requester ID of the device must match that of the primary Requester ID in the Master Section
- Calculated Flash Linear address must fall between primary region base/limit
- Direct Write not allowed
- Direct Read Cache contents are reset to 0s on a read from a different master

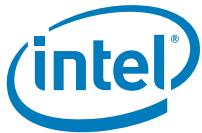
#### 5.26.3.2 Register Access Security

- Only primary region masters can access the registers

#### Note:

Processor running Gigabit Ethernet software can access Gigabit Ethernet registers

- Masters are only allowed to read or write those regions; they have read/write permission
- Using the Flash Region Access Permissions, one master can give another master read/write permissions to their area
- Using the five Protected Range registers, each master can add separate read/write protection above that granted in the Flash Descriptor for their own accesses
  - Example: BIOS may want to protect different regions of BIOS from being erased
  - Ranges can extend across region boundaries



## 5.26.4 Serial Flash Device Compatibility Requirements

A variety of serial flash devices exist in the market. For a serial flash device to be compatible with the PCH SPI bus, it must meet the minimum requirements detailed in the following sections.

**Note:** All PCH platforms have require Intel® Management Engine Firmware.

### 5.26.4.1 PCH SPI Based BIOS Requirements

A serial flash device must meet the following minimum requirements when used explicitly for system BIOS storage.

- Erase size capability of at least one of the following: 64 Kbytes, 8 Kbytes, 4 Kbytes, or 256 bytes.
- Device must support multiple writes to a page without requiring a preceding erase cycle (Refer to [Section 5.26.5](#))
- Serial flash device must ignore the upper address bits such that an address of FFFFFFFh aliases to the top of the flash memory.
- SPI Compatible Mode 0 support (clock phase is 0 and data is latched on the rising edge of the clock).
- If the device receives a command that is not supported or incomplete (less than 8 bits), the device must complete the cycle gracefully without any impact on the flash content.
- An erase command (page, sector, block, chip, and so forth) must set all bits inside the designated area (page, sector, block, chip, and so forth) to 1 (Fh).
- Status Register bit 0 must be set to 1 when a write, erase or write to status register is in progress and cleared to 0 when a write or erase is NOT in progress.
- Devices requiring the Write Enable command must automatically clear the Write Enable Latch at the end of Data Program instructions.
- Byte write must be supported. The flexibility to perform a write between 1 byte to 64 bytes is recommended.
- Hardware Sequencing requirements are optional in BIOS only platforms.
- SPI flash parts that do not meet Hardware sequencing command set requirements may work in BIOS only platforms using software sequencing.

### 5.26.4.2 Integrated LAN Firmware SPI Flash Requirements

A serial flash device that will be used for system BIOS and Integrated LAN or Integrated LAN only must meet all the SPI Based BIOS Requirements plus:

- Hardware sequencing
- 4-, 8-, or 64KB erase capability must be supported.

#### 5.26.4.2.1 SPI Flash Unlocking Requirements for Integrated LAN

BIOS must ensure there is no SPI flash based read/write/erase protection on the GbE region. GbE firmware and drivers for the integrated LAN need to be able to read, write and erase the GbE region at all times.



### 5.26.4.3 Intel® Management Engine Firmware (Intel® ME) Firmware SPI Flash Requirements

Intel® Management Engine Firmware must meet the SPI flash based BIOS Requirements plus:

- Hardware Sequencing.
- Flash part must be uniform 4KB erasable block throughout the entire device or have 64KB blocks with the first block (lowest address) divided into 4KB or 8KB blocks.
- Write protection scheme must meet SPI flash unlocking requirements for Intel® ME.

#### 5.26.4.3.1 SPI Flash Unlocking Requirements for Intel® Management Engine (Intel® ME)

Flash devices must be globally unlocked (read, write, and erase access on the ME region) from power on by writing 00h to the flash's status register to disable write protection.

If the status register must be unprotected, it must use the enable write status register command 50h or write enable 06h.

Opcode 01h (write to status register) must then be used to write a single byte of 00h into the status register. This must unlock the entire part. If the SPI flash's status register has non-volatile bits that must be written, Bits 5:2 of the flash's status register must be all 0h to indicate that the flash is unlocked.

If Bits 5:2 return a non zero values, the Intel® ME Firmware will send a write of 00h to the status register. This must keep the flash part unlocked.

If there is no need to execute a write enable on the status register, then opcodes 06h and 50h must be ignored.

After global unlock, BIOS has the ability to lock down small sections of the flash as long as they do not involve the Intel® ME or GbE region.

### 5.26.4.4 Hardware Sequencing Requirements

Table 5-55 contains a list of commands and the associated opcodes that a SPI-based serial flash device must support in order to be compatible with hardware sequencing.

**Table 5-55. Hardware Sequencing Commands and Opcode Requirements (Sheet 1 of 2)**

Commands	Opcode	Notes
Write to Status Register	01h	Writes a byte to the SPI flash status register. Enable Write to the Status register command must be run prior to this command.
Program Data	02h	Single byte or 64 byte write as determined by flash part capabilities and software.
Read Data	03h	
Write Disable	04h	
Read Status	05h	Outputs contents of the SPI flash status register
Write Enable	06h	
Fast Read	0Bh	
Enable Write to Status Register	06h or 50h	Enables a bit in the status register to allow an update to the status register

**Table 5-55. Hardware Sequencing Commands and Opcode Requirements (Sheet 2 of 2)**

Commands	Opcode	Notes
Erase	Programmable	256B, 4 Kbyte, 8 Kbyte or 64 Kbyte
Full Chip Erase	C7h	
JEDEC* ID	9Fh	See <a href="#">Section 5.26.4.4.3</a> .

#### 5.26.4.4.1 Single Input, Dual Output Fast Read

The PCH now supports the functionality of a single input, dual output fast read. Opcode and address phase are shifted in serially to the serial flash SI (Serial In) pin. Data is read out after 8 clocks (dummy bits or wait states) from both the SI and SO pin, effectively doubling the throughput of each fast read output. To enable this functionality, both Single Input Dual Output Fast Read Supported and Fast Read supported must be enabled.

#### 5.26.4.4.2 Serial Flash Discoverable Parameters (SFDP)

As the number of features keeps growing in the serial flash, the need for correct, accurate configuration increases. A method of determining configuration information is Serial Flash Discoverable Parameters (SFDP). Information, such as VSCC values and flash attributes, can be read directly from the flash parts. The discoverable parameter read opcode behaves like a fast read command. The opcode is 5Ah and the address cycle is 24-bits long. After the opcode 5Ah and address are clocked in, there will then be eight clocks (8 wait states) before valid data is clocked out. SFDP is a capability of the flash part; confirm with target flash vendor to see if it is supported.

For BIOS to take advantage of the 5Ah opcode, it needs to be programmed in the software sequencing registers.

#### 5.26.4.4.3 JEDEC\* ID

Since each serial flash device may have unique capabilities and commands, the JEDEC\* ID is the necessary mechanism for identifying the device so the uniqueness of the device can be comprehended by the controller (master). The JEDEC\* ID uses the opcode 9Fh and a specified implementation and usage model. This JEDEC\* Standard Manufacturer and Device ID read method is defined in Standard JESD21-C, PRN03-NV.

### 5.26.5 Multiple Page Write Usage Model

The system BIOS and Intel® Management Engine Firmware usage models require that the serial flash device support multiple writes to a page (minimum of 512 writes) without requiring a preceding erase command. BIOS commonly uses capabilities, such as counters, that are used for error logging and system boot progress logging. These counters are typically implemented by using byte-writes to 'increment' the bits within a page that have been designated as the counter. The Intel® ME Firmware usage model requires the capability for multiple data updates within any given page. These data updates occur using byte-writes without executing a preceding erase to the given page. Both the BIOS and Intel® ME Firmware multiple page write usage models apply to sequential and non-sequential data writes.

**Note:**

This usage model requirement is based on any given bit only being written once from a 1 to a 0 without requiring the preceding erase. An erase would be required to change bits back to the 1 state.

### 5.26.5.1 Soft Flash Protection

There are two types of flash protection that are not defined in the flash descriptor supported by the PCH:

1. BIOS Range Write Protection
2. SMI#-Based Global Write Protection

Both mechanisms are logically OR'd together such that if any of the mechanisms indicate that the access should be blocked, then it is blocked. [Table 5-56](#) provides a summary of the mechanisms.

**Table 5-56. Flash Protection Mechanism Summary**

Mechanism	Accesses Blocked	Range Specific?	Reset-Override or SMI#-Override?	Equivalent Function on FWH
BIOS Range Write Protection	Writes	Yes	Reset Override	FWH Sector Protection
Write Protect	Writes	No	SMI# Override	Same as Write Protect in Intel® ICHs for FWH

A blocked command will appear to software to finish, except that the Blocked Access status bit is set in this case.

### 5.26.5.2 BIOS Range Write Protection

The PCH provides a method for blocking writes to specific ranges in the SPI flash when the Protected BIOS Ranges are enabled. This is achieved by checking the Opcode type information (which can be locked down by the initial Boot BIOS) and the address of the requested command against the base and limit fields of a Write Protected BIOS range.

**Note:** Once BIOS has locked down the Protected BIOS Range registers, this mechanism remains in place until the next system reset.

### 5.26.5.3 SMI# Based Global Write Protection

The PCH provides a method for blocking writes to the SPI flash when the Write Protected bit is cleared (that is, protected). This is achieved by checking the Opcode type information (which can be locked down by the initial Boot BIOS) of the requested command.

The Write Protect and Lock Enable bits interact in the same manner for SPI BIOS as they do for the FWH BIOS.

## 5.26.6 Flash Device Configurations

The PCH-based platform must have a SPI flash connected directly to the PCH with a valid descriptor and Intel® Management Engine Firmware. BIOS may be stored in other locations such as the Firmware Hub and SPI flash hooked up directly to an embedded controller for Mobile platforms.

**Note:** This will not avoid the direct SPI flash connected to PCH requirement.

## 5.26.7 SPI Flash Device Recommended Pinout

Table 5-57 contains the recommended serial flash device pin-out for an 8-pin device. Use of the recommended pin-out on an 8-pin device reduces complexities involved with designing the serial flash device onto a motherboard and allows for support of a common footprint usage model (refer to [Section 5.26.8.1](#)).

**Table 5-57. Recommended Pinout for 8-Pin Serial Flash Device**

Pin Number	Signal
1	Chips Select
2	Data Output
3	Write Protect
4	Ground
5	Data Input
6	Serial Clock
7	Hold/Reset
8	Supply Voltage

Although an 8-pin device is preferred over a 16-pin device due to footprint compatibility, [Table 5-58](#) contains the recommended serial flash device pin-out for a 16-pin SOIC.

## 5.26.8 Serial Flash Device Package

**Table 5-58. Recommended Pinout for 16-Pin Serial Flash Device**

Pin Number	Signal	Pin Number	Signal
1	Hold/Reset	9	Write Protect
2	Supply Voltage	10	Ground
3	No Connect	11	No Connect
4	No Connect	12	No Connect
5	No Connect	13	No Connect
6	No Connect	14	No Connect
7	Chip Select	15	Serial Data In
8	Serial Data Out	16	Serial Clock

### 5.26.8.1 Common Footprint Usage Model

To minimize platform motherboard redesign and to enable platform Bill of Material (BOM) selectability, many PC System OEMs design their motherboard with a single common footprint. This common footprint allows population of a soldered down device or a socket that accepts a leadless device. This enables the board manufacturer to support, using selection of the appropriate BOM, either of these solutions on the same system without requiring any board redesign.



The common footprint usage model is desirable during system debug and by flash content developers since the leadless device can be easily removed and reprogrammed without damage to device leads. When the board and flash content is mature for high-volume production, both the socketed leadless solution and the soldered down leaded solution are available through BOM selection.

### 5.26.8.2 Serial Flash Device Package Recommendations

It is highly recommended that the common footprint usage model be supported. An example of how this can be accomplished is as follows:

- The recommended pin-out for 8-pin serial flash devices is used (refer to [Section 5.26.7](#)).
- The 8-pin device is supported in either an 8-contact VDFPN (6x5 mm MLP) package or an 8-contact WSON (5x6 mm) package. These packages can fit into a socket that is land pattern compatible with the wide body SO8 package.
- The 8-pin device is supported in the SO8 (150 mil) and in the wide-body SO8 (200 mil) packages.

The 16-pin device is supported in the SO16 (300 mil) package.

## 5.27 Intel® Serial I/O General Purpose SPI Interface

There are two general purpose SPI interfaces to support devices that use serial protocols for transferring data such as sensors on the platform.

**Note:** Each interface consists of 4 wires: a clock (CLK), a chip select (CS), and 2 data lines (MOSI and MISO). The signals are multiplexed with GPIO pins.

**Note:** For details on supported OS, refer to the *Intel® Serial IO Bus Drivers Product Requirement Document (PRD)*. Refer to IBL/CDI document 526515.

### 5.27.1 Overview and Features

The general purpose SPI is full-duplex synchronous serial interface, supporting the Motorola\* SPI protocol. The GSPI interface operates in master mode only, and supports serial bit rate up to 25Mb/s. Serial data formats may range from 4- to 32-bits in length.

Two on-chip memory blocks function as independent FIFOs for data, one for each direction. The blocks are 256 entries deep x32-bits wide. The FIFOs may be loaded or emptied by the system processor using single transfers or DMA burst transfer.

### 5.27.2 Controller Behavior

The general purpose SPI controllers can only be set to operate as a master.

The processor and DMA access data through the transmit and receive FIFOs.

A processor access takes the form of programmed I/O, transferring one FIFO entry per access. Processor accesses must always be 32-bits wide. Processor writes to the FIFOs are 32-bits wide, but the PCH will ignore all bits beyond the programmed FIFO data size. Processor reads to the FIFOs are also 32-bits wide, but the receive data written into the Receive FIFO is stored with '0' in the most significant bits (MSB) down to the programmed data size.

The FIFOs can also be accessed by DMA bursts, which must be in multiples of 1, 2, or 4 bytes, and must be transfer one FIFO entry per access.

A programmable FIFO trigger threshold, when exceeded, generates an interrupt or DMA service request that, if enabled, signals the processor or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO.

The GSPI controller, as a master, provides the clock signal and controls the chip select line. Commands codes as well as data values are serially transferred on the data signals. The PCH asserts a chip select line to select the corresponding peripheral device with which it wants to communicate. The clock line is brought to the device whether it is selected or not. The clock serves as synchronization of the data communication.

### 5.27.3 DMA Controller Interface

The general purpose SPI controllers have an optional built-in DMA handshaking interface to an internal DMA controller. The interface can be used to request and control transfers.

The GSPI controllers use FIFOs with size of 256x32 for the receive and transmit FIFOs.

### 5.27.4 Power Management

Each GSPI controller supports hardware managed clock gating and Runtime D3 functional clock gating mechanisms. Power gating of the GSPI controller is not supported.

#### 5.27.4.1 Hardware Managed

The GSPI controller provides idle detection logic that will be used to locally gate the controller's clocks.

##### 5.27.4.1.1 Runtime D3

The GSPI controllers support Runtime D3. The GSPI controller will not be placed into the D3<sub>HOT</sub> state until the GSPI controllers are fully idle.

##### 5.27.4.1.2 Latency Tolerance Reporting (LTR)

To support Intel Power Optimizer, the GSPI controller supports the LTR mechanism.

Latency Tolerance Reporting is used to allow the system to make better choices on which power state to choose. For example, the system should not enter a power state that has an exit latency that is longer than the latency tolerance of an I/O stream. Each interface module supports this by reporting the latency tolerance.

There are two options for how LTR will be handled:

1. In the standard mode, software will write to the host controllers software LTR register. It is the responsibility of software to update the LTR with the appropriate value based on the bus data rate.
2. In the auto mode, the BIOS will write to the "host controllers Auto LTR Active Value" register and software LTR register.
  - a. When the host controller goes active, the reported LTR value will be the value in the Auto LTR register.
  - b. When the host controller goes inactive (idle), the reported LTR value will be taken from the software LTR register.



## 5.27.5 Interrupts

Each GSPI controller has an interrupt line that is used to notify the driver that service is required. Each interrupt line is assigned to interrupt PCI INT [A-D] or ACPI IRQ[5-7,13]. All interrupts are active high and their behavior is level interrupt.

## 5.27.6 Error Handling

Errors that might occur on the external GSPI signals are comprehended by the GSPI controller and reported to the GSPI bus driver through the standard MMIO registers.

## 5.28 Intel® Serial I/O Secure Digital I/O (SDIO) Interface

The SDIO interface is only intended for connection to an external Wi-Fi controller. The interface will not support general-purpose connections, such as SD cards. The physical connection to the Wi-Fi controller is expected to be static. That means the Wi-Fi peripheral is not expected to be removed/inserted dynamically by the end users. Typically, the Wi-Fi controller would be soldered onto the same board as the PCH or it would be on the some type of riser card that is soldered to the same board as the PCH.

**Note:** SDIO wireless solution does not support Intel AMT.

**Note:** The SDIO interface appears to the host as a standard PCIe\* function; however, the PCIe\* Configuration space can be hidden and it will, thus, appears as an ACPI device.

**Note:** For details on supported OS, refer to the *Intel® Serial IO Bus Drivers Product Requirement Document (PRD)*. Refer to IBL/CDI document 526515.

### 5.28.1 Feature Overview

- Meets SDIO Physical Layer Specification 3.01
- Meets SDIO Host Controller Specification 3.0, including the ADMA2. 32-bit only
- Supports SDIO Default Speed (12.5 MByte/sec) and SDR25 (25 MByte/sec) modes of operation
- Supports DMA (32-bit only) and Non-DMA modes of operation
- Supports 1.8V and 3.3V (static only selection)
- Supports both PCIe\* and ACPI device interface models (BIOS selectable)
- Supports power management of the SDIO peripheral
- The SDIO host controller will only access main memory

### 5.28.2 Controller Overview

SDIO is an industry standard interface that is related to the SD/SD card specification. However, the PCH SDIO interface is intended only for connection to a Wi-Fi controller. The interface will not support general-purpose connections, such as SD cards.

The PCH SDIO interface supports the following operation modes detailed in the following table.

**Table 5-59. SDIO Operation Modes**

Mode	Bus Clock	Data Width	Signal Voltage	Data Latch	Rate Mb/s
Default Speed	25 MHz	4 bits	3.3V or 1.8V	Rising Edge	12.5
SDR25	50 MHz	4 bits	1.8V	Rising Edge	25

### 5.28.2.1 Interrupt

The host controller generates interrupts based on events, such as the completion of commands and external signaling from the peripheral.

The SDIO interface has an interrupt line that is used to notify the driver that service is required. the interrupt line is assigned to interrupt PCI INT [A] or ACPI IRQ[5]. All interrupts are active high and their behavior is level interrupt.

## 5.28.3 Power Management

The SDIO interface supports several power management mechanisms to enhance the power consumption on the interface.

### 5.28.3.1 Runtime D3 Support

The SDIO interface supports runtime D3. The sequence for entry to D3 on SDIO is as follows:

- Verify that the Host controller is idle (no commands pending)
- Set the D3 enable bit

The sequence for exit from D3 on SDIO is as follows:

- D3 enable bit cleared (return to D0)
- Software re-initializes SDIO controller

### 5.28.3.2 Hardware Clock Gating

When the SDIO interface is disabled, the clock to the SDIO unit will be shut down.

When the SDIO interface is enabled, the PCH supports a Hardware Auto-Clock Gating mechanism. When the SDIO host controller is idle, the PCH will gate many internal clocks needed for the SDIO interface.

**Note:** The Auto-Clock Gate Disable bit can disable this feature.

### 5.28.3.3 Latency Tolerance Reporting

To support Intel Power Optimization, the SDIO controller supports LTR mechanism.

There are two options for how LTR will be handled:

1. In the standard mode, the software will write to the host controllers software LTR register. It is the responsibility of software to update the LTR with the appropriate value based on the bus data rate.



2. In auto mode, the BIOS will write to the “host controllers Auto LTR Active Value” register and software LTR register.
  - a. When the host controller goes active, the reported LTR value will be the value in the Auto LTR register.
  - b. When the host controller goes inactive (idle), the reported LTR value will be taken from the software LTR register

Some Wi-Fi controllers have FIFOs that are insufficient to handle the full 3 ms latency of the maximum LTR value. When this happens, received packets will be lost, resulting in significant performance degradation and higher system power. Thus, the maximum latency value should not be used with these types of devices

## 5.29 Intel® Serial I/O UART Controllers

**Note:**

The PCH integrates two UART controllers supporting up to 3.8 Mbit/s. The controllers can be used in the low-speed, full-speed, and high-speed modes. The controllers are based on the 16550 industry standard and communicate with serial data ports that conform to the RS-232 interface protocol.

**Note:**

For details on supported OS, refer to the *Intel® Serial IO Bus Drivers Product Requirement Document (PRD)*. Refer to IBL/CDI document 526515.

### 5.29.1 Feature Overview

The PCH UART controllers provide the following functionality based on the 16550 industry standard:

- Programmable character properties, such as number of data bits per character (5–8), optional parity bit (with odd or even select), and number of stop bits (1, 1.5, or 2)
- Line break generation and detection.
- DMA signaling with two programmable modes.
- Prioritized interrupt identification.
- Programmable FIFO enable/disable.
- Programmable serial data baud rate

### 5.29.2 DMA Controller Interface

The UART Controllers have an optional built-in DMA handshaking interface to an internal DMA Controller. The interface can be used to request and control transfers.

### 5.29.3 Interrupts

Each UART interface has an interrupt line that is used to notify the driver that service is required. Each interrupt line is assigned to interrupt PCI INT [A-D] or ACPI IRQ[5-7, 13]. All interrupts are active high and their behavior is level interrupt

## 5.29.4 Power Management

Each UART interface will support hardware managed clock gating, Runtime D3 functional clock gating mechanism, and Latency Tolerance Reporting.

### 5.29.4.1 Runtime D3 Support

The power state for each UART interface is set in its respective PCI private Configuration register space. The power state field of the Power Management Control and Status register is used to select the D0 or D3 power state.

### 5.29.4.2 Hardware Managed Clock Gating

The UART controller hardware provides idle detection logic that will be used to locally gate the controller's clocks.

### 5.29.4.3 Latency Tolerance Reporting

To support the Intel® Power Optimization, the PCH SPI controller supports the LTR mechanism.

There are two options for how LTR will be handled:

1. In the standard mode, the software will write to the host controllers software LTR register. It is the responsibility of software to update the LTR with the appropriate value based on the bus data rate.
2. In the auto mode, the BIOS will write to the "host controllers Auto LTR Active Value" register and software LTR register.
  - a. When the host controller goes active, the reported LTR value will be the value in the Auto LTR register.
  - b. When the host controller goes inactive (idle), the reported LTR value will be taken from the software LTR register

## 5.30 Feature Capability Mechanism

A set of registers are included in the PCH LPC Interface (Device 31, Function 0, offset E0h–EBh) that allow the system software or BIOS to easily determine the features supported by the PCH. These registers can be accessed through LPC PCI configuration space; thus, allowing for convenient single point access mechanism for Chipset feature detection.

This set of registers consists of:

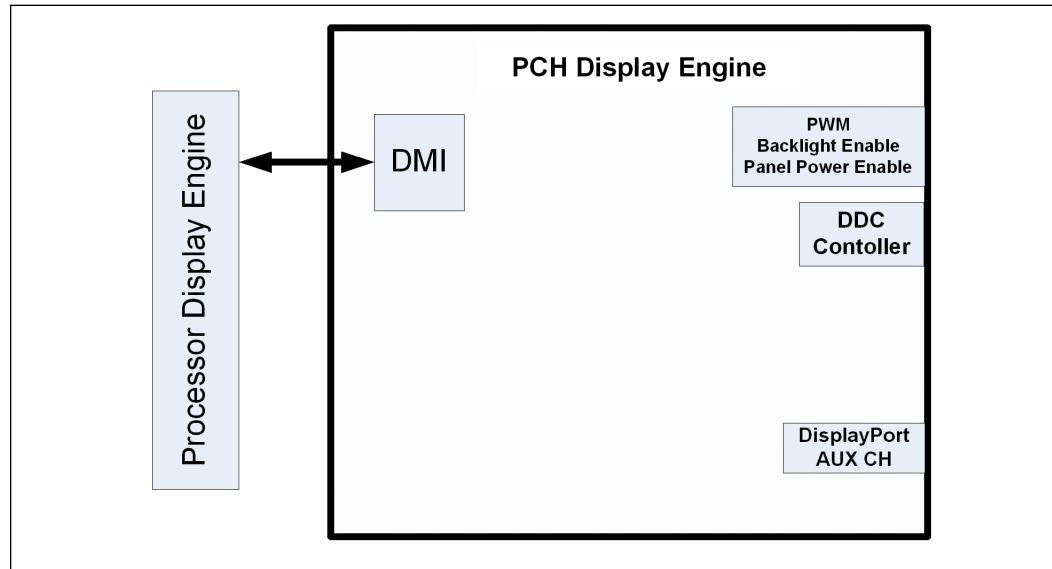
- Capability ID (FDCAP)
- Capability Length (FDLEN)
- Capability Version and Vendor-Specific Capability ID (FDVER)
- Feature Vector (FVECT)

## 5.31 PCH Display Interface

Display is divided between processor and PCH. The processor houses memory interface, display planes, pipes, and digital display interfaces/ports while PCH has transcoder and analog display interface or port. The PCH integrates analog display interface only.

Figure 5-14 shows the PCH Display Architecture.

**Figure 5-14. PCH Display Architecture**



### 5.31.1 Digital Display Side Band Signals

The PCH integrates digital display side band signals AUX CH, DDC bus, and Hot-Plug Detect signals even though digital display interfaces are moved to processor. There are two pairs of AUX CH, DDC Clock/Data, and Hot-Plug Detect signals on the PCH that correspond to digital display interface/ports.

#### 5.31.1.1 DisplayPort\* AUX CH

Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. AUX CH is an AC coupled differential signal.

#### 5.31.1.2 Display Data Channel (DDC)

The DDC bus is used for communication between the host system and display. Three pairs of DDC (DDC\_CLK and DDC\_DATA) signals exist on the PCH that correspond to three digital ports on the processor. DDC follows I<sup>2</sup>C protocol.

#### 5.31.1.3 Hot-Plug Detect

The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device for DisplayPort\* and HDMI\*. It is a 3.3V tolerant signal pin on the PCH.

### 5.31.1.4 Map of Digital Display Side Band Signals Per Display Configuration

Table 5-60 lists PCH display side band signals associated with each digital port in the processor. Depending on whether a digital interface is configured as HDMI\* or DisplayPort\* on the processor, the corresponding signal on the PCH must be routed on the board as indicated by Table 5-60.

**Table 5-60. Display Digital Interface/PCH Signals**

Display Digital Interface	PCH Signals
Digital Display Interface B	Interface Configured as DisplayPort* <ul style="list-style-type: none"> <li>• DDPB_AUXP</li> <li>• DDPB_AUXN</li> </ul> Interface Configured as HDMI* <ul style="list-style-type: none"> <li>• DDPB_CTRLCLK</li> <li>• DDPB_CTRLDATA</li> </ul> Interface Configured as DisplayPort*/HDMI* <ul style="list-style-type: none"> <li>• DDPB_HPD</li> </ul>
Digital Display Interface C	Interface Configured as DisplayPort*           DDPC_AUXP           DDPC_AUXN           Interface Configured as HDMI*           DDPC_CTRLCLK           DDPC_CTRLDATA           Interface Configured as DisplayPort*/HDMI*           DDPC_HPD
Digital Display Interface D	Interface Configured as DisplayPort*           DDPD_AUXP           DDPD_AUXN           Interface Configured as HDMI*           DDPD_CTRLCLK           DDPD_CTRLDATA           Interface Configured as DisplayPort*/HDMI*           DDPD_HPD

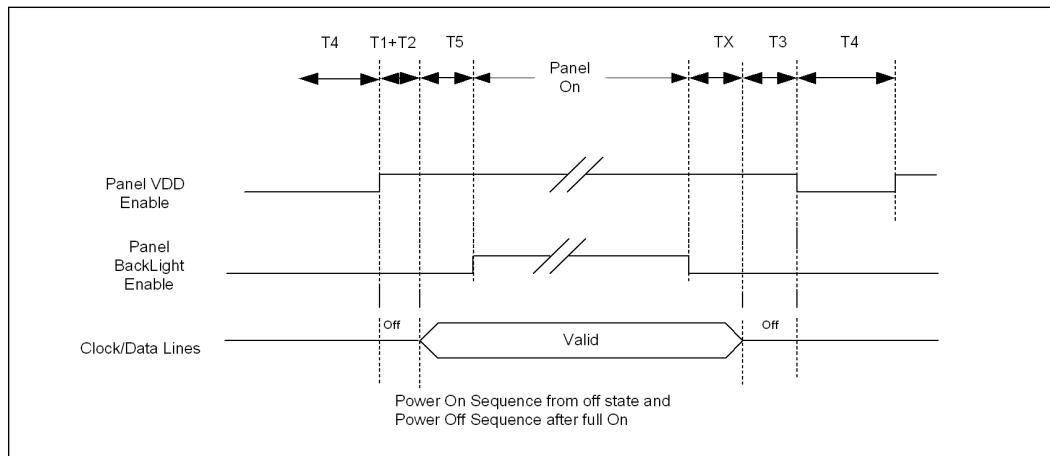
### 5.31.1.5 Panel Power Sequencing and Backlight Control

PCH continues to integrate Panel power sequencing and Backlight control signals for eDP\* interfaces on the processor.

This section provides details for the power sequence timing relationship of the panel power, the backlight enable, and the eDP data timing delivery. To meet the panel power timing specification requirements two signals, eDP\_VDD\_EN and eDP\_BKLT\_EN, are provided to control the timing sequencing function of the panel and the backlight power supplies.

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state, and the eDP data lines are all managed by an internal power sequencer.

**Figure 5-15. Panel Power Sequencing**



**Note:** Support for programming parameters TX and T1 through T5 using software is provided.

### 5.31.1.6 Pulse Width Modulation (PWM) Output Frequency and Calculation

The BKLTCCTL is driven at PWM output frequency with a programmable duty cycle that represents the different brightness levels. Software programs the PWM increment and frequency divider in order to set the frequency, then enables the backlight (BKLTCEN), then programs the duty cycle as needed to adjust the brightness level. Below are the valid settings:

- PWM clock frequency = 24 MHz
- PWM increment = 128 or 16, selectable by software
- PWM frequency divider maximum = 65,536
  - PWM output frequency range with 100 brightness levels and increment 128 = 3 to 1,875 Hz
  - PWM output frequency range with 100 brightness levels and increment 16 = 23 to 15,000 Hz
  - PWM output frequency range with 256 brightness levels and increment 128 = 3 to 732 Hz
  - PWM output frequency range with 256 brightness levels and increment 16 = 23 to 5,859 Hz

## 5.32 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows for multiple, independent operating systems to be running simultaneously on a single system. Intel® VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. The first revision of this technology (Intel® VT-x) added hardware support in the processor to improve the virtualization performance and robustness. The second revision of this specification (Intel® VT-d) adds Chipset hardware implementation to improve I/O performance and robustness.

The Intel® VT-d specification and other Intel® VT documents can be referenced here: <http://www.intel.com/technology/platform-technology/virtualization/index.htm>

### 5.32.1 Intel® VT-d Objectives

The key Intel® VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Virtualization allows for the creation of one or more partitions on a single system. This could be multiple partitions in the same operating system or there can be multiple operating system instances running on the same system offering benefits such as system consolidation, legacy migration, activity partitioning or security.

### 5.32.2 Intel® VT-d Features Supported

- The following devices and functions support FLR in the PCH:
  - High Definition Audio (Device 27: Function 0)
  - SATA Host Controller 1 (Device 31: Function 2)
  - USB 2.0 (EHCI) Host Controller 1 (Device 29: Function 0)
  - USB 2.0 (EHCI) Host Controller 2 (Device 26: Function 0)
  - GbE Lan Host Controller (Device 25: Function 0)
- Interrupt virtualization support for IOxAPIC
- Virtualization support for HPETs

### 5.32.3 Support for Function Level Reset (FLR) in PCH

Intel® VT-d allows system software (VMM/OS) to assign I/O devices to multiple domains. The system software, then, requires ways to reset I/O devices or their functions within, as it assigns/re-assigns I/O devices from one domain to another. The reset capability is required to ensure the devices have undergone proper re-initialization and are not keeping the stale state. A standard ability to reset I/O devices is also useful for the VMM in case where a guest domain with assigned devices has become unresponsive or has crashed.

PCI Express\* defines a form of device hot reset that can be initiated through the Bridge Control register of the root/switch port to which the device is attached. However, the hot reset cannot be applied selectively to specific device functions. Also, no similar standard functionality exists for resetting root-complex integrated devices.

Current reset limitations can be addressed through a *function level reset* (FLR) mechanism that allows software to independently reset specific device functions.

### 5.32.4 Virtualization Support for PCH IOxAPIC

The Intel® VT-d architecture extension requires Interrupt Messages to go through the similar address remapping as any other memory request. This is to allow domain isolation for interrupts such that a device assigned in one domain is not allowed to generate interrupts to another domain.

The address remapping for Intel® VT-d is based on the Bus:Device:Function field associated with the requests. Hence, it is required for the internal IOxAPIC to initiate the Interrupt Messages using a unique Bus:Device:Function.

The PCH supports BIOS programmable unique Bus:Device:Function for the internal IOxAPIC. The Bus:Device:Function field does not change the IOxAPIC functionality in anyway, nor promoting IOxAPIC as a stand-alone device. The field is only used by the IOxAPIC in the following:

- As the Requestor ID when initiating Interrupt Messages to the processor
- As the Completer ID when responding to the reads targeting the IOxAPIC's Memory-Mapped I/O registers



### 5.32.5 Virtualization Support for High Precision Event Timer (HPET)

The Intel® VT-d architecture extension requires Interrupt Messages to go through the similar address remapping as any other memory request. This is to allow domain isolation for interrupts such that a device assigned in one domain is not allowed to generate interrupts to another domain.

The address remapping for Intel® VT-d is based on the Bus:Device:Function field associated with the requests. Hence, it is required for the HPET to initiate processor message interrupts using unique Bus:Device:Function.

The PCH supports BIOS programmable unique Bus:Device:Function for each of the HPET timers. The Bus:Device:Function field does not change the HPET functionality in any way, nor promoting it as a stand-alone device. The field is only used by the HPET timer in the following:

- As the Requestor ID when initiating processor message interrupts to the processor
- As the Completer ID when responding to the reads targeting its Memory-Mapped registers
- The registers for the programmable Bus:Device:Function for HPET timer 7:0 reside under the D31:F0 LPC Bridge's configuration space.

## 5.33 Intel® Smart Sound Technology (Intel® SST) (D19:F0)

The PCH provides integrated audio DSP capabilities. This feature is to provide DSP capabilities to the codec attached through the PCM/I<sup>2</sup>S interface. The goal of the SST subsystem is to provide hardware acceleration for common audio and voice functions such as audio encode/decode, acoustic echo cancellation, noise cancellation, and so on. With such acceleration, the PCH is expected to enable platforms to provide longer music playback times and VOIP call times

### 5.33.1 Intel® Smart Sound Technology (Intel® SST) Subsystem Overview

The Intel® SST subsystem consists of:

- 320 MHz DSP Core
- DSP tightly-coupled memories
  - 320KB instruction SRAM
  - 640KB data SRAM
- DSP Configuration registers
- 2 x DMA engines (8 channels each) with each channel operating independently
- 2 x I<sup>2</sup>S audio codec interfaces for connection low power audio and Bluetooth® codecs.

## 5.34 Intel® Rapid Storage Technology (Intel® RST) for PCIe\* Storage

Intel® Rapid Storage Technology for PCIe\* Storage provides an aggregation point for PCIe\* and SATA storage devices enabling both of them to be controlled by the Intel® RST driver. This Chipset feature allows a high performance PCIe\* SSD device to be used as a stand-alone SSD with the Intel® RST driver. For systems using Intel® Smart Response Technology, this feature can be used to enable a PCIe\* SSD to cache a SATA HDD though they are physically separate devices on different interfaces.

Intel® Rapid Storage Technology for PCIe\* Storage is disabled by default upon PLTRST# de-assertion. During the discovery and initialization, BIOS enables this feature if functionality is required. Once enabled, this feature must not be disabled without going through the PLTRST#.

### 5.34.1 Supported Features Summary

#### Intel® Rapid Storage Technology for PCIe\* Storage

- A single PCIe\* SSD device (AHCI or NVM Express)
- PCIe\* x1 or x2 Gen2 interconnect

**Note:**

x4 is not supported)

- 128 byte maximum payload size
- Early power shutdown indication through the PME\_Turn\_Off message
- Only Intel® RST driver supported
- Driving the SATALED# pin on behalf of the Intel® Rapid Storage Technology for PCIe\* Storage device by means of the Intel vendor specific VDM over the PCIe\* interface
- BIOS-assist during boot for the discovery and initialization sequence

The PCH supports multiplexing of the Intel® Rapid Storage Technology for PCIe\* Storage device onto selected PCIe\* lanes, including the multiplexed SATA/PCIe\* Flex I/O lanes. Refer to [Table 2-3](#) and [Table 11-3](#) for the PCH SKU Flexible I/O Map.

- x2 on Ports 11 and 12

**Note:**

Hot-plug is not supported on PCIe\* lanes enabled for the Intel® Rapid Storage Technology for PCIe\* Storage.

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# 6

# Electrical Characteristics

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This chapter contains the DC and AC characteristics for the PCH. AC timing diagrams are included.

## 6.1 Absolute Maximum Ratings

**Table 6-1. PCH Absolute Maximum Ratings**

Parameter	Maximum Limits
Voltage on any 3.3V Pin with respect to Ground	-0.5 to Vcc3_3 + 0.4V, Absolute maximum = 3.7V
Voltage on any 1.8V Pin with respect to Ground	-0.5 to VCC1_8 + 0.5V
Voltage on any 1.5V Pin with respect to Ground	-0.5 to VCC1_5 + 0.5V
Voltage on any 1.05V Pin with respect to Ground	-0.5 to 1.3V
1.05V Supply Voltage with respect to Ground	-0.5 to 1.3V
1.5V Supply Voltage with respect to Ground	-0.5 to 1.8V
1.8V Supply Voltage with respect to Ground	-0.5 to 2.3V
3.3V Supply Voltage with respect to Ground	-0.5 to 3.7V

**Table 6-1** specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the PCH contains protective circuitry to resist damage from Electrostatic Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

## 6.2 PCH Power Supply Range

**Table 6-2. PCH Power Supply Range**

Power Supply	Minimum	Nominal	Maximum
1.05V	0.998V	1.05V	1.10V
1.5V	1.43V	1.50V	1.58V
1.8V	1.71V	1.80V	1.89V
3.3V	3.14V	3.30V	3.47V

## 6.3 General DC Characteristics

**Table 6-3. Mobile 5th Generation Intel® Core™ Processor Family I/O, Mobile Intel® Pentium® Processor Family I/O, and Intel® Celeron® Processor Family I/O Measured  $I_{cc}^{10}$**

Voltage Rail	Voltage (V)	$I_{cc\max}$ Current (A) <sup>3</sup>	$I_{cc\text{idle}}$ Current (A) <sup>3</sup>	$I_{cc\text{idle}}$ Current (A) <sup>3</sup>	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	2.063 <sup>8,9</sup>	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.954 <sup>8,9</sup>	0	0	
VCCAPLL	1.05	0.057 <sup>7,9</sup>	0	0	0
VCCSATA3PLL	1.05	0.043 <sup>5,9</sup>	0	0	0
VCCUSB3PLL	1.05	0.042 <sup>5,9</sup>	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.185	0	0	0
VCCHSIO	1.05	1.878 <sup>5,6,9</sup>	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCSDIO	1.8	0.010	0	0	0
VCCASW	1.05	0.658	0.019	0	0
VCCSPI	3.3	0.018	<1mA	0	0
VCCHDA	3.3	0.011	0	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.065	0.008	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.002	0	0
DcpSus1 <sup>4</sup>	1.05	0.109	0.003	0	0
DcpSus2 <sup>4</sup>	1.05	0.025	0.000	0	0
DcpSus3 <sup>4</sup>	1.05	0.010	0.002	0	0
DcpSus4 <sup>4</sup>	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.119	0.002	0.002	0
VCCRTC	3.3	<1mA	<1mA	<1mA	6µA See notes 1, 2

**NOTE:**

1. G3 state shown to provide an estimate of battery life.
2.  $I_{cc}$  (RTC) data is taken with VCCRTC at 3.0V while the system is in a mechanical off (G3) state at room temperature.
3.  $I_{cc\max}$  estimates assumes 110 °C.
4. This applies to External Suspend VR powered mode. In Internal Suspend VR mode, DcpSus1, DcpSus2, DcpSus3, DcpSus4 is a No Connect and hence  $I_{cc\max}$  information is not applicable.
5.  $I_{cc\max}$  is <1mA when HSIO is power gated
6. Assumes maximum configuration of 4 SATA ports, 8 PCIe\* Lanes, 2-USB 3.0 ports.  $I_{cc\max}$  can be reduced by: 129mA for each SATA port disabled, 124mA for each PCIe\* Lane disabled and 105mA for each USB 3.0 port disabled.
7. 43 mA when all USB 2.0 ports are disabled.
8.  $I_{cc\max}$  reduced by 26.8mA per un-used USB 2.0 port.
9.  $I_{cc\max}$  reduction is an estimated guidance.

10. The  $I_{ccmax}$  value is a steady state current that can happen after respective power ok has asserted (or reset signal has de-asserted).

**Table 6-4. Intel® Core™ M Processor I/O Platform Measured  $I_{cc}$ <sup>13</sup>**

Voltage Rail	Voltage (V)	$S_0$ $I_{ccmax}$ Current (A) <sup>3</sup>	$S_x$ $I_{cc}$ Idle Current (A) <sup>3</sup>	Deep $S_x$ $I_{cc}$ Idle Current (A) <sup>3</sup>	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.765	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.656	0	0	0
VCC1_05_PHY	1.05	0.045	0	0	0
VCC1_05_USB	1.05	0.270 <sup>11,12</sup>	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCHDAPLL	1.05	0.030	0	0	0
VCCOPIPLL	1.05	0.011	0	0	0
VCCSATA3PLL	1.05	0.043 <sup>9,12</sup>	0	0	0
VCCUSB3PLL	1.05	0.042 <sup>9,12</sup>	0	0	0
VCCUSB2PLL	1.05	0.016 <sup>10,12</sup>	0	0	0
VCCPCIEPHY	1.05	0.802 <sup>6,9,12</sup>	0	0	0
VCCSATAPHY	1.05	0.564 <sup>7,9,12</sup>	0	0	0
VCCUSB3PHY	1.05	0.511 <sup>8,9,12</sup>	0	0	0
VCCCLK1	1.05	0.004	0	0	0
VCCCLK2	1.05	0.004	0	0	0
VCCCLK3	1.05	0.004	0	0	0
VCCCLK4	1.05	0.093	0	0	0
VCCCLK5	1.05	0.014	0	0	0
VCCCLK6	1.05	0.053	0	0	0
VCCCLK7	1.05	0.014	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCCTS3_3	3.3	0.001	0	0	0
VCC3_3	3.3	0.040	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCSDIO	1.8	0.010	0	0	0
VCCASW	1.05	0.658	0.019 <sup>5</sup>	0	0
VCCSPI	3.3	0.018	<1mA	0	0
VCCHDA	3.3	0.011	0	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.065	0.008	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.002	0	0
VCCSUS3_3_RTC	3.3	0.000	0.000	0	0
DcpSus1 <sup>4</sup>	1.05	0.109	0.003	0	0
DcpSus2 <sup>4</sup>	1.05	0.025	0.000	0	0
DcpSus3 <sup>4</sup>	1.05	0.010	0.002	0	0

Table 6-4. Intel® Core™ M Processor I/O Platform Measured  $I_{cc}$ <sup>13</sup>

Voltage Rail	Voltage (V)	S0 Iccmax Current (A) <sup>3</sup>	Sx Icc Idle Current (A) <sup>3</sup>	Deep Sx Icc Idle Current (A) <sup>3</sup>	G3
DcpSus4 <sup>4</sup>	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.002	0.002	0
VCCRTC	3.3	<1mA	<1mA	<1mA	6µA See notes 1, 2

**NOTE:**

1. G3 state shown to provide an estimate of battery life.
2. Icc (RTC) data is taken with VCCRTC at 3.0V while the system is in a mechanical off (G3) state at room temperature.
3. Iccmax estimates assumes 110 °C.
4. This applies to External Suspend VR powered mode. In Internal Suspend VR mode, DcpSus1, DcpSus2, DcpSus3, DcpSus4 is a No Connect and hence Iccmax information is not applicable.
5. Iccmax for VCCASW is base on Sx/M3
6. Calculation based on 182mA for 1st PCIe lane enabled + 124mA for each additional PCIe\* lane. Iccmax number assumes PCIe\* Ports 3, 4, and 5 are enabled (total of 6 PCIe\* lanes).
7. Calculation based on 158mA for 1st SATA port + 129mA for each additional SATA port. Iccmax number assumes all 4 SATA ports are enabled.
8. Calculation based on 53mA constant + 105mA for each USB 3.0 port, 124mA for each PCIe\* lane. Iccmax number assumes 2 PCIe\* lane (that is, PCIe\* Ports 1 and 2) and 2-USB 3.0 ports are enabled.
9. Iccmax is <1mA when respective MPHY rail is power gated.
10. Iccmax is <1mA when all USB 2.0 ports are disabled.
11. 26.8mA per USB 2.0 port. Iccmax number assumes all 10, USB 2.0 ports are enabled.
12. Iccmax reduction is provided as estimated guidance.
13. The Iccmax value is a steady state current that can happen after respective power ok has asserted (or reset signal has de-asserted).

Table 6-5. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 1 of 7)

Type	Symbol	Parameter	Minimum	Maximum	Unit	Condition	Notes
		Associated Signals: LFRAME#, LAD[3:0], PME#, PLTRST#, SLP_S0#, SERIRQ, SPI_IO3, SPI_IO2, SPI_MOSI, SPI_MISO, SPI_CLK, SPI_CS[2:0]#, OC[3:0]#/GPIO[43:40], PCIECLKRQ[5:0]#/GPIO[23:18], SATA[3:0]GP/GPIO[37:34], DEVSLP[2:0]/GPIO[39,38,33], HSIOPC/GPIO71, SPKR/GPIO81, CLKRUN#/GPIO32, BMBUSY#/GPIO76, LAN_PHY_PWR_CTRL/GPIO12, BATLOW#/GPIO72, GPIO[59, 56, 49:44, 27, 25, 17:13, 10:8]					2
Input	V <sub>CC</sub>	Supply Voltage Reference	3.14	3.47	V		
	V <sub>IH</sub>	Input High Voltage	0.5 x V <sub>CC</sub>	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.3 x V <sub>CC</sub>	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		3
Output	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
	V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> - 0.5	V <sub>CC</sub>	V	I <sub>oh</sub> =-0.5mA	1
	V <sub>OL</sub>	Output Low Voltage	0	0.4	V	I <sub>ol</sub> =1.5mA	

**Table 6-5. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 2 of 7)**

Type	Symbol	Parameter	Minimum	Maximum	Unit	Condition	Notes
Associated Signals: UART0_RXD/GPIO91, UART0_TXD/GPIO92, UART0_RTS#/GPIO93, UART0_CTS#/GPIO94, UART1_RXD/GPIO0, UART1_TXD/GPIO1, UART1_RST#/GPIO2, UART1_CTS#/GPIO3, GSPI0_CS#/GPIO83, GSPI0_CLK/GPIO84, GSPI0_MISO/GPIO85, GSPI0_MOSI/GPIO86, GSPI1_CS#/GPIO87, GSPI1_CLK/GPIO88, GSPI1_MISO/GPIO89, GSPI1_MOSI/GPIO90							2
	V <sub>CC</sub>	Supply Voltage Reference	3.14	3.47	V		
Input	V <sub>IH</sub>	Input High Voltage	0.5 × V <sub>CC</sub>	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.3 × V <sub>CC</sub>	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	0.9 × V <sub>CC</sub>	—	V	I <sub>oh</sub> =-0.5mA	1
	V <sub>OL</sub>	Output Low Voltage	—	0.1 × V <sub>CC</sub>	V	I <sub>ol</sub> =1.5mA	
	R <sub>out</sub>	Output Drive Resistance	40	63	Ω	V <sub>pad</sub> =V <sub>CC</sub> /2	
	R <sub>pu</sub>	WPU Resistance	14	28	KΩ	V <sub>pad</sub> =V <sub>CC</sub> /2	
	R <sub>pd</sub>	WPD Resistance	14	28	KΩ	V <sub>pad</sub> =V <sub>CC</sub> /2	
Associated Signals: SDIO_CLK/GPIO64, SDIO_CMD/GPIO65, SDIO_D0/GPIO66, SDIO_D1/GPIO67, SDIO_D2/GPIO68, SDIO_D3/GPIO69, SDIO_POWER_EN/GPIO70							2
3.3V Operation							
	V <sub>CC</sub>	Supply Voltage Reference	3.14	3.47	V		
Input	V <sub>IH</sub>	Input High Voltage	0.625 × V <sub>CC</sub>	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.25 × V <sub>CC</sub>	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	0.9 × V <sub>CC</sub>	—	V	I <sub>oh</sub> =-0.5mA	1
	V <sub>OL</sub>	Output Low Voltage	—	0.1 × V <sub>CC</sub>	V	I <sub>ol</sub> =1.5mA	
	R <sub>out</sub>	Output Drive Resistance	40	63	Ω	V <sub>pad</sub> =V <sub>CC</sub> /2	
	R <sub>pu</sub>	WPU Resistance	14	28	KΩ	V <sub>pad</sub> =V <sub>CC</sub> /2	
	R <sub>pd</sub>	WPD Resistance	14	28	KΩ	V <sub>pad</sub> =V <sub>CC</sub> /2	
1.8V Operation							
	V <sub>CC</sub>	Supply Voltage Reference	1.71	1.89	V		
Input	V <sub>IH</sub>	Input High Voltage	1.27	V <sub>CC</sub> + 0.5	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.58	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		

Table 6-5. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 3 of 7)

Type	Symbol	Parameter	Minimum	Maximum	Unit	Condition	Notes
Output	V <sub>OH</sub>	Output High Voltage	0.9 × V <sub>CC</sub>	—	V	I <sub>oh</sub> =-0.5mA	1
	V <sub>OL</sub>	Output Low Voltage	—	0.1 × V <sub>CC</sub>	V	I <sub>ol</sub> =1.5mA	
	R <sub>out</sub>	Output Drive Resistance	40	63	Ω	V <sub>pad</sub> =V <sub>CC</sub> /2	
	R <sub>pu</sub>	WPU Resistance	20	50	KΩ	V <sub>pad</sub> =V <sub>CC</sub> /2	
	R <sub>pd</sub>	WPD Resistance	20	50	KΩ	V <sub>pad</sub> =V <sub>CC</sub> /2	
Associated Signals: ACPRESENT/GPIO31, SLP_LAN#, PWRBTN#, SLP_S4#, SLP_A#, SLP_WLAN#/GPIO29, SLP_S3#, SLP_SUS#, WAKE#, SLP_S5#/GPIO63, SM_DRAMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, SUSACK#, SUS_STAT#/GPIO61, SUSCLK/GPIO62, CL_RST#, SYS_RESET#, SATALED#, RCIN#/GPIO82, PIRQ[D:A]#/GPIO[80:77], GPIO[57, 55:50, 28, 26, 24]							2
	V <sub>CC</sub>	Supply Voltage Reference	3.14	3.47	V		
Input	V <sub>HYS</sub>	Schmitt Trigger Hysteresis	250	—	mV		
	V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	μA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> - 0.5	V <sub>CC</sub>	V	I <sub>oh</sub> =-4.5mA	1
	V <sub>OL</sub>	Output Low Voltage	0	0.4	V	I <sub>ol</sub> =4.5mA	
Associated Signals: SMBALERT#/GPIO11, SMBCLK, SMBDATA, SML0ALERT#/GPIO60, SML0CLK, SML0DATA, SML1ALERT#/PCHHOT#/GPIO73, SML1CLK/GPIO75, SML1DATA/GPIO74, GPIO58							2
	V <sub>CC</sub>	Supply Voltage Reference	3.14	3.47	V		
	V <sub>HYS</sub>	Schmitt Trigger Hysteresis	0.1 × V <sub>CC</sub>	—	V		
Input	V <sub>IH</sub>	Input High Voltage	2.1	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	μA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> - 0.5	V <sub>CC</sub>	V	I <sub>oh</sub> =-1mA	1
	V <sub>OL</sub>	Output Low Voltage	0	0.4	V	I <sub>ol</sub> =4mA	
-	V <sub>NOISE</sub>	Signal Noise Immunity from 10 MHz to 100 MHz	300	—	mV		
	C <sub>BUS</sub>	Capacitive Load per Bus Segment	—	400	pF		4
Associated Signals: I2C0_SDA/GPIO4, I2C0_SCL/GPIO5, I2C1_SDA/GPIO6, I2C1_SCL/GPIO7							2
Standard mode 100Kbits/s, Fast Mode 400Kbit/s, Fast Mode Plus 1Mbit/s							
	V <sub>CC</sub>	Nominal Bus Voltage	3.14	3.47	V		
	V <sub>CC18</sub>	Nominal Bus Voltage for 1.8V signaling	1.71	1.89	V		

**Table 6-5. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 4 of 7)**

Type	Symbol	Parameter	Minimum	Maximum	Unit	Condition	Notes
	V <sub>HYS</sub>	Schmitt Trigger Hysteresis	0.1 × V <sub>CC</sub>		V		
Input	V <sub>IH</sub>	Input High Voltage	2.1	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	V		
	V <sub>IH18</sub>	Input High Voltage for 1.8V signaling	0.7 × V <sub>CC18</sub>	V <sub>CC18</sub>	V		
	V <sub>IL18</sub>	Input Low Voltage for 1.8V signaling	-0.5	0.3 × V <sub>CC18</sub>	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> - 0.5	V <sub>CC</sub>	V	I <sub>oh</sub> =-1mA	1
	V <sub>OL</sub>	Output Low Voltage	0	0.4	V	I <sub>ol</sub> =4mA	
-	V <sub>NOISE</sub>	Signal Noise Immunity From 10 MHz to 100 MHz	300	—	mV		
	V <sub>NOISE18</sub>	Signal Noise Immunity From 10 MHz to 100 MHz	200	—	mV		
	C <sub>BUS</sub>	Capacitive Load per Bus Segment	—	400	pF		4
Associated Signals: eDP_BKL滕, eDP_BKL滕CTL, eDP_VDDEN, DDPB_CTRLCLK, DDPC_CTRLCLK, DDPB_CTRLDATA, DDPC_CTRLDATA							2
Standard mode 100Kbit/s, Fast Mode 400Kbit/s, Fast Mode Plus 1Mbit/s							
	V <sub>CC</sub>	Supply Voltage Reference	3.14	3.47	V		
Input	V <sub>HYS</sub>	Schmitt Trigger Hysteresis	0.1 × V <sub>CC</sub>	—	V		
	V <sub>IH</sub>	Input High Voltage	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.3 × V <sub>CC</sub>	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> - 0.5	V <sub>CC</sub>	V	I <sub>oh</sub> =-1mA	
	V <sub>OL</sub>	Low Level Output Voltage	0.0	0.4	V	I <sub>ol</sub> =4mA	
Associated Signals: SYS_PWROK, APWROK							2
	V <sub>CC</sub>	Supply Voltage Reference	3.14	3.47	V		
Input	V <sub>HYS</sub>	Schmitt Trigger Hysteresis	250	—	mV		
	V <sub>IH</sub>	Input High Voltage	2.1	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		

Table 6-5. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 5 of 7)

Type	Symbol	Parameter	Minimum	Maximum	Unit	Condition	Notes
Associated Signals: JTAGX, PCH_TDO, PCH_TMS, PCH_TDI, PCH_TCK, PCH_TRST#							2, 12
	VCC	Supply Voltage Reference	0.998	1.10	V		
Input	V <sub>IH</sub>	Input High Voltage	GTL: 0.8 CMOS:0.6	V <sub>CC</sub> + 0.25	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	GTL: 0.5 CMOS:0.4	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	μA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	0.75	V <sub>CC</sub>	V	I <sub>oh</sub> =-0.5mA	1
	V <sub>OL</sub>	Output Low Voltage	0	0.3	V	I <sub>ol</sub> =0.5mA	
Associated Signals: CL_DATA, CL_CLK							2
	CL_VRef	Supply Voltage Reference	0.12 x VCCSUS3_3	0.12 x VCCSUS3_3	V		
Input	V <sub>HYS</sub>	Schmitt Trigger Hysteresis	100	—	mV		
	V <sub>IH</sub>	Input High Voltage	CL_Vref + 0.075	1.2	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	CL_Vref - 0.075	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	μA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	610		mV	R <sub>load</sub> = 100 ohm to GND	1
	V <sub>OL</sub>	Output Low Voltage	0	150	mV	I <sub>ol</sub> =1mA	
Associated Signals: HDA_SDO/I2S0_TXD, HDA_SYNC/I2S0_SFRM, HDA_SDI1/I2S1_RXD, HDA_RST#/I2S_MCLK, HDA.Dock_EN#/I2S1_TXD, HDA_BCLK/I2S0_SCLK, HDA_SDI0/I2S0_RXD, HDA.Dock_RST#/I2S1_SFRM, I2S1_SCLK							2, 7
	VCC	Supply Voltage Reference	3.14	3.47	V		
Input	V <sub>IH</sub>	Input High Voltage	0.65 x V <sub>CC</sub>	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.35 x V <sub>CC</sub>	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	μA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	0.9 x V <sub>CC</sub>	V <sub>CC</sub>	V	I <sub>oh</sub> =-0.5mA	
	V <sub>OL</sub>	Output Low Voltage	0	0.1 x V <sub>CC</sub>	V	I <sub>ol</sub> =1.5mA	
Associated Signals: HDA_SDO/I2S0_TXD, HDA_SYNC/I2S0_SFRM, HDA_SDI1/I2S1_RXD, HDA_RST#/I2S_MCLK, HDA.Dock_EN#/I2S1_TXD, HDA_BCLK/I2S0_SCLK, HDA_SDI0/I2S0_RXD, HDA.Dock_RST#/I2S1_SFRM, I2S1_SCLK							2, 8
	VCC	Supply Voltage Reference	1.71	1.89	V		

**Table 6-5. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 6 of 7)**

Type	Symbol	Parameter	Minimum	Maximum	Unit	Condition	Notes
Input	V <sub>IH</sub>	Input High Voltage	0.6 x V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.4 x V <sub>CC</sub>	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	0.9 x V <sub>CC</sub>	V <sub>CC</sub>	V	I <sub>oh</sub> =-0.5mA	
	V <sub>OL</sub>	Output Low Voltage	0	0.1 x V <sub>CC</sub>	V	I <sub>ol</sub> =1.5mA	
Associated Signals: HDA_SDO/I2S0_TXD, HDA_SYNC/I2S0_SFRM, HDA_SDI1/I2S1_RXD, HDA_RST#/I2S_MCLK, HDA.Dock_EN#/I2S1_TXD, HDA_BCLK/I2S0_SCLK, HDA_SDI0/I2S0_RXD, HDA.Dock_RST#/I2S1_SFRM, I2S1_SCLK							2, 7
	V <sub>CC</sub>	Supply Voltage Reference	1.43	1.58	V		
Input	V <sub>IH</sub>	Input High Voltage	0.6 x V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.4 x V <sub>CC</sub>	V		
	I <sub>IL</sub>	Input Leakage Current	-10	10	µA		
	C <sub>IN</sub>	Input Pin Capacitance	—	10	pF		
Output	V <sub>OH</sub>	Output High Voltage	0.9 x V <sub>CC</sub>	V <sub>CC</sub>	V	I <sub>oh</sub> =-0.5mA	
	V <sub>OL</sub>	Output Low Voltage	0	0.1 x V <sub>CC</sub>	V	I <sub>ol</sub> =1.5mA	
Associated Signals: DDPB_HPD, DDPC_HPD, eDP_HPD							2
	V <sub>CC</sub>	Supply Voltage Reference	3.14	3.47	V		
Input	V <sub>HYS</sub>	Schmitt Trigger Hysteresis	200	—	mV		
	V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 0.4	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.8	V		
	I <sub>IL</sub>	Input Leakage Current	0	10	µA		
Associated Signals: RSMRST#, INTVRMEN, SRTCRLST#, INTRUDER#, PCH_PWROK, DPWROK, DSWVRMEN							
Input	V <sub>IH</sub>	Input High Voltage	0.65 x V <sub>CRCR</sub>	V <sub>CRCR</sub> +0.5	V		6, 11
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.3 x V <sub>CRCR</sub>	V		11
Associated Signals: RTCRST#							
Input	V <sub>IH</sub>	Input High Voltage	0.75 x V <sub>CRCR</sub>	V <sub>CRCR</sub> +0.5	V		6, 10, 11
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.4 x V <sub>CRCR</sub>	V		10, 11
Associated Signals: RTCX1							
Input	V <sub>IH</sub>	Input High Voltage	0.8	1.2	V		
	V <sub>IL</sub>	Input Low Voltage	-0.5	0.1	V		

Table 6-5. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 7 of 7)

Type	Symbol	Parameter	Minimum	Maximum	Unit	Condition	Notes
Associated Signals: XTAL24_IN							9
Input	$V_{IH}$	Input High Voltage	0.7	1.2	V		
	$V_{IL}$	Input Low Voltage	-0.25	0.15	V		
Associated Signals: CLKOUT_LPC[1:0]							9
Input	$V_{OL}$	Output Low Voltage	-	0.4	V	-1mA	
	$V_{OH}$	Output High Voltage	2.4	-	V	1mA	

**NOTES:**

1. The  $V_{OH}$  specification does not apply to open-collector or open-drain drivers. Signals of this type must have an external pull-up resistor, and that is what determines the high-output voltage level. Refer to [Chapter 2](#) for details on signal types.
2. Input characteristics apply when a signal is configured as Input or to signals that are only Inputs. Output characteristics apply when a signal is configured as an Output or to signals that are only Outputs. Refer to [Chapter 2](#) for details on signal types.
3. PME# Input Current Leakage is 1  $\mu$ A maximum
4. Only applies to Fast Mode Plus (1Mbit/s). Standard and Fast Mode can handle full 550 pF per industry specification.
5. The PCH pins do not have tolerance for 5V.
6. VCCRTC is the voltage applied to the VCCRTC well of the PCH. When the system is in a G3 state, this is generally supplied by the coin cell battery, but for S5 and greater, this is generally VCCSUS3\_3.
7. Refer to HD Audio Specification for AC drive current templates.
8. Nominal output drive resistance = 20 ohms @  $V_{cc}/2$
9. Vpk-pk minimum for XTAL24 = 500mV
10.  $V_{IHmin}$  should not be used as the reference point for T200 timing. See T200 specification for measurement point details.
11. These buffers have input hysteresis.  $V_{IH}$  levels are for rising edge transitions and  $V_{IL}$  levels are for falling edge transitions.
12. The PCH\_TCK buffer type is CMOS. JTAGX, PCH\_TDO, PCH\_TMS, and PCH\_TDI are GTL.

Table 6-6. Differential Signal DC Characteristics (Sheet 1 of 3)

Symbol	Parameter	Minimum	Maximum	Unit	Conditions	Notes
Associated Signals: <b>PERn[2:1]</b> /USB3Rn[4:3], <b>PERp[2:1]</b> /USB3Rp[4:3], <b>PETn[2:1]</b> /USB3Tn[4:3], <b>PETp[2:1]</b> /USB3Tp[4:3], <b>PERn[4:3]</b> , <b>PERp[4:3]</b> , <b>PETn[4:3]</b> , <b>PETp[4:3]</b> , <b>PERn5_L[3:0]</b> , <b>PERp5_L[3:0]</b> , <b>PETn5_L[3:0]</b> , <b>PETp5_L[3:0]</b> , <b>SATA_Rn[3:0]</b> / <b>PERn6_L[0:3]</b> , <b>SATA_Rp[3:0]</b> / <b>PERp6_L[0:3]</b> , <b>SATA_Tn[3:0]</b> / <b>PETn6_L[0:3]</b> , <b>SATA_Tp[3:0]</b> / <b>PETp6_L[0:3]</b>					9	
VTX-DIFF P-P	Differential Peak to Peak Output Voltage	0.8	1.2	V		1
VTX-DIFF P-P - Low	Low power differential Peak to Peak Output Voltage	0.4	1.2	V		
VTX_CM-ACp	TX AC Common Mode Output Voltage (2.5 GT/s)	—	20	mV		
ZTX-DIFF-DC	DC Differential TX Impedance	80	120	Ω		
VRX-DIFF p-p	Differential Input Peak to Peak Voltage	0.175	1.2	V		1
VRX_CM-ACp	AC peak Common Mode Input Voltage	—	150	mV		
Gen 2						
VTX-DIFF P-P	Differential Peak to Peak Output Voltage	0.8	1.2	V		
VTX-DIFF P-P - Low	Low power differential Peak to Peak Output Voltage	0.4	1.2	V		
VTX_CM-Acp-p	TX AC Common Mode Output Voltage (5GT/s)	—	100	mV		
ZTX-DIFF-DC	DC Differential TX Impedance	80	120	Ω		
VRX-DIFF p-p	Differential Input Peak to Peak Voltage	0.1	1.2	V		
VRX_CM-ACp	AC peak Common Mode Input Voltage	—	150	mV		
Associated Signals: <b>SATA_Rn[3:0]</b> / <b>PERn6_L[0:3]</b> , <b>SATA_Rp[3:0]</b> / <b>PERp6_L[0:3]</b> , <b>SATA_Tn[3:0]</b> / <b>PETn6_L[0:3]</b> , <b>SATA_Tp[3:0]</b> / <b>PETp6_L[0:3]</b>						
VIMIN- Gen1i	Minimum Input Voltage - 1.5Gb/s internal SATA	325	—	mVdiff p-p		2
VIMAX-Gen1i	Maximum Input Voltage - 1.5Gb/s internal SATA	—	600	mVdiff p-p		2
VIMIN-Gen1m	Minimum Input Voltage - 1.5Gb/s eSATA	240	—	mVdiff p-p		2
VIMAX-Gen1m	Maximum Input Voltage - 1.5Gb/s eSATA	—	600	mVdiff p-p		2
VIMIN-Gen2i	Minimum Input Voltage - 3.0Gb/s internal SATA	275	—	mVdiff p-p		2
VIMAX-Gen2i	Maximum Input Voltage - 3.0Gb/s internal SATA	—	750	mVdiff p-p		2
VIMIN-Gen2m	Minimum Input Voltage - 3.0 Gb/s eSATA	240	—	mVdiff p-p		2
VIMAX-Gen2m	Maximum Input Voltage - 3.0Gb/s eSATA	—	750	mVdiff p-p		2
VIMIN-Gen3i	Minimum Input Voltage - 6.0Gb/s internal SATA	240	—	mVdiff p-p		2
VIMAX-Gen3i	Maximum Input Voltage - 6.0Gb/s internal SATA	—	1000	mVdiff p-p		2



Table 6-6. Differential Signal DC Characteristics (Sheet 2 of 3)

Symbol	Parameter	Minimum	Maximum	Unit	Conditions	Notes
VOMIN-Gen1i,m	Minimum Output Voltage 1.5Gb/s internal and eSATA	400	—	mVdiff p-p		3
VOMAX-Gen1i,m	Maximum Output Voltage 1.5Gb/s internal and eSATA	—	600	mVdiff p-p		3
VOMIN-Gen2i,m	Minimum Output Voltage 3.0Gb/s internal and eSATA	400	—	mVdiff p-p		3
VOMAX-Gen2i,m	Maximum Output Voltage 3.0Gb/s internal and eSATA	—	700	mVdiff p-p		3
VOMIN-Gen3i	Minimum Output Voltage 6.0Gb/s internal SATA	200	—	mVdiff p-p		3
VOMAX-Gen3i	Maximum Output Voltage 6.0Gb/s internal SATA	—	900	mVdiff p-p		3
Associated Signals: USB2n[9:0], USB2p[9:0]						10
VDI	Differential Input Sensitivity	0.2	—	V		4, 6
VCM	Differential Common Mode Range	0.8	2.5	V		5, 6
VSE	Single-Ended Receiver Threshold	0.8	2	V		6
VCRS	Output Signal Crossover Voltage	1.3	2	V		6
VOL	Output Low Voltage	—	0.4	V	$I_{OL}=5mA$	6
VOH	Output High Voltage	3.3 V – 0.5	—	V	$I_{OH}=-2mA$	6
VHSSQ	HS Squelch Detection Threshold	100	150	mV		7
VHSDSC	HS Disconnect Detection Threshold	525	625	mV		7
VHSCM	HS Data Signaling Common Mode Voltage Range	-50	500	mV		7
VHSOI	HS Idle Level	-10	10	mV		7
VHSOH	HS Data Signaling High	360	440	mV		7
VHSOL	HS Data Signaling Low	-10	10	mV		7
VCHIRPJ	Chirp J Level	700	1100	mV		7
VCHIRPK	Chirp K Level	-900	-500	mV		7
Associated Signals: <b>USB3Rn[4:3]/PERn[2:1]</b> , <b>USB3Rp[4:3]/PERp[2:1]</b> , <b>USB3Tn[4:3]/PETn[2:1]</b> , <b>USB3Tp[4:3]/PETp[2:1]</b> , <b>USB3Rn[2:1]</b> , <b>USB3Rp[2:1]</b> , <b>USB3Tn[2:1]</b> , <b>USB3Tp[2:1]</b>						
VTX-DIFF-PP	Differential Peak to Peak Output Voltage	0.8	1.2	V		
VTX-DIFF P-P - Low	Low power differential Peak to Peak Output Voltage	0.4	1.2	V		8
VTX_CM-Acp-p	TX AC Common Mode Output Voltage (5GT/s)	—	100	mV		
ZTX-DIFF-DC	DC Differential TX Impedance	80	120	$\Omega$		
VRX-DIFF p-p	Differential Input Peak to Peak Voltage	0.1	1.2	V		
VRX_CM-ACp	AC peak Common Mode Input Voltage	—	150	mV		

**Table 6-6. Differential Signal DC Characteristics (Sheet 3 of 3)**

Symbol		Parameter	Minimum	Maximum	Unit	Conditions	Notes
Associated Signals: RTCX1							11
Input	V <sub>IH</sub>	Input High Voltage	0.8	1.2	V		
	V <sub>IL</sub>	Input Low Voltage	-0.25	0.1	V		

**NOTES:**

- PCI Express mVdiff p-p =  $2*|PETp[x] - PETn[x]|$ ; PCI Express mVdiff p-p =  $2*|PERp[x] - PERn[x]|$
- SATA Vdiff, RX ( $V_{IMAX}/V_{IMIN}$ ) is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p =  $2*|SATA[x]RXP - SATA[x]RXN|$ .
- SATA Vdiff, tx ( $V_{OMIN}/V_{OMAX}$ ) is measured at the SATA connector on the transmit side (generally, the motherboard connector), where SATA mVdiff p-p =  $2*|SATA[x]TXP - SATA[x]TXN|$
- $V_{DI} = |USBPx[P] - USBPx[N]|$
- Includes VDI range
- Applies to Low-Speed/Full-Speed USB
- Applies to High-Speed USB 2.0.
- USB 3.0 mVdiff p-p =  $2*|USB3Rp[x] - USB3Rn[x]|$ ; USB 3.0 mVdiff p-p =  $2*|USB3Tp[x] - USB3Tn[x]|$
- Maximum PCIe\* DC voltage is 3.6V, as specified in PCIe spec and maximum spike should not exceed 5.4V as specified in the JEDEC\* specification JESD78.
- 10-USB 2.0 ports are not available on all SKUs. Refer to [Table 2-3](#) and [Table 2-5](#) for available SKUs.

**Table 6-7. Other DC Characteristics**

Symbol	Parameter	Min.	Nom.	Max.	Unit	Notes
VCC1_05	Internal Logic and Core Well I/O Voltage	0.998	1.05	1.10	V	1
VCCCLK	1.05V Supply for clock buffers	0.998	1.05	1.10	V	1
VCCHSIO	1.05V Supply for HSIO core well logic	0.998	1.05	1.10	V	1
VCCAPLL	Analog Power Supply for USB 2.0 and Audio PLL	0.998	1.05	1.10	V	1
VCCACLKPLL	Analog Power Supply for internal clock PLL	0.998	1.05	1.10	V	1
VCCUSB3PLL	Analog Power Supply for USB 3.0 and PCIe* PLL	0.998	1.05	1.10	V	1
VCCSATA3PLL	Analog Power Supply for SATA3 PLL	0.998	1.05	1.10	V	1
VCCTS1_5	1.5V Supply for Thermal Sensor and Diodes	1.43	1.5	1.58	V	1
VCCSDIO (1.8V Mode)	1.8V supply for SDIO	1.71	1.8	1.89	V	1
VCCSDIO (3.3V Mode)	3.3V supply for SDIO	3.14	3.3	3.47	V	1
VCC3_3	I/O Buffer Voltage	3.14	3.3	3.47	V	1
VCCASW	1.05V Supply for Intel® Management Engine and Integrated LAN	0.998	1.05	1.10	V	1
VCCHDA	High Definition Audio or I <sup>2</sup> S I/O Buffer Voltage	3.14	3.3	3.47	V	1
VCCHDA (I <sup>2</sup> S low voltage)	I <sup>2</sup> S Low Voltage Mode I/O Buffer Voltage	1.71	1.8	1.89	V	1
VCCHDA (HDA low voltage)	High Definition Audio Low Voltage Mode I/O Buffer Voltage	1.43	1.5	1.58	V	1
VCCSUS3_3	Suspend Well I/O Buffer Voltage	3.14	3.3	3.47	V	1
VCCSPI	3.3V Supply for SPI Controller Logic	3.14	3.3	3.47	V	1
VCCDSW3_3	3.3V supply for Deep Sx wells	3.14	3.3	3.47	V	1
VCCRTC (G3-S0)	Battery Voltage	2.0	3.3	3.47	V	1, 2

**NOTES:**

- The I/O buffer supply voltage is measured at the PCH package pins. The tolerances shown in [Table 6-7](#) are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a roll off of 3db/decade above 20 MHz.
- Maximum Crystal ESR is 50 kOhms.

## 6.4 AC Characteristics

Table 6-8. PCI Express\* Interface Timings

Symbol	Parameter	Min.	Max.	Unit	Figures	Notes
<b>Transmitter and Receiver Timings</b>						
UI (Gen1)	Unit Interval – PCI Express*	399.88	400.12	ps		5
UI (Gen 2)	Unit Interval – PCI Express*	199.9	200.1	ps		5
$T_{TX-EYE}$ (Gen 1/ Gen 2)	Minimum Transmission Eye Width	0.7	—	UI	6-28	1,2
$T_{TX-RISE/Fall}$ (Gen 1)	D+/D- TX Out put Rise/Fall time	0.125	—	UI		1,2
$T_{TX-RISE/Fall}$ (Gen 2)	D+/D- TX Out put Rise/Fall time	0.15	—	UI		1,2
$T_{RX-EYE}$ (Gen 1/ Gen 2)	Minimum Receiver Eye Width	0.40	—	UI	6-29	3,4
$T_{Min-Pulse}$ (Gen 2)	Instantaneous lone Pulse Width	0.9	—	UI		

**NOTES:**

1. Specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive TX UIs. (also refer to the Transmitter compliance eye diagram)
2. A  $T_{TX-EYE} = 0.70$  UI provides for a total sum of deterministic and random jitter budget of  $T_{TXJITTER-MAX} = 0.30$  UI for the Transmitter collected over any 250 consecutive TX UIs. The  $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$  specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load documented in the PCI Express\* specification 2.0 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
4. A  $T_{RX-EYE} = 0.40$  UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The  $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$  specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total 0.6 UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
5. Nominal Unit Interval is 400 ps for 2.5 GT/s and 200 ps for 5 GT/s.

**Table 6-9. DisplayPort\* Aux Interface**

Signal Group: DDPB\_AUXP, DDPB\_AUXN, DDPC\_AUXP, DDPC\_AUXN

Symbol	Parameter	Min.	Nom.	Max.	Unit
UI	AUX unit interval	0.4	0.5	0.6	μs
T-Aux_bus_park	AUX CH bus park time	10	—	—	ns
Tcycle-to-cycle jitter	Maximum allowable UI variation within a single transaction at the connector pins of a transmitting device	—	—	0.04	UI
Tcycle-to-cycle jitter	Maximum allowable UI variation within a single transaction at the connector pins of a receiving device	—	—	0.05	UI

**Table 6-10. DDC Characteristics**

Signal Group: eDP\_VDD\_EN, eDP\_BKL滕, eDP\_BKLCTL, DDP[C:B]\_CTRLCLK, DDP[C:B]\_CTRLDATA

Symbol	Parameter	Standard Mode	Fast Mode		1 MHz		Units
		Max.	Min.	Max.	Min.	Max.	
$F_{SCL}$	Operating Frequency	100	0	400	0	1000	KHz
$T_r$	Rise Time <sup>1</sup>	1000	$20+0.1C_b^2$	300	—	120	ns
$T_f$	Fall Time <sup>1</sup>	300	$20+0.1C_b^2$	300	—	120	ns

**NOTES:**

1. Measurement Point for Rise and Fall time:  $V_{IL}(\max)-V_{IH}(\min)$
2.  $C_b$  = total capacitance of one bus line in pF. If mixed with High-speed mode devices, faster fall times according to High-Speed mode  $T_r/T_f$  are allowed.

**Table 6-11. DisplayPort\* Hot-Plug Detect Interface**

Signal Group: DDPB\_HPD, DDPC\_HPD, eDP\_HPD

Symbol	Parameter	Min.	Max.	Unit	Figures	Notes
$T_{ir}$	Input Time Rise	50	500	ps		
$T_{if}$	Input Time Fall	50	500	ps		
$T_{idr}$	Input Delay Rise	0.3	2.5	ns		
$T_{idf}$	Input Delay Fall	0.3	2.5	ns		

**Table 6-12. Clock Timings (Sheet 1 of 3)**

Sym	Parameter	Min.	Max.	Unit	Notes	Figure
<b>LPC Clock (CLKOUT_LPC[1:0])</b>						
t1	Period	41.16	42.18	ns		6-11
t2	High Time	16.67	25.00	ns		6-11
t3	Low Time	16.67	25.00	ns		6-11
	Duty Cycle	40	60	%		
t4	Rising Edge Rate	0.6	4.0	V/ns	18.	6-11
t5	Falling Edge Rate	0.6	4.0	V/ns	18.	6-11
	Jitter	—	500	ps	8,9	
	Flight Time (PCH to Device)		3	ns		



Table 6-12. Clock Timings (Sheet 2 of 3)

Sym	Parameter	Min.	Max.	Unit	Notes	Figure
<b>CLKOUT_PCIE[5:0]_[P,N], CLKOUT_ITPXD_P[N]</b>						
Period	Period SSC On	9.849	10.201	ns		6-30
Period	Period SSC Off	9.849	10.151	ns		6-30
DtyCyc	Duty Cycle	40	60	%		6-30
V_Swing	Differential Output Swing	300	—	mV		6-30
Slew_rise	Rising Edge Rate	1.5	4	V/ns		6-30
Slew_fall	Falling Edge Rate	1.5	4	V/ns		6-30
	Jitter	—	150	ps	8,9,10	
SSC	Spread Spectrum	0	0.5	%	13,14	
<b>SMBus/SMLink Clock (SMBCLK, SML[1:0]CLK)</b>						
f <sub>smb</sub>	Operating Frequency	10	100	KHz		
t <sub>18</sub>	High Time	4.0	50	μs	2	6-20
t <sub>19</sub>	Low Time	4.7	—	μs		6-20
t <sub>20</sub>	Rise Time	—	1000	ns		6-20
t <sub>21</sub>	Fall Time	—	300	ns		6-20
<b>SMLink0 (SML0CLK) (See Note 15)</b>						
f <sub>smb</sub>	Operating Frequency	0	400	KHz		
t <sub>18_SMLFM</sub>	High Time	0.6	50	μs	2	6-20
t <sub>19_SMLFM</sub>	Low Time	1.3	—	μs		6-20
t <sub>20_SMLFM</sub>	Rise Time	—	300	ns		6-20
t <sub>21_SMLFM</sub>	Fall Time	—	300	ns		6-20
<b>SMLink0 (SML0CLK) (See Note 17)</b>						
f <sub>smb</sub>	Operating Frequency	0	1000	KHz		
t <sub>18_SMLFMP</sub>	High Time	0.26	—	μs	2	6-20
t <sub>19_SMLFMP</sub>	Low Time	0.5	—	μs		6-20
t <sub>20_SMLFMP</sub>	Rise Time	—	120	ns		6-20
t <sub>21_SMLFMP</sub>	Fall Time	—	120	ns		6-20
<b>HDA_BCLK (Intel® High Definition Audio)</b>						
f <sub>HDA</sub>	Operating Frequency	24.0	—	MHz		
	Frequency Tolerance	—	100	ppm		
t <sub>26a</sub>	Input Jitter (refer to Clock Chip Specification)	—	300	ppm		
t <sub>27a</sub>	High Time (Measured at 0.75 Vcc)	18.75	22.91	ns		6-11
t <sub>28a</sub>	Low Time (Measured at 0.35 Vcc)	18.75	22.91	ns		6-11
<b>Suspend Clock (SUSCLK)</b>						
f <sub>susclk</sub>	Operating Frequency	32	—	KHz	4	
t <sub>39</sub>	High Time	9.5	—	μs	4	
t <sub>39a</sub>	Low Time	9.5	—	μs	4	
<b>XTAL24_IN/XTAL24_OUT</b>						
ppm <sup>12</sup>	Crystal Tolerance cut accuracy maximum	—	35 ppm(@ 25 °C ±3 °C)			
ppm <sup>12</sup>	Temp Stability Maximum	—	30 ppm(10 – 70 °C)			
ppm <sup>12</sup>	Aging Maximum	—	5 ppm			

**Table 6-12. Clock Timings (Sheet 3 of 3)**

Sym	Parameter	Min.	Max.	Unit	Notes	Figure
<b>SPI_CLK</b>						
Slew_Rise	Output Rise Slew Rate (0.2Vcc - 0.6Vcc)	1	4	V/ns	11	6-31
Slew_Fall	Output Fall Slew Rate (0.6Vcc - 0.2Vcc)	1	4	V/ns	11	6-31

**NOTES:**

1. The CLK48 expects a 40/60% duty cycle.
2. The maximum high time (t18 Max) provide a simple ensured method for devices to detect bus idle conditions.
3. BCLK Rise and Fall times are measured from 10% VDD and 90% VDD.
4. SUSCLK duty cycle can range from 30% minimum to 70% maximum.
5. Edge rates in a system as measured from 0.8 – 2.0V.
6. The active frequency can be 5 MHz, 50 MHz, or 62.5 MHz depending on the interface speed. Dynamic changes of the normal operating frequency are not allowed.
7. Testing condition: 1 kΩ pull-up to Vcc, 1 kΩ pull-down and 10 pF pull-down and 1/2 inch trace (see [Figure 6-31](#) for more detail).
8. Jitter is specified as cycle-to-cycle as measured between two rising edges of the clock being characterized. Period minimum and maximum includes cycle-to-cycle jitter and is also measured between two rising edges of the clock being characterized.
9. On all jitter measurements care should be taken to set the zero crossing voltage (for rising edge) of the clock to be the point where the edge rate is the fastest. Using a Math function = Average(Derivative(Ch1)) and set the averages to 64, place the cursors where the slope is the highest on the rising edge—usually this lower half of the rising edge. The reason this is defined is for users trying to measure in a system it is impossible to get the probe exactly at the end of the Transmission line with large Flip-Chip components. This results in a reflection induced ledge in the middle of the rising edge and will significantly increase measured jitter.
10. Phase jitter requirement: The designated Gen 2 outputs will meet the reference clock jitter requirements from the *PCI Express Gen 2 Base Specification*. The test is to be performed on a component test board under quiet conditions with all clock outputs on. Jitter analysis is performed using a standardized tool provided by the PCI SIG. Measurement methodology is defined in the Intel document "*PCI Express Reference Clock Jitter Measurements*". This is not for CLKOUT\_PCIE[7:0].
11. Testing condition: 1 kΩ pull-up to Vcc, 1 kΩ pull-down and 10 pF pull-down and 1/2 inch trace (see [Figure 6-31](#) for more detail).
12. Total of crystal cut accuracy, frequency variations due to temperature, parasitics, load capacitance variations, and aging is recommended to be less than 90 ppm.
13. Spread Spectrum (SSC) is referenced to rising edge of the clock.
14. Spread Spectrum (SSC) of 0.25% on CLKOUT\_PCIE[7:0] and CLKOUT\_PEG\_[B:A] is used for WiMAX friendly clocking purposes.
15. When SMLink0 is configured to run in Fast Mode (FM) using soft strap, the supported operating range is 0 kHz ~ 400 kHz, but the typical operating frequency is in the range of 300 kHz – 400 kHz.
16. The 25 MHz output option for CLKOUTFLEX2 is derived from the 25 MHz crystal input to the PCH. The PPM of the 25 MHz output is equivalent to that of the crystal.
17. When SMLink0 is configured to run in Fast Mode Plus (FMP) using a soft strap, the supported operating range is 0 Hz ~ 1 MHz, but the typical operating frequency is in the range of 900 kHz – 1000 KHz. This is the default mode for this interface.
18. Test load: 10 pF to ground. Measured at 0.2 \* Vcc - 0.8 \* Vcc.

**Note:**

Refer to Note 3 of Table 4-4 in Section 4.2.2.2 and Note 2 of Table 4-6 in Section 4.2.3.2 of the PCI Local Bus Specification, Revision 2.3 for measurement details.

Table 6-13. Universal Serial Bus (Gen 2) Timing

Sym	Parameter	Min.	Max.	Units	Notes	Figure
<b>Full-speed Source (Note 7)</b>						
t100	USBPx+, USBPx- Driver Rise Time	4	20	ns	1,6 $C_L = 50 \text{ pF}$	6-17
t101	USBPx+, USBPx- Driver Fall Time	4	20	ns	1,6 $C_L = 50 \text{ pF}$	6-17
t102	Source Differential Driver Jitter - To Next Transition - For Paired Transitions	-3.5 -4	3.5 4	ns ns	2, 3	6-18
t103	Source SE0 interval of EOP	160	175	ns	4	6-19
t104	Source Jitter for Differential Transition to SE0 Transition	-2	5	ns	5	
t105	Receiver Data Jitter Tolerance - To Next Transition - For Paired Transitions	-18.5 -9	18.5 9	ns ns	3	6-18
t106	EOP Width: Must accept as EOP	82	—	ns	4	6-19
t107	Width of SE0 interval during differential transition	—	14	ns		
<b>Low-speed Source (Note 8)</b>						
t108	USBPx+, USBPx – Driver Rise Time	75	300	ns	$1,6 \text{ } C_L = 200 \text{ pF}$ $C_L = 600 \text{ pF}$	6-17
t109	USBPx+, USBPx – Driver Fall Time	75	300	ns	$1,6 \text{ } C_L = 200 \text{ pF}$ $C_L = 600 \text{ pF}$	6-17
t110	Source Differential Driver Jitter To Next Transition For Paired Transitions	-25 -14	25 14	ns ns	2,3	6-18
t111	Source SE0 interval of EOP	1.25	1.50	μs	4	6-19
t112	Source Jitter for Differential Transition to SE0 Transition	-40	100	ns	5	
t113	Receiver Data Jitter Tolerance - To Next Transition - For Paired Transitions	-152 -200	152 200	ns ns	3	6-18
t114	EOP Width: Must accept as EOP	670	—	ns	4	6-19
t115	Width of SE0 interval during differential transition	—	210	ns		

**NOTES:**

- Driver output resistance under steady state drive is specified at  $28 \Omega$  at minimum and  $43 \Omega$  at maximum.
- Timing difference between the differential data signals.
- Measured at crossover point of differential data signals.
- Measured at 50% swing point of data signals.
- Measured from last crossover point to 50% swing point of data line at leading edge of EOP.
- Measured from 10% to 90% of the data signal.
- Full-speed Data Rate has minimum of 11.97Mb/s and maximum of 12.03Mb/s.
- Low-speed Data Rate has a minimum of 1.48Mb/s and a maximum of 1.52Mb/s.

**Table 6-14. SATA Interface Timings**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
UI	Gen I Operating Data Period	666.43	670.23	ps		
UI-2	Gen II Operating Data Period (3Gb/s)	333.21	335.11	ps		
UI-3	Gen III Operating Data Period (6Gb/s)	166.6083	166.6667	ps		
t120gen1	Rise Time	0.15	0.41	UI	1	
t120gen2	Rise Time	0.2	0.41	UI	1	
t120gen3	Rise Time	0.2	0.48	UI	1	
t121gen1	Fall Time	0.15	0.41	UI	2	
t121gen2	Fall Time	0.2	0.41	UI	2	
t121gen3	Fall Time	0.2	0.48	UI	2	
t122	TX differential skew	—	20	ps		
t123	COMRESET	304	336	ns	3	
t124	COMWAKE transmit spacing	101.3	112	ns	3	
t125	OOB Operating Data period	646.67	686.67	ns	4	

**NOTES:**

1. 20–80% at transmitter
2. 80–20% at transmitter
3. As measured from 100mV differential crosspoints of last and first edges of burst.
4. Operating data period during Out-Of-Band burst transmissions.

Table 6-15. SMBus and SMLink Timing

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t130	Bus Free Time Between Stop and Start Condition	4.7	—	μs		6-20
t130SMLFM	Bus Free Time Between Stop and Start Condition	1.3	—	μs	5	6-20
t130SMLFMP	Bus Free Time Between Stop and Start Condition	0.5	—	μs	5	6-20
t131	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	4.0	—	μs		6-20
t131SMLFM	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	0.6	—	μs	5	6-20
t131SMLFMP	Hold Time after (repeated) Start Condition. After this period, the first clock is generated.	0.26	—	μs	5	6-20
t132	Repeated Start Condition Setup Time	4.7	—	μs		6-20
t132SMLFM	Repeated Start Condition Setup Time	0.6	—	μs	5	6-20
t132SMLFMP	Repeated Start Condition Setup Time	0.26	—	μs	5	6-20
t133	Stop Condition Setup Time	4.0	—	μs		6-20
t133SMLFM	Stop Condition Setup Time	0.6	—	μs	5	6-20
t133SMLFMP	Stop Condition Setup Time	0.26	—	μs	5	6-20
t134	Data Hold Time	300	—	ns	4	6-20
t134SMLFM	Data Hold Time	0	—	ns	4, 5	6-20
t134SMLFMP	Data Hold Time	0	—	ns	4, 5	6-20
t135	Data Setup Time	250	—	ns		6-20
t135SMLFM	Data Setup Time	100	—	ns	5	6-20
t135SMLFMP	Data Setup Time	50	—	ns	5	6-20
t136	Device Time Out	25	35	ms	1	
t137	Cumulative Clock Low Extend Time (slave device)	—	25	ms	2	6-21
t138	Cumulative Clock Low Extend Time (master device)	—	10	ms	3	6-21
T <sub>por</sub>	Time in which a device must be operational after power-on reset	—	500	ms		

**NOTES:**

1. A device will timeout when any clock low exceeds this value.
2. t137 is the cumulative time a slave device is allowed to extend the clock cycles in one message from the initial start to stop. If a slave device exceeds this time, it is expected to release both its clock and data lines and reset itself.
3. t138 is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from start-to-ack, ack-to-ack, or ack-to-stop.
4. t134 has a minimum timing for I<sup>2</sup>C of 0 ns, while the minimum timing for SMBus/SMLINK is 300 ns.
5. Timings with the SMLFM designator apply only to SMLink0 and only when SMLink0 is operating in Fast Mode.

**Table 6-16. Intel® High Definition Audio (Intel® HD Audio) Timing**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t143	Time duration for which HDA_SDO is valid before HDA_BCLK edge.	7	—	ns		6-23
t144	Time duration for which HDA_SDO is valid after HDA_BCLK edge.	7	—	ns		6-23
t145	Setup time for HDA_SDI[1:0] at rising edge of HDA_BCLK	15	—	ns		6-23
t146	Hold time for HDA_SDI[1:0] at rising edge of HDA_BCLK	0	—	ns		6-23

**Table 6-17. LPC Timing**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t150	LAD[3:0] Valid Delay from CLKOUT_LPC[1:0] Rising	3	24.67	ns		6-12
t151	LAD[3:0] Output Enable Delay from CLKOUT_LPC[1:0] Rising	2	—	ns		6-16
t152	LAD[3:0] Float Delay from CLKOUT_LPC[1:0] Rising	—	28	ns		6-14
t153	LAD[3:0] Setup Time to CLKOUT_LPC[1:0] Rising	17.67	—	ns		6-13
t154	LAD[3:0] Hold Time from CLKOUT_LPC[1:0] Rising	2	—	ns		6-13
t157	LFRAME# Valid Delay from CLKOUT_LPC[1:0] Rising	3	24.67	ns		6-12

**Table 6-18. Miscellaneous Timings**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t160	SERIRQ Setup Time to PCICLK Rising	7	—	ns		6-13
t161	SERIRQ Hold Time from PCICLK Rising	0	—	ns		6-13
t162	GPIO, USB Resume Pulse Width	2	—	RTCCLK		6-15
t163	SPKR Valid Delay from OSC Rising	—	200	ns		6-12
t164	SERR# Active to NMI Active	—	200	ns		
t165	<b>(Intel® Core™ M processor)</b> VCCPCIEPHY, VCCSATAPHY, VCCUSB3PHY ramp rate <b>(U-Processor Line)</b> VCCHSIO ramp rate		0.7	V/μs		
t166	VCCUSB3PLL, VCCSATA3PLL, SATA_IREF, SATA_RCOMP, PCIE_IREF, PCIE_RCOMP ramp rate	—	0.1	V/μs		

**Table 6-19. SPI Timings (20 MHz)**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t180a	Serial Clock Frequency - 20 MHz operation	17.2	18.4	MHz	1	
t183a	Tco of SPI_MOSI and SPI_IO[3:2] with respect to serial clock falling edge at the host	-5	13	ns		6-22
t184a	Setup of SPI_MISO and SPI_IO[3:2] with respect to serial clock falling edge at the host	16	—	ns		6-22
t185a	Hold of SPI_MISO and SPI_IO[3:2] with respect to serial clock falling edge at the host	0	—	ns		6-22
t186a	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising at the host	30	—	ns		6-22
t187a	Hold of SPI_CS[1:0]# de-assertion with respect to serial clock falling at the host	30	—	ns		6-22
t188a	SPI_CLK high time	26.37	—	ns		6-22
t189a	SPI_CLK low time	26.82	—	ns		6-22

**NOTES:**

1. The typical clock frequency driven by the PCH is 17.86 MHz.
2. Measurement point for low time and high time is taken at 0.5(VccSPI).

**Table 6-20. SPI Timings (33 MHz)**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t180b	Serial Clock Frequency - 33 MHz operation	29.83	33.81	MHz	1	
t183b	Tco of SPI_MOSI and SPI_IO[3:2] with respect to serial clock falling edge at the host	-5	5	ns		6-22
t184b	Setup of SPI_MISO and SPI_IO[3:2] with respect to serial clock falling edge at the host	8	—	ns		6-22
t185b	Hold of SPI_MISO and SPI_IO[3:2] with respect to serial clock falling edge at the host	0	—	ns		6-22
t186b	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising at the host	30	—	ns		6-22
t187b	Hold of SPI_CS[1:0]# de-assertion with respect to serial clock falling at the host	30	—	ns		6-22
t188b	SPI_CLK High time	14.88	—	ns		6-22
t189b	SPI_CLK Low time	15.18	—	ns		6-22

**NOTES:**

1. The typical clock frequency driven by the PCH is 33 MHz.
2. Measurement point for low time and high time is taken at 0.5(VccSPI).

**Table 6-21. SPI Timings (50 MHz) (Sheet 1 of 2)**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t180c	Serial Clock Frequency - 50 MHz operation	46.99	53.40	MHz	1	
t183c	Tco of SPI_MOSI and SPI_IO[3:2] with respect to serial clock falling edge at the host	-3	3	ns		6-22
t184c	Setup of SPI_MISO and SPI_IO[3:2] with respect to serial clock falling edge at the host	8	—	ns		6-22
t185c	Hold of SPI_MISO and SPI_IO[3:2] with respect to serial clock falling edge at the host	0	—	ns		6-22
t186c	Setup of SPI_CS[1:0]# assertion with respect to serial clock rising edge at the host	30	—	ns		6-22

**Table 6-21. SPI Timings (50 MHz) (Sheet 2 of 2)**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t187c	Hold of SPI_CS[1:0]# assertion with respect to serial clock falling edge at the host	30	—	ns		6-22
t188c	SPI_CLK High time	7.1	—	ns	2, 3	6-22
t189c	SPI_CLK Low time	11.17	—	ns	2, 3	6-22

**NOTES:**

1. Typical clock frequency driven by the PCH is 50 MHz.
2. When using 50 MHz mode ensure target flash component can meet t188c and t189c specifications. Measurement should be taken at a point as close as possible to the package pin.
3. Measurement point for low time and high time is taken at 0.5(VccSPI).

**Table 6-22. Controller Link Receive Timings**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t190	Single bit time	13	—	ns		6-32
t191	Single clock period	30	—	ns		6-32
t192	Rise time/Fall time	0.11	3.5	V/ns	1	6-33
t193	Setup time before CL_CLK1	0.9	—	ns		6-32
t194	Hold time after CL_CLK1	0.9	—	ns		6-32
V <sub>IL_AC</sub>	Input low voltage (AC)	—	CL_Vref - 0.08	V	2	
V <sub>IH_AC</sub>	Input high voltage (AC)	CL_Vref + 0.08	—	V	2	

**NOTES:**

1. Measured from (CL\_Vref - 50mV to CL\_Vref + 50mV) at the receiving device side. No test load is required for this measurement as the receiving device fulfills this purpose.
2. CL\_Vref = 0.12\*(VccSus3\_3).

**Table 6-23. USB 3.0 Interface Transmit and Receiver Timings**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
UI	Unit Interval – USB 3.0 (5.0 GT/s)	199.9	200.1	ps		
T <sub>TX-EYE</sub>	Minimum Transmission Eye Width	0.625	—	UI		
P <sub>U3</sub>	Polling Period U3 State	-	100	mS		
P <sub>RX-Detect</sub>	Polling Period Rx Detect	-	100	mS		

**Table 6-24. SDIO Timings (Sheet 1 of 2)**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
<b>VCCSDIO = 1.8V</b>						
F	Operating Frequency	-	50	MHz		
T <sub>RISE</sub>	Output Rise Time (20 – 80%)	0.907	1.531	ns		
T <sub>FALL</sub>	Output Fall Time (80 – 20%)	0.868	1.425	ns		
Slew_Rise	Rise Slope	0.639	1.29	V/ns		
Slew_Fall	Fall Slope	0.686	1.349	V/ns		
<b>VCCSDIO = 3.3V</b>						
F	Operating Frequency	0.014	25	MHz		
T <sub>RISE</sub>	Output Rise Time (20 – 80%)	0.877	1.273	ns		



Table 6-24. SDIO Timings (Sheet 2 of 2)

Sym	Parameter	Min.	Max.	Units	Notes	Figure
$T_{FALL}$	Output Fall Time (80 – 20%)	0.827	1.191	ns		
Slew_Rise	Rise Slope	1.452	2.388	V/ns		
Slew_Fall	Fall Slope	1.552	2.531	V/ns		

Table 6-25. GSPI Timings

Sym	Parameter	Min.	Max.	Units	Notes	Figure
$F$	Operating Frequency	—	25	MHz		
$T_{RISE}$	Output Rise Time (20–80%)	0.877	1.273	ns		
$T_{FALL}$	Output Fall Time (80–20%)	0.827	1.191	ns		
Slew_Rise	Output Rise Slope	1.452	2.388	V/ns		
Slew_Fall	Output Fall Slope	1.552	2.531	V/ns		

Table 6-26. UART Timings

Sym	Parameter	Min.	Max.	Units	Notes	Figure
$F$	Operating Frequency	-	4	MHz		
$T_{RISE}$	Output Rise Time (20 – 80%)	0.877	1.273	ns		
$T_{FALL}$	Output Fall Time (80 – 20%)	0.827	1.191	ns		
Slew_Rise	Output Rise Slope	1.452	2.388	V/ns		
Slew_Fall	Output Fall Slope	1.552	2.531	V/ns		

Table 6-27. Windows\* InstantGo Power Save Mode (Windows\* InstantGo PSM) Timings

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes	Figure
$V_{1.05A\text{ACTIVE}}$	Voltage of $V_{1.05A}$ <sup>1</sup> in S0	0.998	1.05	1.102	V		6-34
$V_{1.05A\text{PSM}}$	Voltage of $V_{1.05A}$ <sup>2</sup> in Windows* InstantGo PSM <sup>3</sup>	0.902	0.95	0.997	V		6-34
$T_{\text{PSM\_EXIT}}$	Windows InstantGo PSM Exit Time	-	-	50	us		6-34
$V_{1.05A\text{PSM\_RAMPUP\_RATE}}$	$V_{1.05A\text{PSM}}$ Ramp Up Rate to $V_{1.05A\text{ACTIVE}}$ on a Windows InstantGo PSM exit	5		100	mV/us		6-34

## NOTES:

1.  $V_{1.05A}$  must ramp directly to  $V_{1.05A\text{ACTIVE}}$  on G3 exit or Deep Sx exit.
2.  $V_{1.05A}$  includes all 1.05A rails supplied to the processor. This includes VCCST, VCC1\_05, VCC1\_05\_PHY, VCC1\_05\_USB2, VCCCLK1 to VCCCLK7, VCCAPLL, VCCACLKPLL, VCCHDAPLL, VCCUSB2PLL, VCCOPIPLL, VCCASW and DCPSUS1 to DCPSUS4 (DCPSUS applies to External Suspend VR mode only).
3. In Windows\* InstantGo Power Save Mode (InstantGo PSM) SLP\_S0# will be asserted and VCCHSIO, VCCSATAPHY, VCCUSB3PHY, VCCUSB3PLL and VCCSATAPLL are expected to be at 0V.
4. This feature is only supported on platforms that are configured for External Suspend VR Mode. This means that INTVRMEN strap is pulled down and DCPSUS1, DCPSUS2, DCPSUS3 and DCPSUS4 are powered from an external power source.

## 6.5 Power Sequencing and Reset Signal Timings

**Table 6-28. Power Sequencing and Reset Signal Timings (Sheet 1 of 2)**

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t200	VccRTC active to RTCRST# de-assertion	9	—	ms	26	6-1 6-2
t200a	RTCRST# de-assertion to DPWROK high	1	—	us		6-1 6-2
t200b	VccDSW3_3 active to DPWROK high	10	—	ms		6-1 6-2
t200c	VccDSW3_3 active to VccSus3_3 active	0	—	ms		6-1 6-2
t201	VccSUS active to RSMRST# de-assertion	10	—	ms	1	6-1 6-2
t202	DPWROK high to SLP_SUS# de-assertion	95	—	ms	2, 3, 32	6-1 6-2
t202a	RSMRST# and SLP_SUS# de-assertion to SUSCLK toggling	5	—	ms	3, 4	6-1 6-2
t203	SLP_S5# high to SLP_S4# high	30	—	μs	5, 29	6-3
t204	SLP_S4# high to SLP_S3# high	30	—	μs	6	6-3
t205a	Vcc active to PCH_PWROK high	5	—	ms	7, 13	
t205b	PCH_PWROK high to PLTRST# de-assertion	99	—	ms	24	
t206	PCH_PWROK deglitch time	1	—	ms	8	
t207	VccASW active to APWROK high	1	—	ms		
t208	PCH_PWROK high to PCH clock outputs stable	1	—	ms	9	
t209	PCH clock output stable to PROCPWRGD high	1	—	ms		
t210	PROCPWRGD and SYS_PWROK high to SUS_STAT# de-assertion	1	—	ms		
t211	SUS_STAT# de-assertion to PLTRST# de-assertion	60	—	μs		
t212	APWROK high to SPI soft strap Reads	500	—	μs	22	
t213	APWROK high to CL_RST# de-asserted	500	—	μs	10	
t214	DMI message and all PCI Express ports and DMI in L2/L3 state to SUS_STAT# active	60	—	μs		6-6
t215	SUS_STAT# active to PLTRST# active	210	—	μs		6-6
t217	PLTRST# active to PROCPWRGD inactive	30	—	μs		6-6
t218	PROCPWRGD inactive to clocks invalid	10	—	μs	33	6-6
t219	Clocks invalid to SLP_S3# assertion	2	—	μs		6-6
t220	SLP_S3# low to SLP_S4# low	30	—	μs		6-6
t221	SLP_S4# low to SLP_S5# low	30	—	μs		6-6
t222	SLP_S3# active to PCH_PWROK de-asserted	0	—			6-6
t225	VccRTC active to VccDSW3_3 active	0	—	ms	1, 12	6-2
t227	VccSus active to VccASW active	0	—	ms	1	
t229	VccASW active to Vcc active	0	—	ms		
t230	APWROK high to PCH_PWROK high	0	—	ms		

Table 6-28. Power Sequencing and Reset Signal Timings (Sheet 2 of 2)

Sym	Parameter	Min.	Max.	Units	Notes	Figure
t231	PCH_PWROK low to Vcc rail falling	40	—	ns	13, 15,16,2 7, 28	
t232	APWROK falling to VccASW rail falling	40	—	ns	15,16,2 7, 28	
t233	SLP_S3# assertion to Vcc rail falling	5	—	μs	13, 14	
t234	DPWROK falling to VccDSW3_3rail falling	40	—	ns	15,16,2 7, 28	
t235	RSMRST# assertion to VccSUS rail falling	40	—	ns	1, 15,16,2 7,28	6-7
t236	RTC RST# de-assertion to VccRTC rail falling	0	—	ms		6-7
t237	SLP_LAN# (or LANPHYPC) rising to Intel LAN Phy power high and stable	—	20	ms		
t238	DPWROK falling to any of VccDSW3_3, VccSUS, VccASW, or Vcc rail falling	70	—	ns	1, 13,15,1 6,27,28	
t241	VccSus supplies active to Vcc supplies active	0	—	ms	1, 13	
t242	HDA_RST# active low pulse width	1	—	μs		
t244	VccSus active to SLP_S5#, SLP_S4#, SLP_S3#, SUS_STAT#, PLTRST# and PCIRST# valid	—	50	ns	21	
t246	S4 Wake Event to SLP_S4# inactive (S4 Wake)	See Note Below			5	
t247	S3 Wake Event to SLP_S3# inactive (S3 Wake)	See Note Below			6	
t251	RSMRST# de-assertion to APWROK assertion	0	—	ms		
t252	THRMTRIP# active to SLP_S3#, SLP_S4#, SLP_S5# active	—	175	ns		
t253	RSMRST# rising edge transition from 20% to 80%	—	50	μs		
t254	RSMRST# falling edge transition	—	50	μs	18, 19	
t255	DPWROK rising edge transition from 20% to 80%	—	50	μs		
t256	DPWROK falling edge transition	—	50	μs	19, 20	
t257	Power-cycle duration for a global reset other than G3 or Deep Sx. Also the duration of a host reset with power-cycle.	4-5	—	sec	25	
t258	<b>(U-Processor Line)</b> HSIOPC assertion to VCCHS10, VCCUSB3PLL and VCCSATA3PLL active		65	μs	30, 31, 32,34	
t258a	<b>(Intel® Core™ M processor)</b> PCIEPHY_PC assertion to VCCPCIEPHY active		65	μs	30, 31, 32,34	
t258b	<b>(Intel® Core™ M processor)</b> SATAPHY_PC assertion to VCCSATAPHY and VCCSATA3PLL active		65	μs	30, 31, 32,34	
t258c	<b>(Intel® Core™ M processor)</b> USB3PHY_PC assertion to VCCUSB3PHY and VCCUSB3PLL active		65	μs	30, 31, 32,34	

**NOTES:**

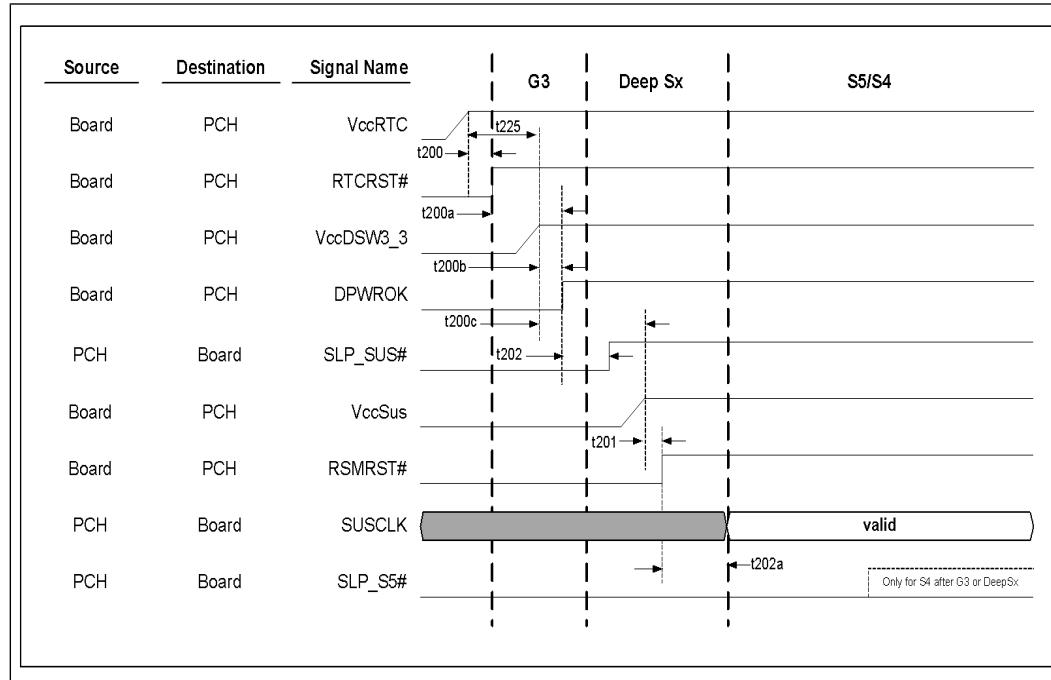
1. VccSus supplies include VCCSUS3\_3 and VccHDA (if VCCHDA is on suspend well). Also includes DcpSus for mobile platforms that power DcpSus externally.
2. This timing is a nominal value counted using RTC clock. If RTC clock isn't already stable at the rising edge of RSMRST#, this timing could be shorter or longer than the specified value.



3. Platforms not supporting Deep Sx will typically have SLP\_SUS# left as no connect. Hence DPWROK high and RSMRST# de-assertion to SUSCLK toggling would be  $t202+t202a=100$  ms minimum.
4. Platforms supporting Deep Sx will have SLP\_SUS# de-assert prior to RSMRST#. Platforms not supporting Deep Sx will have RSMRST# de-assert prior to SLP\_SUS#.
5. Dependency on SLP\_S4# and SLP\_A# stretching
6. Dependency on SLP\_S3# and SLP\_A# stretching
7. PCI/PCIe 2.0 specification requires that the power rails associated with PCI/PCIe (typically, the 3.3V, 5V, and 1V core well rails) have been valid for 100 ms prior to PLTRST# de-assertion. System designers must ensure the requirement is met on the platforms.
8. Ensure PCH\_PWROK is a solid logic '1' before proceeding with the boot sequence.  
Note: If PCH\_PWROK drops after t206, it will be considered a power failure.
9. Timing is dependant on whether 25 MHz crystal is stable by the time PCH\_PWROK is high.
10. Requires SPI messaging to be completed.
11. The negative minimum timing implies that DRAMPWROK must either fall before SLP\_S4# or within 100 ns after it.
12. The VccDSW3\_3 supplies must never be active while the VccRTC supply is inactive.
13. Vcc includes VCC1\_05, VCCCLK, VCCHSIO, VCCUSB3PLL, VCCSATA3PLL, VCCAPLL, VCCACLKPLL, VCCTS1\_5, VCCSDIO, VCC3\_3 and VCCASW (if Intel® ME only powered in S0).
14. A Power rail is considered to be inactive when the rail is at its nominal voltage minus 5% or less.
15. Board design may meet (t231 AND t232 AND t234 AND t235) OR (t238).
16. The definition of rail falling for this timing requirement is as follows:
  - 1) VCCDSW3\_3 and VCCSUS3\_3 is 2.9V;
  - 2) VCCASW and DCPSUS (in external suspend VR mode) is 0.92V;
  - 3) VCC is 0.99V.
17. If RTC clock is not already stable at RSMRST# rising edge, this time may be longer.
18. RSMRST# falling edge must transition to 0.8 V or less before VccSus3\_3 drops to 2.9V.
19. The 50  $\mu$ s should be measured from  $V_{IH}$  to  $V_{IL}$  (2 – 0.78V).
20. DPWROK falling edge must transition to 0.8V or less before VccDSW3\_3 drops to 2.9V
21. This is an internal timing showing when the signals (SLP\_S5#, SLP\_S4#, SLP\_S3#, SUS\_STAT#, PLTRST# and PCIRST#) are valid after VccSus rail is Active.
22. APWROK high to SPI soft strap Read is an internal PCH timing. The timing cannot be measured externally and included here for general power sequencing reference.
23. If Deep Sx was entered from S3. SLP\_S4# will remain high while DRAMPWROK is undriven.
24. Timing enabled through soft strap. If t205b is not enabled, the platform is responsible for controlling the assertion timing of PCH\_PWROK and SYS\_PWROK in such a way that it satisfies the PCIe timing requirement of power stable to reset de-assertion.
25. Programmable using PM\_CFG.PWR\_CYC\_DUR. Default is 4 – 5 seconds.
26. Measured from VCCRTC – 10% to RTCRST# reaching 55%\*VCCRTC. VCCRTC is defined as the final settling voltage that the rail ramps.
27. Requirement applies to power failure and surprise power-down scenario. As long as the board follows the recommended power-well control signals (that is, SLP\_S3#, SLP\_A# and SLP\_SUS#), the PCH guarantees proper isolation during the normal graceful power down events.
28. Ensure respective PWROK signals (PCH\_PWROK, APWROK and RSMRST#) toggle appropriately during normal power state transition (for example, S0->Sx->S0, S0->Deep Sx->S0, and so forth.) even if the supply voltage does not drop below the specified value. Use of the stretch registers can be used to achieve this.
29. Timing does not apply after Deep Sx exit when Intel® ME has configured SLP\_S5# and/or SLP\_S4# to rise with SLP\_A#.
30. Full Icc load must be supported by then, end of t258.
31. "Active" is defined as VCCmin and is 1.05V – 5%.
32. VCCHSIO, VCCPCIEPHY, VCCSATAPHY and VCCUSB3PHY cannot take the full 65  $\mu$ s maximum ramp time due to the filters on VCCUSB3PLL and VCCSATA3PLL. Based on the existing recommended filter capacitors for the PLLs, VCCHSIO, VCCPCIEPHY, VCCSATAPHY and VCCUSB3PHY rails will need to ramp within ~22  $\mu$ s.
33. Reflects the default minimum timing. T218 is configurable using PM\_CFG.TIMING\_218.
34. This timing requirement is only applicable in S0 when exiting from MPHY power gated mode. This timing is not applicable on G3/Sx exit to S0.

## 6.6 Power Management Timing Diagrams

Figure 6-1. G3 w/RTC Loss to S4/S5 (with Deep Sx Support) Timing Diagram



**Note:** VCCSUS rail ramps up later in comparison to VCCDSW due to assumption that SLP\_SUS# is used to control power to VCCSUS.

Figure 6-2. G3 w/RTC Loss to S4/S5 (Without Deep Sx Support) Timing Diagram

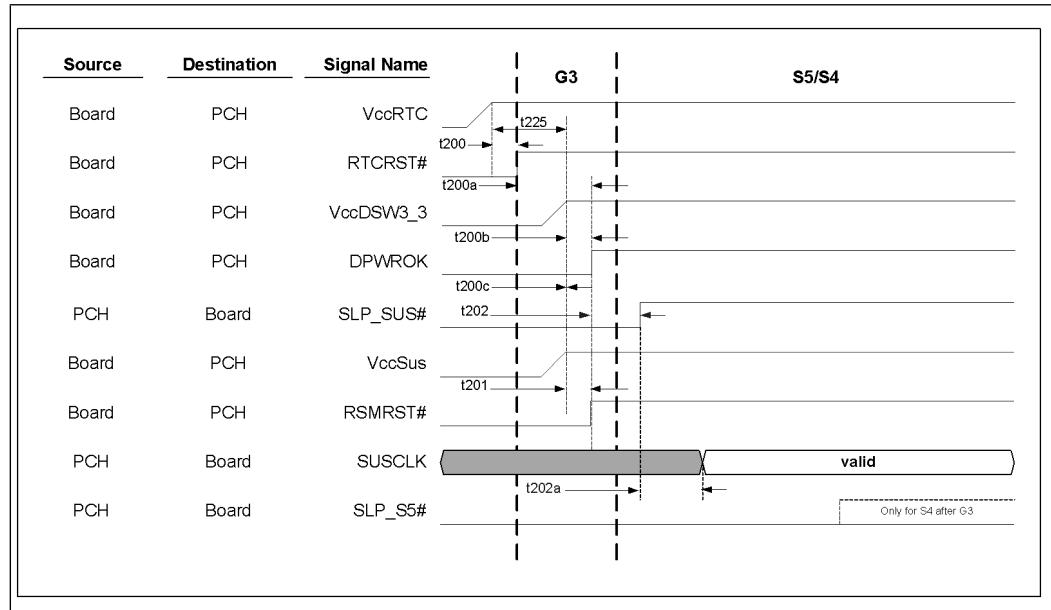


Figure 6-3. S5 to S0 Timing Diagram

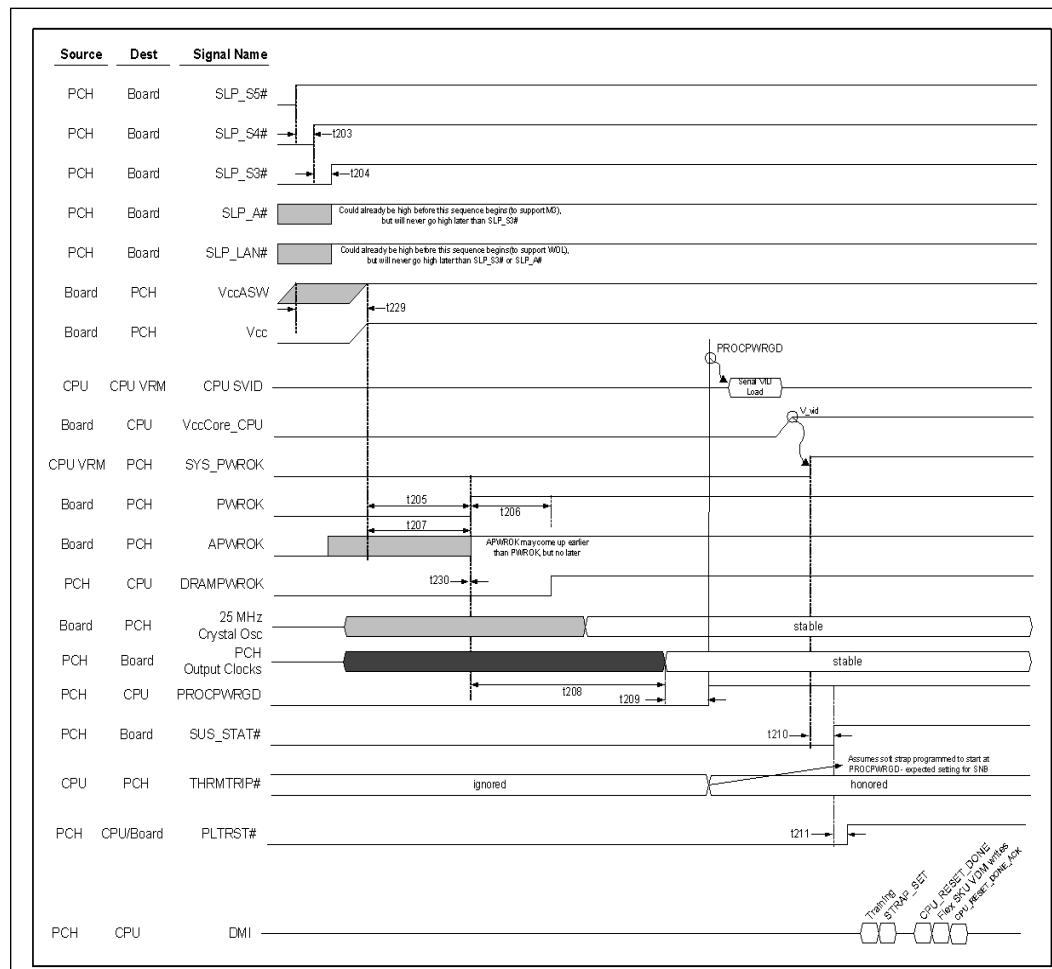


Figure 6-4. S3/M3 to S0 Timing Diagram

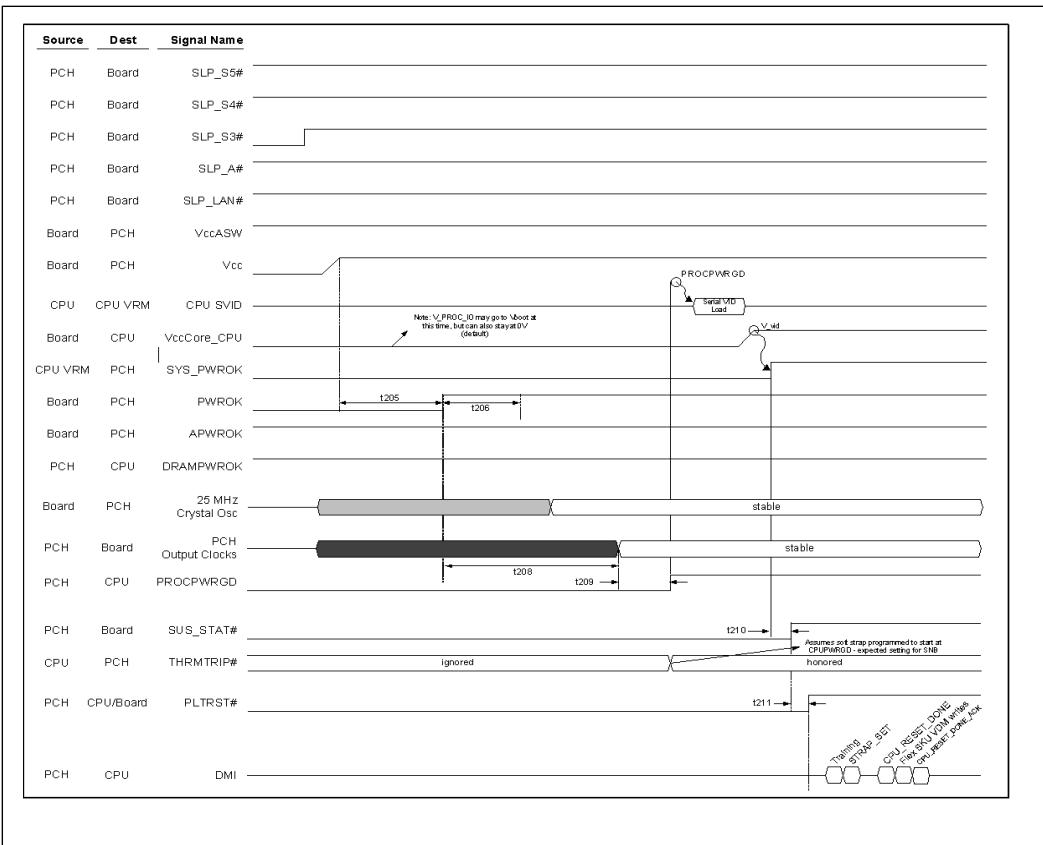


Figure 6-5. S5/M-Off—S5/M3 Timing Diagram

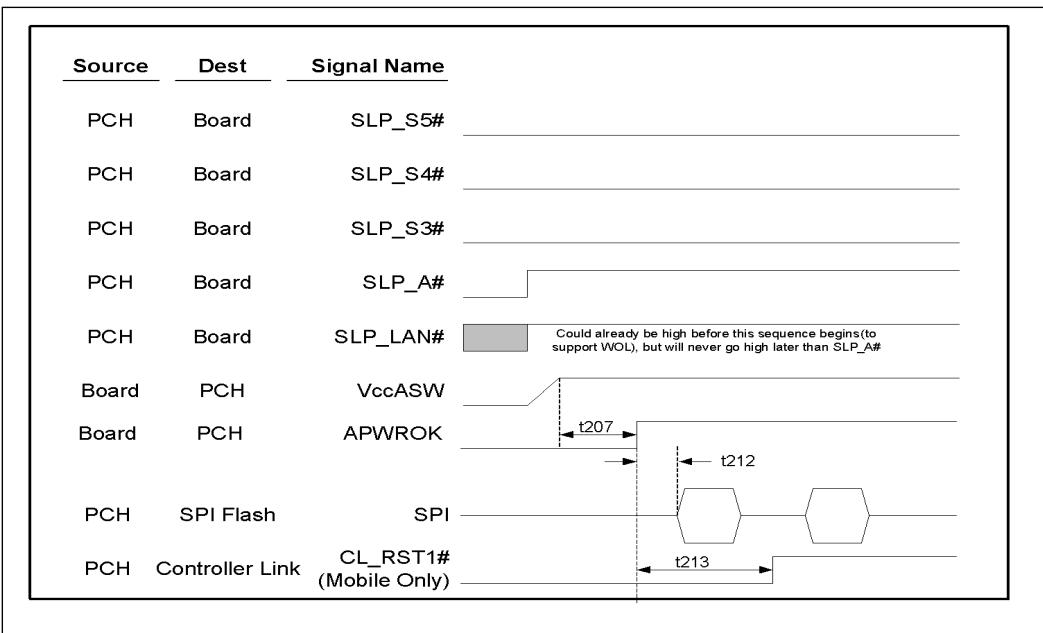


Figure 6-6. S0 to S5 Timing Diagram

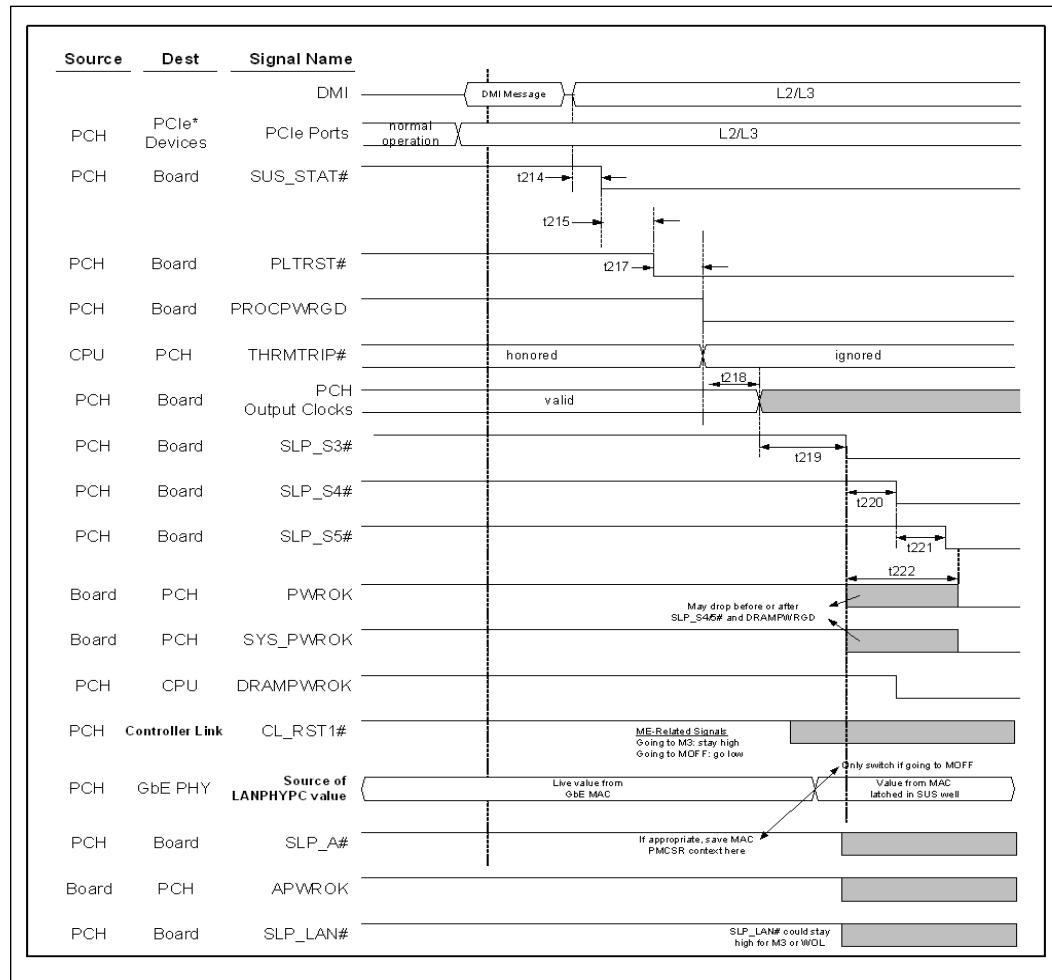


Figure 6-7. S3/S4/S5 to Deep Sx to G3 w/RTC Loss Timing Diagram

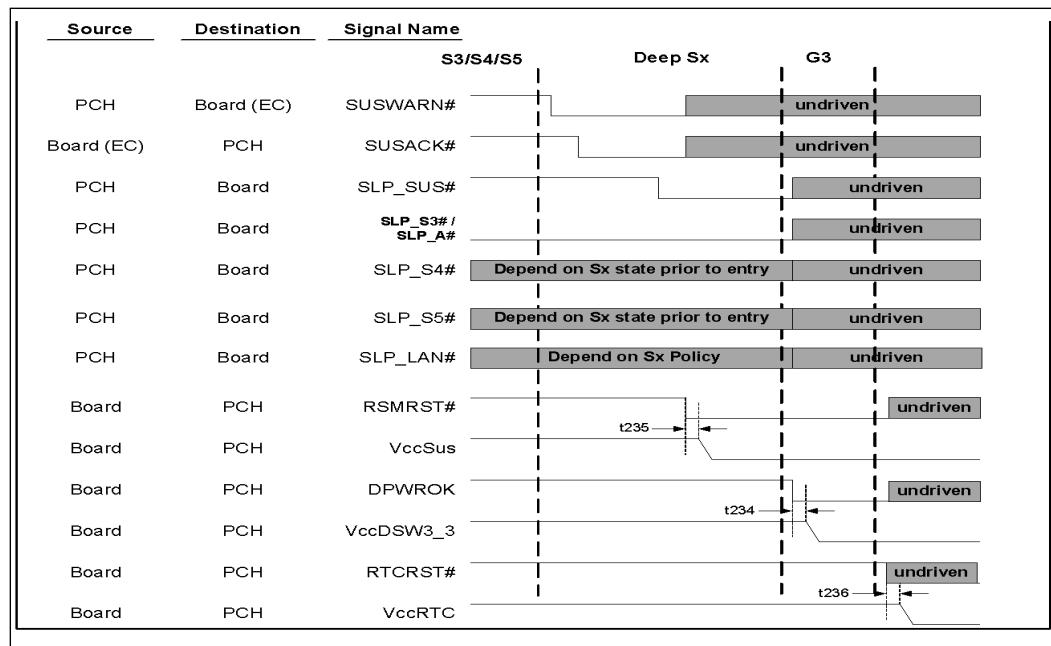
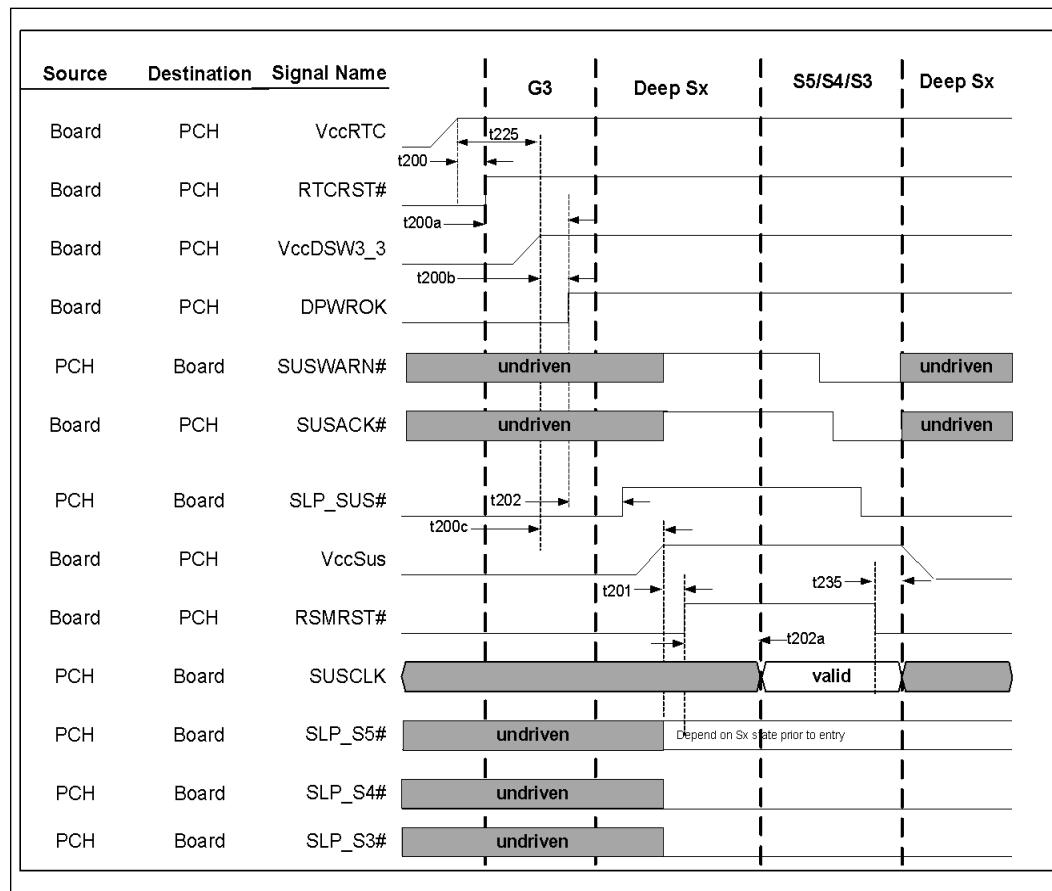


Figure 6-8. G3 to Deep Sx Timing Diagram

**Note:**

On a Deep Sx supported platform, platform must transition to Sx state upon G3 exit, prior to determining that conditions are met for a Deep Sx transition (G3->Sx->Deep Sx).

## 6.7 AC Timing Diagrams

Figure 6-9. Clock Cycle Time

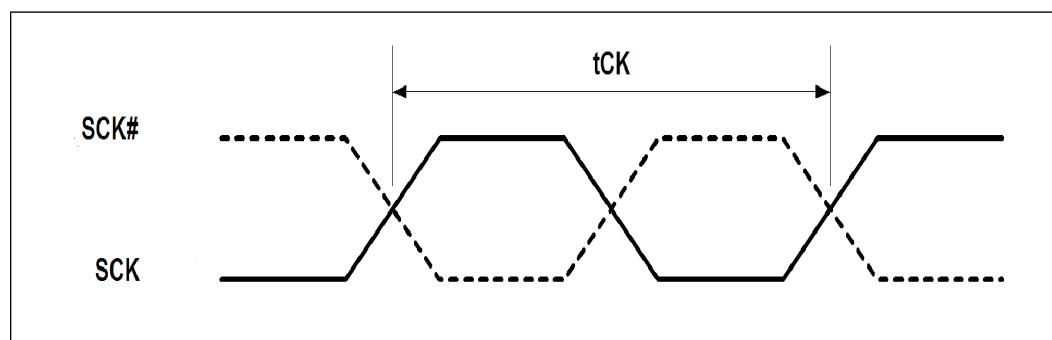


Figure 6-10. Transmitting Position (Data to Strobe)

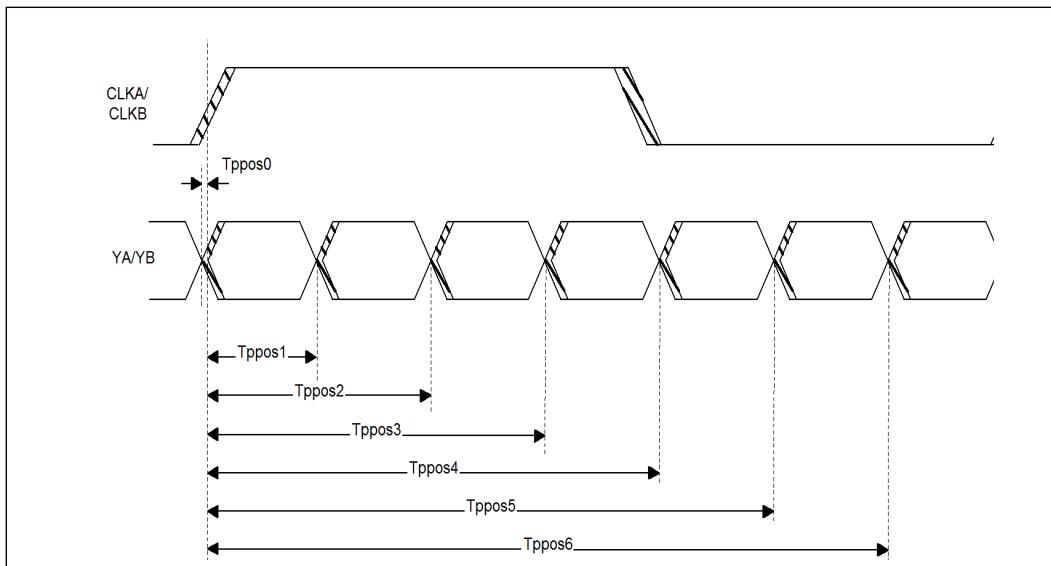


Figure 6-11. Clock Timing

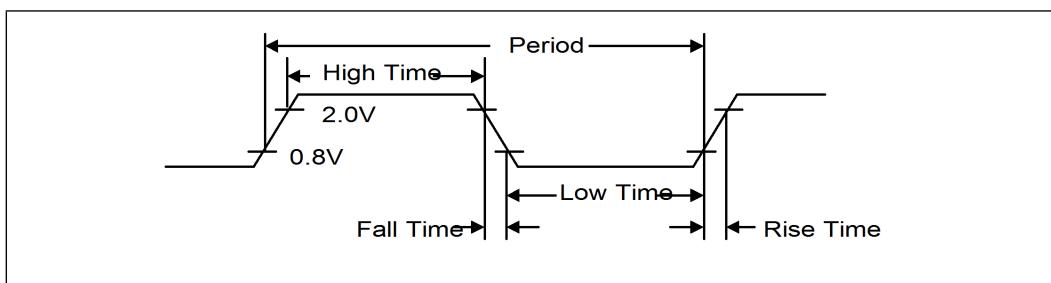


Figure 6-12. Valid Delay from Rising Clock Edge

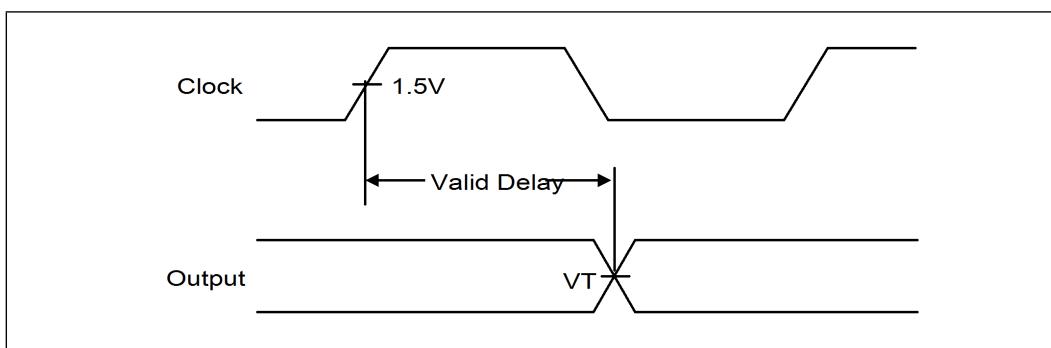


Figure 6-13. Setup and Hold Times

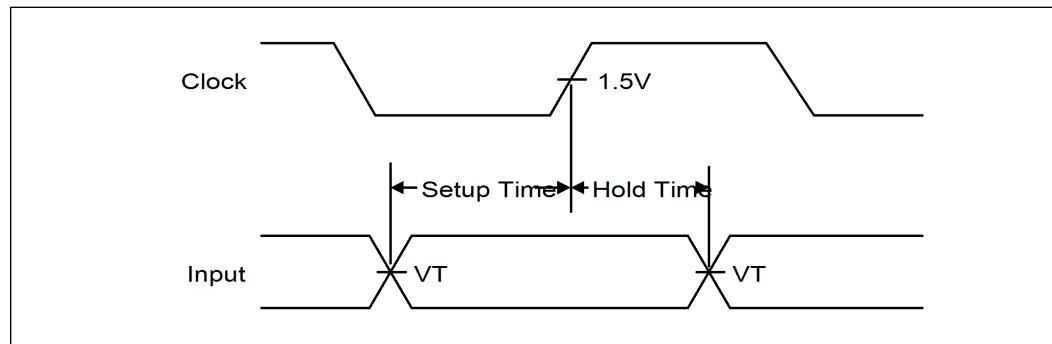


Figure 6-14. Float Delay

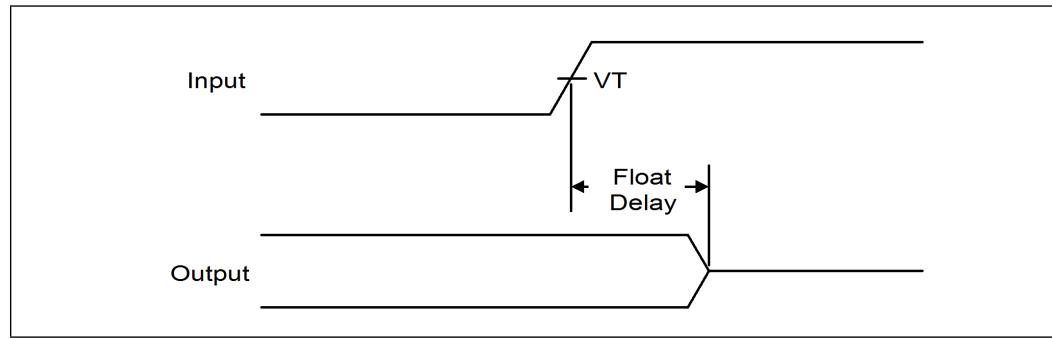


Figure 6-15. Pulse Width

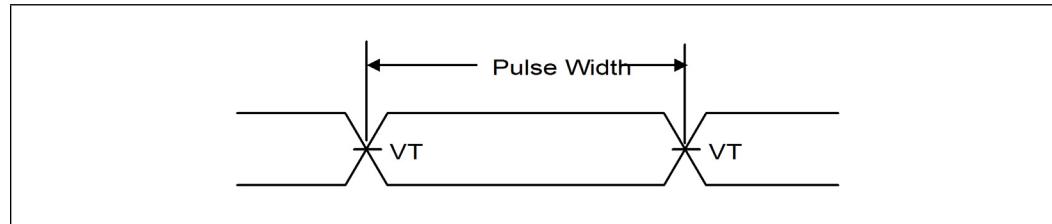


Figure 6-16. Output Enable Delay

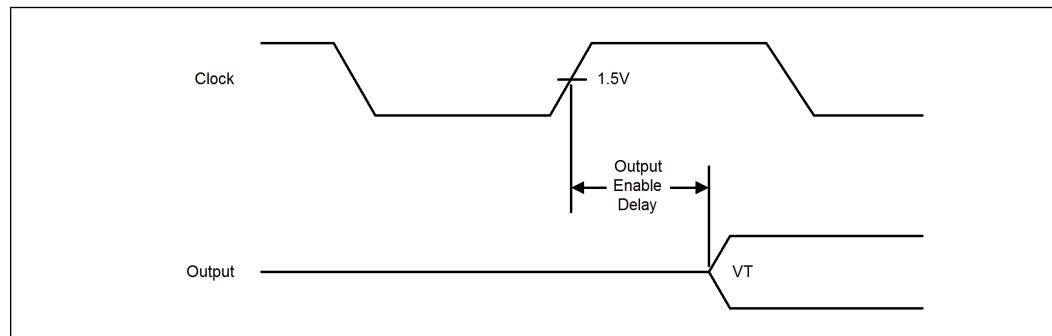


Figure 6-17. USB Rise and Fall Times

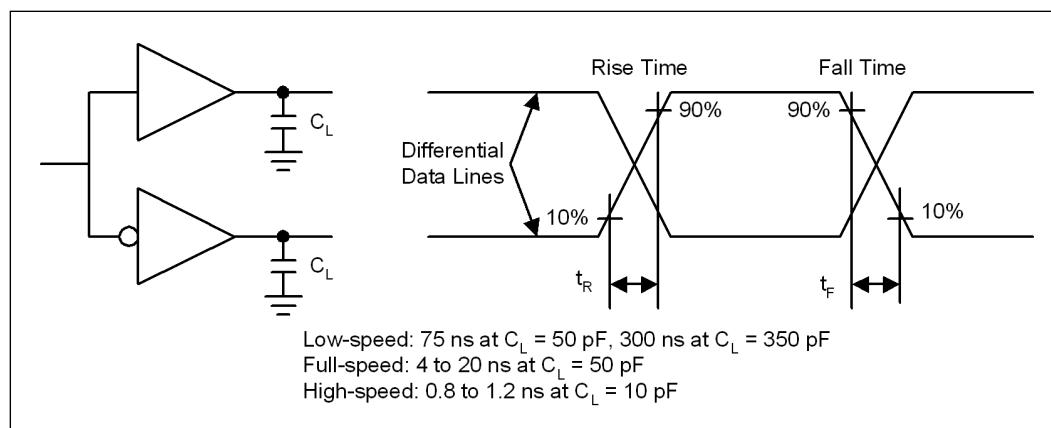


Figure 6-18. USB Jitter

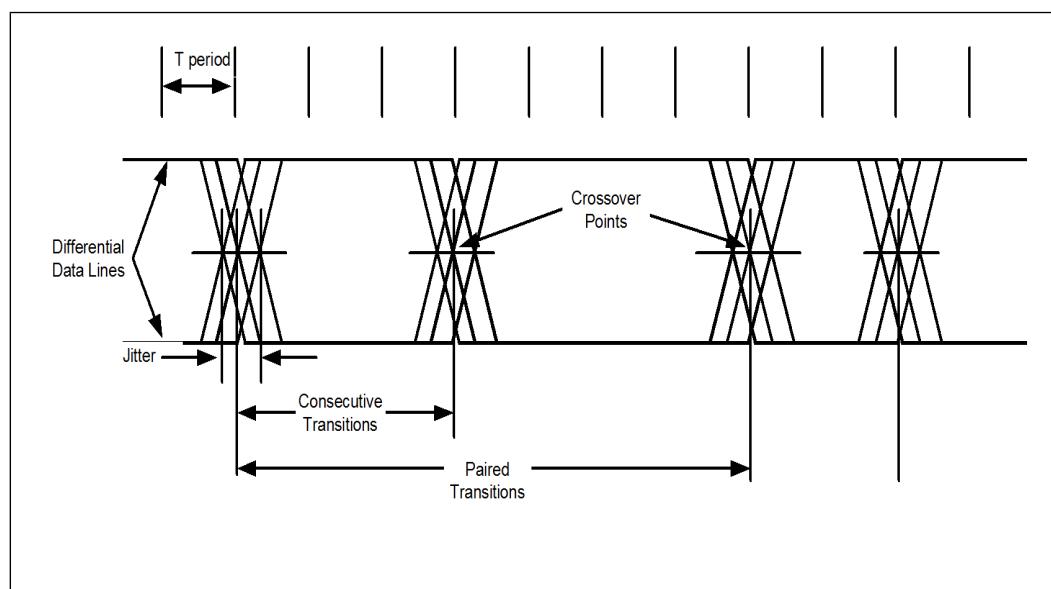


Figure 6-19. USB EOP Width

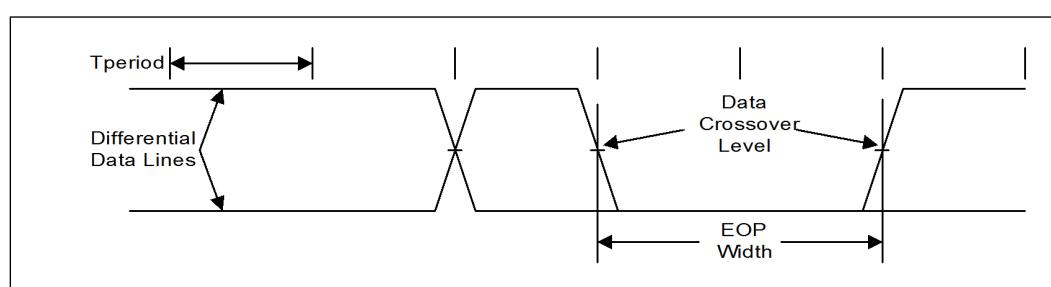
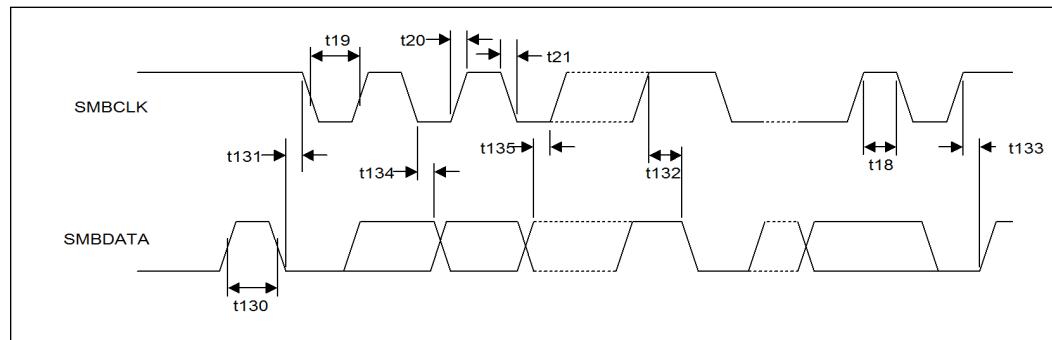
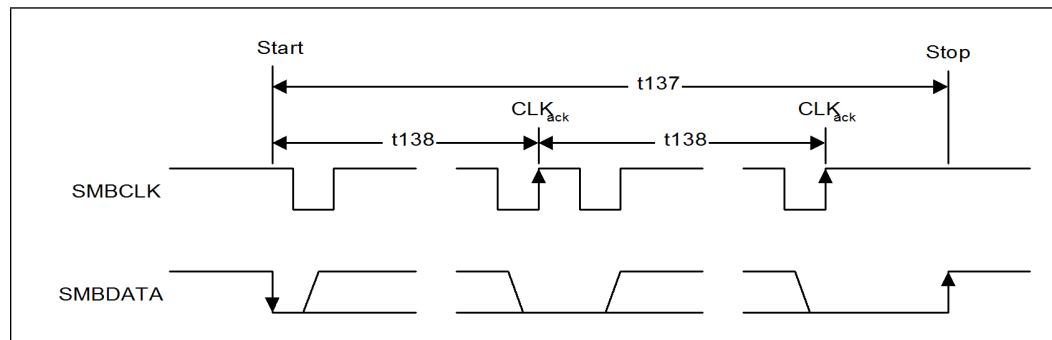


Figure 6-20. SMBus/SMLink Transaction



**Note:** t<sub>xx</sub> also refers to t<sub>xx\_SM</sub>, t<sub>xxx</sub> also refers to t<sub>xxxSMLFM</sub>, SMBCLK also refers to SML[1:0]CLK, and SMBDATA also refers to SML[1:0]DATA in Figure 6-20.

Figure 6-21. SMBus/SMLink Timeout



**Note:** SMBCLK also refers to SML[1:0]CLK and SMBDATA also refers to SML[1:0]DATA in Figure 6-21.

Figure 6-22. SPI Timings

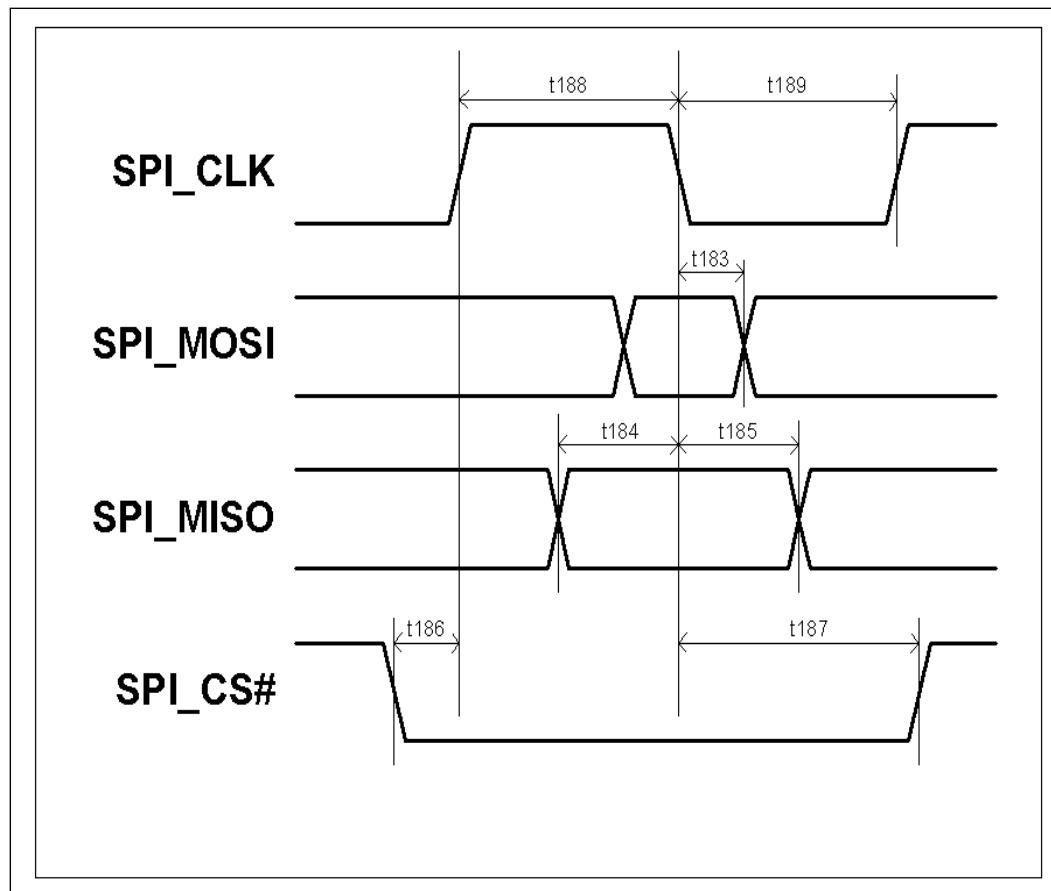


Figure 6-23. Intel® High Definition Audio (Intel® HD Audio) Input and Output Timings

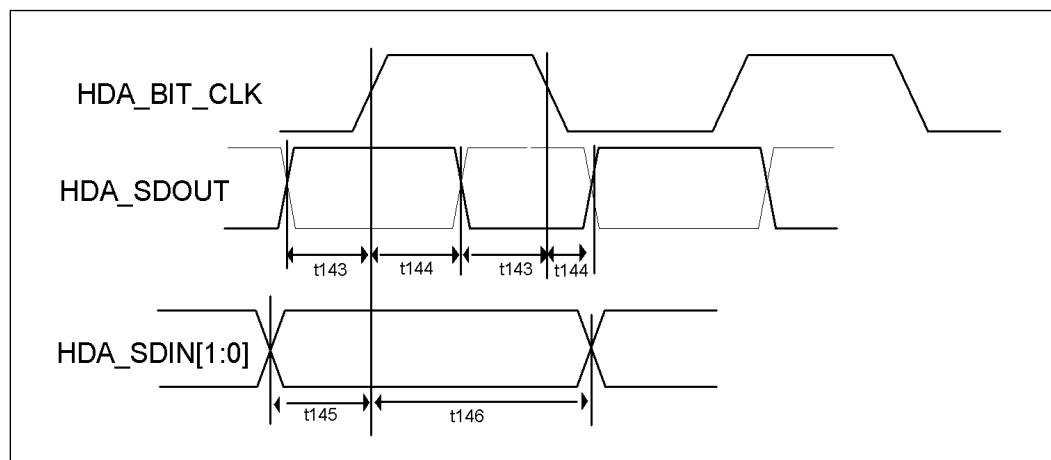


Figure 6-24. Dual Channel Interface Timings—A

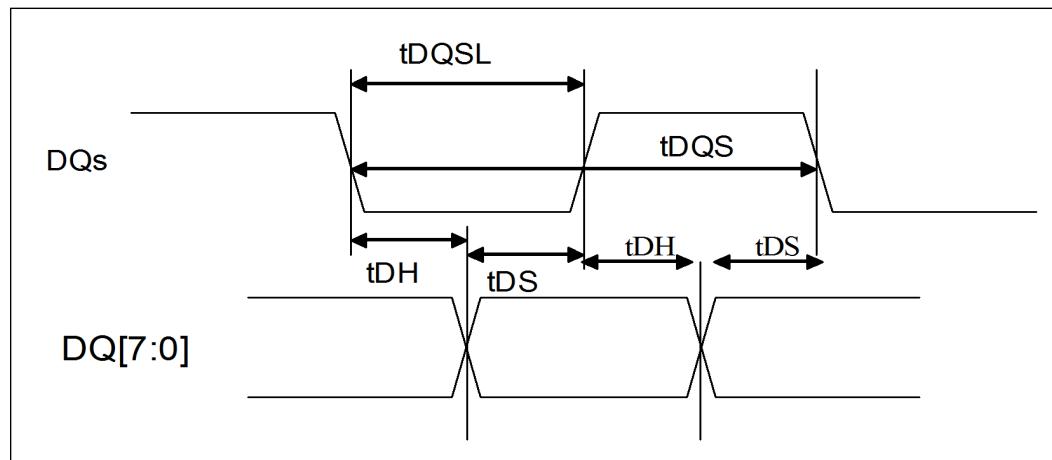


Figure 6-25. Dual Channel Interface Timings—B

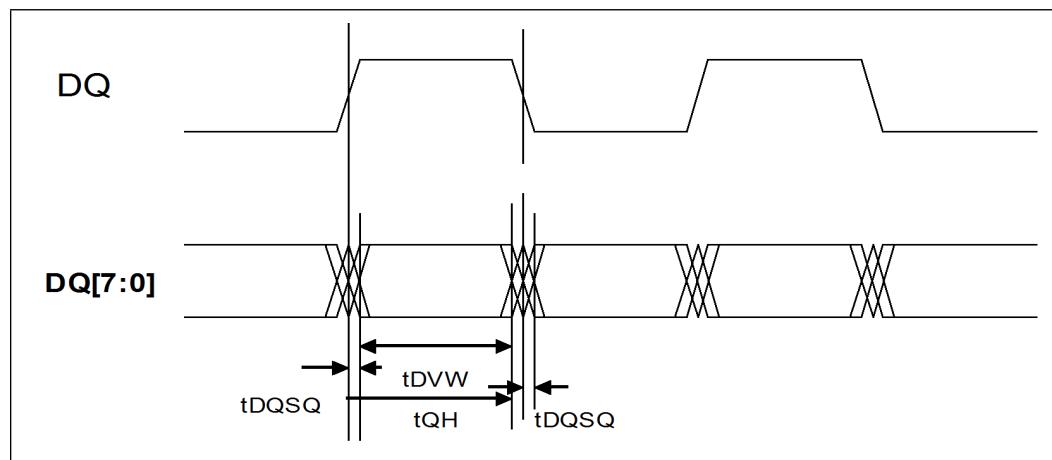


Figure 6-26. LVDS Load and Transition Times

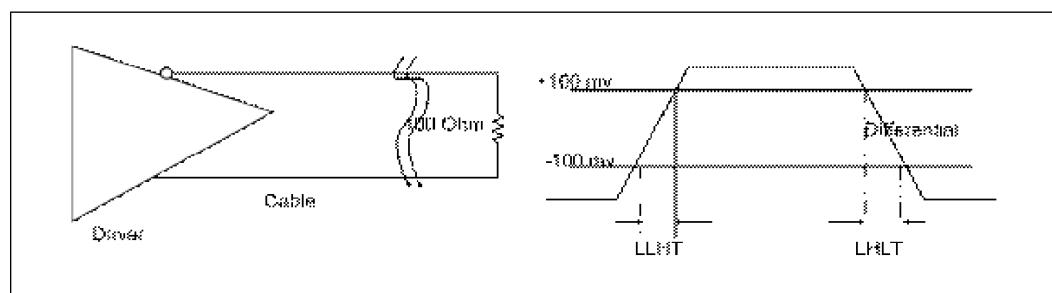


Figure 6-27. Transmitting Position (Data to Strobe)

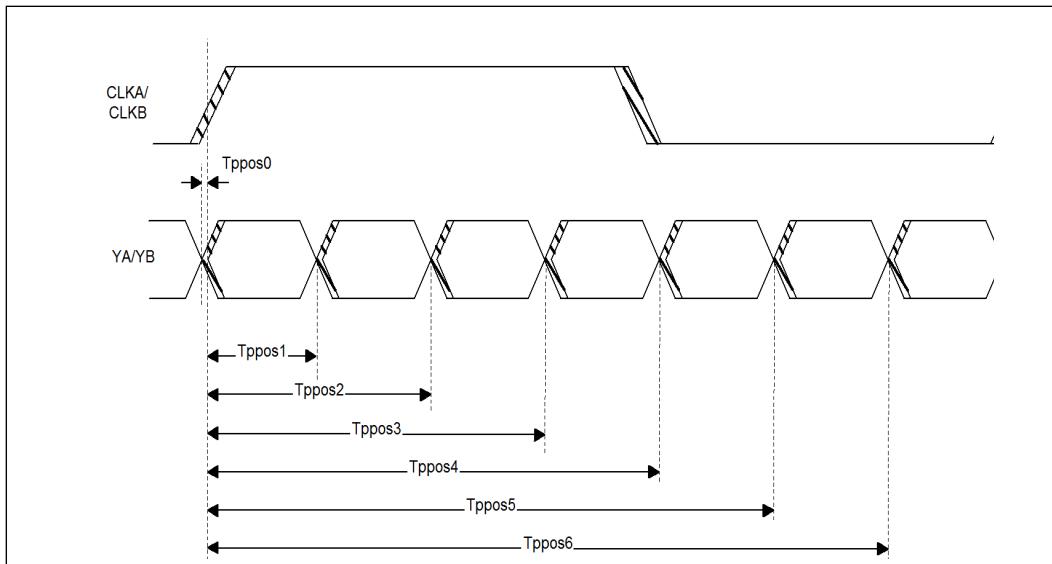


Figure 6-28. PCI Express Transmitter Eye

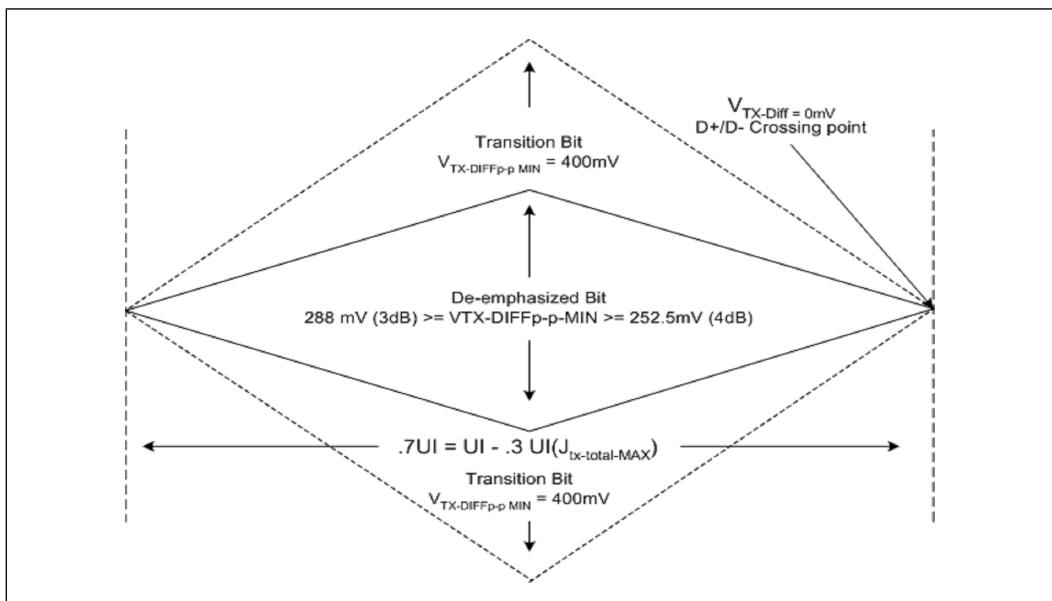


Figure 6-29. PCI Express\* Receiver Eye

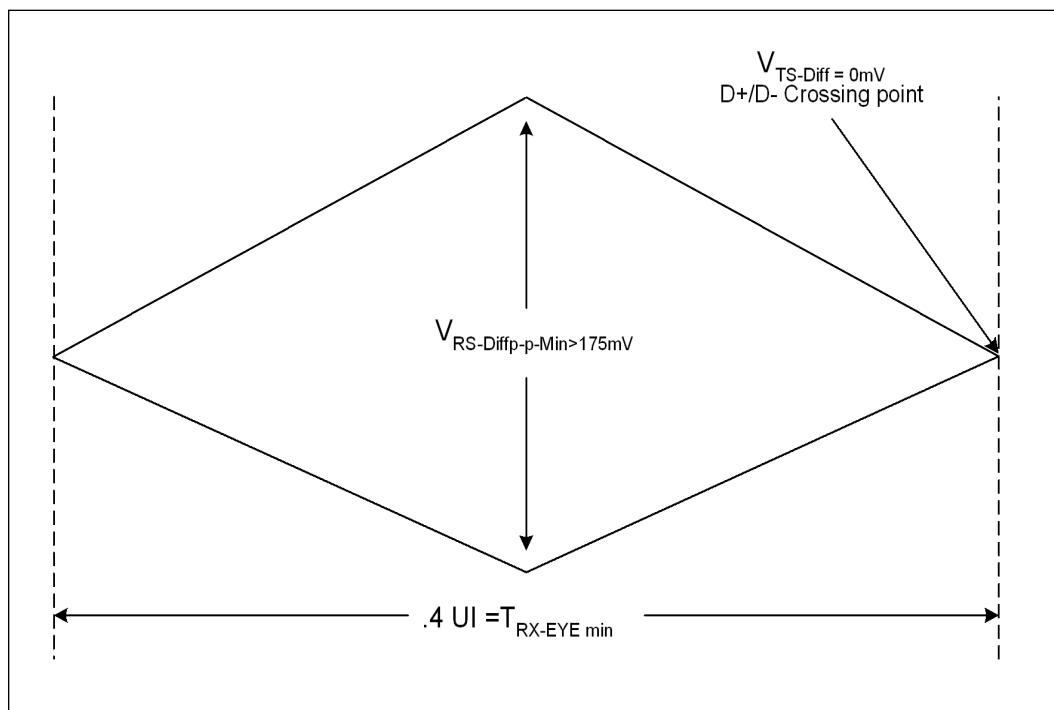
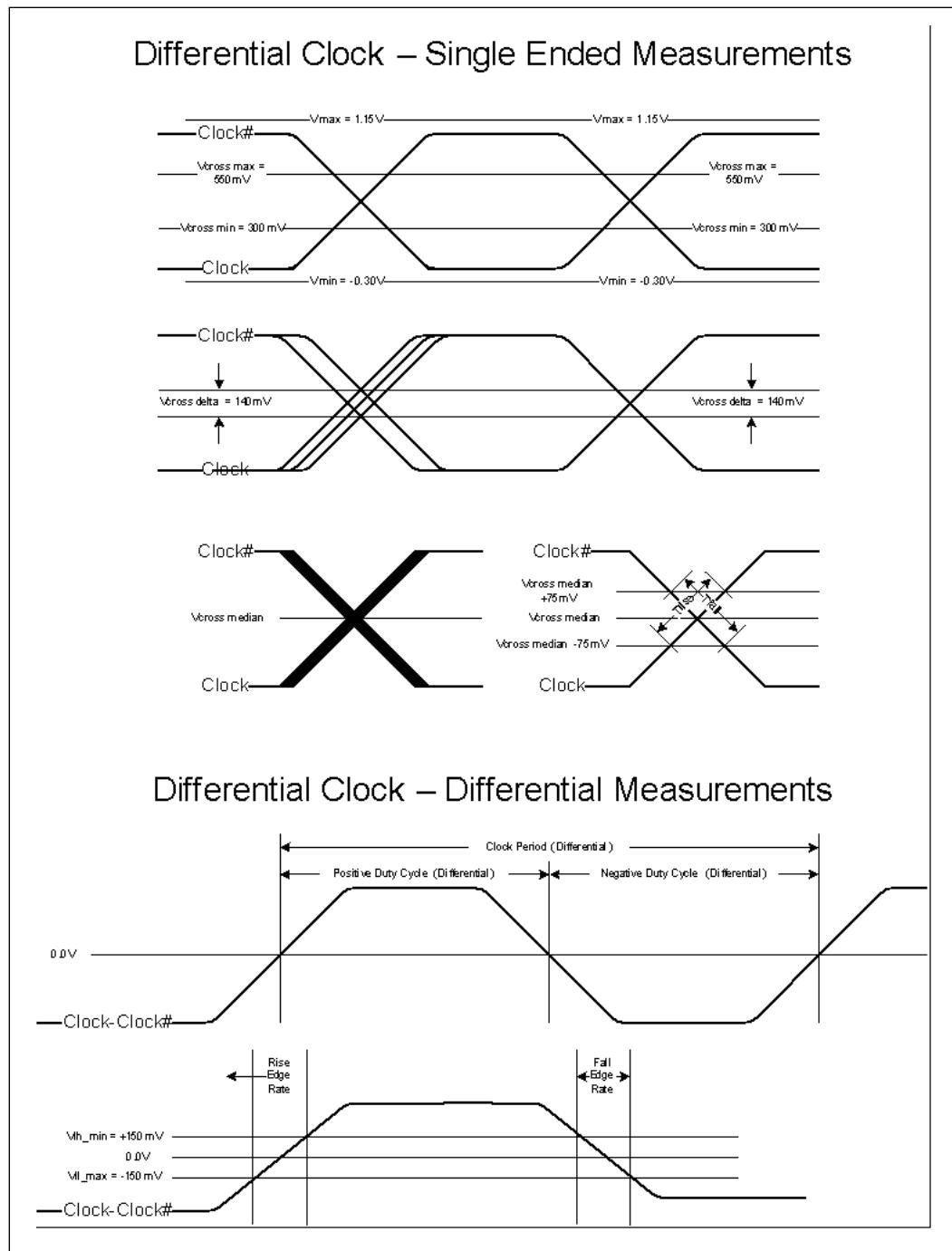


Figure 6-30. Measurement Points for Differential Waveforms



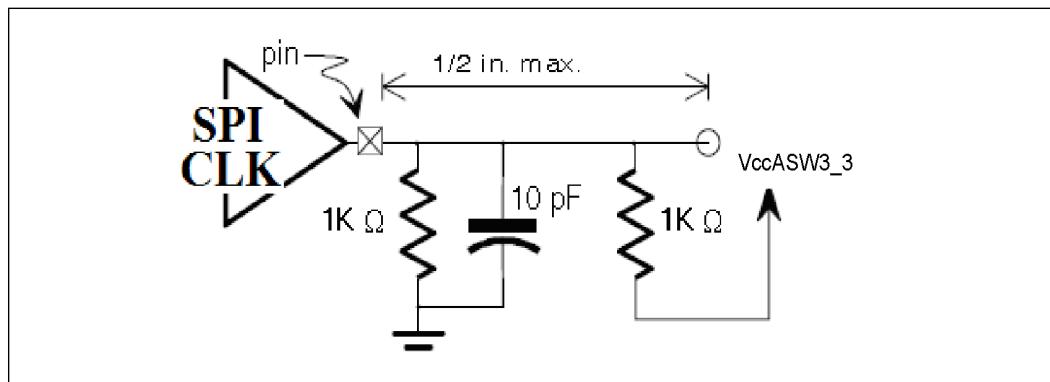
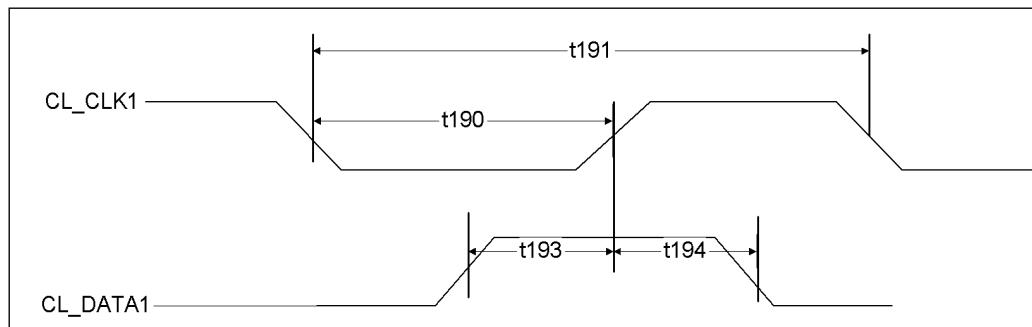
**Figure 6-31. PCH Test Load****Figure 6-32. Controller Link Receive Timings**

Figure 6-33. Controller Link Receive Slew Rate

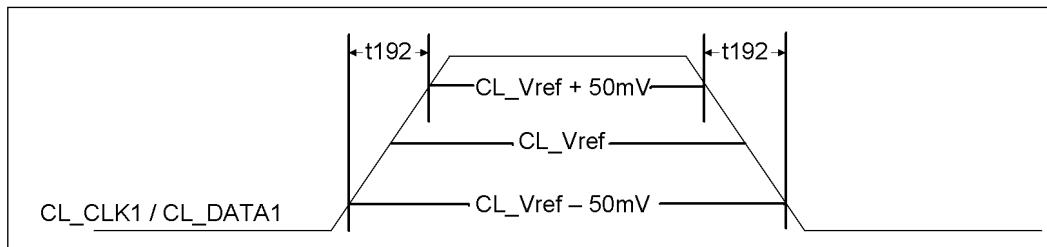


Figure 6-34. Windows\* InstantGo Power Save Mode (Windows\* InstantGo PSM) Timing Diagram

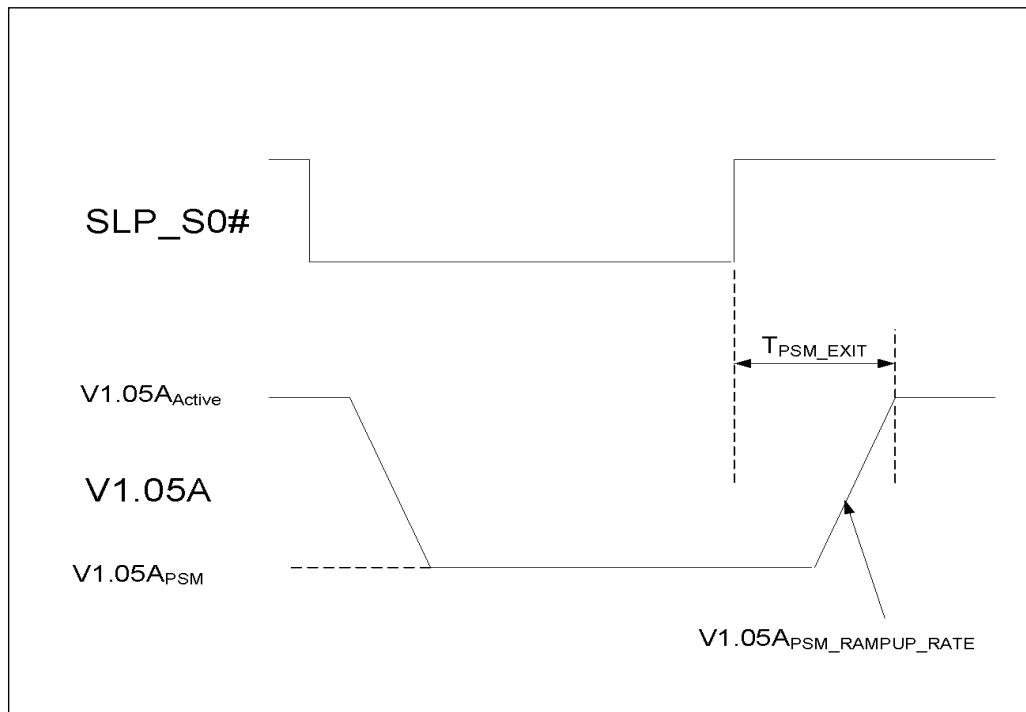


Figure 6-35. Vbus to PCH DSW Well Ramp Up/Down Requirement

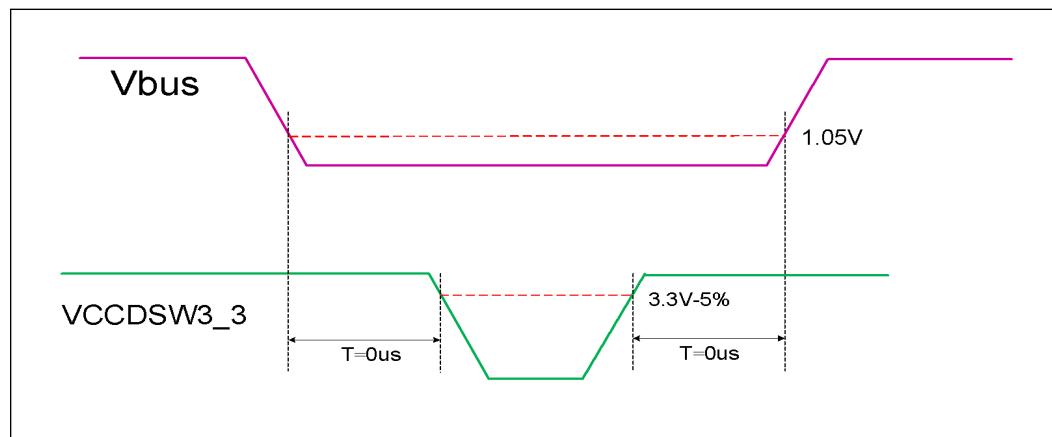


Figure 6-36. Suspend Well Ramp Up/Down Requirement

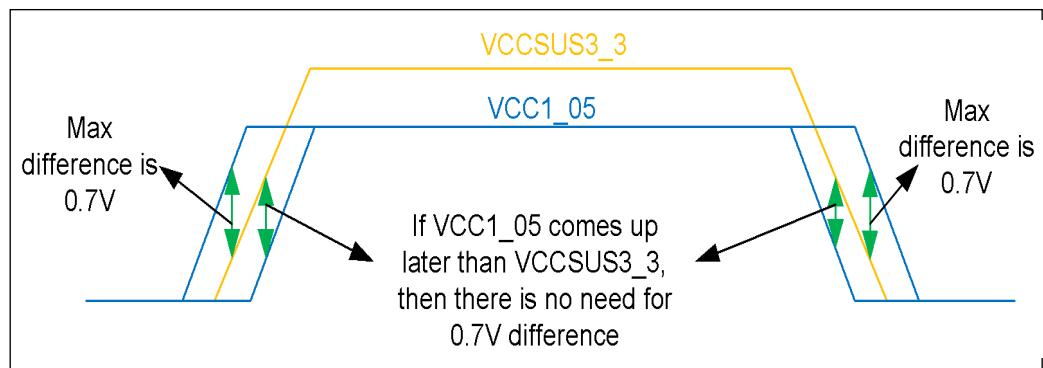
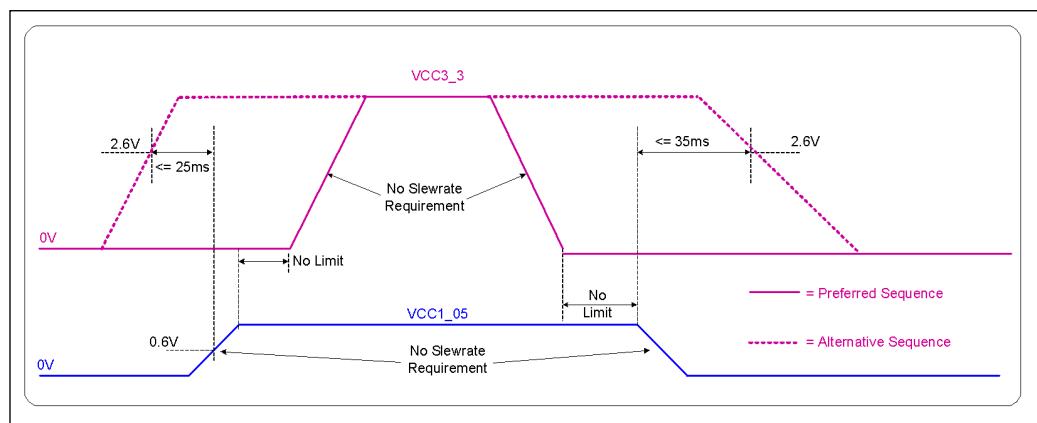
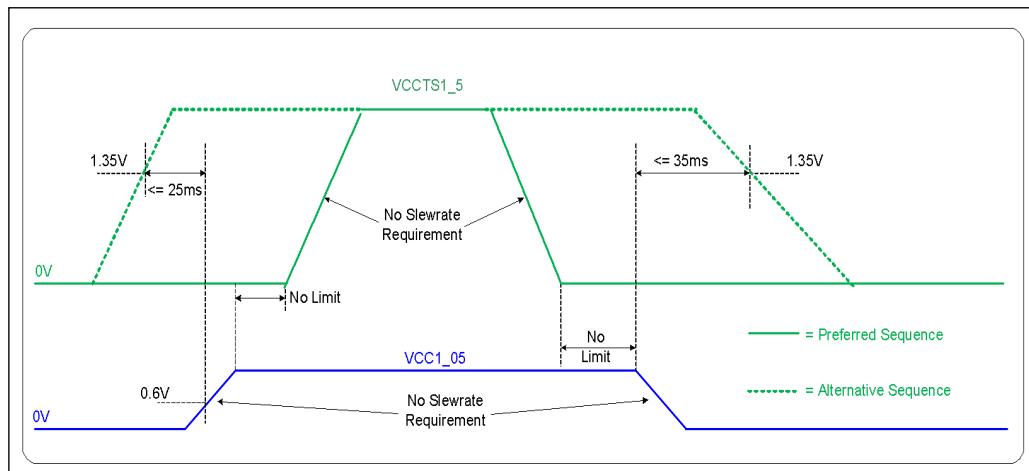


Figure 6-37. Sequencing Requirements Between PCH VCC3\_3 and VCC1\_05 Core Rail



**Figure 6-38. Sequencing Requirements Between PCH VCCTS1\_5 and VCC1\_05 Core Rail**



## 6.8 Sequencing Rails Within the Same Well

**Table 6-29. VCCDSW3\_3 to Vbus Voltage Ramp Up/Down Requirements**

Voltage Rail 1	Voltage Rail 2	Power-Up Requirement	Power-Down Requirement	Figure
VCCDSW3_3	Platform USB Vbus	VCCDSW3_3 ramps up before Vbus reaches 1.05V while ramping up.	VCCDSW3_3 ramps down after Vbus reaches 1.05V while ramping down.	6-35

**Table 6-30. Suspend Well Voltage Ramp Up/Down Requirements**

Voltage Rail 1	Voltage Rail 2	Power-Up Requirement	Power-Down Requirement	Figure
VCCSUS3_3 (Note 1)	DCPSUS1, DCPSUS2, DCPSUS3 DCPSUS4	VCCSUS3_3 must be powered up before DCPSUS, or not more than 0.7V below DCPSUS* while the two rails ramp up.	VCCSUS3_3 must be powered down after DCPSUS, or not more than 0.7V below DCPSUS while the two rails ramp down.	6-36

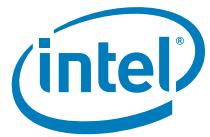
**NOTES:**

1. In external VR mode, this relationship needs to be met by the platform. In internal VR mode, the PCH will meet this timing.

**Table 6-31. Core Well Voltage Ramp Up/Down Requirements**

Voltage Rail 1	Voltage Rail 2	Power-Up Requirement	Power-Down Requirement	Figure
VCC1_05	VCC3_3	Preferred Option: <ul style="list-style-type: none"> <li>VCC1_05 powers up before VCC3_3</li> </ul> Alternative Option: <ul style="list-style-type: none"> <li>VCC3_3 may power up before VCC1_05, but VCC1_05 must ramp up to 0.6V within 25 ms of VCC3_3 ramping to 2.6V.</li> </ul>	Preferred Option: <ul style="list-style-type: none"> <li>VCC1_05 powers down after VCC3_3</li> </ul> Alternative Option: <ul style="list-style-type: none"> <li>VCC1_05 may power down before VCC3_3, but VCC3_3 must ramp down to 2.6V within 35 ms assuming a linear ramp.</li> </ul>	6-37
VCC1_05	VCCTS1_5	Preferred Option: <ul style="list-style-type: none"> <li>VCC1_05 powers up before VCCTS1_5</li> </ul> Alternative Option: <ul style="list-style-type: none"> <li>VCCTS1_5 may power up before VCC1_05, but VCC1_05 must ramp up to 0.6V within 25 ms of VCCTS1_5 ramping to 1.35V.</li> </ul>	Preferred Option: <ul style="list-style-type: none"> <li>VCC1_05 powers down after VCCTS1_5</li> </ul> Alternative Option: <ul style="list-style-type: none"> <li>VCC1_05 may power down before VCCTS1_5, but VCCTS1_5 must ramp down to 1.35V within 35 ms assuming a linear ramp.</li> </ul>	6-38

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## 7

# Register and Memory Mapping

The PCH contains registers that are located in the processor's I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes the PCH I/O and memory maps at the register-set level. Register access is also described. Register-level address maps and Individual register bit descriptions are provided in the following chapters. The following notations and definitions are used in the register/instruction description chapters.

<b>RO</b>	Read Only. In some cases, if a register is read only, writes to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
<b>WO</b>	Write Only. In some cases, if a register is write only, reads to this register location have no effect. However, in other cases, two separate registers are located at the same location where a read accesses one of the registers and a write accesses the other register. See the I/O and memory map tables for details.
<b>R/W</b>	Read/Write. A register with this attribute can be read and written.
<b>R/WC</b>	Read/Write Clear. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.
<b>R/WO</b>	Read/Write-Once. A register bit with this attribute can be written only once after power up. After the first write, the bit becomes RO.
<b>R/WL</b>	Read/Write Lockable. A register bit with the attribute can be read at any time but writes may only occur if the associated lock bit is set to unlock. If the associated lock bit is set to lock, this register bit becomes RO unless otherwise indicated.
<b>R/WLO</b>	Read/Write, Lock-Once. A register bit with this attribute can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes RO.
<b>R/W/SN</b>	Read/Write register initial value loaded from NVM.
<b>Reserved</b>	The value of reserved bits must never be changed. For details, see <a href="#">Section 7.2</a> .
<b>Default</b>	When the PCH is reset, it sets its registers to predetermined default states. It is the responsibility of the system initialization software to determine configuration, operating parameters, and optional system features that are applicable, and to program the PCH registers accordingly.

## 7.1 PCI Devices and Functions

The PCH incorporates a variety of PCI devices and functions, as shown in [Table 7-1](#).

If for some reason, the particular system platform does not want to support any one of the Device Functions, with the exception of D30:F0, they can individually be disabled. The integrated Gigabit Ethernet controller will be disabled if no Platform LAN Connect component is detected (See [Section 5.3](#)). When a function is disabled, it does not appear at all to the software. A disabled function will not respond to any register reads or writes, insuring that these devices appear hidden to software.

**Table 7-1. PCI Devices and Functions**

Bus:Device:Function	Function Description
Bus 0:Device 31:Function 0	LPC Controller <sup>1</sup>
Bus 0:Device 31:Function 2	SATA Controller
Bus 0:Device 31:Function 3	SMBus Controller
Bus 0:Device 31:Function 6	Thermal Subsystem
Bus 0:Device 29:Function 0 <sup>2</sup>	USB EHCI Controller
Bus 0:Device 28:Function 0	PCI Express* Port 1
Bus 0:Device 28:Function 1	PCI Express* Port 2
Bus 0:Device 28:Function 2	PCI Express* Port 3
Bus 0:Device 28:Function 3	PCI Express* Port 4
Bus 0:Device 28:Function 4	PCI Express* Port 5
Bus 0:Device 28:Function 5	PCI Express* Port 6
Bus 0:Device 27:Function 0	Intel® High Definition Audio Controller
Bus 0:Device 25:Function 0	Gigabit Ethernet Controller
Bus 0:Device 23:Function 0	SDIO Controller
Bus 0:Device 22:Function 0	Intel® Management Engine Interface #1
Bus 0:Device 22:Function 1	Intel® Management Engine Interface #2
Bus 0:Device 22:Function 2	IDE-R
Bus 0:Device 22:Function 3	KT
Bus 0:Device 21:Function 0	Intel® Serial I/O DMA
Bus 0:Device 21:Function 1	Intel® Serial I/O I <sup>2</sup> C Controller #0
Bus 0:Device 21:Function 2	Intel® Serial I/O I <sup>2</sup> C Controller #1
Bus 0:Device 21:Function 3	Intel® Serial I/O GSPI Controller #0
Bus 0:Device 21:Function 4	Intel® Serial I/O GSPI Controller #1
Bus 0:Device 21:Function 5	Intel® Serial I/O UART Controller #0
Bus 0:Device 21:Function 6	Intel® Serial I/O UART Controller #1
Bus 0:Device 20:Function 0	xHCI Controller
Bus 0:Device 19:Function 0	Intel® Smart Sound Technology Controller

**NOTES:**

1. The PCI-to-LPC bridge contains registers that control LPC, Power Management, System Management, GPIO, Processor Interface, RTC, Interrupts, Timers, and DMA.
2. Prior to BIOS initialization of the PCH USB subsystem, the EHCI controllers will appear as Function 7. After BIOS initialization, the EHCI controllers will be Function 0.
3. This table shows the default PCI Express\* Function Number-to-Root Port mapping. Function numbers for a given root port are assignable through the "Root Port Function Number and Hidden for PCI Express\* Root Ports" register (RCBA+0404h).

## 7.2 PCI Configuration Map

Each PCI function on the PCH has a set of PCI configuration registers. The register address map tables for these register sets are included at the beginning of the chapter for the particular function.

Configuration Space registers are accessed through configuration cycles on the PCI bus by the Host bridge using configuration mechanism #1 detailed in the *PCI Local Bus Specification, Revision 2.3*.

Some of the PCI registers contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions, and then written back. Software does not need to perform read, merge, write operation for the configuration address register.

In addition to reserved bits within a register, the configuration space contains reserved locations. Software should not write to reserved PCI configuration locations in the device-specific region (above address offset 3Fh).

## 7.3 I/O Map

The I/O map is divided into Fixed and Variable address ranges. Fixed ranges cannot be moved, but in some cases can be disabled. Variable ranges can be moved and can also be disabled.

### 7.3.1 Fixed I/O Address Ranges

Table 7-2 shows the Fixed I/O decode ranges from the processor perspective.

**Note:**

For each I/O range, there may be separate behavior for reads and writes. I/O cycles that go to target ranges that are marked as "Reserved" will not be decoded by the PCH, and will be passed to PCI unless the Subtractive Decode Policy bit is set (D31:F0:Offset 42h, bit 0). If a PCI master targets one of the fixed I/O target ranges, it will be positively decoded by the PCH in medium speed.

Address ranges that are not listed or marked "Reserved" are **not** decoded by the PCH (unless assigned to one of the variable ranges).

**Table 7-2. Fixed I/O Ranges Decoded by PCH (Sheet 1 of 2)**

I/O Address	Read Target	Write Target	Internal Unit
00h-1Fh	RESERVED	RESERVED	Not Decoded
20h-21h	Interrupt Controller	Interrupt Controller	Interrupt
24h-25h	Interrupt Controller	Interrupt Controller	Interrupt
28h-29h	Interrupt Controller	Interrupt Controller	Interrupt
2Ch-2Dh	Interrupt Controller	Interrupt Controller	Interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt Controller	Interrupt Controller	Interrupt
34h-35h	Interrupt Controller	Interrupt Controller	Interrupt
38h-39h	Interrupt Controller	Interrupt Controller	Interrupt
3Ch-3Dh	Interrupt Controller	Interrupt Controller	Interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT (8254)
43h	RESERVED	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	RESERVED	Timer/Counter	PIT
60h	Microcontroller	Microcontroller	Forwarded to LPC
61h	NMI Controller	NMI Controller	Processor I/F
62h	Microcontroller	Microcontroller	Forwarded to LPC
63h	NMI Controller	NMI Controller	Processor I/F
64h	Microcontroller	Microcontroller	Forwarded to LPC
65h	NMI Controller	NMI Controller	Processor I/F
66h	Microcontroller	Microcontroller	Forwarded to LPC
67h	NMI Controller	NMI Controller	Processor I/F
70h	RESERVED <sup>1</sup>	NMI and RTC Controller	RTC
71h	RTC Controller	RTC Controller	RTC
72h	RTC Controller	NMI and RTC Controller	RTC
73h	RTC Controller	RTC Controller	RTC
74h	RTC Controller	NMI and RTC Controller	RTC
75h	RTC Controller	RTC Controller	RTC
76h	RTC Controller	NMI and RTC Controller	RTC
77h	RTC Controller	RTC Controller	RTC
80h	LPC or PCIe <sup>2</sup>	LPC or PCIe <sup>2</sup>	Forwarded to LPC or PCIe*
81h-83h	RESERVED	RESERVED	Not Decoded
84h-86h	RESERVED	LPC or PCIe*	Forwarded to LPC or PCIe*
87h	RESERVED	RESERVED	Not Decoded
88h	RESERVED	LPC or PCIe <sup>2</sup>	Forwarded to LPC or PCIe*
89h-8Bh	RESERVED	RESERVED	Not Decoded
8Ch-8Eh	RESERVED	LPC or PCIe <sup>2</sup>	Forwarded to LPC or PCIe*
8Fh	RESERVED	RESERVED	Not Decoded
90h	Alias to 80h	Alias to 80h	Forwarded to LPC
91h	RESERVED	RESERVED	Not Decoded

**Table 7-2. Fixed I/O Ranges Decoded by PCH (Sheet 2 of 2)**

I/O Address	Read Target	Write Target	Internal Unit
92h	Reset Generator	Reset Generator	Processor I/F
93h-9Fh	RESERVED	RESERVED	Forwarded to LPC
A0h-A1h	Interrupt Controller	Interrupt Controller	Interrupt
A4h-A5h	Interrupt Controller	Interrupt Controller	Interrupt
A8h-A9h	Interrupt Controller	Interrupt Controller	Interrupt
ACh-ADh	Interrupt Controller	Interrupt Controller	Interrupt
B0h-B1h	Interrupt Controller	Interrupt Controller	Interrupt
B2h-B3h	Power Management	Power Management	Power Management
B4h-B5h	Interrupt Controller	Interrupt Controller	Interrupt
B8h-B9h	Interrupt Controller	Interrupt Controller	Interrupt
BCh-BDh	Interrupt Controller	Interrupt Controller	Interrupt
C0h-DFh	RESERVED	RESERVED	Not Decoded
F0h	Interrupt Controller	Interrupt Controller	Processor I/F
170h-177h	SATA Controller, PCI, or PCIe*	SATA Controller, PCI, or PCIe*	SATA
1F0h-1F7h	SATA Controller, PCI, or PCIe*	SATA Controller, PCI, or PCIe*	SATA
200h-207h	Gameport Low	Gameport Low	Forwarded to LPC
208h-20Fh	Gameport High	Gameport High	Forwarded to LPC
376h	SATA Controller, PCI, or PCIe*	SATA Controller, PCI, or PCIe*	SATA
3F6h	SATA Controller, PCI, or PCIe*	SATA Controller, PCI, or PCIe*	SATA
4D0h-4D1h	Interrupt Controller	Interrupt Controller	Interrupt
CF9h	Reset Generator	Reset Generator	Processor I/F

**NOTES:**

1. See [Section 10.6.2](#).
2. Depends on RPD bit. See [Chapter 10](#).

### 7.3.2 Variable I/O Decode Ranges

Table 7-3 shows the Variable I/O Decode Ranges. They are set using Base Address Registers (BARs) or other configuration bits in the various PCI configuration spaces. The plug-N-play software (PCI or ACPI) can use their configuration mechanisms to set and adjust these values.

**Warning:** The Variable I/O Ranges should not be set to conflict with the Fixed I/O Ranges. Unpredictable results if the configuration software allows conflicts to occur. The PCH does not perform any checks for conflicts.

**Table 7-3. Variable I/O Decode Ranges**

Range Name	Map To	Size (Bytes)	Target
ACPI	Anywhere in 64KB I/O Space	64	Power Management
IDE Bus Master	Anywhere in 64KB I/O Space	1. 16 or 32 2. 16	1. SATA Host Controller #1, #2 2. IDE-R
Native IDE Command	Anywhere in 64KB I/O Space <sup>1</sup>	8	1. SATA Host Controller #1, #2 2. IDE-R
Native IDE Control	Anywhere in 64KB I/O Space <sup>1</sup>	4	1. SATA Host Controller #1, #2 2. IDE-R
SATA Index/Data Pair	Anywhere in 64KB I/O Space	16	SATA Host Controller #1, #2
SMBus	Anywhere in 64KB I/O Space	32	SMBus Unit
TCO	96 Bytes above ACPI Base	32	TCO Unit
GPIO	Anywhere in 64KB I/O Space	128	GPIO Unit
Parallel Port	3 Ranges in 64KB I/O Space	8 <sup>3</sup>	LPC Peripheral
Serial Port 1	8 Ranges in 64KB I/O Space	8	LPC Peripheral
Serial Port 2	8 Ranges in 64KB I/O Space	8	LPC Peripheral
Floppy Disk Controller	2 Ranges in 64KB I/O Space	8	LPC Peripheral
LAN	Anywhere in 64KB I/O Space	32 <sup>2</sup>	LAN Unit
LPC Generic 1	Anywhere in 64KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 2	Anywhere in 64KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 3	Anywhere in 64KB I/O Space	4 to 256	LPC Peripheral
LPC Generic 4	Anywhere in 64KB I/O Space	4 to 256	LPC Peripheral
I/O Trapping Ranges	Anywhere in 64KB I/O Space	1 to 256	Trap on Backbone
PCI Bridge	Anywhere in 64KB I/O Space	I/O Base/Limit	PCI Bridge
PCI Express* Root Ports	Anywhere in 64KB I/O Space	I/O Base/Limit	PCI Express* Root Ports 1-8
KT	Anywhere in 64KB I/O Space	8	KT

**NOTES:**

1. All ranges are decoded directly from DMI. The I/O cycles will not be seen on PCI, except the range associated with PCI bridge.
2. The LAN range is typically not used, as the registers can also be accessed by means of a memory space.
3. There is also an alias 400h above the parallel port range that is used for ECP parallel ports.

## 7.4 Memory Map

Table 7-4 shows (from the processor perspective) the memory ranges that the PCH decodes. Cycles that arrive from processor that are not directed to any of the internal memory targets that decode directly from processor will be driven out on PCIe\*, unless the Subtractive Decode Policy bit is set (D31:F0:Offset 42h, bit 0).

PCI cycles generated by external PCI masters will be positively decoded, unless they fall in the PCI-to-PCI bridge memory forwarding ranges (those addresses are reserved for PCI peer-to-peer traffic). If the cycle is not in the internal LAN controller's range, it will be forwarded up to DMI. Software must not attempt locks to the PCH memory-mapped I/O ranges for EHCI and HPET. If attempted, the lock is not honored, which means potential deadlock conditions may occur.

**Table 7-4. Memory Decode Ranges from Processor Perspective (Sheet 1 of 2)**

Memory Range	Target	Dependency/Comments
0000 0000h-000D FFFFh 0010 0000h-TOM (Top of Memory)	Main Memory	TOM registers in Host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS Decode Enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS Decode Enable register is set
FEC_ _000h-FEC_ _040h	I/O(x) APIC inside PCH	FEC " " is controlled using APIC Range Select (ASEL) field and APIC Enable (AEN) bit
FEC1 0000h-FEC1 7FFF	PCI Express* Port 1	PCI Express* Root Port 1 I/OxAPIC Enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI Express* Port 2	PCI Express* Root Port 2 I/OxAPIC Enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI Express* Port 3	PCI Express* Root Port 3 I/OxAPIC Enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI Express* Port 4	PCI Express* Root Port 4 I/OxAPIC Enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI Express* Port 5	PCI Express* Root Port 5 I/OxAPIC Enable (PAE) set
FEC3 8000h-FEC3 FFFFh	Reserved	
FEC4 0000h-FEC4 7FFF	Reserved	
FEC4 8000h-FEC4 FFFF	PCI Express* Port 8	PCI Express* Root Port 8 I/OxAPIC Enable (PAE) set
FFC0 0000h-FFC7 FFFFh FF80 0000h-FF87 FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 8 in BIOS Decode Enable register is set
FFC8 0000h-FFCF FFFFh FF88 0000h-FF8F FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 9 in BIOS Decode Enable register is set
FFD0 0000h-FFD7 FFFFh FF90 0000h-FF97 FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 10 in BIOS Decode Enable register is set
FFD8 0000h-FFDF FFFFh FF98 0000h-FF9F FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 11 in BIOS Decode Enable register is set
FFE0 000h-FFE7 FFFFh FFA0 0000h-FFA7 FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 12 in BIOS Decode Enable register is set
FFE8 0000h-FFEF FFFFh FFA8 0000h-FFAF FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 13 in BIOS Decode Enable register is set
FFF0 0000h-FFF7 FFFFh FFB0 0000h-FFB7 FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 14 in BIOS Decode Enable register is set
FFF8 0000h-FFFF FFFFh FFB8 0000h-FFBF FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Always enabled. The top two 64KB blocks of this range can be swapped, as described in Section 7.4.1.
FF70 0000h-FF7F FFFFh FF30 0000h-FF3F FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 3 in BIOS Decode Enable register is set
FF60 0000h-FF6F FFFFh FF20 0000h-FF2F FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 2 in BIOS Decode Enable register is set

**Table 7-4. Memory Decode Ranges from Processor Perspective (Sheet 2 of 2)**

Memory Range	Target	Dependency/Comments
FF50 0000h-FF5F FFFFh FF10 0000h-FF1F FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 1 in BIOS Decode Enable register is set
FF40 0000h-FF4F FFFFh FF00 0000h-FF0F FFFFh	LPC or SPI (or PCI) <sup>2</sup>	Bit 0 in BIOS Decode Enable register is set
128KB anywhere in 4GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARA)
4KB anywhere in 4GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARB)
1KB anywhere in 4GB range	USB EHCI Controller #1 <sup>1</sup>	Enable using standard PCI mechanism (D29:F0)
64KB anywhere in 4GB range	USB xHCI Controller	Enable using standard PCI mechanism (D20:F0)
16KB anywhere in 64-bit addressing space	Intel® High Definition Audio Host Controller	Enable using standard PCI mechanism (D27:F0)
FED0 X000h-FED0 X3FFh	High Precision Event Timers <sub>1</sub>	BIOS determines the "fixed" location which is one of four, 1KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
FED4 0000h-FED4 FFFFh	TPM on LPC	None
Memory Base/Limit anywhere in 4GB range	PCI Bridge	Enable by means of standard PCI mechanism (D30:F0)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Bridge	Enable by means of standard PCI mechanism (D30:F0)
64KB anywhere in 4GB range	LPC	LPC Generic Memory Range. Enable by means of setting bit[0] of the LPC Generic Memory Range register (D31:F0:offset 98h).
32 Bytes anywhere in 64-bit address range	SMBus	Enable by means of standard PCI mechanism (D31:F3)
2KB anywhere above 64KB to 4GB range	SATA Host Controller #1	AHCI memory-mapped registers. Enable by means of standard PCI mechanism (D31:F2)
Memory Base/Limit anywhere in 4GB range	PCI Express® Root Ports 1-6	Enable by means of standard PCI mechanism (D28: F 0-5)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Express® Root Ports 1-6	Enable by means of standard PCI mechanism (D28:F 0-5)
4KB anywhere in 64-bit address range	Thermal Reporting	Enable by means of standard PCI mechanism (D31:F6 TBAR/TBARTH)
4KB anywhere in 64-bit address range	Thermal Reporting	Enable by means of standard PCI mechanism (D31:F6 TBARB/TBARBH)
16 Bytes anywhere in 64-bit address range	Intel® MEI #1, #2	Enable by means of standard PCI mechanism (D22:F 1:0)
4KB anywhere in 4GB range	KT	Enable by means of standard PCI mechanism (D22:F3)
16KB anywhere in 4GB range	Root Complex Register Block (RCRB)	Enable by means of setting bit[0] of the Root Complex Base Address register (D31:F0:offset F0h).
16KB anywhere in 4GB range	LPSS Controllers	Enable by means of standard PCI mechanism (D21:F0 - 6, D23: F0).
1MB anywhere in 4GB range	Intel® SST Controller	Enable by means of setting bit[0] of the Root Complex Base Address register (D31:F0:offset F0h).

**NOTES:**

1. Software must not attempt locks to memory mapped I/O ranges for USB EHCI or High Precision Event Timers. If attempted, the lock is not honored, which means potential deadlock conditions may occur.
2. PCI is the target when the Boot BIOS Destination selection bits are set to 10b (Chipset Configuration Registers:Offset 3401 bits 11:10). When PCI is selected, the Firmware Hub Decode Enable bits have no effect.

## 7.4.1 Boot-Block Update Scheme

The PCH supports a “top swap” mode that has the PCH swap the top block in the FWH or SPI flash (the boot-block) with another location. This allows for safe update of the boot-block (even if a power failure occurs). When the “Top Swap” Enable bit is set, the PCH will invert A16 for cycles going to the upper two 64KB blocks in the FWH or appropriate address lines as selected in Top Swap Block size soft strap for SPI.

Specifically for FHW, in this mode accesses to FFFF\_0000h–FFFF\_FFFFh are directed to FFFE\_0000h–FFFE\_FFFFh and vice versa. When the Top Swap Enable bit is 0, the PCH will not invert A16.

Specifically for SPI, in this mode the “Top Swap” behavior is as described below. When the Top Swap Enable bit is 0, the PCH will not invert any address bit.

**Table 7-5. SPI Mode Address Swapping**

Top Swap Block Size Value	Accesses To	Being Directed To
000 (64KB)	FFFF_0000h–FFFF_FFFFh	FFFE_0000h–FFFE_FFFFh and vice versa
001 (128KB)	FFFE_0000h–FFFE_FFFFh	FFFC_0000h–FFFD_FFFFh and vice versa
010 (256KB)	FFFC_0000h–FFFE_FFFFh	FFF8_0000h–FFF9_FFFFh and vice versa
011–111	Reserved	Reserved

This bit is automatically set to 0 by RTCRST#, but not by PLTRST#.

The scheme is based on the concept that the top block is reserved as the “boot” block, and the block immediately below the top block is reserved for doing boot-block updates.

The algorithm is:

1. Software copies the top block to the block immediately below the top
2. Software checks that the copied block is correct. This could be done by performing a checksum calculation.
3. Software sets the Top Swap bit. This will invert the appropriate address bits for the cycles going to the FWH or SPI.
4. Software erases the top block.
5. Software writes the new top block.
6. Software checks the new top block.
7. Software clears the Top Swap bit.

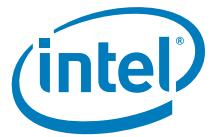
If a power failure occurs at any point after step 3, the system will be able to boot from the copy of the boot-block that is stored in the block below the top. This is because the Top Swap bit is backed in the RTC well.

**Note:** The top-block swap mode may be forced by an external strapping option (See [Section 2.27](#)). When top-block swap mode is forced in this manner, the Top Swap bit cannot be cleared by software. A re-boot with the strap removed will be required to exit a forced top-block swap mode.

**Note:** Top swap mode only affects accesses to the Firmware Hub space, not feature space for FWH.

**Note:** The top swap mode has no effect on accesses below FFFE\_0000h for FWH.

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# 8 Chipset Configuration Registers

This section describes all registers and base functionality that is related to Chipset configuration and not a specific interface (such as LPC, USB, or PCI Express\*). It contains the root complex register block that describes the behavior of the upstream internal link.

This block is mapped into memory space, using the Root Complex Base Address (RCBA) register of the PCI-to-LPC bridge. Accesses in this space must be limited to 32-bit (DWord) quantities. Burst accesses are not allowed.

- All Chipset Configuration registers are located in the core well, unless otherwise indicated.

## 8.1 Chipset Configuration Registers (Memory Space)

**Note:** Address locations that are not shown should be treated as Reserved (see [Chapter 7](#) for details).

**Table 8-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
0400h-0403	RPC	Root Port Configuration	0000000yh	R/W, RO
0404h-0407h	RPFN	Root Port Function Number and Hide for PCI Express* Root Ports	76543210h	R/WO, RO
1E00h-1E03h	TRSR	Trap Status	00000000h	R/WC, RO
1E10h-1E17h	TRCR	Trapped Cycle	0000000000000000h	RO
1E18h-1E1Fh	TWDR	Trapped Write Data	0000000000000000h	RO
1E80h-1E87h	IOTR0	I/O Trap Register 0	0000000000000000h	R/W
1E88h-1E8Fh	IOTR1	I/O Trap Register 1	0000000000000000h	R/W
1E90h-1E97h	IOTR2	I/O Trap Register 2	0000000000000000h	R/W
1E98h-1E9Fh	IOTR3	I/O Trap Register 3	0000000000000000h	R/W
2014h-2017h	V0CTL	Virtual Channel 0 Resource Control	80000010h	R/WL, RO
201Ah-201Bh	V0STS	Virtual Channel 0 Resource Status	0000h	RO
2020h-2023h	V1CTL	Virtual Channel 1 Resource Control	00000000h	R/W, RO, R/WL
2026h-2027h	V1STS	Virtual Channel 1 Resource Status	0000h	RO
20ACh-20AFh	REC	Root Error Command	0000h	R/W
2234h-2327h	DMIC	DMI Control	00000000h	R/W, RO
3000h-3001h	TCTL	TCO Configuration	00h	R/W, RO
3100h-3103h	D31IP	Device 31 Interrupt Pin	03243200h	R/W, RO
3108h-310Bh	D29IP	Device 29 Interrupt Pin	10004321h	R/W, RO
310Ch-310Fh	D28IP	Device 28 Interrupt Pin	00214321h	R/W, RO
3110h-3113h	D27IP	Device 27 Interrupt Pin	00000001h	R/W, RO
3118h-311Bh	D25IP	Device 25 Interrupt Pin	00000001h	R/W, RO
3124h-3127h	D22IP	Device 22 Interrupt Pin	00004321h	R/W, RO

**Table 8-1. Chipset Configuration Register Memory Map (Memory Space) (Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
3128h-312Bh	D20IP	Device 20 Interrupt Pin	00000021h	R/W, RO
3140h-3141h	D31IR	Device 31 Interrupt Route	3210h	R/W, RO
3144h-3145h	D29IR	Device 29 Interrupt Route	3210h	R/W, RO
3146h-3147h	D28IR	Device 28 Interrupt Route	3210h	R/W, RO
3148h-3149h	D27IR	Device 27 Interrupt Route	3210h	R/W, RO
3150h-3151h	D25IR	Device 25 Interrupt Route	3210h	R/W, RO
3158h-315Bh	D23IR	Device 23 Interrupt Route	00000000h	R/W, RO
315Ch-315Dh	D22IR	Device 22 Interrupt Route	3210h	R/W, RO
3160h-3161h	D20IR	Device 20 Interrupt Route	3210h	R/W, RO
3164h-3167h	D21IR	Device 21 Interrupt Route	00003210h	R/W, RO
3168h-316Bh	D19IR	Device 19 Interrupt Route	00000000h	R/W, RO
31E0h-31E3h	ACPIIRQEN	ACPI IRQ Enable	00000000h	R/W, RO
31FEh-31FFh	OIC	Other Interrupt Control	0000h	R/W, RO
3300h-3303h	WADT_AC	Wake Alarm Device Timer: AC	FFFFFFFh	R/W
3304h-3307h	WADT_DC	Wake Alarm Device Timer: DC	FFFFFFFh	R/W
3308h-330Bh	WADT_EXP_AC	Wake Alarm Device Expired Timer: AC	FFFFFFFh	R/W
330Ch-330Fh	WADT_EXP_DC	Wake Alarm Device Expired Timer: DC	FFFFFFFh	R/W
3310h-3313h	PRSTS	Power and Reset Status	05000000h	RO, R/WC
3318h-331Bh	PM_CFG	Power Management Configuration	00000000h	R/W, RO
3328h-332Bh	DEEP_S3_POL	Deep Sx From S3 Power Policies	00000000h	R/W, RO
332Ch-332Fh	DEEP_S4_POL	Deep Sx From S4 Power Policies	00000000h	R/W, RO
3330h-3333h	DEEP_S5_POL	Deep Sx From S5 Power Policies	00000000h	R/W, RO
3334-3337h	DSX_CFG	Deep Sx Configuration	00000000h	R/W, RO
33C8h-33CBh	PMSYNC_CFG	PMSYNC Configuration	00000000h	R/W, RO
33FCh	ACPI_TMR_CTL	ACPI Timer Control	00h	RO, R/W, R/WS, RO
3400h-3403h	RC	RTC Configuration	00000000h	R/W, R/WLO, RO
3404h-3407h	HPTC	High Precision Timer Configuration	00000000h	R/W
3410h-3413h	GCS	General Control and Status	00000yy4h	R/W, R/WLO, RO
3414h-3414h	BUC	Backed Up Control	0000000xb	R/W, RO
3418h-341Bh	FD	Function Disable	00000000h	R/W, RO
341Ch-341Fh	CG	Clock Gating	00000000h	R/W, RO
3420h-3420h	FDSW	Function Disable SUS Well	00h	R/W, RO
3424h-3425h	DISPBDF	Display Bus, Device and Function Initialization	0010h	R/W, RO
3428h-342Bh	FD2	Function Disable 2	00000000h	R/W, RO
3434-3435h	PRCSUS	Power Reduction Control SUS Well	0000h	R/W, RO

### 8.1.1 RPC—Root Port Configuration Register

Offset Address: 0400–0403h Attribute: R/W, RO  
 Default Value: 0000000yh (y = 00xxb) Size: 32 bits

Bit	Description
31:12	Reserved
11	<b>GbE Over PCIe* Root Port Enable (GBEPCIERPEN)</b> —R/W. 0 = GbE MAC/PHY communication is not enabled over PCI Express*. 1 = The PCI Express* port selected by the GBEPCIEPORTSEL register will be used for GbE MAC/PHY over PCI Express* communication The default value for this bit is set by the GBE_PCIE_EN soft strap. <b>Note:</b> GbE and PCIe* will use the output of this register bit and not the soft strap.
10:8	<b>GbE Over PCIe* Root Port Select (GBEPCIERPSEL)</b> —R/W. If the GBEPCIERPEN is a '1', then this field determines which port is used for GbE MAC/PHY communication over PCI Express*. This register field is set by soft strap and is writable to support separate PHY on motherboard and docking station. 111 = Port 8 (Lane 7) 110 = Port 7 (Lane 6) 101 = Port 6 (Lane 5) 100 = Port 5 (Lane 4) 011 = Port 4 (Lane 3) 010 = Port 3 (Lane 2) 001 = Port 2 (Lane 1) 000 = Port 1 (Lane 0) The default value for this field is set by the GBE_PCIEPORTSEL[2:0] soft strap. <b>Note:</b> GbE and PCIe* will use the output of this field and not the soft strap.
7:4	Reserved
3:2	<b>Port Configuration2 (PC2)</b> —RO. This controls how the PCI bridges are organized in various modes of operation for Ports 5–8. For the following mappings, if a port is not shown, it is considered a x1 port with no connection. This bit is set by the PCIEPCS2[1:0] soft strap. 11 = 1 x4, Port 5 (x4) 10 = 2 x2, Port 5 (x2), Port 7 (x2) 01 = 1x2 and 2x1s, Port 5 (x2), Port 7 (x1) and Port 8(x1) 00 = 4 x1s, Port 5 (x1), Port 6 (x1), Port 7 (x1) and Port 8 (x1)
1:0	<b>Port Configuration (PC)</b> —RO. This controls how the PCI bridges are organized in various modes of operation for Ports 1–4. For the following mappings, if a port is not shown, it is considered a x1 port with no connection. These bits are set by the PCIEPCS1[1:0] soft strap. 11 = 1 x4, Port 1 (x4) 10 = 2 x2, Port 1 (x2), Port 3 (x2) 01 = 1x2 and 2x1s, Port 1 (x2), Port 3 (x1) and Port 4 (x1) 00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1) and Port 4 (x1)

### 8.1.2

### RPFN—Root Port Function Number and Hide for PCI Express\* Root Ports Register

Offset Address: 0404-0407h  
Default Value: 76543210h

Attribute: R/W, R/WO  
Size: 32 bits

For the PCI Express\* root ports, the assignment of a function number to a root port is not fixed. BIOS may re-assign the function numbers on a port-by-port basis. This capability will allow BIOS to disable/hide any root port and still have Functions 0 thru N-1, where N is the total number of enabled root ports.

Port numbers will remain fixed to a physical root port.

The existing root port Function Disable registers operate on physical ports (not functions).

Port Configuration (1x4, 4x1, and so on) is not affected by the logical Function number assignment and is associated with physical ports.

**Note:**

The difference between hiding versus disabling a port is that a hidden port is not able to claim downstream Configuration cycles **only**. Memory and I/O cycles are still claimed by that hidden port. A disabled port is turned off and not able to claim downstream Configuration, Memory, and I/O cycles—it saves power. For PCIe\* ports that are multiplexed out through Flexible I/O (so the alternative I/O technology, USB 3.0 or SATA, is chosen), the PCIe\* port is disabled (not hidden). Function disable is covered in [Section 8.1.52](#).

Bit	Description
31:24	Reserved
23	<b>Root Port 6 Configuration Hide (RP6CH)</b> —R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to 1, the root port will not claim any downstream configuration transactions.
22:20	<b>Root Port 6 Function Number (RP6FN)</b> —R/WO. These bits set the function number for PCI Express* Root Port 6. This root port function number must be a unique value from the other root port function numbers.
19	<b>Root Port 5 Configuration Hide (RP5CH)</b> —R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to 1, the root port will not claim any downstream configuration transactions.
18:16	<b>Root Port 5 Function Number (RP5FN)</b> —R/WO. These bits set the function number for PCI Express* Root Port 5. This root port function number must be a unique value from the other root port function numbers.
15	<b>Root Port 4 Configuration Hide (RP4CH)</b> —R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to 1, the root port will not claim any downstream configuration transactions.
14:12	<b>Root Port 4 Function Number (RP4FN)</b> —R/WO. These bits set the function number for PCI Express* Root Port 4. This root port function number must be a unique value from the other root port function numbers.
11	<b>Root Port 3 Configuration Hide (RP3CH)</b> —R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to 1, the root port will not claim any downstream configuration transactions.
10:8	<b>Root Port 3 Function Number (RP3FN)</b> —R/WO. These bits set the function number for PCI Express* Root Port 3. This root port function number must be a unique value from the other root port function numbers.
7	<b>Root Port 2 Configuration Hide (RP2CH)</b> —R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to 1, the root port will not claim any downstream configuration transactions.

Bit	Description
6:4	<b>Root Port 2 Function Number (RP2FN)</b> —R/W. These bits set the function number for PCI Express* Root Port 2. This root port function number must be a unique value from the other root port function numbers.
3	<b>Root Port 1 Configuration Hide (RP1CH)</b> —R/W. This bit is used to hide the root port and any devices behind it from being discovered by the operating system. When set to 1, the root port will not claim any downstream configuration transactions.
2:0	<b>Root Port 1 Function Number (RP1FN)</b> —R/W. These bits set the function number for PCI Express* Root Port 1. This root port function number must be a unique value from the other root port function numbers.

### 8.1.3 UPDCR—Upstream Peer Decode Configuration Register

Offset Address: 1014–1017h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Each of the bits represents an upstream requesting channel. When set, it indicates that the requesting channel is capable of peer requests, in such a way that the backbone is required to perform peer decode to determine the target of the transaction. When cleared, it indicates that the requesting channel is only capable of issuing upstream requests.

Bit	Description
31:6	Reserved
5	<b>PCI Express* Root Port C (6) CHID0 Peer Decode Enable (RPCPDE0)</b> —R/W.
4	<b>PCI Express* Root Port B (5) CHID0 Peer Decode Enable (RPBPDE0)</b> —R/W.
3	<b>PCI Express* Root Port A (1-4) CHID3 Peer Decode Enable (RPAPDE3)</b> —R/W.
2	<b>PCI Express* Root Port A (1-4) CHID2 Peer Decode Enable (RPAPDE2)</b> —R/W.
1	<b>PCI Express* Root Port A (1-4) CHID1 Peer Decode Enable (RPAPDE1)</b> —R/W.
0	<b>PCI Express* Root Port A (1-4) CHID0 Peer Decode Enable (RPAPDE0)</b> —R/W.

### 8.1.4 BSPR—Backbone Scratch Pad Register 1104

Offset Address: 1104–1107h      Attribute: RO  
 Default Value: See below      Size: 32 bits

Bit	Description
31:10	Reserved
9	<b>Backbone Peer Posted Disable (BPPD)</b> —RO. When set backbone will not allow any peer posted cycles regardless of the Upstream Peer Decode Configuration (UPD) settings.  <b>Note:</b> Default value is based on PCHSTRP9.BPPD soft strap.
8	<b>Backbone Peer Non-Posted Disable (BPNPD)</b> —RO. When set backbone will not allow any peer non-posted cycles regardless of the Upstream Peer Decode Configuration (UPD) settings.  <b>Note:</b> Default value is based on PCHSTRP9.BPNPD soft strap.
7:0	Reserved

## 8.1.5 TRSR—Trap Status Register

Offset Address: 1E00–1E03h      Attribute: R/WC, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:4	Reserved
3:0	<p><b>Cycle Trap SMI# Status (CTSS)</b>—R/WC. These bits are set by hardware when the corresponding Cycle Trap register is enabled and a matching cycle is received (and trapped). These bits are OR'ed together to create a single status bit in the Power Management register space.</p> <p><b>Note:</b> SMI# and trapping must be enabled in order to set these bits. These bits are set before the completion is generated for the trapped cycle; thereby, ensuring that the processor can enter the SMI# handler when the instruction completes. Each status bit is cleared by writing a 1 to the corresponding bit location in this field.</p>

## 8.1.6 TRCR—Trapped Cycle Register

Offset Address: 1E10–1E17h      Attribute: RO  
 Default Value: 0000000000000000h      Size: 64 bits

This register saves information about the I/O Cycle that was trapped and generated the SMI# for software to read.

Bit	Description
63:25	Reserved
24	<p><b>Read/Write# (RWI)</b>—RO.            0 = Trapped cycle was a write cycle.            1 = Trapped cycle was a read cycle.</p>
23:20	Reserved
19:16	<p><b>Active-high Byte Enables (AHBE)</b>—RO. This is the DWord-aligned byte enables associated with the trapped cycle. A (one) 1 in any bit location indicates that the corresponding byte is enabled in the cycle.</p>
15:2	<p><b>Trapped I/O Address (TIOA)</b>—RO. This is the DWord-aligned address of the trapped cycle.</p>
1:0	Reserved

## 8.1.7 TWDR—Trapped Write Data Register

Offset Address: 1E18–1E1Fh      Attribute: RO  
 Default Value: 0000000000000000h      Size: 64 bits

This register saves the data from I/O write cycles that are trapped for software to read.

Bit	Description
63:32	Reserved
31:0	<p><b>Trapped I/O Data (TIOD)</b>—RO. DWord of I/O write data. This field is undefined after trapping a read cycle.</p>

### 8.1.8 IOTRn—I/O Trap Register (0-3)

Offset Address:	1E80–1E87h Register 0 1E88–1E8Fh Register 1 1E90–1E97h Register 2 1E98–1E9Fh Register 3	Attribute:	R/W, RO
Default Value:	0000000000000000h	Size:	64 bits

These registers are used to specify the set of I/O cycles to be trapped and to enable this functionality.

Bit	Description
63:50	Reserved
49	<b>Read/Write Mask (RWM)</b> —R/W. 0 = The cycle must match the type specified in bit 48. 1 = Trapping logic will operate on both read and write cycles.
48	<b>Read/Write# (RWIO)</b> —R/W. 0 = Write 1 = Read <b>Note:</b> The value in this field does not matter if bit 49 is set.
47:40	Reserved
39:36	<b>Byte Enable Mask (BEM)</b> —R/W. A (one) 1 in any bit position indicates that any value in the corresponding byte enable bit in a received cycle will be treated as a match. The corresponding bit in the Byte Enables field, below, is ignored.
35:32	<b>Byte Enables (TBE)</b> —R/W. Active-high DWord-aligned byte enables.
31:24	Reserved
23:18	<b>Address[7:2] Mask (ADMA)</b> —R/W. A (one) 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for traps on address ranges up to 256 bytes in size.
17:16	Reserved
15:2	<b>I/O Address[15:2] (IOAD)</b> —R/W. DWord-aligned address
1	Reserved
0	<b>Trap and SMI# Enable (TRSE)</b> —R/W. 0 = Trapping and SMI# logic disabled. 1 = The trapping logic specified in this bit is enabled.

### 8.1.9 V0CTL—Virtual Channel 0 Resource Control Register

Offset Address: 2014–2017h  
 Default Value: 80000010h

Attribute: R/WL, RO  
 Size: 32 bits

Bit	Description
31	<b>Virtual Channel Enable (EN)</b> —RO. Always set to 1. VC0 is always enabled and cannot be disabled.
30:27	Reserved
26:24	<b>Virtual Channel Identifier (ID)</b> —RO. Indicates the ID to use for this virtual channel.
23:16	Reserved
15:10	<b>Extended TC/VC Map (ETVM)</b> —R/WL. Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express* reserved TC[3] traffic class bit. These bits are locked if the TCLOCKDN bit (RCBA+0050h:bit 31) is set.
9:7	Reserved
6:1	<b>Transaction Class/Virtual Channel Map (TVM)</b> —R/WL. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. These bits are locked if the TCLOCKDN bit (RCBA+0050h:bit 31) is set.
0	Reserved

### 8.1.10 V0STS—Virtual Channel 0 Resource Status Register

Offset Address: 201A–201Bh  
 Default Value: 0000h

Attribute: RO  
 Size: 16 bits

Bit	Description
15:2	Reserved
1	<b>VC Negotiation Pending (NP)</b> —RO. When set, this bit indicates the virtual channel is still being negotiated with ingress ports.
0	Reserved

### 8.1.11 V1CTL—Virtual Channel 1 Resource Control Register

Offset Address: 2020–2023h  
 Default Value: 00000000h

Attribute: R/W, R/WL, RO  
 Size: 32 bits

Bit	Description
31	<b>Virtual Channel Enable (EN)</b> —R/W. Enables the VC when set. Disables the VC when cleared.
30:28	Reserved
27:24	<b>Virtual Channel Identifier (ID)</b> —R/W. Indicates the ID to use for this virtual channel.
23:16	Reserved
15:10	<b>Extended TC/VC Map (ETVM)</b> —R/WL. Defines the upper 8-bits of the VC0 16-bit TC/VC mapping registers. These registers use the PCI Express* reserved TC[3] traffic class bit. These bits are locked if the TCLOCKDN bit (RCBA+0050h:bit 31) is set.
9:8	Reserved
7:1	<b>Transaction Class/Virtual Channel Map (TVM)</b> —R/WL. Indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel. These bits are locked if the TCLOCKDN bit (RCBA+0050h:bit 31) is set.
0	Reserved

### 8.1.12 V1STS—Virtual Channel 1 Resource Status Register

Offset Address: 2026–2027h      Attribute: RO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:2	Reserved
1	<b>VC Negotiation Pending (NP)</b> —RO. When set, this bit indicates the virtual channel is still being negotiated with ingress ports.
0	Reserved

### 8.1.13 REC—Root Error Command Register

Offset Address: 20AC–20AFh      Attribute: R/W, RO  
 Default Value: 0000h      Size: 32 bits

Bit	Description
31	<b>Drop Poisoned Downstream Packets (DPDP)</b> —R/W. This bit determines how downstream packets on DMI are handled that are received with the EP field set, indicating poisoned data: 0 = Packets are forwarded downstream without forcing the UT field set. 1 = This packet and all subsequent packets with data received on DMI for any VC will have their Unsupported Transaction (UT) field set causing them to master Abort downstream. Packets without data (such as memory, I/O, and Configuration read requests) are allowed to proceed.
30:0	Reserved

### 8.1.14 DMIC—DMI Control Register

Offset Address: 2234–2237h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>DMI Clock Gate Enable (DMICGEN)</b> —R/W. BIOS must program this field to 1b.

### 8.1.15 DMC—DMI Miscellaneous Control Register

Offset Address: 2304–2307h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>DMC Field 1</b> —R/W. BIOS must program this field to F88400h.

### 8.1.16 TCTL—TCO Configuration Register

Offset Address: 3000–3001h  
Default Value: 00h

Attribute: R/W, RO  
Size: 8 bits

Bit	Description
7	<b>TCO IRQ Enable (IE)</b> —R/W 0 = TCO IRQ is disabled. 1 = TCO IRQ is enabled, as selected by the TCO_IRQ_SEL field.
6:3	Reserved
2:0	<b>TCO IRQ Select (IS)</b> —R/W. Specifies on which IRQ the TCO will internally appear. If not using the APIC, the TCO interrupt must be routed to IRQ9–11, and that interrupt is not sharable with the SERIRQ stream, but is shareable with other PCI interrupts. If using the APIC, the TCO interrupt can also be mapped to IRQ20–23, and can be shared with other interrupt. 000 = IRQ 9 001 = IRQ 10 010 = IRQ 11 011 = Reserved 100 = IRQ 20 (only if APIC enabled) 101 = IRQ 21 (only if APIC enabled) 110 = IRQ 22 (only if APIC enabled) 111 = IRQ 23 (only if APIC enabled) When setting the these bits, the IE bit should be cleared to prevent glitching. When the interrupt is mapped to APIC interrupts 9, 10, or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.

### 8.1.17 D31IP—Device 31 Interrupt Pin Register

Offset Address: 3100–3103h  
 Default Value: 03243200h

Attribute: R/W, RO  
 Size: 32 bits

Bit	Description
31:28	Reserved
27:24	<b>Thermal Sensor Pin (TSIP)</b> —R/W. Indicates which pin the Thermal Sensor controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
23:20	<b>SATA Pin 2 (SIP2)</b> —R/W. Indicates which pin the SATA controller 2 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
19:16	Reserved
15:12	<b>SMBus Pin (SMP)</b> —R/W. Indicates which pin the SMBus controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
11:8	<b>SATA Pin (SIP)</b> —R/W. Indicates which pin the SATA controller drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–Fh = Reserved
7:4	Reserved
3:0	LPC Bridge Pin (LIP)—RO. Currently, the LPC bridge does not generate an interrupt, so this field is read-only and 0.

### 8.1.18 D29IP—Device 29 Interrupt Pin Register

Offset Address: 3108–310Bh  
 Default Value: 10004321h

Attribute: R/W, RO  
 Size: 32 bits

Bit	Description
31:4	Reserved
3:0	<b>EHCI #1 Pin (E1P)</b> —R/W. Indicates which pin the EHCI controller #1 drives as its interrupt, if controller exists. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–7h = Reserved

**Note:** EHCI Controller #1 is mapped to Device 29 Function 0.

### 8.1.19 D28IP—Device 28 Interrupt Pin Register

Offset Address: 310C–310Fh  
 Default Value: 00214321h

Attribute: R/W, RO  
 Size: 32 bits

Bit	Description
31:28	<b>PCI Express* #8 Pin (P8IP)</b> —R/W. Indicates which pin the PCI Express* port #8 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–7h = Reserved
27:24	<b>PCI Express* #7 Pin (P7IP)</b> —R/W. Indicates which pin the PCI Express* port #7 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–7h = Reserved
23:20	<b>PCI Express* #6 Pin (P6IP)</b> —R/W. Indicates which pin the PCI Express* port #6 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h–7h = Reserved
19:16	<b>PCI Express* #5 Pin (P5IP)</b> —R/W. Indicates which pin the PCI Express* port #5 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–7h = Reserved

Bit	Description
15:12	<b>PCI Express* #4 Pin (P4IP)</b> —R/W. Indicates which pin the PCI Express* port #4 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# (Default) 5h-7h = Reserved
11:8	<b>PCI Express* #3 Pin (P3IP)</b> —R/W. Indicates which pin the PCI Express* port #3 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# 3h = INTC# (Default) 4h = INTD# 5h-7h = Reserved
7:4	<b>PCI Express* #2 Pin (P2IP)</b> —R/W. Indicates which pin the PCI Express* port #2 drives as its interrupt. 0h = No interrupt 1h = INTA# 2h = INTB# (Default) 3h = INTC# 4h = INTD# 5h-7h = Reserved
3:0	<b>PCI Express* #1 Pin (P1IP)</b> —R/W. Indicates which pin the PCI Express* port #1 drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-7h = Reserved

### 8.1.20 D27IP—Device 27 Interrupt Pin Register

Offset Address: 3110–3113h      Attribute: R/W, RO  
 Default Value: 00000001h      Size: 32 bits

Bit	Description
31:4	Reserved
3:0	<b>Intel® High Definition Audio Pin (ZIP)</b> —R/W. Indicates which pin the Intel® High Definition Audio controller drives as its interrupt. 0h = No interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h-Fh = Reserved

### 8.1.21 D25IP—Device 25 Interrupt Pin Register

Offset Address: 3118–311Bh      Attribute: R/W, RO  
 Default Value: 00000001h      Size: 32 bits

Bit	Description
31:4	Reserved
3:0	<b>GbE LAN Pin (LIP)</b> —R/W. Indicates which pin the internal GbE LAN controller drives as its interrupt. 0h = No Interrupt 1h = INTA# (Default) 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved

### 8.1.22 D22IP—Device 22 Interrupt Pin Register

Offset Address: 3124–3127h      Attribute: R/W, RO  
 Default Value: 00004321h      Size: 32 bits

Bit	Description
31:16	Reserved
15:12	<b>KT Pin (KTIP)</b> —R/W. Indicates which pin the Keyboard text PCI functionality drives as its interrupt. 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved
11:8	<b>IDE-R Pin (IDERIP)</b> —R/W. Indicates which pin the IDE Redirect PCI functionality drives as its interrupt. 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved
7:4	<b>Intel® MEI #2 Pin (MEI2IP)</b> —R/W. Indicates which pin the Intel® Management Engine Interface #2 drives as its interrupt. 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved
3:0	<b>Intel® MEI #1 Pin (MEI1IP)</b> —R/W. Indicates which pin the Intel® Management Engine Interface controller #1 drives as its interrupt. 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved

### 8.1.23 D20IP—Device 20 Interrupt Pin Register

Offset Address: 3128–312bh Attribute: R/W, RO  
 Default Value: 00000021h Size: 32 bits

Bit	Description
31:4	Reserved
3:0	<b>xHCI Pin (xHCIIP)</b> —R/W. Indicates which pin the xHCI drives as its interrupt. 0h = No Interrupt 1h = INTA# 2h = INTB# 3h = INTC# 4h = INTD# 5h–Fh = Reserved

### 8.1.24 D31IR—Device 31 Interrupt Route Register

Offset Address: 3140–3141h Attribute: R/W, RO  
 Default Value: 3210h Size: 16 bits

Bit	Description
15	Reserved
14:12	<b>Interrupt D Pin Route (IDR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	<b>Interrupt C Pin Route (ICR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	<b>Interrupt B Pin Route (IBR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 31 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 31 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.25 D29IR—Device 29 Interrupt Route Register

Offset Address: 3144–3145h  
 Default Value: 3210h

Attribute: R/W, RO  
 Size: 16 bits

Bit	Description
15	Reserved
14:12	<b>Interrupt D Pin Route (IDR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	<b>Interrupt C Pin Route (ICR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	<b>Interrupt B Pin Route (IBR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 29 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 29 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.26 D28IR—Device 28 Interrupt Route Register

Offset Address: 3146–3147h  
 Default Value: 3210h

Attribute: R/W, RO  
 Size: 16 bits

Bit	Description
15	Reserved
14:12	<b>Interrupt D Pin Route (IDR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	<b>Interrupt C Pin Route (ICR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	<b>Interrupt B Pin Route (IBR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 28 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 28 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.27 D27IR—Device 27 Interrupt Route Register

Offset Address: 3148–3149h  
 Default Value: 3210h

Attribute: R/W, RO  
 Size: 16 bits

Bit	Description
15	Reserved
14:12	<b>Interrupt D Pin Route (IDR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	<b>Interrupt C Pin Route (ICR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	<b>Interrupt B Pin Route (IBR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 27 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 27 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.28 D25IR—Device 25 Interrupt Route Register

Offset Address: 3150-3151h  
 Default Value: 3210h

Attribute: R/W, RO  
 Size: 16 bits

Bit	Description
15	Reserved
14:12	<b>Interrupt D Pin Route (IDR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 25 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	<b>Interrupt C Pin Route (ICR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 25 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	<b>Interrupt B Pin Route (IBR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 25 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 25 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.29 D23IR—Device 23 Interrupt Route Register

Offset Address: 3158–315Bh  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 23 single function device. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.30 D22IR—Device 22 Interrupt Route Register

Offset Address: 315C-315Dh  
Default Value: 3210h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15	Reserved
14:12	<b>Interrupt D Pin Route (IDR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 22 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	<b>Interrupt C Pin Route (ICR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 22 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	<b>Interrupt B Pin Route (IBR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 22 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 22 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.31 D20IR—Device 20 Interrupt Route Register

Offset Address: 3160–3161h  
 Default Value: 3210h

Attribute: R/W, RO  
 Size: 16 bits

Bit	Description
15	Reserved
14:12	<b>Interrupt D Pin Route (IDR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 20 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	<b>Interrupt C Pin Route (ICR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 20 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	<b>Interrupt B Pin Route (IBR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 20 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 20 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.32 D21IR—Device 21 Interrupt Route Register

Offset Address: 3164–3167h  
 Default Value: 00003210h

Attribute: R/W, RO  
 Size: 32 bits

Bit	Description
31:15	Reserved
14:12	<b>Interrupt D Pin Route (IDR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTD# pin reported for device 21 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# (Default) 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
11	Reserved
10:8	<b>Interrupt C Pin Route (ICR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTC# pin reported for device 21 functions. 0h = PIRQA# 1h = PIRQB# 2h = PIRQC# (Default) 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
7	Reserved
6:4	<b>Interrupt B Pin Route (IBR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTB# pin reported for device 21 functions. 0h = PIRQA# 1h = PIRQB# (Default) 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#
3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 21 functions. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.33 D19IR—Device 19 Interrupt Route Register

Offset Address: 3168–316Bh      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:3	Reserved
2:0	<b>Interrupt A Pin Route (IAR)</b> —R/W. Indicates which physical pin on the PCH is connected to the INTA# pin reported for device 19 single function device. 0h = PIRQA# (Default) 1h = PIRQB# 2h = PIRQC# 3h = PIRQD# 4h = PIRQE# 5h = PIRQF# 6h = PIRQG# 7h = PIRQH#

### 8.1.34 ACPIIRQEN—ACPI IRQ Enable Register

Offset Address: 31E0–31E3h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:14	Reserved
13	<b>ACPI IRQ13 Enable (A13E)</b> —R/W. Same description as bit A3E except this is for IRQ13.
12:8	Reserved
7	<b>ACPI IRQ7 Enable (A7E)</b> —R/W. Same description as bit A3E except this is for IRQ7.
6	<b>ACPI IRQ6 Enable (A6E)</b> —R/W. Same description as bit A3E except this is for IRQ6.
5	<b>ACPI IRQ5 Enable (A5E)</b> —R/W. Same description as bit A3E except this is for IRQ5.
4	<b>ACPI IRQ4 Enable (A4E)</b> —R/W. Same description as bit A3E except this is for IRQ4.
3	<b>ACPI IRQ3 Enable (A3E)</b> —R/W. This bit should be set to indicate there is an ACPI IRQ3 interrupt source. When set, this bit steers the interrupt aware from non-sharable Serial IRQ slot. <b>Note:</b> The ACPI IRQ sources are the Intel Serial I/O Controllers and the Intel Smart Sound Technology.
2:0	Reserved

### 8.1.35 OIC—Other Interrupt Control Register

Offset Address: 31FE-31FFh Attribute: R/W, RO  
 Default Value: 0000h Size: 16 bits

Bit	Description
15:12	Reserved
11	<b>IOAPIC Entry 24-39 Disable (IOA24_39_D)</b> —R/W. When this bit is set to 1, the IOAPIC Entry 24-39 are disabled and the address offsets corresponding to the IOAPIC Entry 24-39 Redirection Table become reserved.  <b>Note:</b> If IOA24_39_D is set to 1, then BIOS shall program IOAPIC index register VER.MRE to a value of $\leq 17h$ . If BIOS programs IOAPIC index register VER.MRE to a value $> 17h$ , then this bit should be left at 0.
10:9	Reserved
8	<b>APIC Enable (AEN)</b> —R/W. 0 = The internal IOxAPIC is disabled. 1 = Enables the internal IOxAPIC and its address decode. <b>Note:</b> Software should read this register after modifying APIC enable bit prior to access to the IOxAPIC address range.
7:0	<b>APIC Range Select (ASEL)</b> —R/W. These bits define address bits 19:12 for the IOxAPIC range. The default value of 00h enables compatibility with prior PCH products as an initial value. This value must not be changed unless the IOxAPIC Enable bit is cleared.

**Note:** FEC1\_0000h-FEC4\_FFFFh is allocated to PCIe\* when I/OxAPIC Enable (PAE) bit is set.

### 8.1.36 WADT\_AC—Wake Alarm Device Timer—AC Register

Offset Address: 3300-3303h Attribute: R/W  
 Default Value: FFFFFFFFh Size: 32 bits

Bit	Description
31:0	<b>Wake Alarm Device Timer Value for AC Mode (WADT_AC_VAL)</b> —R/W. This field contains the 32-bit wake alarm device timer value (1 second granularity) for AC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0: <ul style="list-style-type: none"> <li>If on AC power, GPE0_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0_EN.WADT_EN is 1.</li> <li>If power source is DC at this time, the status bit is not set. However, if AC power subsequently returns to the platform, the AC Expired Timer begins running. Refer to WADT_EXP_AC for more details.</li> <li>The timer returns to its default value of FFFFFFFFh.</li> </ul> <b>Note:</b> This register is on DSW and reset by DPWROK.

### 8.1.37 WADT\_DC—Wake Alarm Device Timer—DC Register

Offset Address: 3304–3307h  
 Default Value: FFFFFFFFh

Attribute: R/W  
 Size: 32 bits

Bit	Description
31:0	<p><b>Wake Alarm Device Timer Value for DC Mode (WADT_DC_VAL)</b>—R/W. This field contains the 32-bit wake alarm device timer value (1 second granularity) for DC power. The timer begins decrementing when written to a value other than FFFFFFFFh (regardless of the power source when the write occurs). Upon counting down to 0:</p> <ul style="list-style-type: none"> <li>• If on DC power, GPE0_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0_EN.WADT_EN is 1.</li> <li>• If power source is AC at this time, the status bit is not set. However, if DC power subsequently returns to the platform, the DC Expired Timer begins running. Refer to WADT_EXP_DC for more details.</li> <li>• The timer returns to its default value of FFFFFFFFh.</li> </ul> <p><b>Note:</b> This register is on DSW and reset by DPWROK.</p>

### 8.1.38 WADT\_EXP\_AC—Wake Alarm Device Expired Timer—AC Register

Offset Address: 3308–330Bh  
 Default Value: FFFFFFFFh

Attribute: R/W  
 Size: 32 bits

Bit	Description
31:0	<p><b>Wake Alarm Device Expired Timer Value for AC Mode (WADT_EXP_AC_VAL)</b>—R/W. This field contains the 32-bit wake alarm device “Expired Timer” value (1 second granularity) for AC power. The timer begins decrementing after switching from DC to AC power, in the case where the WADT_AC timer has already expired while platform was on DC power. This timer only decrements while operating on AC power. So if the power source switches back to DC power, the timer will stop (but not reset). When AC power returns, the timer will again begin decrementing.</p> <p>Upon expiration of this timer:</p> <ul style="list-style-type: none"> <li>• If on AC power, GPE0_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0_EN.WADT_EN is 1.</li> <li>• Both the AC and DC Expired Timers return to their default value of FFFFFFFFh.</li> </ul> <p><b>Note:</b> This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFF.</p> <p><b>Note:</b> This register is on DSW and reset by DPWROK.</p>



### 8.1.39 WADT\_EXP\_DC—Wake Alarm Device Expired Timer—DC Register

Offset Address: 330C–330Fh Attribute: R/W  
Default Value: FFFFFFFFh Size: 32 bits

Bit	Description
31:0	<p><b>Wake Alarm Device Expired Timer Value for DC Mode (WADT_EXP_DC_VAL)</b>—R/W. This field contains the 32-bit wake alarm device “Expired Timer” value (1 second granularity) for DC power. The timer begins decrementing after switching from AC to DC power, in the case where the WADT_DC timer has already expired while platform was on AC power. This timer only decrements while operating on DC power. So if the power source switches back to AC power, the timer will stop (but not reset). When DC power returns, the timer will again begin decrementing.</p> <p>Upon expiration of this timer:</p> <ul style="list-style-type: none"> <li>• If on DC power, GPE0_STS.WADT_STS will be set. This status bit being set will generate a host wake if GPE0_EN.WADT_EN is 1.</li> <li>• Both the AC and DC Expired Timers return to their default value of FFFFFFFFh.</li> </ul> <p><b>Note:</b> This timer will only begin decrementing under the conditions described above if this field has been configured for something other than its default value of FFFFFFFF.</p> <p><b>Note:</b> This register is on DSW and reset by DPWROK.</p>

### 8.1.40 PRSTS—Power and Reset Status Register

Offset Address: 3310–3313h Attribute: R/WC, RO  
Default Value: 05000000h Size: 32 bits

Bit	Description
31:16	Reserved
15	Power Management Watchdog Timer—R/WC. This bit is set when the Power Management watchdog timer causes a global reset.
14:7	Reserved
6	<b>Intel® Management Engine Watchdog Timer Status</b> —R/WC. This bit is set when the Intel® Management Engine watchdog timer causes a global reset.
5	<b>Wake On LAN Override Wake Status (WOL_OVR_WK_STS)</b> —R/WC. This bit gets set when all of the following conditions are met: <ul style="list-style-type: none"> <li>• Integrated LAN Signals a Power Management Event</li> <li>• The system is not in S0</li> <li>• The “WoL Enable Override” bit is set in configuration space.</li> </ul> BIOS can read this status bit to determine this wake source. Software clears this bit by writing a 1 to it.
4	<b>PRSTS Field 1</b> —R/W. BIOS may program this field.
3	<b>Intel® ME Host Power Down (ME_HOST_PWRDN)</b> —R/WC. This bit is set when the Intel® Management Engine generates a host reset with power down.
2	<b>Intel® ME Host Reset Warm Status (ME_HRST_WARM_STS)</b> —R/WC. This bit is set when the Intel® Management Engine generates a Host reset without power cycling. Software clears this bit by writing a 1 to this bit position.
1	<b>Intel® ME Host Reset Cold Status (ME_HRST_COLD_STS)</b> —R/WC. This bit is set when the Intel® Management Engine generates a Host reset with power cycling. Software clears this bit by writing a 1 to this bit position.
0	<b>Intel® ME WAKE STATUS (ME_WAKE_STS)</b> —R/WC. This bit is set when the Intel® Management Engine generates a Non-Maskable wake event, and is not affected by any other enable bit. When this bit is set, the Host Power Management logic wakes to S0.

## 8.1.41 PM\_CFG—Power Management Configuration Register

Offset Address: 3318–331Bh  
 Default Value: 00000020h

Attribute: R/W, R/WL, RO  
 Size: 32 bits

Bit	Description
31:27	Reserved
26:24	<b>PM_CFG Field 1</b> —R/W. BIOS may write to this field.
23	Reserved
22	<b>PM_CFG Field 0</b> —R/W. BIOS may write to this field.
21	<b>RTC Wake from Deep Sx Disable (RTC_DS_WAKE_DIS)</b> —R/W. When set, this bit disables RTC wakes from waking the system from Deep Sx. This bit is reset by RTCRST#.
20	Reserved
19:18	<p><b>SLP_SUS# Minimum Assertion Width (SLP_SUS_MIN_ASST_WDTH)</b>—R/WL. This field indicates the minimum assertion width of the SLP_SUS# signal to guarantee that the SUS power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power circuits, and so on.</p> <p>Valid values are:</p> <ul style="list-style-type: none"> <li>11 = 4 seconds</li> <li>10 = 1 second</li> <li>01 = 500 ms</li> <li>00 = 0 ms (that is, stretching disabled—default)</li> </ul> <p>These bits are cleared by RTCRST# assertion.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This field is RO when the SLP Stretching Policy Lock-Down bit is set.</li> <li>2. This field is ignored when exiting G3 or Deep Sx states if the “Disable SLP Stretching After SUS Well Power Up” bit is set. Unlike with all other SLP_* pin stretching, this disable bit only impacts SLP_SUS# stretching during G3 exit rather than both G3 and Deep Sx exit. SLP_SUS# stretching always applies to Deep Sx regardless of the disable bit.</li> <li>3. For platforms that enable Deep Sx, BIOS must program SLP_SUS# stretching to be greater than or equal to the largest stretching value on any other SLP_* pin (SLP_S3#, SLP_S4#, SLP_LAN# or SLP_A#).</li> </ol>
17:16	<p><b>SLP_A# Minimum Assertion Width (SLP_A_MIN_ASST_WDTH)</b>—R/W. This field indicates the minimum assertion width of the SLP_A# signal to guarantee that the ASW power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power circuits, and so on.</p> <p>Valid values are:</p> <ul style="list-style-type: none"> <li>11 = 2 seconds</li> <li>10 = 98 ms</li> <li>01 = 4 seconds</li> <li>00 = 0 ms (that is, stretching disabled – default)</li> </ul> <p>These bits are cleared by RTCRST# assertion.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This field is RO when the SLP Stretching Policy Lock-Down bit is set.</li> <li>2. This field is ignored when exiting G3 or Deep Sx states if the “Disable SLP Stretching After SUS Well Power Up” bit is set.</li> </ol>
15:14	<p><b>SLP_LAN# Minimum Assertion Width (SLP_LAN_MIN_ASST_WDTH)</b>—R/WL. This field indicates the minimum assertion width of the SLP_LAN# signal to guarantee that the PHY power supplies have been fully power-cycled. This value may be modified per platform depending on power supply capacitance, board capacitance, power circuits, and so on.</p> <p>Valid values are:</p> <ul style="list-style-type: none"> <li>11 = 2 seconds</li> <li>10 = 50 ms</li> <li>01 = 1 ms</li> <li>00 = 0 ms (that is, stretching disabled – default)</li> </ul> <p>These bits are cleared by RTCRST# assertion.</p> <p><b>Note:</b> This field is RO when the SLP Stretching Policy Lock-Down bit is set.</p>
13:11	Reserved



Bit	Description
10	<p><b>Power Button Debounce Mode (PB_DB_MODE)</b>—R/W. This bit controls when interrupts (SMI#, SCI) are generated in response to assertion of the PWRBTN# pin.</p> <p>0 = The 16 ms debounce period applies to all usages of the PWRBTN# pin (legacy behavior). An SMI#, SCI interrupt response to an assertion of PWRBTN# pin event is not generated until after this 16 ms debounce period.</p> <p>1 = When a falling edge occurs on the PWRBTN# pin, an SMI#/SCI interrupt is generated immediately. The debounce timer starts and is used to mask subsequent interrupts during this 16 ms period.</p> <p><b>Note:</b> Power button override logic always samples the post-debounce version of the pin.</p>
9:8	<p><b>Reset Power-Cycle Duration (PWR_CYC_DUR)</b>—R/WL. This field indicates the minimum time a platform will stay in reset (SLP_S3#, SLP_S4#, SLP_S5# asserted and SLP_A# and SLP_LAN# asserted if applicable) during a host reset with power-cycle, host reset with power down or a global reset. The duration programmed in this field takes precedence over the applicable SLP_# stretch timers in these reset scenarios.</p> <p>Valid values are:</p> <ul style="list-style-type: none"> <li>11 = 1-2 seconds</li> <li>10 = 2-3 seconds</li> <li>01 = 3-4 seconds</li> <li>00 = 4-5 seconds (default)</li> </ul> <p>These bits are cleared by RTCRST# assertion.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>This field is RO when the SLP Stretching Policy Lock-Down bit is set.</li> <li>The duration programmed in this field should never be smaller than the stretch duration programmed in the following registers: <ul style="list-style-type: none"> <li>— GEN_PMCN_3.SLP_S3_MIN_ASST_WDTH</li> <li>— GEN_PMCN_3.SLP_S4_MIN_ASST_WDTH</li> <li>— PM_CFG.SLP_A_MIN_ASST_WDTH</li> <li>— PM_CFG.SLP_LAN_MIN_ASST_WDTH</li> </ul> </li> </ol>
7:2	Reserved
1:0	<p><b>Timing T218 (TIMING_T218)</b>—R/W. This field configures the t218 timing involved in the power down flow (PROCPWRGD inactive to clocks invalid. Encodings are all minimum timings.</p> <p>00 = 10 <math>\mu</math>s (default)</p> <p>01 = 100 <math>\mu</math>s</p> <p>10 = 1 ms</p> <p>11 = 10 ms</p> <p>These bits are cleared by RSMRST# assertion.</p>

### 8.1.42 DEEP\_S3\_POL—Deep Sx From S3 Power Policies Register

Offset Address: 3328-332Bh  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

This register is in the RTC power well and is reset by RTCRST# assertion.

Bit	Description
31:2	Reserved
1	<b>Deep Sx From S3 Enable in DC Mode (DPS3_EN_DC)</b> —R/W. A (one) 1 in this bit enables the platform to enter Deep Sx while operating in S3 on DC power (based on the ACPRESENT pin value).
0	<b>Deep Sx From S3 Enable in AC Mode (DPS3_EN_AC)</b> —R/W. A (one) 1 in this bit enables the platform to enter Deep Sx while operating in S3 on AC power (based on the ACPRESENT pin value). Required to be programmed to 0 on mobile.

### 8.1.43 DEEP\_S4\_POL—Deep Sx From S4 Power Policies Register

Offset Address: 332C-332Fh Attribute: R/W, RO  
Default Value: 00000000h Size: 32 bits

This register is in the RTC power well and is reset by RTCRST# assertion.

Bit	Description
31:2	Reserved
1	<b>Deep Sx From S4 Enable in DC Mode (DPS4_EN_DC)</b> —R/W. A (one) 1 in this bit enables the platform to enter Deep Sx while operating in S4 on DC power (based on the ACPRESENT pin value).
0	<b>Deep Sx From S4 Enable in AC Mode (DPS4_EN_AC)</b> —R/W. A (one) 1 in this bit enables the platform to enter Deep Sx while operating in S4 on AC power (based on the ACPRESENT pin value). Required to be programmed to 0 on mobile.

### 8.1.44 DEEP\_S5\_POL—Deep Sx From S5 Power Policies Register

Offset Address: 3330-3333h Attribute: R/W, RO  
Default Value: 00000000h Size: 32 bits

This register is in the RTC power well and is reset by RTCRST# assertion.

Bit	Description
31:16	Reserved
15	<b>Deep Sx From S5 Enable in DC Mode (DPS5_EN_DC)</b> —R/W. A (one) 1 in this bit enables the platform to enter Deep Sx while operating in S5 on DC power (based on the ACPRESENT pin value).
14	<b>Deep Sx From S5 Enable in AC Mode (DPS5_EN_AC)</b> —R/W. A (one) 1 in this bit enables the platform to enter Deep Sx while operating in S5 on AC power (based on the ACPRESENT pin value). Required to be programmed to 0 on mobile.
13:0	Reserved

### 8.1.45 DSX\_CFG—Deep Sx Configuration Register

Offset Address: 3334–3337h  
 Default Value: 00000000h

Attribute: R/W, RO  
 Size: 32 bits

This register is in the RTC power well and is reset by RTCRST# assertion.

Bit	Description
31:3	Reserved
2	<p><b>WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN)</b>—R/W. When this bit is 1 the PCI Express* WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case).</p> <p>When this bit is 0:</p> <ul style="list-style-type: none"> <li>Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time.</li> <li>Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled.</li> </ul> <p><b>Note:</b> Deep Sx disabled configuration must leave this bit at 0.</p>
1	<p><b>ACPRESENT Pin Pull-down in Deep Sx Disable (ACPRE_PDSX_DIS)</b>—R/W. When this bit is '1', the internal pull-down on this ACPRESENT pin is disabled. However, the pull-down is not necessarily enabled if the bit is '0'. To support ME wakes from Deep Sx using GPIO2, the pin is always monitored regardless of the value of this host policy bit.</p> <p>When this bit is 0:</p> <ul style="list-style-type: none"> <li>Deep Sx configurations: The PCH internal pull-down on ACPRESENT is enabled in Deep Sx and during G3 exit.</li> <li>Deep Sx disabled configurations: The PCH internal pull-down on ACPRESENT is always disabled.</li> </ul> <p><b>Note:</b> Deep Sx disabled configuration must leave this bit at '0' and the pull-down is disabled even though the bit is 0.</p>
0	<p><b>GP27 Pin Deep Sx Enable (GP27_PIN_DSX_EN)</b>—R/W. When this bit is '1', the GP27 pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must drive the pin to the correct value while in Deep Sx.</p> <p>When this bit is 0:</p> <ul style="list-style-type: none"> <li>Deep Sx configurations: The PCH internal pull-down on GP27 pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time.</li> <li>Deep Sx disabled configurations: The PCH internal pull-down on GP27 pin is never enabled.</li> </ul> <p><b>Note:</b> Deep Sx disabled configuration must leave this bit at '0'.</p>

### 8.1.46 PMSYNC\_CFG—PMSYNC Configuration Register

Offset Address: 33C8–33CBh      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:12	Reserved
11	<b>GPIO_D Pin Selection (GPIO_D_SEL)</b> —R/W. There are two possible GPIOs that can be routed to the GPIO_D PMSYNC state. This bit selects between them. 0 = GPIO80 (default) 1 = GPIO79
10	<b>GPIO_C Pin Selection (GPIO_C_SEL)</b> —R/W. There are two possible GPIOs that can be routed to the GPIO_C PMSYNC state. This bit selects between them. 0 = GPIO37 (default) 1 = GPIO78
9	<b>GPIO_B Pin Selection (GPIO_B_SEL)</b> —R/W. There are two possible GPIOs that can be routed to the GPIO_B PMSYNC state. This bit selects between them. 0 = GPIO79 (default) 1 = GPIO37
8	<b>GPIO_A Pin Selection (GPIO_A_SEL)</b> —R/W. There are two possible GPIOs that can be routed to the GPIO_A PMSYNC state. This bit selects between them. 0 = GPIO78 (default) 1 = GPIO80
7:0	Reserved

### 8.1.47 ACPI\_TMR\_CTL—ACPI Timer Control Register

Offset Address: 33FCh      Attribute: R/W, R/WS, RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:2	Reserved
1	<b>ACPI Timer Disable (ACPI_TIM_DIS)</b> —R/W. This bit determines whether the ACPI Timer is enabled to run. When enabled, the timer only runs during S0. 0 = ACPI Timer is enabled (default) 1 = ACPI Timer is disabled (halted at the current value)
0	<b>ACPI Timer Clear (ACPI_TIM_CLR)</b> —R/WS. Writing a 1 to this bit will clear the ACPI Timer to all 0s. Hardware will automatically clear the bit back to 0 once the timer clear operation has completed. Writing a 0 to this bit will have no effect.

### 8.1.48 RC—RTC Configuration Register

Offset Address: 3400–3403h      Attribute: R/W, R/WLO, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:5	Reserved
4	<b>Upper 128 Byte Lock (UL)</b> —R/WLO 0 = Bytes not locked. 1 = Bytes 38h–3Fh in the upper 128-byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any ensured data. Bit reset on system reset.
3	<b>Lower 128 Byte Lock (LL)</b> —R/WLO 0 = Bytes not locked. 1 = Bytes 38h–3Fh in the lower 128-byte bank of RTC RAM are locked and cannot be accessed. Writes will be dropped and reads will not return any ensured data. Bit reset on system reset.
2	<b>Upper 128 Byte Enable (UE)</b> —R/W 0 = Bytes locked. 1 = The upper 128-byte bank of RTC RAM can be accessed.
1:0	Reserved

### 8.1.49 HPTC—High Precision Timer Configuration Register

Offset Address: 3404–3407h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:8	Reserved
7	<b>Address Enable (AE)</b> —R/W 0 = Address disabled. 1 = The PCH will decode the High Precision Timer memory address range selected by bits 1:0 below.
6:2	Reserved
1:0	<b>Address Select (AS)</b> —R/W. This 2-bit field selects 1 of 4 possible memory address ranges for the High Precision Timer functionality. The encodings are: 00 = FED0_0000h – FED0_03FFh 01 = FED0_1000h – FED0_13FFh 10 = FED0_2000h – FED0_23FFh 11 = FED0_3000h – FED0_33FFh

## 8.1.50 GCS—General Control and Status Register

Offset Address: 3410–3413h Attribute: R/W, R/WLO, RO  
 Default Value: 00000yy4h (yy = xx0000x0b) Size: 32 bits

Bit	Description						
31:13	Reserved						
12:11	<b>Function Level Reset Capability Structure Select (FLRCSEL)</b> —R/W. 0 = Function Level Reset (FLR) will utilize the standard capability structure with unique capability ID assigned by PCISIG. 1 = Vendor Specific Capability Structure is selected for FLR.						
10	<b>Boot BIOS Strap (BBS)</b> —R/W. This field determines the destination of accesses to the BIOS memory range. The default values for these bits represent the strap values of GSPI_MOSI/GPIO86 at the rising edge of PWROK. <table border="1" data-bbox="652 696 913 792"> <thead> <tr> <th>Bits 10</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0b</td><td>SPI</td></tr> <tr> <td>1b</td><td>LPC</td></tr> </tbody> </table> When SPI or LPC is selected, the range that is decoded is further qualified by other configuration bits described in the respective sections. The value in this field can be overwritten by software as long as the BIOS Interface Lock-Down (bit 0) is not set.	Bits 10	Description	0b	SPI	1b	LPC
Bits 10	Description						
0b	SPI						
1b	LPC						
9	<b>Server Error Reporting Mode (SERM)</b> —R/W. 0 = The PCH is the final target of all errors. The processor sends a messages to the PCH for the purpose of generating NMI. 1 = The processor is the final target of all errors from PCI Express* and DMI. In this mode, if the PCH detects a fatal, non-fatal, or correctable error on DMI or its downstream ports, it sends a message to the processor. If the PCH receives an ERR_* message from the downstream port, it sends that message to the processor.						
8:6	Reserved						
5	<b>No Reboot (NR)</b> —R/W. This bit is set when the "No Reboot" strap (SPKR pin on the PCH) is sampled high on PWROK. This bit may be set or cleared by software if the strap is sampled low but may not override the strap when it indicates "No Reboot". 0 = System will reboot upon the second timeout of the TCO timer. 1 = The TCO timer will count down and generate the SMI# on the first timeout, but will not reboot on the second timeout.						
4	<b>Alternate Access Mode Enable (AME)</b> —R/W. 0 = Disabled. 1 = Alternate access read only registers can be written, and write only registers can be read. Before entering a low power state, several registers from powered down parts may need to be saved. In the majority of cases, this is not an issue, as registers have read and write paths. However, several of the ISA compatible registers are either read only or write only. To get data out of write-only registers, and to restore data into read-only registers, the PCH implements an alternate access mode. For a list of these registers, see <a href="#">Section 5.11.10</a> .						
3	<b>Shutdown Policy Select (SPS)</b> —R/W. 0 = PCH will drive INIT# in response to the shutdown Vendor Defined Message (VDM). (default) 1 = PCH will treat the shutdown VDM similar to receiving a CF9h I/O write with data value 06h, and will drive PLTRST# active.						

Bit	Description
2	<p><b>Reserved Page Route (RPR)</b>—R/W. Determines where to send the reserved page registers. These addresses are sent to PCI or LPC for the purpose of generating POST codes. The I/O addresses modified by this field are: 80h, 84h, 85h, 86h, 88h, 8Ch, 8Dh, and 8Eh.</p> <p>0 = Writes will be forwarded to LPC, shadowed within the PCH, and reads will be returned from the internal shadow</p> <p>1 = Writes will be forwarded to PCI, shadowed within the PCH, and reads will be returned from the internal shadow.</p> <p><b>Note:</b> If some writes are done to LPC/PCI to these I/O ranges, and then this bit is flipped, such that writes will now go to the other interface, the reads will not return what was last written. Shadowing is performed on each interface.</p> <p>The aliases for these registers, at 90h, 94h, 95h, 96h, 98h, 9Ch, 9Dh, and 9Eh, are always decoded to LPC.</p>
1	Reserved
0	<p><b>BIOS Interface Lock-Down (BILD)</b>—R/WLO.</p> <p>0 = Disabled.</p> <p>1 = Prevents BUC.TS (offset 3414, bit 0) and GCS.BBS (offset 3410h, bits 11:10) from being changed. This bit can only be written from 0 to 1 once.</p>

### 8.1.51 BUC—Backed Up Control Register

Offset Address: 3414–3414h      Attribute: R/W, RO  
 Default Value: 0000000xb      Size: 8 bits

All bits in this register are in the RTC well and only cleared by RTCRST#.

Bit	Description
7:6	Reserved
5	<p><b>LAN Disable</b>—R/W</p> <p>0 = LAN is Enabled</p> <p>1 = LAN is Disabled.</p> <p>Changing the internal GbE controller from disabled to enabled requires a system reset (write of 0Eh to CF9h (RST_CNT register)) immediately after clearing the LAN disable bit. A reset is not required if changing the bit from enabled to disabled.</p> <p>This bit is locked by the Function Disable SUS Well Lockdown register. Once locked, this bit cannot be changed by software.</p>
4	<p><b>Daylight Savings Override (SDO)</b>—R/W</p> <p>0 = Daylight Savings feature is dependent on Daylight Savings Enable bit located at RTC_REGB.DSE.</p> <p>1 = Daylight Savings feature is ALWAYS DISABLED, regardless of the setting in RTC_REGB.DSE.</p>
3:1	Reserved
0	<p><b>Top Swap (TS)</b>—R/W</p> <p>0 = PCH will not invert A16, A17 or A18.</p> <p>1 = PCH will invert A16, A17 or A18 for cycles going to the BIOS space.</p> <p>If booting from LPC (FWH), then the boot-block size is 64KB and A16 is inverted if Top Swap is enabled.</p> <p>If booting from SPI, then the Top Swap Block size soft strap determines if A16, A17, or A18 should be inverted if Top Swap is enabled.</p> <p>If PCH is strapped for Top Swap (SDIO_D0/GPIO66 is high at rising edge of PWROK), then this bit cannot be cleared by software. The strap jumper should be removed and the system rebooted.</p>

## 8.1.52 FD—Function Disable Register

Offset Address: 3418–341Bh      Attribute: R/W, RO  
 Default Value: See bit description      Size: 32 bits

When disabling a function, only the configuration space is disabled. Software must ensure that all functionality within a controller that is not desired (such as memory spaces, I/O spaces, and DMA engines) is disabled prior to disabling the function.

When a function is disabled, software must not attempt to re-enable it. A disabled function can only be re-enabled by a platform reset.

Bit	Description
31:28	Reserved
27	<b>xHCI Disable (XHD)</b> —R/W. Default is 0. 0 = The xHCI controller (D20:F0) is enabled. 1 = The xHCI controller (D20:F0) is disabled.
26:25	Reserved
24	<b>Thermal Sensor Registers Disable (TTD)</b> —R/W. Default is 0. 0 = Thermal Sensor Registers (D31:F6) are enabled. 1 = Thermal Sensor Registers (D31:F6) are disabled.
23:22	Reserved
21	<b>PCI Express* 6 Disable (PE6D)</b> —R/W. Default is 0. When disabled, the link for this port is put into the “link down” state. 0 = PCI Express* port #6 is enabled. 1 = PCI Express* port #6 is disabled.
20	<b>PCI Express* 5 Disable (PE5D)</b> —R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express* port #5 is enabled. 1 = PCI Express* port #5 is disabled.
19	<b>PCI Express* 4 Disable (PE4D)</b> —R/W. Default is 0. When disabled, the link for this port is put into the “link down” state. 0 = PCI Express* port #4 is enabled. 1 = PCI Express* port #4 is disabled. <b>Note:</b> This bit must be set when Port 1 is configured as a x4.
18	<b>PCI Express* 3 Disable (PE3D)</b> —R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express* port #3 is enabled. 1 = PCI Express* port #3 is disabled. <b>Note:</b> This bit must be set when Port 1 is configured as a x4.
17	<b>PCI Express* 2 Disable (PE2D)</b> —R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express* port #2 is enabled. 1 = PCI Express* port #2 is disabled. <b>Note:</b> This bit must be set when Port 1 is configured as a x4 or a x2.
16	<b>PCI Express* 1 Disable (PE1D)</b> —R/W. Default is 0. When disabled, the link for this port is put into the link down state. 0 = PCI Express* port #1 is enabled. 1 = PCI Express* port #1 is disabled. <b>Note:</b> When this bit is set, RPN (RCBA+404h) should be used to re-assign PCIe* port #1 (function 0) to another PCIe* port. This is needed to remain compliant to PCIe* specification which requires function 0 to be defined for a multi-function device.
15	<b>EHCI #1 Disable (EHC11D)</b> —R/W. Default is 0. 0 = The EHCI #1 is enabled. 1 = The EHCI #1 is disabled.

Bit	Description
14	<p><b>LPC Bridge Disable (LBD)</b>—R/W. Default is 0.</p> <p>0 = The LPC bridge is enabled.</p> <p>1 = The LPC bridge is disabled. Unlike the other disables in this register, the following additional spaces will no longer be decoded by the LPC bridge:</p> <ul style="list-style-type: none"> <li>— Memory cycles below 16MB (1000000h)</li> <li>— I/O cycles below 64KB (10000h)</li> <li>— The Internal I/OxAPIC at FEC0_0000 to FECF_FFFF</li> </ul> <p>Memory cycle in the LPC BIOS range below 4GB will still be decoded when this bit is set; however, the aliases at the top of 1MB (the E and F segment) no longer will be decoded.</p>
13:5	Reserved
4	<p><b>Intel® High Definition Audio Disable (HDAD)</b>—R/W. Default is 0.</p> <p>0 = The Intel High Definition Audio controller is enabled.</p> <p>1 = The Intel High Definition Audio controller is disabled and its PCI configuration space is not accessible.</p>
3	<p><b>SMBus Disable (SD)</b>—R/W. Default is 0.</p> <p>0 = The SMBus controller is enabled.</p> <p>1 = The SMBus controller is disabled. Setting this bit only disables the PCI configuration space.</p>
2	<p><b>Serial ATA Disable 1 (SAD1)</b>—R/W. Default is 0.</p> <p>0 = The SATA controller #1 (D31:F2) is enabled.</p> <p>1 = The SATA controller #1 (D31:F2) is disabled.</p>
1	<p><b>Intel® SST Disable (SSTD)</b>—R/W. Default is 0.</p> <p>0 = The Intel® SST controller (D19:F0) is enabled.</p> <p>1 = The Intel® SST controller (D19:F0) is disabled.</p> <p><b>Note:</b> Feature may be disabled on certain SKU. If feature is disabled based on SKU, this bit is read-only as 1.</p>
0	BIOS must program this field to 1b.

### 8.1.53 CG—Clock Gating Register

Offset Address: 341C-341Fh  
 Default Value: 00000000h

Attribute: R/W, RO  
 Size: 32 bits

Bit	Description
31:29	<b>CG Field 3—R/W</b> BIOS may program this field.
28	<b>GPIO Dynamic Clock Gating Enable (GPDCGE)—R/W</b> 0 = GPIO Dynamic Clock Gating is Disabled 1 = GPIO Dynamic Clock Gating is Enabled
27	<b>HPET Dynamic Clock Gating Enable (GPDCGE)—R/W</b> 0 = HPET Dynamic Clock Gating is Disabled 1 = HPET Dynamic Clock Gating is Enabled
26	<b>CG Field 2—R/W</b> BIOS may program this field.
25	<b>8254 Static Clock Gating Enable (8254CGE)—R/W</b> 0 = 8254 Timer Static Clock Gating is Disabled 1 = 8254 Timer Static Clock Gating is Enabled
24	CG Field 1—R/W BIOS may program this field.
23	<b>LAN Static Clock Gating Enable (LANSCGE)—R/W</b> 0 = LAN Static Clock Gating is Disabled 1 = LAN Static Clock Gating is Enabled when the LAN Disable bit is set in the Backed Up Control RTC register.
22	<b>High Definition Audio Dynamic Clock Gate Enable—R/W</b> 0 = High Definition Audio Dynamic Clock Gating is Disabled 1 = High Definition Audio Dynamic Clock Gating is Enabled
21	<b>High Definition Audio Static Clock Gate Enable—R/W</b> 0 = High Definition Audio Static Clock Gating is Disabled 1 = High Definition Audio Static Clock Gating is Enabled
20:6	Reserved
5	<b>SMBus Clock Gating Enable (SMBCGEN)—R/W</b> 0 = SMBus Clock Gating is Disabled. 1 = SMBus Clock Gating is Enabled. <b>Note:</b> Setting this bit will also clock gate all the TCO logic functionality.
4:0	Reserved

### 8.1.54 FDSW—Function Disable SUS Well Register

Offset Address: 3420h  
 Default Value: 00h

Attribute: R/W, RO  
 Size: 8 bits

Bit	Description
7	<b>Function Disable SUS Well Lockdown (FDSWL)—R/W</b> 0 = FDSW registers are not locked down 1 = FDSW registers are locked down and this bit will remain set until a global reset occurs. <b>Note:</b> This bit must be set when Intel Active Management Technology is enabled.
6:0	Reserved

### 8.1.55 DISPBF—Display Bus, Device, and Function Initialization Register

Offset Address: 3424–3425h Attribute: R/W  
 Default Value: 0010h Size: 16 bits

Bit	Description
15:8	<b>Display Bus Number (DBN)</b> —R/W. The bus number of the Display in the processor. BIOS must program this field to 0h.
7:3	<b>Display Device Number (DDN)</b> —R/W. The device number of the Display in the processor. BIOS must program this field to 2h.
2:0	<b>Display Function Number (DFN)</b> —R/W. The function number of the Display in the processor. BIOS must program this field to 0h.

### 8.1.56 FD2—Function Disable 2 Register

Offset Address: 3428–342Bh Attribute: R/W, RO  
 Default Value: 00000000h Size: 32 bits

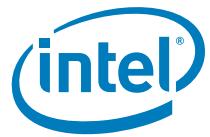
Bit	Description
31:5	Reserved
4	<b>KT Disable (KTD)</b> —R/W. Default is 0. 0 = Keyboard Text controller (D22:F3) is enabled. 1 = Keyboard Text controller (D22:F3) is Disabled
3	<b>IDE-R Disable (IRERD)</b> —R/W. Default is 0. 0 = IDE Redirect controller (D22:F2) is Enabled. 1 = IDE Redirect controller (D22:F2) is Disabled.
2	<b>Intel® MEI #2 Disable (MEI2D)</b> —R/W. Default is 0. 0 = Intel® MEI controller #2 (D22:F1) is enabled. 1 = Intel® MEI controller #2 (D22:F1) is disabled.
1	<b>Intel® MEI #1 Disable (MEI1D)</b> —R/W. Default is 0. 0 = Intel® MEI controller #1 (D22:F0) is enabled. 1 = Intel® MEI controller #1 (D22:F0) is disabled.
0	<b>Display BDF Enable (DBDFEN)</b> —R/W.

### 8.1.57 PRCSUS—Power Reduction Control SUS Well Register

Offset Address: 3434–3435h Attribute: R/W, RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7:3	Reserved
2	<b>GPIO Suspend Well Dynamic Clock Gating Enable (GPSUSDCGE)</b> —R/W. Default is 0. 0 = GPIO controller dynamic clock gating is disabled. 1 = GPIO controller dynamic clock gating is enabled.
1:0	<b>PRCSUS Field 1</b> —R/W. Default is 0. BIOS may program this field.

§ §



# 9 Gigabit LAN Configuration Registers

## 9.1 Gigabit LAN Configuration Registers (Gigabit LAN—D25:F0)

**Note:** Register address locations that are not shown in [Table 9-1](#) should be treated as Reserved. All GbE registers are located in the VCCASW power well.

**Table 9-1. Gigabit LAN Configuration Registers Address Map (Gigabit LAN—D25:F0) (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Code	020000h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	MBARA	Memory Base Address A	00000000h	R/W, RO
14h–17h	MBARB	Memory Base Address B	00000000h	R/W, RO
18h–1Bh	MBARC	Memory Base Address C	00000001h	R/W, RO
2Ch–2Dh	SVID	Subsystem Vendor ID	See register description	RO
2Eh–2Fh	SID	Subsystem ID	See register description	RO
30h–33h	ERBA	Expansion ROM Base Address	See register description	RO
34h	CAPP	Capabilities List Pointer	C8h	RO
3Ch–3Dh	INTR	Interrupt Information	See register description	R/W, RO
3Eh–3Fh	MLMG	Maximum Latency/Minimum Grant	0000h	RO
A0h–A3h	STCL	System Time Capture Low	00000000h	RO
A4h–A7h	STCH	System Time Capture High	00000000h	RO
A8h–ABh	LTR	Latency Tolerance Reporting	00000000h	R/W
C8h–C9h	CLIST1	Capabilities List 1	D001h	RO
CAh–CBh	PMC	PCI Power Management Capability	See register description	RO
CCh–CDh	PMCS	PCI Power Management Control and Status	See register description	R/WC, R/W, RO

**Table 9-1. Gigabit LAN Configuration Registers Address Map (Gigabit LAN—D25:F0) (Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
CFh	DR	Data Register	See register description	RO
D0h–D1h	CLIST2	Capabilities List Register 2	E005h	R/WO, RO
D2h–D3h	MCTL	Message Control	0080h	R/W, RO
D4h–D7h	MADDL	Message Address Low	See register description	R/W
D8h–DBh	MADDH	Message Address High	See register description	R/W
DCh–DDh	MDAT	Message Data	See register description	R/W
E0h–E1h	FLRCAP	Function Level Reset Capability	0009h	RO
E2h–E3h	FLRCLV	Function Level Reset Capability Length and Value	See register description	R/WO, RO
E4h–E5h	DEVCTRL	Device Control	0000h	R/W, RO

### 9.1.1 VID—Vendor Identification Register (Gigabit LAN—D25:F0)

Address Offset: 00h–01h  
 Default Value: 8086h

Attribute: RO  
 Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel. The field may be auto-loaded from the NVM at address 0Dh during INIT time depending on the “Load Vendor/Device ID” bit field in NVM word 0Ah with a default value of 8086h.

### 9.1.2 DID—Device Identification Register (Gigabit LAN—D25:F0)

Address Offset: 02h–03h  
 Default Value: See bit description

Attribute: RO  
 Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH Gigabit LAN controller. The field may be auto-loaded from the NVM word 0Dh during initialization time depending on the “Load Vendor/Device ID” bit field in NVM word 0Ah.

### 9.1.3 PCICMD—PCI Command Register (Gigabit LAN—D25:F0)

Address Offset: 04h–05h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable</b> —R/W. This disables pin-based INTx# interrupts on enabled hot-plug and power management events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for hot-plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and de-assert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	<b>Fast Back to Back Enable (FBE)</b> —RO. Hardwired to 0.
8	<b>SERR# Enable (SEE)</b> —R/W 0 = Disable 1 = Enables the Gb LAN controller to generate an SERR# message when PSTS.SSE is set.
7	<b>Wait Cycle Control (WCC)</b> —RO. Hardwired to 0.
6	<b>Parity Error Response (PER)</b> —R/W 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	<b>Palette Snoop Enable (PSE)</b> —RO. Hardwired to 0.
4	<b>Postable Memory Write Enable (PMWE)</b> —RO. Hardwired to 0.
3	<b>Special Cycle Enable (SCE)</b> —RO. Hardwired to 0.
2	<b>Bus Master Enable (BME)</b> —R/W 0 = Disable. All cycles from the device are master aborted 1 = Enable. Allows the root port to forward cycles onto the backbone from a Gigabit LAN device.
1	<b>Memory Space Enable (MSE)</b> —R/W 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the Gigabit LAN device.
0	<b>I/O Space Enable (IOSE)</b> —R/W. This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the Gigabit LAN device.

### 9.1.4 PCISTS—PCI Status Register (Gigabit LAN—D25:F0)

Address Offset: 06h–07h  
 Default Value: 0010h

Attribute: R/WC, RO  
 Size: 16 bits

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC 0 = No parity error detected. 1 = Set when the Gb LAN controller receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D25:F0, bit 6) is not set.
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No system error signaled. 1 = Set when the Gb LAN controller signals a system error to the internal SERR# logic.
13	<b>Received Master Abort (RMA)</b> —R/WC 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the GbE LAN controller receives a completion with unsupported request status from the backbone.
12	<b>Received Target Abort (RTA)</b> —R/WC 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the Gb LAN controller receives a completion with completer abort from the backbone.
11	<b>Signaled Target Abort (STA)</b> —R/WC 0 = No target abort received. 1 = Set whenever the Gb LAN controller forwards a target abort received from the downstream device onto the backbone.
10:9	<b>DEVSEL# Timing Status (DEV_STS)</b> —RO. Hardwired to 0.
8	<b>Master Data Parity Error Detected (DPED)</b> —R/WC 0 = No data parity error received. 1 = Set when the Gb LAN Controller receives a completion with a data parity error on the backbone and PCIMD.PER (D25:F0, bit 6) is set.
7	<b>Fast Back to Back Capable (FB2BC)</b> —RO. Hardwired to 0.
6	Reserved
5	<b>66 MHz Capable</b> —RO. Hardwired to 0.
4	<b>Capabilities List</b> —RO. Hardwired to 1. Indicates the presence of a capabilities list.
3	<b>Interrupt Status</b> —RO. Indicates status of hot-plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D25:F0:04h:bit 10).
2:0	Reserved

### 9.1.5 RID—Revision Identification Register (Gigabit LAN—D25:F0)

Offset Address: 08h Attribute: RO  
 Default Value: See bit description Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See <a href="#">Section 1.4</a> for the value of the RID Register.

### 9.1.6 CC—Class Code Register (Gigabit LAN—D25:F0)

Address Offset: 09h–0Bh Attribute: RO  
 Default Value: 020000h Size: 24 bits

Bit	Description
23:0	<b>Class Code</b> —RO. Identifies the device as an Ethernet Adapter. 020000h = Ethernet Adapter.

### 9.1.7 CLS—Cache Line Size Register (Gigabit LAN—D25:F0)

Address Offset: 0Ch Attribute: R/W  
 Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Cache Line Size</b> —R/W. This field is implemented by PCI devices as a read/write field for legacy compatibility purposes but has no impact on any device functionality.

### 9.1.8 PLT—Primary Latency Timer Register (Gigabit LAN—D25:F0)

Address Offset: 0Dh Attribute: RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Latency Timer (LT)</b> —RO. Hardwired to 0.



## 9.1.9 HEADTYP—Header Type Register (Gigabit LAN—D25:F0)

Address Offset: 0Eh  
Default Value: 00h

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	<b>Header Type (HT)</b> —RO 00h = Indicates this is a single function device.

## 9.1.10 MBARA—Memory Base Address Register A (Gigabit LAN—D25:F0)

Address Offset: 10h-13h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

The internal CSR registers and memories are accessed as direct memory mapped offsets from the base address register. Software may only access whole DWord at a time.

Bit	Description
31:17	<b>Base Address (BA)</b> —R/W. Software programs this field with the base address of this region.
16:4	<b>Memory Size (MSIZE)</b> —RO. Memory size is 128KB.
3	<b>Prefetchable Memory (PM)</b> —RO. The GbE LAN controller does not implement prefetchable memory.
2:1	<b>Memory Type (MT)</b> —RO. Set to 00b indicating a 32-bit BAR.
0	<b>Memory/I/O Space (MIOs)</b> —RO. Set to 0 indicating a Memory Space BAR.

## 9.1.11 MBARB—Memory Base Address Register B (Gigabit LAN—D25:F0)

Address Offset: 14h-17h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

The internal registers that are used to access the LAN Space in the External FLASH device. Access to these registers are direct memory-mapped offsets from the base address register. Software may only access a DWord at a time.

Bit	Description
31:12	<b>Base Address (BA)</b> —R/W. Software programs this field with the base address of this region.
11:4	<b>Memory Size (MSIZE)</b> —RO. Memory size is 4KB.
3	<b>Prefetchable Memory (PM)</b> —RO. Set to 0b indicating the Gb LAN controller does not implement prefetchable memory.
2:1	<b>Memory Type (MT)</b> —RO. Set to 00b indicating a 32-bit BAR.
0	<b>Memory/I/O Space (MIOs)</b> —RO. Set to 0 indicating a Memory Space BAR.

### 9.1.12 MBARC—Memory Base Address Register C (Gigabit LAN—D25:F0)

Address Offset: 18h–1Bh      Attribute: R/W, RO  
 Default Value: 00000001h      Size: 32 bits

Internal registers, and memories, can be accessed using I/O operations. There are two, 4-Byte registers in the I/O mapping window: Address Register and Data Register. Software may only access a DWord at a time.

Bit	Description
31:5	<b>Base Address (BA)</b> —R/W. Software programs this field with the base address of this region.
4:1	<b>I/O Size (IOSIZE)</b> —RO. I/O space size is 32 Bytes.
0	<b>Memory/I/O Space (MIOS)</b> —RO. Set to 1 indicating an I/O Space BAR.

### 9.1.13 SVID—Subsystem Vendor ID Register (Gigabit LAN—D25:F0)

Address Offset: 2Ch–2Dh      Attribute: RO  
 Default Value: See bit description      Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —RO. This value may be loaded automatically from the NVM Word 0Ch upon power up or reset depending on the “Load Subsystem ID” bit field in NVM word 0Ah. A value of 8086h is default for this field upon power up if the NVM does not respond or is not programmed. All functions are initialized to the same value.

### 9.1.14 SID—Subsystem ID Register (Gigabit LAN—D25:F0)

Address Offset: 2Eh–2Fh      Attribute: RO  
 Default Value: See bit description      Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —RO. This value may be loaded automatically from the NVM Word 0Bh upon power up or reset depending on the “Load Subsystem ID” bit field in NVM word 0Ah with a default value of 0000h. This value is loadable from NVM word location 0Ah.

### 9.1.15 ERBA—Expansion ROM Base Address Register (Gigabit LAN—D25:F0)

Address Offset: 30h–33h      Attribute: RO  
 Default Value: See bit description      Size: 32 bits

Bit	Description
31:0	<b>Expansion ROM Base Address (ERBA)</b> —RO. This register is used to define the address and size information for boot-time access to the optional FLASH memory. If no Flash memory exists, this register reports 00000000h.

### 9.1.16 CAPP—Capabilities List Pointer Register (Gigabit LAN—D25:F0)

Address Offset: 34h      Attribute: RO  
 Default Value: C8h      Size: 8 bits

Bit	Description
7:0	<b>Capabilities Pointer (PTR)</b> —RO. Indicates that the pointer for the first entry in the capabilities list is at C8h in configuration space.

### 9.1.17 INTR—Interrupt Information Register (Gigabit LAN—D25:F0)

Address Offset: 3Ch–3Dh      Attribute: R/W, RO  
 Default Value: 0100h      Size: 16 bits  
 Function Level Reset: No

Bit	Description
15:8	<b>Interrupt Pin (IPIN)</b> —RO. Indicates the interrupt pin driven by the GbE LAN controller. 01h = The GbE LAN controller implements legacy interrupts on INTA.
7:0	<b>Interrupt Line (ILINE)</b> —R/W. Default = 00h. Software written value indicates which interrupt line (vector) the interrupt is connected. No hardware action is taken on this register.

### 9.1.18 MLMG—Maximum Latency/Minimum Grant Register (Gigabit LAN—D25:F0)

Address Offset: 3Eh–3Fh      Attribute: RO  
 Default Value: 0000h      Size: 8 bits

Bit	Description
7:0	<b>Maximum Latency/Minimum Grant (MLMG)</b> —RO. Not used. Hardwired to 00h.

### 9.1.19 STCL—System Time Control Low Register (Gigabit LAN—D25:F0)

Address Offset: A0h–A3h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>System Time Control Low (STCL)</b> —RO. Lower 32 bits of the system time capture used for audio stream synchronization.

### 9.1.20 STCH—System Time Control High Register (Gigabit LAN—D25:F0)

Address Offset: A4h–A7h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>System Time Control High (STCH)</b> —RO. Upper 32 bits of the system time capture used for audio stream synchronization.

### 9.1.21 LTRCAP—System Time Control High Register (Gigabit LAN—D25:F0)

Address Offset: A8h–ABh      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:29	Reserved
28:26	<b>Maximum Non-Snoop Latency Scale (MNSLS)</b> —R/W. Provides a scale for the value contained within the Maximum Non-Snoop Latency Value field. 000b = Value times 1 ns 001b = Value times 32 ns 010b = Value times 1,024 ns 011b = Value times 32,768 ns 100b = Value times 1,048,576 ns 101b = Value times 33,554,432 ns 110b–111b = Reserved
25:16	<b>Maximum Non-Snoop Latency (MNSL)</b> —R/W. Specifies the maximum non-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. This field is also an indicator of the platforms maximum latency, should an endpoint send up LTR Latency Values with the Requirement bit not set.
15:13	Reserved
12:10	<b>Maximum Snoop Latency Scale (MSLS)</b> —R/W. Provides a scale for the value contained within the Maximum Snoop Latency Value field. 000b = Value times 1 ns 001b = Value times 32 ns 010b = Value times 1,024 ns 011b = Value times 32,768 ns 100b = Value times 1,048,576 ns 101b = Value times 33,554,432 ns 110b–111b = Reserved
9:0	<b>Maximum Snoop Latency (MSL)</b> —R/W. Specifies the maximum snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less. This field is also an indicator of the platforms maximum latency, should an endpoint send up LTR Latency Values with the Requirement bit not set.

### 9.1.22 CLIST1—Capabilities List Register 1 (Gigabit LAN—D25:F0)

Address Offset: C8h–C9h      Attribute: RO  
 Default Value: D001h      Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —RO. Value of D0h indicates the location of the next pointer.
7:0	<b>Capability ID (CID)</b> —RO. Indicates the linked list item is a PCI Power Management Register.

### 9.1.23 PMC—PCI Power Management Capabilities Register (Gigabit LAN—D25:F0)

Address Offset: CAh–CBh      Attribute: RO  
 Default Value: See bit descriptions      Size: 16 bits  
 Function Level Reset: No (Bits 15:11 only)

Bit	Description														
15:11	<b>PME_Support (PMES)</b> —RO. This five-bit field indicates the power states in which the function may assert PME#. It depend on PM Ena and AUX-PWR bits in word 0Ah in the NVM: <table> <thead> <tr> <th>Condition</th> <th>Functionality</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>PM Ena=0</td> <td>No PME at all states</td> <td>0000b</td> </tr> <tr> <td>PM Ena and AUX-PWR=0</td> <td>PME at D0 and D3<sub>HOT</sub></td> <td>01001b</td> </tr> <tr> <td>PM Ena and AUX-PWR=1</td> <td>PME at D0, D3<sub>HOT</sub> and D3<sub>COLD</sub></td> <td>11001b</td> </tr> </tbody> </table> <p>These bits are not reset by Function Level Reset.</p>			Condition	Functionality	Value	PM Ena=0	No PME at all states	0000b	PM Ena and AUX-PWR=0	PME at D0 and D3 <sub>HOT</sub>	01001b	PM Ena and AUX-PWR=1	PME at D0, D3 <sub>HOT</sub> and D3 <sub>COLD</sub>	11001b
Condition	Functionality	Value													
PM Ena=0	No PME at all states	0000b													
PM Ena and AUX-PWR=0	PME at D0 and D3 <sub>HOT</sub>	01001b													
PM Ena and AUX-PWR=1	PME at D0, D3 <sub>HOT</sub> and D3 <sub>COLD</sub>	11001b													
10	<b>D2_Support (D2S)</b> —RO. The D2 state is not supported.														
9	<b>D1_Support (D1S)</b> —RO. The D1 state is not supported.														
8:6	<b>Aux_Current (AC)</b> —RO. Required current defined in the Data register.														
5	<b>Device Specific Initialization (DSI)</b> —RO. Set to 1. The GbE LAN Controller requires its device driver to be executed following transition to the D0 un-initialized state.														
4	Reserved														
3	<b>PME Clock (PMEC)</b> —RO. Hardwired to 0.														
2:0	<b>Version (VS)</b> —RO. Hardwired to 010b to indicate support for <i>Revision 1.1 of the PCI Power Management Specification</i> .														

### 9.1.24 PMCS—PCI Power Management Control and Status Register (Gigabit LAN—D25:F0)

Address Offset: CCh—CDh Attribute: R/WC, R/W, RO  
 Default Value: See bit description Size: 16 bits  
 Function Level Reset: No (Bit 8 only)

Bit	Description
15	<b>PME Status (PMES)</b> —R/WC. This bit is set to 1 when the function detects a wake-up event independent of the state of the PMEE bit. Writing a 1 will clear this bit.
14:13	<b>Data Scale (DSC)</b> —RO. This field indicates the scaling factor to be used when interpreting the value of the Data register. For the GbE LAN and common functions this field equals 01b (indicating 0.1 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7, (or 8 for Function 0). Otherwise, it equals 00b. For the manageability functions, this field equals 10b (indicating 0.01 watt units) if the PM is enabled in the NVM, and the Data_Select field is set to 0, 3, 4, 7. Otherwise, it equals 00b.
12:9	<b>Data Select (DSL)</b> —R/W. This four-bit field is used to select which data is to be reported through the Data register (offset CFh) and Data_Scale field. These bits are writeable only when Power Management is enabled using NVM. 0h = D0 Power Consumption 3h = D3 Power Consumption 4h = D0 Power Dissipation 7h = D3 Power Dissipation 8h = Common Power All other values are reserved.
8	<b>PME Enable (PMEE)</b> —R/W. If Power Management is enabled in the NVM, writing a 1 to this bit will enable Wakeup. If Power Management is disabled in the NVM, writing a 1 to this bit has no affect, and will not set the bit to 1. This bit is not reset by Function Level Reset.
7:4	Reserved, Returns a value of 0000.
3	<b>No Soft Reset (NSR)</b> —RO. Defines if the device executed internal reset on the transition to D0. The LAN controller always reports 0 in this field.
2	Reserved, Returns a value of 0b.
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the GbE LAN Controller and to set a new power state. The values are: 00 = D0 state (default) 01 = Ignored 10 = Ignored 11 = D3 state (Power Management must be enabled in the NVM or this cycle will be ignored).

### 9.1.25 DR—Data Register (Gigabit LAN—D25:F0)

Address Offset: CFh Attribute: RO  
 Default Value: See bit description Size: 8 bits

Bit	Description
7:0	<b>Reported Data (RD)</b> —RO. This register is used to report power consumption and heat dissipation. This register is controlled by the Data_Select field in the PMCS (Offset CCh, bits 12:9), and the power scale is reported in the Data_Scale field in the PMCS (Offset CCh, bits 14:13). The data in this field is loaded from the NVM if PM is enabled in the NVM or with a default value of 00h otherwise.

### 9.1.26 CLIST2—Capabilities List Register 2 (Gigabit LAN—D25:F0)

Address Offset: D0h–D1h Attribute: R/WO, RO  
 Default Value: E005h Size: 16 bits  
 Function Level Reset: No (Bits 15:8 only)

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —R/WO. Value of E0h points to the Function Level Reset capability structure. These bits are not reset by Function Level Reset.
7:0	<b>Capability ID (CID)</b> —RO. Indicates the linked list item is a Message Signaled Interrupt Register.

### 9.1.27 MCTL—Message Control Register (Gigabit LAN—D25:F0)

Address Offset: D2h–D3h Attribute: R/W, RO  
 Default Value: 0080h Size: 16 bits

Bit	Description
15:8	Reserved
7	<b>64-bit Capable (CID)</b> —RO. Set to 1 to indicate that the GbE LAN Controller is capable of generating 64-bit message addresses.
6:4	<b>Multiple Message Enable (MME)</b> —RO. Returns 000b to indicate that the GbE LAN controller only supports a single message.
3:1	<b>Multiple Message Capable (MMC)</b> —RO. The GbE LAN controller does not support multiple messages.
0	<b>Message Signal Interrupt Enable (MSIE)</b> —R/W. 0 = MSI generation is disabled. 1 = The Gb LAN controller will generate MSI for interrupt assertion instead of INTx signaling.

### 9.1.28 MADDL—Message Address Low Register (Gigabit LAN—D25:F0)

Address Offset: D4h–D7h      Attribute: R/W  
 Default Value: See bit description      Size: 32 bits

Bit	Description
31:0	<b>Message Address Low (MADDL)</b> —R/W. Written by the system to indicate the lower 32 bits of the address to use for the MSI memory write transaction. The lower two bits will always return 0 regardless of the write operation.

### 9.1.29 MADDH—Message Address High Register (Gigabit LAN—D25:F0)

Address Offset: D8h–DBh      Attribute: R/W  
 Default Value: See bit description      Size: 32 bits

Bit	Description
31:0	<b>Message Address High (MADDH)</b> —R/W. Written by the system to indicate the upper 32 bits of the address to use for the MSI memory write transaction.

### 9.1.30 MDAT—Message Data Register (Gigabit LAN—D25:F0)

Address Offset: DCh–DDh      Attribute: R/W  
 Default Value: See bit description      Size: 32 bits

Bit	Description
31:0	<b>Message Data (MDAT)</b> —R/W. Written by the system to indicate the lower 16 bits of the data written in the MSI memory write DWord transaction. The upper 16 bits of the transaction are written as 0000h.

### 9.1.31 FLRCAP—Function Level Reset Capability Register (Gigabit LAN—D25:F0)

Address Offset: E0h–E1h      Attribute: RO  
 Default Value: 0009h      Size: 16 bits

Bit	Description
15:8	<b>Next Pointer</b> —RO. This field provides an offset to the next capability item in the capability list. The value of 00h indicates the last item in the list.
7:0	<b>Capability ID</b> —RO. The value of this field depends on the FLRCSEL bit. 13h = If FLRCSEL = 0 09h = If FLRCSEL = 1, indicating vendor specific capability. FLRCSEL is located at RCBA + 3410(bit 12). See <a href="#">Chapter 8</a> .

### 9.1.32 FLRCLV—Function Level Reset Capability Length and Version Register (Gigabit LAN—D25:F0)

Address Offset: E2h–E3h Attribute: R/WO, RO  
 Default Value: See Description. Size: 16 bits  
 Function Level Reset: No (Bits 9:8 Only When FLRCSEL = 0)

**When FLRCSEL = 0**, this register is defined as follows:

Bit	Description
15:10	Reserved
9	<b>Function Level Reset Capability</b> —R/WO 1 = Support for Function Level Reset. This bit is not reset by Function Level Reset.
8	<b>TXP Capability</b> —R/WO 1 = Indicates support for the Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	<b>Capability Length</b> —RO. The value of this field indicates the number of bytes of the vendor specific capability as required by the PCI specification. It has the value of 06h for the Function Level Reset capability.

**When FLRCSEL = 1**, this register is defined as follows:

Bit	Description
15:12	<b>Vendor Specific Capability ID</b> —RO. A value of 2h in this field identifies this capability as Function Level Reset.
11:8	<b>Capability Version</b> —RO. The value of this field indicates the version of the Function Level Reset Capability. Default is 0h.
7:0	<b>Capability Length</b> —RO. The value of this field indicates the number of bytes of the vendor specific capability as required by the PCI specification. It has the value of 06h for the Function Level Reset capability.

### 9.1.33 DEVCTRL—Device Control Register (Gigabit LAN—D25:F0)

Address Offset: E4–E5h Attribute: R/W, RO  
 Default Value: 0000h Size: 16 bits

Bit	Description
15:9	Reserved
8	Transactions Pending (TXP)—R/W 1 = Indicates the controller has issued Non-Posted requests which have not been completed. 0 = Indicates that completions for all Non-Posted requests have been received.
7:1	Reserved
0	<b>Initiate Function Level Reset</b> —R/W. This bit is used to initiate an FLT transition. A write of 1 initiates the transition. Since hardware must not respond to any cycles until Function Level Reset completion, the value read by software from this bit is 0.

## 9.2 Gigabit LAN Capabilities and Status Registers

The internal CSR registers and memories are accessed as direct memory mapped offsets from the base address register in [Section 9.1.10](#). Software may only access whole DWord at a time.

**Note:** Register address locations that are not shown in [Table 9-2](#) should be treated as Reserved.

**Table 9-2. Gigabit LAN Capabilities and Status Registers Address Map (Gigabit LAN—Memory Based Address Register A (MBARA))**

MBARA + Offset	Mnemonic	Register Name	Default	Attribute
00h-03h	GBECSR_00	Gigabit Ethernet Capabilities and Status Register 00	00100241h	R/W
18h-1Bh	GBECSR_18	Gigabit Ethernet Capabilities and Status Register 18	01501000h	R/W/SN
20h-23h	GBECSR_20	Gigabit Ethernet Capabilities and Status Register 20	1000XXXXh	R/W/V
2Ch-2Fh	GBECSR_2C	Gigabit Ethernet Capabilities and Status Register 2C	00000000h	R/W
F00h-F03h	GBECSR_F00	Gigabit Ethernet Capabilities and Status Register F00	00010008h	R/W/V
F10h-F13h	GBECSR_F10	Gigabit Ethernet Capabilities and Status Register F10	0004000Ch	R/W/SN
5400h-5403h	GBECSR_5400	Gigabit Ethernet Capabilities and Status Register 5400	XXXXXXXXh	R/W
5404h-5407h	GBECSR_5404	Gigabit Ethernet Capabilities and Status Register 5404	XXXXXXXXh	R/W
5800h-5803h	GBECSR_5800	Gigabit Ethernet Capabilities and Status Register 5800	00000008h	R/W/SN
5B54h-5B57h	GBECSR_5B54	Gigabit Ethernet Capabilities and Status Register 5B54	60000040h	RO

### 9.2.1 GBECSR\_00—Gigabit Ethernet Capabilities and Status Register 00

Address Offset: MBARA + 00h  
Default Value: 00100241h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:25	Reserved
24	<b>PHY Power Down (PHYPDN)</b> —R/W. When cleared (0b), the PHY power down setting is controlled by the internal logic of PCH.
23:0	Reserved

## 9.2.2 GBECSR\_18—Gigabit Ethernet Capabilities and Status Register 18

Address Offset: MBARA + 18h      Attribute: R/W/SN  
 Default Value: 01501000h      Size: 32 bits

Bit	Description
31:21	Reserved
20	<b>PHY Power Down Enable (PHYPDEN)</b> —R/W/SN. When set, this bit enables the PHY to enter a low-power state when the LAN controller is at the DM-Off/D3 or with no WOL.
19:0	Reserved

## 9.2.3 GBECSR\_20—Gigabit Ethernet Capabilities and Status Register 20

Address Offset: MBARA + 20h      Attribute: RO, R/W/V  
 Default Value: 1000XXXXh      Size: 32 bits

Bit	Description
31	<b>WAIT</b> —RO. Set to 1 by the Gigabit Ethernet Controller to indicate that a PCI Express* to SMBus transition is taking place. The ME/Host should not issue new MDIC transactions while this bit is set to 1. This bit is auto cleared by hardware after the transition has occurred.
30	<b>Error—R/W/V</b> . Set to 1 by the Gigabit Ethernet Controller when it fails to complete an MDI read. Software should make sure this bit is clear before making an MDI read or write command.
29	Reserved
28	<b>Ready Bit (RB)</b> —R/W/V. Set to 1 by the Gigabit Ethernet Controller at the end of the MDI transaction. This bit should be reset to 0 by software at the same time the command is written.
27:26	<b>MDI Type</b> —R/W/V. 01 = MDI Write 10 = MDI Read All other values are reserved.
25:21	<b>LAN Connected Device Address (PHYADD)</b> —R/W/V.
20:16	<b>LAN Connected Device Register Address (PHYREGADD)</b> —R/W/V.
15:0	<b>DATA</b> —R/W/V.

### 9.2.4 GBECR\_2C—Gigabit Ethernet Capabilities and Status Register 2C

Address Offset: MBARA + 2Ch      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31	<b>WOL Indication Valid (WIV)</b> —R/W. Set to 1 by BIOS to indicate that the WOL indication setting in bit 30 of this register is valid.
30	<b>WOL Enable Setting by BIOS (WESB)</b> —R/W. 1 = WOL Enabled in BIOS. 0 = WOL Disabled in BIOS.
29:0	Reserved

### 9.2.5 GBECR\_F00—Gigabit Ethernet Capabilities and Status Register F00

Address Offset: MBARA + F00h      Attribute: R/W/V  
 Default Value: 00010008h      Size: 32 bits

Bit	Description
31:6	Reserved
5	<b>Software Semaphore FLAG (SWFLAG)</b> —R/W/V. This bit is set by the device driver to gain access permission to shared CSR registers with the firmware and hardware.
4:0	Reserved

### 9.2.6 GBECR6—Gigabit Ethernet Capabilities and Status Register 6

Address Offset: MBARA + F10h      Attribute: R/W/SN  
 Default Value: 0004000Ch      Size: 32 bits

Bit	Description
31:7	Reserved
6	<b>Global GbE Disable (GGD)</b> —R/W/SN. Prevents the PHY from auto-negotiating 1000Mb/s link in all power states.
5:4	Reserved
3	<b>GbE Disable at non D0a (GDD)</b> —R/W/SN. Prevents the PHY from auto-negotiating 1000Mb/s link in all power states except D0a. This bit must be set since GbE is not supported in Sx states.
2	<b>LPLU in non D0a (LPLUND)</b> —R/W/SN. Enables the PHY to negotiate for the slowest possible link in all power states except D0a.
1	<b>LPLU in D0a (LPLUD)</b> —R/W/SN. Enables the PHY to negotiate for the slowest possible link in all power states. This bit overrides bit 2.
0	Reserved

### 9.2.7 GBECSR\_5400—Gigabit Ethernet Capabilities and Status Register 5400

Address Offset: MBARA + 5400h      Attribute: R/W  
 Default Value: XXXXXXXXh      Size: 32 bits

Bit	Description
31:0	<b>Receive Address Low (RAL)</b> —R/W. The lower 32 bits of the 48-bit Ethernet Address.

### 9.2.8 GBECSR\_5404—Gigabit Ethernet Capabilities and Status Register 5404

Address Offset: MBARA + 5404h      Attribute: R/W  
 Default Value: XXXXXXXXh      Size: 32 bits

Bit	Description
31	<b>Address Valid</b> —R/W.
30:16	Reserved
15:0	<b>Receive Address High (RAH)</b> —R/W. The lower 16 bits of the 48-bit Ethernet Address.

### 9.2.9 GBECSR\_5800—Gigabit Ethernet Capabilities and Status Register 5800

Address Offset: MBARA + 5800h      Attribute: R/W/SN  
 Default Value: 00000008h      Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Advanced Power Management Enable (APME)</b> —R/W/SN. 1 = APM Wakeup is enabled 0 = APM Wakeup is disabled

### 9.2.10 GBECSR\_5B54—Gigabit Ethernet Capabilities and Status Register 5B54

Address Offset: MBARA + 5B54h      Attribute: RO  
 Default Value: 60000040h      Size: 32 bits

Bit	Description
31:16	Reserved
15	<b>Firmware Valid Bit (FWVAL)</b> —RO. 1 = Firmware is ready 0 = Firmware is not ready
14:0	Reserved

§ §

# 10 *LPC Interface Bridge Registers (D31:F0)*

The LPC bridge function of the PCH resides in PCI D31:F0. This function contains many other functional units, such as Interrupt controllers, Timers, Power Management, System Management, GPIO, RTC, and LPC Configuration Registers.

Registers and functions associated with other functional units are described in their respective sections.

## 10.1 PCI Configuration Registers (LPC I/F—D31:F0)

**Note:** Address locations that are not shown should be treated as Reserved.

**Table 10-1. LPC Interface PCI Register Address Map (LPC I/F—D31:F0) (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0007h	R/W, RO
06h–07h	PCISTS	PCI Status	0210h	R/WC, RO
08h	RID	Revision Identification	See register description	R/WO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	01h	RO
0Bh	BCC	Base Class Code	06h	RO
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	80h	RO
2Ch–2Fh	SS	Subsystem Identifiers	00000000h	R/WO
34h	CAPP	Capability List Pointer	E0h	RO
40h–43h	PMBASE	ACPI Base Address	00000001h	R/W, RO
44h	ACPI_CNTL	ACPI Control	00h	R/W, RO
48h–4Bh	GPIOBASE	GPIO Base Address	00000001h	R/W, RO
4Ch	GC	GPIO Control	00h	R/W, RO
60h–63h	PIRQ[n]_ROUT	PIRQ[A–D] Routing Control	80808080h	R/W
64h	SIRQ_CNTL	Serial IRQ Control	10h	R/W, RO
68h–6Bh	PIRQ[n]_ROUT	PIRQ[E–H] Routing Control	80808080h	R/W
6Ch–6Dh	LPC_IBDF	IOxAPIC Bus:Device:Function	00F8h	R/W
70h–7Fh	LPC_HnBDF	HPET Configuration	00F8h	R/W
80h	LPC_I/O_DEC	I/O Decode Ranges	0000h	R/W
82h–83h	LPC_EN	LPC I/F Enables	0000h	R/W, RO
84h–87h	GEN1_DEC	LPC I/F Generic Decode Range 1	00000000h	R/W, RO

**Table 10-1. LPC Interface PCI Register Address Map (LPC I/F—D31:F0) (Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
88h-8Bh	GEN2_DEC	LPC I/F Generic Decode Range 2	00000000h	R/W, RO
8Ch-8Eh	GEN3_DEC	LPC I/F Generic Decode Range 3	00000000h	R/W, RO
90h-93h	GEN4_DEC	LPC I/F Generic Decode Range 4	00000000h	R/W, RO
94h-97h	ULKMC	USB Legacy Keyboard/Mouse Control	00002000h	RO, R/WC, R/W
98h-9Bh	LGMR	LPC I/F Generic Memory Range	00000000h	R/W
A0h-CFh		Power Management (See <a href="#">Section 10.7.1</a> )		
D0h-D3h	BIOS_SEL1	BIOS Select 1	00112233h	R/W, RO
D4h-D5h	BIOS_SEL2	BIOS Select 2	4567h	R/W
D8h-D9h	BIOS_DEC_EN1	BIOS Decode Enable 1	FFCFh	R/W, RO
DCh	BIOS_CNTL	BIOS Control	20h	R/WLO, R/W, RO
E0h-E1h	FDCAP	Feature Detection Capability ID	0009h	RO
E2h	FDLEN	Feature Detection Capability Length	0Ch	RO
E3h	FDVER	Feature Detection Version	10h	RO
E4h-E7h	FVECIDX	Feature Vector Index	00000000h	R/W, RO
E8h-EBh	FVECD	Feature Vector Data	See Description	RO
F0h-F3h	RCBA	Root Complex Base Address	00000000h	R/W, RO

### 10.1.1 VID—Vendor Identification Register (LPC I/F—D31:F0)

Offset Address: 00h-01h      Attribute: RO  
 Default Value: 8086h      Size: 16-bit  
 Lockable: No      Power Well: Core

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

### 10.1.2 DID—Device Identification Register (LPC I/F—D31:F0)

Offset Address: 02h-03h      Attribute: RO  
 Default Value: See bit description      Size: 16-bit  
 Lockable: No      Power Well: Core

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH LPC bridge. See <a href="#">Section 1.4</a> for the value of the DID Register.



### 10.1.3 PCICMD—PCI COMMAND Register (LPC I/F—D31:F0)

Offset Address: 04h–05h Attribute: R/W, RO  
 Default Value: 0007h Size: 16 bits  
 Lockable: No Power Well: Core

Bit	Description
15:10	Reserved
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	<b>SERR# Enable (SERR_EN)</b> —R/W. The LPC bridge generates SERR# if this bit is set.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	<b>Parity Error Response Enable (PERE)</b> —R/W. 0 = No action is taken when detecting a parity error. 1 = Enables the PCH LPC bridge to respond to parity errors detected on backbone interface.
5	<b>VGA Palette Snoop (VPS)</b> —RO. Hardwired to 0.
4	<b>Memory Write and Invalidate Enable (MWIE)</b> —RO. Hardwired to 0.
3	<b>Special Cycle Enable (SCE)</b> —RO. Hardwired to 0.
2	<b>Bus Master Enable (BME)</b> —RO. Bus Masters cannot be disabled.
1	<b>Memory Space Enable (MSE)</b> —RO. Memory space cannot be disabled on LPC.
0	<b>I/O Space Enable (IOSE)</b> —RO. I/O space cannot be disabled on LPC.

### 10.1.4 PCISTS—PCI Status Register (LPC I/F—D31:F0)

Offset Address: 06h–07h Attribute: RO, R/WC  
 Default Value: 0210h Size: 16-bit  
 Lockable: No Power Well: Core

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC. Set when the LPC bridge detects a parity error on the internal backbone. Set even if the PCICMD.PERE bit (D31:F0:04, bit 6) is 0. 0 = Parity Error Not detected. 1 = Parity Error detected.
14	<b>Signaled System Error (SSE)</b> —R/WC. Set when the LPC bridge signals a system error to the internal SERR# logic.
13	<b>Master Abort Status (RMA)</b> —R/WC. 0 = Unsupported request status not received. 1 = The bridge received a completion with unsupported request status from the backbone.
12	<b>Received Target Abort (RTA)</b> —R/WC. 0 = Completion abort not received. 1 = Completion with completion abort received from the backbone.
11	<b>Signaled Target Abort (STA)</b> —R/WC. 0 = Target abort Not generated on the backbone. 1 = LPC bridge generated a completion packet with target abort status on the backbone.
10:9	<b>DEVSEL# Timing Status (DEV_STS)</b> —RO. 01 = Medium Timing.



Bit	Description
8	<p><b>Data Parity Error Detected (DPED)</b>—R/WC</p> <p>0 = All conditions listed below Not met.</p> <p>1 = Set when all three of the following conditions are met:</p> <ul style="list-style-type: none"> <li>— LPC bridge receives a completion packet from the backbone from a previous request,</li> <li>— Parity error has been detected (D31:F0:06, bit 15)</li> <li>— PCICMD.PERE bit (D31:F0:04, bit 6) is set.</li> </ul>
7	<b>Fast Back to Back Capable (FBC)</b> —RO. Hardwired to 0.
6	Reserved
5	<b>66 MHz Capable (66MHZ_CAP)</b> —RO. Hardwired to 0.
4	<b>Capabilities List (CLIST)</b> —RO. Capability list exists on the LPC bridge.
3	<b>Interrupt Status (IS)</b> —RO. The LPC bridge does not generate interrupts.
2:0	Reserved

## 10.1.5 RID—Revision Identification Register (LPC I/F—D31:F0)

Offset Address: 08h Attribute: R/W  
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	<b>Revision ID (RID)</b> —R/WO. See <a href="#">Section 1.4</a> for the value of the RID Register.

## 10.1.6 PI—Programming Interface Register (LPC I/F—D31:FO)

Offset Address: 09h Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Programming Interface</b> —RO

### 10.1.7 SCC—Sub Class Code Register (LPC I/F—D31:F0)

Offset Address: 0Ah Attribute: RO  
Default Value: 01h Size: 8 bits

Bit	Description
7:0	<b>Sub Class Code</b> —RO. 8-bit value that indicates the category of bridge for the LPC bridge. 01h = PCI-to-ISA bridge.

### 10.1.8 BCC—Base Class Code Register (LPC I/F—D31:F0)

Offset Address: 0Bh Attribute: RO  
Default Value: 06h Size: 8 bits

Bit	Description
7:0	<b>Base Class Code</b> —RO. 8-bit value that indicates the type of device for the LPC bridge. 06h = Bridge device.

### 10.1.9 PLT—Primary Latency Timer Register (LPC I/F—D31:F0)

Offset Address: 0Dh Attribute: RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7:3	<b>Master Latency Count (MLC)</b> —Reserved
2:0	Reserved

### 10.1.10 HEADTYP—Header Type Register (LPC I/F—D31:F0)

Offset Address: 0Eh Attribute: RO  
 Default Value: 80h Size: 8 bits

Bit	Description
7	<b>Multi-Function Device</b> —RO. This bit is 1 to indicate a multi-function device.
6:0	<b>Header Type</b> —RO. This 7-bit field identifies the header layout of the configuration space.

### 10.1.11 SS—Subsystem Identifiers Register (LPC I/F—D31:F0)

Offset Address: 2Ch–2Fh Attribute: R/WO  
 Default Value: 00000000h Size: 32 bits

This register is initialized to logic 0 by the assertion of PLTRST#. This register can be written only once after PLTRST# de-assertion.

Bit	Description
31:16	<b>Subsystem ID (SSID)</b> —R/WO. This is written by BIOS. No hardware action taken on this value.
15:0	<b>Subsystem Vendor ID (SSVID)</b> —R/WO. This is written by BIOS. No hardware action taken on this value.

### 10.1.12 CAPP—Capability List Pointer Register (LPC I/F—D31:F0)

Offset Address: 34h Attribute: RO  
 Default Value: E0h Size: 8 bits

Bit	Description
7:0	<b>Capability Pointer (CP)</b> —RO. Indicates the offset of the first Capability item.

### 10.1.13 PMBASE—ACPI Base Address Register (LPC I/F—D31:F0)

Offset Address:	40h–43h	Attribute:	R/W, RO
Default Value:	00000001h	Size:	32 bits
Lockable:	No	Usage:	ACPI, Legacy

Power Well: Core

Sets base address for ACPI I/O registers, GPIO registers and TCO I/O registers. These registers can be mapped anywhere in the 64K I/O space on 256-byte boundaries.

Bit	Description
31:16	Reserved
15:8	<b>Base Address</b> —R/W. This field provides 256 bytes of I/O space for ACPI, GPIO, and TCO logic. This is placed on a 256-byte boundary.
7:1	Reserved
0	<b>Resource Type Indicator (RTE)</b> —RO. Hardwired to 1 to indicate I/O space.

### 10.1.14 ACPI\_CNTL—ACPI Control Register (LPC I/F—D31:F0)

Offset Address:	44h	Attribute:	R/W
Default Value:	00h	Size:	8 bit
Lockable:	No	Usage:	ACPI, Legacy

Power Well: Core

Bit	Description																		
7	<b>ACPI Enable (ACPI_EN)</b> —R/W 0 = Disable. 1 = Decode of the I/O range pointed to by the ACPI base register is enabled, and the ACPI power management function is enabled. The APM power management ranges (B2/B3h) are always enabled and are not affected by this bit.																		
6:3	Reserved																		
2:0	<b>SCI IRQ Select (SCI_IRQ_SEL)</b> —R/W Specifies on which IRQ the SCI will internally appear. If not using the APIC, the SCI must be routed to IRQ9–11, and that interrupt is not sharable with the SERIRQ stream, but is sharable with other PCI interrupts. If using the APIC, the SCI can also be mapped to IRQ20–23, and can be shared with other interrupts. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>SCI Map</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>IRQ9</td> </tr> <tr> <td>001b</td> <td>IRQ10</td> </tr> <tr> <td>010b</td> <td>IRQ11</td> </tr> <tr> <td>011b</td> <td>Reserved</td> </tr> <tr> <td>100b</td> <td>IRQ20 (Only available if APIC enabled)</td> </tr> <tr> <td>101b</td> <td>IRQ21 (Only available if APIC enabled)</td> </tr> <tr> <td>110b</td> <td>IRQ22 (Only available if APIC enabled)</td> </tr> <tr> <td>111b</td> <td>IRQ23 (Only available if APIC enabled)</td> </tr> </tbody> </table> <p>When the interrupt is mapped to APIC interrupts 9, 10 or 11, the APIC should be programmed for active-high reception. When the interrupt is mapped to APIC interrupts 20 through 23, the APIC should be programmed for active-low reception.</p>	Bits	SCI Map	000b	IRQ9	001b	IRQ10	010b	IRQ11	011b	Reserved	100b	IRQ20 (Only available if APIC enabled)	101b	IRQ21 (Only available if APIC enabled)	110b	IRQ22 (Only available if APIC enabled)	111b	IRQ23 (Only available if APIC enabled)
Bits	SCI Map																		
000b	IRQ9																		
001b	IRQ10																		
010b	IRQ11																		
011b	Reserved																		
100b	IRQ20 (Only available if APIC enabled)																		
101b	IRQ21 (Only available if APIC enabled)																		
110b	IRQ22 (Only available if APIC enabled)																		
111b	IRQ23 (Only available if APIC enabled)																		

### 10.1.15 GPIOBASE—GPIO Base Address Register (LPC I/F—D31:F0)

Offset Address: 48h–4Bh      Attribute: R/W, RO  
 Default Value: 00000001h      Size: 32 bits

Bit	Description
31:16	Reserved. Always 0.
15:10	<b>Base Address (BA)</b> —R/W. Provides the 256 bytes of I/O space for GPIO.
9:1	Reserved. Always 0.
0	RO. Hardwired to 1 to indicate I/O space.

### 10.1.16 GC—GPIO Control Register (LPC I/F—D31:F0)

Offset Address: 4Ch      Attribute: R/W, RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:5	Reserved
4	<b>GPIO Enable (EN)</b> —R/W. This bit enables/disables decode of the I/O range pointed to by the GPIO Base Address register (D31:F0:48h) and enables the GPIO function. 0 = Disable. 1 = Enable.
3:1	Reserved
0	<b>GPIO Lockdown Enable (GLE)</b> —R/W. This bit enables lockdown of certain GPIO registers. Refer to section regarding the specific registers and bits affected. 0 = Disable. 1 = Enable. When this bit is written from 1-to-0, an SMI# is generated, if enabled. This ensures that only SMM code can change the above GPIO registers after they are locked down.

### 10.1.17 PIRQ[n]\_ROUT—PIRQ[A,B,C,D] Routing Control Register (LPC I/F—D31:F0)

Offset Address: PIRQA – 60h, PIRQB – 61h, PIRQC – 62h, PIRQD – 63h Attribute: R/W, RO

Default Value: 80h Size: 8 bit  
Lockable: No Power Well: Core

Bit	Description																																							
7	<b>Interrupt Routing Enable (IRQEN)</b> —R/W. 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259. <b>Note:</b> The BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.																																							
6:4	Reserved																																							
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0101b	IRQ5	1101b	Reserved																																					
0110b	IRQ6	1110b	IRQ14																																					
0111b	IRQ7	1111b	IRQ15																																					

### 10.1.18 SIRQ\_CNTL—Serial IRQ Control Register (LPC I/F—D31:F0)

Offset Address: 64h Attribute: R/W, RO  
 Default Value: 10h Size: 8 bit  
 Lockable: No Power Well: Core

Bit	Description
7	<b>Serial IRQ Enable (SIRQEN)</b> —R/W 0 = The buffer is input only and internally SERIRQ will be a 1. 1 = Serial IRQs will be recognized. The SERIRQ pin will be configured as SERIRQ.
6	<b>Serial IRQ Mode Select (SIRQMD)</b> —R/W 0 = The serial IRQ machine will be in quiet mode. 1 = The serial IRQ machine will be in continuous mode. <b>Note:</b> For systems using Quiet Mode, this bit should be set to 1 (Continuous Mode) for at least one frame after coming out of reset before switching back to Quiet Mode. Failure to do so will result in the PCH not recognizing SERIRQ interrupts.
5:2	<b>Serial IRQ Frame Size (SIRQSZ)</b> —RO. Fixed field that indicates the size of the SERIRQ frame as 21 frames.
1:0	<b>Start Frame Pulse Width (SFPW)</b> —R/W. This is the number of 24-MHz clocks that the SERIRQ pin will be driven low by the serial IRQ machine to signal a start frame. In continuous mode, the PCH will drive the start frame for the number of clocks specified. In quiet mode, the PCH will drive the start frame for the number of clocks specified minus one, as the first clock was driven by the peripheral. 00 = 4 clocks 01 = 6 clocks 10 = 8 clocks 11 = Reserved

### 10.1.19 PIRQ[n]\_ROUT—PIRQ[E,F,G,H] Routing Control Register (LPC I/F—D31:F0)

Offset Address: PIRQE – 68h, PIRQF – 69h, PIRQG – 6Ah, PIRQH – 6Bh Attribute: R/W, RO

Default Value: 80h Size: 8 bits  
Lockable: No Power Well: Core

Bit	Description																																							
7	<b>Interrupt Routing Enable (IRQEN)</b> —R/W 0 = The corresponding PIRQ is routed to one of the ISA-compatible interrupts specified in bits[3:0]. 1 = The PIRQ is not routed to the 8259.  <b>Note:</b> The BIOS must program this bit to 0 during POST for any of the PIRQs that are being used. The value of this bit may subsequently be changed by the OS when setting up for I/O APIC interrupt delivery mode.																																							
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0111b	IRQ7	1111b	IRQ15																																					

### 10.1.20 LPC\_IBDF—IOxAPIC Bus:Device:Function Register (LPC I/F—D31:F0)

Offset Address: 6Ch–6Dh Attribute: R/W  
Default Value: 00F8h Size: 16 bits

Bit	Description									
15:0	<b>IOxAPIC Bus:Device:Function (IBDF)</b> —R/W. This field specifies the bus:device:function that the PCH IOxAPIC will be using for the following: <ul style="list-style-type: none"> <li>As the Requester ID when initiating Interrupt Messages to the processor.</li> <li>As the Completer ID when responding to the reads targeting the IOxAPIC's Memory-Mapped I/O registers.</li> </ul> The 16-bit field comprises the following: <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>15:8</td> <td>Bus Number</td> </tr> <tr> <td>7:3</td> <td>Device Number</td> </tr> <tr> <td>2:0</td> <td>Function Number</td> </tr> </tbody> </table> This field defaults to Bus 0: Device 31: Function 0 after reset. BIOS can program this field to provide a unique bus:device:function number for the internal IOxAPIC.		Bits	Description	15:8	Bus Number	7:3	Device Number	2:0	Function Number
Bits	Description									
15:8	Bus Number									
7:3	Device Number									
2:0	Function Number									

### 10.1.21 **LPC\_HnBDF—HPET n Bus:Device:Function Register (LPC I/F—D31:F0)**

Address Offset	H0BDF 70h-71h H1BDF 72h-73h H2BDF 74h-75h H3BDF 76h-77h H4BDF 78h-79h H5BDF 7Ah-7Bh H6BDF 7Ch-7Dh H7BDF 7Eh-7Fh	Attribute: R/W
Default Value:	00F8h	Size: 16 bits

Bit	Description								
15:0	<p><b>HPET n Bus:Device:Function (HnBDF)</b>—R/W. This field specifies the bus:device:function that the PCH's HPET n will be using in the following:</p> <ul style="list-style-type: none"> <li>As the Requester ID when initiating Interrupt Messages to the processor</li> <li>As the Completer ID when responding to the reads targeting the corresponding HPET's Memory-Mapped I/O registers</li> </ul> <p>The 16-bit field comprises the following:</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>15:8</td><td>Bus Number</td></tr> <tr> <td>7:3</td><td>Device Number</td></tr> <tr> <td>2:0</td><td>Function Number</td></tr> </tbody> </table> <p>This field is default to Bus 0: Device 31: Function 0 after reset. BIOS shall program this field accordingly if unique bus:device:function number is required for the corresponding HPET.</p>	Bits	Description	15:8	Bus Number	7:3	Device Number	2:0	Function Number
Bits	Description								
15:8	Bus Number								
7:3	Device Number								
2:0	Function Number								

### 10.1.22 **LPC\_I/O\_DEC—I/O Decode Ranges Register (LPC I/F—D31:F0)**

Offset Address: 80h      Attribute: R/W, RO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:13	Reserved
12	<b>FDD Decode Range</b> —R/W. Determines which range to decode for the FDD Port 0 = 3F0h – 3F5h, 3F7h (Primary) 1 = 370h – 375h, 377h (Secondary)
11:10	Reserved
9:8	<b>LPT Decode Range</b> —R/W. This field determines which range to decode for the LPT Port. 00 = 378h – 37Fh and 778h – 77Fh 01 = 278h – 27Fh (port 279h is read only) and 678h – 67Fh 10 = 3BCh – 3BEh and 7BCh – 7BEh 11 = Reserved
7	Reserved
6:4	<b>COMB Decode Range</b> —R/W. This field determines which range to decode for the COMB Port. 000 = 3F8h – 3FFh (COM1) 001 = 2F8h – 2FFh (COM2) 010 = 220h – 227h 011 = 228h – 22Fh 100 = 238h – 23Fh 101 = 2E8h – 2EFh (COM4) 110 = 338h – 33Fh 111 = 3E8h – 3EFh (COM3)
3	Reserved
2:0	<b>COMA Decode Range</b> —R/W. This field determines which range to decode for the COMA Port. 000 = 3F8h – 3FFh (COM1) 001 = 2F8h – 2FFh (COM2) 010 = 220h – 227h 011 = 228h – 22Fh 100 = 238h – 23Fh 101 = 2E8h – 2EFh (COM4) 110 = 338h – 33Fh 111 = 3E8h – 3EFh (COM3)

### 10.1.23 LPC\_EN—LPC I/F Enables Register (LPC I/F—D31:F0)

Offset Address: 82h – 83h  
 Default Value: 0000h

Attribute: R/W, RO  
 Size: 16 bits  
 Power Well: Core

Bit	Description
15:14	Reserved
13	<b>CNF2_LPC_EN</b> —R/W. Microcontroller Enable # 2. 0 = Disable. 1 = Enables the decoding of the I/O locations 4Eh and 4Fh to the LPC interface. This range is used for a microcontroller.
12	<b>CNF1_LPC_EN</b> —R/W. Super I/O Enable. 0 = Disable. 1 = Enables the decoding of the I/O locations 2Eh and 2Fh to the LPC interface. This range is used for Super I/O devices.
11	<b>MC_LPC_EN</b> —R/W. Microcontroller Enable # 1. 0 = Disable. 1 = Enables the decoding of the I/O locations 62h and 66h to the LPC interface. This range is used for a microcontroller.
10	<b>KBC_LPC_EN</b> —R/W. Keyboard Enable. 0 = Disable. 1 = Enables the decoding of the I/O locations 60h and 64h to the LPC interface. This range is used for a microcontroller.
9	<b>GAMEH_LPC_EN</b> —R/W. High Gameport Enable 0 = Disable. 1 = Enables the decoding of the I/O locations 208h to 20Fh to the LPC interface. This range is used for a gameport.
8	<b>GAMEL_LPC_EN</b> —R/W. Low Gameport Enable 0 = Disable. 1 = Enables the decoding of the I/O locations 200h to 207h to the LPC interface. This range is used for a gameport.
7:4	Reserved
3	<b>FDD_LPC_EN</b> —R/W. Floppy Drive Enable 0 = Disable. 1 = Enables the decoding of the FDD range to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register (D31:F0:80h, bit 12).
2	<b>LPT_LPC_EN</b> —R/W. Parallel Port Enable 0 = Disable. 1 = Enables the decoding of the LPT range to the LPC interface. This range is selected in the LPC_FDD/LPT Decode Range Register (D31:F0:80h, bit 9:8).
1	<b>COMB_LPC_EN</b> —R/W. Com Port B Enable 0 = Disable. 1 = Enables the decoding of the COMB range to the LPC interface. This range is selected in the LPC_COM Decode Range Register (D31:F0:80h, bits 6:4).
0	<b>COMA_LPC_EN</b> —R/W. Com Port A Enable 0 = Disable. 1 = Enables the decoding of the COMA range to the LPC interface. This range is selected in the LPC_COM Decode Range Register (D31:F0:80h, bits 3:2).

### 10.1.24 GEN1\_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0)

Offset Address: 84h–87h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits  
Power Well: Core

Bit	Description
31:24	Reserved
23:18	<b>Generic I/O Decode Range Address[7:2] Mask</b> —R/W. A (one) 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	<b>Generic I/O Decode Range 1 Base Address (GEN1_BASE)</b> —R/W <b>Note:</b> The PCH does not provide decode down to the word or byte level
1	Reserved
0	<b>Generic Decode Range 1 Enable (GEN1_EN)</b> —R/W 0 = Disable. 1 = Enable the Gen 1 I/O range to be forwarded to the LPC I/F

### 10.1.25 GEN2\_DEC—LPC I/F Generic Decode Range 2 Register (LPC I/F—D31:F0)

Offset Address: 88h–8Bh  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits  
Power Well: Core

Bit	Description
31:24	Reserved
23:18	<b>Generic I/O Decode Range Address[7:2] Mask</b> —R/W. A (one) 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	<b>Generic I/O Decode Range 2 Base Address (GEN2_BASE)</b> —R/W. <b>Note:</b> The PCH does not provide decode down to the word or byte level.
1	Reserved
0	<b>Generic Decode Range 2 Enable (GEN2_EN)</b> —R/W 0 = Disable. 1 = Enable the Gen 2 I/O range to be forwarded to the LPC I/F

### 10.1.26 GEN3\_DEC—LPC I/F Generic Decode Range 3 Register (LPC I/F—D31:F0)

Offset Address: 8Ch – 8Eh      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits  
                                     Power Well: Core

Bit	Description
31:24	Reserved
23:18	<b>Generic I/O Decode Range Address[7:2] Mask</b> —R/W. A (one) 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	<b>Generic I/O Decode Range 3 Base Address (GEN3_BASE)</b> —R/W. <b>Note:</b> The PCH does not provide decode down to the word or byte level
1	Reserved
0	<b>Generic Decode Range 3 Enable (GEN3_EN)</b> —R/W. 0 = Disable. 1 = Enable the Gen 3 I/O range to be forwarded to the LPC I/F

### 10.1.27 GEN4\_DEC—LPC I/F Generic Decode Range 4 Register (LPC I/F—D31:F0)

Offset Address: 90h – 93h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits  
                                     Power Well: Core

Bit	Description
31:24	Reserved
23:18	<b>Generic I/O Decode Range Address[7:2] Mask</b> —R/W. A (one) 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	<b>Generic I/O Decode Range 4 Base Address (GEN4_BASE)</b> —R/W <b>Note:</b> The PCH does not provide decode down to the word or byte level
1	Reserved
0	<b>Generic Decode Range 4 Enable (GEN4_EN)</b> —R/W 0 = Disable. 1 = Enable the GEN 4 I/O range to be forwarded to the LPC I/F

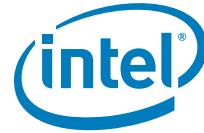


### 10.1.28 ULKMC—USB Legacy Keyboard/Mouse Control Register (LPC I/F—D31:F0)

Offset Address: 94h – 97h  
Default Value: 00002000h

Attribute: RO, R/WC, R/W  
Size: 32 bits  
Power Well: Core

Bit	Description
31:16	Reserved
15	<b>SMI Caused by End of Pass-Through (SMIBYENDPS)</b> —R/WC. This bit indicates if the event occurred. Even if the corresponding enable bit is not set in bit 7, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event occurred
14:12	Reserved
11	<b>SMI Caused by Port 64 Write (TRAPBY64W)</b> —R/WC. This bit indicates if the event occurred. Even if the corresponding enable bit is not set in bit 3, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. The A20 Gate Pass-through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event occurred.
10	<b>SMI Caused by Port 64 Read (TRAPBY64R)</b> —R/WC. This bit indicates if the event occurred. Even if the corresponding enable bit is not set in bit 2, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event occurred.
9	<b>SMI Caused by Port 60 Write (TRAPBY60W)</b> —R/WC. This bit indicates if the event occurred. Even if the corresponding enable bit is not set in bit 1, this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. The A20 Gate Pass-through Logic allows specific port 64h writes to complete without setting this bit. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event occurred.
8	<b>SMI Caused by Port 60 Read (TRAPBY60R)</b> —R/WC. This bit indicates if the event occurred. Even if the corresponding enable bit is not set in the bit 0, then this bit will still be active. It is up to the SMM code to use the enable bit to determine the exact cause of the SMI#. 0 = Software clears this bit by writing a 1 to the bit location in any of the controllers. 1 = Event occurred.
7	<b>SMI at End of Pass-Through Enable (SMIATENDPS)</b> —R/W. This bit enables SMI at the end of a pass-through. This can occur if an SMI is generated in the middle of a pass-through, and needs to be serviced later. 0 = Disable 1 = Enable
6	<b>Pass Through State (PSTATE)</b> —RO 0 = If software needs to reset this bit, it should set bit 5 in all of the host controllers to 0. 1 = Indicates that the state machine is in the middle of an A20 GATE Pass-through sequence.
5	<b>A20Gate Pass-Through Enable (A20PASSEN)</b> —R/W 0 = Disable. 1 = Enable. Allows A20GATE sequence Pass-Through function. A specific cycle sequence involving writes to port 60h and 64h does not result in the setting of the SMI status bits. <b>Note:</b> A20M# functionality is not supported.
4	<b>SMI on USB IRQ Enable (USBSMIEN)</b> —R/W 0 = Disable 1 = Enable. USB interrupt will cause an SMI event.
3	<b>SMI on Port 64 Writes Enable (64WEN)</b> —R/W 0 = Disable 1 = Enable. A (one) 1 in bit 11 will cause an SMI event.



Bit	Description
2	<b>SMI on Port 64 Reads Enable (64REN)</b> —R/W 0 = Disable 1 = Enable. A (one) 1 in bit 10 will cause an SMI event.
1	<b>SMI on Port 60 Writes Enable (60WEN)</b> —R/W 0 = Disable 1 = Enable. A (one) 1 in bit 9 will cause an SMI event.
0	<b>SMI on Port 60 Reads Enable (60REN)</b> —R/W 0 = Disable 1 = Enable. A (one) 1 in bit 8 will cause an SMI event.

### 10.1.29 LGMR—LPC I/F Generic Memory Range Register (LPC I/F—D31:F0)

Offset Address: 98h – 9Bh  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits  
Power Well: Core

Bit	Description
31:16	<b>Memory Address[31:16]</b> —R/W. This field specifies a 64KB memory block anywhere in the 4GB memory space that will be decoded to LPC as standard LPC memory cycle if enabled.
15:1	Reserved
0	<b>LPC Memory Range Decode Enable</b> —R/W. When this bit is set to 1, then the range specified in bits 31:16 of this register is enabled for decoding to LPC.

### 10.1.30 BIOS\_SEL1—BIOS Select 1 Register (LPC I/F—D31:F0)

Offset Address: D0h–D3h  
 Default Value: 00112233h

Attribute: R/W, RO  
 Size: 32 bits

Bit	Description
31:28	<b>BIOS_F8_IDSEL</b> —RO. IDSEL for two 512KB BIOS memory ranges and one, 128KB memory range. This field is fixed at 0000. The IDSEL programmed in this field addresses the following memory ranges: FFF8 0000h – FFFF FFFFh FFB8 0000h – FFBF FFFFh 000E 0000h – 000F FFFFh
27:24	<b>BIOS_F0_IDSEL</b> —R/W. IDSEL for two, 512KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFF0 0000h – FFF7 FFFFh FFB0 0000h – FFB7 FFFFh
23:20	<b>BIOS_E8_IDSEL</b> —R/W. IDSEL for two, 512KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE8 0000h – FFEF FFFFh FFA8 0000h – FFAF FFFFh
19:16	<b>BIOS_E0_IDSEL</b> —R/W. IDSEL for two, 512KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFE0 0000h – FFE7 FFFFh FFA0 0000h – FFA7 FFFFh
15:12	<b>BIOS_D8_IDSEL</b> —R/W. IDSEL for two, 512KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD8 0000h – FFDF FFFFh FF98 0000h – FF9F FFFFh
11:8	<b>BIOS_D0_IDSEL</b> —R/W. IDSEL for two, 512KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFD0 0000h – FFD7 FFFFh FF90 0000h – FF97 FFFFh
7:4	<b>BIOS_C8_IDSEL</b> —R/W. IDSEL for two, 512KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC8 0000h – FFCF FFFFh FF88 0000h – FF8F FFFFh
3:0	<b>BIOS_C0_IDSEL</b> —R/W. IDSEL for two, 512KB BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FFC0 0000h – FFC7 FFFFh FF80 0000h – FF87 FFFFh

### 10.1.31 BIOS\_SEL2—BIOS Select 2 Register (LPC I/F—D31:F0)

Offset Address: D4h–D5h      Attribute: R/W  
 Default Value: 4567h      Size: 16 bits

Bit	Description
15:12	<b>BIOS_70_IDSEL</b> —R/W. IDSEL for two, 1-M BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF70 0000h – FF7F FFFFh FF30 0000h – FF3F FFFFh
11:8	<b>BIOS_60_IDSEL</b> —R/W. IDSEL for two, 1-M BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF60 0000h – FF6F FFFFh FF20 0000h – FF2F FFFFh
7:4	<b>BIOS_50_IDSEL</b> —R/W. IDSEL for two, 1-M BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF50 0000h – FF5F FFFFh FF10 0000h – FF1F FFFFh
3:0	<b>BIOS_40_IDSEL</b> —R/W. IDSEL for two, 1-M BIOS memory ranges. The IDSEL programmed in this field addresses the following memory ranges: FF40 0000h – FF4F FFFFh FF00 0000h – FF0F FFFFh

### 10.1.32 BIOS\_DEC\_EN1—BIOS Decode Enable Register (LPC I/F—D31:F0)

Offset Address: D8h–D9h      Attribute: R/W, RO  
 Default Value: FFCFh      Size: 16 bits

Bit	Description
15	<b>BIOS_F8_EN</b> —RO. This bit enables decoding two, 512KB BIOS memory ranges, and one, 128KB memory range. 0 = Disable 1 = Enable the following ranges for the BIOS FFF80000h – FFFFFFFFh FFB80000h – FFBFFFFFh
14	<b>BIOS_F0_EN</b> —R/W. This bit enables decoding two, 512KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS: FFF00000h – FFFF7FFFFh FFB00000h – FFB7FFFFh
13	<b>BIOS_E8_EN</b> —R/W. This bit enables decoding two, 512KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS: FFE80000h – FFEFFFFFh FFA80000h – FFAFFFFFh
12	<b>BIOS_E0_EN</b> —R/W. This bit enables decoding two, 512KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS: FFE00000h – FFE7FFFFh FFA00000h – FFA7FFFFh
11	<b>BIOS_D8_EN</b> —R/W. This bit enables decoding two, 512KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FFD80000h – FFDFFFFFh FF980000h – FF9FFFFFh

Bit	Description
10	<b>BIOS_D0_EN</b> —R/W. This bit enables decoding two, 512KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FFD00000h – FFD7FFFFh FF900000h – FF97FFFFh
9	<b>BIOS_C8_EN</b> —R/W. This bit enables decoding two, 512KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FFC80000h – FFCFFFFFh FF880000h – FF8FFFFFh
8	<b>BIOS_CO_EN</b> —R/W. This bit enables decoding two, 512KB BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FFC00000h – FFC7FFFFh FF800000h – FF87FFFFh
7	<b>BIOS_Legacy_F_EN</b> —R/W. This enables the decoding of the legacy 64KB range at F0000h – FFFFFh. 0 = Disable. 1 = Enable the following legacy ranges for the BIOS F0000h – FFFFFh <b>Note:</b> The decode for the BIOS legacy F segment is enabled only by this bit and is not affected by the GEN_PMC1.iA64_EN bit.
6	<b>BIOS_Legacy_E_EN</b> —R/W. This enables the decoding of the legacy 64KB range at E0000h – EFFFFh. 0 = Disable. 1 = Enable the following legacy ranges for the BIOS E0000h – EFFFFh <b>Note:</b> The decode for the BIOS legacy E segment is enabled only by this bit and is not affected by the GEN_PMC1.iA64_EN bit.
5:4	Reserved
3	<b>BIOS_70_EN</b> —R/W. Enables decoding two, 1-M BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FF70 0000h – FF7F FFFFh FF30 0000h – FF3F FFFFh
2	<b>BIOS_60_EN</b> —R/W. Enables decoding two, 1-M BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FF60 0000h – FF6F FFFFh FF20 0000h – FF2F FFFFh
1	<b>BIOS_50_EN</b> —R/W. Enables decoding two, 1-M BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FF50 0000h – FF5F FFFFh FF10 0000h – FF1F FFFFh
0	<b>BIOS_40_EN</b> —R/W. Enables decoding two, 1-M BIOS memory ranges. 0 = Disable. 1 = Enable the following ranges for the BIOS FF40 0000h – FF4F FFFFh FF00 0000h – FF0F FFFFh

**Note:** This register affects the BIOS decode regardless of whether the BIOS is resident on LPC or SPI. The concept of Feature Space does not apply to SPI-based flash. The PCH simply decodes these ranges as memory accesses when enabled for the SPI flash interface.

### 10.1.33 BIOS\_CNTL—BIOS Control Register (LPC I/F—D31:F0)

Offset Address: DCh Attribute: R/WLO, R/W, RO  
 Default Value: 20h Size: 8 bits  
 Lockable: No Power Well: Core

Bit	Description										
7:6	Reserved										
5	<b>SMM BIOS Write Protect Disable (SMM_BWP)</b> —R/WLO. This bit defines when the BIOS region can be written by the host. 0 = BIOS region SMM protection is disabled. The BIOS Region is writable regardless if processors are in SMM or not. (Set this field to 0 for legacy behavior) 1 = BIOS region SMM protection is enabled. The BIOS Region is not writable unless all processors are in SMM.										
4	<b>Top Swap Status (TSS)</b> —RO. This bit provides a read-only path to view the state of the Top Swap bit that is at offset 3414h, bit 0.										
3:2	<b>SPI Read Configuration (SRC)</b> —R/W. This 2-bit field controls two policies related to BIOS reads on the SPI interface: Bit 3 – Prefetch Enable Bit 2 – Cache Disable Settings are summarized below: <table> <thead> <tr> <th>Bits 3:2</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td><b>No prefetching, but caching enabled.</b> 64B demand reads load the read buffer cache with “valid” data, allowing repeated code fetches to the same line to complete quickly</td></tr> <tr> <td>01b</td><td><b>No prefetching and no caching.</b> One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache.</td></tr> <tr> <td>10b</td><td><b>Prefetching and Caching enabled.</b> This mode is used for long sequences of short reads to consecutive addresses (that is, shadowing).</td></tr> <tr> <td>11b</td><td><b>Reserved. This is an invalid configuration,</b> caching must be enabled when prefetching is enabled.</td></tr> </tbody> </table>	Bits 3:2	Description	00b	<b>No prefetching, but caching enabled.</b> 64B demand reads load the read buffer cache with “valid” data, allowing repeated code fetches to the same line to complete quickly	01b	<b>No prefetching and no caching.</b> One-to-one correspondence of host BIOS reads to SPI cycles. This value can be used to invalidate the cache.	10b	<b>Prefetching and Caching enabled.</b> This mode is used for long sequences of short reads to consecutive addresses (that is, shadowing).	11b	<b>Reserved. This is an invalid configuration,</b> caching must be enabled when prefetching is enabled.
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11b	<b>Reserved. This is an invalid configuration,</b> caching must be enabled when prefetching is enabled.										
1	<b>BIOS Lock Enable (BLE)</b> —R/WO. 0 = Setting the BIOSWE will not cause SMIs. 1 = Enables setting the BIOSWE bit to cause SMIs. <b>Notes:</b> 1. When this bit is set, SMM_BWP is locked down. 2. Once set, this bit can only be cleared by a PLTRST#										
0	<b>BIOS Write Enable (BIOSWE)</b> —R/W. 0 = Only read cycles permitted to Firmware Hub I/F or SPI. 1 = Access to the BIOS space is enabled for both read and write cycles. When this bit is written from a 0 to a 1 and BIOS Lock Enable (BLE) is also set, an SMI# is generated. This ensures that only SMI code can update BIOS.										

### 10.1.34 FDCAP—Feature Detection Capability ID Register (LPC I/F—D31:F0)

Offset Address: E0h–E1h  
Default Value: 0009h

Attribute: RO  
Size: 16 bits  
Power Well: Core

Bit	Description
15:8	<b>Next Item Pointer (NEXT)</b> —RO. Configuration offset of the next Capability Item. 00h indicates the last item in the Capability List.
7:0	<b>Capability ID</b> —RO. Indicates a Vendor Specific Capability

### 10.1.35 FDLEN—Feature Detection Capability Length Register (LPC I/F—D31:F0)

Offset Address: E2h  
Default Value: 0Ch

Attribute: RO  
Size: 8 bits  
Power Well: Core

Bit	Description
7:0	<b>Capability Length</b> —RO. Indicates the length of this Vendor Specific capability, as required by PCI Specification.

### 10.1.36 FDVER—Feature Detection Version Register (LPC I/F—D31:F0)

Offset Address: E3h  
Default Value: 10h

Attribute: RO  
Size: 8 bits  
Power Well: Core

Bit	Description
7:4	<b>Vendor-Specific Capability ID</b> —RO. A value of 1h in this 4-bit field identifies this Capability as Feature Detection Type. This field allows software to differentiate the Feature Detection Capability from other Vendor-Specific capabilities.
3:0	<b>Capability Version</b> —RO. This field indicates the version of the Feature Detection capability.

### 10.1.37 FVECIDX—Feature Vector Index Register (LPC I/F—D31:F0)

Offset Address: E4h–E7h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits  
Power Well: Core

Bit	Description
31:6	Reserved
5:2	<b>Index (IDX)</b> —R/W. This field is a 4-bit index pointer into the 64-byte Feature Vector space. Data is read from the FVECD register. This points to a DWord register.
1:0	Reserved

## 10.1.38 FVECD—Feature Vector Data Register (LPC I/F—D31:F0)

Offset Address: E8h–EBh  
 Default Value: See Description  
 Attribute: RO  
 Size: 32 bits  
 Power Well: Core

Bit	Description
31:0	<b>Data (DATA)</b> —RO. 32-bit data value that is read from the Feature Vector offset pointed to by FVECIDX.

## 10.1.39 Feature Vector Space

### 10.1.39.1 FVECO—Feature Vector Register 0

FVECIDX.IDX: 0000b  
 Default Value: See Description  
 Attribute: RO  
 Size: 32 bits  
 Power Well: Core

Bit	Description															
31:26	Reserved															
25	<b>SATA Port 3 6Gb/s Capability</b> —RO 0 = Capable 1 = Disabled															
24	<b>SATA Port 2 6Gb/s Capability</b> —RO 0 = Capable 1 = Disabled															
23:21	Reserved															
20	<b>SATA Ports 2 and 3</b> —RO 0 = Ports Enabled 1 = Ports Disabled															
19:18	<b>RAID Capability</b> —RO <table> <thead> <tr> <th>Bit 19</th> <th>Bit 18</th> <th>Capability</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>No RAID</td> </tr> <tr> <td>0</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>0</td> <td>RAID 0/1/5/10</td> </tr> <tr> <td>1</td> <td>1</td> <td>RAID 0/1/5/10 and Intel® Smart Response Technology</td> </tr> </tbody> </table>	Bit 19	Bit 18	Capability	0	0	No RAID	0	1	Reserved	1	0	RAID 0/1/5/10	1	1	RAID 0/1/5/10 and Intel® Smart Response Technology
Bit 19	Bit 18	Capability														
0	0	No RAID														
0	1	Reserved														
1	0	RAID 0/1/5/10														
1	1	RAID 0/1/5/10 and Intel® Smart Response Technology														
17:16	<b>SATA Port 4 PCIe* Port 6 Lane 0 Mode</b> —RO 00 = Statically Assign to SATA Port 4 01 = Statically Assign to PCIe* Port 6 Lane 0 10 = Assign based on PCH soft strap SATAP4_PCIEP6L0_MODE 11 = Undefined															
15:14	<b>SATA Port 3 PCIe* Port 6 Lane 1 Mode</b> —RO 00 = Statically Assign to SATA Port 3 01 = Statically Assign to PCIe* Port 6 Lane 1 10 = Assign based on PCH soft strap SATAP3_PCIEP6L1_MODE 11 = Undefined															

Bit	Description
13:12	<b>SATA Port 1 PCIe* Port 6 Lane 2 Mode</b> —RO 00 = Statically Assign to SATA Port 1 01 = Statically Assign to PCIe* Port 6 Lane 2 10 = Assign based on PCH soft strap SATAP1_PCIEP6L2_MODE 11 = Undefined
11:10	<b>SATA Port 0 PCIe* Port 6 Lane 3 Mode</b> —RO 00 = Statically Assign to SATA Port 0 01 = Statically Assign to PCIe* Port 6 Lane 3 10 = Assign based on PCH soft strap SATAP0_PCIEP6L3_MODE 11 = Undefined
9:5	Reserved
4	<b>Intel® PCI Express* Storage Technology</b> —RO 0 = Capable 1 = Disabled
3:0	Reserved

#### 10.1.39.2 FVEC1—Feature Vector Register 1

FVECIDX.IDX: 0001b      Attribute: RO  
 Default Value: See Description      Size: 32 bits  
                                     Power Well: Core

Bit	Description
31:0	Reserved

#### 10.1.39.3 FVEC2—Feature Vector Register 2

FVECIDX.IDX: 0010b      Attribute: RO  
 Default Value: See Description      Size: 32 bits  
                                     Power Well: Core

Bit	Description
31:21	Reserved
20	<b>USB Redirect (USBr) Capability</b> —RO 0 = Capable 1 = Disabled
19:0	Reserved

#### 10.1.39.4 FVEC3—Feature Vector Register 3

FVECIDX.IDX: 0011b      Attribute: RO  
 Default Value: See Description      Size: 32 bits  
                                     Power Well: Core

Bit	Description
31:0	Reserved

### 10.1.40 RCBA—Root Complex Base Address Register (LPC I/F—D31:F0)

Offset Address: F0–F3h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:14	<b>Base Address (BA)</b> —R/W. Base Address for the root complex register block decode range. This address is aligned on a 16KB boundary.
13:1	Reserved
0	<b>Enable (EN)</b> —R/W. When set, this bit enables the range specified in BA to be claimed as the Root Complex Register Block.

## 10.2 Timer I/O Registers

Port	Aliases	Register Name	Default Value	Type
40h	50h	Counter 0 Interval Time Status Byte Format	0XXXXXXXXb	RO
		Counter 0 Counter Access Port	Undefined	R/W
41h	51h	Counter 1 Interval Time Status Byte Format	0XXXXXXXXb	RO
		Counter 1 Counter Access Port	Undefined	R/W
42h	52h	Counter 2 Interval Time Status Byte Format	0XXXXXXXXb	RO
		Counter 2 Counter Access Port	Undefined	R/W
43h	53h	Timer Control Word	Undefined	WO
		Timer Control Word	XXXXXXXX0b	WO
		Counter Latch Command	X0h	WO



### 10.2.1 TCW—Timer Control Word Register

I/O Address: 43h  
Default Value: All bits undefined

Attribute: WO  
Size: 8 bits

This register is programmed prior to any counter being accessed to specify counter modes. Following part reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

Bit	Description														
7:6	<b>Counter Select</b> —WO. The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1. 00 = Counter 0 select 01 = Counter 1 select 10 = Counter 2 select 11 = Read Back Command														
5:4	<b>Read/Write Select</b> —WO. These bits are the read/write control bits. The actual counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2). 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB														
3:1	<b>Counter Mode Selection</b> —WO. These bits select one of six possible modes of operation for the selected counter.														
	<table> <thead> <tr> <th>Bit Value</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Mode 0 Out signal on end of count (=0)</td> </tr> <tr> <td>001b</td> <td>Mode 1 Hardware retriggerable one-shot</td> </tr> <tr> <td>x10b</td> <td>Mode 2 Rate generator (divide by n counter)</td> </tr> <tr> <td>x11b</td> <td>Mode 3 Square wave output</td> </tr> <tr> <td>100b</td> <td>Mode 4 Software triggered strobe</td> </tr> <tr> <td>101b</td> <td>Mode 5 Hardware triggered strobe</td> </tr> </tbody> </table>	Bit Value	Mode	000b	Mode 0 Out signal on end of count (=0)	001b	Mode 1 Hardware retriggerable one-shot	x10b	Mode 2 Rate generator (divide by n counter)	x11b	Mode 3 Square wave output	100b	Mode 4 Software triggered strobe	101b	Mode 5 Hardware triggered strobe
Bit Value	Mode														
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x10b	Mode 2 Rate generator (divide by n counter)														
x11b	Mode 3 Square wave output														
100b	Mode 4 Software triggered strobe														
101b	Mode 5 Hardware triggered strobe														
0	Binary/BCD Countdown Select—WO. 0 = Binary countdown is used. The largest possible binary count is $2^{16}$ . 1 = Binary coded decimal (BCD) count is used. The largest possible BCD count is $10^4$ .														

There are two special commands that can be issued to the counters through this register – the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined. These register formats are described in the following two sub-sections.



### RDBK\_CMD—Read Back Command

The Read Back Command is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read. Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Bit	Description
7:6	<b>Read Back Command.</b> Must be 11 to select the Read Back Command
5	<b>Latch Count of Selected Counters.</b> 0 = Current count value of the selected counters will be latched 1 = Current count will not be latched
4	<b>Latch Status of Selected Counters.</b> 0 = Status of the selected counters will be latched 1 = Status will not be latched
3	<b>Counter 2 Select.</b> 1 = Counter 2 count and/or status will be latched
2	<b>Counter 1 Select.</b> 1 = Counter 1 count and/or status will be latched
1	<b>Counter 0 Select.</b> 1 = Counter 0 count and/or status will be latched.
0	Reserved. Must be 0.

### LTCH\_CMD—Counter Latch Command

The Counter Latch Command latches the current count value. This command is used to insure that the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2). The count must be read according to the programmed format; that is, if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

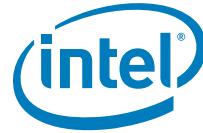
Bit	Description
7:6	<b>Counter Selection.</b> These bits select the counter for latching. If "11" is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Counter 1 10 = Counter 2
5:4	<b>Counter Latch Command.</b> 00 = Selects the Counter Latch Command.
3:0	Reserved, must be 0.

## 10.2.2 SBYTE\_FMT—Interval Timer Status Byte Format Register

I/O Address: Counter 0 = 40h,  
                   Counter 1 = 41h,                   Attribute:            RO  
                   Counter 2 = 42h                   Size:                8 bits per counter  
 Default Value: Bits[6:0] undefined, Bit 7=0

Each counter's status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2) returns the status byte. The status byte returns the following:

Bit	Description
7	<b>Counter OUT Pin State</b> —RO. 0 = OUT pin of the counter is also a 0 1 = OUT pin of the counter is also a 1
6	<b>Count Register Status</b> —RO. This bit indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the counter mode; however, until the count is loaded into the counting element (CE), the count value will be incorrect. 0 = Count has been transferred from CR to CE and is available for reading. 1 = Null Count. Count has not been transferred from CR to CE and is not yet available for reading.
5:4	<b>Read/Write Selection Status</b> —RO. These bits reflect the read/write selection made through bits 5:4 of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection. 00 = Counter Latch Command 01 = Read/Write Least Significant Byte (LSB) 10 = Read/Write Most Significant Byte (MSB) 11 = Read/Write LSB then MSB
3:1	<b>Mode Selection Status</b> —RO. These bits return the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above. 000 = Mode 0—Out signal on end of count (=0) 001 = Mode 1—Hardware retriggerable one-shot x10 = Mode 2—Rate generator (divide by n counter) x11 = Mode 3—Square wave output 100 = Mode 4—Software triggered strobe 101 = Mode 5—Hardware triggered strobe
0	<b>Countdown Type Status</b> —RO. This bit reflects the current countdown type. 0 = Binary countdown 1 = Binary Coded Decimal (BCD) countdown.



### 10.2.3 Counter Access Ports Register

I/O Address:	Counter 0 – 40h, Counter 1 – 41h, Counter 2 – 42h	Attribute:	R/W
Default Value:	All bits undefined	Size:	8 bits

Bit	Description
7:0	<b>Counter Port</b> —R/W. Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.

## 10.3 8259 Interrupt Controller (PIC) Registers

### 10.3.1 Interrupt Controller I/O MAP

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ 0–7), and at A0h and A1h for the slave controller (IRQ 8–13). These registers have multiple functions, depending upon the data written to them. [Table 10-2](#) shows the different register possibilities for each address.

**Table 10-2. Programmable Interrupt Controller (PIC) Registers**

Port	Aliases	Register Name	Default Value	Type
20h	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch	Master PIC ICW1 INIT. Cmd Word 1	Undefined	WO
		Master PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Master PIC OCW3 Op Ctrl Word 3	X01XXX10b	WO
21h	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh	Master PIC ICW2 INIT. Cmd Word 2	Undefined	WO
		Master PIC ICW3 INIT. Cmd Word 3	Undefined	WO
		Master PIC ICW4 INIT. Cmd Word 4	01h	WO
		Master PIC OCW1 Op Ctrl Word 1	00h	R/W
A0h	A4h, A8h, ACh, B0h, B4h, B8h, BCh	Slave PIC ICW1 INIT. Cmd Word 1	Undefined	WO
		Slave PIC OCW2 Op Ctrl Word 2	001XXXXXb	WO
		Slave PIC OCW3 Op Ctrl Word 3	X01XXX10b	WO
A1h	A5h, A9h, ADh, B1h, B5h, B9h, BDh	Slave PIC ICW2 INIT. Cmd Word 2	Undefined	WO
		Slave PIC ICW3 INIT. Cmd Word 3	Undefined	WO
		Slave PIC ICW4 INIT. Cmd Word 4	01h	WO
		Slave PIC OCW1 Op Ctrl Word 1	00h	R/W
4D0h	–	Master PIC Edge/Level Triggered	00h	R/W
4D1h	–	Slave PIC Edge/Level Triggered	00h	R/W

**Note:**

Refer to the **Note** addressing active-low interrupt sources in the 8259 Interrupt Controllers section ([Section 5.6](#)).

### 10.3.2 ICW1—Initialization Command Word 1 Register

Offset Address: Master Controller – 20h      Attribute: WO  
                  Slave Controller – A0h      Size: 8 bits/controller  
Default Value: All bits undefined

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence during which the following occurs:

1. The Interrupt Mask register is cleared.
2. IRQ7 input is assigned priority 7.
3. The slave mode address is set to 7.
4. Special mask mode is cleared and Status Read is set to IRR.

Once this write occurs, the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Bit	Description
7:5	<b>ICW/OCW Select</b> —WO. These bits are MCS-85 specific, and not needed. 000 = Should be programmed to "000"
4	<b>ICW/OCW Select</b> —WO. 1 = This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
3	<b>Edge/Level Bank Select (LTIM)</b> —WO. Disabled. Replaced by the edge/level triggered control registers (ELCR, D31:F0:4D0h, D31:F0:4D1h).
2	<b>ADI</b> —WO. 0 = Ignored for the PCH. Should be programmed to 0.
1	<b>Single or Cascade (SNGL)</b> —WO. 0 = Must be programmed to a 0 to indicate two controllers operating in cascade mode.
0	<b>ICW4 Write Required (IC4)</b> —WO. 1 = This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.



### 10.3.3 ICW2—Initialization Command Word 2 Register

Offset Address: Master Controller – 21h      Attribute: WO  
                   Slave Controller – A1h      Size: 8 bits/controller  
     Default Value: All bits undefined

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits 7:3 is used by the processor to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Bit	Description																													
7:3	<b>Interrupt Vector Base Address</b> —WO. Bits 7:3 define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.																													
2:0	<b>Interrupt Request Level</b> —WO. When writing ICW2, these bits should all be 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three-bit binary code: <table> <thead> <tr> <th>Code</th> <th>Master Interrupt</th> <th>Slave Interrupt</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>IRQ0</td> <td>IRQ8</td> </tr> <tr> <td>001b</td> <td>IRQ1</td> <td>IRQ9</td> </tr> <tr> <td>010b</td> <td>IRQ2</td> <td>IRQ10</td> </tr> <tr> <td>011b</td> <td>IRQ3</td> <td>IRQ11</td> </tr> <tr> <td>100b</td> <td>IRQ4</td> <td>IRQ12</td> </tr> <tr> <td>101b</td> <td>IRQ5</td> <td>IRQ13</td> </tr> <tr> <td>110b</td> <td>IRQ6</td> <td>IRQ14</td> </tr> <tr> <td>111b</td> <td>IRQ7</td> <td>IRQ15</td> </tr> </tbody> </table>			Code	Master Interrupt	Slave Interrupt	000b	IRQ0	IRQ8	001b	IRQ1	IRQ9	010b	IRQ2	IRQ10	011b	IRQ3	IRQ11	100b	IRQ4	IRQ12	101b	IRQ5	IRQ13	110b	IRQ6	IRQ14	111b	IRQ7	IRQ15
Code	Master Interrupt	Slave Interrupt																												
000b	IRQ0	IRQ8																												
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100b	IRQ4	IRQ12																												
101b	IRQ5	IRQ13																												
110b	IRQ6	IRQ14																												
111b	IRQ7	IRQ15																												

### 10.3.4 ICW3—Master Controller Initialization Command Word 3 Register

Offset Address: 21h      Attribute: WO  
     Default Value: All bits undefined      Size: 8 bits

Bit	Description	
7:3	0 = These bits must be programmed to 0.	
2	<b>Cascaded Interrupt Controller IRQ Connection</b> —WO. This bit indicates that the slave controller is cascaded on IRQ2. When IRQ8#–IRQ15 is asserted, it goes through the slave controller's priority resolver. The slave controller's INTR output onto IRQ2. IRQ2 then goes through the master controller's priority solver. If it wins, the INTR signal is asserted to the processor, and the returning interrupt acknowledge returns the interrupt vector for the slave controller. 1 = This bit must always be programmed to a 1.	
1:0	0 = These bits must be programmed to 0.	

### 10.3.5 ICW3—Slave Controller Initialization Command Word 3 Register

Offset Address: A1h Attribute: WO  
 Default Value: All bits undefined Size: 8 bits

Bit	Description
7:3	0 = These bits must be programmed to 0.
2:0	<b>Slave Identification Code</b> —WO. These bits are compared against the slave identification code broadcast by the master controller from the trailing edge of the first internal INTA# pulse to the trailing edge of the second internal INTA# pulse. These bits must be programmed to 02h to match the code broadcast by the master controller. When 02h is broadcast by the master controller during the INTA# sequence, the slave controller assumes responsibility for broadcasting the interrupt vector.

### 10.3.6 ICW4—Initialization Command Word 4 Register

Offset Address: Master Controller – 021h Attribute: WO  
 Slave Controller – 0A1h Size: 8 bits  
 Default Value: 01h

Bit	Description
7:5	0 = These bits must be programmed to 0.
4	<b>Special Fully Nested Mode (SFNM)</b> —WO. 0 = Should normally be disabled by writing a 0 to this bit. 1 = Special fully nested mode is programmed.
3	<b>Buffered Mode (BUF)</b> —WO. 0 = Must be programmed to 0 for the PCH. This is non-buffered mode.
2	<b>Master/Slave in Buffered Mode</b> —WO. Not used. 0 = Should always be programmed to 0.
1	<b>Automatic End of Interrupt (AEOI)</b> —WO. 0 = This bit should normally be programmed to 0. This is the normal end of interrupt. 1 = Automatic End of Interrupt (AEOI) mode is programmed.
0	<b>Microprocessor Mode</b> —WO. 1 = Must be programmed to 1 to indicate that the controller is operating in an Intel Architecture-based system.

### 10.3.7 OCW1—Operational Control Word 1 (Interrupt Mask) Register

Offset Address: Master Controller – 021h      Attribute: R/W  
 Slave Controller – 0A1h      Size: 8 bits  
 Default Value: 00h

Bit	Description
7:0	<b>Interrupt Request Mask</b> —R/W. When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests will again be accepted by the controller. Masking IRQ2 on the master controller will also mask the interrupt requests from the slave controller.

### 10.3.8 OCW2—Operational Control Word 2 Register

Offset Address: Master Controller – 020h      Attribute: WO  
 Slave Controller – 0A0h      Size: 8 bits  
 Default Value: Bit[4:0]=undefined, Bit[7:5]=001

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	<b>Rotate and EOI Codes</b> (R, SL, EOI)—WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = Rotate in Auto EOI Mode (Clear) 001 = Non-specific EOI command 010 = No Operation 011 = Specific EOI Command 100 = Rotate in Auto EOI Mode (Set) 101 = Rotate on Non-Specific EOI Command 110 = Set Priority Command 111 = Rotate on Specific EOI Command L0 – L2 Are Used
4:3	<b>OCW2 Select</b> —WO. When selecting OCW2, bits 4:3 = 00
2:0	<b>Interrupt Level Select</b> (L2, L1, L0)—WO. L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined below, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case.

Code	Interrupt Level	Code	Interrupt Level
000b	IRQ0/8	000b	IRQ4/12
001b	IRQ1/9	001b	IRQ5/13
010b	IRQ2/10	010b	IRQ6/14
011b	IRQ3/11	011b	IRQ7/15

### 10.3.9 OCW3—Operational Control Word 3 Register

Offset Address: Master Controller – 020h      Attribute: WO  
                   Slave Controller – 0A0h      Size: 8 bits  
  Default Value: Bit[6,0]=0, Bit[7,4:2]=undefined,  
                   Bit[5,1]=1

Bit	Description
7	Reserved. Must be 0.
6	<b>Special Mask Mode (SMM)</b> —WO 1 = The Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/disabling of the other channel's mask bits. Bit 5, the ESMM bit, must be set for this bit to have any meaning.
5	<b>Enable Special Mask Mode (ESMM)</b> —WO 0 = Disable. The SMM bit becomes a "don't care". 1 = Enable the SMM bit to set or reset the Special Mask Mode.
4:3	<b>OCW3 Select</b> —WO. When selecting OCW3, bits 4:3 = 01
2	<b>Poll Mode Command</b> —WO 0 = Disable. Poll Command is not issued. 1 = Enable. The next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
1:0	<b>Register Read Command</b> —WO. These bits provide control for reading the In Service Register (ISR) and the Interrupt Request Register (IRR). When bit 1=0, bit 0 will not affect the register read selection. When bit 1=1, bit 0 selects the register status returned following an OCW3 read. If bit 0=0, the IRR will be read. If bit 0=1, the ISR will be read. Following ICW initialization, the default OCW3 port address read will be "read IRR". To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 = No Action 01 = No Action 10 = Read IRQ Register 11 = Read IS Register

### 10.3.10 ELCR1—Master Controller Edge/Level Triggered Register

Offset Address: 4D0h  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The cascade channel, IRQ2, the heart beat timer (IRQ0), and the keyboard controller (IRQ1), cannot be put into level mode.

Bit	Description
7	<b>IRQ7 ECL</b> —R/W 0 = Edge 1 = Level
6	<b>IRQ6 ECL</b> —R/W 0 = Edge 1 = Level.
5	<b>IRQ5 ECL</b> —R/W 0 = Edge 1 = Level
4	<b>IRQ4 ECL</b> —R/W 0 = Edge 1 = Level
3	<b>IRQ3 ECL</b> —R/W 0 = Edge 1 = Level
2:0	Reserved, must be 0.

### 10.3.11 ELCR2—Slave Controller Edge/Level Triggered Register

Offset Address: 4D1h  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

In edge mode, (bit[x] = 0), the interrupt is recognized by a low to high transition. In level mode (bit[x] = 1), the interrupt is recognized by a high level. The real-time clock, IRQ8#, and the floating point error interrupt, IRQ13, cannot be programmed for level mode.

Bit	Description
7	<b>IRQ15 ECL</b> —R/W 0 = Edge 1 = Level
6	<b>IRQ14 ECL</b> —R/W 0 = Edge 1 = Level
5	Reserved, must be 0.
4	<b>IRQ12 ECL</b> —R/W 0 = Edge 1 = Level
3	<b>IRQ11 ECL</b> —R/W 0 = Edge 1 = Level
2	<b>IRQ10 ECL</b> —R/W 0 = Edge 1 = Level
1	<b>IRQ9 ECL</b> —R/W 0 = Edge 1 = Level
0	Reserved, must be 0.

## 10.4 Advanced Programmable Interrupt Controller (APIC)

### 10.4.1 APIC Register Map

The APIC is accessed using an indirect addressing scheme. Two registers are visible by software for manipulation of most of the APIC registers. These registers are mapped into memory space. The address bits 19:12 of the address range are programmable through bits 7:0 of OIC register (Chipset Configuration Registers:Offset 31FEh). The registers are shown in [Table 10-3](#).

**Table 10-3. APIC Direct Registers**

Address	Mnemonic	Register Name	Size	Attribute
FEC_ _0000h	IND	Index	8 bits	R/W
FEC_ _0010h	DAT	Data	32 bits	R/W
FEC_ _0040h	EOIR	EOI	32 bits	WO

[Table 10-4](#) lists the registers that can be accessed within the APIC using the Index Register. When accessing these registers, accesses must be done one DWord at a time. For example, software should never access byte 2 from the Data register before accessing bytes 0 and 1. The hardware will not attempt to recover from a bad programming model in this case.

**Table 10-4. APIC Indirect Registers**

Index	Mnemonic	Register Name	Size	Attribute
00h	ID	Identification	32 bits	R/W
01h	VER	Version	32 bits	RO
02–0Fh	—	Reserved	—	RO
10–11h	REDIR_TBL0	Redirection Table 0	64 bits	R/W, RO
12–13h	REDIR_TBL1	Redirection Table 1	64 bits	R/W, RO
...	...	...	...	...
3E–3Fh	REDIR_TBL23	Redirection Table 23	64 bits	R/W, RO
40–41h	REDIR_TBL24	Redirection Table 24	64 bits	R/W, RO
42–43h	REDIR_TBL25	Redirection Table 25	64 bits	R/W, RO
...	...	...	...	...
5E–5Fh	REDIR_TBL39	Redirection Table 39	64 bits	R/W, RO
60–FFh	—	Reserved	—	RO

## 10.4.2 IND—Index Register

Memory Address FEC\_ \_0000h      Attribute: R/W  
 Default Value: 00h      Size: 8 bits

The Index Register will select which APIC indirect register to be manipulated by software. The selector values for the indirect registers are listed in [Table 10-4](#). Software will program this register to select the desired APIC internal register.

Bit	Description
7:0	<b>APIC Index</b> —R/W. This is an 8-bit pointer into the I/O APIC register table.

## 10.4.3 DAT—Data Register

Memory Address FEC\_ \_0000h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

This is a 32-bit register specifying the data to be read or written to the register pointed to by the Index register. This register can only be accessed in DWord quantities.

Bit	Description
7:0	<b>APIC Data</b> —R/W. This is a 32-bit register for the data to be read or written to the APIC indirect register ( <a href="#">Figure 10-4</a> ) pointed to by the Index register (Memory Address FEC0_0000h).

## 10.4.4 EOIR—EOI Register

Memory Address FEC\_ \_0000h      Attribute: WO  
 Default Value: N/A      Size: 32 bits

The EOI register is present to provide a mechanism to maintain the level-triggered semantics for level-triggered interrupts issued on the parallel bus.

When a write is issued to this register, the I/O APIC will check the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the RemoteIRR bit (Index Offset 10h, bit 14) for that I/O Redirection Entry will be cleared.

**Note:** If multiple I/O Redirection entries, for any reason, assign the same vector for more than one interrupt input, each of those entries will have the RemoteIRR bit reset to 0. The interrupt, which was prematurely reset, will not be lost because if its input remained active when the RemoteIRR bit was cleared, the interrupt will be reissued and serviced at a later time. Only bits 7:0 are actually used. Bits 31:8 are ignored by the PCH.

**Note:** To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.

Bit	Description
31:8	Reserved. To provide for future expansion, the processor should always write a value of 0 to Bits 31:8.
7:0	<b>Redirection Entry Clear</b> —WO. When a write is issued to this register, the I/O APIC will check this field, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the RemoteIRR bit for that I/O Redirection Entry will be cleared.

## 10.4.5 ID—Identification Register

Index Offset: 00h Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

The APIC ID serves as a physical name of the APIC. The APIC bus arbitration ID for the APIC is derived from its I/O APIC ID. This register is reset to 0 on power-up reset.

Bit	Description
31:28	Reserved
27:24	<b>APIC ID</b> —R/W. Software must program this value before using the APIC.
23:16	Reserved
15	Scratchpad Bit.
14:0	Reserved

## 10.4.6 VER—Version Register

Index Offset: 01h Attribute: RO, R/WO  
 Default Value: 00170020h Size: 32 bits

Each I/O APIC contains a hardwired Version Register that identifies different implementation of APIC and their versions. The maximum redirection entry information is also in this register to let software know how many interrupt are supported by this APIC.

Bit	Description
31:24	Reserved
23:16	<b>Maximum Redirection Entries (MRE)</b> —R/WO. This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. It is equal to the number of interrupt input pins minus one and is in the range 0 through 239. In the PCH this field defaults to 17h to indicate 24 interrupts. BIOS must write to this field after PLTRST# to lockdown the value. This allows BIOS to use some of the entries for its own purpose and thus advertising fewer IOxAPIC Redirection Entries to the operating system. BIOS may program this field up to 27h (maximum 40 entries).
15	<b>Pin Assertion Register Supported (PRQ)</b> —RO. Indicate that the IOxAPIC does not implement the Pin Assertion register.
14:8	Reserved
7:0	<b>Version (VS)</b> —RO. This is a version number that identifies the implementation version.

### 10.4.7 REDIR\_TBL—Redirection Table Register

Index Offset: 10h–11h (vector 0) through 5E–5Fh (vector 39) Attribute: R/W, RO  
 Default Value: Bit 16 = 1. All other bits undefined Size: 64 bits each, (accessed as two, 32-bit quantities)

The Redirection Table has a dedicated entry for each interrupt input pin. The information in the Redirection Table is used to translate the interrupt manifestation on the corresponding interrupt pin into an APIC message.

The APIC will respond to an edge triggered interrupt as long as the interrupt is held until after the acknowledge cycle has begun. Once the interrupt is detected, a delivery status bit internally to the I/O APIC is set. The state machine will step ahead and wait for an acknowledgment from the APIC unit that the interrupt message was sent. Only then will the I/O APIC be able to recognize a new edge on that interrupt pin. That new edge will only result in a new invocation of the handler if its acceptance by the destination APIC causes the Interrupt Request register bit to go from 0 to 1. (In other words, if the interrupt was not already pending at the destination.)

**Note:** For entries 24:39, refer to OIC.IOA24\_39\_D register (RCBA+31FEh).

Bit	Description
63:56	<b>Destination</b> —R/W. If bit 11 of this entry is 0 (Physical), then bits 59:56 specifies an APIC ID. In this case, bits 63:59 should be programmed by software to 0. If bit 11 of this entry is 1 (Logical), then bits 63:56 specify the logical destination address of a set of processors.
55:48	<b>Extended Destination ID (EDID)</b> —RO. These bits are sent to a local APIC only when in Processor System Bus mode. They become bits 11:4 of the address.
47:17	Reserved
16	<b>Mask</b> —R/W. 0 = Not masked: An edge or level on this interrupt pin results in the delivery of the interrupt to the destination. 1 = Masked: Interrupts are not delivered nor held pending. Setting this bit after the interrupt is accepted by a local APIC has no effect on that interrupt. This behavior is identical to the device withdrawing the interrupt before it is posted to the processor. It is software's responsibility to deal with the case where the mask bit is set after the interrupt message has been accepted by a local APIC unit but before the interrupt is dispensed to the processor.
15	<b>Trigger Mode</b> —R/W. This field indicates the type of signal on the interrupt pin that triggers an interrupt. 0 = Edge triggered. 1 = Level triggered.
14	<b>Remote IRR</b> —R/W. This bit is used for level triggered interrupts; its meaning is undefined for edge triggered interrupts. 0 = Reset when an EOI message is received from a local APIC. 1 = Set when Local APIC/s accept the level interrupt sent by the I/O APIC.
13	<b>Interrupt Input Pin Polarity</b> —R/W. This bit specifies the polarity of each interrupt signal connected to the interrupt pins. 0 = Active high. 1 = Active low.
12	<b>Delivery Status</b> —RO. This field contains the current status of the delivery of this interrupt. Writes to this bit have no effect. 0 = Idle. No activity for this interrupt. 1 = Pending. Interrupt has been injected, but delivery is not complete.



Bit	Description
11	<b>Destination Mode</b> —R/W. This field determines the interpretation of the Destination field. 0 = Physical. Destination APIC ID is identified by bits 59:56. 1 = Logical. Destinations are identified by matching bit 63:56 with the Logical Destination in the Destination Format register and Logical Destination register in each Local APIC.
10:8	<b>Delivery Mode</b> —R/W. This field specifies how the APICs listed in the destination field should act upon reception of this signal. Certain Delivery Modes will only operate as intended when used in conjunction with a specific trigger mode. These encodings are listed in the <b>Note</b> below.
7:0	<b>Vector</b> —R/W. This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

**Note:** Delivery Mode encoding:

- 000 = Fixed. Deliver the signal on the INTR signal of all processor cores listed in the destination. Trigger Mode can be edge or level.
- 001 = Lowest Priority. Deliver the signal on the INTR signal of the processor core that is executing at the lowest priority among all the processors listed in the specified destination. Trigger Mode can be edge or level.
- 010 = SMI (System Management Interrupt). Requires the interrupt to be programmed as edge triggered. The vector information is ignored but must be programmed to all 0s for future compatibility: **not supported**
- 011 = Reserved
- 100 = NMI. Deliver the signal on the NMI signal of all processor cores listed in the destination. Vector information is ignored. NMI is treated as an edge triggered interrupt even if it is programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The NMI delivery mode does not set the RIRR bit. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the NMI pin is reached again, the interrupt will be sent again: **not supported**
- 101 = INIT. Deliver the signal to all processor cores listed in the destination by asserting the INIT signal. All addressed local APICs will assume their INIT state. INIT is always treated as an edge triggered interrupt even if programmed as level triggered. For proper operation this redirection table entry must be programmed to edge triggered. The INIT delivery mode does not set the RIRR bit. If the redirection table is incorrectly set to level, the loop count will continue counting through the redirection table addresses. Once the count for the INIT pin is reached again, the interrupt will be sent again: **not supported**
- 110 = Reserved
- 111 = ExtINT. Deliver the signal to the INTR signal of all processor cores listed in the destination as an interrupt that originated in an externally connected 8259A compatible interrupt controller. The INTA cycle that corresponds to this ExtINT delivery will be routed to the external controller that is expected to supply the vector. Requires the interrupt to be programmed as edge triggered.

## 10.5 Real Time Clock Registers

### 10.5.1 I/O Register Address Map

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A–D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM, and will be accessible even when the RTC module is disabled (using the RTC configuration register). Registers A–D do not physically exist in the RAM.

All data movement between the host processor and the real-time clock is done through registers mapped to the standard I/O space. The register map is shown in the following table.

**Table 10-5. RTC I/O Registers**

I/O Locations	If U128E bit = 0	Function
70h and 74h	Also alias to 72h and 76h	Real-Time Clock (Standard RAM) Index Register
71h and 75h	Also alias to 73h and 77h	Real-Time Clock (Standard RAM) Target Register
72h and 76h		Extended RAM Index Register (if enabled)
73h and 77h		Extended RAM Target Register (if enabled)

**Notes:**

1. I/O locations 70h and 71h are the standard legacy location for the real-time clock. The map for this bank is shown in [Table 10-6](#). Locations 72h and 73h are for accessing the extended RAM. The extended RAM bank is also accessed using an indexed scheme. I/O address 72h is used as the address pointer and I/O address 73h is used as the data register. Index addresses above 127h are not valid. If the extended RAM is not needed, it may be disabled.
2. Software must preserve the value of bit 7 at I/O addresses 70h. When writing to this address, software must first read the value, and then write the same value for bit 7 during the sequential address write. Port 70h is not directly readable. The only way to read this register is through Alt Access mode. Although RTC Index bits 6:0 are readable from port 74h, bit 7 will always return 0. If the NMI# enable is not changed during normal operation, software can alternatively read this bit once and then retain the value for all subsequent writes to port 70h.

## 10.5.2 Indexed Registers

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70/71h or 72/73h), as shown in the following table.

**Table 10-6. RTC (Standard) RAM Bank**

Index	Name
00h	Seconds
01h	Seconds Alarm
02h	Minutes
03h	Minutes Alarm
04h	Hours
05h	Hours Alarm
06h	Day of Week
07h	Day of Month
08h	Month
09h	Year
0Ah	Register A
0Bh	Register B
0Ch	Register C
0Dh	Register D
0Eh–7Fh	114 Bytes of User RAM

### 10.5.2.1 RTC\_REGA—Register A

RTC Index:	0A	Attribute:	R/W
Default Value:	Undefined	Size:	8 bit
Lockable:	No	Power Well:	RTC

This register is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other PCH reset signal.

Bit	Description
7	<b>Update In Progress (UIP)</b> —R/W. This bit may be monitored as a status flag. 0 = The update cycle will not start for at least 488 $\mu$ s. The time, calendar, and alarm information in RAM is always available when the UIP bit is 0. 1 = The update is soon to occur or is in progress.
6:4	<b>Division Chain Select (DV[2:0])</b> —R/W. These three bits control the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal. 010 = Normal Operation 11X = Divider Reset 101 = Bypass 15 stages (test mode only) 100 = Bypass 10 stages (test mode only) 011 = Bypass 5 stages (test mode only) 001 = Invalid 000 = Invalid
3:0	<b>Rate Select (RS[3:0])</b> —R/W. Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if the PIE bit is set in Register B. Otherwise, this tap will set the PF flag of Register C. If the periodic interrupt is not to be used, these bits should all be set to 0. RS3 corresponds to bit 3. 0000 = Interrupt never toggles 0001 = 3.90625 ms 0010 = 7.8125 ms 0011 = 122.070 $\mu$ s 0100 = 244.141 $\mu$ s 0101 = 488.281 $\mu$ s 0110 = 976.5625 $\mu$ s 0111 = 1.953125 ms 1000 = 3.90625 ms 1001 = 7.8125 ms 1010 = 15.625 ms 1011 = 31.25 ms 1100 = 62.5 ms 1101 = 125 ms 1110 = 250 ms 1111 = 500 ms

### 10.5.2.2 RTC\_REGB—Register B (General Configuration)

RTC Index: 0Bh Attribute: R/W  
 Default Value: U0U00UUU (U: Undefined) Size: 8 bit  
 Lockable: No Power Well: RTC

Bit	Description
7	<b>Update Cycle Inhibit (SET)</b> —R/W. Enables/Inhibits the update cycles. This bit is not affected by RSMRST# nor any other reset signal. 0 = Update cycle occurs normally once each second. 1 = A current update cycle will abort and subsequent update cycles will not occur until SET is returned to 0. When SET is 1, the BIOS may initialize time and calendar bytes safely. <b>Note:</b> This bit should be set then cleared early in BIOS POST after each power-up directly after coin-cell battery insertion.
6	<b>Periodic Interrupt Enable (PIE)</b> —R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur with a time base set with the RS bits of register A.
5	<b>Alarm Interrupt Enable (AIE)</b> —R/W. This bit is cleared by RTCRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the AF is set by an alarm match from the update cycle. An alarm can occur once a second, one an hour, once a day, or one a month.
4	<b>Update-Ended Interrupt Enable (UIE)</b> —R/W. This bit is cleared by RSMRST#, but not on any other reset. 0 = Disable. 1 = Enable. Allows an interrupt to occur when the update cycle ends.
3	<b>Square Wave Enable (SQWE)</b> —R/W. This bit serves no function in the PCH. It is left in this register bank to provide compatibility with the Motorola 146818B. The PCH has no SQW pin. This bit is cleared by RSMRST#, but not on any other reset.
2	<b>Data Mode (DM)</b> —R/W. This bit specifies either binary or BCD data representation. This bit is not affected by RSMRST# nor any other reset signal. 0 = BCD 1 = Binary
1	<b>Hour Format (HOURFORM)</b> —R/W. This bit indicates the hour byte format. This bit is not affected by RSMRST# nor any other reset signal. 0 = Twelve-hour mode. In twelve-hour mode, the seventh bit represents AM as 0 and PM as one. 1 = Twenty-four hour mode.
0	<b>Daylight Savings Enable (DSE)</b> —R/W. The Daylight Savings Enable bit triggers 2 special hour updates per year when set to '1'. One is on the first Sunday in April, where time increments from 1:59:59 AM to 3:00:00 AM. The other is the last Sunday in October when the time first reaches 1:59:59 AM, it is changed to 1:00:00 AM. The time must increment normally for at least 2 update cycles (seconds) previous to these conditions for the time change to occur properly. 0 = Daylight Savings feature is disabled. 1 = Daylight Savings feature is enabled. <b>Note:</b> If BUC.DSO bit is set, this DSE bit continues to be R/W but daylight savings feature is ALWAYS DISABLED. <b>Note:</b> This bit is not affected by RSMRST# nor any other reset signal.



### 10.5.2.3 RTC\_REGC—Register C (Flag Register)

RTC Index: 0Ch Attribute: RO  
Default Value: 00U00000 (U: Undefined) Size: 8 bit  
Lockable: No Power Well: RTC

Writes to Register C have no effect.

Bit	Description
7	<b>Interrupt Request Flag (IRQF)</b> —RO. IRQF = (PF * PIE) + (AF * AIE) + (UF * UFE). This bit also causes the RTC Interrupt to be asserted. This bit is cleared upon RSMRST# or a read of Register C.
6	<b>Periodic Interrupt Flag (PF)</b> —RO. This bit is cleared upon RSMRST# or a read of Register C. 0 = If no taps are specified using the RS bits in Register A, this flag will not be set. 1 = Periodic interrupt Flag will be 1 when the tap specified by the RS bits of register A is 1.
5	<b>Alarm Flag (AF)</b> —RO. 0 = This bit is cleared upon RTCRST# or a read of Register C. 1 = Alarm Flag will be set after all Alarm values match the current time.
4	<b>Update-Ended Flag (UF)</b> —RO. 0 = The bit is cleared upon RSMRST# or a read of Register C. 1 = Set immediately following an update cycle for each second.
3:0	Reserved. Will always report 0.

### 10.5.2.4 RTC\_REGD—Register D (Flag Register)

RTC Index: 0Dh Attribute: R/W  
Default Value: 10UUUUUU (U: Undefined) Size: 8 bit  
Lockable: No Power Well: RTC

Bit	Description
7	<b>Valid RAM and Time Bit (VRT)</b> —R/W. 0 = This bit should always be written as a 0 for write cycle; however, it will return a 1 for read cycles. 1 = This bit is hardwired to 1 in the RTC power well.
6	Reserved, this bit always returns a 0 and should be set to 0 for write cycles.
5:0	<b>Date Alarm</b> —R/W. These bits store the date of month alarm value. If set to 000000b, then a don't care state is assumed. The host must configure the date alarm for these bits to do anything; however, they can be written at any time. If the date alarm is not enabled, these bits will return 0s to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.



## 10.6 Processor Interface Registers

Table 10-7 is the register address map for the processor interface registers.

**Table 10-7. Processor Interface PCI Register Address Map**

Offset	Mnemonic	Register Name	Default	Attribute
61h	NMI_SC	NMI Status and Control	00h	R/W, RO
70h	NMI_EN	NMI Enable	80h	R/W (special)
92h	PORT92	INIT	00h	R/W, RO
CF9h	RST_CNT	Reset Control	00h	R/W, RO

### 10.6.1 NMI\_SC—NMI Status and Control Register

I/O Address: 61h Attribute: R/W, RO  
 Default Value: 00h Size: 8 bit  
 Lockable: No Power Well: Core

Bit	Description
7	<b>SERR# NMI Source Status (SERR#_NMI_STS)</b> —RO 1 = Bit is set if a PCI agent detected a system error and pulses the PCI SERR# line and if bit 2 (PCI_SERR_EN) is cleared. This interrupt source is enabled by setting bit 2 to 0. To reset the interrupt, set bit 2 to 1 and then set it to 0. When writing to port 61h, this bit must be 0. <b>Note:</b> This bit is set by any of the PCH internal sources of SERR; this includes SERR assertions forwarded from the secondary PCI bus, errors on a PCI Express* port, or other internal functions that generate SERR#.
6	<b>IOCHK# NMI Source Status (IOCHK_NMI_STS)</b> —RO 1 = Bit is set if an LPC agent (using SERIRQ) asserted IOCHK# and if bit 3 (IOCHK_NMI_EN) is cleared. This interrupt source is enabled by setting bit 3 to 0. To reset the interrupt, set bit 3 to 1 and then set it to 0. When writing to port 61h, this bit must be a 0.
5	<b>Timer Counter 2 OUT Status (TMR2_OUT_STS)</b> —RO. This bit reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed following any PCI reset for this bit to have a determinate value. When writing to port 61h, this bit must be a 0.
4	<b>Refresh Cycle Toggle (REF_TOGGLE)</b> —RO. This signal toggles from either 0-to-1 or 1-to-0 at a rate that is equivalent to when refresh cycles would occur. When writing to port 61h, this bit must be a 0. <b>Note:</b> This bit will not toggle when CG.CG_Field_1 is set (RCBA+341Ch, bit 24).
3	<b>IOCHK# NMI Enable (IOCHK_NMI_EN)</b> —R/W 0 = Enabled. 1 = Disabled and cleared.
2	<b>PCI SERR# Enable (PCI_SERR_EN)</b> —R/W 0 = SERR# NMIs are enabled. 1 = SERR# NMIs are disabled and cleared.
1	<b>Speaker Data Enable (SPKR_DAT_EN)</b> —R/W 0 = SPKR output is a 0. 1 = SPKR output is equivalent to the Counter 2 OUT signal value.
0	<b>Timer Counter 2 Enable (TMR2_EN)</b> —R/W 0 = Disable 1 = Enable

## 10.6.2 NMI\_EN—NMI Enable (and Real Time Clock Index) Register

I/O Address:	70h	Attribute:	R/W (special)
Default Value:	80h	Size:	8 bit
Lockable:	No	Power Well:	Core

**Note:** The RTC Index field is write-only for normal operation. This field can only be read in Alt-Access Mode.

**Note:** This register is aliased to Port 74h (documented in [Table 10-5](#)), and all bits are readable at that address.

Bits	Description
7	<b>NMI Enable (NMI_EN)</b> —R/W (special). 0 = Enable NMI sources. 1 = Disable All NMI sources.
6:0	<b>Real Time Clock Index Address (RTC_INDEX)</b> —R/W (special). This data goes to the RTC to select which register or CMOS RAM address is being accessed.

## 10.6.3 PORT92—INIT Register

I/O Address:	92h	Attribute:	R/W, RO
Default Value:	00h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7:1	Reserved
0	<b>INIT_NOW</b> —R/W. When this bit transitions from a 0 to a 1, the PCH will force INIT# active for sixteen 24-MHz clocks.

## 10.6.4 RST\_CNT—Reset Control Register

I/O Address:	CF9h	Attribute:	R/W, RO
Default Value:	00h	Size:	8 bit
Lockable:	No	Power Well:	Core

Bit	Description
7:4	Reserved
3	<p><b>Full Reset (FULL_RST)</b>—R/W. This bit is used to determine the states of SLP_S3#, SLP_S4#, and SLP_S5# after a CF9 hard reset (SYS_RST =1 and RST_CPU is set to 1), after PWROK going low (with RSMRST# high), or after two TCO timeouts.</p> <p>0 = PCH will keep SLP_S3#, SLP_S4# and SLP_S5# high.</p> <p>1 = PCH will drive SLP_S3#, SLP_S4# and SLP_S5# low for 3 – 5 seconds.</p> <p><b>Note:</b> When this bit is set, it also causes the full power-cycle (SLP_S3/4/5# assertion) in response to SYS_RESET#, PWROK#, and Watchdog timer reset sources.</p>
2	<p><b>Reset Processor (RST_CPU)</b>—R/W. When this bit transitions from a 0 to a 1, it initiates a hard or soft reset, as determined by the SYS_RST bit—bit 1 of this register.</p>
1	<p><b>System Reset (SYS_RST)</b>—R/W. This bit is used to determine a hard or soft reset to the processor.</p> <p>0 = When RST_CPU bit goes from 0 to 1, the PCH performs a soft reset by activating INIT# for sixteen 24-MHz clocks.</p> <p>1 = When RST_CPU bit goes from 0 to 1, the PCH performs a hard reset by activating PLTRST# and SUS_STAT# active for a minimum of about 1 millisecond. In this case, SLP_S3#, SLP_S4#, and SLP_S5# state (assertion or de-assertion) depends on the FULL_RST bit setting. The PCH main power well is reset when this bit is 1. It also resets the resume well bits (except for those noted throughout this document).</p>
0	Reserved

## 10.7 Power Management Registers

The power management registers are distributed within the PCI Device 31: Function 0 space, as well as a separate I/O range. Each register is described below. Unless otherwise indicated, bits are in the main (core) power well.

Bits not explicitly defined in each register are assumed to be reserved. When writing to a reserved bit, the value should always be 0. Software should not attempt to use the value read from a reserved bit, as it may not be consistently 1 or 0.

### 10.7.1 Power Management PCI Configuration Registers (PM—D31:F0)

Table 10-8 shows a small part of the configuration space for PCI Device 31: Function 0. It includes only those registers dedicated for power management. Some of the registers are only used for Legacy Power management schemes.

**Table 10-8. Power Management PCI Register Address Map (PM—D31:F0)**

Offset	Mnemonic	Register Name	Default	Attribute
A0h-A1h	GEN_PMCON_1	General Power Management Configuration 1	0000h	R/W, R/WLO, RO
A2-A3h	GEN_PMCON_2	General Power Management Configuration 2	2000h	R/W, R/WC, RO
A4h-A5h	GEN_PMCON_3	General Power Management Configuration 3	4206h	R/W, R/WC, RO, R/WL
A6h	GEN_PMCON_LOCK	General Power Management Configuration Lock	00h	RO, R/WL
AAh	BM_BREAK_EN_2	BM_BREAK_EN Register #2	00h	R/W, RO
ABh	BM_BREAK_EN	BM_BREAK_EN Register	00h	R/W, RO

### 10.7.1.1 GEN\_PMCON\_1—General PM Configuration 1 Register (PM—D31:F0)

Offset Address:	A0-A1h	Attribute:	R/W, RO, R/WLO
Default Value:	0000h	Size:	16-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	Core

Bit	Description
15	<b>GEN_PMCON_1 Field 6</b> —R/W. BIOS may write to this field.
14	<b>GEN_PMCON_1 Field 5</b> —R/W. BIOS may write to this field.
13	<b>GEN_PMCON_1 Field 4</b> —R/W. BIOS may write to this field.
1	<b>GEN_PMCON_1 Field 3</b> —R/W. BIOS may write to this field.
10	<b>BIOS_PCI_EXP_EN</b> —R/W. This bit acts as a global enable for the SCI associated with the PCI Express* ports. 0 = The various PCI Express* ports and processor cannot cause the PCI_EXP_STS bit to go active. 1 = The various PCI Express* ports and processor can cause the PCI_EXP_STS bit to go active.
9	<b>PWRBTN_LVL</b> —RO. This bit indicates the current state of the PWRBTN# signal. 0 = Low 1 = High
8	Reserved
7:5	<b>GEN_PMCON_1 Field 1</b> —R/W. BIOS may write to this field.
4	<b>SMI_LOCK</b> —R/WLO. When this bit is set, writes to the GLB_SMI_EN bit (PMBASE + 30h, bit 0) will have no effect. Once the SMI_LOCK bit is set, writes of 0 to SMI_LOCK bit will have no effect (that is, once set, this bit can only be cleared by PLTRST#).
3	Reserved
2	<b>PCI CLKRUN# Enable (CLKRUN_EN)</b> —R/W. 0 = Disable. PCH drives the CLKRUN# signal low. 1 = Enable CLKRUN# logic to control the system 24-MHz clock using the CLKRUN# signal.  <b>Notes:</b> 1. When the SLP_EN# bit is set, the PCH drives the CLKRUN# signal low regardless of the state of the CLKRUN_EN bit. This ensures that the PCI and LPC clocks continue running during a transition to a sleep state. 2. This bit should be set mutually exclusive with the PSEUDO_CLKRUN_EN bit. Setting CLKRUN_EN in a non-mobile SKU could result in unspecified behavior.
1:0	<b>Periodic SMI# Rate Select (PER_SMI_SEL)</b> —R/W. Set by software to control the rate at which periodic SMI# is generated. 00 = 64 seconds 01 = 32 seconds 10 = 16 seconds 11 = 8 seconds

### 10.7.1.2 GEN\_PMCON\_2—General PM Configuration 2 Register (PM—D31:F0)

Offset Address:	A2—A3h	Attribute:	R/W, RO, R/WC
Default Value:	2000h	Size:	16-bit
Lockable:	No	Usage:	ACPI, Legacy
		Power Well:	RTC, SUS

Bit	Description
15	Reserved
14	<b>DC_PP_DIS</b> —R/W. On DC PHY Power Disable. <ul style="list-style-type: none"> <li>When this bit is set, SLP_LAN# will be driven low when ACPRESENT is low. This indicates that LAN PHY should be powered off on battery mode.</li> <li>When this bit is cleared (default), ACPRESENT state does not impact SLP_LAN# value.</li> </ul> Refer to <a href="#">Section 5.11.11.5</a> for more details on SLP_LAN# value. This bit is reset by RTCRST#.
13	<b>DSX_PP_DIS</b> —R/W. In Deep Sx PHY Power Disable. <ul style="list-style-type: none"> <li>When this bit is set (default), SLP_LAN# will be driven low in Deep Sx.</li> <li>When cleared, SLP_LAN# status in Deep Sx is dependant on status of Sx_PP_EN setting.</li> </ul> Refer to <a href="#">Section 5.11.11.5</a> for more details on SLP_LAN# value. This bit is reset by RTCRST#.
12	<b>AG3_PP_EN</b> —R/W. After G3 PHY Power Enable. <ul style="list-style-type: none"> <li>When this bit is cleared (default), SLP_LAN# will be driven low upon exiting G3.</li> <li>When this bit is set, SLP_LAN# value is dependant on DSX_PP_DIS and Sx_PP_EN setting.</li> </ul> Refer to <a href="#">Section 5.11.11.5</a> for more details on SLP_LAN# value. This bit is reset by RTCRST#.
11	<b>Sx_PP_EN</b> —R/W. Sx PHY Power Enable (Non G3 to Sx entry) <ul style="list-style-type: none"> <li>When this bit is cleared (default), SLP_LAN# will be driven low in Sx/M-Off.</li> <li>When this bit is set, SLP_LAN# will be driven high in Sx/M-Off.</li> </ul> Refer to <a href="#">Section 5.11.11.5</a> for more details on SLP_LAN# value. This bit is on VCCDSW3_3 and is reset when DSW is reset.
10:8	Reserved
7	<b>DRAM Initialization Bit</b> —R/W. This bit does not affect hardware functionality in any way. BIOS is expected to set this bit prior to starting the DRAM initialization sequence and to clear this bit after completing the DRAM initialization sequence. BIOS can detect that a DRAM initialization sequence was interrupted by a reset by reading this bit during the boot sequence. <ul style="list-style-type: none"> <li>If the bit is 1, then the DRAM initialization was interrupted.</li> <li>This bit is reset by the assertion of the RSMRST# pin.</li> </ul>
6	Reserved
5	<b>Memory Placed in Self-Refresh (MEM_SR)</b> —RO. <ul style="list-style-type: none"> <li>If the bit is 1, DRAM should have remained powered and held in Self-Refresh through the last power state transition (that is, the last time the system left S0).</li> <li>This bit is reset by the assertion of the RSMRST# pin.</li> </ul>
4	<b>System Reset Status (SRS)</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = SYS_RESET# button Not pressed. 1 = PCH sets this bit when the SYS_RESET# button is pressed. BIOS is expected to read this bit and clear it, if it is set. <b>Notes:</b> <ol style="list-style-type: none"> <li>This bit is also reset by RSMRST# and CF9h resets.</li> <li>The SYS_RESET# is implemented in the Main power well. This pin must be properly isolated and masked to prevent incorrectly setting this Suspend well status bit.</li> </ol>

Bit	Description
3	<p><b>Processor Thermal Trip Status (CTS)</b>—R/WC</p> <p>0 = Software clears this bit by writing a 1 to it.</p> <p>1 = This bit is set when PLTRST# is inactive and THRMTTRIP# goes active while the system is in an S0 or S1 state.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This bit is also reset by RSMRST#, and CF9h resets. It is not reset by the shutdown and reboot associated with the processor THRMTTRIP# event.</li> <li>2. The CF9h reset in the description refers to CF9h type core well reset that includes SYS_RESET#, PWROK/SYS_PWROK low, SMBus hard reset, TCO Timeout. This type of reset will clear CTS bit.</li> </ol>
2	<p><b>Minimum SLP_S4# Assertion Width Violation Status</b>—R/WC</p> <p>0 = Software clears this bit by writing a 1 to it.</p> <p>1 = Hardware sets this bit when the SLP_S4# assertion width is less than the time programmed in the SLP_S4# Minimum Assertion Width field (D31:F0:Offset A4h:bits 5:4). The PCH begins the timer when SLP_S4# is asserted during S4/S5 entry or when the RSMRST# input is de-asserted during SUS well power-up. This bit is functional regardless of the values in the SLP_S4# Assertion Stretch Enable (D31:F0:Offset A4h:bit 3) and in the Disable SLP Stretching after SUS Well Power Up (D31:F0:Offset A4h:bit 12).</p> <p><b>Note:</b> This bit is reset by the assertion of the RSMRST# pin, but can be set in some cases before the default value is readable.</p>
1	<p><b>SYS_PWROK Failure (SYSPWR_FLR)</b>—R/WC</p> <p>0 = This bit will be cleared only be software writing a 1 back to the bit or by SUS well power loss.</p> <p>1 = This bit will be set any time SYS_PWROK drops unexpectedly when the system was in S0 or S1 state.</p>
0	<p><b>PWROK Failure (PWROK_FLR)</b>—R/WC</p> <p>0 = This bit will be cleared only be software writing a 1 back to the bit or by SUS well power loss.</p> <p>1 = This bit will be set any time PWROK goes low when the system was in S0 or S1 state.</p> <p><b>Note:</b> See <a href="#">Section 5.11.11.3</a> for more details about the PWROK pin functionality.</p>

### 10.7.1.3 GEN\_PMCN\_3—General PM Configuration 3 Register (PM—D31:F0)

Offset Address: A4–A5h  
Default Value: 4206h  
Lockable: No

Attribute: R/W, R/WC, RO, R/WL  
Size: 16-bit  
Usage: ACPI, Legacy  
Power Well: RTC, SUS

Bit	Description																	
15	<p><b>PME_B0_S5_Disable (PME_B0_S5_DIS)</b>—R/W. When set to 1, this bit blocks wake events from PME_B0_STS in S5, regardless of the state of PME_B0_EN. When cleared (default), wake events from PME_B0_STS are allowed in S5 if PME_B0_EN = 1.</p> <p>Wakes from power states other than S5 are not affected by this policy bit.</p> <p>The net effect of setting PME_B0_S5_DIS = '1' is described by the truth table below.</p> <p>Y = Wake; N = Don't wake; B0 = PME_B0_EN; OV = WoL Enable Override</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>B0/OV</th> <th>S1/S3/S4</th> <th>S5</th> </tr> <tr> <td>00</td> <td>N</td> <td>N</td> </tr> <tr> <td>01</td> <td>N</td> <td>Y (LAN only)</td> </tr> <tr> <td>11</td> <td>Y (all PME B0 sources)</td> <td>Y (LAN only)</td> </tr> <tr> <td>10</td> <td>Y (all PME B0 sources)</td> <td>N</td> </tr> </table> <p>This bit is cleared by the RTCRST# pin.</p>			B0/OV	S1/S3/S4	S5	00	N	N	01	N	Y (LAN only)	11	Y (all PME B0 sources)	Y (LAN only)	10	Y (all PME B0 sources)	N
B0/OV	S1/S3/S4	S5																
00	N	N																
01	N	Y (LAN only)																
11	Y (all PME B0 sources)	Y (LAN only)																
10	Y (all PME B0 sources)	N																
14	<p><b>SUS Well Power Failure (SUS_PWR_FLR)</b>—R/WC</p> <p>0 = Software writes a 1 to this bit to clear it.</p> <p>1 = This bit is set to '1' whenever SUS well power is lost, as indicated by RSMRST# assertion.</p> <p>This bit is in the SUS well, and defaults to '1' based on RSMRST# assertion (not cleared by any type of reset).</p>																	
13	<p><b>WoL Enable Override (WOL_EN_OVRD)</b>—R/W</p> <p>0 = WoL policies are determined by PMEBO enable bit and appropriate LAN status bits.</p> <p>1 = Enable appropriately configured integrated LAN to wake the system in S5 only regardless of the value in the PME_B0_EN bit in the GPE0_EN register.</p> <p>This bit is cleared by the RTCRST# pin.</p>																	
12	<p><b>Disable SLP Stretching After SUS Well Power Up (DIS_SLP_STRCH_SUS_UP)</b>—R/WL</p> <p>0 = Enables stretching on SLP signals after SUS power failure as enabled and configured in other fields.</p> <p>1 = Disables stretching on SLP signals when powering up after a SUS well power loss, regardless of the state of the SLP_S4# Assertion Stretch Enable (bit 3).</p> <p>This bit is cleared by the RTCRST# pin.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This field is RO when the SLP Stretching Policy Lock-Down bit is set.</li> <li>2. If this bit is cleared, SLP stretch timers start on SUS well power-up (the PCH has no ability to count stretch time while the SUS well is powered down).</li> <li>3. This policy bit has a different effect on SLP_SUS# stretching than on the other SLP_* pins since SLP_SUS# is the control signal for one of the scenarios where SUS well power is lost (Deep Sx). The effect of setting this bit to '1' on: <ul style="list-style-type: none"> <li>— SLP_S3# and SLP_S4# stretching: disabled after any SUS power loss.</li> <li>— SLP_SUS# stretching: disabled after G3, but no impact on Deep Sx.</li> </ul> </li> </ol>																	
11:10	<p><b>SLP_S3# Minimum Assertion Width (SLP_S3_MIN_ASST_WDTH)</b>—R/WL This 2-bit value indicates the minimum assertion width of the SLP_S3# signal to ensure that the Main power supplies have been fully power-cycled.</p> <p>Valid Settings are:</p> <p>00 = 60 <math>\mu</math>s  01 = 1 ms  10 = 50 ms  11 = 2 seconds</p> <p>This bit is cleared by the RSMRST# pin.</p> <p><b>Note:</b> This field is RO when the SLP Stretching Policy Lock-Down bit is set.</p>																	



Bit	Description
9	<b>General Reset Status (GEN_RST_STS)</b> —R/WC. This bit is set by hardware whenever PLTRST# asserts for any reason other than going into a software-entered sleep state (using PM1CNT.SLP_EN write) or a suspend well power failure (RSMRST# pin assertion). BIOS is expected to consult and then write a 1 to clear this bit during the boot flow before determining what action to take based on PM1_STS.WAK_STS = 1. If GEN_RST_STS = 1, the cold reset boot path should be followed rather than the resume path, regardless of the setting of WAK_STS. This bit is cleared by the RSMRST# pin.
8	Reserved
7:6	<b>SWSMI_RATE_SEL</b> —R/W. This field indicates when the SWSMI timer will time out. Valid values are: 00 = 1.5 ms ± 0.6 ms 01 = 16 ms ± 4 ms 10 = 32 ms ± 4 ms 11 = 64 ms ± 4 ms These bits are not cleared by any type of reset except RTCRST#.
5:4	<b>SLP_S4# Minimum Assertion Width(SLP_S4_MIN_ASST_WDTH)</b> —R/WL This field indicates the minimum assertion width of the SLP_S4# signal to ensure that the DRAM modules have been safely power-cycled. Valid values are: 11 = 1 second 10 = 2 seconds 01 = 3 seconds 00 = 4 seconds This value is used in two ways: 1. If the SLP_S4# assertion width is ever shorter than this time, a status bit is set for BIOS to read when S0 is entered. 2. If enabled by bit 3 in this register, the hardware will prevent the SLP_S4# signal from de-asserting within this minimum time period after asserting. RTCRST# forces this field to the conservative default state (00b). <b>Notes:</b> 1. This field is RO when the SLP Stretching Policy Lock-Down bit is set. 2. The logic that measures this time is in the suspend power well. Therefore, when leaving a G3 or Deep Sx state, the minimum time is measured from the de-assertion of the internal suspend well reset (unless the "Disable SLP Stretching After SUS Well Power Up" bit is set).
3	<b>SLP_S4# Assertion Stretch Enable</b> —R/WL 0 = The SLP_S4# minimum assertion time is defined in Power Sequencing and Reset Signal Timings table. 1 = The SLP_S4# signal minimally assert for the time specified in bits 5:4 of this register. This bit is cleared by RTCRST#. <b>Note:</b> This bit is RO when the SLP Stretching Policy Lock-Down bit is set.
2	<b>RTC Power Status (RTC_PWR_STS)</b> —R/W. This bit is set when RTCRST# indicates a weak or missing battery. The bit is not cleared by any type of reset. The bit will remain set until the software clears it by writing a 0 back to this bit position.
1	<b>Power Failure (PWR_FLR)</b> —R/WC. This bit is in the Deep Sx well and defaults to 1 based on DPWROK de-assertion (not cleared by any type of reset). 0 = Indicates that the trickle current has not failed since the last time the bit was cleared. Software clears this bit by writing a 1 to it. 1 = Indicates that the trickle current (from the main battery or trickle supply) was removed or failed. <b>Note:</b> Clearing CMOS in a PCH-based platform can be done by using a jumper on RTCRST# or GPI. Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low.
0	<b>AFTERG3_EN</b> —R/W. This bit determines what state to go to when power is re-applied after a power failure (G3 state). This bit is in the RTC well and is only cleared by RTCRST# assertion. 0 = System will return to S0 state (boot) after power is re-applied. 1 = System will return to the S5 state (except if it was in S4, in which case it will return to S4). In the S5 state, the only enabled wake event is the Power Button or any enabled wake event that was preserved through the power failure.

**Note:** RSMRST# is sampled using the RTC clock. Therefore, low times that are less than one RTC clock period may not be detected by the PCH.

#### 10.7.1.4 GEN\_PMCN\_LOCK—General Power Management Configuration Lock Register

Offset Address: A6h Attribute: R/WLO, RO  
 Default Value: 00h Size: 8 bit  
 Lockable: No Usage: ACPI  
 Power Well: Core

Bit	Description
7:3	Reserved
2	<b>SLP Stretching Policy Lock-Down (SLP_STR_POL_LOCK)</b> —R/WLO. When set to 1, this bit locks down the Disable SLP Stretching After SUS Well Power Up, SLP_S3# Minimum Assertion Width, SLP_S4# Minimum Assertion Width, SLP_S4# Assertion Stretch Enable bits in the GEN_PMCN_3 register, making them read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. This bit is cleared by platform reset.
1	<b>ACPI_BASE_LOCK</b> —R/WLO. When set to 1, this bit locks down the ACPI Base Address Register (ABASE) at offset 40h. The Base Address Field becomes read-only. This bit becomes locked when a value of 1b is written to it. Writes of 0 to this bit are always ignored. Once locked by writing 1, the only way to clear this bit is to perform a platform reset.
0	Reserved

#### 10.7.1.5 BM\_BREAK\_EN\_2 Register #2 (PM—D31:F0)

Offset Address: AAh Attribute: R/W, RO  
 Default Value: 00h Size: 8 bits  
 Lockable: No Usage: ACPI, Legacy  
 Power Well: Core

Bit	Description
7:2	Reserved
1	<b>xHCI Break Enable (xHCI_BREAK_EN)</b> —R/W 0 = xHCI traffic will not cause BM_STS to be set. 1 = xHCI traffic will cause BM_STS to be set.
0	<b>SATA3 Break Enable (SATA3_BREAK_EN)</b> —R/W 0 = SATA3 traffic will not cause BM_STS to be set. 1 = SATA3 traffic will cause BM_STS to be set.

### 10.7.1.6 BM\_BREAK\_EN Register (PM—D31:F0)

Offset Address:	ABh	Attribute:	R/W
Default Value:	00h	Size:	8 bit
Lockable:	No	Usage:	ACPI, Legacy
Power Well:	Core		

Bit	Description
7	<b>Storage Break Enable (STORAGE_BREAK_EN)</b> —R/W 0 = Serial ATA traffic will not cause BM_STS to be set. 1 = Serial ATA traffic will cause BM_STS to be set.
6	<b>PCIE_BREAK_EN</b> —R/W 0 = PCI Express* traffic will not cause BM_STS to be set. 1 = PCI Express* traffic will cause BM_STS to be set.
5:3	Reserved
2	<b>EHCI_BREAK_EN</b> —R/W 0 = EHCI traffic will not cause BM_STS to be set. 1 = EHCI traffic will cause BM_STS to be set.
1	Reserved
0	<b>HDA_BREAK_EN</b> —R/W 0 = Intel® High Definition Audio traffic will not cause BM_STS to be set. 1 = Intel® High Definition Audio traffic will cause BM_STS to be set.



## 10.7.2 APM I/O Decode Register

Table 10-9 shows the I/O registers associated with APM support. This register space is enabled in the PCI Device 31: Function 0 space (APMDEC\_EN), and cannot be moved (fixed I/O location).

**Table 10-9. APM Register Map**

Address	Mnemonic	Register Name	Default	Type
B2h	APM_CNT	Advanced Power Management Control Port	00h	R/W
B3h	APM_STS	Advanced Power Management Status Port	00h	R/W

### 10.7.2.1 APM\_CNT—Advanced Power Management Control Port Register

I/O Address: B2h Attribute: R/W  
Default Value: 00h Size: 8 bit  
Lockable: No Usage: Legacy Only  
Power Well: Core

Bit	Description
7:0	Used to pass an APM command between the operating system and the SMI handler. Writes to this port not only store data in the APMC register, but also generates an SMI# when the APMC_EN bit is set.

### 10.7.2.2 APM\_STS—Advanced Power Management Status Port Register

I/O Address: B3h Attribute: R/W  
Default Value: 00h Size: 8 bit  
Lockable: No Usage: Legacy Only  
Power Well: Core

Bit	Description
7:0	Used to pass data between the operating system and the SMI handler. Basically, this is a scratchpad register and is not affected by any other register or function (other than a PCI reset).

### 10.7.3 Power Management I/O Registers

Table 10-10 shows the registers associated with ACPI and Legacy power management support. These register locations are all offsets from the ACPI base address defined in the PCI Device 31: Function 0 space (PMBASE), and can be moved to any 256-byte aligned I/O location. In order to access these registers, the ACPI Enable bit (ACPI\_EN) must be set. The registers are defined to support the ACPI 4.0a specification and generally use the same bit names.

**Note:** All reserved bits and registers will always return 0 when read, and will have no effect when written.

**Table 10-10. ACPI and Legacy I/O Register Map**

PMBASE + Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	PM1_STS	PM1 Status	0000h	R/WC, RO
02h-03h	PM1_EN	PM1 Enable	0000h	R/W, RO
04h-07h	PM1_CNT	PM1 Control	00000000h	R/W, WO, RO
08h-0Bh	PM1_TMR	PM1 Timer	00000000h	RO
30h-33h	SMI_EN	SMI# Control and Enable	00000002h	R/W, WO, R/WO, RO
34h-37h	SMI_STS	SMI Status	00000000h	R/WC, RO
42h	GPE_CNTL	General Purpose Event Control	00h	R/W, RO
44h-45h	DEVACT_STS	Device Activity Status	0000h	R/WC, RO
50h	PM2_CNT	Power Management 2 Control	00h	R/W, RO
80h-83h	GPE0_STS[31:0]	General Purpose Event 0 Status [31:0] Register	00000000h	R/WC
84h-87h	GPE0_STS[63:32]	General Purpose Event 0 Status [64:32] Register	00000000h	R/WC
88h-8Bh	GPE0_STS[94:64]	General Purpose Event 0 Status [94:64] Register	00000000h	R/WC, RO
8Ch-8Fh	GPE0_STS[127:96]	General Purpose Event 0 Status [127:96] Register	00000000h	R/WC, RO
90h-93h	GPE0_EN[31:0]	General Purpose Event 0 Enable [31:0] Register	00000000h	R/W
94h-97h	GPE0_EN[63:32]	General Purpose Event 0 Enable [63:32] Register	00000000h	R/W
98h-9Bh	GPE0_EN[94:64]	General Purpose Event 0 Enable [94:64] Register	00000000h	R/W, RO
9Ch-9Fh	GPE0_EN[127:96]	General Purpose Event 0 Enable [127:96] Register	00000000h	R/W

### 10.7.3.1 PM1\_STS—Power Management 1 Status Register

I/O Address:	PMBASE + 00h	Attribute:	R/WC, RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 12–15: Suspend Bit 11: RTC, Bits 8, 10, and 14: DSW		

If bit 10 or 8 in this register is set, and the corresponding \_EN bit is set in the PM1\_EN register, then the PCH will generate a Wake Event. Once back in an S0 state (or if already in an S0 state when the event occurs), the PCH will also generate an SCI if the SCI\_EN bit is set, or an SMI# if the SCI\_EN bit is not set.

**Note:** Bit 5 does not cause an SMI# or a wake event. Bit 0 does not cause a wake event but can cause an SMI# or SCI.

Bit	Description
15	<p><b>Wake Status (WAK_STS)</b>—R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by RSMRST#.</p> <p>0 = Software clears this bit by writing a 1 to it.</p> <p>1 = Set by hardware when the system is in one of the sleep states (using the SLP_EN bit) and an enabled wake event occurs. Upon setting this bit, the PCH will transition the system to the ON state.</p> <p>If the AFTERG3_EN bit is not set and a power failure (such as removed batteries) occurs without the SLP_EN bit set, the system will return to an S0 state when power returns, and the WAK_STS bit will not be set.</p> <p>If the AFTERG3_EN bit is set and a power failure occurs without the SLP_EN bit having been set, the system will go into an S5 state when power returns, and a subsequent wake event will cause the WAK_STS bit to be set. Any subsequent wake event would have to be caused by either a Power Button press, or an enabled wake event that was preserved through the power failure (enable bit in the RTC well).</p>
14	<p><b>PCI Express* Wake Status (PCIEXPWAK_STS)</b>—R/WC.</p> <p>0 = Software clears this bit by writing a 1 to it. If the WAKE# pin is still active during the write or the PME message received indication has not been cleared in the root port, then the bit will remain active (that is, all inputs to this bit are level-sensitive).</p> <p>1 = This bit is set by hardware to indicate that the system woke due to a PCI Express* wakeup event. This wakeup event can be caused by the PCI Express* WAKE# pin being active or receipt of a PCI Express* PME message at a root port. This bit is set only when one of these events causes the system to transition from a non-S0 system power state to the S0 system power state. This bit is set independent of the state of the PCIEXP_WAKE_DIS bit.</p> <p><b>Note:</b> This bit does not itself cause a wake event or prevent entry to a sleeping state. Thus, if the bit is 1 and the system is put into a sleeping state, the system will not automatically wake.</p>
13:12	Reserved
11	<p><b>Power Button Override Status (PWRBTNOR_STS)</b>—R/WC</p> <p>0 = Software clears this bit by writing a 1 to it.</p> <p>1 = This bit is set any time a Power Button Override occurs (that is, the power button is pressed for at least 4 consecutive seconds), due to the corresponding bit in the SMBus slave message, Intel® ME Initiated Power Button Override, Intel® ME Initiated Host Reset with Power down or due to an internal thermal sensor catastrophic condition. The power button override causes an unconditional transition to the S5 state. The BIOS or SCI handler clears this bit by writing a 1 to it. This bit is not affected by hard resets using CF9h writes, and is not reset by RSMRST#. Thus, this bit is preserved through power failures. If this bit is still asserted when the global SCI_EN is set, an SCI will be generated.</p> <p><b>Note:</b> Upon entry to S5 due to an event described above, if Deep Sx is enabled and conditions are met per <a href="#">Section 5.11.8.6</a>, the system will transition to Deep Sx.</p>
10	<p><b>RTC Status (RTC_STS)</b>—R/WC. This bit is not affected by hard resets caused by a CF9 write, but is reset by DPWROK.</p> <p>0 = Software clears this bit by writing a 1 to it.</p> <p>1 = Set by hardware when the RTC generates an alarm (assertion of the IRQ8# signal). Additionally, if the RTC_EN bit (PMBASE + 02h, bit 10) is set, the setting of the RTC_STS bit will generate a wake event.</p>
9	Reserved



Bit	Description
8	<p><b>Power Button Status (PWRBTN_STS)</b>—R/WC. This bit is not affected by hard resets caused by a CF9 write but is reset by DPWROK.</p> <p>0 = If the PWRBTN# signal is held low for more than 4 seconds, the hardware clears the PWRBTN_STS bit, sets the PWRBTNOR_STS bit, and the system transitions to the S5 state with only PWRBTN# enabled as a wake event. This bit can be cleared by software by writing a one to the bit position.</p> <p>1 = This bit is set by hardware when the PWRBTN# signal is asserted Low, independent of any other enable bit. In the S0 state, while PWRBTN_EN and PWRBTN_STS are both set, an SCI (or SMI# if SCI_EN is not set) will be generated. In any sleeping state S1–S5, while PWRBTN_EN (PMBASE + 02h, bit 8) and PWRBTN_STS are both set, a wake event is generated.</p> <p><b>Note:</b> If the PWRBTN_STS bit is cleared by software while the PWRBTN# signal is still asserted, this will not cause the PWRBTN_STS bit to be set. The PWRBTN# signal must go inactive and active again to set the PWRBTN_STS bit.</p> <p><b>Note:</b> Upon entry to S5 due to an event described above, if Deep Sx is enabled and conditions are met per <a href="#">Section 5.11.8.6</a>, the system will transition to Deep Sx.</p>
7:6	Reserved
5	<p><b>Global Status (GBL_STS)</b>—R/WC</p> <p>0 = The SCI handler should then clear this bit by writing a 1 to the bit location.</p> <p>1 = Set when an SCI is generated due to BIOS wanting the attention of the SCI handler. BIOS has a corresponding bit, BIOS_RLS, which will cause an SCI and set this bit.</p>
4	<p><b>Bus Master Status (BM_STS)</b>—R/WC. This bit will not cause a wake event, SCI or SMI#.</p> <p>0 = Software clears this bit by writing a 1 to it.</p> <p>1 = Set by the PCH when a PCH visible bus master requests access to memory or the BMBUSY# signal is active.</p>
3:1	Reserved
0	<p><b>Timer Overflow Status (TMROF_STS)</b>—R/WC</p> <p>0 = The SCI or SMI# handler clears this bit by writing a 1 to the bit location.</p> <p>1 = This bit gets set any time bit 22 of the 24-bit timer goes high (bits are numbered from 0 to 23). This will occur every 2.3435 seconds. When the TMROF_EN bit (PMBASE + 02h, bit 0) is set, the setting of the TMROF_STS bit will additionally generate an SCI or SMI# (depending on the SCI_EN).</p>

### 10.7.3.2 PM1\_EN—Power Management 1 Enable Register

I/O Address:	PMBASE + 02h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Bits 0–7: Core, Bits 8–9, 11–13, 15: Suspend, Bit 14: DSW, Bit 10: RTC		

Bit	Description
15	Reserved
14	<p><b>PCI Express* Wake Disable (PCIEXPWAK_DIS)</b>—R/W. Modification of this bit has no impact on the value of the PCIEXP_WAKE_STS bit.</p> <p>0 = Inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register enabled to wake the system.</p> <p>1 = Inputs to the PCIEXP_WAKE_STS bit in the PM1 Status register disabled from waking the system.</p>
13:11	Reserved
10	<p><b>RTC Event Enable (RTC_EN)</b>—R/W. This bit is in the RTC well to allow an RTC event to wake after a power failure.</p> <p>0 = No SCI (or SMI#) or wake event is generated when RTC_STS (PMBASE + 00h, bit 10) goes active.</p> <p>1 = An SCI (or SMI#) or wake event will occur when this bit is set and the RTC_STS bit goes active.</p>
9	Reserved

Bit	Description														
8	<b>Power Button Enable (PWRBTN_EN)</b> —R/W. This bit is used to enable the setting of the PWRBTN_STS bit to generate a power management event (SMI#, SCI). PWRBTN_EN has no effect on the PWRBTN_STS bit (PMBASE + 00h, bit 8) being set by the assertion of the power button. The Power Button is always enabled as a Wake event. 0 = Disable. 1 = Enable.														
7:6	Reserved														
5	<b>Global Enable (GBL_EN)</b> —R/W. When both the GBL_EN and the GBL_STS bit (PMBASE + 00h, bit 5) are set, an SCI is raised. 0 = Disable. 1 = Enable SCI on GBL_STS going active.														
4:1	Reserved														
0	<b>Timer Overflow Interrupt Enable (TMROF_EN)</b> —R/W. Works in conjunction with the SCI_EN bit (PMBASE + 04h, bit 0) as described below: <table> <thead> <tr> <th>TMROF_EN</th> <th>SCI_EN</th> <th>Effect when TMROF_STS is set</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>No SMI# or SCI</td> </tr> <tr> <td>1</td> <td>0</td> <td>SMI#</td> </tr> <tr> <td>1</td> <td>1</td> <td>SCI</td> </tr> </tbody> </table>			TMROF_EN	SCI_EN	Effect when TMROF_STS is set	0	X	No SMI# or SCI	1	0	SMI#	1	1	SCI
TMROF_EN	SCI_EN	Effect when TMROF_STS is set													
0	X	No SMI# or SCI													
1	0	SMI#													
1	1	SCI													

### 10.7.3.3 PM1\_CNT—Power Management 1 Control Register

I/O Address: PMBASE + 04h Attribute: R/W, WO, RO  
Default Value: 00000000h Size: 32 bits  
Lockable: No Usage: ACPI or Legacy  
Power Well: Bits 0–9, 13–31: Core,  
Bits 10–12: RTC

Bit	Description																				
31:14	Reserved																				
13	<b>Sleep Enable (SLP_EN)</b> —WO. Setting this bit causes the system to sequence into the Sleep state defined by the SLP_TYP field.																				
12:10	<b>Sleep Type (SLP_TYP)</b> —R/W. This 3-bit field defines the type of Sleep the system should enter when the SLP_EN bit is set to 1. These bits are only reset by RTCRST#. <table> <thead> <tr> <th>Code</th> <th>Master Interrupt</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>ON: Typically maps to S0 state.</td> </tr> <tr> <td>001b</td> <td>Puts Processor Core in S1 state.</td> </tr> <tr> <td>010b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>Reserved</td> </tr> <tr> <td>100b</td> <td>Reserved</td> </tr> <tr> <td>101b</td> <td>Suspend-To-RAM. Assert SLP_S3#: Typically maps to S3 state.</td> </tr> <tr> <td>110b</td> <td>Suspend-To-Disk. Assert SLP_S3#, and SLP_S4#: Typically maps to S4 state.</td> </tr> <tr> <td>111b</td> <td>Soft Off. Assert SLP_S3#, SLP_S4#, and SLP_S5#: Typically maps to S5 state.</td> </tr> </tbody> </table>			Code	Master Interrupt	000b	ON: Typically maps to S0 state.	001b	Puts Processor Core in S1 state.	010b	Reserved	011b	Reserved	100b	Reserved	101b	Suspend-To-RAM. Assert SLP_S3#: Typically maps to S3 state.	110b	Suspend-To-Disk. Assert SLP_S3#, and SLP_S4#: Typically maps to S4 state.	111b	Soft Off. Assert SLP_S3#, SLP_S4#, and SLP_S5#: Typically maps to S5 state.
Code	Master Interrupt																				
000b	ON: Typically maps to S0 state.																				
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010b	Reserved																				
011b	Reserved																				
100b	Reserved																				
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110b	Suspend-To-Disk. Assert SLP_S3#, and SLP_S4#: Typically maps to S4 state.																				
111b	Soft Off. Assert SLP_S3#, SLP_S4#, and SLP_S5#: Typically maps to S5 state.																				
9:3	Reserved																				



Bit	Description
2	<b>Global Release (GBL_RLS)</b> —WO 0 = This bit always reads as 0. 1 = ACPI software writes a 1 to this bit to raise an event to the BIOS. BIOS software has corresponding enable and status bits to control its ability to receive ACPI events.
1	<b>Bus Master Reload (BM_RLD)</b> —R/W. This bit is treated as a scratchpad bit. This bit is reset to 0 by PLTRST# 0 = Bus master requests will not cause a break from the C3 state. 1 = Enables Bus Master requests (internal or external) to cause a break from the C3 state. If software fails to set this bit before going to C3 state, the PCH will still return to a snooperable state from C3 or C4 states due to bus master activity.
0	<b>SCI Enable (SCI_EN)</b> —R/W. Selects the SCI interrupt or the SMI# interrupt for various events including the bits in the PM1_STS register (bit 10, 8, 0), and bits in GPE0_STS. 0 = These events will generate an SMI#. 1 = These events will generate an SCI.

#### 10.7.3.4 PM1\_TMR—Power Management 1 Timer Register

I/O Address: PMBASE + 08h Attribute: RO  
 Default Value: 00000000h Size: 32 bits  
 Lockable: No Usage: ACPI  
 Power Well: Core

Bit	Description
31:24	Reserved
23:0	<b>Timer Value (TMR_VAL)</b> —RO. Returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (14.31818 MHz divided by 4). It is reset to 0 during a PCI reset, and then continues counting as long as the system is in the S0 state. After an S1 state, the counter will not be reset; it will continue counting from the last value in S0 state. Anytime bit 22 of the timer goes HIGH to LOW (bits referenced from 0 to 23), the TMROF_STS bit (PMBASE + 00h, bit 0) is set. The High-to-Low transition will occur every 2.3435 seconds. If the TMROF_EN bit (PMBASE + 02h, bit 0) is set, an SCI interrupt is also generated.

### 10.7.3.5 SMI\_EN—SMI Control and Enable Register

I/O Address:	PMBASE + 30h	Attribute:	R/W, WO, R/WL, RO
Default Value:	00000002h	Size:	32 bits
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

**Note:** This register is symmetrical to the SMI status register.

Bit	Description
31	<b>xHCI SMI Enable (xHCI_SMI_EN)</b> —R/W. 0 = Disable 1 = Enables xHCI to cause SMI#.
30	<b>ME SMI Enable (ME_SMI_EN)</b> —R/W. 0 = Disable 1 = Enables Intel® ME to cause SMI#.
29:28	Reserved
27	<b>GPIO_UNLOCK_SMI_EN</b> —R/WO. Setting this bit will cause the PCH to generate an SMI# when the GPIO_UNLOCK_SMI_STS bit is set in the SMI_STS register. Once written to 1, this bit can only be cleared by PLTRST#.
26:19	Reserved
18	<b>INTEL_USB2_EN</b> —R/W. 0 = Disable 1 = Enables Intel-Specific EHCI SMI logic to cause SMI#.
17	<b>LEGACY_USB2_EN</b> —R/W. 0 = Disable 1 = Enables legacy EHCI logic to cause SMI#.
16:15	Reserved
14	<b>PERIODIC_EN</b> —R/W. 0 = Disable. 1 = Enables the PCH to generate an SMI# when the PERIODIC_STS bit (PMBASE + 34h, bit 14) is set in the SMI_STS register (PMBASE + 34h).
13	<b>TCO_EN</b> —R/WL. 0 = Disables TCO logic generating an SMI#. If the NMI2SMI_EN bit is set, SMIs that are caused by re-routed NMIs will not be gated by the TCO_EN bit. Even if the TCO_EN bit is 0, NMIs will still be routed to cause SMIs. 1 = Enables the TCO logic to generate SMI#.  <b>Note:</b> This bit cannot be written once the TCO_LOCK bit is set.
12	Reserved
11	<b>MCSMI_EN Microcontroller SMI Enable (MCSMI_EN)</b> —R/W. 0 = Disable. 1 = Enables PCH to trap accesses to the microcontroller range (62h or 66h) and generate an SMI#. <b>Note</b> that “trapped” cycles will be claimed by the PCH on PCI, but not forwarded to LPC.
10:8	Reserved
7	<b>BIOS Release (BIOS_RLS)</b> —WO. 0 = This bit will always return 0 on reads. Writes of 0 to this bit have no effect. 1 = Enables the generation of an SCI interrupt for ACPI software when a one is written to this bit position by BIOS software.  <b>Note:</b> GBL_STS being set will cause an SCI, even if the SCI_EN bit is not set. Software must take great care not to set the BIOS_RLS bit (that causes GBL_STS to be set) if the SCI handler is not in place.



Bit	Description
6	<b>Software SMI# Timer Enable (SWSMI_TMR_EN)</b> —R/W. 0 = Disable. Clearing the SWSMI_TMR_EN bit before the timer expires will reset the timer and the SMI# will not be generated. 1 = Starts Software SMI# Timer. When the SWSMI timer expires (the timeout period depends upon the SWSMI_RATE_SEL bit setting), SWSMI_STS is set and an SMI# is generated. SWSMI_TMR_EN stays set until cleared by software.
5	<b>APMC_EN</b> —R/W. 0 = Disable. Writes to the APM_CNT register will not cause an SMI#. 1 = Enables writes to the APM_CNT register to cause an SMI#.
4	<b>SLP_SMI_EN</b> —R/W. 0 = Disables the generation of SMI# on SLP_EN. This bit must be 0 before the software attempts to transition the system into a sleep state by writing a 1 to the SLP_EN bit. 1 = A write of 1 to the SLP_EN bit—bit 13 in the PM1_CNT register will generate an SMI#, and the system will not transition to the sleep state based on that write to the SLP_EN bit.
3	<b>LEGACY_USB_EN</b> —R/W. 0 = Disable. 1 = Enables legacy USB circuit to cause SMI#.
2	<b>BIOS_EN</b> —R/W. 0 = Disable. 1 = Enables the generation of SMI# when ACPI software writes a 1 to the GBL_RLS bit (D31:F0:PMBase + 04h:bit 2). If the BIOS_STS bit (D31:F0:PMBase + 34h:bit 2), which gets set when software writes 1 to GBL_RLS bit, is already a 1 at the time that BIOS_EN becomes 1, an SMI# will be generated when BIOS_EN gets set.
1	<b>End of SMI (EOS)</b> —R/W (special). This bit controls the arbitration of the SMI signal to the processor. This bit must be set for the PCH to assert SMI# low to the processor after SMI# has been asserted previously. 0 = Once the PCH asserts SMI# low, the EOS bit is automatically cleared. 1 = When this bit is set to 1, the SMI# signal will be de-asserted for four 24-MHz clocks before its assertion. In the SMI handler, the processor should clear all pending SMIs (by servicing them and then clearing their respective status bits), set the EOS bit, and exit SMM. This will allow the SMI arbiter to re-assert SMI upon detection of an SMI event and the setting of a SMI status bit. <b>Note:</b> The PCH is able to generate 1st SMI after reset even though EOS bit is not set. Subsequent SMI requires EOS bit to be set.
0	<b>GBL_SMI_EN</b> —R/W. 0 = No SMI# will be generated by PCH. This bit is reset by a PCI reset event. 1 = Enables the generation of SMI# in the system upon any enabled SMI event. <b>Note:</b> When the SMI_LOCK bit is set, this bit cannot be changed.

### 10.7.3.6 SMI\_STS—SMI Status Register

I/O Address:	PMBASE + 34h	Attribute:	RO, R/WC, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Usage:	ACPI or Legacy
Power Well:	Core		

**Note:**

If the corresponding \_EN bit is set when the \_STS bit is set, the PCH will cause an SMI# (except bits 8–10 and 12, which do not need enable bits since they are logic ORs of other registers that have enable bits). The PCH uses the same GPE0\_EN register (I/O address: PMBase+2Ch) to enable/disable both SMI and ACPI SCI general purpose input events. ACPI OS assumes that it owns the entire GPE0\_EN register per the ACPI specification. Problems arise when some of the general-purpose inputs are enabled as SMI by BIOS, and some of the general purpose inputs are enabled for SCI. In this case ACPI OS turns off the enabled bit for any GPIx input signals that are not indicated as SCI general-purpose events at boot, and exit from sleeping states. BIOS should define a dummy control method that prevents the ACPI OS from clearing the SMI GPE0\_EN bits.

Bit	Description
31:28	Reserved
27	<b>GPIO_UNLOCK_SMI_STS</b> —R/WC. This bit will be set if the GPIO registers lockdown logic is requesting an SMI#. Writing a 1 to this bit position clears this bit to 0.
26	<b>SPI_STS</b> —RO. This bit will be set if the SPI logic is generating an SMI#. This bit is read only because the sticky status and enable bits associated with this function are located in the SPI registers.
25:22	Reserved
21	<b>MONITOR_STS</b> —RO. This bit will be set if the Trap/SMI logic has caused the SMI. This will occur when the processor or a bus master accesses an assigned register (or a sequence of accesses). See <a href="#">Section 8.1.17</a> through <a href="#">Section 8.1.31</a> for details on the specific cause of the SMI.
20	<b>PCI_EXP_SMI_STS</b> —RO. PCI Express* SMI event occurred. This could be due to a PCI Express* PME event or hot-plug event.
19	Reserved
18	<b>INTEL_USB2_STS</b> —RO. This non-sticky read-only bit is a logical OR of each of the SMI status bits in the Intel-Specific EHCI SMI Status Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated EHCIs are represented with this bit.
17	<b>LEGACY_USB2_STS</b> —RO. This non-sticky read-only bit is a logical OR of each of the SMI status bits in the EHCI Legacy Support Register ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. Writes to this bit will have no effect. All integrated EHCIs are represented with this bit.
16	<b>SMBus SMI Status (SMBUS_SMI_STS)</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = This bit is set from the 64 KHz clock domain used by the SMBus. Software must wait at least 15.63 $\mu$ s after the initial assertion of this bit before clearing it. 1 = Indicates that the SMI# was caused by: 1. The SMBus Slave receiving a message that an SMI# should be caused, or 2. The SMBALERT# signal goes active and the SMB_SMI_EN bit is set and the SMBALERT_DIS bit is cleared, or 3. The SMBus Slave receiving a Host Notify message and the HOST_NOTIFY_INTREN and the SMB_SMI_EN bits are set, or 4. The PCH detecting the SMLINK_SLAVE_SMI command while in the S0 state.
15	<b>SERIRQ_SMI_STS</b> —RO. 0 = SMI# was not caused by the SERIRQ decoder. 1 = Indicates that the SMI# was caused by the SERIRQ decoder. <b>Note:</b> This is not a sticky bit.



Bit	Description
14	<b>PERIODIC_STS</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set at the rate determined by the PER_SMI_SEL bits. If the PERIODIC_EN bit (PMBASE + 30h, bit 14) is also set, the PCH generates an SMI#.
13	<b>TCO_STS</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = SMI# not caused by TCO logic. 1 = Indicates the SMI# was caused by the TCO logic. This is not a wake event.
12	<b>Device Monitor Status (DEVMON_STS)</b> —RO 0 = SMI# not caused by Device Monitor. 1 = Set if bit 0 of the DEVACT_STS register (PMBASE + 44h) is set. The bit is not sticky, so writes to this bit will have no effect.
11	<b>Microcontroller SMI# Status (MCSMI_STS)</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = Indicates that there has been no access to the power management microcontroller range (62h or 66h). 1 = Set if there has been an access to the power management microcontroller range (62h or 66h) and the Microcontroller Decode Enable #1 bit in the LPC Bridge I/O Enables configuration register is 1 (D31:F0:Offset 82h:bit 11). This implementation assumes that the Microcontroller is on LPC. If this bit is set, and the MCSMI_EN bit is also set, the PCH will generate an SMI#.
10	1 = <b>GPIO_SMI_STS</b> —RO. This bit will be a '1' if any GPIO that is enabled trigger SMI is asserted. GPIOs that are not routed to cause an SMI# will have no effect on this bit.
9	1 = <b>GPE0_STS</b> —RO. This bit is a logical OR of the bits 18, 17, 16, 13, 11, 10, 8 and 2 in the GPE0_STS register (PMBASE + 8Ch) that also have the corresponding bit set in the GPE0_EN register (PMBASE + 9Ch).
8	<b>PM1_STS_REG</b> —RO. This is an ORs of the bits in the ACPI PM1 Status Register (offset PMBASE+00h) that can cause an SMI#. 0 = SMI# was not generated by a PM1_STS event. 1 = SMI# was generated by a PM1_STS event.
7	Reserved
6	<b>SWSMI_TMR_STS</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = Software SMI# Timer has not expired. 1 = Set by the hardware when the Software SMI# Timer expires.
5	<b>APM_STS</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = No SMI# generated by write access to APM Control register with APMCH_EN bit set. 1 = SMI# was generated by a write access to the APM Control register with the APMC_EN bit set.
4	<b>SLP_SMI_STS</b> —R/WC. Software clears this bit by writing a 1 to the bit location. 0 = No SMI# caused by write of 1 to SLP_EN bit when SLP_SMI_EN bit is also set. 1 = Indicates an SMI# was caused by a write of 1 to SLP_EN bit when SLP_SMI_EN bit is also set.
3	<b>LEGACY_USB_STS</b> —RO. This bit is a logical OR of each of the SMI status bits in the USB Legacy Keyboard/Mouse Control Registers ANDed with the corresponding enable bits. This bit will not be active if the enable bits are not set. 0 = SMI# was not generated by USB Legacy event. 1 = SMI# was generated by USB Legacy event.
2	<b>BIOS_STS</b> —R/WC. 0 = No SMI# generated due to ACPI software requesting attention. 1 = This bit gets set by hardware when a 1 is written by software to the GBL_RLS bit (D31:F0:PMBase + 04h:bit 2). When both the BIOS_EN bit (D31:F0:PMBase + 30h:bit 2) and the BIOS_STS bit are set, an SMI# will be generated. The BIOS_STS bit is cleared when software writes a 1 to its bit position.
1:0	Reserved

### 10.7.3.7 GPE\_CNTL—General Purpose Control Register

I/O Address:	PMBASE +42h	Attribute:	R/W, RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Usage:	ACPI or Legacy
Power Well:			Bits 0–1, 3–7: Suspend Bit 2: RTC

Bit	Description
7:2	Reserved
1	<b>SWGPE_CTRL</b> —R/W. This bit allows software to control the assertion of SWGPE_STS bit. This bit is used by hardware as the level input signal for the SWGPE_STS bit in the GPE0_STS register. When SWGPE_CTRL is 1, SWGPE_STS will be set to 1, and writes to SWGPE_STS with a value of 1 to clear SWGPE_STS will result in SWGPE_STS being set back to 1 by hardware. When SWGPE_CTRL is 0, writes to SWGPE_STS with a value of 1 will clear SWGPE_STS to 0. In addition to being cleared by RSMRST# assertion, the PCH also clears this bit due to a Power Button Override event, Intel® ME Initiated Power Button Override, Intel® ME Initiated Host Reset with Power down, SMBus unconditional power down, processor thermal trip event, or due to an internal thermal sensor catastrophic condition.
0	Reserved

### 10.7.3.8 DEVACT\_STS—Device Activity Status Register

I/O Address:	PMBASE +44h	Attribute:	R/WC, RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Usage:	Legacy Only
Power Well:	Core		

Each bit indicates if an access has occurred to the corresponding device's trap range, or for bits 6:9 if the corresponding PCI interrupt is active. This register is used in conjunction with the Periodic SMI# timer to detect any system activity for legacy power management. The periodic SMI# timer indicates if it is the right time to read the DEVACT\_STS register (PMBASE + 44h).

**Note:** Software clears bits that are set in this register by writing a 1 to the bit position.

Bit	Description
15:13	Reserved
12	<b>KBC_ACT_STS</b> —R/WC. KBC (60/64h). 0 = Indicates that there has been no access to this device I/O range. 1 = This device I/O range has been accessed. Clear this bit by writing a 1 to the bit location.
11:10	Reserved
9	<b>PIRQDH_ACT_STS</b> —R/WC. PIRQ[D or H]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
8	<b>PIRQCG_ACT_STS</b> —R/WC. PIRQ[C or G]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.

Bit	Description
7	<b>PIRQBF_ACT_STS</b> —R/WC. PIRQ[B or F]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
6	<b>PIRQAE_ACT_STS</b> —R/WC. PIRQ[A or E]. 0 = The corresponding PCI interrupts have not been active. 1 = At least one of the corresponding PCI interrupts has been active. Clear this bit by writing a 1 to the bit location.
5:0	Reserved

### 10.7.3.9 PM2\_CNT—Power Management 2 Control Register

I/O Address:	PMBASE + 50h	Attribute:	R/W, RO
Default Value:	00h	Size:	8 bits
Lockable:	No	Usage:	ACPI
Power Well:	Core		

Bit	Description
7:1	Reserved
0	<b>Arbiter Disable (ARB_DIS)</b> —R/W This bit is a scratch pad bit for legacy software compatibility.

### 10.7.3.10 GPEO\_STS[31:0]—General Purpose Event 0 Status [31:0] Register

I/O Address:	PMBASE + 80-83h	Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Usage:	ACPI
Power Well:	Bits 7:0, 23:16: Core, Bits 15:8, 31:24: Suspend		

This register is symmetrical to the General Purpose Event 0 Enable [31:0] register.

Bit	Description
31:0	<p><b>GPIO[31:0] Status (GPIO[31:0]_STS)</b>—These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is high (or low if the corresponding GP_INV bit is set). If the corresponding enable bit is set in the GPE0_EN register, then when the GPIO[n]_STS bit is set:</p> <ul style="list-style-type: none"> <li>• If system is in an S1-S5 state, the event will also wake the system</li> <li>• If system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPIO_ROUT bits for the corresponding GPIO. These bits are sticky bits and are cleared by writing a 1 back to this bit position.</li> </ul>

### 10.7.3.11 GPE0\_STS[63:32]—General Purpose Event 0 Status [63:32] Register

I/O Address:	PMBASE + 84–87h	Attribute:	R/WC
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Usage:	ACPI
Power Well:			Bits 7:0, 23:16: Core, Bits 15:8, 31:24: Suspend

This register is symmetrical to the General Purpose Event 0 Enable [63:32] register.

Bit	Description
31:0	<b>GPI[63:32] Status (GPI[63:32]_STS)</b> —R/WC. These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is high (or low if the corresponding GP_INV bit is set). If the corresponding enable bit is set in the GPE0_EN register, then when the GPI[n].STS bit is set: <ul style="list-style-type: none"> <li>• If system is in an S1–S5 state, the event will also wake the system</li> <li>• If system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPI_ROUT bits for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position.</li> </ul>

### 10.7.3.12 GPE0\_STS[94:64]—General Purpose Event 0 Status [94:64] Register

I/O Address:	PMBASE + 88–8Bh	Attribute:	R/WC, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Usage:	ACPI
Power Well:			Bits 7:0, 31:12: Core, Bits 11:8; Suspend

This register is symmetrical to the General Purpose Event 0 Enable [94:64] register.

Bit	Description
31	Reserved
30:0	<b>GPI[94:64] Status (GPI[94:64]_STS)</b> —R/WC. These bits are set any time the corresponding GPIO is set up as an input and the corresponding GPIO signal is high (or low if the corresponding GP_INV bit is set). If the corresponding enable bit is set in the GPE0_EN register, then when the GPI[n].STS bit is set: <ul style="list-style-type: none"> <li>• If system is in an S1–S5 state, the event will also wake the system</li> <li>• If system is in an S0 state (or upon waking back to an S0 state), an SCI will be caused, depending on the GPI_ROUT bits for the corresponding GPI. These bits are sticky bits and are cleared by writing a 1 back to this bit position.</li> </ul>

### 10.7.3.13 GPE0\_STS[127:96]—General Purpose Event 0 Status [127:96]

I/O Address:	PMBASE + 8C–8Fh	Attribute:	R/WC, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Usage:	ACPI
Power Well:			Bits 31:24, 15:0: Suspend, Bit 23:16: DSW

This register is symmetrical to the General Purpose Event 0 Enable [94:64] register.

Bit	Description
31:19	Reserved
18	<b>Wake Alarm Device Timer Status (WADT_STS)</b> —R/WC. This bit is set whenever any of the wake alarm device timers signal a timer expiration.
17	Reserved



Bit	Description
16	<b>GPIO[27] Status (GP27_STS)</b> —R/WC. This bit is set whenever GPIO[27] is seen asserted low. GPIO[27] is always monitored as an input for the purpose of setting this bit, regardless of the actual GPIO configuration.
15:14	Reserved
13	<b>Power Management Event Bus 0 Status (PME_B0_STS)</b> —R/WC. This bit will be set to 1 by the PCH when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN bit and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_EN bit is set, and the system is in an S1–S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. The default for this bit is 0. Writing a 1 to this bit position clears this bit. The following are internal devices which can set this bit: <ul style="list-style-type: none"> <li>• Intel® HD Audio</li> <li>• Intel® Management Engine “maskable” wake events</li> <li>• Integrated LAN</li> <li>• SATA</li> <li>• EHCI</li> <li>• xHCI</li> <li>• Intel® SST</li> </ul>
12	<b>ME SCI Status (ME_SCI_STS)</b> —R/WC. This bit will be set when Intel® ME is requesting an SCI. Software must clear the ME source of the SCI before clearing this bit.
11	<b>Power Management Event Status (PME_STS)</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the PME# signal goes active. Additionally, if the PME_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_STS bit will generate an SCI or SMI# (if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S1–S4 state (or S5 state due to setting SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event. If the system is in an S5 state due to power button override or a power failure, then PME_STS will not cause a wake event or SCI.
10	<b>Battery Low Status (BATLOW_STS)</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = BATLOW# Not asserted 1 = Set by hardware when the BATLOW# signal is asserted.
9	<b>PCI Express* Status (PCI_EXP_STS)</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware to indicate that: <ul style="list-style-type: none"> <li>• The PME event message was received on one or more of the PCI Express* ports</li> <li>• An Assert PMEGPE message received from the processor</li> </ul> <b>Notes:</b> <ol style="list-style-type: none"> <li>1. The PCI WAKE# pin has no impact on this bit.</li> <li>2. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a de-assert PMEGPE message must be received prior to the software write in order for the bit to be cleared.</li> <li>3. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the level-triggered SCI will remain active.</li> <li>4. A race condition exists where the PCI Express* device sends another PME message because the PCI Express* device was not serviced within the time when it must re-send the message. This may result in a spurious interrupt, and this is comprehended and approved by the <i>PCI Express* Specification, Revision 1.0a</i>. The window for this race condition is approximately 95–105 milliseconds.</li> </ol>
8	Reserved

Bit	Description
16	<b>GPIO[27] Status (GP27_STS)</b> —R/WC. This bit is set whenever GPIO[27] is seen asserted low. GPIO[27] is always monitored as an input for the purpose of setting this bit, regardless of the actual GPIO configuration.
15:14	Reserved
13	<b>Power Management Event Bus 0 Status (PME_B0_STS)</b> —R/WC. This bit will be set to 1 by the PCH when any internal device with PCI Power Management capabilities on bus 0 asserts the equivalent of the PME# signal. Additionally, if the PME_B0_EN bit and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_B0_STS bit will generate an SCI (or SMI# if SCI_EN is not set). If the PME_B0_EN bit is set, and the system is in an S1–S4 state (or S5 state due to SLP_TYP and SLP_EN), then the setting of the PME_B0_STS bit will generate a wake event. If the system is in an S5 state due to power button override, then the PME_B0_STS bit will not cause a wake event or SCI. The default for this bit is 0. Writing a 1 to this bit position clears this bit. The following are internal devices which can set this bit: <ul style="list-style-type: none"> <li>• Intel® HD Audio</li> <li>• Intel® Management Engine “maskable” wake events</li> <li>• Integrated LAN</li> <li>• SATA</li> <li>• EHCI</li> <li>• xHCI</li> <li>• Intel® SST</li> </ul>
12	<b>ME SCI Status (ME_SCI_STS)</b> —R/WC. This bit will be set when Intel® ME is requesting an SCI. Software must clear the ME source of the SCI before clearing this bit.
11	<b>Power Management Event Status (PME_STS)</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware when the PME# signal goes active. Additionally, if the PME_EN and SCI_EN bits are set, and the system is in an S0 state, then the setting of the PME_STS bit will generate an SCI or SMI# (if SCI_EN is not set). If the PME_EN bit is set, and the system is in an S1–S4 state (or S5 state due to setting SLP_TYP and SLP_EN), then the setting of the PME_STS bit will generate a wake event. If the system is in an S5 state due to power button override or a power failure, then PME_STS will not cause a wake event or SCI.
10	<b>Battery Low Status (BATLOW_STS)</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = BATLOW# Not asserted 1 = Set by hardware when the BATLOW# signal is asserted.
9	<b>PCI Express* Status (PCI_EXP_STS)</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = Set by hardware to indicate that: <ul style="list-style-type: none"> <li>• The PME event message was received on one or more of the PCI Express* ports</li> <li>• An Assert PMEGPE message received from the processor</li> </ul> <b>Notes:</b> <ol style="list-style-type: none"> <li>1. The PCI WAKE# pin has no impact on this bit.</li> <li>2. If the PCI_EXP_STS bit went active due to an Assert PMEGPE message, then a de-assert PMEGPE message must be received prior to the software write in order for the bit to be cleared.</li> <li>3. If the bit is not cleared and the corresponding PCI_EXP_EN bit is set, the level-triggered SCI will remain active.</li> <li>4. A race condition exists where the PCI Express* device sends another PME message because the PCI Express* device was not serviced within the time when it must re-send the message. This may result in a spurious interrupt, and this is comprehended and approved by the <i>PCI Express* Specification, Revision 1.0a</i>. The window for this race condition is approximately 95–105 milliseconds.</li> </ol>
8	Reserved



Bit	Description
7	<b>SMBus Wake Status (SMB_WAK_STS)</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = Wake event not caused by the PCH's SMBus logic. 1 = Set by hardware to indicate that the wake event was caused by the PCH's SMBus logic. The SMI handler should then clear this bit. <b>NOTES:</b> 1. The SMBus controller will independently cause an SMI#, so this bit does not need to do so (unlike the other bits in this register). 2. This bit is set by the SMBus slave command 01h (Wake/SMI#) even when the system is in the S0 state. Therefore, to avoid an instant wake on subsequent transitions to sleep states, software must clear this bit after each reception of the Wake/SMI# command or just prior to entering the sleep state. 3. The SMBALERT_STS bit (SMB_BASE+00h:Bit 5) should be cleared by software before the SMB_WAK_STS bit is cleared.
6	<b>TCOSCI Status (TCOSCI_STS)</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = TCO logic or thermal sensor logic did Not cause SCI. 1 = Set by hardware when the TCO logic or thermal sensor logic causes an SCI.
5:3	Reserved
2	<b>Software GPE Status (SWGPE_STS)</b> —R/WC. The SWGPE_CTRL bit—bit 1 of GPE_CTRL reg acts as a level input to this bit.
1	<b>Hot-Plug Status (HOT_PLUG_STS)</b> —R/WC. 0 = This bit is cleared by writing a 1 to this bit position. 1 = When a PCI Express* hot-plug event occurs. This will cause an SCI if the HOT_PLUG_EN and SCI_EN bits are set.
0	Reserved

#### 10.7.3.14 GPE0\_EN[31:0]—General Purpose Event 0 Enable [31:0] Register

I/O Address: PMBASE + 90–93h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits  
 Lockable: No      Usage: ACPI  
 Power Well: Bits 7:0, 23:16: Core,  
                  Bit 15:8, 31:24: Suspend

This register is symmetrical to the General Purpose Event 0 Status [31:0] register.

Bit	Description
31:0	<b>GPE0 GPI [31:0] Enable (GPE0_GPI[31:0]_EN)</b> —R/W. These bits enable the corresponding GPI[n]_STS bits being set to cause an SCI and/or wake event.

#### 10.7.3.15 GPE0\_EN[63:32]—General Purpose Event 0 Enable [63:32] Register

I/O Address: PMBASE + 94–97h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits  
 Lockable: No      Usage: ACPI  
 Power Well: Bits 7:0, 23:16: Core,  
                  Bit 15:8, 31:24: Suspend

This register is symmetrical to the General Purpose Event 0 Status [63:32] register.

Bit	Description
31:0	<b>GPE0 GPI [63:32] Enable (GPE0_GPI[63:32]_EN)</b> —R/W. These bits enable the corresponding GPI[n]_STS bits being set to cause an SCI and/or wake event.

#### 10.7.3.16 GPE0\_EN[94:64]—General Purpose Event 0 Enable [94:64] Register

I/O Address:	PMBASE + 98–9Bh	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Usage:	ACPI
Power Well:	Bits 7:0, 31:12: Core, Bit 11:8: Suspend		

This register is symmetrical to the General Purpose Event 0 Status [94:64] register.

Bit	Description
31	Reserved
30:0	<b>GPE0 GPIO [94:64] Enable (GPE0_GPI[94:64]_EN)</b> —R/W. These bits enable the corresponding GPIO[n].STS bits being set to cause an SCI and/or wake event.

#### 10.7.3.17 GPE0\_EN[127:96]—General Purpose Event 0 Enables [127:96] Register

I/O Address:	PMBASE + 9C–9Fh	Attribute:	R/W, RO
Default Value:	0000000000000000h	Size:	32 bits
Lockable:	No	Usage:	ACPI
Power Well:	Bits 31:24, 15:14, 12, 9, 7, 6:0: Suspend, Bit 23:17: DSW, Bit 16, 13, 11, 10, 8: RTC		

This register is symmetrical to the General Purpose Event 0 Status register.

Bit	Description
31:19	Reserved
18	<b>Wake Alarm Device Timer Enable (WADT_EN)</b> —R/W 0 = Disable. 1 = Enable the setting of the WADT_STS bit to generate a wake event/SCI/SMI#.
17	Reserved
16	<b>GPIO[27] Enable (GP27_EN)</b> —R/W 0 = Disable. 1 = Enable the setting of the GP27_STS bit to generate a wake event/SCI/SMI#. The wake enable configuration persists after a G3 state. <b>Note:</b> Host wake events from the PHY through GP27 cannot be disabled by clearing this bit. <b>Note:</b> In the Deep Sx state, GPIO27 has no GPIO functionality other than wake enable capability if this corresponding bit is set. <b>Note:</b> Setting this bit will enable GPIO27 to generate a wake event from Sx or Deep Sx. Setting GPIO_IE27 (GPIOBASE+90h, bit 27) will enable GPIO27 to generate a wake event from Sx only.
15:14	Reserved
13	<b>Power Management Event Bus 0 Enable (PME_B0_EN)</b> —R/W 0 = Disable 1 = Enables the setting of the PME_B0_STS bit to generate a wake event and/or an SCI or SMI#.
12	<b>ME SCI Enable (ME_SCI_EN)</b> —R/W 0 = Disable 1 = Enables the setting of the ME_SCI_STS bit to generate a SCI.
11	<b>Power Management Event Enable (PME_EN)</b> —R/W 0 = Disable. 1 = Enables the setting of the PME_STS bit to generate a wake event and/or an SCI.



Bit	Description
10	<b>Low Battery Enable (BATLOW_EN)</b> —R/W 0 = Disable. 1 = Enables the BATLOW# signal to cause an SMI# or SCI (depending on the SCI_EN bit) when it goes low. This bit does not prevent the BATLOW# signal from inhibiting the wake event.
9	<b>PCI Express* Enable (PCI_EXP_EN)</b> —R/W 0 = Disable SCI generation upon PCI_EXP_STS bit being set. 1 = Enables PCH to cause an SCI when PCI_EXP_STS bit is set. This is used to allow the PCI Express** ports, including the link to the processor, to cause an SCI due to wake/PME events.
8	Reserved
7	Reserved
6	<b>TCOSCI Enable (TCOSCI_EN)</b> —R/W 0 = Disable. 1 = Enables the setting of the TCOSCI_STS to generate an SCI.
5:3	Reserved
2	<b>Software GPE Enable (SWGPE_EN)</b> —R/W. This bit allows software to control the assertion of SWGPE_STS bit. This bit, when set to 1, enables the Software GPE function. If SWGPE_CTRL is written to a 1, hardware will set SWGPE_STS (acts as a level input). If SWGPE_STS, SWGPE_EN, and SCI_EN are all 1s, an SCI will be generated. If SWGPE_STS = 1, SWGPE_EN = 1, SCI_EN = 0, and GBL_SMI_EN = 1, then an SMI# will be generated.
1	<b>Hot-Plug Enable (HOT_PLUG_EN)</b> —R/W 0 = Disables SCI generation upon the HOT_PLUG_STS bit being set. 1 = Enables the PCH to cause an SCI when the HOT_PLUG_STS bit is set. This is used to allow the PCI Express* ports to cause an SCI due to hot-plug events.
0	Reserved

## 10.8 System Management TCO Registers

The TCO logic is accessed using registers mapped to the PCI configuration space (D31:F0) and the system I/O space. For TCO PCI Configuration registers, see LPC D31:F0 PCI Configuration registers.

### TCO Register I/O Map

The TCO I/O registers reside in a 32-byte range pointed to by a TCOBASE value, which is, PMBASE + 60h in the PCI Configuration space. The following table shows the mapping of the registers within that 32-byte range. Each register is described in the following sections.

**Table 10-11. TCO I/O Register Address Map**

TCOBASE + Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	TCO_RLD	TCO Timer Reload and Current Value	0000h	R/W, RO
02h	TCO_DAT_IN	TCO Data In	00h	R/W
03h	TCO_DAT_OUT	TCO Data Out	00h	R/W
04h-05h	TCO1_STS	TCO1 Status	2000h	R/WC, RO
06h-07h	TCO2_STS	TCO2 Status	0000h	R/WC, RO
08h-09h	TCO1_CNT	TCO1 Control	0000h	R/W, R/WLO, R/WC
0Ah-0Bh	TCO2_CNT	TCO2 Control	0008h	R/W
0Ch-0Dh	TCO_MESSAGE1, TCO_MESSAGE2	TCO Message 1 and 2	00h	R/W
0Eh	TCO_WDCNT	TCO Watchdog Control	00h	R/W
0Fh	—	Reserved	—	—
10h	SW_IRQ_GEN	Software IRQ Generation	03h	R/W
11h	—	Reserved	—	—
12h-13h	TCO_TMR	TCO Timer Initial Value	0004h	R/W
14h-1Fh	—	Reserved	—	—

### 10.8.1 TCO\_RLD—TCO Timer Reload and Current Value Register

I/O Address:	TCOBASE +00h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:10	Reserved
9:0	<b>TCO Timer Value</b> —R/W. Reading this register will return the current count of the TCO timer. Writing any value to this register will reload the timer to prevent the timeout.

### 10.8.2 TCO\_DAT\_IN—TCO Data In Register

I/O Address:	TCOBASE +02h	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	<b>TCO Data In Value</b> —R/W. This data register field is used for passing commands from the operating system to the SMI handler. Writes to this register will cause an SMI and set the SW_TCO_SMI bit in the TCO1_STS register (D31:F0:04h).

### 10.8.3 TCO\_DAT\_OUT—TCO Data Out Register

I/O Address:	TCOBASE +03h	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Core

Bit	Description
7:0	<b>TCO Data Out Value</b> —R/W. This data register field is used for passing commands from the SMI handler to the operating system. Writes to this register will set the TCO_INT_STS bit in the TCO1_STS register. It will also cause an interrupt, as selected by the TCO_INT_SEL bits.

## 10.8.4 TCO1\_STS—TCO1 Status Register

I/O Address:	TCOBASE +04h	Attribute:	R/WC, RO
Default Value:	2000h	Size:	16-bit
Lockable:	No	Power Well:	Core (Except bit 7, in RTC)

Bit	Description
15:14	Reserved
13	<b>TCO_SLVSEL (TCO Slave Select)</b> —RO. This register bit is read-only by Host and indicates the value of TCO Slave Select soft strap. Refer to the PCH soft straps section of the SPI Chapter for details.
12	<b>DMISERR_STS</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = PCH received a DMI special cycle message using DMI indicating that it wants to cause an SERR#. The software must read the processor to determine the reason for the SERR#.
11	Reserved
10	<b>DMISMI_STS</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = PCH received a DMI special cycle message using DMI indicating that it wants to cause an SMI. The software must read the processor to determine the reason for the SMI.
9	<b>DMISCI_STS</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = PCH received a DMI special cycle message using DMI indicating that it wants to cause an SCI. The software must read the processor to determine the reason for the SCI.
8	<b>BIOSWR_STS</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = PCH sets this bit and generates an SMI# to indicate an invalid attempt to write to the BIOS. This occurs when either: a) The BIOSWP bit is changed from 0 to 1 and the BLD bit is also set, or b) any write is attempted to the BIOS and the BIOSWP bit is also set. <b>Note:</b> On write cycles attempted to the 4MB lower alias to the BIOS space, the BIOSWR_STS will not be set.
7	<b>NEWCENTURY_STS</b> —R/WC. This bit is in the RTC well. 0 = Cleared by writing a 1 to the bit position or by RTCRST# going active. 1 = This bit is set when the Year byte (RTC I/O space, index offset 09h) rolls over from 99 to 00. Setting this bit will cause an SMI# (but not a wake event). <b>Note:</b> The NEWCENTURY_STS bit is not valid when the RTC battery is first installed (or when RTC power has not been maintained). Software can determine if RTC power has not been maintained by checking the RTC_PWR_STS bit (D31:F0:A4h, bit 2), or by other means (such as a checksum on RTC RAM). If RTC power is determined to have not been maintained, BIOS should set the time to a valid value and then clear the NEWCENTURY_STS bit. The NEWCENTURY_STS bit may take up to 3 RTC clocks for the bit to be cleared after a 1 is written to the bit to clear it. After writing a 1 to this bit, software should not exit the SMI handler until verifying that the bit has actually been cleared. This will ensure that the SMI is not re-entered.
6:4	Reserved
3	<b>TIMEOUT</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = Set by PCH to indicate that the SMI was caused by the TCO timer reaching 0.
2	<b>TCO_INT_STS</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = SMI handler caused the interrupt by writing to the TCO_DAT_OUT register (TCOBASE + 03h).
1	<b>SW_TCO_SMI</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = Software caused an SMI# by writing to the TCO_DAT_IN register (TCOBASE + 02h).
0	<b>NMI2SMI_STS</b> —RO 0 = Cleared by clearing the associated NMI status bit. 1 = Set by the PCH when an SMI# occurs because an event occurred that would otherwise have caused an NMI (because NMI2SMI_EN is set).



## 10.8.5 TCO2\_STS—TCO2 Status Register

I/O Address:	TCOBASE +06h	Attribute:	R/WC, RO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Resume (Except Bit 0, in RTC)

Bit	Description
15:5	Reserved
4	<b>SMLink Slave SMI Status (SMLINK_SLV_SMI_STS)</b> —R/WC. Allow the software to go directly into a pre-determined sleep state. This avoids race conditions. Software clears this bit by writing a 1 to it. 0 = The bit is reset by RSMRST#, but not due to the PCI Reset associated with exit from S3–S5 states. 1 = PCH sets this bit to 1 when it receives the SMI message on the SMLink Slave Interface.
3:2	Reserved
1	<b>SECOND_TO_STS</b> —R/WC 0 = Software clears this bit by writing a 1 to it, or by a RSMRST#. 1 = PCH sets this bit to 1 to indicate that the TIMEOUT bit had been (or is currently) set and a second timeout occurred before the TCO_RLD register was written. If this bit is set and the NO_REBOOT Configuration bit is 0, then the PCH will reboot the system after the second timeout. The reboot is done by asserting PLTRST#.
0	<b>Intruder Detect (INTRD_DET)</b> —R/WC 0 = Software clears this bit by writing a 1 to it, or by RTCRST# assertion. 1 = Set by PCH to indicate that an intrusion was detected. This bit is set even if the system is in G3 state.  <b>Notes:</b> 1. This bit has a recovery time. After writing a 1 to this bit position (to clear it), the bit may be read back as a 1 for up to 65 microseconds before it is read as a 0. Software must be aware of this recovery time when reading this bit after clearing it. 2. If the INTRUDER# signal is active when the software attempts to clear the INTRD_DET bit, the bit will remain as a 1, and the SMI# will be generated again immediately. The SMI handler can clear the INTRD_SEL bits (TCOBASE + 0Ah, bits 2:1), to avoid further SMIs. However, if the INTRUDER# signal goes inactive and then active again, there will not be further SMIs (because the INTRD_SEL bits would select that no SMI# be generated). 3. If the INTRUDER# signal goes inactive some point after the INTRD_DET bit is written as a 1, then the INTRD_DET signal will go to a 0 when INTRUDER# input signal goes inactive. This is slightly different than a classic sticky bit, since most sticky bits would remain active indefinitely when the signal goes active and would immediately go inactive when a 1 is written to the bit.

## 10.8.6 TCO1\_CNT—TCO1 Control Register

I/O Address: TCOBASE +08h      Attribute: R/W, R/WLO, R/WC  
Default Value: 0000h      Size: 16 bits  
Lockable: No      Power Well: Core

Bit	Description																	
15:13	Reserved																	
12	<b>TCO_LOCK</b> —R/WLO. When set to 1, this bit prevents writes from changing the TCO_EN bit (in offset 30h of Power Management I/O space). Once this bit is set to 1, it can not be cleared by software writing a 0 to this bit location. A core-well reset is required to change this bit from 1 to 0. This bit defaults to 0.																	
11	<b>TCO Timer Halt (TCO_TMR_HLT)</b> —R/W 0 = The TCO Timer is enabled to count. 1 = The TCO Timer will halt. It will not count, and thus cannot reach a value that will cause an SMI# or set the SECOND_TO_STS bit. When set, this bit will prevent rebooting and prevent Alert On LAN event messages from being transmitted on the SMLink (but not Alert On LAN heartbeat messages).																	
10	Reserved																	
9	<b>NMI2SMI_EN</b> —R/W 0 = Normal NMI functionality. 1 = Forces all NMIs to instead cause SMIs. The functionality of this bit is dependent upon the settings of the NMI_EN bit and the GBL_SMI_EN bit as detailed in the following table.																	
	<table> <thead> <tr> <th>NMI_EN</th> <th>GBL_SMI_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>0b</td> <td>No SMI# at all because GBL_SMI_EN = 0</td> </tr> <tr> <td>0b</td> <td>1b</td> <td>SMI# will be caused due to NMI events</td> </tr> <tr> <td>1b</td> <td>0b</td> <td>No SMI# at all because GBL_SMI_EN = 0</td> </tr> <tr> <td>1b</td> <td>1b</td> <td>No SMI# due to NMI because NMI_EN = 1</td> </tr> </tbody> </table>			NMI_EN	GBL_SMI_EN	Description	0b	0b	No SMI# at all because GBL_SMI_EN = 0	0b	1b	SMI# will be caused due to NMI events	1b	0b	No SMI# at all because GBL_SMI_EN = 0	1b	1b	No SMI# due to NMI because NMI_EN = 1
NMI_EN	GBL_SMI_EN	Description																
0b	0b	No SMI# at all because GBL_SMI_EN = 0																
0b	1b	SMI# will be caused due to NMI events																
1b	0b	No SMI# at all because GBL_SMI_EN = 0																
1b	1b	No SMI# due to NMI because NMI_EN = 1																
8	<b>NMI_NOW</b> —R/WC 0 = Software clears this bit by writing a 1 to it. The NMI handler is expected to clear this bit. Another NMI will not be generated until the bit is cleared. 1 = Writing a 1 to this bit causes an NMI. This allows the BIOS or SMI handler to force an entry to the NMI handler.																	
7:0	Reserved																	

### 10.8.7 TCO2\_CNT—TCO2 Control Register

I/O Address:	TCOBASE +0Ah	Attribute:	R/W
Default Value:	0008h	Size:	16 bits
Lockable:	No	Power Well:	Resume

Bit	Description
15:6	Reserved
5:4	<p><b>OS_POLICY</b>—R/W. OS-based software writes to these bits to select the policy that the BIOS will use after the platform resets due to the WDT. The following convention is recommended for the BIOS and OS:</p> <p>00 = Boot normally 01 = Shut down 10 = Do not load operating system. Hold in pre-boot state and use LAN to determine next step 11 = Reserved</p> <p><b>Note:</b> These are just scratchpad bits. They should not be reset when the TCO logic resets the platform due to Watchdog Timer.</p>
3	<p><b>GPIO11_ALERT_DISABLE</b>—R/W. At reset (using RSMRST# asserted) this bit is set and GPIO11 alerts are disabled.</p> <p>0 = Enable. 1 = Disable GPIO11/SMBALERT# as an alert source for the heartbeats and the SMBus slave.</p>
2:1	<p><b>INTRD_SEL</b>—R/W. This field selects the action to take if the INTRUDER# signal goes active.</p> <p>00 = No interrupt or SMI# 01 = Interrupt (as selected by TCO_INT_SEL). 10 = SMI 11 = Reserved</p>
0	Reserved

### 10.8.8 TCO\_MESSAGE1 and TCO\_MESSAGE2 Registers

I/O Address:	TCOBASE +0Ch (Message 1)	Attribute:	R/W
	TCOBASE +0Dh (Message 2)		
Default Value:	00h	Size:	8 bits
Lockable:	No	Power Well:	Resume

Bit	Description
7:0	<b>TCO_MESSAGE[n]</b> —R/W. BIOS can write into these registers to indicate its boot progress. The external microcontroller can read these registers to monitor the boot progress.



### 10.8.9 TCO\_WDCNT—TCO Watchdog Control Register

Offset Address: TCOBASE + 0Eh Attribute: R/W  
Default Value: 00h Size: 8 bits  
Power Well: Resume

Bit	Description
7:0	The BIOS or system management software can write into this register to indicate more details on the boot progress. The register will reset to 00h based on a RSMRST# (but not PLTRST#). The external microcontroller can read this register to monitor boot progress.

### 10.8.10 SW\_IRQ\_GEN—Software IRQ Generation Register

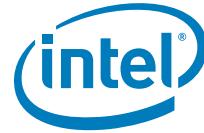
Offset Address: TCOBASE + 10h Attribute: R/W  
Default Value: 03h Size: 8 bits  
Power Well: Core

Bit	Description
7:2	Reserved
1	<b>IRQ12_CAUSE</b> —R/W. When software sets this bit to 1, IRQ12 will be asserted. When software sets this bit to 0, IRQ12 will be de-asserted.
0	<b>IRQ1_CAUSE</b> —R/W. When software sets this bit to 1, IRQ1 will be asserted. When software sets this bit to 0, IRQ1 will be de-asserted.

### 10.8.11 TCO\_TMR—TCO Timer Initial Value Register

I/O Address: TCOBASE +12h Attribute: R/W  
Default Value: 0004h Size: 16 bits  
Lockable: No Power Well: Core

Bit	Description
15:10	Reserved
9:0	<b>TCO Timer Initial Value</b> —R/W. Value that is loaded into the timer each time the TCO_RLD register is written. Values of 0000h or 0001h will be ignored and should not be attempted. The timer is clocked at approximately 0.6 seconds, and thus allows timeouts ranging from 1.2 second to 613.8 seconds. <b>Note:</b> The timer has an error of $\pm 1$ tick (0.6 seconds). The TCO Timer will only count down in the S0 state.



## 10.9 General Purpose I/O Registers

The control for the general purpose I/O signals is handled through a 1 Kbyte I/O space. The base offset for this space is selected by the GPIOBASE register.

**Note:** Unused GPIOs should be individually tied to power to ensure the input buffer is stable and not dissipating needless power. However, additional power savings (up to 5  $\mu$ W per unused GPIO in some corner and high temperature cases) can be achieved if these unused GPIOs are pulled down to ground instead of pulled up to power. In either case, the value of the resistor used should be in the range of 4.7  $\text{K}\Omega$  to 50  $\text{K}\Omega$ . The unused GPIOs should remain configured in default GPIO state and input sensing should be disabled by setting the corresponding GPIOs B.GPINDIS = 1.

**Table 10-12. Registers to Control GPIO Address Map (Sheet 1 of 2)**

GPIOBASE + Offset	Mnemonic	Register Name	Default	Attribute
00h-03h	GPIO_OWN[31:0]	GPIO Ownership	B96BA1FFh	R/W
04h-07h	GPIO_OWN[63:32]	GPIO Ownership	EEFF6EFFh	R/W
08h-0Bh	GPIO_OWN[94:64]	GPIO Ownership	0h	R/W
0Ch-0Fh	—	Reserved	02FE0100h	—
10h-11h	GPIPIRQ2IOXAPIC	GPI PIRQ to IOxAPIC Enable	0000h	R/W
12h-17h	—	Reserved	0h	—
18h-1Bh	GPO_BLINK	GPIO Blink Enable	00040000h	R/W
1Ch-1Fh	GP_SER_BLINK	GP Serial Blink	00000000h	R/W
20h-23h	GP_SB_CMDSTS	GP Serial Blink Command Status	00008000h	R/W, RO
24h-27h	GP_GB_DATA[31:0]	GP Serial Blink Data	00000000h	R/W
28h-29h	GPI_NMI_EN[47:32]	GPI NMI Enable [47:32]	0000h	R/W
2Ah-2Bh	GPI_NMI_STS[47:32]	GPI NMI Status [47:32]	0000h	R/WC
2Ch-2Fh	—	Reserved	00000000h	R/W
30h-33h	GPI_ROUT[94:0]	GPI Interrupt Input Route	020300FEh (Mobile only) / 020300FFh (Desktop only)	R/W
3Ch-3Fh	—	Reserved	0h	—
40h-43h	—	Reserved	00000030h (mobile only)/ 00000130h (desktop only)	R/W
44h-47h	—	Reserved	00000FF0h	R/W
48h-4Bh	—	Reserved	000000C0h	R/W
4Ch-4Fh	—	Reserved	—	—
50h-53h	ALT_GPI_SMI_STS[47:32]	Alternate GPIO SMI Status	000000C0h	R/WC, RO
54h-57h	ALT_GPI_SMI_EN[47:32]	Alternate GPIO SMI Enable	000000C0h	R/W, RO
58h-5Fh	—	Reserved	—	—
60h-63h	GP_RST_SEL[31:0]	GPIO Reset Select 1	01000000h	R/W, RO
64h-67h	GP_RST_SEL[63:32]	GPIO Reset Select 2	00000000h	R/W, RO
68h-6Bh	GP_RST_SEL[94:64]	GPIO Reset Select 3	00000000h	R/W, RO
6Ch-7Bh	—	Reserved	—	—
7Ch-7Fh	GPIO_GC	GPIO Global Configuration	00000000h	R/W
80h-83h	GPI_IS[31:0]	GPI Interrupt Status [31:0]	00000000h	R/WC
84h-87h	GPI_IS[63:32]	GPI Interrupt Status [63:32]	00000000h	R/WC
88h-8Bh	GPI_IS[94:64]	GPI Interrupt Status [94:64]	00000000h	R/WC
90h-93h	GPI_IE[31:0]	GPI Interrupt Enable [31:0]	00000000h	R/W

**Table 10-12. Registers to Control GPIO Address Map (Sheet 2 of 2)**

GPIOBASE + Offset	Mnemonic	Register Name	Default	Attribute
94h-97h	GPI_IE[63:32]	GPIO Interrupt Enable [63:32]	00000000h	R/W
98h-9Bh	GPI_IE[94:64]	GPIO Interrupt Enable [94:64]	00000000h	R/W
100h + n*8h	GPnCONFIGA	GPIO Configuration A	see register description	R/W, RO
104h + n*8h	GPnCONFIGB	GPIO Configuration B	see register description	R/W, RO

### 10.9.1 **GPIO\_OWN[31:0]—GPIO Ownership Register**

Offset Address: GPIOBASE + 00h Attribute: R/W  
 Default Value: see below Size: 32 bits  
 Lockable: No Power Well: Core for 0:7, 16:23,  
 Resume for 8:15, 24:31

Bit	Description
31:0	<b>GPIO_OWN[31:0]</b> —R/W. With GPIO_USE_SEL[n] selecting GPIO mode, GPIO_OWN[n] (where n is the pin number) determines the appropriate status bit update. 0 = (ACPI driver) GPIO controller ensures that GPIO[n] event shall be reflected in GPE01.GPI_STS, GPI_NMI_STS, and ALT_GPI_SMI_STS register. GPI_IS update is masked. 1 = (GPIO driver) GPIO controller ensures that GPIO[n] event shall be reflected in the GPI_IS[n]. GPE01.GPI_STS, GPI_NMI_STS, and ALT_GPI_SMI_STS updates are masked. If a pin[n] is unassigned, then the Ownership register bit[n] is recommended to be left at default value.

### 10.9.2 **GPIO\_OWN[63:32]—GPIO Ownership Register**

Offset Address: GPIOBASE + 04h Attribute: R/W  
 Default Value: see below Size: 32 bits  
 Lockable: No Power Well: Core for 0:7, 16:23,  
 Resume for 8:15, 24:31

Bit	Description
31:0	<b>GPIO_OWN[63:32]</b> —R/W. With GPIO_USE_SEL[n] selecting GPIO mode, GPIO_OWN[n] (where n is the pin number) determines the appropriate status bit update. 0 = (ACPI driver) GPIO controller ensures that GPIO[n] event shall be reflected in GPE01.GPI_STS, GPI_NMI_STS and ALT_GPI_SMI_STS register. GPI_IS update is masked. 1 = (GPIO driver) GPIO controller ensures that GPIO[n] event shall be reflected in the GPI_IS[n]. GPE01.GPI_STS, GPI_NMI_STS and ALT_GPI_SMI_STS updates are masked. If a pin[n] is unassigned, then the Ownership register bit[n] is recommended to be left at default value.



### 10.9.3 GPIO\_OWN[94:64]—GPIO Ownership Register

Offset Address:	GPIOBASE +08h	Attribute:	R/W
Default Value:	see below	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	<b>GPIO_OWN[94:64]</b> —R/W. With GPIO_USE_SEL[n] selecting GPIO mode, GPIO_OWN[n] (where n is the pin number) determines the appropriate status bit update. 0 = (ACPI driver) GPIO controller ensures that GPIO[n] event shall be reflected in GPE01.GPI_STS, GPI_NMI_STS and ALT_GPI_SMI_STS register. GPI_IS update is masked. 1 = (GPIO driver) GPIO controller ensures that GPIO[n] event shall be reflected in the GPI_IS[n]. GPE01.GPI_STS, GPI_NMI_STS and ALT_GPI_SMI_STS updates are masked. If a pin[n] is unassigned, then the Ownership register bit[n] is recommended to be left at default value.

### 10.9.4 GPIPIRQ2IOXAPIC—GPI PIRQ to IOxAPIC Enable Register

Offset Address:	GPIOBASE +10h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core for 0:15

Bit	Description
15:0	<b>GPI PIRQ to IOxAPIC Enable</b> —R/W. GPIPIRQ2IOXAPIC enables the corresponding GPIO PIRQ[X:I] pin to generate IOxAPIC interrupt[39:24]. 0 = GPI Peripheral IRQ is masked from IOxAPIC. 1 = GPI is routed as Peripheral IRQ to IOxAPIC. Bit[15] corresponds to PIRQ[X] and IOxAPIC[39]. Bit[14:1] corresponds to PIRQ[W:J] and IOxAPIC[38:25], respectively. Bit[0] corresponds to PIRQ[I] and IOxAPIC[24].

### 10.9.5 GPO\_BLINK—GPO Blink Enable Register

Offset Address:	GPIOBASE +18h	Attribute:	R/W
Default Value:	see below	Size:	32 bits
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	<b>GP_BLINK[31:0]</b> —R/W. The setting of this bit has no effect if the corresponding GPIO signal is programmed as an input or the GPIO is not blink-capable. 0 = The corresponding GPIO will function normally. 1 = If the corresponding GPIO is programmed as an output, the output signal will blink at a rate of approximately once per second. The high and low times have approximately 0.5 seconds each. The GP_LVL bit is not altered when this bit is set. The value of the corresponding GP_LVL bit remains unchanged during the blink process, and does not effect the blink in any way. The GP_LVL bit is not altered when programmed to blink. It will remain at its previous value. When configured in native mode, writes to these bits have no effect. The value reported in this register is undefined when programmed as native mode. These bits revert to the default value based on RSMRST# or a write to the CF9h register (but not just on PLTRST#).

## 10.9.6 GP\_SER\_BLINK—GP Serial Blink Register

Offset Address:	GPIOBASE +1Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	<p><b>GP_SER_BLINK[31:0]</b>—R/W. The setting of this bit has no effect if the corresponding GPIO is programmed as an input or if the corresponding GPIO has the GPO_BLINK bit set.</p> <p>0 = The corresponding GPIO will function normally.</p> <p>1 = When using serial blink, this bit should be set to a 1 while the corresponding GP_IO_SEL bit is set to 1. Setting the GP_IO_SEL bit to 0 after the GP_SER_BLINK bit ensures PCH will not drive a 1 on the pin as an output. When this corresponding bit is set to a 1 and the pin is configured to output mode, the serial blink capability is enabled. The PCH will serialize messages through an open-drain buffer configuration.</p> <p>The value of the corresponding GP_LVL bit remains unchanged and does not impact the serial blink capability in any way.</p> <p>Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined.</p>

## 10.9.7 GP\_SB\_CMDSTS—GP Serial Blink Command Status Register

Offset Address:	GPIOBASE +20h	Attribute:	R/W, RO
Default Value:	00000800h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:24	Reserved
23:22	<p><b>Data Length Select (DLS)</b>—R/W. This field determines the number of bytes to serialize on GPIO.</p> <p>00 = Serialize bits 7:0 of GP_SB_DATA (1 byte)</p> <p>01 = Serialize bits 15:0 of GP_SB_DATA (2 bytes)</p> <p>10 = Undefined – Software must not write this value</p> <p>11 = Serialize bits 31:0 of GP_SB_DATA (4 bytes)</p> <p>Software should not modify the value in this register unless the Busy bit is clear. Writes to this register have no effect when the corresponding pin is configured in native mode and the read value returned is undefined.</p>
21:16	<p><b>Data Rate Select (DRS)</b>—R/W. This field selects the number of 166.67 ns time intervals (4 clock periods of 24 MHz clock) to count between Manchester data transitions. The default of 8h results in a 1333.33 ns minimum time between transitions. A value of 0h in this register field produces undefined behavior.</p> <p>Software should not modify the value in this register field unless the Busy bit is clear.</p>
15:9	Reserved
8	<p><b>Busy</b>—RO. This read-only status bit is the hardware indication that a serialization is in progress. Hardware sets this bit to 1 based on the Go bit being set. Hardware clears this bit when the Go bit is cleared by the hardware.</p>
7:1	Reserved
0	<p><b>Go</b>—R/W. This bit is set to 1 by software to start the serialization process. Hardware clears the bit after the serialized data is sent. Writes of 0 to this register bit have no effect. Software should not write this bit to 1 unless the Busy status bit is cleared.</p>



### 10.9.8 GP\_GB\_DATA[31:0]—GP Serial Blink Data Register

Offset Address:	GPIOBASE +24h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core

Bit	Description
31:0	<b>GP_GB_DATA[31:0]</b> —R/W. This register contains the data serialized out. The number of bits shifted out are selected through the DLS field in the GP_SB_CMDSTS register. This register should not be modified by software when the Busy bit is set.

### 10.9.9 GPI\_NMI\_EN[47:32]—GPI NMI Enable Register

Offset Address:	GPIOBASE +28h	Attribute:	R/W
Default Value:	00000h	Size:	16 bits
Lockable:	Yes	Power Well:	Core for 0:7 Resume for 8:15

Bit	Description
15:0	<b>GPI_NMI_EN[47:32]</b> —R/W. This bit only has effect if the corresponding GPIO is used as an input and its GPI_ROUT register is being programmed to NMI functionality. When set to 1, it used to allow active-low and active-high inputs (depends on inversion bit) to cause NMI.

### 10.9.10 GPI\_NMI\_STS[47:32]—GPI NMI Status Register

Offset Address:	GPIOBASE +2Ah	Attribute:	R/WC
Default Value:	00000h	Size:	16 bits
Lockable:	No	Power Well:	Core for 0:7 Resume for 8:15

Bit	Description
15:0	<b>GPI_NMI_STS[47:32]</b> —R/WC. This bit is set if the corresponding GPIO is used as in GPIO mode, set up as an input, and its GPI_ROUT register is being programmed to NMI functionality and also GPI_NMI_EN bit is set when it detects either: 1) active-high edge when its corresponding GPI_INV is configured with value 0. 2) active-low edge when its corresponding GPI_INV is configured with value 1. <b>Note:</b> Writing value of 1 will clear the bit, while writing value of 0 have no effect.

### 10.9.11 **GPI\_ROUT[94:0]**—GPIO Input Route Register

Offset Address:	GPIOBASE +30h	Attribute:	R/W
Default Value:	see below	Size:	96 bits
Lockable:	No		
Power Well:	Core for 0:7, 16:23, 39:32, 55:41, 71:64, 87:80 Resume for 8:15, 24:31, 47:40, 63:56, 79:72, 95:88		

Bit	Description
95	Reserved
94:0	<p><b>GPI_ROUT[94:0]</b>—R/W. If GPIO[n] is implemented and set to GPIO Mode input, the pin can be routed to cause NMI (if supported by pin), SMI (if supported by pin) or SCI. If the GPIO is not set to GPIO Mode input, this field has no effect.</p> <p>0 = SCI, 1 = NMI or SMI (dependant on the respective NMI_EN or ALT_GPI_SMI_EN enable bit)</p> <p><b>Note:</b> Not all pins are SMI/NMI trigger capable. Refer to GPI SMI Enable and NMI Enable register sections.</p>

### 10.9.12 **ALT\_GPI\_SMI\_STS[47:32]**—Alternate GPI SMI Status Register

Offset Address:	GPIOBASE +50h	Attribute:	R/WC, RO
Default Value:	000000C0h	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

This register corresponds to GPIO[47:32]. Bit 0 corresponds to GPIO32 and bit 15 corresponds to GPIO47.

Bit	Description
31:16	Reserved
15:0	<p><b>ALT_GPI_SMI_STS[47:32]</b>—R/WC</p> <p>These bits report the status of the corresponding GPIOs if GPIO_USE_SEL[n]=„1“.</p> <p>0 = Inactive 1 = Active</p> <p>These bits are sticky. If the following conditions are true, then an SMI# will be generated if the ALT_GPI_SMI_STS bit set:</p> <ol style="list-style-type: none"> <li>1. The corresponding bit in the ALT_GPI_SMI_EN register is set</li> <li>2. The corresponding GPIO must be routed in the GPI_ROUT register to cause an SMI.</li> <li>3. The corresponding GPIO must be implemented.</li> </ol> <p>Default for these bits are dependent on the state of the GPIO pins.</p> <p>When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits are ignored and have no effect to the pin value. The value reported in this register is undefined when programmed as native mode.</p>



### 10.9.13 ALT\_GPI\_SMI\_EN[47:32]—Alternate GPI SMI Enable Register

Offset Address:	GPIOBASE +54h	Attribute:	R/W, RO
Default Value:	000000C0h	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

This register corresponds to GPIO[47:32]. Bit 0 corresponds to GPIO32 and bit 15 corresponds to GPIO47.

Bit	Description
31:16	Reserved.
15:0	<p><b>ALT_GPI_SMI_EN[47:32]</b>—R/W. These bits are used to enable the corresponding GPI to cause an SMI#. If GPIO_USE_SEL[n] = "1".</p> <p>0 = Disable SMI# generation. 1 = Enable SMI# generation.</p> <p>These bits are sticky. If the following conditions are true, then an SMI# will be generated if the ALT_GPI_SMI_STS bit set:</p> <ol style="list-style-type: none"> <li>1. The corresponding bit in the ALT_GPI_SMI_STS register is set</li> <li>2. The corresponding GPI must be routed in the GPI_ROUT register to cause an SMI.</li> <li>3. The corresponding GPIO must be implemented.</li> </ol> <p>Default for these bits are dependent on the state of the GPI pins.</p> <p>When configured in native mode (GPIO_USE_SEL[n] is 0), writes to these bits are ignored and have no effect to the pin value. The value reported in this register is undefined when programmed as native mode.</p>

### 10.9.14 GP\_RST\_SEL[31:0]—GPIO Reset Select Register

Offset Address:	GPIOBASE +60h	Attribute:	R/W, RO
Default Value:	01000000h	Size:	32 bits
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:24	<p><b>GP_RST_SEL[31:24]</b>—R/W.</p> <p>0 = Corresponding GPIO registers will be reset by SYS_RESET# assertion or CF9h reset (06h or 0Eh). 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.</p> <p><b>Note:</b> GPIO[24] register bits are not cleared by CF9h reset by default. <b>Note:</b> Corresponding GPIO registers will NOT reset during Sx transition. SYS_RESET# is a CORE well pin and is un-driven in Sx states.</p>
23:16	Reserved
15:8	<p><b>GP_RST_SEL[15:8]</b>—R/W.</p> <p>0 = Corresponding GPIO registers will be reset by SYS_RESET# assertion or CF9h reset (06h or 0Eh). 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.</p> <p><b>Note:</b> Corresponding GPIO registers will NOT reset during Sx transition. SYS_RESET# is a CORE well pin and is un-driven in Sx states.</p>
7:0	Reserved

### 10.9.15 GP\_RST\_SEL[63:32]—GPIO Reset Select Register

Offset Address:	GPIOBASE +64h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	Yes	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:24	<b>GP_RST_SEL[63:56]</b> —R/W 0 = Corresponding GPIO registers will be reset by SYS_RESET# assertion or CF9h reset (06h or 0Eh). 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.  <b>Note:</b> Corresponding GPIO registers will NOT reset during Sx transition. SYS_RESET# is a CORE well pin and is un-driven in Sx states.
23:16	Reserved
15:8	<b>GP_RST_SEL[47:40]</b> —R/W 0 = Corresponding GPIO registers will be reset by SYS_RESET# assertion or CF9h reset (06h or 0Eh). 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.  <b>Note:</b> Corresponding GPIO registers will NOT reset during Sx transition. SYS_RESET# is a CORE well pin and is un-driven in Sx states.
7:0	Reserved

### 10.9.16 GP\_RST\_SEL[75:64]—GPIO Reset Select Register

Offset Address:	GPIOBASE +68h	Attribute:	R/W, RO
Default Value:	00000000h	Size:	32 bits
Lockable:	Yes	Power Well:	Core for 0:7, 12:31, Resume for 8:11

Bit	Description
31:12	Reserved
11:8	<b>GP_RST_SEL[75:72]</b> —R/W 0 = Corresponding GPIO registers will be reset by SYS_RESET# assertion or CF9h reset (06h or 0Eh). 1 = Corresponding GPIO registers will be reset by RSMRST# assertion only.  <b>Note:</b> Corresponding GPIO registers will NOT reset during Sx transition. SYS_RESET# is a CORE well pin and is un-driven in Sx states.
7:0	Reserved

### 10.9.17 GPIO\_GC—GPIO Global Configuration Register

Offset Address:	GPIOBASE + 7Ch	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Resume

Bit	Description
31:2	Reserved.
1:0	<b>GPIO_IRQ_ROUTE[1:0]</b> —R/W. Specifies the APIC IRQ globally for all GPIO pins (GPI_IS with corresponding GPI_IE). 00 = IRQ14 01 = IRQ15 10 = reserved 11 = reserved

### 10.9.18 GPI\_IS[31:0]—GPI Interrupt Status [31:0] Register

Offset Address:	GPIOBASE + 80h	Attribute:	R/WC, R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description												
31:0	<p><b>GPI Interrupt Status (GPI_IS[31:0])</b>—R/WC. This bit is set if:</p> <ol style="list-style-type: none"> <li>1. The corresponding GPIO_OWN[31:0] bit n = '1' to indicate GPIO driver ownership</li> <li>2. The corresponding GPnConfigA.GPIO_USE_SEL='1' to indicate GPIO Mode</li> <li>3. An edge or level event is detected</li> </ol> <p>If the corresponding GPnConfigA.GPI_LxEb='0' to indicate Edge Mode:</p> <table border="1"> <tr> <th>GPnConfigA.GPI_INV</th> <th>GPI_IS[31:0] bit n is set to '1' by</th> </tr> <tr> <td>0</td> <td>Pin rising edge</td> </tr> <tr> <td>1</td> <td>Pin falling edge</td> </tr> </table> <p>If the corresponding GPnConfigA.GPI_LxEb='1' to indicate Level Mode:</p> <table border="1"> <tr> <th>GPnConfigA.GPI_INV</th> <th>GPI_IS[31:0] bit n is set to '1' by</th> </tr> <tr> <td>0</td> <td>Pin at '1' level</td> </tr> <tr> <td>1</td> <td>Pin at '0' level</td> </tr> </table> <p><b>Note:</b> The state of GPI_IE[31:0] bit n does not prevent the setting of the corresponding GPI_IS[31:0] bit n. Software writes '1' to clear a bit.</p>	GPnConfigA.GPI_INV	GPI_IS[31:0] bit n is set to '1' by	0	Pin rising edge	1	Pin falling edge	GPnConfigA.GPI_INV	GPI_IS[31:0] bit n is set to '1' by	0	Pin at '1' level	1	Pin at '0' level
GPnConfigA.GPI_INV	GPI_IS[31:0] bit n is set to '1' by												
0	Pin rising edge												
1	Pin falling edge												
GPnConfigA.GPI_INV	GPI_IS[31:0] bit n is set to '1' by												
0	Pin at '1' level												
1	Pin at '0' level												

## 10.9.19 **GPI\_IS[63:32]**—GPI Interrupt Status [63:32] Register

Offset Address:	GPIOBASE +84h	Attribute:	R/WC, R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description													
31:0	<p><b>GPI Interrupt Status (GPI_IS[63:32])</b>—R/WC. This bit is set if:</p> <ol style="list-style-type: none"> <li>1. The corresponding GPIO_OWN[63:32] bit n = '1' to indicate GPIO driver ownership</li> <li>2. The corresponding GPnConfigA.GPIO_USE_SEL='1' to indicate GPIO Mode</li> <li>3. An edge or level event is detected</li> </ol> <p>If the corresponding GPnConfigA.GPIO_LxEb='0' to indicate Edge Mode:</p> <table border="1"> <thead> <tr> <th>GPnConfigA.GPIO_INV</th> <th>GPIO_IS[63:32] bit n is set to '1' by</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Pin rising edge</td> </tr> <tr> <td>1</td> <td>Pin falling edge</td> </tr> </tbody> </table> <p>If the corresponding GPnConfigA.GPIO_LxEb='1' to indicate Level Mode:</p> <table border="1"> <thead> <tr> <th>GPnConfigA.GPIO_INV</th> <th>GPIO_IS[63:32] bit n is set to '1' by</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Pin at '1' level</td> </tr> <tr> <td>1</td> <td>Pin at '0' level</td> </tr> </tbody> </table> <p><b>Note:</b> The state of GPIO_IE[63:32] bit n does not prevent the setting of the corresponding GPIO_IS[63:32] bit n. Software writes '1' to clear a bit.</p>		GPnConfigA.GPIO_INV	GPIO_IS[63:32] bit n is set to '1' by	0	Pin rising edge	1	Pin falling edge	GPnConfigA.GPIO_INV	GPIO_IS[63:32] bit n is set to '1' by	0	Pin at '1' level	1	Pin at '0' level
GPnConfigA.GPIO_INV	GPIO_IS[63:32] bit n is set to '1' by													
0	Pin rising edge													
1	Pin falling edge													
GPnConfigA.GPIO_INV	GPIO_IS[63:32] bit n is set to '1' by													
0	Pin at '1' level													
1	Pin at '0' level													

## 10.9.20 GPI\_IS[94:64]—GPI Interrupt Status [94:64] Register

Offset Address:	GPIOBASE +88h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 12:31, Resume for 8:11

Bit	Description												
31	Reserved												
30:0	<p><b>GPI Interrupt Status (GPI_IS[94:64])</b>—R/WC. This bit is set if:</p> <ol style="list-style-type: none"> <li>1. The corresponding GPIO_OWN[94:64] bit n = '1' to indicate GPIO driver ownership</li> <li>2. The corresponding GPnConfigA.GPIO_USE_SEL='1' to indicate GPIO Mode</li> <li>3. An edge or level event is detected</li> </ol> <p>If the corresponding GPnConfigA.GPI_LxEb='0' to indicate Edge Mode:</p> <table border="1"> <tr> <td>GPnConfigA.GPI_INV</td><td>GPI_IS[94:64] bit n is set to '1' by</td></tr> <tr> <td>0</td><td>Pin rising edge</td></tr> <tr> <td>1</td><td>Pin falling edge</td></tr> </table> <p>If the corresponding GPnConfigA.GPI_LxEb='1' to indicate Level Mode:</p> <table border="1"> <tr> <td>GPnConfigA.GPI_INV</td><td>GPI_IS[94:64] bit n is set to '1' by</td></tr> <tr> <td>0</td><td>Pin at '1' level</td></tr> <tr> <td>1</td><td>Pin at '0' level</td></tr> </table> <p><b>Note:</b> The state of GPI_IE[94:64] bit n does not prevent the setting of the corresponding GPI_IS[94:64] bit n. Software writes '1' to clear a bit.</p>	GPnConfigA.GPI_INV	GPI_IS[94:64] bit n is set to '1' by	0	Pin rising edge	1	Pin falling edge	GPnConfigA.GPI_INV	GPI_IS[94:64] bit n is set to '1' by	0	Pin at '1' level	1	Pin at '0' level
GPnConfigA.GPI_INV	GPI_IS[94:64] bit n is set to '1' by												
0	Pin rising edge												
1	Pin falling edge												
GPnConfigA.GPI_INV	GPI_IS[94:64] bit n is set to '1' by												
0	Pin at '1' level												
1	Pin at '0' level												

### 10.9.21 GPI\_IE[31:0]—GPI Interrupt Enable [31:0] Register

Offset Address:	GPIOBASE +90h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	<b>GPI Interrupt Enable (GPI_IE[31:0])</b> —R/W. These bits enable the corresponding GPIOn to generate APIC interrupt. With $\text{GPI\_IE}[31:0]$ bit $n=1$ and $\text{GPI\_IS}[31:0]$ bit $n=1$ , an interrupt is generated. Refer to <code>GPIO_GC.GPIO_IRQ_ROUTE</code> for interrupt routing.

## 10.9.22 **GPI\_IE[63:32]**—GPI Interrupt Enable [63:32] Register

Offset Address:	GPIOBASE +94h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 16:23, Resume for 8:15, 24:31

Bit	Description
31:0	<b>GPI Interrupt Enable (GPI_IE[63:32])</b> —R/W. These bits enable the corresponding GPIOn to generate APIC interrupt. With <b>GPI_IE[63:32]</b> bit n='1' and <b>GPI_IS[63:32]</b> bit n='1', an interrupt is generated. Refer to <b>GPIO_GC.GPIO_IRQ_ROUTE</b> for interrupt routing.

## 10.9.23 **GPI\_IE[94:64]**—GPI Interrupt Enable [94:64] Register

Offset Address:	GPIOBASE +98h	Attribute:	R/W
Default Value:	00000000h	Size:	32 bits
Lockable:	No	Power Well:	Core for 0:7, 12:31, Resume for 8:11

Bit	Description
31	Reserved.
30:0	<b>GPI Interrupt Enable (GPI_IE[94:64])</b> —R/W. These bits enable the corresponding GPIOn to generate APIC interrupt. With <b>GPI_IE[94:64]</b> bit n='1' and <b>GPI_IS[94:64]</b> bit n='1', an interrupt is generated. Refer to <b>GPIO_GC.GPIO_IRQ_ROUTE</b> for interrupt routing.

## 10.9.24 GPnCONFIGA—GPIO Configuration A Register (Where n = GPIO Pin Number)

Offset Address: GPIOBASE +100h + n\*8h Attribute: R/W, RO  
 Default Value: see below Size: 32 bits  
 Lockable: see below  
 Power Well: Register will reside in the same well as the GPIOn, refer to [Table 2.24](#)

Bit	Description
31	<p><b>GPO_LVL</b>—R/W. If GPIO[n] is programmed to be an output (by means of the corresponding bit in the GPIO_IO_SEL register), then the corresponding GPO_LVL bit can be updated by software to drive a high or low value on the output pin.    0 = Low (Default)    1 = High</p> <p><b>Note:</b> When GPIO[n] is configured to be an input, writes to these bits are stored but have no effect to the pin value. This allows output value to be programmed prior to changing the pin direction from input to output.</p> <p><b>Note:</b> When configured in native mode (GPIO_USE_SEL[n] = 0), writes to these bits are stored but have no effect to the pin value during native mode.</p> <p>This bit is lockable by GLE.</p>
30	<p><b>GPI_LVL</b>—RO. If GPIO[n] is programmed as an input in GPIO Mode, then the corresponding GPI_LVL bit reflects the state of the input signal. This is also true during GPIO Mode output.    0 = Low    1 = High</p> <p><b>Note:</b> If GPINDIS bit for GPIO[n] is set to "1", then the value reported is undefined. Writes will have no effect.</p> <p><b>Note:</b> The value reported in this register is undefined when the pin is programmed as native mode.</p> <p><b>Note:</b> Default state will depend on pad value and whether there are on-board pull-up/pull-down on respective GPI.</p>
29:5	Reserved
4	<p><b>GPI_LxEb</b>—R/W. This affects the GPI_IS[n] setting.    0 = Edge Mode (Default)    1 = Level Mode</p> <p>This bit is lockable by GLE.</p>
3	<p><b>GPI_INV</b>—R/W. This bit only has effect if the corresponding GPIO is used as an input and used by the GPE logic or GPI_IS setting, where the polarity matters.    0 = GPI is sent as-is to the GPE logic or GPI_IS[n] that is using it. (Default)    1 = GPI is inverted before it is sent to the GPE logic or GPI_IS[n] that is using it.</p> <p>This is used to allow active-low and active-high inputs to cause IRQ, SMI#, SCI or NMI. This bit has no effect on the value that is reported in the GPI_LVL register.</p> <p>This bit is lockable by GLE.</p>
2	<p><b>GPIO_IO_SEL</b>—R/W. In GPIO Mode (refer to <a href="#">GPIO_USE_SEL</a>):    0 = Corresponding GPIO signal is programmed as an output.    1 = Corresponding GPIO signal is programmed as an input.</p> <p><b>Note:</b> Refer to <a href="#">Table 2.24</a> to determine whether respective GPIO defaults to GPI or GPO.</p> <p>This bit is lockable by GLE.</p>
1	Reserved
0	<p><b>GPIO_USE_SEL</b>—R/W. Enables GPIO[n] to be used as a GPIO rather than for Native function.    0 = Corresponding GPIO signal is used a Native function (also default for un-implemented GPIO).    1 = Corresponding GPIO signal is used as GPIO mode (also default for non-multiplexed GPIO).    Dedicated (non-multiplexed) GPIOs must report 1b in this register bit. Un-implemented GPIOs must report 0b in this register bit. If GPIO versus Native mode is configured by means of soft strap, the corresponding GPIO[n]_USE_SEL bit has no effect.</p> <p><b>Note:</b> For GPIO pins being multiplexed with MGPIO, the Intel® ME GPIO override has the highest priority over GPIO_USE_SEL or soft straps.</p> <p><b>Note:</b> Refer to <a href="#">Table 2.24</a> to determine whether respective GPIO defaults to native or GPIO mode.</p> <p>This bit is lockable by GLE.</p>

### 10.9.25 GPnCONFIGB—GPIO Configuration B Register (Where n = GPIO Pin Number)

Offset Address: GPIOBASE +104h + n\*8h Attribute: R/W, RO  
 Default Value: see below Size: 32 bits  
 Lockable: see below  
 Power Well: Register will reside in the same well as the GPIOn, refer to [Table 2.24](#)

Bit	Description
31:3	Reserved
2	<b>GPINDIS</b> —R/W In GPIO Mode (refer to GPIO_USE_SEL), this bit allows the input circuitry to be disabled. 0 = Input sensing enable. (Default) 1 = Input sensing disable. Depending on buffer type, the signal may reflect steady state level 0 or 1 once input sensing is disabled. Software is recommended to disable input sensing if a GPIO mode pin is used for output-only usage (that is, set as GPO). This field has no effect on the input sensing control beyond GPIO mode. This bit is lockable by GLE.
1:0	<b>GPIWP</b> —R/W In GPIO Mode (refer to GPIO_USE_SEL), this bit allows the weak internal pull to be activated. 00 = none 01 = pull-down 10 = pull-up 11 = invalid This field has no effect on the pin state beyond GPIO mode. <b>Note:</b> Refer to <a href="#">Table 2.24</a> for default state of respective GPIO/native mode and whether there are weak internal pull-up or pull-down. This bit is lockable by GLE.

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# 11 SATA Controller Registers (D31:F2)

## 11.1 PCI Configuration Registers (SATA-D31:F2)

**Note:**

Address locations that are not shown should be treated as Reserved.

All of the SATA registers are in the core well. None of the registers can be locked.

**Table 11-1. PCI Configuration Registers (SATA-D31:F2) Address Map (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	8086h	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	02B0h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	See register description	See register description
0Ah	SCC	Sub Class Code	See register description	See register description
0Bh	BCC	Base Class Code	01h	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
10h-13h	—	Reserved	00000000h	R/W, RO
14h-17h	—	Reserved	00000000h	R/W, RO
18h-1Bh	—	Reserved	00000000h	R/W, RO
1Ch-1Fh	—	Reserved	00000000h	R/W, RO
20h-23h	—	Reserved	00000000h	R/W, RO
24h-27h	ABAR	AHCI Base Address	00000000h	R/W, RO
2Ch-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAP	Capabilities Pointer	80h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
40h-41h	—	Reserved	0000h	R/W
42h-43h	—	Reserved	0000h	R/W
44h	—	Reserved	00h	R/W
48h	—	Reserved	00h	R/W
4Ah-4Bh	—	Reserved	0000h	R/W
54h-57h	—	Reserved	00000000h	R/W

**Table 11-1. PCI Configuration Registers (SATA-D31:F2) Address Map (Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
70h-71h	PID	PCI Power Management Capability ID	See register description	RO
72h-73h	PC	PCI Power Management Capabilities	See register description	RO
74h-75h	PMCS	PCI Power Management Control and Status	See register description	R/W, RO, R/WC
80h-81h	MSICI	Message Signaled Interrupt Capability ID	7005h	R/W, RO
82h-83h	MSIMC	Message Signaled Interrupt Message Control	0000h	RO, R/W
84h-87h	MSIMA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
88h-89h	MSIMD	Message Signaled Interrupt Message Data	0000h	R/W
90h	MAP	Address Map	0000h	R/W, R/WO, RO
92h-93h	PCS	Port Control and Status	0000h	R/W, RO
94h-97h	SCLKGC	SATA Clock Gating Control	00000000h	R/W, RO
98h-9Bh	SCLKGC2	SATA Clock Gating Control 2	00000000h	R/W, RO
9Ch-9Fh	SGC	SATA General Configuration	00000000h	R/W, R/WO, RO
A8h-ABh	SATACR0	SATA Capability Register 0	00100012h	RO, R/WO
ACh-AFh	SATACR1	SATA Capability Register 1	00000048h	RO
B0h-B1h	FLRCID	FLR Capability ID	0009h	RO
B2h-B3h	FLRCLV	FLR Capability Length and Version	See register description	R/WO, RO
B4h-B5h	FLRC	FLR Control	0000h	RO, R/W
C0h	—	Reserved	00h	R/W
C4h	—	Reserved	00h	R/WC
D0h-D3h	SP	Scratch Pad	00000000h	R/W
E0h-E3h	BFCS	BIST FIS Control/Status	00000000h	R/W, R/WC
E4h-E7h	BFTD1	BIST FIS Transmit Data, DW1	00000000h	R/W
E8h-EBh	BFTD2	BIST FIS Transmit Data, DW2	00000000h	R/W

**Note:** The PCH SATA controller is not arbitrated as a PCI device; therefore, it does not need a master latency timer.



### 11.1.1 VID—Vendor Identification Register (SATA—D31:F2)

Offset Address: 00h–01h Attribute: RO  
 Default Value: 8086h Size: 16 bit  
 Lockable: No Power Well: Core

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

### 11.1.2 DID—Device Identification Register (SATA—D31:F2)

Offset Address: 02h–03h Attribute: RO  
 Default Value: See bit description Size: 16 bits  
 Lockable: No Power Well: Core

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH SATA controller. <b>Note:</b> The value of this field will change dependent upon the value of the MAP Register. See <a href="#">Section 11.1.24</a>

### 11.1.3 PCICMD—PCI Command Register (SATA—D31:F2)

Address Offset: 04h–05h Attribute: RO, R/W  
 Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable</b> —R/W. This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt and MSI is not enabled. 1 = Internal INTx# messages will not be generated.
9	1 = Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = SERR# messages will not be generated. 1 = SERR# messages are generated if bit 8 of the PCISTS register is set or bit 8 of the SGC register is set.
7	Wait Cycle Control (WCC)—RO. Hardwired to 0.
6	<b>Parity Error Response (PER)</b> —R/W 0 = Disabled. SATA controller will not generate PERR# when a data parity error is detected. 1 = Enabled. SATA controller will generate PERR# when a data parity error is detected.
5	VGA Palette Snoop (VPS)—RO. Hardwired to 0.
4	Postable Memory Write Enable (PMWE)—RO. Hardwired to 0.
3	Special Cycle Enable (SCE)—RO. Hardwired to 0.
2	<b>Bus Master Enable (BME)</b> —R/W. This bit controls the SATA controller's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	<b>Memory Space Enable (MSE)</b> —R/W/RO. Controls access to the SATA controller's target memory space (for AHCI). This bit is RO 0 when not in AHCI/RAID modes.
0	<b>I/O Space Enable (IOSE)</b> —R/W. This bit controls access to the I/O space registers. 0 = Disables access to the Legacy or Native IDE ports (both Primary and Secondary) as well as the Bus Master I/O registers. 1 = Enable. The Base Address register for the Bus Master registers should be programmed before this bit is set.

### 11.1.4 PCISTS—PCI Status Register (SATA—D31:F2)

Address Offset: 06h–07h  
Default Value: 02B0h

Attribute: R/WC, RO  
Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC 0 = No parity error detected by SATA controller. 1 = SATA controller detects a parity error on its interface.
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No SERR# detected by SATA controller. 1 = SATA controller detects a SERR# on its interface.
13	<b>Received Master Abort (RMA)</b> —R/WC 0 = Master abort not generated. 1 = SATA controller received a master abort.
12	<b>Received Target Abort (TMA)</b> —R/WC 0 = Target abort not generated. 1 = SATA controller received a target abort.
11	<b>Signaled Target Abort (STA)</b> —R/WC. This bit must be set by a target device whenever it terminates a transaction with Target Abort. Devices that will never signal a Target.
10:9	DEVSEL# Timing Status (DEV_STS)—RO 01 = Hardwired; Controls the device select time for the SATA controller's PCI interface.
8	<b>Data Parity Error Detected (DPED)</b> —R/WC. For PCH, this bit can only be set on read completions received from the bus when there is a parity error. 0 = No data parity error received. 1 = SATA controller, as a master, either detects a parity error or sees the parity error line asserted, and the parity error response bit—bit 6 of the command register is set.
7	Fast Back to Back Capable (FB2BC)—RO. Hardwired to 1.
6	Reserved
5	66 MHz Capable (66MHZ_CAP)—RO. Hardwired to 1.
4	<b>Capabilities List (CAP_LIST)</b> —RO. This bit indicates the presence of a capabilities list. The minimum requirement for the capabilities list must be PCI power management for the SATA controller.
3	<b>Interrupt Status (INTS)</b> —RO. Reflects the state of INTx# messages, IRQ14 or IRQ15. 0 = Interrupt is cleared (independent of the state of Interrupt Disable bit in the command register [offset 04h]). 1 = Interrupt is to be asserted
2:0	Reserved

### 11.1.5 RID—Revision Identification Register (SATA—D31:F2)

Offset Address: 08h  
Default Value: See bit description

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See Section 1.4 for the value of the RID Register.

## 11.1.6 PI—Programming Interface Register (SATA—D31:F2)

### 11.1.6.1 When Sub Class Code Register (D31:F2:Offset 0Ah) = 01h

Address Offset: 09h Attribute: R/W, RO  
 Default Value: 8Ah Size: 8 bits

Bit	Description
7	This read-only bit is a 1 to indicate that the PCH supports bus master operation
6:4	Reserved. Will always return 0.
3	<b>Secondary Mode Native Capable (SNC)</b> —RO. Hardwired to '1' to indicate secondary controller supports both legacy and native modes.
2	<b>Secondary Mode Native Enable (SNE)</b> —R/W. Determines the mode that the secondary channel is operating in. 0 = Secondary controller operating in legacy (compatibility) mode 1 = Secondary controller operating in native PCI mode. If this bit is set by software, then the PNE bit—bit 0 of this register must also be set by software. While in theory these bits can be programmed separately, such a configuration is not supported by hardware.
1	<b>Primary Mode Native Capable (PNC)</b> —RO. Hardwired to '1' to indicate primary controller supports both legacy and native modes.
0	<b>Primary Mode Native Enable (PNE)</b> —R/W. Determines the mode that the primary channel is operating in. 0 = Primary controller operating in legacy (compatibility) mode. 1 = Primary controller operating in native PCI mode. If this bit is set by software, then the SNE bit—bit 2 of this register must also be set by software simultaneously.

### 11.1.6.2 When Sub Class Code Register (D31:F2:Offset 0Ah) = 04h

Address Offset: 09h Attribute: RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Interface (IF)</b> —RO. When configured as RAID, this register becomes read only 0.

### 11.1.6.3 When Sub Class Code Register (D31:F2:Offset 0Ah) = 06h

Address Offset: 09h Attribute: RO  
 Default Value: 01h Size: 8 bits

Bit	Description
7:0	<b>Interface (IF)</b> —RO. Indicates that the SATA Controller is an AHCI HBA that has a major revision of 1.

### 11.1.7 SCC—Sub Class Code Register (SATA-D31:F2)

Address Offset: 0Ah Attribute: RO  
Default Value: See bit description Size: 8 bits

Bit	Description									
7:0	<p><b>Sub Class Code (SCC)</b>  This field specifies the sub-class code of the controller, per the table below:</p> <table> <thead> <tr> <th>MAP.SMS (D31:F2:Offset 90h:bit 7:6) Value</th> <th>SCC Register Value</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>01h (Test Mode)</td> </tr> <tr> <td>01b</td> <td>06h (AHCI Controller)</td> </tr> <tr> <td>10b</td> <td>04h (RAID Controller)</td> </tr> </tbody> </table> <p><b>Note:</b> Not all SCC values may be available for a given SKU. See <a href="#">Section 2.3</a> for details on storage controller capabilities.</p>	MAP.SMS (D31:F2:Offset 90h:bit 7:6) Value	SCC Register Value	00b	01h (Test Mode)	01b	06h (AHCI Controller)	10b	04h (RAID Controller)	
MAP.SMS (D31:F2:Offset 90h:bit 7:6) Value	SCC Register Value									
00b	01h (Test Mode)									
01b	06h (AHCI Controller)									
10b	04h (RAID Controller)									

### 11.1.8 BCC—Base Class Code Register (SATA-D31:F2|SATA-D31:F2)

Address Offset: 0Bh Attribute: RO  
Default Value: 01h Size: 8 bits

Bit	Description
7:0	<b>Base Class Code (BCC)</b> —RO 01h = Mass storage device

### 11.1.9 PMLT—Primary Master Latency Timer Register (SATA-D31:F2)

Address Offset: 0Dh Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Master Latency Timer Count (MLTC)</b> —RO 00h = Hardwired. The SATA controller is implemented internally, and is not arbitrated as a PCI device, so it does not need a Master Latency Timer.

### 11.1.10 HTYPE—Header Type Register (SATA-D31:F2)

Address Offset: 0Eh      Attribute: RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7	<b>Multi-function Device (MFD)</b> —RO. Indicates this SATA controller is not part of a multifunction device.
6:0	<b>Header Layout (HL)</b> —RO. Indicates that the SATA controller uses a target device layout.

### 11.1.11 ABAR—AHCI Base Address Register (SATA-D31:F2)

The register represents a memory BAR allocating space for the AHCI memory registers defined in [Section 11.4](#).

Address Offset: 24–27h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:11	<b>Base Address (BA)</b> —R/W. Base address of register memory space (aligned to 2KB)
10:4	Reserved
3	<b>Prefetchable (PF)</b> —RO. Indicates that this range is not prefetchable
2:1	<b>Type (TP)</b> —RO. Indicates that this range can be mapped anywhere in 32-bit address space.
0	<b>Resource Type Indicator (RTE)</b> —RO. Hardwired to 0 to indicate a request for register memory space.

**Note:**

1. The ABAR register must be set to a value of 0001\_0000h or greater.

### 11.1.12 SVID—Subsystem Vendor Identification Register (SATA-D31:F2)

Address Offset: 2Ch–2Dh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits  
 Lockable: No      Power Well: Core  
 Function Level Reset: No

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —R/WO. Value is written by BIOS. No hardware action taken on this value.

### 11.1.13 SID—Subsystem Identification Register (SATA-D31:F2)

Address Offset:	2Eh–2Fh	Attribute:	R/WO
Default Value:	0000h	Size:	16 bits
Lockable:	No	Power Well:	Core
Function Level Reset:	No		

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —R/WO. Value is written by BIOS. No hardware action taken on this value.

### 11.1.14 CAP—Capabilities Pointer Register (SATA-D31:F2)

Address Offset:	34h	Attribute:	RO
Default Value:	80h	Size:	8 bits

Bit	Description
7:0	<b>Capabilities Pointer (CAP_PTR)</b> —RO. Indicates that the first capability pointer offset is 80h. This value changes to 70h if the Sub Class Code (SCC) (Dev 31:F2:0Ah) is configured as IDE mode (value of 01).

### 11.1.15 INT\_LN—Interrupt Line Register (SATA-D31:F2)

Address Offset:	3Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bits
Function Level Reset:	No		

Bit	Description
7:0	<b>Interrupt Line</b> —R/W. This field is used to communicate to software the interrupt line that the interrupt pin is connected. Interrupt Line register is not reset by FLR.

### 11.1.16 INT\_PN—Interrupt Pin Register (SATA-D31:F2)

Address Offset:	3Dh	Attribute:	RO
Default Value:	See Register Description	Size:	8 bits

Bit	Description
7:0	<b>Interrupt Pin</b> —RO. This reflects the value of D31IP.SIP (Chipset Configuration Registers:Offset 3100h:bits 11:8).

### 11.1.17 PID—PCI Power Management Capability Identification Register (SATA—D31:F2)

Address Offset: 70h–71h      Attribute: RO  
 Default Value: See Register Description      Size: 16 bits

Bits	Description
15:8	<b>Next Capability (NEXT)</b> —R/W A8h is the location of the Serial ATA capability structure. A8h is the recommended setting for non-IDE mode. If the controller is to operate in IDE mode, BIOS is requested to program this field to 00h. <b>Note:</b> Refer to the SGC.REGLOCK description in order to lock the register to become RO. This bit is not reset by Function Level Reset.
7:0	<b>Capability ID (CID)</b> —RO. Hardwired to 01h. Indicates that this pointer is a PCI power management.

### 11.1.18 PC—PCI Power Management Capabilities Register (SATA—D31:F2)

Address Offset: 72h–73h      Attribute: RO  
 Default Value: See Register Description      Size: 16 bits

Bits	Description
15:11	<b>PME Support (PME_SUP)</b> —RO. 00000 = If SCC = 01h, indicates no PME support in IDE mode. 01000 = If SCC is not 01h, in a non-IDE mode, indicates PME# can be generated from the D3 <sub>HOT</sub> state in the SATA host controller.
10	<b>D2 Support (D2_SUP)</b> —RO. Hardwired to 0. The D2 state is not supported
9	<b>D1 Support (D1_SUP)</b> —RO. Hardwired to 0. The D1 state is not supported
8:6	<b>Auxiliary Current (AUX_CUR)</b> —RO. PME# from D3 <sub>COLD</sub> state is not supported; therefore, this field is 000b.
5	<b>Device Specific Initialization (DSI)</b> —RO. Hardwired to 0 to indicate that no device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PME_CLK)</b> —RO. Hardwired to 0 to indicate that 24-MHz clock is not required to generate PME#.
2:0	<b>Version (VER)</b> —RO. Hardwired to 011 to indicates support for Revision 1.2 of the PCI Power Management Specification.

### 11.1.19 PMCS—PCI Power Management Control and Status Register (SATA—D31:F2)

Address Offset: 74h–75h      Attribute: R/W, R/WC, RO  
 Default Value: 0008h      Size: 16 bits  
 Function Level Reset: No (Bits 8 and 15)

Bits	Description
15	<b>PME Status (PMES)</b> —R/WC. Bit is set when a PME event is to be requested, and if this bit and PMEE is set, a PME# will be generated from the SATA controller <b>Note:</b> Whenever SCC = 01h, hardware will automatically change the attribute of this bit to RO 0. Software is advised to clear PMEE and PMES together prior to changing SCC thru MAP.SMS. This bit is not reset by Function Level Reset.

Bits	Description
14:9	Reserved
8	<p><b>PME Enable (PMEE)</b>—R/W. When set, the SATA controller asserts PME# when exiting D3<sub>HOT</sub> on a wake event.</p> <p><b>Note:</b> Whenever SCCSCC = 01h, hardware will automatically change the attribute of this bit to RO 0. Software is advised to clear PMEE and PMES together prior to changing SCC through MAP.SMS.</p> <p>This bit is not reset by Function Level Reset.</p>
7:4	Reserved
3	<p><b>No Soft Reset (NSFRST)</b>—RO. These bits are used to indicate whether devices transitioning from D3<sub>HOT</sub> state to D0 state will perform an internal reset.</p> <p>0 = Device transitioning from D3<sub>HOT</sub> state to D0 state perform an internal reset.</p> <p>1 = Device transitioning from D3<sub>HOT</sub> state to D0 state do not perform an internal reset.</p> <p>Configuration content is preserved. Upon transition from the D3<sub>HOT</sub> state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits.</p> <p>Regardless of this bit, the controller transition from D3<sub>HOT</sub> state to D0 state by a system or bus segment reset will return to the state D0 uninitialized with only PME context preserved if PME is supported and enabled.</p>
2	Reserved
1:0	<p><b>Power State (PS)</b>—R/W. These bits are used both to determine the current power state of the SATA controller and to set a new power state.</p> <p>00 = D0 state</p> <p>11 = D3<sub>HOT</sub> state</p> <p>When in the D3<sub>HOT</sub> state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked.</p>

### 11.1.20 MSICI—Message Signaled Interrupt Capability Identification Register (SATA—D31:F2)

Address Offset: 80h–81h  
Default Value: 7005h

Attribute: R/W, RO  
Size: 16 bits

**Note:** There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
15:8	<p><b>Next Pointer (NEXT)</b>—R/W. Indicates the next item in the list is the PCI power management pointer.</p> <p>BIOS may program this field to A8h indicating that the next item is Serial ATA Capability Structure.</p> <p><b>Note:</b> Refer the SGC.REGLOCK description in order to lock the register to become RO.</p> <p>This bit is not reset by a Function Level Reset</p>
7:0	<b>Capability ID (CID)</b> —RO. Capabilities ID indicates MSI.

### 11.1.21 MSIMC—Message Signaled Interrupt Message Control Register (SATA—D31:F2)

Address Offset: 82h–83h Attribute: R/W, RO  
Default Value: 0000h Size: 16 bits

**Note:** There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description																							
15:8	Reserved																							
7	<b>64-bit Address Capable (C64)</b> —RO. Capable of generating a 32-bit message only.																							
6:4	<b>Multiple Message Enable (MME)</b> —RO. = 000 (and MSIE is set), a single MSI message will be generated for all SATA ports, and bits [15:0] of the message vector will be driven from MD[15:0]. For 6 port components:																							
	<table border="1"> <thead> <tr> <th>MME</th><th colspan="4">Value Driven on Message Signal Interrupt Memory Write</th></tr> <tr> <th></th><th>Bits[15:3]</th><th>Bit[2]</th><th>Bit[1]</th><th>Bit[0]</th></tr> </thead> <tbody> <tr> <td>000, 001, 010</td><td>MD[15:3]</td><td>MD[2]</td><td>MD[1]</td><td>MD[0]</td></tr> <tr> <td>011</td><td>MD[15:3]</td><td>Port 0: 0 Port 1: 0 Port 2: 0 Port 3: 0 Port 4: 1 Port 5: 1</td><td>Port 0: 0 Port 1: 0 Port 2: 1 Port 3: 1 Port 4: 0 Port 5: 0</td><td>Port 0: 0 Port 1: 1 Port 2: 0 Port 3: 1 Port 4: 0 Port 5: 1</td></tr> </tbody> </table>				MME	Value Driven on Message Signal Interrupt Memory Write					Bits[15:3]	Bit[2]	Bit[1]	Bit[0]	000, 001, 010	MD[15:3]	MD[2]	MD[1]	MD[0]	011	MD[15:3]	Port 0: 0 Port 1: 0 Port 2: 0 Port 3: 0 Port 4: 1 Port 5: 1	Port 0: 0 Port 1: 0 Port 2: 1 Port 3: 1 Port 4: 0 Port 5: 0	Port 0: 0 Port 1: 1 Port 2: 0 Port 3: 1 Port 4: 0 Port 5: 1
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	All other MME values are reserved. If this field is set to one of these reserved values, the results are undefined.																							
	<b>Note:</b> The CCC interrupt is generated on unimplemented port (AHCI PI register bit equal to 0). If CCC interrupt is disabled, no MSI shall be generated for the port dedicated to the CCC interrupt. When CCC interrupt occurs, MD[2:0] is dependant on CCC_CTL.INT (in addition to MME).																							
3:1	<b>Multiple Message Capable (MMC)</b> —RO. MMC is not supported.																							
0	<b>MSI Enable (MSIE)</b> —R/W, RO. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. This bit is R/W when SC.SCC is not 01h and is read-only 0 when SCC is 01h. The CMD.ID bit has no effect on MSI.																							
	<b>Note:</b> Software must clear this bit to 0 to disable MSI first before changing the number of messages allocated in the MMC field. Software must also make sure this bit is cleared to '0' when operating in legacy mode (when GHC.AE = 0).																							

### 11.1.22 MSIMA—Message Signaled Interrupt Message Address Register (SATA—D31:F2)

Address Offset: 84h–87h      Attribute: R/W, RO  
Default Value: 00000000h      Size: 32 bits

**Note:** There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
31:2	<b>Address (ADDR)</b> —R/W. Lower 32 bits of the system specified message address, always DWord aligned.
1:0	Reserved

### 11.1.23 MSIMD—Message Signaled Interrupt Message Data Register (SATA—D31:F2)

Address Offset: 88h–89h      Attribute: R/W  
Default Value: 0000h      Size: 16 bits

**Note:** There is no support for MSI when the software is operating in legacy (IDE) mode when AHCI is not enabled. Prior to switching from AHCI to IDE mode, software **must** make sure that MSI is disabled.

Bits	Description
15:0	<b>Data (DATA)</b> —R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word of the data bus of the MSI memory write transaction. When the MME field is set to '001' or '010', bit [0] and bits [1:0] respectively of the MSI memory write transaction will be driven based on the source of the interrupt rather than from MD[2:0]. See the description of the MME field.

### 11.1.24 MAP—Address Map Register (SATA—D31:F2)

Address Offset: 90h      Attribute: R/W, R/WO, RO  
Default Value: 0000h      Size: 16 bits  
Function Level Reset: No (Bits 7:5 and 13:8 only)

Bits	Description
15:8	Reserved
7:6	<b>SATA Mode Select (SMS)</b> —R/W. Software programs these bits to control the mode in which the SATA Controller should operate: 00b = SATA Test Mode 01b = AHCI mode 10b = RAID mode 11b = Reserved  <b>Notes:</b> 1. The SATA Function Device ID will change based on the value of this register. 2. Software shall not manipulate SMS during runtime operation; that is, the operating system will not do this. The BIOS may choose to switch from one mode to another during POST. These bits are not reset by Function Level Reset.
5	<b>SATA Port-to-Controller Configuration (SC)</b> —RO. Up to 4 SATA ports are supported. This bit is not reset by Function Level Reset.
4:0	Reserved



### 11.1.25 PCS—Port Control and Status Register (SATA—D31:F2)

Address Offset:	92h–93h	Attribute:	R/W, RO
Default Value:	0000h	Size:	16 bits
Function Level Reset:	No		

By default, the SATA ports are set to the disabled state (bits [3:0] = 0). When enabled by software, the ports can transition between the on, partial, and slumber states and can detect devices. When disabled, the port is in the “off” state and cannot detect any devices.

If an AHCI aware or RAID enabled operating system is being booted, then system BIOS shall insure that all supported SATA ports are enabled prior to passing control to the operating system. Once the AHCI is aware the operating system is booted, it becomes the enabling/disabling policy owner for the individual SATA ports. This is accomplished by manipulating a port’s PxSCTL and PxCMD fields. Because an AHCI or RAID is aware the operating system will typically not have knowledge of the PxE bits and because the PxE bits act as master on/off switches for the ports, pre-boot software must insure that these bits are set to 1—prior to booting the operating system, regardless as to whether or not a device is currently on the port.

Bits	Description
15	<b>OOB Retry Mode (ORM)</b> —R/W 0 = The SATA controller will not retry after an OOB failure 1 = The SATA controller will continue to retry after an OOB failure until successful (infinite retry)
14:12	Reserved
11	<b>Port 3Present (P3P)</b> —RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P3E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 3 has been detected.
10	<b>Port 2 Present (P2P)</b> —RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P2E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 2 has been detected.
9	<b>Port 1 Present (P1P)</b> —RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P1E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 1 has been detected.
8	<b>Port 0 Present (POP)</b> —RO. The status of this bit may change at any time. This bit is cleared when the port is disabled using P0E. This bit is not cleared upon surprise removal of a device. 0 = No device detected. 1 = The presence of a device on Port 0 has been detected.
7:4	Reserved
3	<b>Port 3Enabled (P3E)</b> —R/W/RO 0 = Disabled. The port is in the ‘off’ state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. <b>Notes:</b> 1. This bit takes precedence over P3CMD.SUD (offset ABAR+298h:bit 1). When MAP.SPD[3] is 1 this is reserved and is read-only 0.
2	<b>Port 2 Enabled (P2E)</b> —R/W/RO 0 = Disabled. The port is in the ‘off’ state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. <b>Notes:</b> This bit takes precedence over P2CMD.SUD (offset ABAR+218h:bit 1). When MAP.SPD[2] is 1, this is reserved and is read-only 0.

Bits	Description
1	<b>Port 1 Enabled (P1E)</b> —R/W/RO 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. <b>Note:</b> This bit takes precedence over P1CMD.SUD (offset ABAR+198h:bit 1). When MAP.SPD[1] is 1 this is reserved and is read-only 0.
0	<b>Port 0 Enabled (POE)</b> —R/W/RO 0 = Disabled. The port is in the 'off' state and cannot detect any devices. 1 = Enabled. The port can transition between the on, partial, and slumber states and can detect devices. <b>Note:</b> This bit takes precedence over P0CMD.SUD (offset ABAR+118h:bit 1). When MAP.SPD[0] is 1, this is reserved and is read-only 0.

### 11.1.26 SCLKGC—SATA Clock Gating Control Register

Address Offset: 94h–97h      Attribute: R/W, RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:28	Reserved
27:24	<b>Port Clock Disable (PCD)</b> —R/W 0 = All clocks to the associated port logic will operate normally. 1 = The backbone clock driven to the associated port logic is gated and will not toggle. Bit 27: Port 3 Bit 26: Port 2 Bit 25: Port 1 Bit 24: Port 0 If a port is not available, software shall set the corresponding bit to 1. Software can also set the corresponding bits to 1 on ports that are disabled. Software cannot set the PCD [port x]=1 if the corresponding PCS.PxE=1 in either Dev31Func2 or AHCI GHC.PI[x] = "1".
23:16	Reserved
15	<b>Port 0 or Port 3 DEVSLP Multiplex (POP3_DEVSLP)</b> —R/W 0 = SATA port 0 DEVSLP being driven externally out on DEVSLP0/GPIO33 pin when in native mode. 1 = SATA port 3 DEVSLP being driven externally out on DEVSLP0/GPIO33 pin when in native mode.
14:	Reserved

### 11.1.27 SCLKGC2—SATA Clock Gating Control 2 Register

Address Offset: 98h–9Bh  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:25	Reserved
24	<p><b>SATA MPHY Dynamic Power Gating Enable (PHYDPGE)</b>—R/W 0 = SATA host controller does not perform dynamic MPHY power gating flow. 1 = SATA host controller supports MPHY dynamic power gating flow.</p> <p>For platforms with only internal SSDs or HDDs, set PHYPDGE=1 to enable SATA MPHY dynamic power gating flow. Use the default value PHYPDGE=0 if the platform has one or more of the following:</p> <ul style="list-style-type: none"> <li>• SATA hot-plug enabled port (PxCMD.HPCP=1)</li> <li>• SATA external port (PxCMD.ESP=1)</li> <li>• SATA slimline port with zero-power ODD (ZPODD) attached (or other AN capable ODD)</li> </ul> <p><b>Note:</b> BIOS is requested to program this field to '1' if the system supports MPHY dynamic power gating and none of the SATA ports require Listen Mode usage.</p> <p><b>Note:</b> BIOS is recommended to program this field to '1' after programming the PCS configuration register.</p>
23:0	Reserved

### 11.1.28 SGC—SATA General Configuration Register

Address Offset: 9Ch–9Fh Attribute: R/W, R/WO, RO  
Default Value: 00000000h Size: 32 bits  
Function Level Reset: No

Bit	Description
31	<b>Register Lock (REGLOCK)</b> —R/WO 0 = Will not lock CAP.CAP_PTR, PID.NEXT, MSICI.NEXT, or SATACR0.NEXT 1 = Setting this bit will lock CAP.CAP_PTR, PID.NEXT, MSICI.NEXT, and SATACR0.NEXT. Once locked, these register bits will become RO. BIOS is requested to program this field prior to IOS handoff. This bit is not reset by a Function Level Reset.
30:15	Reserved
14:12	<b>Maximum Payload Size (MPS)</b> —R/W. These bits select the maximum write request size that the SATA host controller will initiate for DMA write to memory. The SATA host controller will internally break up larger write requests based on these bits. 000b = 128 address aligned bytes maximum payload size 111b = 64 address aligned bytes maximum payload size. This bit is not reset by a Function Level Reset.
11:10	Reserved
9	<b>Unsupported Request Reporting Enable (URRE)</b> —R/WC. If set to 1 by software, it allows reporting of an Unsupported Request as a system error.
8	Unsupported Request Detected (URD)—R/W. This bit is set to 1 by hardware when an Unsupported request is detected.
7 (Non-RAID Capable SKUs Only)	Reserved
7 (RAID Capable SKUs Only)	<b>Alternate ID Enable (AIE)</b> —R/WO. 0 = Clearing this bit when in RAID mode, the SATA Controller located at Device 31: Function 2 will report its Device ID as 282Ah for all Mobile SKUs of the PCH. Clearing this bit is required for the Intel® Rapid Storage Technology driver (including the Microsoft* Windows* Vista operating system and later in-box version of the driver) to load on the platform. Intel® Smart Response Technology also requires that the bit be cleared in order to be enabled on the platform. 1 = Setting this bit when in RAID mode, the SATA Controller located at Device 31: Function 2 will report its Device ID as 9C07h for all Mobile SKUs of the Chipset. This setting will prevent the Intel® Rapid Storage Technology driver (including the Microsoft* Windows* operating system in-box version of the driver) from loading on the platform. During the Microsoft* Windows* OS installation, the user will be required to "load" (formerly done by pressing the F6 button on the keyboard) the appropriate RAID storage driver that is enabled by this setting. This field is reset by PLTRST#. BIOS is required to reprogram the value of this bit after resuming from S3, S4 and S5.
6	<b>Alternate ID Select (AIES)</b> —R/WO. BIOS must write to this bit field.
5	Reserved—BIOS may write to this field.
4:1	Reserved
0	<b>SATA 4-port All Master Configuration Indicator (SATA4PMIND)</b> —RO. 0 = Normal configuration. 1 = Reserved <b>Note:</b> BIOS must also make sure that corresponding port clocks are gated (using SCLKCG configuration register).

### 11.1.29 SATACR0—SATA Capability Register 0 (SATA-D31:F2)

Address Offset: A8h–ABh Attribute: RO, R/WO  
 Default Value: 00100012h Size: 32 bits  
 Function Level Reset: No (Bits 15:8 only)

**Note:** This register is read-only 0 when SCC is 01h.

Bit	Description
31:24	Reserved
23:20	<b>Major Revision (MAJREV)</b> —RO. Major revision number of the SATA Capability Pointer implemented.
19:16	<b>Minor Revision (MINREV)</b> —RO. Minor revision number of the SATA Capability Pointer implemented.
15:8	<b>Next Capability Pointer (NEXT)</b> —R/W. The value 00h indicates the final item in the SATA Capability List. <b>Note:</b> Refer to the SGC.REGLOCK description in order to lock the register to become RO.
7:0	<b>Capability ID (CAP)</b> —R/W. The Value of 12h has been assigned by the PCI SIG to designate the SATA Capability pointer.

### 11.1.30 SATACR1—SATA Capability Register 1 (SATA-D31:F2)

Address Offset: ACh–AFh Attribute: RO  
 Default Value: 00000048h Size: 32 bits

**Note:** This register is read-only 0 when SCC is 01h.

Bit	Description
31:16	Reserved
15:4	<b>BAR Offset (BAROFST)</b> —RO. Indicates the offset into the BAR where the Index/Data pair are located (in DWord granularity). The Index and Data I/O registers are located at offset 10h within the I/O space defined by LBAR. A value of 004h indicates offset 10h. 000h = 0h offset 001h = 4h offset 002h = 8h offset 003h = Bh offset 004h = 10h offset ... FFFh = 3FFFh offset (maximum 16KB)
3:0	<b>BAR Location (BARLOC)</b> —RO. Indicates the absolute PCI Configuration register address of the BAR containing the Index/Data pair (in DWord granularity). The Index and Data I/O registers reside within the space defined by LBAR in the SATA controller. A value of 8h indicates offset 20h, which is LBAR. 0000 – 0011b = reserved 0100b = 10h => BAR0 0101b = 14h => BAR1 0110b = 18h => BAR2 0111b = 1Ch => BAR3 1000b = 20h => LBAR 1001b = 24h => BAR5 1010-1110b = reserved 1111b = Index/Data pair in PCI Configuration space. This is not supported in the PCH.

### 11.1.31 FLRCID—FLR Capability ID Register (SATA-D31:F2)

Address Offset: B0–B1h  
Default Value: 0009h

Attribute: RO  
Size: 16 bits

Bit	Description	
15:8	<b>Next Capability Pointer</b> —RO. 00h indicates the final item in the capability list.	
7:0	<b>Capability ID</b> —RO. The value of this field depends on the FLRCSEL (RCBA+3410h:bit 12) bit.	
	<b>FLRCSEL (RCBA+3410h:bit 12) Value</b>	<b>Capability ID Register Value</b>
	0b	13h
	1b	00h (Vendor Specific)

### 11.1.32 FLRCLV—FLR Capability Length and Version Register (SATA-D31:F2)

Address Offset: B2–B3h  
Default Value: xx06h  
Function Level Reset: No (Bit 9:8 Only when FLRCSEL = 0)

When FLRCSEL (RCBA+3410h:bit 12) = 1, this register is RO.

Bit	Description
15:10	Reserved
9	<b>FLR Capability</b> —R/W 1 = Support for Function Level reset. This bit is not reset by the Function Level Reset.
8	<b>TXP Capability</b> —R/W 1 = Support for Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	<b>Vendor-Specific Capability ID</b> —RO. This field indicates the number of bytes of this Vendor Specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.

### 11.1.33 FLRC—FLR Control Register (SATA-D31:F2)

Address Offset: B4–B5h  
Default Value: 0000h

Attribute: RO, R/W  
Size: 16 bits

When FLRCSEL (RCBA+3410h:bit 12) = 1, this register is RO.

Bit	Description
15:9	Reserved
8	<b>Transactions Pending (TXP)</b> —RO 0 = Controller has received all non-posted requests. 1 = Controller has issued non-posted requests which has not been completed.
7:1	Reserved
0	<b>Initiate FLR</b> —R/W. Used to initiate FLR transition. A write of 1 indicates FLR transition. Since hardware must not respond to any cycles till FLR completion the value read by software from this bit is 0.



### 11.1.34 SP Scratch Pad Register (SATA-D31:F2)

Address Offset: D0h Attribute: R/W  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Data (DT)</b> —R/W. This is a read/write register that is available for software to use. No hardware action is taken on this register.

### 11.1.35 BFCS—BIST FIS Control/Status Register (SATA-D31:F2)

Address Offset: E0h–E3h Attribute: R/W, R/WC, RO  
Default Value: 00000000h Size: 32 bits

Bits	Description
31:13	Reserved
12	<b>Port 2 BIST FIS Initiate (P2BFI)</b> —R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 2, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 2 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P2BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully. <b>Note:</b> Bit may be Reserved depending on if port is available in the given SKU. See <a href="#">Section 2.3</a> for details if port is available.
11	<b>BIST FIS Successful (BFS)</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_OK completion status from the device. <b>Note:</b> This bit must be cleared by software prior to initiating a BIST FIS.
10	<b>BIST FIS Failed (BFF)</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set any time a BIST FIS transmitted by PCH receives an R_ERR completion status from the device. <b>Note:</b> This bit must be cleared by software prior to initiating a BIST FIS.
9	<b>Port 1 BIST FIS Initiate (P1BFI)</b> —R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 1, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 1 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P1BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.
8	<b>Port 0 BIST FIS Initiate (P0BFI)</b> —R/W. When a rising edge is detected on this bit field, the PCH initiates a BIST FIS to the device on Port 0, using the parameters specified in this register and the data specified in BFTD1 and BFTD2. The BIST FIS will only be initiated if a device on Port 0 is present and ready (not partial/slumber state). After a BIST FIS is successfully completed, software must disable and re-enable the port using the PxE bits at offset 92h prior to attempting additional BIST FISes or to return the PCH to a normal operational mode. If the BIST FIS fails to complete, as indicated by the BFF bit in the register, then software can clear then set the P0BFI bit to initiate another BIST FIS. This can be retried until the BIST FIS eventually completes successfully.

Bits	Description
7:2	<b>BIST FIS Parameters (BFP)</b> —R/W. These 6 bits form the contents of the upper 6 bits of the BIST FIS Pattern Definition in any BIST FIS transmitted by the PCH. This field is not port specific—its contents will be used for any BIST FIS initiated on port 0, port 1, port 2, or port 3. The specific bit definitions are: Bit 7: T – Far End Transmit mode Bit 6: A – Align Bypass mode Bit 5: S – Bypass Scrambling Bit 4: L – Far End Retimed Loopback Bit 3: F – Far End Analog Loopback Bit 2: P – Primitive bit for use with Transmit mode
1:0	Reserved

### 11.1.36 BFTD1—BIST FIS Transmit Data1 Register (SATA—D31:F2)

Address Offset: E4h–E7h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bits	Description
31:0	<b>BIST FIS Transmit Data 1</b> —R/W. The data programmed into this register will form the contents of the second DWord of any BIST FIS initiated by the PCH. This register is not port specific—its contents will be used for BIST FIS initiated on any port. Although, the 2nd and 3rd DWords of the BIST FIS are only meaningful when the “T” bit of the BIST FIS is set to indicate “Far-End Transmit mode”; the contents of this register will be transmitted as the BIST FIS 2nd DWord, regardless of whether or not the “T” bit is indicated in the BFCS register (D31:F2:E0h).

### 11.1.37 BFTD2—BIST FIS Transmit Data2 Register (SATA—D31:F2)

Address Offset: E8h–EBh      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bits	Description
31:0	<b>BIST FIS Transmit Data 2</b> —R/W. The data programmed into this register will form the contents of the third DWord of any BIST FIS initiated by the PCH. This register is not port specific—its contents will be used for BIST FIS initiated on any port. Although the 2nd and 3rd DWords of the BIST FIS are only meaningful when the “T” bit of the BIST FIS is set to indicate “Far-End Transmit mode”, this register’s contents will be transmitted as the BIST FIS 3rd DWord, regardless of whether or not the “T” bit is indicated in the BFCS register (D31:F2:E0h).

## 11.2 Bus Master IDE I/O Registers (D31:F2)

The PCH does not support IDE mode. These registers are retained for SATA Testing Purposes Only.

The bus master IDE function uses 16 bytes of I/O space, allocated using the BAR register, located in D31:F2 Configuration space, offset 20h. All bus master IDE I/O space registers can be accessed as byte, word, or DWord quantities. Reading reserved bits returns an indeterminate, inconsistent value, and writes to reserved bits have no affect (but should not be attempted). These registers are only used for legacy operation. Software must not use these registers when running AHCI. All I/O registers are reset by Function Level Reset. The register address I/O map is shown in [Table 11-2](#).

**Table 11-2. Bus Master IDE I/O Register Address Map**

BAR+Offset	Mnemonic	Register	Default	Attribute
00h	BMICP	Command Register Primary	00h	R/W
01h	—	Reserved	—	RO
02h	BMISP	Bus Master IDE Status Register Primary	00h	R/W, R/WC, RO
03h	—	Reserved	—	RO
04h–07h	BMIDP	Bus Master IDE Descriptor Table Pointer Primary	xxxxxxxxh	R/W
08h	BMICS	Command Register Secondary	00h	R/W
09h	—	Reserved	—	RO
0Ah	BMISS	Bus Master IDE Status Register Secondary	00h	R/W, R/WC, RO
0Bh	—	Reserved	—	RO
0Ch–0Fh	BMIDS	Bus Master IDE Descriptor Table Pointer Secondary	xxxxxxxxh	R/W
10h	AIR	AHCI Index Register	00000000h	R/W, RO
14h	AIDR	AHCI Index Data Register	xxxxxxxxh	R/W

### 11.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F2)

Address Offset:	Primary: BAR + 00h Secondary: BAR + 08h	Attribute:	R/W, RO
Default Value:	00h	Size:	8 bits

**Note:** The PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description
7:4	Reserved. Returns 0.
3	<b>Read/Write Control (R/WC)</b> —R/W. This bit sets the direction of the bus master transfer. This bit must NOT be changed when the bus master function is active. 0 = Memory reads 1 = Memory writes
2:1	Reserved, Returns 0.
0	<b>Start/Stop Bus Master (START)</b> —R/W 0 = All state information is lost when this bit is cleared. Master mode operation cannot be stopped and then resumed. If this bit is reset while bus master operation is still active (that is, the Bus Master IDE Active bit (D31:F2:BAR + 02h, bit 0) of the Bus Master IDE Status register for that IDE channel is set) and the drive has not yet finished its data transfer (the Interrupt bit in the Bus Master IDE Status register for that IDE channel is not set), the bus master command is said to be aborted and data transferred from the drive may be discarded instead of being written to system memory. 1 = Enables bus master operation of the controller. Bus master operation does not actually start unless the Bus Master Enable bit (D31:F2:04h, bit 2) in PCI configuration space is also set. Bus master operation begins when this bit is detected changing from 0 to 1. The controller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halted by writing a 0 to this bit. <b>Note:</b> This bit is intended to be cleared by software after the data transfer is completed, as indicated by either the Bus Master IDE Active bit being cleared or the Interrupt bit of the Bus Master IDE Status register for that IDE channel being set, or both. Hardware does not clear this bit automatically. If this bit is cleared to 0 prior to the DMA data transfer being initiated by the drive in a device to memory data transfer, then the PCH will not send DMAT to terminate the data transfer. Software intervention (such as, sending SRST) is required to reset the interface in this condition.

## 11.2.2 BMIS[P,S]—Bus Master IDE Status Register (D31:F2)

Address Offset: Primary: BAR + 02h      Attribute: R/W, R/WC, RO  
                     Secondary: BAR + 0Ah  
 Default Value: 00h      Size: 8 bits

**Note:** PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description
7	<b>Simplex Only</b> —RO 0 = Both bus master channels (primary and secondary) can be operated independently and can be used at the same time. 1 = Only one channel may be used at the same time.
6	<b>Drive 1 DMA Capable</b> —R/W 0 = Not Capable. 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 1 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The PCH does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
5	<b>Drive 0 DMA Capable</b> —R/W 0 = Not Capable 1 = Capable. Set by device dependent code (BIOS or device driver) to indicate that drive 0 for this channel is capable of DMA transfers, and that the controller has been initialized for optimum performance. The PCH does not use this bit. It is intended for systems that do not attach BMIDE to the PCI bus.
4:3	Reserved. Returns 0.
2	<b>Interrupt</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = Set when a device FIS is received with the 'I' bit set, provided that software has not disabled interrupts using the IEN bit of the Device Control register.
1	<b>Error</b> —R/WC 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set when the controller encounters a target abort or master abort when transferring data on PCI.
0	<b>Bus Master IDE Active (ACT)</b> —RO. 0 = This bit is cleared by the PCH when the last transfer for a region is performed, where EOT for that region is set in the region descriptor. It is also cleared by the PCH when the Start Bus Master bit (D31:F2:BAR+ 00h, bit 0) is cleared in the Command register. When this bit is read as a 0, all data transferred from the drive during the previous bus master command is visible in system memory, unless the bus master command was aborted. 1 = Set by the PCH when the Start bit is written to the Command register.

### 11.2.3 BMID[P,S]—Bus Master IDE Descriptor Table Pointer Register (D31:F2)

Address Offset: Primary: BAR + 04h-07h Attribute: R/W, RO  
Secondary: BAR + 0Ch-0Fh  
Default Value: All bits undefined Size: 32 bits

**Note:** The PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description
31:2	<b>Address of Descriptor Table (ADDR)</b> —R/W. The bits in this field correspond to bits 31:2 of the memory location of the Physical Region Descriptor (PRD). The Descriptor Table must be DWord-aligned. The Descriptor Table must not cross a 64-K boundary in memory.
1:0	Reserved

### 11.2.4 AIR—AHCI Index Register (D31:F2)

Address Offset: Primary: BAR + 10h Attribute: R/W, RO  
Default Value: 00000000h Size: 32 bits

This register is available only when SCC is not 01h.

**Note:** The PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description
31:11	Reserved
10:2	<b>Index (INDEX)</b> —R/W. This Index register is used to select the DWord offset of the Memory Mapped AHCI register to be accessed. A DWord, Word, or Byte access is specified by the active byte enables of the I/O access to the Data register.
1:0	Reserved

### 11.2.5 AIDR—AHCI Index Data Register (D31:F2)

Address Offset: Primary: BAR + 14h Attribute: R/W  
Default Value: All bits undefined Size: 32 bits

This register is available only when SCC is not 01h.

**Note:** The PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description
31:0	<b>Data (DATA)</b> —R/W. This Data register is a “window” through which data is read or written to the AHCI memory mapped registers. A read or write to this Data register triggers a corresponding read or write to the memory mapped register pointed to by the Index register. The Index register must be setup prior to the read or write to this Data register. A physical register is not actually implemented as the data is actually stored in the memory mapped registers. Since this is not a physical register, the “default” value is the same as the default value of the register pointed to by Index.



## 11.3 Serial ATA Index/Data Pair Superset Registers

All of these I/O registers are in the core well. They are exposed only when SCC is 01h (that is, IDE programming interface).

These are Index/Data Pair registers that are used to access the Serial ATA superset registers (Serial ATA Status (PxSSTS), Serial ATA Control (PxSCTL) and Serial ATA Error (PxSERR)). The I/O space for these registers is allocated through SIDPBA. Locations with offset from 08h to 0Fh are reserved for future expansion. Software-write operations to the reserved locations will have no effect while software-read operations to the reserved locations will return 0.

**Note:** The PCH does not support IDE mode. These registers are retained for SATA Testing Purposes Only.

Offset	Mnemonic	Register
00h-03h	SINDEX	Serial ATA Index
04h-07h	SDATA	Serial ATA Data
08h-0Ch	—	Reserved
0Ch-0Fh	—	Reserved

### 11.3.1 SINDEX—Serial ATA Index Register (D31:F2)

Address Offset: SIDPBA + 00h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

**Note:** PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description
31:16	Reserved
15:8	<b>Port Index (PIDX)</b> —R/W. This Index field is used to specify the port of the SATA controller at which the port-specific SSTS, SCTL, and SERR registers are located. 00h = Primary Master (Port 0) 01h = Primary Slave (Port 2) 02h = Secondary Master (Port 1) 03h = Secondary Slave (Port 3) All other values are Reserved.
7:0	<b>Register Index (RIDX)</b> —R/W. This index field is used to specify one out of three registers currently being indexed into. These three registers are the Serial ATA superset SStatus, SControl and SError memory registers and are port specific; hence for this SATA controller, there are four sets of these registers. Refer to <a href="#">Section 11.4.2.10</a> , <a href="#">Section 11.4.2.11</a> , and <a href="#">Section 11.4.2.12</a> for definitions of the SStatus, SControl and SError registers. 00h = SSTS 01h = SCTL 02h = SERR All other values are Reserved.

### 11.3.2 SDATA—Serial ATA Data Register (D31:F2)

Address Offset: SIDPBA + 04h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

**Note:** The PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description
31:0	<p><b>Data (DATA)</b>—R/W. This Data register is a “window” through which data is read or written to from the register pointed to by the Serial ATA Index (SINDX) register above.</p> <p><b>Note:</b> A physical register is not actually implemented as the data is actually stored in the memory mapped registers.</p> <p>Since this is not a physical register, the “default” value is the same as the default value of the register pointed to by SINDX.RIDX field.</p>

#### 11.3.2.1 PxSSTS—Serial ATA Status Register (D31:F2)

Address Offset:      Attribute: RO, RO  
Default Value: 00000000h      Size: 32 bits

SDATA when SINDX.RIDX is 00h. This is a 32-bit register that conveys the current state of the interface and host. The PCH updates it continuously and asynchronously. When the PCH transmits a COMRESET to the device, this register is updated to its reset values.

**Note:** The PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description												
31:12	Reserved												
11:8	<p><b>Interface Power Management (IPM)</b>—RO. Indicates the current interface state:</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Device not present or communication not established</td> </tr> <tr> <td>1h</td> <td>Interface in active state</td> </tr> <tr> <td>2h</td> <td>Interface in PARTIAL power management state</td> </tr> <tr> <td>6h</td> <td>Interface in SLUMBER power management state</td> </tr> <tr> <td>8h</td> <td>Interface in DEVSLP power management state</td> </tr> </tbody> </table> <p>All other values reserved.</p>	Value	Description	0h	Device not present or communication not established	1h	Interface in active state	2h	Interface in PARTIAL power management state	6h	Interface in SLUMBER power management state	8h	Interface in DEVSLP power management state
Value	Description												
0h	Device not present or communication not established												
1h	Interface in active state												
2h	Interface in PARTIAL power management state												
6h	Interface in SLUMBER power management state												
8h	Interface in DEVSLP power management state												
7:4	<p><b>Current Interface Speed (SPD)</b>—RO. Indicates the negotiated interface communication speed.</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Device not present or communication not established</td> </tr> <tr> <td>1h</td> <td>Gen 1 communication rate negotiated</td> </tr> <tr> <td>2h</td> <td>Gen 2 communication rate negotiated</td> </tr> <tr> <td>3h</td> <td>Gen 3 communication rate negotiated</td> </tr> </tbody> </table> <p>All other values reserved.</p> <p>The PCH Supports Gen 1 communication rates (1.5Gb/s), Gen 2 rates (3.0Gb/s) and Gen 3 rates (6.0Gb/s)</p>	Value	Description	0h	Device not present or communication not established	1h	Gen 1 communication rate negotiated	2h	Gen 2 communication rate negotiated	3h	Gen 3 communication rate negotiated		
Value	Description												
0h	Device not present or communication not established												
1h	Gen 1 communication rate negotiated												
2h	Gen 2 communication rate negotiated												
3h	Gen 3 communication rate negotiated												



Bit	Description	
3:0	<b>Device Detection (DET)</b> —RO. Indicates the interface device detection and Phy state.	
	Value	Description
	0h	No device detected and Phy communication not established
	1h	Device presence detected but Phy communication not established
	3h	Device presence detected and Phy communication established
	4h	Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode
		All other values reserved.

### 11.3.2.2 PxSCTL—Serial ATA Control Register (D31:F2)

Address Offset: 00000000h Attribute: R/W, RO  
Default Value: 00000000h Size: 32 bits

SDATA when SINDEX.RIDX is 01h. This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the PCH or the interface. Reads from the register return the last value written to it.

**Note:** The PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description
31:20	Reserved
19:16	<b>Port Multiplier Port (PMP)</b> —R/W. This field is not used by AHCI.
15:12	<b>Select Power Management (SPM)</b> —R/W. This field is not used by AHCI.
11:8	<b>Interface Power Management Transitions Allowed (IPM)</b> —R/W. Indicates which power states the PCH is allowed to transition to:
Value	Description
0h	No interface restrictions
1h	Transitions to the PARTIAL state disabled
2h	Transitions to the SLUMBER state disabled
3h	Transitions to both PARTIAL and SLUMBER states disabled
4h	Transitions to the DEVSLP power management state disabled
5h	Transitions to the PARTIAL and DEVSLP power management states are disabled
6h	Transitions to the SLUMBER and DEVSLP power management states are disabled
7h	Transitions to the PARTIAL, SLUMBER and DEVSLP power management states are disabled
	All other values reserved.

Bit	Description											
7:4	<p><b>Speed Allowed (SPD)</b>—R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field.</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No speed negotiation restrictions</td> </tr> <tr> <td>1h</td> <td>Limit speed negotiation to Gen 1 communication rate</td> </tr> <tr> <td>2h</td> <td>Limit speed negotiation to Gen 2 communication rate</td> </tr> <tr> <td>3h</td> <td>Limit speed negotiation to Gen 3 communication rate</td> </tr> </tbody> </table> <p>All other values reserved. The PCH Supports Gen 1 communication rates (1.5Gb/s), Gen 2 rates (3.0Gb/s) and Gen 3 rates (6.0Gb/s)</p>		Value	Description	0h	No speed negotiation restrictions	1h	Limit speed negotiation to Gen 1 communication rate	2h	Limit speed negotiation to Gen 2 communication rate	3h	Limit speed negotiation to Gen 3 communication rate
Value	Description											
0h	No speed negotiation restrictions											
1h	Limit speed negotiation to Gen 1 communication rate											
2h	Limit speed negotiation to Gen 2 communication rate											
3h	Limit speed negotiation to Gen 3 communication rate											
3:0	<p><b>Device Detection Initialization (DET)</b>—R/W. Controls the PCH’s device detection and interface initialization.</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No device detection or initialization action requested</td> </tr> <tr> <td>1h</td> <td>Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized</td> </tr> <tr> <td>4h</td> <td>Disable the Serial ATA interface and put Phy in offline mode</td> </tr> </tbody> </table> <p>All other values reserved. When this field is written to a 1h, the PCH initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. This field may only be changed to 1h or 4h when PxCMD.ST is 0. Changing this field while the PCH is running results in undefined behavior.</p>		Value	Description	0h	No device detection or initialization action requested	1h	Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized	4h	Disable the Serial ATA interface and put Phy in offline mode		
Value	Description											
0h	No device detection or initialization action requested											
1h	Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized											
4h	Disable the Serial ATA interface and put Phy in offline mode											

### 11.3.2.3 PxSERR—Serial ATA Error Register (D31:F2)

Address Offset: Default Value: 00000000h Attribute: R/WC, RO Size: 32 bits

SDATA when SINDx.RIDX is 02h.

Bits 26:16 of this register contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

**Note:** PCH does not support IDE mode. This register is retained for SATA Testing Purposes Only.

Bit	Description	
31:27	Reserved	
26	<p><b>Exchanged (X)</b>—R/WC. When set to one, this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1 anytime a COMINIT signal is received. This bit is reflected in the POIS.PCS bit.</p>	
25	<p><b>Unrecognized FIS Type (F)</b>—R/WC. Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.</p>	
24	<p><b>Transport state transition error (T)</b>—R/WC. Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.</p>	

Bit	Description
23	<b>Link Sequence Error (S)</b> —R/WC. Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition.
22	<b>Handshake (H)</b> —R/WC. Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	<b>CRC Error (C)</b> —R/WC. Indicates that one or more CRC errors occurred with the Link Layer.
20	<b>Disparity Error (D)</b> —R/WC. This field is not used by AHCI.
19	<b>10b to 8b Decode Error (B)</b> —R/WC. Indicates that one or more 10b to 8b decoding errors occurred.
18	<b>Comm Wake (W)</b> —R/WC. Indicates that a Comm Wake signal was detected by the Phy.
17	<b>Phy Internal Error (I)</b> —R/WC. Indicates that the Phy detected some internal error.
16	<b>PhyRdy Change (N)</b> —R/WC. When set to 1, this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the PCH, this bit will be set when PhyRdy changes from a 0 -> 1 or a 1 -> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a 1 to it.
15:12	Reserved
11	<b>Internal Error (E)</b> —R/WC. The SATA controller failed due to a master or target abort when attempting to access system memory.
10	<b>Protocol Error (P)</b> —R/WC. A violation of the Serial ATA protocol was detected.  <b>Note:</b> The PCH does not set this bit for all protocol violations that may occur on the SATA link.
9	<b>Persistent Communication or Data Integrity Error (C)</b> —R/WC. A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.
8	<b>Transient Data Integrity Error (T)</b> —R/WC. A data integrity error occurred that was not recovered by the interface.
7:2	Reserved
1	<b>Recovered Communications Error (M)</b> —R/WC. Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	<b>Recovered Data Integrity Error (I)</b> —R/WC. A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

## 11.4 AHCI Registers (D31:F2)

**Note:** These registers are AHCI-specific and available when the PCH is properly configured. The Serial ATA Status, Control, and Error registers are special exceptions and may be accessed on all PCH components if properly configured; see [Section 11.3](#) for details.

The memory mapped registers within the SATA controller exist in non-cacheable memory space. Additionally, locked accesses are not supported. If software attempts to perform locked transactions to the registers, indeterminate results may occur. Register accesses shall have a maximum size of 64-bits; 64-bit access must not cross an 8-byte alignment boundary. All memory registers are reset by Function Level Reset unless specified otherwise.

The registers are broken into two sections—generic host control and port control. The port control registers are the same for all ports, and there are as many registers banks as there are ports.

**Table 11-3. AHCI Register Address Map**

ABAR + Offset	Mnemonic	Register
00-1Fh	GHC	Generic Host Control
20h-FFh	—	Reserved
100h-17Fh	P0PCR	Port 0 port control registers
180h-1FFh	P1PCR	Port 1 port control registers
200h-27Fh	P2PCR	Port 2 port control registers <b>Note:</b> Registers may be Reserved depending on if port is available in the given SKU. See <a href="#">Section 2.3</a> for details if port is available.
280h-2FFh	P3PCR	Port 3 port control registers <b>Note:</b> Registers may be Reserved depending on if port is available in the given SKU. See <a href="#">Section 2.3</a> for details if port is available.
300h-37Fh	--	Reserved
380h-3FFh	--	Reserved



## 11.4.1 AHCI Generic Host Control Registers (D31:F2)

Table 11-4. Generic Host Controller Register Address Map

ABAR + Offset	Mnemonic	Register	Default	Attribute
00h-03h	CAP	Host Capabilities	FF22FFC2h (desktop) DE127F03h (mobile)	R/WO, RO
04h-07h	GHC	Global PCH Control	00000000h	R/W, RO
08h-0Bh	IS	Interrupt Status	00000000h	R/WC, RO
0Ch-0Fh	PI	Ports Implemented	00000000h	R/WO, RO
10h-13h	VS	AHCI Version	00010300h	RO
1Ch-1Fh	EM_LOC	Enclosure Management Location	01600002h	RO
20h-23h	EM_CTRL	Enclosure Management Control	07010000h	R/W, R/WO, RO
24h-27h	CAP2	HBA Capabilities Extended	00000004h	RO
C8h-C9h	RSTF	Intel® RST Feature Capabilities	003Fh	R/WO, RO

### 11.4.1.1 CAP—Host Capabilities Register (D31:F2)

Address Offset: ABAR + 00h-03h Attribute: R/WO, RO  
Default Value: FF22FFC2h (Desktop) Size: 32 bits  
DE127F03h (Mobile)

Function Level Reset: No

All bits in this register that are R/WO are reset only by PLTRST#.

Bit	Description
31	<b>Supports 64-bit Addressing (S64A)</b> —RO. Indicates that the SATA controller can access 64-bit data structures. The 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry are read/write.
30	<b>Supports Command Queue Acceleration (SCQA)</b> —R/WO. When set to 1, indicates that the SATA controller supports SATA command queuing using the DMA Setup FIS. The PCH handles DMA Setup FISes natively, and can handle auto-activate optimization through that FIS.
29	<b>Supports SNotification Register (SSNTF)</b> —RO. When set to 1, indicates the SATA controller supports the PxSNTF (SNotification) register and its associated functionality. When cleared to 0, the SATA host does not support the PxSNTF (SNotification) register and its associated functionality.
28	<b>Supports Mechanical Presence Switch (SMPS)</b> —R/WO. When set to 1, indicates whether the SATA controller supports mechanical presence switches on its ports for use in hot-plug operations. This value is loaded by platform BIOS prior to operating system initialization.
27	<b>Supports Staggered Spin-up (SSS)</b> —R/WO. Indicates whether the SATA controller supports staggered spin-up on its ports, for use in balancing power spikes. This value is loaded by platform BIOS prior to OS initialization. 0 = Staggered spin-up not supported. 1 = Staggered spin-up supported.
26	<b>Supports Aggressive Link Power Management (SALP)</b> —R/WO 0 = Software shall treat the PxCMD.ALPE and PxCMD.ASP bits as reserved. 1 = The SATA controller supports auto-generating link requests to the partial or slumber states when there are no commands to process.
25	<b>Supports Activity LED (SAL)</b> —R/WO. Indicates that the SATA controller supports a single output pin (SATALED#) which indicates activity.

Bit	Description
24	<b>Supports Command List Override (SCLO)</b> —R/WO. When set to 1, indicates that the Controller supports the PxCMD.CLO bit and its associated function. When cleared to 0, the Controller is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.
23:20	<b>Interface Speed Support (ISS)</b> —R/WO. Indicates the maximum speed the SATA controller can support on its ports. 1h = 1.5Gb/s; 2h = 3Gb/s; 3h = 6Gb/s The default of this field is dependent upon the PCH SKU. If at least one PCH SATA port supports 6Gb/s, the default will be 3h. If no PCH SATA ports support 6Gb/s, then the default will be 2h and writes of 3h will be ignored by the PCH. See <a href="#">Section 2.3</a> for details on 6Gb/s port availability.
19	<b>Supports Non-Zero DMA Offsets (SNZO)</b> —RO. Reserved, as per the AHCI Revision 1.3 specification
18	<b>Supports AHCI Mode Only (SAM)</b> —RO. The SATA controller may optionally support AHCI access mechanism only. 0 = SATA controller supports both IDE and AHCI Modes 1 = SATA controller supports AHCI Mode Only  <b>Note:</b> BIOS should program this field as "1" since IDE mode is not supported.
17:16	Reserved
15	<b>PIO Multiple DRQ Block (PMD)</b> —RO. Hardwired to 1. The SATA controller supports PIO Multiple DRQ Command Block
14	<b>Slumber State Capable (SSC)</b> —R/WO. When set to 1, the SATA controller supports the slumber state.
13	<b>Partial State Capable (PSC)</b> —R/WO. When set to 1, the SATA controller supports the partial state.
12:8	<b>Number of Command Slots (NCS)</b> —RO. Hardwired to 1Fh to indicate support for 32 slots.
7	<b>Command Completion Coalescing Supported (CCCS)</b> —RO. 0 = Command Completion Coalescing Not Supported 1 = Command Completion Coalescing Supported
6	<b>Enclosure Management Supported (EMS)</b> —RO. 0 = Enclosure Management Not Supported 1 = Enclosure Management Supported
5	<b>Supports External SATA (SXS)</b> —R/WO. 0 = External SATA is not supported on any ports 1 = External SATA is supported on one or more ports When set, software can examine each SATA port's Command register (PxCMD) to determine which port is routed externally.
4:0	<b>Number of Ports (NPS)</b> —RO. Indicates number of supported ports. The number of ports indicated in this field may be more than the number of ports indicated in the PI (ABAR + 0Ch) register. Field value dependent on number of ports available in a given SKU. See <a href="#">Section 2.3</a> for details.

### 11.4.1.2 GHC—Global PCH Control Register (D31:F2)

Address Offset: ABAR + 04h-07h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31	<b>AHCI Enable (AE)</b> —RO. When set, this bit indicates that an AHCI driver is loaded and the controller will be talked to using AHCI mechanisms. Software will communicate with the PCH using AHCI. The PCH will not have to allow command processing using both AHCI and legacy mechanisms. When CAP.SAM is "1" per BIOS recommendation, this bit is Read Only and shall have a reset value of '1'.
30:3	Reserved
2	<b>MSI Revert to Single Message (MRSM)</b> —RO: When set to 1 by hardware, this bit indicates that the host controller requested more than one MSI vector but has reverted to using the first vector only. When this bit is cleared to 0, the Controller has not reverted to single MSI mode (that is, hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if MC.MME < MC.MMC). "MC.MSIE = 1" (MSI is enabled) "MC.MMC > 0" (multiple messages requested) "MC.MME" > 0" (more than one message allocated) "MC.MME! = MC.MMC" (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when MC.MSIE = 1 and MC.MME = 0h. In this case, the hardware has been programmed to use single MSI mode, and is not "reverting" to that mode. For PCH, the Controller shall always revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit is ignored when GHC.HR = 1.
1	<b>Interrupt Enable (IE)</b> —R/W. This global bit enables interrupts from the PCH. 0 = All interrupt sources from all ports are disabled. 1 = Interrupts are allowed from the AHCI controller.
0	<b>Controller Reset (HR)</b> —R/W. Resets the PCH AHCI controller. 0 = No effect 1 = When set by software, this bit causes an internal reset of the PCH AHCI controller. All state machines that relate to data transfers and queuing return to an idle condition, and all ports are re-initialized using COMRESET. <b>Note:</b> For further details, consult Section 10.4.3 of the Serial ATA Advanced Host Controller Interface specification, revision 1.3.

### 11.4.1.3 IS—Interrupt Status Register (D31:F2)

Address Offset: ABAR + 08h-0Bh      Attribute: R/WC, RO  
Default Value: 00000000h      Size: 32 bits

This register indicates which of the ports within the controller have an interrupt pending and require service.

Bit	Description
31:4	Reserved. Returns 0.
3	<b>Interrupt Pending Status Port[3] (IPS[3])—R/WC.</b> 0 = No interrupt pending. 1 = Port 3 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
2	<b>Interrupt Pending Status Port[2] (IPS[2])—R/WC.</b> 0 = No interrupt pending. 1 = Port 2 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
1	<b>Interrupt Pending Status Port[1] (IPS[1])—R/WC.</b> 0 = No interrupt pending. 1 = Port 1 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.
0	<b>Interrupt Pending Status Port[0] (IPS[0])—R/WC.</b> 0 = No interrupt pending. 1 = Port 0 has an interrupt pending. Software can use this information to determine which ports require service after an interrupt.

### 11.4.1.4 PI—Ports Implemented Register (D31:F2)

Address Offset: ABAR + 0Ch-0Fh      Attribute: R/WO, RO  
Default Value: 00000000h      Size: 32 bits  
Function Level Reset: No

This register indicates which ports are exposed to the PCH. It is loaded by platform BIOS. It indicates which ports that the device supports are available for software to use. For ports that are not available, software must not read or write to registers within that port. After BIOS issues initial write to this register, BIOS is requested to issue two reads to this register. If BIOS accesses any of the port specific AHCI address range before setting PI bit, BIOS is required to read the PI register before the initial write to the PI register.

Bit	Description
31:4	Reserved. Returns 0.
3	<b>Ports Implemented Port 3 (PI3)—R/WO</b> 0 = The port is not implemented. 1 = The port is implemented. <b>Note:</b> Bit may be Reserved and RO '0' depending on if port is available in the given SKU. See Section 2.3 for details if port is available.
2	<b>Ports Implemented Port 1 (PI2)—R/WO</b> 0 = The port is not implemented. 1 = The port is implemented.
1	<b>Ports Implemented Port 1 (PI1)—R/WO</b> 0 = The port is not implemented. 1 = The port is implemented.
0	<b>Ports Implemented Port 0 (PI0)—R/WO</b> 0 = The port is not implemented. 1 = The port is implemented.

#### 11.4.1.5 VS—AHCI Version Register (D31:F2)

Address Offset: ABAR + 10h-13h      Attribute: RO  
 Default Value: 00010300h      Size: 32 bits

This register indicates the major and minor version of the AHCI specification. It is BCD encoded. The upper two bytes represent the major version number, and the lower two bytes represent the minor version number. Example: Version 3.12 would be represented as 00030102h. The current version of the specification is 1.30 (00010300h).

Bit	Description
31:16	<b>Major Version Number (MJR)</b> —RO. Indicates the major version is 1.
15:0	<b>Minor Version Number (MNR)</b> —RO. Indicates the minor version is 30.

#### 11.4.1.6 EM\_LOC—Enclosure Management Location Register (D31:F2)

Address Offset: ABAR + 1Ch-1Fh      Attribute: RO  
 Default Value: 01600002h      Size: 32 bits

This register identifies the location and size of the enclosure management message buffer. This register is reserved if enclosure management is not supported (that is, CAP.EMS = 0).

Bit	Description
31:16	<b>Offset (OFST)</b> —RO. The offset of the message buffer in DWords from the beginning of the ABAR.
15:0	<b>Buffer Size (SZ)</b> —RO. Specifies the size of the transmit message buffer area in DWords. The PCH SATA controller only supports transmit buffer. A value of 0 is invalid.

#### 11.4.1.7 EM\_CTRL—Enclosure Management Control Register (D31:F2)

Address Offset: ABAR + 20h-23h      Attribute: R/W, R/WO, RO  
Default Value: 07010000h      Size: 32 bits

This register is used to control and obtain status for the enclosure management interface. This register includes information on the attributes of the implementation, enclosure management messages supported, the status of the interface, whether any message are pending, and is used to initiate sending messages. This register is reserved if enclosure management is not supported (CAP\_EMS = 0).

Bit	Description
31:27	Reserved
26	<b>Activity LED Hardware Driven (ATTR.ALHD)</b> —R/WO. 1 = The SATA controller drives the activity LED for the LED message type in hardware and does not utilize software for this LED. The host controller does not begin transmitting the hardware based activity signal until after software has written CTL.TM=1 after a reset condition.
25	<b>Transmit Only (ATTR.XMT)</b> —RO. 0 = The SATA controller supports transmitting and receiving messages. 1 = The SATA controller only supports transmitting messages and does not support receiving messages.
24	<b>Single Message Buffer (ATTR.SMB)</b> —RO. 0 = There are separate receive and transmit buffers such that unsolicited messages could be supported. 1 = The SATA controller has one message buffer that is shared for messages to transmit and messages received. Unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer.
23:20	Reserved
19	<b>SGPIO Enclosure Management Messages (SUPP.SGPIO)</b> —RO. 1 = The SATA controller supports the SGPIO register interface message type.
18	<b>SES-2 Enclosure Management Messages (SUPP.SES2)</b> —RO. 1 = The SATA controller supports the SES-2 message type.
17	<b>SAF-TE Enclosure Management Messages (SUPP.SAFTE)</b> —RO. 1 = The SATA controller supports the SAF-TE message type.
16	<b>LED Message Types (SUPP.LED)</b> —RO. 1 = The SATA controller supports the LED message type.
15:10	Reserved
9	<b>Reset (RST)</b> —R/W 0 = A write of 0 to this bit by software will have no effect. 1 = When set by software, The SATA controller resets all enclosure management message logic and takes all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the SATA controller completes the reset operation, the SATA controller sets the value to 0.
8	<b>Transmit Message (CTL.TM)</b> —R/W 0 = A write of 0 to this bit by software will have no effect. 1 = When set by software, The SATA controller transmits the message contained in the message buffer. When the message is completely sent, the SATA controller sets the value to 0. Software must not change the contents of the message buffer while CTL.TM is set to 1.
7:1	Reserved
0	<b>Message Received (STS.MR)</b> —RO. Message Received is not supported in the PCH.



#### 11.4.1.8 CAP2—HBA Capabilities Extended Register

Address Offset: ABAR + 24h-27h Attribute: R/WO, RO  
 Default Value: 00000004h Size: 32 bits  
 Function Level Reset: No

This register indicates basic capabilities of the HBA to driver software. The R/WO bits in this register are only cleared upon PLTRST#.

Bit	Description
31:6	Reserved
5	<b>DEVSLP Entrance from Slumber Only (DESO)</b> —R/WO. This bit specifies that the host will only assert DEVSLP if the interface is in Slumber. 0 = The host may enter DEVSLP from any link state (Active, Partial, or Slumber) 1 = The host shall ignore software direct entrance to DEVSLP by means of PxCMD.ICC bit unless PxSSTS.IPM = 6h.
4	<b>Aggressive DEVSLP Management Support (SADM)</b> —R/WO. 0= Aggressive DEVSLP Management is not supported and software will treat the PxDEVSLP.ADSE field as reserved. 1= The host supports hardware assertion of the DEVSLP signal after the idle timeout expires.
3	<b>Supports DEVSLP (SDS)</b> —R/WO. 0 = DEVSLP is not supported 1 = DEVSLP is supported
2	<b>Automatic Partial to Slumber Transitions (APST)</b> —R/WO. 0 = Not supported 1 = Supported
1	Reserved
0	<b>BIOS/OS Handoff (BOH)</b> —RO. Not supported.

#### 11.4.1.9 RSTF—Intel® RST Feature Capabilities Register

Address Offset: ABAR + C8h-C9h Attribute: R/WO, RO  
 Default Value: 003Fh Size: 16 bits  
 Function Level Reset: No

No hardware action is taken on this register. This register is needed for the Intel® Rapid Storage Technology software. These bits are set by BIOS to request the feature from the appropriate Intel Rapid Storage Technology software.

Bit	Description
15:12	Reserved
11:10	<b>OROM UI Normal Delay (OUD)</b> —R/WO. The values of these bits specify the delay of the OROM UI Splash Screen in a normal status. 00 = 2 Seconds (Default) 01 = 4 Seconds 10 = 6 Seconds 11 = 8 Seconds If bit 5 = 0b these values will be disregarded.
9	<b>Intel® Smart Response Technology Enable Request (SEREQ)</b> —R/WO. Indicates the requested status of the Intel Smart Response Technology support. 0 = Disabled 1 = Enabled

Bit	Description
8	<b>Intel® RRT Only on eSATA (ROES)</b> —R/WO. Indicates the request that only Intel® Rapid Recovery Technology (RRT) volumes can span internal and external SATA (eSATA). If not set, any RAID volume can span internal and external SATA. 0 = Disabled 1 = Enabled
7	Reserved
6	<b>HDD Unlock (HDDLK)</b> —R/WO. Indicates the requested status of HDD password unlock in the OS. 0 = Disabled 1 = Enabled
5	<b>Intel® RST OROM UI (RSTOROMUI)</b> —R/WO. Indicates the requested status of the Intel® RST OROM UI display. 0 = The Intel RST OROM UI and banner are not displayed if all disks and RAID volumes have a normal status. 1 = The Intel RST OROM UI is displayed during each boot.
4	<b>Intel® RRT Enable (RSTE)</b> —R/WO. Indicates the requested status of the Intel® Rapid Recovery Technology support. 0 = Disabled 1 = Enabled
3	<b>RAID 5 Enable (R5E)</b> —R/WO. Indicates the requested status of RAID 5 support. 0 = Disabled 1 = Enabled
2	<b>RAID 10 Enable (R10E)</b> —R/WO. Indicates the requested status of RAID 10 support. 0 = Disabled 1 = Enabled
1	<b>RAID 1 Enable (R1E)</b> —R/WO. Indicates the requested status of RAID 1 support. 0 = Disabled 1 = Enabled
0	<b>RAID 0 Enable (R0E)</b> —R/WO. Indicates the requested status of RAID 0 support. 0 = Disabled 1 = Enabled

## 11.4.2 Port Registers (D31:F2)

Ports not available will result in the corresponding Port DMA register space being reserved. The controller shall ignore writes to the reserved space on write cycles and shall return 0 on read cycle accesses to the reserved location.

**Note:** Registers shall return 0 on read cycle accesses to the reserved location.

**Note:** Registers maybe reserved depending on if the port is available in the given SKU. See [Section 2.3](#) to determine if the port is available.

**Table 11-5. Port [3:0] DMA Register Address Map (Sheet 1 of 3)**

ABAR + Offset	Mnemonic	Register
100h-103h	P0CLB	Port 0 Command List Base Address
104h-107h	P0CLBU	Port 0 Command List Base Address Upper 32 bits
108h-10Bh	P0FB	Port 0 FIS Base Address
10Ch-10Fh	P0FBU	Port 0 FIS Base Address Upper 32 bits
110h-113h	POIS	Port 0 Interrupt Status
114h-117h	POIE	Port 0 Interrupt Enable
118h-11Bh	P0CMD	Port 0 Command
11Ch-11Fh	—	Reserved
120h-123h	P0TFD	Port 0 Task File Data
124h-127h	P0SIG	Port 0 Signature
128h-12Bh	P0SSTS	Port 0 Serial ATA Status
12Ch-12Fh	P0SCTL	Port 0 Serial ATA Control
130h-133h	P0SERR	Port 0 Serial ATA Error
134h-137h	P0SACT	Port 0 Serial ATA Active
138h-13Bh	P0CI	Port 0 Command Issue
13Ch-13Fh	P0SNFT	P0SNFT
140h-143h	—	Reserved
144h-147h	P0DEVSLP	Port 0 Device Sleep
148h-17Fh	—	Reserved
180h-183h	P1CLB	Port 1 Command List Base Address
184h-187h	P1CLBU	Port 1 Command List Base Address Upper 32 bits
188h-18Bh	P1FB	Port 1 FIS Base Address
18Ch-18Fh	P1FBU	Port 1 FIS Base Address Upper 32 bits
190h-193h	P1IS	Port 1 Interrupt Status
194h-197h	P1IE	Port 1 Interrupt Enable
198h-19Bh	P1CMD	Port 1 Command
19Ch-19Fh	—	Reserved
1A0h-1A3h	P1TFD	Port 1 Task File Data
1A4h-1A7h	P1SIG	Port 1 Signature
1A8h-1ABh	P1SSTS	Port 1 Serial ATA Status
1ACh-1AFh	P1SCTL	Port 1 Serial ATA Control
1B0h-1B3h	P1SERR	Port 1 Serial ATA Error

**Table 11-5. Port [3:0] DMA Register Address Map (Sheet 2 of 3)**

ABAR + Offset	Mnemonic	Register
1B4h-1B7h	P1SACT	Port 1 Serial ATA Active
1B8h-1BBh	P1CI	Port 1 Command Issue
1BCh-1BFh	P1SNFT	P1SNFT
1C0h-1C3h	—	Reserved
1C4h-1C7h	P1DEVSLP	Port 1 Device Sleep
1C8h-1FFh	—	Reserved
200h-203h	P2CLB	Port 2 Command List Base Address
204h-207h	P2CLBU	Port 2 Command List Base Address Upper 32 bits
208h-20Bh	P2FB	Port 2 FIS Base Address
20Ch-20Fh	P2FBU	Port 2 FIS Base Address Upper 32 bits
210h-213h	P2IS	Port 2 Interrupt Status
214h-217h	P2IE	Port 2 Interrupt Enable
218h-21Bh	P2CMD	Port 2 Command
21Ch-21Fh	—	Reserved
220h-223h	P2TFD	Port 2 Task File Data
224h-227h	P2SIG	Port 2 Signature
228h-22Bh	P2SSTS	Port 2 Serial ATA Status
22Ch-22Fh	P2SCTL	Port 2 Serial ATA Control
230h-233h	P2SERR	Port 2 Serial ATA Error
234h-237h	P2SACT	Port 2 Serial ATA Active
238h-23Bh	P2CI	Port 2 Command Issue
23Ch-23Fh	P2SNFT	P2SNFT
240h-243h	—	Reserved
244h-247h	P2DEVSLP	Port 2 Device Sleep
247h-27Fh	—	Reserved
280h-283h	P3CLB	Port 3 Command List Base Address
284h-287h	P3CLBU	Port 3 Command List Base Address Upper 32 bits
288h-28Bh	P3FB	Port 3 FIS Base Address
28Ch-28Fh	P3FBU	Port 3 FIS Base Address Upper 32 bits
290h-293h	P3IS	Port 3 Interrupt Status
294h-297h	P3IE	Port 3 Interrupt Enable
298h-29Bh	P3CMD	Port 3 Command
29Ch-29Fh	—	Reserved
2A0h-2A3h	P3TFD	Port 3 Task File Data
2A4h-2A7h	P3SIG	Port 3 Signature
2A8h-2ABh	P3SSTS	Port 3 Serial ATA Status
2ACh-2AFh	P3SCTL	Port 3 Serial ATA Control
2B0h-2B3h	P3SERR	Port 3 Serial ATA Error
2B4h-2B7h	P3SACT	Port 3 Serial ATA Active
2B8h-2BBh	P3CI	Port 3 Command Issue

**Table 11-5. Port [3:0] DMA Register Address Map (Sheet 3 of 3)**

ABAR + Offset	Mnemonic	Register
2BCh-2BFh	P3SNFT	P3SNFT
2C0h-2C3h	—	Reserved
2C4h-2C7h	P2DEVSLP	Port 2 Device Sleep
2C8h-2FFh	—	Reserved

#### 11.4.2.1 PxCLB—Port [3:0] Command List Base Address Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 100h      Attribute: R/W, RO  
 Port 1: ABAR + 180h  
 Port 2: ABAR + 200h  
 Port 3: ABAR + 280h

Default Value: Undefined      Size: 32 bits

Bit	Description
31:10	<b>Command List Base Address (CLB)</b> —R/W. Indicates the 32-bit base for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address range is 1KB in length. This address must be 1KB aligned as indicated by bits 31:10 being read/write. These bits are not reset on a Controller reset.
9:0	Reserved

#### 11.4.2.2 PxCLBU—Port [3:0] Command List Base Address Upper 32-Bits Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 104h      Attribute: R/W  
 Port 1: ABAR + 184h  
 Port 2: ABAR + 204h  
 Port 3: ABAR + 284h

Default Value: Undefined      Size: 32 bits

Bit	Description
31:0	<b>Command List Base Address Upper (CLBU)</b> —R/W. Indicates the upper 32-bits for the command list base address for this port. This base is used when fetching commands to execute. These bits are not reset on a Controller reset.

#### 11.4.2.3 PxFB—Port [3:0] FIS Base Address Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 108h      Attribute: R/W, RO  
 Port 1: ABAR + 188h  
 Port 2: ABAR + 208h  
 Port 3: ABAR + 288h

Default Value: Undefined      Size: 32 bits

Bit	Description
31:8	<b>FIS Base Address (FB)</b> —R/W. Indicates the 32-bit base for received FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256-byte aligned, as indicated by bits 31:3 being read/write. These bits are not reset on a Controller reset.
7:0	Reserved

#### 11.4.2.4 PxFBU—Port [3:0] FIS Base Address Upper 32-Bits Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 10Ch      Attribute: R/W  
 Port 1: ABAR + 18Ch  
 Port 1: ABAR + 20Ch  
 Port 2: ABAR + 28Ch

Default Value: Undefined      Size: 32 bits

Bit	Description
31:0	<b>FIS Base Address Upper (FBU)</b> —R/W. Indicates the upper 32-bits for the received FIS base for this port. These bits are not reset on a Controller reset.

### 11.4.2.5 PxIS—Port [3:0] Interrupt Status Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 110h      Attribute: R/WC, RO  
                   Port 1: ABAR + 190h  
                   Port 2: ABAR + 210h  
                   Port 3: ABAR + 290h  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31	<b>Cold Port Detect Status (CPDS)</b> —RO. Cold presence detect is not supported.
30	<b>Task File Error Status (TFES)</b> —R/WC. This bit is set whenever the status register is updated by the device and the error bit (PxTFD.bit 0) is set.
29	<b>Host Bus Fatal Error Status (HBFS)</b> —R/WC. Indicates that the PCH encountered an error that it cannot recover from due to a bad software pointer. In PCI, such an indication would be a target or master abort.
28	<b>Host Bus Data Error Status (HBDS)</b> —R/WC. Indicates that the PCH encountered a data error (uncorrectable ECC/parity) when reading from or writing to system memory.
27	<b>Interface Fatal Error Status (IFS)</b> —R/WC. Indicates that the PCH encountered an error on the SATA interface which caused the transfer to stop.
26	<b>Interface Non-fatal Error Status (INFS)</b> —R/WC. Indicates that the PCH encountered an error on the SATA interface but was able to continue operation.
25	Reserved
24	<b>Overflow Status (OFS)</b> —R/WC. Indicates that the PCH received more bytes from a device than was specified in the PRD table for the command.
23	<b>Incorrect Port Multiplier Status (IPMS)</b> —R/WC. The PCH SATA controller does not support Port Multipliers.
22	<b>PhyRdy Change Status (PRCS)</b> —RO. When set to one, this bit indicates the internal PhyRdy signal changed state. This bit reflects the state of PxSERR.DIAG.N. Unlike most of the other bits in the register, this bit is RO and is only cleared when PxSERR.DIAG.N is cleared.  <b>Note:</b> The internal PhyRdy signal also transitions when the port interface enters partial or slumber power management states. Partial and slumber must be disabled when Surprise Removal Notification is desired; otherwise, the power management state transitions will appear as false insertion and removal events.
21:8	Reserved
7	<b>Device Interlock Status (DIS)</b> —R/WC. When set, this bit indicates that a platform mechanical presence switch has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid in systems that support a mechanical presence switch (CAP.SIS [ABAR+00:bit 28] set). For systems that do not support a mechanical presence switch, this bit will always be 0.
6	<b>Port Connect Change Status (PCS)</b> —RO. This bit reflects the state of PxSERR.DIAG.X. (ABAR+130h/1D0h/230h/2D0h, bit 26) Unlike other bits in this register, this bit is only cleared when PxSERR.DIAG.X is cleared. 0 = No change in Current Connect Status. 1 = Change in Current Connect Status.
5	<b>Descriptor Processed (DPS)</b> —R/WC. A PRD with the I bit set has transferred all its data.
4	<b>Unknown FIS Interrupt (UFS)</b> —RO. When set to 1, this bit indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to 0 by software clearing the PxSERR.DIAG.F bit to 0. This bit does not directly reflect the PxSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when the FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1 or the two bits may become out of sync.
3	<b>Set Device Bits Interrupt (SDBS)</b> —R/WC. A Set Device Bits FIS has been received with the I bit set and has been copied into system memory.
2	<b>DMA Setup FIS Interrupt (DSS)</b> —R/WC. A DMA Setup FIS has been received with the I bit set and has been copied into system memory.
1	<b>PIO Setup FIS Interrupt (PSS)</b> —R/WC. A PIO Setup FIS has been received with the I bit set, it has been copied into system memory, and the data related to that FIS has been transferred.

Bit	Description
0	<b>Device to Host Register FIS Interrupt (DHRS)</b> —R/WC. A D2H Register FIS has been received with the I bit set, and has been copied into system memory.

#### 11.4.2.6 PxIE—Port [3:0] Interrupt Enable Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 114h      Attribute: R/W, RO  
 Port 1: ABAR + 194h  
 Port 2: ABAR + 214h  
 Port 3: ABAR + 294h

Default Value: 00000000h      Size: 32 bits

This register enables and disables the reporting of the corresponding interrupt to system software. When a bit is set (1) and the corresponding interrupt condition is active, then an interrupt is generated. Interrupt sources that are disabled (0) are still reflected in the status registers.

Bit	Description
31	<b>Cold Presence Detect Enable (CPDE)</b> —RO. Cold Presence Detect is not supported.
30	<b>Task File Error Enable (TFEE)</b> —R/W. When set, and GHC.IE and PxTFD.STS.ERR (due to a reception of the error register from a received FIS) are set, the PCH will generate an interrupt.
29	<b>Host Bus Fatal Error Enable (HBFE)</b> —R/W. When set, and GHC.IE and PxS.HBFS are set, the PCH will generate an interrupt.
28	<b>Host Bus Data Error Enable (HBDE)</b> —R/W. When set, and GHC.IE and PxS.HBDS are set, the PCH will generate an interrupt.
27	<b>Interface Fatal Error Status (IFS)</b> —R/WC. Indicates that the PCH encountered an error on the SATA interface which caused the transfer to stop.
26	<b>Interface Non-fatal Error Enable (INFE)</b> —R/W. When set, GHC.IE is set, and PxIS.INFS is set, the PCH will generate an interrupt.
25	Reserved
24	<b>Overflow Error Enable (OFE)</b> —R/W. When set, and GHC.IE and PxS.OFS are set, the PCH will generate an interrupt.
23	<b>Incorrect Port Multiplier Enable (IPME)</b> —R/W. The PCH SATA controller does not support Port Multipliers. BIOS and storage software should keep this bit cleared to 0.
22	<b>PhyRdy Change Interrupt Enable (PRCE)</b> —R/W. When set, and GHC.IE is set, and PxIS.PRCS is set, the PCH shall generate an interrupt.
21:8	Reserved
7	<b>Device Mechanical Enable (DMPE)</b> —R/W. When set, and PxIS.DIS is set, the PCH will generate an interrupt. For systems that do not support an mechanical presence switch, this bit shall be a read-only 0.
6	<b>Port Change Interrupt Enable (PCE)</b> —R/W. When set, and GHC.IE and PxS.PCS are set, the PCH will generate an interrupt.
5	<b>Descriptor Processed Interrupt Enable (DPE)</b> —R/W. When set, and GHC.IE and PxS.DPS are set, the PCH will generate an interrupt.
4	<b>Unknown FIS Interrupt Enable (UFIE)</b> —R/W. When set, and GHC.IE is set and an unknown FIS is received, the PCH will generate this interrupt.
3	<b>Set Device Bits FIS Interrupt Enable (SDBE)</b> —R/W. When set, and GHC.IE and PxS.SDBS are set, the PCH will generate an interrupt.
2	<b>DMA Setup FIS Interrupt Enable (DSE)</b> —R/W. When set, and GHC.IE and PxS.DSS are set, the PCH will generate an interrupt.
1	<b>PIO Setup FIS Interrupt Enable (PSE)</b> —R/W. When set, and GHC.IE and PxS.PSS are set, the PCH will generate an interrupt.
0	<b>Device to Host Register FIS Interrupt Enable (DHRE)</b> —R/W. When set, and GHC.IE and PxS.DHRS are set, the PCH will generate an interrupt.

### 11.4.2.7 PxCMD—Port [3:0] Command Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 118h      Attribute: R/W, RO, R/WO  
 Port 1: ABAR + 198h  
 Port 2: ABAR + 218h  
 Port 3: ABAR + 298h

Default Value: 0000w00wh      Size: 32 bits  
 where w = 00?0b (for?, see bit description)

Function Level Reset: Yes, with exceptions (FLR not reset for bits 21, 19, and 18)

Bit	Description	
31:28	Value	Definition
	31:28	<b>Interface Communication Control (ICC)</b> —R/W. This is a four bit field that can be used to control reset and power states of the interface. Writes to this field will cause actions on the interface, either as primitives or an OOB sequence, and the resulting status of the interface will be reported in the PxSSTS register (Address offset Port 0:ABAR+124h, Port 1: ABAR+1A4h, Port 2: ABAR+224h, Port 3: ABAR+2A4h).
	8	DEVSLP: This will cause the PCH to assert the DEVSLP signal associated with the port. The PCH will ignore the DEVSLP idle timeout value that is specified by PxDEVSLP.DITO. Software will only request DEVSLP when the interface is in an idle state (that is, PxCI is cleared to 0h and PxSACT is cleared to 0h). If the interface is not idle at the time this register is written, then the PCH will take no action and the interface will remain in its current state. If pxCAP2.DESO is set to '1' and PxSSTS.IPM is not set to '6h', then the host will take no action on the interface and will remain in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion).
	7	Reserved
	6h	Slumber: This will cause the PCH to request a transition of the interface to the slumber state. The SATA device may reject the request and the interface will remain in its current state.
	5h-3h	Reserved
	2h	Partial: This will cause the PCH to request a transition of the interface to the partial state. The SATA device may reject the request and the interface will remain in its current state.
	1h	Active: This will cause the PCH to request a transition of the interface into the active state. If the requested transition is from the DEVSLP state, then the host controller shall wait until PxDEVSLP.DMAT has expired before de-asserting the DEVSLP Signal.
	0h	No-Op/Idle: When software reads this value, it indicates the PCH is not in the process of changing the interface state or sending a device reset, and a new link command may be issued.
	When system software writes a non-reserved value other than No-Op (0h), the PCH will perform the action and update this field back to Idle (0h).	
	If software writes to this field to change the state to a state the link is already in (such as, interface is in the active state and a request is made to go to the active state), the PCH will take no action and return this field to Idle. If the interface is in a low-power state and software wants to transition to a different low-power state, software must first bring the link to active and then initiate the transition to the desired low-power state (with the exception of DEVSLP). The transition to DEVSLP may occur from any other state if CAP2.DESO is cleared to "0". If CAP2.DESO is set to "1", then DEVSLP may only be transitioned to if the link is in Slumber.	
	<b>Note:</b> When the ALPE bit—bit 26 is set, then this register should not be set to 02h or 06h.	

Bit	Description
27	<b>Aggressive Slumber/Partial (ASP)</b> —R/W. When set to 1, and the ALPE bit—bit 26 is set, the PCH shall aggressively enter the slumber state when it clears the PxCI register and the PxSACT register is cleared. When cleared, and the ALPE bit is set, the PCH will aggressively enter the partial state when it clears the PxCI register and the PxSACT register is cleared. If CAP.SALP is cleared to 0, software shall treat this bit as reserved.
26	<b>Aggressive Link Power Management Enable (ALPE)</b> —R/W. When set to 1, the PCH will aggressively enter a lower link power state (partial or slumber) based upon the setting of the ASP bit—bit 27.
25	<b>Drive LED on ATAPI Enable (DLAE)</b> —R/W. When set to 1, the PCH will drive the LED pin active for ATAPI commands (PxCLB[CHz.A] set) in addition to ATA commands. When cleared, the PCH will only drive the LED pin active for ATA commands. See <a href="#">Section 5.15.4</a> for details on the activity LED.
24	<b>Device is ATAPI (ATAPI)</b> —R/W. When set to 1, the connected device is an ATAPI device. This bit is used by the PCH to control whether or not to generate the desktop LED when commands are active. See <a href="#">Section 5.15.4</a> for details on the activity LED.
23	<b>Automatic Partial Slumber Transitions Enabled (APSTE)</b> —R/W. 0 = This port will not perform Automatic Partial to Slumber Transitions. 1 = The HBA may perform Automatic Partial to Slumber Transitions.  <b>Note:</b> Software should only set this bit to '1' if CAP2.APST is set to '1'.
22	Reserved
21	<b>External SATA Port (ESP)</b> —R/WO 0 = This port supports internal SATA devices only. 1 = This port will be used with an external SATA device and hot-plug is supported. When set, CAP.SXS must also be set. This bit is not reset by Function Level Reset.
20	Reserved
19	<b>Mechanical Switch Attached to Port (MPSP)</b> —R/WO. If set to 1, the PCH supports a mechanical presence switch attached to this port. The PCH takes no action on the state of this bit – it is for system software only. For example, if this bit is cleared, and an mechanical presence switch toggles, the PCH still treats it as a proper mechanical presence switch event.  <b>Note:</b> This bit is not reset on a Controller reset or by a Function Level Reset.
18	<b>Hot-Plug Capable Port (HPCP)</b> —R/WO 0 = Port is not capable of hot-plug. 1 = Port is hot-plug capable. This indicates whether the platform exposes this port to a device that can be hot-plugged. SATA by definition is hot-pluggable, but not all platforms are constructed to allow the device to be removed (it may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as "eject device" to the end-user. The PCH takes no action on the state of this bit—it is for system software only. For example, if this bit is cleared, and a hot-plug event occurs, the PCH still treats it as a proper hot-plug event.  <b>Note:</b> This bit is not reset on a Controller reset or by a Function Level Reset.
17:16	Reserved
15	<b>Controller Running (CR)</b> —RO. When this bit is set, the DMA engines for a port are running.
14	<b>FIS Receive Running (FR)</b> —RO. When set, the FIS Receive DMA engine for the port is running.
13	<b>Mechanical Presence Switch State (MPSS)</b> —RO. The MPSS bit reports the state of a mechanical presence switch attached to this port. If CAP.SMPS is set to 1 and the mechanical presence switch is closed, then this bit is cleared to 0. If CAP.SMPS is set to 1 and the mechanical presence switch is open, then this bit is set to 1. If CAP.SMPS is set to '0', then this bit is cleared to 0. Software should only use this bit if both CAP.SMPS and PxCMD.MPSP are set to 1.
12:8	<b>Current Command Slot (CCS)</b> —RO. Indicates the current command slot the PCH is processing. This field is valid when the ST bit is set in this register, and is constantly updated by the PCH. This field can be updated as soon as the PCH recognizes an active command slot, or at some point soon after when it begins processing the command. This field is used by software to determine the current command issue location of the PCH. In queued mode, software shall not use this field, as its value does not represent the current command being executed. Software shall only use PxCI and PxSACT when running queued commands.



Bit	Description
7:5	Reserved
4	<p><b>FIS Receive Enable (FRE)</b>—R/W. When set, the PCH may post received FISes into the FIS receive area pointed to by PxFB (ABAR+108h/188h/208h/288h) and PxFBU (ABAR+10Ch/18Ch/20Ch/28Ch). When cleared, received FISes are not accepted by the PCH, except for the first D2H (device-to-host) register FIS after the initialization sequence.</p> <p>System software must not set this bit until PxFB (PxFBU) have been programmed with a valid pointer to the FIS receive area, and if software wishes to move the base, this bit must first be cleared, and software must wait for the FR bit—bit 14 in this register to be cleared.</p>
3	<p><b>Command List Override (CLO)</b>—R/W. Setting this bit to 1 causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The controller sets this bit to 0 when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to 0. A write to this register with a value of 0 shall have no effect.</p> <p>This bit shall only be set to 1 immediately prior to setting the PxCMD.ST bit to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to 0 before setting PxCMD.ST to 1.</p>
2	<b>Power On Device (POD)</b> —RO. Cold presence detect not supported. Defaults to 1.
1	<p><b>Spin-Up Device (SUD)</b>—R/W/RO. This bit is R/W and defaults to 0 for systems that support staggered spin-up (R/W when CAP.SSS (ABAR+00h:bit 27) is 1). Bit is RO 1 for systems that do not support staggered spin-up (when CAP.SSS is 0).</p> <p>0 = No action.</p> <p>1 = On an edge detect from 0 to 1, the PCH starts a COMRESET initialization sequence to the device.</p> <p>Clearing this bit to 0 does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and PxSCTL.DET=0h, the controller will enter listen mode.</p>
0	<p><b>Start (ST)</b>—R/W. When set, the PCH may process the command list. When cleared, the PCH may not process the command list. Whenever this bit is changed from a 0 to a 1, the PCH starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, the PxCI register is cleared by the PCH upon the PCH putting the controller into an idle state.</p> <p>Refer to section 10.3 of the Serial ATA AHCI Specification for important restrictions on when ST can be set to 1 and cleared to 0.</p>

#### 11.4.2.8 PxTFD—Port [3:0] Task File Data Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 120h      Attribute: RO  
 Port 1: ABAR + 1A0h  
 Port 2: ABAR + 220h  
 Port 3: ABAR + 2A0h

Default Value: 0000007Fh      Size: 32 bits

This is a 32-bit register that copies specific fields of the task file when FISes are received. The FISes that contain this information are: D2H Register FIS, PIO Setup FIS and Set Device Bits FIS.

The FISes that contain this information are:

- D2H Register FIS
- PIO Setup FIS
- Set Device Bits FIS (BSY and DRQ are not updated with this FIS)

Bit	Description		
31:16	Reserved		
15:8	<b>Error (ERR)</b> —RO. Contains the latest copy of the task file error register.		
7:0	<b>Status (STS)</b> —RO. Contains the latest copy of the task file status register. Fields of <b>Note</b> in this register that affect AHCI.		
Bit	Field	Definition	
7	BSY	Indicates the interface is busy	
6:4	N/A	Not applicable	
3	DRQ	Indicates a data transfer is requested	
2:1	N/A	Not applicable	
0	ERR	Indicates an error during the transfer	



### 11.4.2.9 PxSIG—Port [3:0] Signature Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 124h Attribute: RO

Port 1: ABAR + 1A4h

Port 2: ABAR + 224h

Port 3: ABAR + 2A4h

Default Value: FFFFFFFFh Size: 32 bits

This is a 32-bit register that contains the initial signature of an attached device when the first D2H Register FIS is received from that device. It is updated once after a reset sequence.

Bit	Description											
31:0	<p><b>Signature (SIG)</b>—RO. Contains the signature received from a device on the first D2H register FIS. The bit order is as follows:</p> <table> <thead> <tr> <th>Bit</th> <th>Field</th> </tr> </thead> <tbody> <tr> <td>31:24</td> <td>LBA High Register</td> </tr> <tr> <td>23:16</td> <td>LBA Mid Register</td> </tr> <tr> <td>15:8</td> <td>LBA Low Register</td> </tr> <tr> <td>7:0</td> <td>Sector Count Register</td> </tr> </tbody> </table>		Bit	Field	31:24	LBA High Register	23:16	LBA Mid Register	15:8	LBA Low Register	7:0	Sector Count Register
Bit	Field											
31:24	LBA High Register											
23:16	LBA Mid Register											
15:8	LBA Low Register											
7:0	Sector Count Register											

### 11.4.2.10 PxSSTS—Port [3:0] Serial ATA Status Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 128h Attribute: RO

Port 1: ABAR + 1A8h

Port 2: ABAR + 228h

Port 3: ABAR + 2A8h

Default Value: 00000000h Size: 32 bits

This is a 32-bit register that conveys the current state of the interface and host. The PCH updates it continuously and asynchronously. When the PCH transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description															
31:12	Reserved															
11:8	<p><b>Interface Power Management (IPM)</b>—RO. Indicates the current interface state:</p> <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Device not present or communication not established</td> </tr> <tr> <td>1h</td> <td>Interface in active state</td> </tr> <tr> <td>2h</td> <td>Interface in PARTIAL power management state</td> </tr> <tr> <td>6h</td> <td>Interface in SLUMBER power management state</td> </tr> <tr> <td>8h</td> <td>DEVSLP asserted</td> </tr> <tr> <td>All other values reserved.</td> <td></td> </tr> </tbody> </table>		Value	Description	0h	Device not present or communication not established	1h	Interface in active state	2h	Interface in PARTIAL power management state	6h	Interface in SLUMBER power management state	8h	DEVSLP asserted	All other values reserved.	
Value	Description															
0h	Device not present or communication not established															
1h	Interface in active state															
2h	Interface in PARTIAL power management state															
6h	Interface in SLUMBER power management state															
8h	DEVSLP asserted															
All other values reserved.																

Bit	Description													
7:4	<b>Current Interface Speed (SPD)</b> —RO. Indicates the negotiated interface communication speed. <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Device not present or communication not established</td> </tr> <tr> <td>1h</td> <td>Gen 1 communication rate negotiated</td> </tr> <tr> <td>2h</td> <td>Gen 2 communication rate negotiated</td> </tr> <tr> <td>3h</td> <td>Gen 3 communication rate negotiated</td> </tr> <tr> <td>All other values reserved.</td> <td></td> </tr> </tbody> </table> The PCH supports Gen 1 communication rates (1.5Gb/s), Gen 2 rates (3.0Gb/s) and Gen 3 rates (6.0Gb/s) (supported speeds are determined by SKU; see <a href="#">Section 2.3</a> )		Value	Description	0h	Device not present or communication not established	1h	Gen 1 communication rate negotiated	2h	Gen 2 communication rate negotiated	3h	Gen 3 communication rate negotiated	All other values reserved.	
Value	Description													
0h	Device not present or communication not established													
1h	Gen 1 communication rate negotiated													
2h	Gen 2 communication rate negotiated													
3h	Gen 3 communication rate negotiated													
All other values reserved.														
3:0	<b>Device Detection (DET)</b> —RO. Indicates the interface device detection and Phy state: <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No device detected and Phy communication not established</td> </tr> <tr> <td>1h</td> <td>Device presence detected but Phy communication not established</td> </tr> <tr> <td>3h</td> <td>Device presence detected and Phy communication established</td> </tr> <tr> <td>4h</td> <td>Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode</td> </tr> <tr> <td>All other values reserved.</td> <td></td> </tr> </tbody> </table> <b>Note:</b> While the true reset default value of this register is 0h, the value read from this register depends on drive presence and the point in time within the initialization process when the register is read. <b>Note:</b> The means by which the implementation determines device presence may be vendor specific. However, device presence shall always be indicated anytime a COMINIT signal is received.		Value	Description	0h	No device detected and Phy communication not established	1h	Device presence detected but Phy communication not established	3h	Device presence detected and Phy communication established	4h	Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode	All other values reserved.	
Value	Description													
0h	No device detected and Phy communication not established													
1h	Device presence detected but Phy communication not established													
3h	Device presence detected and Phy communication established													
4h	Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode													
All other values reserved.														

#### 11.4.2.11 PxSCTL—Port [3:0] Serial ATA Control Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 12Ch      Attribute: R/W  
 Port 1: ABAR + 1ACh  
 Port 2: ABAR + 22Ch  
 Port 3: ABAR + 2ACh

Default Value: 00000004h      Size: 32 bits

This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the PCH or the interface. Reads from the register return the last value written to it.

Bit	Description
31:20	Reserved
19:16	<b>Port Multiplier Port (PMP)</b> —R/W. This field is not used by AHCI
15:12	<b>Select Power Management (SPM)</b> —R/W. This field is not used by AHCI



Bit	Description																			
11:8	<p><b>Interface Power Management Transitions Allowed (IPM)</b>—R/W. Indicates which power states the PCH is allowed to transition to. If an interface power management state is not allowed by means of this register field, the HBA will not initiate that state and the HBA will PMNAK P any request from the device to enter that state.</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>No interface power management (PM) state restrictions</td></tr> <tr> <td>1h</td><td>Transitions to the PARTIAL state PM disabled</td></tr> <tr> <td>2h</td><td>Transitions to the SLUMBER state PM disabled</td></tr> <tr> <td>3h</td><td>Transitions to both PARTIAL and SLUMBER PM states disabled</td></tr> <tr> <td>4h</td><td>Transitions to DEVSLP power management PM state are disabled.</td></tr> <tr> <td>5h</td><td>Transitions to Partial and DEVSLP PM states are disabled.</td></tr> <tr> <td>6h</td><td>Transitions to Slumber and DEVSLP PM states are disabled.</td></tr> <tr> <td>7h</td><td>Transitions to Partial, Slumber and DEVSLP PM states are disabled.</td></tr> </tbody> </table> <p>All other values reserved</p>	Value	Description	0h	No interface power management (PM) state restrictions	1h	Transitions to the PARTIAL state PM disabled	2h	Transitions to the SLUMBER state PM disabled	3h	Transitions to both PARTIAL and SLUMBER PM states disabled	4h	Transitions to DEVSLP power management PM state are disabled.	5h	Transitions to Partial and DEVSLP PM states are disabled.	6h	Transitions to Slumber and DEVSLP PM states are disabled.	7h	Transitions to Partial, Slumber and DEVSLP PM states are disabled.	
Value	Description																			
0h	No interface power management (PM) state restrictions																			
1h	Transitions to the PARTIAL state PM disabled																			
2h	Transitions to the SLUMBER state PM disabled																			
3h	Transitions to both PARTIAL and SLUMBER PM states disabled																			
4h	Transitions to DEVSLP power management PM state are disabled.																			
5h	Transitions to Partial and DEVSLP PM states are disabled.																			
6h	Transitions to Slumber and DEVSLP PM states are disabled.																			
7h	Transitions to Partial, Slumber and DEVSLP PM states are disabled.																			
7:4	<p><b>Speed Allowed (SPD)</b>—R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field.</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>No speed negotiation restrictions</td></tr> <tr> <td>1h</td><td>Limit speed negotiation to Gen 1 communication rate</td></tr> <tr> <td>2h</td><td>Limit speed negotiation to Gen 2 communication rate</td></tr> <tr> <td>3h</td><td>Limit speed negotiation to Gen 3 communication rate</td></tr> </tbody> </table> <p>The PCH Supports Gen 1 communication rates (1.5Gb/s), Gen 2 rates (3.0Gb/s) and Gen 3 rates (6.0Gb/s) (supported speeds are determined by SKU; see <a href="#">Section 2.3</a>) If software changes SPD after port has been enabled, software is required to perform a port reset using DET=1h. This field shall remain 1h until set to another value by software.</p>	Value	Description	0h	No speed negotiation restrictions	1h	Limit speed negotiation to Gen 1 communication rate	2h	Limit speed negotiation to Gen 2 communication rate	3h	Limit speed negotiation to Gen 3 communication rate									
Value	Description																			
0h	No speed negotiation restrictions																			
1h	Limit speed negotiation to Gen 1 communication rate																			
2h	Limit speed negotiation to Gen 2 communication rate																			
3h	Limit speed negotiation to Gen 3 communication rate																			
3:0	<p><b>Device Detection Initialization (DET)</b>—R/W. Controls the PCH's device detection and interface initialization.</p> <table> <thead> <tr> <th>Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>No device detection or initialization action requested</td></tr> <tr> <td>1h</td><td>Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized</td></tr> <tr> <td>4h</td><td>Disable the Serial ATA interface and put Phy in offline mode</td></tr> </tbody> </table> <p>All other values reserved.</p> <p>When this field is written to a 1h, the PCH initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface.</p> <p>This field may only be changed when PxCMD.ST is 0. Changing this field while the PCH is running results in undefined behavior. When PxCMD.ST is set to „1”, this field should have a value of 0h.</p> <p><b>Note:</b> It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.</p>	Value	Description	0h	No device detection or initialization action requested	1h	Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized	4h	Disable the Serial ATA interface and put Phy in offline mode											
Value	Description																			
0h	No device detection or initialization action requested																			
1h	Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized																			
4h	Disable the Serial ATA interface and put Phy in offline mode																			

#### 11.4.2.12 PxSERR—Port [3:0] Serial ATA Error Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 130h      Attribute: R/WC  
 Port 1: ABAR + 1B0h  
 Port 2: ABAR + 230h  
 Port 3: ABAR + 2B0h

Default Value: 00000000h      Size: 32 bits

Bits 26:16 of this register contain diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

Bit	Description
31:27	Reserved
26	<b>Exchanged (X)</b> —R/WC. When set to 1, this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1 anytime a COMINIT signal is received. This bit is reflected in the PxIS.PCS bit.
25	<b>Unrecognized FIS Type (F)</b> —R/WC. Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.
24	<b>Transport state transition error (T)</b> —R/WC. Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	<b>Link Sequence Error (S)</b> —R/WC. Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition.
22	<b>Handshake (H)</b> —R/WC. Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	<b>CRC Error (C)</b> —R/WC. Indicates that one or more CRC errors occurred with the Link Layer.
20	<b>Disparity Error (D)</b> —R/WC. This field is not used by AHCI.
19	<b>10b to 8b Decode Error (B)</b> —R/WC. Indicates that one or more 10b to 8b decoding errors occurred.
18	<b>Comm Wake (W)</b> —R/WC. Indicates that a Comm Wake signal was detected by the Phy.
17	<b>Phy Internal Error (I)</b> —R/WC. Indicates that the Phy detected some internal error.
16	<b>PhyRdy Change (N)</b> —R/WC. When set to 1, this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the PCH, this bit will be set when PhyRdy changes from a 0 -> 1 or a 1 -> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a 1 to it.
15:12	Reserved
11	<b>Internal Error (E)</b> —R/WC. The SATA controller failed due to a master or target abort when attempting to access system memory.
10	<b>Protocol Error (P)</b> —R/WC. A violation of the Serial ATA protocol was detected. <b>Note:</b> The PCH does not set this bit for all protocol violations that may occur on the SATA link.
9	<b>Persistent Communication or Data Integrity Error (C)</b> —R/WC. A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.



Bit	Description
8	<b>Transient Data Integrity Error (T)</b> —R/WC. A data integrity error occurred that was not recovered by the interface.
7:2	Reserved.
1	<b>Recovered Communications Error (M)</b> —R/WC. Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	<b>Recovered Data Integrity Error (I)</b> —R/WC. A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

#### 11.4.2.13 PxSACT—Port [3:0] Serial ATA Active Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 134h      Attribute: R/W  
 Port 1: ABAR + 1B4h  
 Port 2: ABAR + 234h  
 Port 3: ABAR + 2B4h

Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Device Status (DS)</b> —R/W. System software sets this bit for SATA queuing operations prior to setting the PxCI.CI bit in the same command slot entry. This field is cleared using the Set Device Bits FIS. This field is also cleared when PxCMD.ST (ABAR+118h/198h/218h/298h:bit 0) is written from a '1' to a '0' by software. This field is not cleared by COMRESET or SRST.

#### 11.4.2.14 PxCI—Port [3:0] Command Issue Register (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 138h      Attribute: R/W  
 Port 1: ABAR + 1B8h  
 Port 2: ABAR + 238h  
 Port 3: ABAR + 2B8h

Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Commands Issued (CI)</b> —R/W. This field is set by software to indicate to the PCH that a command has been built-in system memory for a command slot and may be sent to the device. When the PCH receives a FIS that clears the BSY and DRQ bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when PxCMD.ST is set to 1. This field is also cleared when PxCMD.ST (ABAR+118h/198h/218h/298h:bit 0) is written from a '1' to a '0' by software.

#### 11.4.2.15 PxDEVSLP—Port [3:0] Device Sleep (D31:F2)

Registers may be Reserved depending on if port is available in the given SKU. See [Section 2.3](#) for details if port is available.

Address Offset: Port 0: ABAR + 144h  
Port 1: ABAR + 1C4h  
Port 2: ABAR + 244h  
Port 3: ABAR + 2C4h

Default Value: 00000000h  
Function Level Reset: No

Bit	Description
31:29	Reserved <b>Note:</b> These bits are not reset by controller reset
28:25	<b>DITO Multiplier (DM)</b> —R/WO. This field specifies the DITO multiplier that the HBA applies to the specific DITO value, effectively extending the range of DITO from 1 ms to 16368 ms. A value of 0 indicates a multiplier of 1. A maximum multiplier of 16 may be applied. The Host computes the total idle timeout as a product of DM and DITO (that is, DITO actual = DITO * (DM+1)). (These bits are not reset by controller reset)
24:15	<b>DEVSLEP Idle Timeout (DITO)</b> —RW, RO. This field specifies the amount of time (in approximate 1 ms granularity) that the SATA controller will wait before driving the DEVSLP signal. Hardware will reload the port specific DEVSLP timer with this value each time the port transitions out of the DEVSLP state. If CAP2.SDS or CAP2.SADM is cleared to '0', then these bits are RO 0h and software will treat these bits as reserved. Software will only set this value when PxCMD.ST is cleared to '0' and PxDEVSLP ADSE is cleared to '0'. (These bits are not reset by controller reset)
14:10	<b>DEVSLP Minimum Assertion Time (MDAT)</b> —RW, RO. This field specifies the minimum amount of time (in approximate 1 ms granularity) that the SATA controller will assert the DEVSLP signal before it may be de-asserted. The nominal value is 10 ms and the minimum is 1 ms depending on device identification information. If CAP2.SDS or CAP2.SADM is cleared to '0', then these bits are RO 0h and software will treat these bits as reserved. Software will only set this value when PxCMD.ST is cleared to '0' and PxDEVSLP ADSE is cleared to '0' prior to setting PxCMD.ICC to 8h. (These bits are not reset by controller reset)
9:2	<b>DEVSLP Exit Timeout (DETO)</b> —RW, RO. This field specifies the maximum duration (in approximate 1 ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20 ms and the maximum value is 255 ms depending on device identification information. If CAP2.SDS is cleared to '0', then these bits are RO 0h and software will treat these bits as reserved. Software will only set this value when PxCMD.ST is cleared to '0' and PxDEVSLP ADSE is cleared to '0' prior to setting PxCMD.ICC to 8h. (These bits are not reset by controller reset)
1	<b>DEVSLP Present (DSP)</b> —RW, RO. If set to '1', the platform supports DEVSLP on this port. If cleared to '0', the platform does not support DEVSLP on this port. This bit may only be set to '1' if CAP2.SDS is set to '1'. DSP is mutually exclusive with the PxCMD.HPCD bit and the PxCMD.ESP bit. BIOS is requested to program this field to '1' for offset 144h, 1C4h, 244h, and 2C4 which corresponds to PCH SATA Port 0, 1, 2, and 3. <b>Note:</b> These bits are not reset by controller reset
0	<b>Aggressive DEVSLP Enable (ADSE)</b> —RW, RO. This bit is R/W when aggressive DEVSLP management (CAP2.SADM = '1') is supported. This bit is RO when aggressive DEVSLP management is disabled (CAP2.SADM = '0') or CAP2.SDS is cleared to '0'. When this bit is set to '1', the SATA host will assert the DEVSLP signal after the port has been idle for the amount of time specified by the PxDEVSLP.DITO register and the interface is in Slumber. When this bit is cleared to '0', the host will not enter DEVSLP unless software directed by means of PxCMD.ICC. This bit will only be set to '1' if PxDEVSLP.DSP is set to '1'. If this bit is set to '1' and software clears the bit to '0', then the host will de-assert the DEVSLP signal if asserted. (These bits are not reset by controller reset)

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# 12 EHCI Controller Registers (D29:F0)

## 12.1 USB EHCI Configuration Registers (USB EHCI—D29:F0)

**Note:** Prior to BIOS initialization of the PCH USB subsystem, the EHCI controllers will appear as Function 7. After BIOS initialization, the EHCI controllers will be Function 0.

**Note:** Register address locations that are not shown in [Table 12-1](#) should be treated as Reserved (see [Section 7.2](#) for details).

**Table 12-1. USB EHCI PCI Register Address Map (USB EHCI—D29:F0) (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default Value	Attribute
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0290h	R/W, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	20h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	0Ch	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h–13h	MEM_BASE	Memory Base Address	00000000h	R/W, RO
2Ch–2Dh	SVID	USB EHCI Subsystem Vendor Identification	XXXXh	R/W, RWS
2Eh–2Fh	SID	USB EHCI Subsystem Identification	XXXXh	R/W, RWS
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
50h	PWR_CAPID	PCI Power Management Capability ID	01h	RO
51h	NXT_PTR1	Next Item Pointer	58h	R/W
52h–53h	PWR_CAP	Power Management Capabilities	C9C3h	R/W, RWS
54h–55h	PWR_CNTL_STS	Power Management Control/Status	0008h	R/W, R/WC, RO
58h	DEBUG_CAPID	Debug Port Capability ID	0Ah	RO
59h	NXT_PTR2	Next Item Pointer #2	98h	RO
5Ah–5Bh	DEBUG_BASE	Debug Port Base Offset	20A0h	RO
60h	USB_RELNUM	USB Release Number	20h	RO
61h	FL_ADJ	Frame Length Adjustment	20h	R/W, RO
62h–63h	PWAKE_CAP	Port Wake Capabilities	01FFh	R/W, RO
64h–67h	—	Reserved	—	—

**Table 12-1. USB EHCI PCI Register Address Map (USB EHCI—D29:F0) (Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default Value	Attribute
68h–6Bh	LEG_EXT_CAP	USB EHCI Legacy Support Extended Capability	00000001h	R/W, RO
6Ch–6Fh	LEG_EXT_CS	USB EHCI Legacy Extended Support Control/Status	00000000h	R/W, R/WC, RO
70h–73h	SPECIAL_SMI	Intel Specific USB 2.0 SMI	00000000h	R/W, R/WC
74h–77h	OCMAP	Overcurrent Mapping	C0300C03h	R/W
78h–7Dh	—	Reserved	—	—
7E–7Fh	RMHWKCTL	RMH Wake Control	0000h	R/W, RO
80h	ACCESS_CNTL	Access Control	00h	R/W, RO
84h–87h	EHCIIR1	EHCI Initialization Register 1	110C0811h	R/W, RO
98h	FLR_CID	Function Level Reset Capability ID	13h	RO
99h	FLR_NEXT	Function Level Reset Next Capability Pointer	00h	RO
9Ah–9Bh	FLR_CLV	Function Level Reset Capability Length and Version	306h	RO, R/WO
9Ch	FLR_CTRL	Function Level Reset Control	00h	R/W, RO
9Dh	FLR_STS	Function Level Reset Status	00h	RO

**Note:**

All configuration registers in this section are in the core well and reset by a core well reset and the D3-to-D0 warm reset, except as noted.

### 12.1.1 VID—Vendor Identification Register (USB EHCI—D29:F0)

Offset Address: 00h–01h	Attribute: RO
Default Value: 8086h	Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel.

### 12.1.2 DID—Device Identification Register (USB EHCI—D29:F0)

Offset Address: 02h–03h	Attribute: RO
Default Value: See bit description	Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH USB EHCI controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

### 12.1.3 PCICMD—PCI Command Register (USB EHCI—D29:F0)

Address Offset: 04h–05h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:11	Reserved. Read Only
10	<b>Interrupt Disable</b> —R/W 0 = The function is capable of generating interrupts. 1 = The function can not generate its interrupt to the interrupt controller. The corresponding Interrupt Status bit (D29:F0:06h, bit 3) is not affected by the interrupt enable.
9	Fast Back to Back Enable (FBE)—RO. Hardwired to 0.
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = Disables EHC's capability to generate an SERR#. 1 = The Enhanced Host controller (EHC) is capable of generating (internally) SERR# in the following cases: <ul style="list-style-type: none"><li>— When it receive a completion status other than "successful" for one of its DMA initiated memory reads on DMI (and subsequently on its internal interface).</li><li>— When it detects an address or command parity error and the Parity Error Response bit is set.</li><li>— When it detects a data parity error (when the data is going into the EHC) and the Parity Error Response bit is set.</li></ul>
7	<b>Wait Cycle Control (WCC)</b> —RO. Hardwired to 0.
6	<b>Parity Error Response (PER)</b> —R/W 0 = The EHC is not checking for correct parity (on its internal interface). 1 = The EHC is checking for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase.  <b>Note:</b> If the EHC detects bad parity on the address or command phases when the bit is set to 1, the host controller does not take the cycle. It halts the host controller (if currently not halted) and sets the Host System Error bit in the USBSTS register. This applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	<b>VGA Palette Snoop (VPS)</b> —RO. Hardwired to 0.
4	<b>Postable Memory Write Enable (PMWE)</b> —RO. Hardwired to 0.
3	<b>Special Cycle Enable (SCE)</b> —RO. Hardwired to 0.
2	<b>Bus Master Enable (BME)</b> —R/W 0 = Disables this functionality. 1 = Enables the PCH to act as a master on the PCI bus for USB transfers.
1	<b>Memory Space Enable (MSE)</b> —R/W. This bit controls access to the USB 2.0 Memory Space registers. 0 = Disables this functionality. 1 = Enables accesses to the USB 2.0 registers. The Base Address register (D29:F0:10h) for USB 2.0 should be programmed before this bit is set.
0	<b>I/O Space Enable (IOSE)</b> —RO. Hardwired to 0.

### 12.1.4 PCISTS—PCI Status Register (USB EHCI—D29:F0)

 Address Offset: 06h–07h  
 Default Value: 0290h

 Attribute: R/WC, RO  
 Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC 0 = No parity error detected. 1 = This bit is set by the PCH when a parity error is seen by the EHCI controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions.
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No SERR# signaled by the PCH. 1 = This bit is set by the PCH when it signals SERR# (internally). The SER_EN bit, bit 8 of the Command Register, must be 1 for this bit to be set.
13	<b>Received Master Abort (RMA)</b> —R/WC 0 = No master abort received by EHC on a memory access. 1 = This bit is set when EHC, as a master, receives a master abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate a SERR# by setting the SERR# Enable bit.
12	<b>Received Target Abort (RTA)</b> —R/WC 0 = No target abort received by EHC on memory access. 1 = This bit is set when EHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate a SERR# by setting the SERR# Enable bit (D29:F0:04h, bit 8).
11	<b>Signaled Target Abort (STA)</b> —RO. This bit is used to indicate when the EHCI function responds to a cycle with a target abort. There is no reason for this to happen; thus, this bit is hardwired to 0.
10:9	<b>DEVSEL# Timing Status (DEVT_STS)</b> —RO. This 2-bit field defines the timing for DEVSEL# assertion. Read Only
8	<b>Master Data Parity Error Detected (DPED)</b> —R/WC 0 = No data parity error detected on USB 2.0 read completion packet. 1 = This bit is set by the PCH when a data parity error is detected on a USB 2.0 read completion packet on the internal interface to the EHCI host controller and bit 6 of the Command register is set to 1.
7	<b>Fast Back to Back Capable (FB2BC)</b> —RO. Hardwired to 1.
6	<b>User Definable Features (UDF)</b> —RO. Hardwired to 0.
5	<b>66 MHz Capable (66 MHz _CAP)</b> —RO. Hardwired to 0.
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	<b>Interrupt Status</b> —RO. This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = This bit will be 0 when the interrupt is de-asserted. 1 = This bit is a 1 when the interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	Reserved

### 12.1.5 RID—Revision Identification Register (USB EHCI—D29:F0)

 Offset Address: 08h  
 Default Value: See bit description

 Attribute: RO  
 Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See Section 1.4 for the value of the RID Register.



### 12.1.6 PI—Programming Interface Register (USB EHCI—D29:F0)

Address Offset: 09h Attribute: RO  
 Default Value: 20h Size: 8 bits

Bit	Description
7:0	<b>Programming Interface</b> —RO. A value of 20h indicates that this USB 2.0 host controller conforms to the EHCI Specification.

### 12.1.7 SCC—Sub Class Code Register (USB EHCI—D29:F0)

Address Offset: 0Ah Attribute: RO  
 Default Value: 03h Size: 8 bits

Bit	Description
7:0	<b>Sub Class Code (SCC)</b> —RO 03h = Universal serial bus host controller.

### 12.1.8 BCC—Base Class Code Register (USB EHCI—D29:F0)

Address Offset: 0Bh Attribute: RO  
 Default Value: 0Ch Size: 8 bits

Bit	Description
7:0	<b>Base Class Code (BCC)</b> —RO 0Ch = Serial bus controller.

### 12.1.9 PMLT—Primary Master Latency Timer Register (USB EHCI—D29:F0)

Address Offset: 0Dh      Attribute: RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Master Latency Timer Count (MLTC)</b> —RO. Hardwired to 00h. Because the EHCI controller is internally implemented with arbitration on an interface (and not PCI), it does not need a master latency timer.

### 12.1.10 HEADTYP—Header Type Register (USB EHCI—D29:F0)

Address Offset: 0Eh      Attribute: RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7	<b>Multi-Function Device</b> —RO. When set to '1' indicates this is a multifunction device: 0 = Single-function device 1 = Multi-function device.
6:0	Configuration Layout. Hardwired to 00h, which indicates the standard PCI configuration layout.

### 12.1.11 MEM\_BASE—Memory Base Address Register (USB EHCI—D29:F0)

Address Offset: 10h–13h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:10	<b>Base Address</b> —R/W. Bits [31:10] correspond to memory address signals [31:10], respectively. This gives 1KB of locatable memory space aligned to 1KB boundaries.
9:4	Reserved
3	<b>Prefetchable</b> —RO. Hardwired to 0 indicating that this range should not be prefetched.
2:1	<b>Type</b> —RO. Hardwired to 00b indicating that this range can be mapped anywhere within 32-bit address space.
0	<b>Resource Type Indicator (RTE)</b> —RO. Hardwired to 0 indicating that the base address field in this register maps to memory space.



### 12.1.12 SVID—USB EHCI Subsystem Vendor Identification Register (USB EHCI—D29:F0)

Address Offset: 2Ch–2Dh      Attribute: R/W  
 Default Value: XXXXh      Size: 16 bits  
 Reset: None

Bit	Description
15:0	<p><b>Subsystem Vendor ID (SVID)</b>—R/W. This register, in combination with the USB 2.0 Subsystem ID register, enables the operating system to distinguish each subsystem from the others.</p> <p><b>Note:</b> Writes to this register are enabled when the WRT_RDONLY bit (D29:F0:80h, bit 0) is set to 1.</p>

### 12.1.13 SID—USB EHCI Subsystem Identification Register (USB EHCI—D29:F0)

Address Offset: 2Eh–2Fh      Attribute: R/W  
 Default Value: XXXXh      Size: 16 bits  
 Reset: None

Bit	Description
15:0	<p><b>Subsystem ID (SID)</b>—R/W. BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).</p> <p><b>Note:</b> Writes to this register are enabled when the WRT_RDONLY bit (D29:F0:80h, bit 0) is set to 1.</p>

### 12.1.14 CAP\_PTR—Capabilities Pointer Register (USB EHCI—D29:F0)

Address Offset: 34h      Attribute: RO  
 Default Value: 50h      Size: 8 bits

Bit	Description
7:0	<b>Capabilities Pointer (CAP_PTR)</b> —RO. This register points to the starting offset of the USB 2.0 capabilities ranges.

### 12.1.15 INT\_LN—Interrupt Line Register (USB EHCI—D29:F0)

Address Offset: 3Ch      Attribute: R/W  
 Default Value: 00h      Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.



### 12.1.16 INT\_PN—Interrupt Pin Register (USB EHCI—D29:F0)

Address Offset: 3Dh  
Default Value: See Description

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	<p><b>Interrupt Pin</b>—RO. This reflects the value of D29IP.E1IP (Chipset Configuration Registers:Offset 3108:bits 3:0).</p> <p><b>Note:</b> As a single function device, only INTA# may be used while the other three interrupt lines have no meaning. (Refer to PCI 3.0 specification—section 2.2.6 Interrupt Pins).</p> <p><b>Note:</b> Bits 7:4 are always 0h.</p>

## 12.1.17 PWR\_CAPID—PCI Power Management Capability ID Register (USB EHCI—D29:F0)

Address Offset: 50h  
Default Value: 01h

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	<b>Power Management Capability ID</b> —RO. A value of 01h indicates that this is a PCI Power Management capabilities field.

## 12.1.18 NXT\_PTR1—Next Item Pointer #1 Register (USB\_EHCI—D29:F0)

Address Offset: 51h  
Default Value: 58h

Attribute: R/W  
Size: 8 bits

Bit	Description
7:0	<p><b>Next Item Pointer 1 Value</b>—R/W (special). This register defaults to 58h indicating that the next capability registers begin at configuration offset 58h. This register is writable when the WRT_RDONLY bit (D29:F0:80h, bit 0) is set. This allows BIOS to effectively hide the Debug Port capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Only values of 58h (Debug Port and FLR capabilities visible) and 98h (Debug Port invisible, next capability is FLR) are expected to be programmed in this register.</p> <p><b>Note:</b> Register not reset by D3-to-D0 warm reset.</p>

### 12.1.19 PWR\_CAP—Power Management Capabilities Register (USB EHCI—D29:F0)

Address Offset: 52h–53h  
Default Value: C9C3h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:11	<b>PME Support (PME_SUP)</b> —R/W. This 5-bit field indicates the power states in which the function may assert PME#. The PCH EHC does not support the D1 or D2 states. For all other states, the PCH EHC is capable of generating PME#. Software should never need to modify this field.
10	<b>D2 Support (D2_SUP)</b> —RO 0 = D2 State is not supported
9	<b>D1 Support (D1_SUP)</b> —RO 0 = D1 State is not supported
8:6	<b>Auxiliary Current (AUX_CUR)</b> —R/W. The PCH EHC reports 375mA maximum suspend well current required when in the D3 <sub>COLD</sub> state.
5	<b>Device Specific Initialization (DSI)</b> —RO. The PCH reports 0, indicating that no device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PME_CLK)</b> —RO. The PCH reports 0, indicating that no 24-MHz clock is required to generate PME#.
2:0	<b>Version (VER)</b> —RO. The PCH reports 011b, indicating that it complies with Revision 1.2 of the PCI Power Management Specification.

**Notes:**

1. Normally, this register is read-only to report capabilities to the power management software. To report different power management capabilities, depending on the system in which the PCH is used, bits 15:11 and 8:6 in this register are writable when the WRT\_RDONLY bit (D29:F0:80h, bit 0) is set. The value written to this register does not affect the hardware other than changing the value returned during a read.
2. Reset: core well, but not D3-to-D0 warm reset.

## 12.1.20 PWR\_CNTL\_STS—Power Management Control/Status Register (USB EHCI—D29:F0)

Address Offset: 54h–55h Attribute: R/W, R/WC, RO  
 Default Value: 0008h Size: 16 bits  
 Function Level Reset: No (Bits 8 and 15 only)

Bit	Description
15	<p><b>PME Status</b>—R/WC            0 = Writing a 1 to this bit will clear it and cause the internal PME to de-assert (if enabled).            1 = This bit is set when the PCH EHC would normally assert the PME# signal independent of the state of the PME_En bit.</p> <p><b>Note:</b> This bit must be explicitly cleared by the operating system each time the operating system is loaded.            This bit is not reset by Function Level Reset.</p>
14:13	<b>Data Scale</b> —RO. Hardwired to 00b indicating it does not support the associated Data register.
12:9	<b>Data Select</b> —RO. Hardwired to 0000b indicating it does not support the associated Data register.
8	<p><b>PME Enable</b>—R/W            0 = Disable.            1 = Enables the PCH EHC to generate an internal PME signal when PME_Status is 1.</p> <p><b>Note:</b> This bit must be explicitly cleared by the operating system each time it is initially loaded.            This bit is not reset by Function Level Reset.</p>
7:4	Reserved
3	<p><b>No Soft Reset</b>—RW. This bit defines the behavior for D3<sub>HOT</sub> to D0 transition by means of software control of the power state bits.            This bit is protected by the Access Control Bit (80h)            0 = (Default) - EHCI does not do an internal reset upon D3<sub>HOT</sub> to D0            1 = (BIOS can update) - EHCI will do an internal reset upon D3<sub>HOT</sub> to D0 transition causing full context to be lost. A full initialization sequence is needed to return EHCI to D0</p>
2	Reserved
1:0	<p><b>Power State</b>—R/W. This 2-bit field is used both to determine the current power state of EHC function and to set a new power state. The definition of the field values are:            00 = D0 state            11 = D3<sub>HOT</sub> state            If software attempts to write a value of 10b or 01b in to this field, the write operation completes normally; however, the data is discarded and no state change occurs.            When in the D3<sub>HOT</sub> state, the PCH does not accept accesses to the EHC memory range; but the configuration space is still accessible. When not in the D0 state, the generation of the interrupt output is blocked. Specifically, the EHC interrupt is not asserted by the PCH when not in the D0 state.            When software changes this value from the D3<sub>HOT</sub> state to the D0 state, an internal warm (soft) controller reset is generated, and software must re-initialize the function.</p>

**Note:** Reset (bits 15, 8): suspend well, and not D3-to-D0 warm reset nor core well reset.



### 12.1.21 DEBUG\_CAPID—Debug Port Capability ID Register (USB EHCI—D29:F0)

Address Offset: 58h Attribute: RO  
Default Value: 0Ah Size: 8 bits

Bit	Description
7:0	<b>Debug Port Capability ID</b> —RO. Hardwired to 0Ah indicating that this is the start of a Debug Port Capability structure.

### 12.1.22 NXT\_PTR2—Next Item Pointer #2 Register (USB EHCI—D29:F0)

Address Offset: 59h Attribute: RO  
Default Value: 98h Size: 8 bits  
Function Level Reset: No

Bit	Description
7:0	<b>Next Item Pointer 2 Capability</b> —RO. This register points to the next capability in the Function Level Reset capability structure.

### 12.1.23 DEBUG\_BASE—Debug Port Base Offset Register (USB EHCI—D29:F0)

Address Offset: 5Ah–5Bh Attribute: RO  
Default Value: 20A0h Size: 16 bits

Bit	Description
15:13	<b>BAR Number</b> —RO. Hardwired to 001b to indicate the memory BAR begins at offset 10h in the EHCI configuration space.
12:0	<b>Debug Port Offset</b> —RO. Hardwired to 0A0h to indicate that the Debug Port registers begin at offset A0h in the EHCI memory range.

### 12.1.24 USB\_RELNUM—USB Release Number Register (USB EHCI—D29:F0)

Address Offset: 60h Attribute: RO  
Default Value: 20h Size: 8 bits

Bit	Description
7:0	<b>USB Release Number</b> —RO. A value of 20h indicates that this controller follows <i>Universal Serial Bus (USB) Specification</i> , Revision 2.0.

### 12.1.25 FL\_ADJ—Frame Length Adjustment Register (USB EHCI—D29:F0)

Address Offset: 61h Attribute: RO, R/W  
 Default Value: 20h Size: 8 bits  
 Function Level Reset: No

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit (D29:F0:CAPLENGTH + 24h, bit 12) in the USB2.0\_STS register is a 1. Changing value of this register while the host controller is operating yields undefined results. It should not be reprogrammed by USB system software unless the default or BIOS programmed values are incorrect, or the system is restoring the register while returning from a suspended state.

These bits are in suspend well and not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description																	
7:6	Reserved—RO. These bits are reserved for future use and should read as 00b.																	
5:0	<b>Frame Length Timing Value</b> —R/W. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h) that gives a SOF cycle time of 60000.	<b>Frame Length (# 480 MHz Clocks) (decimal)</b> <table> <tr><td>59488</td><td>0</td></tr> <tr><td>59504</td><td>1</td></tr> <tr><td>59520</td><td>2</td></tr> <tr><td>—</td><td>—</td></tr> <tr><td>59984</td><td>31</td></tr> <tr><td>60000</td><td>32</td></tr> <tr><td>—</td><td>—</td></tr> <tr><td>60480</td><td>62</td></tr> </table> <b>Frame Length Timing Value (this register) (decimal)</b>	59488	0	59504	1	59520	2	—	—	59984	31	60000	32	—	—	60480	62
59488	0																	
59504	1																	
59520	2																	
—	—																	
59984	31																	
60000	32																	
—	—																	
60480	62																	



### 12.1.26 PWAKE\_CAP—Port Wake Capability Register (USB EHCI—D29:F0)

Address Offset: 62–63h Attribute: R/W, RO  
 Default Value: 01FFh Size: 16 bits  
 Function Level Reset: No

This register is in the suspend power well. The intended use of this register is to establish a policy about which ports are to be used for wake events. Bit positions 1–10 in the mask correspond to a physical port implemented on the current EHCI controller. A, 1 in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect/connect or overcurrent events as wake-up events. This is an information-only mask register. The bits in this register **do not** affect the actual operation of the EHCI host controller. The system-specific policy can be established by BIOS initializing this register to a system-specific value. System software uses the information in this register when enabling devices and ports for remote wake-up.

These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
15:11	Reserved—RO
10:1	<b>Port Wake Up Capability Mask</b> —R/W. Bit positions 1–10 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 1, bit position 2 corresponds to port 2, and so on.
0	<b>Port Wake Implemented</b> —R/W. A, 1 in this bit indicates that this register is implemented to software.

### 12.1.27 LEG\_EXT\_CAP—USB EHCI Legacy Support Extended Capability Register (USB EHCI—D29:F0)

Address Offset: 68–6Bh Attribute: R/W, RO  
 Default Value: 00000001h Size: 32 bits  
 Power Well: Suspend  
 Function Level Reset: No

**Note:** These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31:25	Reserved—RO. Hardwired to 00h
24	<b>HC OS Owned Semaphore</b> —R/W. System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HC BIOS Owned Semaphore bit reads as clear.
23:17	Reserved—RO. Hardwired to 00h
16	<b>HC BIOS Owned Semaphore</b> —R/W. The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will clear this bit in response to a request for ownership of the EHCI controller by system software.
15:8	<b>Next EHCI Capability Pointer</b> —RO. Hardwired to 00h to indicate that there are no EHCI Extended Capability structures in this device.
7:0	<b>Capability ID</b> —RO. Hardwired to 01h to indicate that this EHCI Extended Capability is the Legacy Support Capability.

### 12.1.28 LEG\_EXT\_CS—USB EHCI Legacy Support Extended Control/Status Register (USB EHCI—D29:F0)

Address Offset: 6C-6Fh Attribute: R/W, R/WC, RO  
 Default Value: 00000000h Size: 32 bits  
 Power Well: Suspend  
 Function Level Reset: No

**Note:** These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31	<b>SMI on BAR</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = Base Address Register (BAR) not written. 1 = This bit is set to 1 when the Base Address Register (BAR) is written.
30	<b>SMI on PCI Command</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = PCI Command (PCICMD) Register Not written. 1 = This bit is set to 1 when the PCI Command (PCICMD) register is written.
29	<b>SMI on OS Ownership Change</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = No HC OS Owned Semaphore bit change. 1 = This bit is set to 1 when the HC operating system Owned Semaphore bit in the LEG_EXT_CAP register (D29:F0:68h, bit 24) transitions from 1 to 0 or 0 to 1.
28:22	Reserved
21	<b>SMI on Async Advance</b> —RO. This bit is a shadow bit of the Interrupt on Async Advance bit (D29:F0:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register.  <b>Note:</b> To clear this bit system software must write a 1 to the Interrupt on Async Advance bit in the USB2.0_STS register.
20	<b>SMI on Host System Error</b> —RO. This bit is a shadow bit of Host System Error bit in the USB2.0_STS register (D29:F0:CAPLENGTH + 24h, bit 4).  <b>Note:</b> To clear this bit system software must write a 1 to the Host System Error bit in the USB2.0_STS register.
19	<b>SMI on Frame List Rollover</b> —RO. This bit is a shadow bit of Frame List Rollover bit (D29:F0:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register.  <b>Note:</b> To clear this bit system software must write a 1 to the Frame List Rollover bit in the USB2.0_STS register.
18	<b>SMI on Port Change Detect</b> —RO. This bit is a shadow bit of Port Change Detect bit (D29:F0:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register.  <b>Note:</b> To clear this bit system software must write a 1 to the Port Change Detect bit in the USB2.0_STS register.
17	<b>SMI on USB Error</b> —RO. This bit is a shadow bit of USB Error Interrupt (USBERRINT) bit (D29:F0:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register.  <b>Note:</b> To clear this bit system software must write a 1 to the USB Error Interrupt bit in the USB2.0_STS register.
16	<b>SMI on USB Complete</b> —RO. This bit is a shadow bit of USB Interrupt (USBINT) bit (D29:F0:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register.  <b>Note:</b> To clear this bit system software must write a 1 to the USB Interrupt bit in the USB2.0_STS register.
15	<b>SMI on BAR Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is 1 and SMI on BAR (D29:F0:6Ch, bit 31) is 1, then the host controller will issue an SMI.



Bit	Description
14	<b>SMI on PCI Command Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is 1 and SMI on PCI Command (D29:F0:6Ch, bit 30) is 1, then the host controller will issue an SMI.
13	<b>SMI on OS Ownership Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1 AND the OS Ownership Change bit (D29:F0:6Ch, bit 29) is 1, the host controller will issue an SMI.
12:6	Reserved
5	<b>SMI on Async Advance Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Async Advance bit (D29:F0:6Ch, bit 21) is a 1, the host controller will issue an SMI immediately.
4	<b>SMI on Host System Error Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Host System Error (D29:F0:6Ch, bit 20) is a 1, the host controller will issue an SMI.
3	<b>SMI on Frame List Rollover Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Frame List Rollover bit (D29:F0:6Ch, bit 19) is a 1, the host controller will issue an SMI.
2	<b>SMI on Port Change Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on Port Change Detect bit (D29:F0:6Ch, bit 18) is a 1, the host controller will issue an SMI.
1	<b>SMI on USB Error Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on USB Error bit (D29:F0:6Ch, bit 17) is a 1, the host controller will issue an SMI immediately.
0	<b>SMI on USB Complete Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the SMI on USB Complete bit (D29:F0:6Ch, bit 16) is a 1, the host controller will issue an SMI immediately.

### 12.1.29 SPECIAL\_SMI—Intel Specific USB 2.0 SMI Register (USB EHCI—D29:F0)

Address Offset: 70h–73h Attribute: R/W, R/WC  
 Default Value: 00000000h Size: 32 bits  
 Power Well: Suspend  
 Function Level Reset: No

**Note:**

These bits are not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description
31:25	Reserved
24:22	<b>SMI on PortOwner</b> —R/WC. Software clears these bits by writing a 1 to it. 0 = No Port Owner bit change. 1 = Bits 24:22 correspond to the Port Owner bits for ports 0 (22) through 3 (24). These bits are set to 1 when the associated Port Owner bits transition from 0 to 1 or 1 to 0.
21	<b>SMI on PMCSR</b> —R/WC. Software clears these bits by writing a 1 to it. 0 = Power State bits Not modified. 1 = Software modified the Power State bits in the Power Management Control/Status (PMCSR) register (D29:F0:54h).
20	<b>SMI on Async</b> —R/WC. Software clears these bits by writing a 1 to it. 0 = No Async Schedule Enable bit change 1 = Async Schedule Enable bit transitioned from 1 to 0 or 0 to 1.
19	<b>SMI on Periodic</b> —R/WC. Software clears this bit by writing a 1 it. 0 = No Periodic Schedule Enable bit change. 1 = Periodic Schedule Enable bit transitions from 1 to 0 or 0 to 1.
18	<b>SMI on CF</b> —R/WC. Software clears this bit by writing a 1 it. 0 = No Configure Flag (CF) change. 1 = Configure Flag (CF) transitions from 1 to 0 or 0 to 1.
17	<b>SMI on HCHalted</b> —R/WC. Software clears this bit by writing a 1 it. 0 = HCHalted did Not transition to 1 (as a result of the Run/Stop bit being cleared). 1 = HCHalted transitions to 1 (as a result of the Run/Stop bit being cleared).
16	<b>SMI on HCReset</b> —R/WC. Software clears this bit by writing a 1 it. 0 = HCRESET did Not transitioned to 1. 1 = HCRESET transitioned to 1.
15:6	<b>SMI on PortOwner Enable</b> —R/W 0 = Disable. 1 = Enable. When any of these bits are 1 and the corresponding SMI on PortOwner bits are 1, then the host controller will issue an SMI. Unused ports should have their corresponding bits cleared.
5	<b>SMI on PMSCR Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is 1 and SMI on PMSCR is 1, then the host controller will issue an SMI.
4	<b>SMI on Async Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is 1 and SMI on Async is 1, then the host controller will issue an SMI
3	<b>SMI on Periodic Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is 1 and SMI on Periodic is 1, then the host controller will issue an SMI.



Bit	Description
2	<b>SMI on CF Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is 1 and SMI on CF is 1, then the host controller will issue an SMI.
1	<b>SMI on HCHalted Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1 and SMI on HCHalted is 1, then the host controller will issue an SMI.
0	<b>SMI on HCReset Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1 and SMI on HCReset is 1, then host controller will issue an SMI.

### 12.1.30 OCMAP—Overcurrent Mapping Register

Address Offset: 74-77h Attribute: R/W  
 Default Value: C0300C03h Size: 32 bits  
 Function Level Reset: No

Bit	Description																		
31:24	<b>OC Mapping 3</b> —R/W. Maps OC3 (EHCI 1) to a set of ports as follows: Map OC3 <table border="1" data-bbox="726 918 1199 1003"> <tr> <td>Bit:</td> <td>31</td> <td>30</td> <td>29</td> <td>28</td> <td>27</td> <td>26</td> <td>25</td> <td>24</td> </tr> <tr> <td>Port:</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> </table> <p>It is software responsibility to ensure that a given port's bit map is set only for one OC pin.</p>	Bit:	31	30	29	28	27	26	25	24	Port:	7	6	5	4	3	2	1	0
Bit:	31	30	29	28	27	26	25	24											
Port:	7	6	5	4	3	2	1	0											
23:16	<b>OC Mapping 2</b> —R/W. Maps OC2 to a set of ports as follows: Map OC2 <table border="1" data-bbox="726 1119 1199 1203"> <tr> <td>Bit:</td> <td>23</td> <td>22</td> <td>21</td> <td>20</td> <td>19</td> <td>18</td> <td>17</td> <td>16</td> </tr> <tr> <td>Port:</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> </table> <p>It is software responsibility to ensure that a given port's bit map is set only for one OC pin.</p>	Bit:	23	22	21	20	19	18	17	16	Port:	7	6	5	4	3	2	1	0
Bit:	23	22	21	20	19	18	17	16											
Port:	7	6	5	4	3	2	1	0											
15:8	<b>OC Mapping 1</b> —R/W. Maps OC1 to a set of ports as follows: Map OC1 <table border="1" data-bbox="726 1320 1199 1404"> <tr> <td>Bit:</td> <td>15</td> <td>14</td> <td>13</td> <td>12</td> <td>11</td> <td>10</td> <td>9</td> <td>8</td> </tr> <tr> <td>Port:</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> </table> <p>It is software responsibility to ensure that a given port's bit map is set only for one OC pin.</p>	Bit:	15	14	13	12	11	10	9	8	Port:	7	6	5	4	3	2	1	0
Bit:	15	14	13	12	11	10	9	8											
Port:	7	6	5	4	3	2	1	0											
7:0	<b>OC Mapping 0</b> —R/W. Maps OC0 to a set of ports as follows: Map OC0 <table border="1" data-bbox="726 1520 1199 1605"> <tr> <td>Bit:</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> <tr> <td>Port:</td> <td>7</td> <td>6</td> <td>5</td> <td>4</td> <td>3</td> <td>2</td> <td>1</td> <td>0</td> </tr> </table> <p>It is software responsibility to ensure that a given port's bit map is set only for one OC pin.</p>	Bit:	7	6	5	4	3	2	1	0	Port:	7	6	5	4	3	2	1	0
Bit:	7	6	5	4	3	2	1	0											
Port:	7	6	5	4	3	2	1	0											

### 12.1.31 RMHWKCTL—RMH Wake Control Register

Address Offset: 7Eh Attribute: R/W, RO  
 Default Value: 0000h Size: 16 bits  
 Function Level Reset: No

Bit	Description
15:9	Reserved
8	<b>RMH Inherit EHCI Wake Control Settings</b> —R/W 0 = Bits 2:0 of this register <b>DO NOT</b> reflect the appropriate bits of EHCI PORTSC0 Bits 22:20. 1 = Bits 2:0 of this register reflect the appropriate bits of EHCI PORTSC0 Bits 22:20.
7:4	Reserved
3	<b>RMH Upstream Wake on Device Resume Disable</b> —R/W 0 = The RMH will initiate a resume on its upstream port and cause a wake when a device resume occurs on an enabled downstream port 1 = The RMH will <b>NOT</b> initiate a resume on its upstream port and cause a wake when a device resume occurs on an enabled downstream port
2	<b>RMH Upstream Wake on OC Disable</b> —R/W 0 = The RMH will initiate a resume on its upstream port and cause a wake when an overcurrent condition occurs downstream port 1 = The RMH will <b>NOT</b> initiate a resume on its upstream port and cause a wake when an overcurrent condition occurs downstream port
1	<b>RMH Upstream Wake on Disconnect Disable</b> —R/W 0 = The RMH will initiate a resume on its upstream port and cause a wake when a disconnect event occurs on a downstream port 1 = The RMH will <b>NOT</b> initiate a resume on its upstream port and cause a wake when a disconnect event occurs on a downstream port
0	<b>RMH Upstream Wake on Connect Disable</b> —R/W 0 = The RMH will initiate a resume on its upstream port and cause a wake when a connect event occurs on a downstream port 1 = The RMH will <b>NOT</b> initiate a resume on its upstream port and cause a wake when a connect event occurs on a downstream port

### 12.1.32 ACCESS\_CNTL—Access Control Register (USB EHCI—D29:F0)

Address Offset: 80h Attribute: R/W  
 Default Value: 00h Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:1	Reserved
0	<b>WRT_RDONLY</b> —R/W. When set to 1, this bit enables a select group of normally read-only registers in the EHC function to be written by software. Registers that may only be written when this mode is entered are noted in the summary tables and detailed description as "Read/Write-Special". The registers fall into two categories: 1. System-configured parameters 2. Status bits

### 12.1.33 EHCIIR1—EHCI Initialization Register 1 (USB EHCI—D29:F0)

Address Offset: 84h Attribute: R/W, RO  
 Default Value: 110C0811h Size: 32 bits

Bit	Description
31:29	Reserved
28	<b>EHCI Prefetch Entry Clear</b> —R/W 0 = EHC will clear prefetched entries in DMA 1 = EHC will not clear prefetched entries in DMA (Default)
27:18	Reserved
17:11	Reserved
10:9	Reserved.
8:5	Reserved
4	<b>Intel® USB Prefetch Based Pause Enable</b> —R/W 0 = Intel® USB Prefetch Based Pause is disabled 1 = Intel® USB Prefetch Based Pause is enabled (Default)
3:0	Reserved

### 12.1.34 FLR\_CID—Function Level Reset Capability ID Register (USB EHCI—D29:F0)

Address Offset: 98h Attribute: RO  
 Default Value: 13h Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:0	<b>Capability ID</b> —RO 13h = Capability ID

### 12.1.35 FLR\_NEXT—Function Level Reset Next Capability Pointer Register (USB EHCI—D29:F0)

Address Offset: 99h Attribute: RO  
 Default Value: 00h Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:0	A value of 00h in this register indicates this is the last capability field.

### 12.1.36 FLR\_CLV—Function Level Reset Capability Length and Version Register (USB EHCI—D29:F0)

Address Offset: 9Ah–9Bh Attribute: R/WO, RO  
 Default Value: 0306h Size: 16 bits  
 Function Level Reset: No

When FLRCSSEL = 0, this register is defined as follows:

Bit	Description
15:10	Reserved
9	<b>FLR Capability</b> —R/WO 1 = Support for Function Level Reset (FLR).
8	<b>TXP Capability</b> —R/WO 1 = Support for Transactions Pending (TXP) bit. TXP must be supported if FLR is supported.
7:0	<b>Capability Length</b> —RO. This field indicates the # of bytes of this vendor specific capability as required by the PCI specification. It has the value of 06h for the FLR capability.



### 12.1.37 FLR\_CTRL—Function Level Reset Control Register (USB EHCI—D29:F0)

Address Offset: 9Ch Attribute: R/W  
 Default Value: 00h Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:1	Reserved
0	<b>Initiate FLR</b> —R/W. This bit is used to initiate FLR transition. A write of 1 initiates FLR transition. Since hardware must not respond to any cycles until FLR completion, the value read by software from this bit is always 0.

### 12.1.38 FLR\_STS—Function Level Reset Status Register (USB EHCI—D29:F0)

Address Offset: 9Dh Attribute: RO  
 Default Value: 00h Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:1	Reserved
0	<b>Transactions Pending (TXP)</b> —RO 0 = Completions for all non-posted requests have been received 1 = Controller has issued non-posted requests which have not been completed

## 12.2 Memory-Mapped I/O Registers

The EHCI memory-mapped I/O space is composed of two sets of registers—Capability Registers and Operational Registers.

**Note:** The PCH EHCI controller will not accept memory transactions (neither reads nor writes) as a target that are locked transactions. The locked transactions should not be forwarded to PCI as the address space is known to be allocated to USB.

**Note:** When the EHCI function is in the D3 PCI power state, accesses to the USB 2.0 memory range are ignored and result a master abort. Similarly, if the Memory Space Enable (MSE) bit is not set in the Command register in configuration space, the memory range will not be decoded by the PCH enhanced host controller (EHC). If the MSE bit is not set, the PCH must default to allowing any memory accesses for the range specified in the BAR to go to PCI. This is because the range may not be valid and, therefore, the cycle must be made available to any other targets that may be currently using that range.

## 12.2.1 Host Controller Capability Registers

These registers specify the limits, restrictions, and capabilities of the host controller implementation. Within the host controller capability registers, only the structural parameters register is writable. These registers are implemented in the suspend well and are only reset by the standard suspend-well hardware reset, not by HCRESET or the D3-to-D0 reset.

**Note:** The EHCI controller does not support as a target memory transactions that are locked transactions. Attempting to access the EHCI controller Memory-Mapped I/O space using locked memory transactions will result in undefined behavior.

**Note:** When the USB 2.0 function is in the D3 PCI power state, accesses to the USB 2.0 memory range are ignored and will result in a master abort. Similarly, if the Memory Space Enable (MSE) bit is not set in the Command register in configuration space, the memory range will not be decoded by the Enhanced Host Controller (EHC). If the MSE bit is not set, the EHC will not claim any memory accesses for the range specified in the BAR.

**Table 12-2. Enhanced Host Controller Capability Registers**

MEM_BASE + Offset	Mnemonic	Register	Default	Attribute
00h	CAPLENGTH	Capabilities Registers Length	20h	RO
02h-03h	HCIVERSION	Host Controller Interface Version Number	0100h	RO
04h-07h	HCSPARAMS	Host Controller Structural Parameters	00200008h	R/W (Special), RO
08h-0Bh	HCCPARAMS	Host Controller Capability Parameters	00036881h	RO

**Note:** "Read/Write Special" means that the register is normally read-only, but may be written when the WRT\_RDONLY bit is set. Because these registers are expected to be programmed by BIOS during initialization, their contents must not get modified by HCRESET or D3-to-D0 internal reset.

### 12.2.1.1 CAPLENGTH—Capability Registers Length Register

Offset: MEM\_BASE + 00h Attribute: RO  
 Default Value: 20h Size: 8 bits

Bit	Description
7:0	<b>Capability Register Length Value</b> —RO. This register is used as an offset to add to the Memory Base register (D29:F0:10h) to find the beginning of the Operational Register Space. This field is hardwired to 20h indicating that the Operation Registers begin at offset 20h.

### 12.2.1.2 HCIVERSION—Host Controller Interface Version Number Register

Offset: MEM\_BASE + 02h-03h Attribute: RO  
 Default Value: 0100h Size: 16 bits

Bit	Description
15:0	<b>Host Controller Interface Version Number</b> —RO. This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms.

### 12.2.1.3 HCSPARAMS—Host Controller Structural Parameters Register

Offset: MEM\_BASE + 04h-07h Attribute: R/W, RO  
 Default Value: 00200008h (D29:F0) Size: 32 bits  
 Function Level Reset: No

**Note:** This register is reset by a suspend well reset and not a D3-to-D0 reset or HCRESET.

Bit	Description
31:24	Reserved
23:20	<b>Debug Port Number (DP_N)</b> —RO. Hardwired to 2h indicating that the Debug Port is on the second lowest numbered port on the EHCI. EHCI#1: Port 1
19:16	Reserved
15:12	<b>Number of Companion Controllers (N_CC)</b> —RO. This field indicates the number of companion controllers associated with this USB EHCI host controller. There are no companion controllers, so this field is set to zero as a read-only bit.
11:8	<b>Number of Ports per Companion Controller (N_PCC)</b> —RO. This field indicates the number of ports supported per companion host controller. This field is 0h indication no other companion controller support.
7:4	Reserved. These bits are reserved and default to 0.
3:0	<b>N_PORTS</b> —R/W. This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 1h to Fh. A, 0 in this field is undefined. For Integrated USB 2.0 Rate Matching Hub Enabled: Each EHCI reports 2 ports by default. Port 0 is assigned to the RMH and port 1 is assigned as the debug port. When the KVM/USB-R feature is enabled, it will show up as Port 2 on the EHCI, and BIOS would need to update this field to 3h.

**Note:** This register is writable when the WRT\_RDONLY bit is set.

#### 12.2.1.4 HCCPARAMS—Host Controller Capability Parameters Register

Offset: MEM\_BASE + 08h–0Bh Attribute: R/W, RO  
 Default Value: 00036881h Size: 32 bits

Bit	Description
31:18	Reserved
17	<b>Asynchronous Schedule Update Capability (ASUC)</b> —R/W. This field is hardwired to 1b to indicate that the EHC hardware supports the Async Schedule prefetch enable bit in the USB2.0_CMD register.
16	<b>Periodic Schedule Update Capability (PSUC)</b> —R/W. This field is hardwired to 1b to indicate that the EHC hardware supports the Periodic Schedule Update Event Flag in the USB2.0_CMD register.
15:8	<b>EHCI Extended Capabilities Pointer (EECP)</b> —RO. This field is hardwired to 68h indicating that the EHCI capabilities list exists and begins at offset 68h in the PCI configuration space.
7:4	<b>Isochronous Scheduling Threshold</b> —R/W. This field indicates relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit 7 is 0, the value of the least significant 3 bits indicates the number of micro-fames a host controller holds, for a set of isochronous data structures (one or more), before flushing the state. When bit 7 is a 1, then host software assumes the host controller may cache an isochronous data structure for an entire frame. Refer to the EHCI specification for details on how software uses this information for scheduling isochronous transfers. This field is hardwired to 8h.
3	Reserved
2	<b>Asynchronous Schedule Park Capability</b> —RO. This bit is hardwired to 0 indicating that the host controller does not support this optional feature
1	<b>Programmable Frame List Flag</b> —RO. 0 = System software must use a frame list length of 1024 elements with this host controller. The USB2.0_CMD register (D29:F0:CAPLENGTH + 20h, bits 3:2) <i>Frame List Size</i> field is a read-only register and must be set to 0. 1 = System software can specify and use a smaller frame list and configure the host controller using the USB2.0_CMD register <i>Frame List Size</i> field. The frame list must always be aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
0	<b>64-bit Addressing Capability</b> —RO. This field documents the addressing range capability of this implementation. The value of this field determines whether software should use the 32-bit or 64-bit data structures. This bit is hardwired to 1. <b>Note:</b> The PCH supports 64-bit addressing only.



## 12.2.2 Host Controller Operational Registers

This section defines the enhanced host controller operational registers. These registers are located after the capabilities registers. The operational register base must be DWord-aligned and is calculated by adding the value in the first capabilities register (CAPLENGTH) to the base address of the enhanced host controller register address space (MEM\_BASE). Since CAPLENGTH is always 20h, [Table 12-3](#) already accounts for this offset. All registers are 32 bits in length.

**Table 12-3. Enhanced Host Controller Operational Register Address Map**

MEM_BASE + Offset	Mnemonic	Register Name	Default	Special Notes	Attribute
20h-23h	USB2.0_CMD	USB 2.0 Command	00080000h		R/W, RO
24h-27h	USB2.0_STS	USB 2.0 Status	00001000h		R/WC, RO
28h-2Bh	USB2.0_INTR	USB 2.0 Interrupt Enable	00000000h		R/W, RO
2Ch-2Fh	FRINDEX	USB 2.0 Frame Index	00000000h		R/W, RO
30h-33h	CTRLDSSEGMENT	Control Data Structure Segment	00000000h		R/W
34h-37h	PERIODICLISTBASE	Period Frame List Base Address	00000000h		R/W, RO
38h-3Bh	ASYNCLISTADDR	Current Asynchronous List Address	00000000h		R/W, RO
3Ch-5Fh	—	Reserved	0h		RO
60h-63h	CONFIGFLAG	Configure Flag	00000000h	Suspend	R/W, RO
64h-67h	PORT0SC	Port 0 Status and Control	00003000h	Suspend	R/W, R/WC, RO
68h-6Bh	PORT1SC	Port 1 Status and Control	00003000h	Suspend	R/W, R/WC, RO
6Ch-6Fh	PORT2SC	Port 2 Status and Control	00003000h	Suspend	R/W, R/WC, RO
70h-73h	PORT3SC	Port 3 Status and Control	00003000h	Suspend	R/W, R/WC, RO
74h-77h	PORT4SC	Port 4 Status and Control	00003000h	Suspend	R/W, R/WC, RO
78h-7Bh	PORT5SC	Port 5 Status and Control	00003000h	Suspend	R/W, R/WC, RO
7Ch-7Fh	PORT6SC	Port 6 Status and Control	00003000h	Suspend	R/W, R/WC, RO
80h-83h	PORT7SC	Port 7 Status and Control	00003000h	Suspend	R/W, R/WC, RO
7Ch-9Fh	—	Reserved	Undefined		RO
A0h-B3h	—	Debug Port Registers	Undefined		See register description
B4h-EFh	—	Reserved	Undefined		RO
F0h	RMHPORTSTS1	RMH Port1 Status Register	0h		RO
F1h	RMHPORTSTS2	RMH Port2 Status Register	0h		RO
F2h	RMHPORTSTS3	RMH Port3 Status Register	0h		RO
F3h	RMHPORTSTS4	RMH Port4 Status Register	0h		RO
F4h	RMHPORTSTS5	RMH Port5 Status Register	0h		RO
F5h	RMHPORTSTS6	RMH Port6 Status Register	0h		RO
F6h	RMHPORTSTS7	RMH Port7 Status Register	0h		RO
F7h	RMHPORTSTS8	RMH Port8 Status Register	0h		RO
F8h-3FFh	—	Reserved	Undefined		RO

**Note:**

Software must read and write these registers using only DWord accesses. These registers are divided into two sets. The first set at offsets MEM\_BASE + 00:3Bh are implemented in the core power well. Unless otherwise noted, the core well registers are reset by the assertion of any of the following:

- Core well hardware reset
- HCRESET
- D3-to-D0 reset

The second set at offsets MEM\_BASE + 60h to the end of the implemented register space are implemented in the Suspend power well. Unless otherwise noted, the suspend well registers are reset by the assertion of either of the following:

- Suspend well hardware reset
- HCRESET

### 12.2.2.1 **USB2.0\_CMD—USB 2.0 Command Register**

Offset: MEM\_BASE + 20-23h Attribute: R/W, RO  
 Default Value: 00080000h Size: 32 bits

Bit	Description																			
31:24	Reserved																			
23:16	<b>Interrupt Threshold Control</b> —R/W. System software uses this field to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. If software writes an invalid value to this register, the results are undefined. <table> <thead> <tr> <th>Value</th> <th>Maximum Interrupt Interval</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Reserved</td> </tr> <tr> <td>01h</td> <td>1 micro-frame</td> </tr> <tr> <td>02h</td> <td>2 micro-frames</td> </tr> <tr> <td>04h</td> <td>4 micro-frames</td> </tr> <tr> <td>08h</td> <td>8 micro-frames (default, equates to 1 ms)</td> </tr> <tr> <td>10h</td> <td>16 micro-frames (2 ms)</td> </tr> <tr> <td>20h</td> <td>32 micro-frames (4 ms)</td> </tr> <tr> <td>40h</td> <td>64 micro-frames (8 ms)</td> </tr> </tbody> </table>		Value	Maximum Interrupt Interval	00h	Reserved	01h	1 micro-frame	02h	2 micro-frames	04h	4 micro-frames	08h	8 micro-frames (default, equates to 1 ms)	10h	16 micro-frames (2 ms)	20h	32 micro-frames (4 ms)	40h	64 micro-frames (8 ms)
Value	Maximum Interrupt Interval																			
00h	Reserved																			
01h	1 micro-frame																			
02h	2 micro-frames																			
04h	4 micro-frames																			
08h	8 micro-frames (default, equates to 1 ms)																			
10h	16 micro-frames (2 ms)																			
20h	32 micro-frames (4 ms)																			
40h	64 micro-frames (8 ms)																			
15:14	Reserved																			
13	<b>Asynch Schedule Update (ASC)</b> —R/W. This bit is used by the EHCI Asynchronous schedule caching function when operating in C0 mode. It is ignored when Asynch caching operates in Cx mode. When this bit is set, it allows the asynch schedule to be cached. When cleared, it causes the cache to be disabled and all modified entries to be written back.																			
12	<b>Periodic Schedule Prefetch Enable</b> —R/W. This bit is used by software to enable the host controller to prefetch the periodic schedule even in C0. 0 = Prefetch based pause enabled only when not in C0. 1 = Prefetch based pause enable in C0. Once software has written a 1b to this bit to enable periodic schedule prefetching, it must disable prefetching by writing a 0b to this bit whenever periodic schedule updates are about to begin. Software should continue to dynamically disable and re-enable the prefetcher surrounding any updates to the periodic scheduler (that is, until the host controller has been reset using a HCRESET).																			
11:8	<b>Unimplemented Asynchronous Park Mode Bits</b> —RO. Hardwired to 000b indicating the host controller does not support this optional feature.																			
7	<b>Light Host Controller Reset</b> —RO. Hardwired to 0. The PCH does not implement this optional reset.																			
6	<b>Interrupt on Async Advance Doorbell</b> —R/W. This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. 0 = The host controller sets this bit to a 0 after it has set the Interrupt on Async Advance status bit (D29:F0:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register to a 1. 1 = Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USB2.0_STS register. If the <i>Interrupt on Async Advance Enable</i> bit in the USB2.0_INTR register (D29:F0:CAPLENGTH + 28h, bit 5) is a 1, then the host controller will assert an interrupt at the next interrupt threshold. See the EHCI specification for operational details. <b>Note:</b> Software should not write a 1 to this bit when the asynchronous schedule is inactive. Doing so will yield undefined results.																			



Bit	Description															
5	<b>Asynchronous Schedule Enable</b> —R/W. This bit controls whether the host controller skips processing the Asynchronous Schedule. 0 = Do not process the Asynchronous Schedule 1 = Use the ASYNCLISTADDR register to access the Asynchronous Schedule.															
4	<b>Periodic Schedule Enable</b> —R/W. This bit controls whether the host controller skips processing the Periodic Schedule. 0 = Do not process the Periodic Schedule 1 = Use the PERIODICLISTBASE register to access the Periodic Schedule.															
3:2	<b>Frame List Size</b> —RO, R/W. This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the frame list. 00b = 1024 elements (4096 bytes) (Default) 01b = 512 elements (2048 bytes) 10b = 256 elements (1024 bytes) for resource constrained environments.															
1	<b>Host Controller Reset (HCRESET)</b> —R/W. This control bit is used by software to reset the host controller. The effects of this on root hub registers are similar to a Chip Hardware Reset (that is, RSMRST# assertion and PWROK de-assertion on the PCH). When software writes a 1 to this bit, the host controller resets its internal pipelines, timers, counters, state machines, and so on to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. <b>Note:</b> PCI configuration registers and Host controller capability registers are not effected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s), with the side effects described in the EHCI specification. Software must re-initialize the host controller in order to return the host controller to an operational state. This bit is set to 0 by the host controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0 to this register bit. Software should not set this bit to a 1 when the HCHalted bit (D29:F0:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register is a 0. Attempting to reset an actively running host controller will result in undefined behavior. This reset may be used to leave EHCI port test modes.															
0	<b>Run/Stop (RS)</b> —R/W 0 = Stop (default) 1 = Run. When set to a 1, the Host controller proceeds with execution of the schedule. The Host controller continues execution as long as this bit is set. When this bit is set to 0, the Host controller completes the current transaction on the USB and then halts. The HCHalted bit in the USB2.0_STS register indicates when the Host controller has finished the transaction and has entered the stopped state. Software should not write a 1 to this field unless the host controller is in the Halted state (that is, HCHalted in the USBSTS register is a 1). The Halted bit is cleared immediately when the Run bit is set. The following table explains how the different combinations of Run and Halted should be interpreted.  <table> <thead> <tr> <th>Run/Stop</th> <th>Halted</th> <th>Interpretation</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>0b</td> <td>In the process of halting</td> </tr> <tr> <td>0b</td> <td>1b</td> <td>Halted</td> </tr> <tr> <td>1b</td> <td>0b</td> <td>Running</td> </tr> <tr> <td>1b</td> <td>1b</td> <td>Invalid – the HCHalted bit clears immediately</td> </tr> </tbody> </table> Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being cleared.	Run/Stop	Halted	Interpretation	0b	0b	In the process of halting	0b	1b	Halted	1b	0b	Running	1b	1b	Invalid – the HCHalted bit clears immediately
Run/Stop	Halted	Interpretation														
0b	0b	In the process of halting														
0b	1b	Halted														
1b	0b	Running														
1b	1b	Invalid – the HCHalted bit clears immediately														

**Note:** The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

### 12.2.2.2 USB2.0\_STS—USB 2.0 Status Register

Offset: MEM\_BASE + 24h-27h Attribute: R/WC, RO  
 Default Value: 00001000h Size: 32 bits

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the EHCI specification for additional information concerning USB 2.0 interrupt conditions.

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Bit	Description
31:16	Reserved
15	<b>Asynchronous Schedule Status</b> —RO. This bit reports the current real status of the Asynchronous Schedule. 0 = Disabled. (Default) 1 = Enabled. <b>Note:</b> The Host controller is not required to <i>immediately</i> disable or enable the Asynchronous Schedule when software transitions the <i>Asynchronous Schedule Enable</i> bit (D29:F0:CAPLENGTH + 20h, bit 5) in the USB2.0_CMD register. When this bit and the <i>Asynchronous Schedule Enable</i> bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	<b>Periodic Schedule Status</b> —RO. This bit reports the current real status of the Periodic Schedule. 0 = Disabled. (Default) 1 = Enabled. <b>Note:</b> The Host controller is not required to <i>immediately</i> disable or enable the Periodic Schedule when software transitions the <i>Periodic Schedule Enable</i> bit (D29:F0:CAPLENGTH + 20h, bit 4) in the USB2.0_CMD register. When this bit and the <i>Periodic Schedule Enable</i> bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	<b>Reclamation</b> —RO. This read-only status bit is used to detect an empty asynchronous schedule. The operational model and valid transitions for this bit are described in Section 4 of the EHCI Specification.
12	<b>HCHalted</b> —RO 0 = This bit is a 0 when the Run/Stop bit is a 1. 1 = The Host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host controller hardware (such as, internal error). (Default)
11:6	Reserved
5	<b>Interrupt on Async Advance</b> —R/WC. System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a 1 to the <i>Interrupt on Async Advance Doorbell</i> bit (D29:F0:CAPLENGTH + 20h, bit 6) in the USB2.0_CMD register. This bit indicates the assertion of that interrupt source.
4	<b>Host System Error</b> —R/WC 0 = No serious error occurred during a host system access involving the Host controller module. 1 = The Host controller sets this bit to 1 when a serious error occurs during a host system access involving the Host controller module. A hardware interrupt is generated to the system. Memory read cycles initiated by the EHC that receive any status other than Successful will result in this bit being set.  When this error occurs, the Host controller clears the Run/Stop bit in the USB2.0_CMD register (D29:F0:CAPLENGTH + 20h, bit 0) to prevent further execution of the scheduled TDs. A hardware interrupt is generated to the system (if enabled in the Interrupt Enable register).
3	<b>Frame List Rollover</b> —R/WC 0 = No <i>Frame List Index</i> rollover from its maximum value to 0. 1 = The Host controller sets this bit to a 1 when the <i>Frame List Index</i> rolls over from its maximum value to 0. Since the PCH only supports the 1024-entry Frame List Size, the <i>Frame List Index</i> rolls over every time FRNUM13 toggles.



Bit	Description
2	<b>Port Change Detect</b> —R/WC. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3-to-D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/disable change, and connect status change). Regardless of the implementation, when this bit is readable (that is, in the D0 state), it must provide a valid view of the Port Status registers. 0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0-to-1 as a result of a J-K transition detected on a suspended port. 1 = The Host controller sets this bit to 1 when any port for which the <i>Port Owner</i> bit is set to 0 has a change bit transition from 0-to-1 or a Force Port Resume bit transition from 0-to-1 as a result of a J-K transition detected on a suspended port.
1	<b>USB Error Interrupt (USBERRINT)</b> —R/WC 0 = No error condition. 1 = The Host controller sets this bit to 1 when completion of a USB transaction results in an error condition (such as, error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and Bit 0 are set. See the EHCI specification for a list of the USB errors that will result in this interrupt being asserted.
0	<b>USB Interrupt (USBINT)</b> —R/WC 0 = No completion of a USB transaction whose Transfer Descriptor had its IOC bit set. No short packet is detected. 1 = The Host controller sets this bit to 1 when the cause of an interrupt is a completion of a USB transaction whose Transfer Descriptor had its IOC bit set. The Host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).

### 12.2.2.3 USB2.0\_INTR—USB 2.0 Interrupt Enable Register

Offset: MEM\_BASE + 28h-2Bh Attribute: R/W, RO  
Default Value: 00000000h Size: 32 bits

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USB2.0\_STS register to allow the software to poll for events. Each interrupt enable bit description indicates whether it is dependent on the interrupt threshold mechanism (see Section 4 of the EHCI specification), or not.

Bit	Description
31:6	Reserved
5	<b>Interrupt on Async Advance Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the Interrupt on Async Advance bit (D29:F0:CAPLENGTH + 24h, bit 5) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	<b>Host System Error Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the Host System Error Status bit (D29:F0:CAPLENGTH + 24h, bit 4) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	<b>Frame List Rollover Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the Frame List Rollover bit (D29:F0:CAPLENGTH + 24h, bit 3) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	<b>Port Change Interrupt Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the Port Change Detect bit (D29:F0:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is a 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.

Bit	Description
1	<b>USB Error Interrupt Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the USBERRINT bit (D29:F0:CAPLENGTH + 24h, bit 1) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBERRINT bit in the USB2.0_STS register.
0	<b>USB Interrupt Enable</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, and the USBINT bit (D29:F0:CAPLENGTH + 24h, bit 0) in the USB2.0_STS register is a 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software by clearing the USBINT bit in the USB2.0_STS register.

#### 12.2.2.4 FRINDEX—Frame Index Register

Offset: MEM\_BASE + 2Ch–2Fh Attribute: R/W, RO  
 Default Value: 00000000h Size: 32 bits

The SOF frame number value for the bus SOF token is derived or alternatively managed from this register. Refer to Section 4 of the EHCI specification for a detailed explanation of the SOF value management requirements on the host controller. The value of FRINDEX must be within 125  $\mu$ s (1 micro-frame) ahead of the SOF token value. The SOF value may be implemented as an 11-bit shadow register. For this discussion, this shadow register is 11 bits and is named SOFV. SOFV updates every 8 micro-frames (1 millisecond). An example implementation to achieve this behavior is to increment SOFV each time the FRINDEX[2:0] increments from 0 to 1.

Software must use the value of FRINDEX to derive the current micro-frame number, both for high-speed isochronous scheduling purposes and to provide the **get** micro-frame number function required to client drivers. Therefore, the value of FRINDEX and the value of SOFV must be kept consistent if the chip is reset or software writes to FRINDEX. Writes to FRINDEX must also **write-through** FRINDEX[13:3] to SOFV[10:0]. In order to keep the update as simple as possible, software should never write a FRINDEX value where the three least significant bits are 111b or 000b.

**Note:**

This register is used by the host controller to index into the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits 12:3 are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index is fixed at 10 for the PCH since it only supports 1024-entry frame lists. This register must be written as a DWord. Word and Byte writes produce undefined results. This register cannot be written unless the Host controller is in the Halted state as indicated by the *HCHalted* bit. A write to this register while the Run/Stop bit is set to a 1 (USB2.0\_CMD register) produces undefined results. Writes to this register also effects the SOF value. See Section 4 of the EHCI specification for details.

Bit	Description
31:14	Reserved
13:0	<b>Frame List Current Index/Frame Number</b> —R/W. The value in this register increments at the end of each time frame (such as, micro-frame). Bits 12:3 are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index.



### 12.2.2.5 CTRLDSEGMENT—Control Data Structure Segment Register

Offset: MEM\_BASE + 30h-33h Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

This 32-bit register corresponds to the most significant address bits 63:32 for all EHCI data structures. Since the PCH hardwires the 64-bit Addressing Capability field in HCCPARAMS to 1, this register is used with the link pointers to construct 64-bit addresses to EHCI control data structures. This register is concatenated with the link pointer from either the PERIODICLISTBASE, ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address. This register allows the host software to locate all control data structures within the same 4GB memory segment.

Bit	Description
31:0	<b>Upper Address[63:32]</b> —R/W. This 12-bit field corresponds to address bits 63:32 when forming a control data structure address.

### 12.2.2.6 PERIODICLISTBASE—Periodic Frame List Base Address Register

Offset: MEM\_BASE + 34h-37h Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

This 32-bit register contains the beginning address of the Periodic Frame List in the system memory. Since the PCH host controller operates in 64-bit mode (as indicated by the 1 in the 64-bit Addressing Capability field in the HCCSPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSEGMENT register. HCD loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host controller to step through the Periodic Frame List in sequence.

Bit	Description
31:12	<b>Base Address (Low)</b> —R/W. These bits correspond to memory address signals 31:12, respectively.
11:0	Reserved

### 12.2.2.7 ASYNCLISTADDR—Current Asynchronous List Address Register

Offset: MEM\_BASE + 38h-3Bh Attribute: R/W, RO  
 Default Value: 00000000h Size: 32 bits

This 32-bit register contains the address of the next asynchronous queue head to be executed. Since the PCH host controller operates in 64-bit mode (as indicated by a 1 in 64-bit Addressing Capability field in the HCCPARAMS register) (offset 08h, bit 0), then the most significant 32 bits of every control data structure address comes from the CTRLDSSEGMENT register (offset 08h). Bits 4:0 of this register cannot be modified by system software and will always return 0s when read. The memory structure referenced by this physical memory pointer is assumed to be 32-byte aligned.

Bit	Description
31:5	<b>Link Pointer Low (LPL)</b> —R/W. These bits correspond to memory address signals 31:5, respectively. This field may only reference a Queue Head (QH).
4:0	Reserved

### 12.2.2.8 CONFIGFLAG—Configure Flag Register

Offset: MEM\_BASE + 60h-63h Attribute: R/W, RO  
 Default Value: 00000000h Size: 32 bits

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

Bit	Description
31:1	Reserved
0	<b>Configure Flag (CF)</b> —R/W. Host software sets this bit as the last action in its process of configuring the Host controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. See Chapter 4 of the EHCI specification for operation details. 0 = Compatibility debug only (default). 1 = Port routing control logic default-routes all ports to this host controller.

### 12.2.2.9 PORTSC—Port N Status and Control Register

Offset: Port 0 RMH: MEM\_BASE + 64h-67h  
 Port 1 Debug Port: MEM\_BASE + 68-6Bh  
 Port 2 USB redirect (if enabled): MEM\_BASE + 6C-6Fh

Attribute: R/W, R/WC, RO  
 Default Value: 00003000h Size: 32 bits

**Note:** This register is associated with the upstream ports of the EHCI controller and does not represent downstream hub ports. USB Hub class commands must be used to determine RMH port status and enable test modes. See Chapter 11 of the USB Specification, Revision 2.0 for more details. Rate Matching Hub wake capabilities can be configured by the RMHWKCTL Register (RCBA+35B0h) located in the Chipset Configuration chapter.

A host controller must implement one or more port registers. Software uses the N\_Port information from the Structural Parameters register to determine how many ports need to be serviced. All ports have the structure defined below. Software must not write to unreported Port Status and Control registers.



This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No device connected
- Port disabled.

When a device is attached, the port state transitions to the attached state and system software will process this as with any status change notification. Refer to Section 4 of the EHCI specification for operational requirements for how change events interact with port suspend mode.

Bit	Description														
31:23	Reserved														
22	<b>Wake on Overcurrent Enable (WKOC_E)</b> —R/W 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status register (offset 54, bit 15) when the overcurrent Active bit—bit 4 of this register—is set.														
21	<b>Wake on Disconnect Enable (WKDSCNNT_E)</b> —R/W 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status register (offset 54, bit 15) when the Current Connect Status changes from connected to disconnected (that is, bit 0 of this register changes from 1 to 0).														
20	<b>Wake on Connect Enable (WKCNNT_E)</b> —R/W 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1 enables the setting of the PME Status bit in the Power Management Control/Status register (offset 54, bit 15) when the Current Connect Status changes from disconnected to connected (that is, bit 0 of this register changes from 0 to 1).														
19:16	<b>Port Test Control</b> —R/W. When this field is 0s, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b – 1111b are reserved):  <table> <thead> <tr> <th>Value</th> <th>Maximum Interrupt Interval</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Test mode not enabled (default)</td> </tr> <tr> <td>0001b</td> <td>Test J_STATE</td> </tr> <tr> <td>0010b</td> <td>Test K_STATE</td> </tr> <tr> <td>0011b</td> <td>Test SE0_NAK</td> </tr> <tr> <td>0100b</td> <td>Test Packet</td> </tr> <tr> <td>0101b</td> <td>FORCE_ENABLE</td> </tr> </tbody> </table> Refer to the USB Specification Revision 2.0, Chapter 7 for details on each test mode.	Value	Maximum Interrupt Interval	0000b	Test mode not enabled (default)	0001b	Test J_STATE	0010b	Test K_STATE	0011b	Test SE0_NAK	0100b	Test Packet	0101b	FORCE_ENABLE
Value	Maximum Interrupt Interval														
0000b	Test mode not enabled (default)														
0001b	Test J_STATE														
0010b	Test K_STATE														
0011b	Test SE0_NAK														
0100b	Test Packet														
0101b	FORCE_ENABLE														
15:14	Reserved														
13	<b>Port Owner</b> —R/W. This bit unconditionally goes to a 0 when the Configured Flag bit in the USB2.0_CMD register makes a 0-to-1 transition. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a 1 to this bit when the attached device is not a high-speed device. A 1 in this bit means that a companion host controller owns and controls the port. See Section 4 of the EHCI Specification for operational details.														
12	<b>Port Power (PP)</b> —RO. Read-only with a value of 1. This indicates that the port does have power.														
11:10	<b>Line Status</b> —RO. These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is 0 and the current connect status bit is set to a 1. 00 = SE0 10 = J-state 01 = K-state 11 = Undefined														
9	Reserved														

Bit	Description														
8	<p><b>Port Reset</b>—R/W. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0.</p> <p>1 = Port is in Reset. 0 = Port is not in Reset.</p> <p><b>Note:</b> When software writes a 0 to this bit, there may be a delay before the bit status changes to a 0. The bit status will not read as a 0 until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (such as, set the <i>Port Enable</i> bit to a 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from 0 to 1.</p> <p>For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2 ms of software writing this bit to a 0. The HCHalted bit (D29:F0:CAPLENGTH + 24h, bit 12) in the USB2.0_STS register should be a 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a 1. This bit is 0 if Port Power is 0.</p> <p><b>Note:</b> System software should not attempt to reset a port if the <i>HCHalted</i> bit in the USB2.0_STS register is a 1. Doing so will result in undefined behavior.</p>														
7	<p><b>Suspend</b>—R/W</p> <p>0 = Port not in suspend state.(Default) 1 = Port in suspend state.</p> <p>Port Enabled Bit and Suspend bit of this register define the port states as follows:</p> <table> <thead> <tr> <th>Port Enabled</th> <th>Suspend</th> <th>Port State</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>Disabled</td> </tr> <tr> <td>1</td> <td>0</td> <td>Enabled</td> </tr> <tr> <td>1</td> <td>1</td> <td>Suspend</td> </tr> </tbody> </table> <p>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The bit status does not change until the port is suspended and that there may be a delay in suspending a port depending on the activity on the port.</p> <p>The host controller will unconditionally set this bit to a 0 when software sets the <i>Force Port Resume</i> bit to a 0 (from a 1). A write of 0 to this bit is ignored by the host controller.</p> <p>If host software sets this bit to a 1 when the port is not enabled (that is, Port enabled bit is a 0), the results are undefined.</p>			Port Enabled	Suspend	Port State	0	X	Disabled	1	0	Enabled	1	1	Suspend
Port Enabled	Suspend	Port State													
0	X	Disabled													
1	0	Enabled													
1	1	Suspend													
6	<p><b>Force Port Resume</b>—R/W</p> <p>0 = No resume (K-state) detected/driven on port. (Default) 1 = Resume detected/driven on port. Software sets this bit to a 1 to drive resume signaling. The Host controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the Port Change Detect bit (D29:F0:CAPLENGTH + 24h, bit 2) in the USB2.0_STS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the Port Change Detect bit.</p> <p><b>Note:</b> When the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification, Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a 1. Software must appropriately time the Resume and set this bit to a 0 when the appropriate amount of time has elapsed. Writing a 0 (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to the high-speed idle.</p>														
5	<p><b>Overcurrent Change</b>—R/WC. The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it.</p> <p>0 = No change. (Default) 1 = There is a change to Overcurrent Active.</p>														
4	<p><b>Overcurrent Active</b>—R/O</p> <p>0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.</p>														
3	<p><b>Port Enable/Disable Change</b>—R/WC. For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a port error). This bit is not set due to the Disabled-to-Enabled transition, nor due to a disconnect. Software clears this bit by writing a 1 to it.</p> <p>0 = No change in status. (Default). 1 = Port enabled/disabled status has changed.</p>														



Bit	Description
2	<b>Port Enabled/Disabled</b> —R/W. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable 1 = Enable (Default)
1	<b>Connect Status Change</b> —R/WC. This bit indicates a change has occurred in the port's Current Connect Status. Software sets this bit to 0 by writing a 1 to it. 0 = No change (Default). 1 = Change in Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit (that is, the bit will remain set).
0	<b>Current Connect Status</b> —RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

#### 12.2.2.10 RMHPORTTSN—RMH Port N Status Register

Offset: Port 0 RMH: MEM\_BASE + F0h  
 Port 1 Debug Port: MEM\_BASE + F1h  
 Port 2 USB redirect (if enabled): MEM\_BASE + F2h  
 Port 3 MEM\_BASE + F3h  
 Port 4 MEM\_BASE + F4h  
 Port 5 MEM\_BASE + F5h  
 Port 6 MEM\_BASE + F6h  
 Port 7 MEM\_BASE + F7h

Attribute: RO  
 Default Value: 0h Size: 8 bits

**Note:** This register should only be used by BIOS to determine entry into Deep Sx from S3.

Bit	Description
7:5	Reserved
4	<b>Current Connection Status</b> —RO Indicates connection status of port.
3	<b>Port Enabled/Disabled</b> —RO. Indicates if the corresponding port is enabled.
2	<b>Over Current Status</b> —RO. Set to 1 if a corresponding OC# pin is asserted.
1	<b>Selective Port Resume</b> —RO. Set to 1 for the duration of a port resume.
0	<b>Selective Port Suspend</b> —RO. Set to 1 when the corresponding port is Suspended.

## 12.2.3 USB 2.0 Based Debug Port Registers

The Debug port's registers are located in the same memory area, defined by the Base Address register (MEM\_BASE), as the standard EHCI registers. The base offset for the debug port registers (A0h) is declared in the Debug Port Base Offset Capability register at Configuration offset 5Ah. The specific EHCI port that supports this debug capability (Port 1 for D29:F0) is indicated by a 4-bit field (bits 20–23) in the HCSPARMS register of the EHCI controller. The address map of the Debug Port registers is shown in [Table 12-4](#).

**Table 12-4. Debug Port Register Address Map**

MEM_BASE + Offset	Mnemonic	Register Name	Default	Attribute
A0-A3h	CNTL_STS	Control/Status	00000000h	R/W, R/WC, RO
A4-A7h	USBPID	USB PIDs	00000000h	R/W, RO
A8-AFh	DATABUF[7:0]	Data Buffer (Bytes 7:0)	00000000 00000000h	R/W
B0-B3h	CONFIG	Configuration	00007F01h	R/W, RO

**Notes:**

1. All of these registers are implemented in the core well and reset by PLTRST#, EHC HCRESET, and a EHC D3-to-D0 transition.
2. The hardware associated with this register provides no checks to ensure that software programs the interface correctly. How the hardware behaves when programmed improperly is undefined.

### 12.2.3.1 CNTL\_STS—Control/Status Register

Offset: MEM\_BASE + A0h      Attribute: R/W, R/WC, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31	Reserved
30	<b>OWNER_CNT</b> —R/W 0 = Ownership of the debug port is NOT forced to the EHCI controller (Default) 1 = Ownership of the debug port is forced to the EHCI controller (that is, immediately taken away from the companion Classic USB Host controller). If the port was already owned by the EHCI controller, then setting this bit has no effect. This bit overrides all of the ownership-related bits in the standard EHCI registers.
29	Reserved
28	<b>ENABLED_CNT</b> —R/W 0 = Software can clear this by writing a 0 to it. The hardware clears this bit for the same conditions where the Port Enable/Disable Change bit (in the PORTSC register) is set. (Default) 1 = Debug port is enabled for operation. Software can directly set this bit if the port is already enabled in the associated PORTSC register (this is enforced by the hardware).
27:17	Reserved
16	<b>DONE_STS</b> —R/WC. Software can clear this by writing a 1 to it. 0 = Request Not complete 1 = Set by hardware to indicate that the request is complete.
15:12	<b>LINK_ID_STS</b> —RO. This field identifies the link interface. 0h = Hardwired. Indicates that it is a USB Debug Port.
11	Reserved
10	<b>IN_USE_CNT</b> —R/W. Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software. This bit is cleared after reset. (This bit has no affect on hardware.)

Bit	Description
9:7	<b>EXCEPTION_STS</b> —RO. This field indicates the exception when the ERROR_GOOD#_STS bit is set. This field should be ignored if the ERROR_GOOD#_STS bit is 0. 000 = No Error. (Default) <b>Note:</b> This should not be seen since this field should only be checked if there is an error. 001 = Transaction error: Indicates the USB 2.0 transaction had an error (CRC, bad PID, timeout, and so on) 010 = Hardware error. Request was attempted (or in progress) when port was suspended or reset. All Other combinations are reserved
6	<b>ERROR_GOOD#_STS</b> —RO 0 = Hardware clears this bit to 0 after the proper completion of a read or write. (Default) 1 = Error has occurred. Details on the nature of the error are provided in the Exception field.
5	<b>GO_CNT</b> —R/W 0 = Hardware clears this bit when hardware sets the DONE_STS bit. (Default) 1 = Causes hardware to perform a read or write request. <b>Note:</b> Writing a 1 to this bit when it is already set may result in undefined behavior.
4	<b>WRITE_READ#_CNT</b> —R/W. Software clears this bit to indicate that the current request is a read. Software sets this bit to indicate that the current request is a write. 0 = Read (Default) 1 = Write
3:0	<b>DATA_LEN_CNT</b> —R/W. This field is used to indicate the size of the data to be transferred. default = 0h. For write operations, this field is set by software to indicate to the hardware how many bytes of data in the Data Buffer are to be transferred to the console. A value of 0h indicates that a zero-length packet should be sent. A value of 1–8 indicates 1–8 bytes are to be transferred. Values 9–Fh are invalid and how hardware behaves if used is undefined. For read operations, this field is set by hardware to indicate to software how many bytes in the Data Buffer are valid in response to a read operation. A value of 0h indicates that a zero length packet was returned and the state of the Data Buffer is not defined. A value of 1–8 indicates 1–8 bytes were received. Hardware is not allowed to return values 9–Fh. The transferring of data always starts with byte 0 in the data area and moves toward byte 7 until the transfer size is reached.

**Notes:**

1. Software should do Read-Modify-Write operations to this register to preserve the contents of bits not being modified. This includes Reserved bits.
2. To preserve the usage of RESERVED bits in the future, software should always write the same value read from the bit until it is defined. Reserved bits will always return 0 when read.

### 12.2.3.2 USBPID—USB PIDs Register

Offset: MEM\_BASE + A4h–A7h Attribute: R/W, RO  
 Default Value: 00000000h Size: 32 bits

This DWord register is used to communicate PID information between the USB debug driver and the USB debug port. The debug port uses some of these fields to generate USB packets, and uses other fields to return PID information to the USB debug driver.

Bit	Description
31:24	Reserved
23:16	<b>RECEIVED_PID_STS[23:16]</b> —RO. Hardware updates this field with the received PID for transactions in either direction. When the controller is writing data, this field is updated with the handshake PID that is received from the device. When the host controller is reading data, this field is updated with the data packet PID (if the device sent data), or the handshake PID (if the device NAKs the request). This field is valid when the hardware clears the GO_DONE#_CNT bit.
15:8	<b>SEND_PID_CNT[15:8]</b> —R/W. Hardware sends this PID to begin the data packet when sending data to USB (that is, WRITE_READ#_CNT is asserted). Software typically sets this field to either DATA0 or DATA1 PID values.
7:0	<b>TOKEN_PID_CNT[7:0]</b> —R/W. Hardware sends this PID as the Token PID for each USB transaction. Software typically sets this field to either IN, OUT, or SETUP PID values.

### 12.2.3.3 DATABUF[7:0]—Data Buffer Bytes [7:0] Register

Offset: MEM\_BASE + A8h–AFh Attribute: R/W  
 Default Value: 0000000000000000h Size: 64 bits

This register can be accessed as 8 separate, 8-bit registers or 2 separate, 32-bit registers.

Bit	Description
63:0	<b>DATABUFFER[63:0]</b> —R/W. This field is the 8 bytes of the data buffer. Bits 7:0 correspond to the least significant byte—byte 0. Bits 63:56 correspond to the most significant byte—byte 7. The bytes in the Data Buffer must be written with data before software initiates a write request. For a read request, the Data Buffer contains valid data when the DONE_STS bit (offset A0, bit 16) is cleared by the hardware, ERROR_GOOD#_STS (offset A0, bit 6) is cleared by the hardware, and the DATA_LENGTH_CNT field (offset A0, bits 3:0) indicates the number of bytes that are valid.

### 12.2.3.4 CONFIG—Configuration Register

Offset: MEM\_BASE + B0–B3h Attribute: R/W, RO  
 Default Value: 00007F01h Size: 32 bits

Bit	Description
31:15	Reserved
14:8	<b>USB_ADDRESS_CNF</b> —R/W. This 7-bit field identifies the USB device address used by the controller for all Token PID generation. (Default = 7Fh)
7:4	Reserved
3:0	<b>USB_ENDPOINT_CNF</b> —R/W. This 4-bit field identifies the endpoint used by the controller for all Token PID generation. (Default = 1h)

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# 13 xHCI Controller Registers (D20:F0)

## 13.1 USB xHCI Configuration Registers (USB xHCI—D20:F0)

**Note:** Register address locations that are not shown in Table 13-1 should be treated as Reserved (see Section 7.2 for details).

**Table 13-1. USB xHCI PCI Register Address Map (USB xHCI—D20:F0) (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default Value	Attribute
00h-01h	VID	Vendor Identification	8086h	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	0290h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	30h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	0Ch	RO
0Dh	PMLT	Primary Master Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h-17h	MEM_BASE	Memory Base Address	00000004h	R/W, RO
2Ch-2Dh	SVID	USB xHCI Subsystem Vendor Identification	0000h	R/W
2Eh-2Fh	SID	USB xHCI Subsystem Identification	0000h	R/W
34h	CAP_PTR	Capabilities Pointer	70h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	00h	RO
40h-43h	XHCC	xHC System Bus Configuration	0000F0FDh	R/W, R/WC
44h-47h	XHCC2	xHC System Bus Configuration 2	00000000h	R/WO, RO
60h	SBRN	Serial Bus Release Number	30h	RO
61h	FL_ADJ	Frame Length Adjustment	20h	R/W
70h	PWR_CAPID	PCI Power Management Capability ID	01h	RO
71h	NXT_PTR1	Next Item Pointer #1	80h	R/W
72h-73h	PWR_CAP	Power Management Capabilities	C9C2h	R/W, RO
74h-75h	PWR_CNTL_STS	Power Management Control/ Status	0008h	R/W, R/WC, RO
80h	MSI_CAPID	Message Signaled Interrupt Capability ID	05h	RO

**Table 13-1. USB xHCI PCI Register Address Map (USB xHCI—D20:F0)  
(Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default Value	Attribute
81h	NXT_PTR2	Next Item Pointer #2	00h	RO
82h-83h	MSI_MCTL	MSI Message Control Register	86h	RO, R/W
84h-87h	MSI_LMAD	MSI Lower Message Address	00000000h	R/W, RO
88h-8Bh	MSI_UMAD	MSI Upper Message Address	000000h	R/W
8Ch-8Fh	MSI_MD	MSI Message Data	00000000h	R/W
B0h-B3h, B4h-B7h, B8h-BBh, BCh-BFh	U2OCMx	xHCI USB 2.0 Overcurrent Pin Mapping x	00000000h	R/W, RO
C0h-C3h, C4h-C7h, C8h-CBh, CCh-CFh	U3OCMx	xHCI USB 3.0 Overcurrent Pin Mapping x	00000000h	R/W, RO
D0h-D3h	XUSB2PR	xHC USB 2.0 Port Routing	00000000h	R/W, RO
D4h-D7h	XUSB2PRM	xHC USB 2.0 Port Routing Mask	00000000h	RO, R/WL
D8h-DBh	USB3PR	USB3 Port Routing	00000000h	R/W, RO
DCh-DFh	USB3PRM	USB3 Port Routing Mask	00000000h	R/WL, RO

### 13.1.1 VID—Vendor Identification Register (USB xHCI—D20:F0)

Offset Address: 00h-01h Attribute: RO  
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel.

### 13.1.2 DID—Device Identification Register (USB xHCI—D20:F0)

Offset Address: 02h-03h Attribute: RO  
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH USB xHCI controller. Refer to Section 1.4 for the value of the Device ID Register.

### 13.1.3 PCICMD—PCI Command Register (USB xHCI—D20:F0)

Address Offset: 04h–05h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable (R/W)</b> 0 = The function is capable of generating interrupts. 1 = The function can not generate its interrupt to the interrupt controller. The corresponding Interrupt Status bit (D20:F0, Offset 06h, bit 3) is not affected by the interrupt enable.
9	<b>Fast Back to Back Enable (FBE)</b> —RO. Hardwired to 0.
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = Disables xHC's capability to generate an SERR#. 1 = The xHCI Host controller (xHC) is capable of generating (internally) SERR# in the following cases: <ul style="list-style-type: none"><li>– When it receive a completion status other than "successful" for one of its DMA initiated memory reads on DMI (and subsequently on its internal interface).</li><li>– When it detects an address or command parity error and the Parity Error Response bit is set.</li><li>– When it detects a data parity error (when the data is going into the xHC) and the Parity Error Response bit is set.</li></ul>
7	<b>Wait Cycle Control (WCC)</b> —RO. Hardwired to 0.
6	<b>Parity Error Response (PER)</b> —R/W 0 = The xHC is not checking for correct parity (on its internal interface). 1 = The xHC is checking for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase.  <b>Note:</b> This applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.
5	<b>VGA Palette Snoop (VPS)</b> —RO. Hardwired to 0.
4	<b>Postable Memory Write Enable (PMWE)</b> —RO. Hardwired to 0.
3	<b>Special Cycle Enable (SCE)</b> —RO. Hardwired to 0.
2	<b>Bus Master Enable (BME)</b> —R/W 0 = Disables this functionality. 1 = Enables the xHC to act as a master on the PCI bus for USB transfers.
1	<b>Memory Space Enable (MSE)</b> —R/W. This bit controls access to the xHC Memory Space registers. 0 = Disables this functionality. 1 = Enables accesses to the xHC Memory Space registers. The Base Address register (D20:F0:10h) should be programmed before this bit is set.
0	<b>I/O Space Enable (IOSE)</b> —RO. Hardwired to 0.

### 13.1.4 PCISTS—PCI Status Register (USB xHCI—D20:F0)

Address Offset: 06h–07h  
Default Value: 0290h

Attribute: R/WC, RO  
Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC 0 = No parity error detected. 1 = This bit is set by the PCH when a parity error is seen by the xHCI controller, regardless of the setting of bit 6 or bit 8 in the Command register or any other conditions.
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No SERR# signaled by the PCH. 1 = This bit is set by the PCH when it signals SERR# (internally). The SER_EN bit—bit 8 of the Command Register must be 1 for this bit to be set.
13	<b>Received Master Abort (RMA)</b> —R/WC. 0 = No master abort received by xHC on a memory access. 1 = This bit is set when xHC, as a master, receives a master abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit.
12	<b>Received Target Abort (RTA)</b> —R/WC. 0 = No target abort received by xHC on memory access. 1 = This bit is set when xHC, as a master, receives a target abort status on a memory access. This is treated as a Host Error and halts the DMA engines. This event can optionally generate an SERR# by setting the SERR# Enable bit.
11	<b>Signaled Target Abort (STA)</b> —RO. This bit is used to indicate when the xHCI function responds to a cycle with a target abort. There is no reason for this to happen, so this bit is hardwired to 0.
10:9	<b>DEVSEL# Timing Status (DEVT_STS)</b> —RO. This 2-bit field defines the timing for DEVSEL# assertion.
8	<b>Master Data Parity Error Detected (DPED)</b> —R/WC 0 = No data parity error detected on USB read completion packet. 1 = This bit is set by the PCH when a data parity error is detected on a xHC read completion packet on the internal interface to the xHCI host controller and bit 6 of the Command register is set to 1.
7	<b>Fast Back to Back Capable (FB2BC)</b> —RO. Hardwired to 1.
6	<b>User Definable Features (UDF)</b> —RO. Hardwired to 0.
5	<b>66 MHz Capable (66 MHz _CAP)</b> —RO. Hardwired to 0.
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 1 indicating that offset 34h contains a valid capabilities pointer.
3	<b>Interrupt Status</b> —RO. This bit reflects the state of this function's interrupt at the input of the enable/disable logic. 0 = This bit will be 0 when the interrupt is de-asserted. 1 = This bit is a 1 when the interrupt is asserted. The value reported in this bit is independent of the value in the Interrupt Enable bit.
2:0	Reserved

### 13.1.5 RID—Revision Identification Register (USB xHCI—D20:F0)

Offset Address: 08h  
Default Value: See bit description

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. Refer to Section 1.4 for the value of the Revision ID Register

### 13.1.6 PI—Programming Interface Register (USB xHCI—D20:F0)

Address Offset: 09h Attribute: RO  
 Default Value: 30h Size: 8 bits

Bit	Description
7:0	<b>Programming Interface</b> —RO. A value of 30h indicates that this USB host controller conforms to the xHCI Specification.

### 13.1.7 SCC—Sub Class Code Register (USB xHCI—D20:F0)

Address Offset: 0Ah Attribute: RO  
 Default Value: 03h Size: 8 bits

Bit	Description
7:0	<b>Sub Class Code (SCC)</b> —RO 03h = Universal Serial Bus host controller.

### 13.1.8 BCC—Base Class Code Register (USB xHCI—D20:F0)

Address Offset: 0Bh Attribute: RO  
 Default Value: 0Ch Size: 8 bits

Bit	Description
7:0	<b>Base Class Code (BCC)</b> —RO 0Ch = Serial bus controller.

### 13.1.9 PMLT—Primary Master Latency Timer Register (USB xHCI—D20:F0)

Address Offset: 0Dh Attribute: RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Master Latency Timer Count (MLTC)</b> —RO. Hardwired to 00h. Because the xHCI controller is internally implemented with arbitration on an interface (and not PCI), it does not need a master latency timer.

### 13.1.10 HEADTYP—Header Type Register (USB xHCI—D20:F0)

Address Offset: 0Eh Attribute: RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7	<b>Multi-Function Device</b> —RO. When set to '1' indicates this is a multifunction device: 0 = Single-function device 1 = Multi-function device.
6:0	Configuration Layout. Hardwired to 00h, which indicates the standard PCI configuration layout.

### 13.1.11 MEM\_BASE—Memory Base Address Register (USB xHCI—D20:F0)

Address Offset: 10h–17h      Attribute: R/W, RO  
 Default Value: 00000004h      Size: 64 bits

Bit	Description
63:16	<b>Base Address</b> —R/W. Bits [63:16] correspond to memory address signals [63:16], respectively. This gives 64KB of relocatable memory space aligned to 64KB boundaries.
15:4	Reserved
3	<b>Prefetchable</b> —RO. Hardwired to 0 indicating that this range should not be prefetched.
2:1	<b>Type</b> —RO. Hardwired to 10 indicating that this range can be mapped anywhere within 64-bit address space.
0	<b>Resource Type Indicator (RTE)</b> —RO. Hardwired to 0 indicating that the base address field in this register maps to memory space.

### 13.1.12 SVID—USB xHCI Subsystem Vendor ID Register (USB xHCI—D20:F0)

Address Offset: 2Ch–2Dh      Attribute: R/W  
 Default Value: XXXXh      Size: 16 bits  
 Reset: None

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —R/W. This register, in combination with the xHC Subsystem ID register, enables the operating system to distinguish each subsystem from the others.

### 13.1.13 SID—USB xHCI Subsystem ID Register (USB xHCI—D20:F0)

Address Offset: 2Eh–2Fh      Attribute: R/W  
 Default Value: XXXXh      Size: 16 bits  
 Reset: None

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —R/W. BIOS sets the value in this register to identify the Subsystem ID. This register, in combination with the Subsystem Vendor ID register, enables the operating system to distinguish each subsystem from other(s).

### 13.1.14 CAP\_PTR—Capabilities Pointer Register (USB xHCI—D20:F0)

Address Offset: 34h      Attribute: RO  
 Default Value: 70h      Size: 8 bits

Bit	Description
7:0	<b>Capabilities Pointer (CAP_PTR)</b> —RO. This register points to the starting offset of the xHC capabilities ranges.

### 13.1.15 INT\_LN—Interrupt Line Register (USB xHCI—D20:F0)

Address Offset: 3Ch Attribute: R/W  
 Default Value: 00h Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is used as a scratchpad register to communicate to software the interrupt line that the interrupt pin is connected to.

### 13.1.16 INT\_PN—Interrupt Pin Register (USB xHCI—D20:F0)

Address Offset: 3Dh Attribute: RO  
 Default Value: See Description Size: 8 bits

Bit	Description
7:0	<b>Interrupt Pin</b> —RO. Bits 3:0 reflect the value of the interrupt pin registers in Chipset configuration space. Bits 7:4 are always 0h

### 13.1.17 XHCC—xHC System Bus Configuration Register (USB xHCI—D20:F0)

Address Offset: 40-43h Attribute: R/W, R/WO, R/WC  
 Default Value: 0000F0FDh Size: 32 bits

Bit	Description
31:25	Reserved
24	<b>Master/Target Abort SERR (RMTASERR)</b> —R/W. When set, this bit allows the out-of-band error reporting from the xHCI Controller to be reported as SERR# (if SERR# reporting is enabled) and thus setting the STS.SSE bit.
23	<b>Unsupported Request Detected (URD)</b> —R/WC. This bit is set by hardware when the xHCI Controller received an unsupported request posted cycle. Once set, this bit is cleared by software.
22	<b>Unsupported Request Report Enable (URRE)</b> —R/W. When set, this bit allows the URD bit to be reported as SERR# (if SERR# reporting is enabled) and thus setting the STS.SSE bit.
21:19	<b>Inactivity Initiated L1 Enable (IIL1E)</b> —R/W. If programmed to a non-zero value, the bit field allows L1 power management to be enabled after the Timeout period specified. 000 = Disabled 001 = 32 bb_cclk 010 = 64 bb_cclk 011 = 128 bb_cclk 100 = 256 bb_cclk 101 = 512 bb_cclk 110 = 1024 bb_cclk 111 = 131072 bb_cclk
18	<b>xHC Initiated L1 Enable (xHCIL1E)</b> —R/W. 0 = xHC-initiated L1 power management is disabled 1 = Allows xHC-initiated L1 power management to be enabled
17	<b>D3 Initiated L1 Enable (D3IL1E)</b> —R/W. 0 = PCI device state D3-initiated L1 power management is disabled 1 = Allows PCI device state D3-initiated L1 power management to be enabled
16:0	Reserved

### 13.1.18 XHCC2—xHC System Bus Configuration Register 2 (USB xHCI—D20:F0)

Address Offset: 44-47h  
Default Value: 00000000h

Attribute: R/WO, RO  
Size: 32 bits

Bit	Description
31	<b>OC Configuration Done (OCCFDONE)</b> —R/WO. This bit is used by BIOS to prevent spurious switching during OC configuration. <b>Note:</b> This bit must be set by BIOS after configuration of the OC mapping bits is complete. Once this bit is set, OC mapping shall not be changed by software.
30:0	Reserved

### 13.1.19 SBRN—Serial Bus Release Number Register (USB xHCI—D20:F0)

Address Offset: 60h  
Default Value: 30h

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	<b>Serial Bus Release Number (SBRN)</b> —RO. A value of 30h indicates that this controller follows USB release 3.0.

### 13.1.20 FL\_ADJ—Frame Length Adjustment Register (USB xHCI—D20:F0)

Address Offset: 61h Attribute: R/W, RO  
 Default Value: 20h Size: 8 bits  
 Function Level Reset: No

This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. When a new value is written into these six bits, the length of the frame is adjusted. Its initial programmed value is system dependent based on the accuracy of hardware USB clock and is initialized by system BIOS. This register should only be modified when the HChalted bit (D20:F0:CAPLENGTH + 84h, bit 0) in the USB\_STS register is a 1. Changing value of this register while the host controller is operating yields undefined results. It should not be reprogrammed by USB system software unless the default or BIOS programmed values are incorrect, or the system is restoring the register while returning from a suspended state.

These bits are in suspend well and not reset by a D3-to-D0 warm rest or a core well reset.

Bit	Description	
7:6	Reserved—RO. These bits are reserved for future use and should read as 00b.	
5:0	<b>Frame Length Timing Value</b> —R/W. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length) is equal to 59488 + value in this field. The default value is decimal 32 (20h), which gives a SOF cycle time of 60000.	
	<b>Frame Length</b> (# 480 MHz Clocks) (Decimal)	<b>Frame Length Timing Value</b> (This Register) (Decimal)
	59488	0
	59504	1
	59520	2
	...	...
	59984	31
	...	...
	60496	63
	60480	62

### 13.1.21 PWR\_CAPID—PCI Power Management Capability ID Register (USB xHCI—D20:F0)

Address Offset: 70h Attribute: RO  
 Default Value: 01h Size: 8 bits

Bit	Description	
7:0	<b>Power Management Capability ID</b> —RO. A value of 01h indicates that this is a PCI Power Management capabilities field.	

### 13.1.22 NXT\_PTR1—Next Item Pointer #1 Register (USB xHCI—D20:F0)

Address Offset: 71h  
Default Value: 80h

Attribute: R/W  
Size: 8 bits

Bit	Description
7:0	<b>Next Item Pointer 1 Value</b> —R/W (special). This register defaults to 80h, which indicates that the next capability registers begin at configuration offset 80h. This register is writable when the ACCTRL bit (D20:F0:40h, bit 31) is '0'. This allows BIOS to effectively hide the next capability registers, if necessary. This register should only be written during system initialization before the plug-and-play software has enabled any master-initiated traffic. Values of 80h implies the next capability is MSI. Values of 00h implies that the MSI capability is hidden.

### 13.1.23 PWR\_CAP—Power Management Capabilities Register (USB xHCI—D20:F0)

Address Offset: 72h–73h  
Default Value: C9C2h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:11	<b>PME Support (PME_SUP)</b> —R/W. This 5-bit field indicates the power states in which the function may assert PME#. The PCH xHC does not support the D1 or D2 states. For all other states, the PCH xHC is capable of generating PME#. Software should never need to modify this field.
10	<b>D2 Support (D2_SUP)</b> —RO. 0 = D2 State is not supported
9	<b>D1 Support (D1_SUP)</b> —RO. 0 = D1 State is not supported
8:6	<b>Auxiliary Current (AUX_CUR)</b> —R/W. The PCH xHC reports 375mA maximum suspend well current required when in the D3 <sub>COLD</sub> state.
5	<b>Device Specific Initialization (DSI)</b> —RO. The PCH reports 0, indicating that no device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PME_CLK)</b> —RO. The PCH reports 0, indicating that no 24-MHz clock is required to generate PME#.
2:0	<b>Version (VER)</b> —RO. The PCH reports 010b, indicating that it complies with Revision 1.1 of the PCI Power Management Specification.

**Notes:**

1. Normally, this register is read-only to report capabilities to the power management software. To report different power management capabilities, depending on the system in which the PCH is used, the write access to this register is controlled by the Access Control bit (D20:F0:40h, bit 31). The value written to this register does not affect the hardware other than changing the value returned during a read.
2. This register is modified and maintained by BIOS
3. Reset: core well, but not D3-to-D0 warm reset.



### 13.1.24 PWR\_CNTL\_STS—Power Management Control/Status Register (USB xHCI—D20:F0)

Address Offset: 74h–75h      Attribute: R/W, R/WC, RO  
 Default Value: 0008h      Size: 16 bits

Bit	Description
15	<p><b>PME Status</b>—R/WC. This bit is set when the PCH xHC would normally assert the PME# signal independent of the state of the PME_En bit. Writing a 1 to this bit will clear it and cause the internal PME to de-assert (if enabled).</p> <p><b>Note:</b> This bit must be explicitly cleared by the operating system each time the operating system is loaded.</p> <p>This bit is not reset by Function Level Reset.</p>
14:13	<b>Data Scale</b> —RO. Hardwired to 00b indicating it does not support the associated Data register.
12:9	<b>Data Select</b> —RO. Hardwired to 0000b indicating it does not support the associated Data register.
8	<p><b>PME Enable (PME_En)</b>—R/W      0 = Disable.      1 = Enables the PCH xHC to generate an internal PME signal when PME_Status is 1.</p> <p><b>Note:</b> This bit must be explicitly cleared by the operating system each time it is initially loaded.</p> <p>This bit is not reset by Function Level Reset.</p>
7:2	Reserved
1:0	<p><b>Power State</b>—R/W. This 2-bit field is used both to determine the current power state of EHC function and to set a new power state. The definition of the field values are:</p> <p>00 = D0 state      11 = D3<sub>HOT</sub> state</p> <p>If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3<sub>HOT</sub> state, the PCH must not accept accesses to the EHC memory range; but the configuration space must still be accessible.</p>

### 13.1.25 MSI\_CAPID—Message Signaled Interrupt (MSI) Capability ID Register (USB xHCI—D20:F0)

Address Offset: 80h      Attribute: RO  
 Default Value: 05h      Size: 8 bits

Bit	Description
7:0	<b>Capability ID</b> —RO. Hardwired to 05h indicating that this is the start of a MSI Capability structure.

### 13.1.26 NEXT\_PTR—Next Item Pointer Register (USB xHCI—D20:F0)

Address Offset: 81h      Attribute: RO  
 Default Value: 00h      Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:0	<b>Next Item Pointer Capability</b> —RO. This register points to the next capability.

### 13.1.27 MSI\_MCTL—Message Signal Interrupt (MSI) Message Control Register (USB xHCI—D20:F0)

Address Offset: 82h-83h  
 Default Value: 0086h

Attribute: RO, R/W  
 Size: 16 bits

Bit	Description
15:8	Reserved
7	<b>64-bit Address Capable (C64)</b> —RO. Capable of generating 64-bit messages.
6:4	<b>Multiple Message Enable (MME)</b> —R/W. Indicates the number of messages the controller should assert. This device supports multiple message MSI.
3:1	<b>Multiple Message Capable (MMC)</b> —RO. This field is set by hardware to reflect the number of Interrupters supported. The controller supports up to 8 interrupters. Encoding for number of Interrupters: 000 = 1 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110-111 = Reserved
0	<b>MSI Enable (MSIE)</b> —R/W. If set to 1, MSI is enabled and the traditional interrupt pins are not used to generate interrupts. If cleared to 0, MSI operation is disabled and the traditional interrupt pins are used.

### 13.1.28 MSI\_LMAD—Message Signal Interrupt (MSI) Lower Message Address Register (USB xHCI—D20:F0)

Address Offset: 84h-87h  
 Default Value: 00000000h

Attribute: R/W  
 Size: 32 bits

Bit	Description
31:2	<b>Lower Message Address</b> —R/W. Lower DWord of the system specified message address.
1:0	Reserved

### 13.1.29 MSI\_UMAD—Message Signal Interrupt (MSI) Upper Message Address Register (USB xHCI—D20:F0)

Address Offset: 88h-8Bh  
 Default Value: 00000000h

Attribute: R/W  
 Size: 32 bits

Bit	Description
31:0	<b>Upper Message Address</b> —R/W. Upper DWord of the system specified message address.

### 13.1.30 MSI\_MD—Message Signal Interrupt (MSI) Message Data Register (USB xHCI—D20:F0)

Address Offset: 8Ch-8Fh      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:16	Reserved
15:0	<b>Data</b> —R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

### 13.1.31 U2OCM1—xHCI USB 2.0 Overcurrent Mapping Register X (USB xHCI—D20:F0)

Address Offset: Overcurrent Mapping Register 0: B0h-B3h, Attribute: R/W  
 Overcurrent Mapping Register 1: B4h-B7h,  
 Overcurrent Mapping Register 2: B8h-BBh,  
 Overcurrent Mapping Register 3: BDh-BFh

Default Value: 00000000h      Size: 32 bits

Bit	Description
31:8	Reserved
7:0	USB 2.0 Port Assignment When Set to 1, Bit 0 maps the OC pin x to USB 2.0 port 0 Bit 1 maps the OC pin x to USB 2.0 port 1 ... Bit 7 maps the OC pin x to USB 2.0 port 7

### 13.1.32 U30CM1—xHCI USB3 Overcurrent Pin Mapping 1 (USB xHCI—D20:F0)

Address Offset: Overcurrent Mapping Register 0: C0h-C3h, Attribute: R/W  
 Overcurrent Mapping Register 1: C4h-C7h,

Overcurrent Mapping Register 2: C8h-CBh,

Overcurrent Mapping Register 3: CDh-CFh

Default Value: 00000000h

Size: 32 bits

Bit	Description
31:4	Reserved
3:0	USB 3.0 Port Assignment When Set to 1, Bit 0 maps the OC pin X to USB 3.0 port 1 Bit 1 maps the OC pin X to USB 3.0 port 2 Bit 2 maps the OC pin X to USB 3.0 port 3 Bit 3 maps the OC pin X to USB 3.0 port 4

### 13.1.33 XUSB2PR—xHC USB 2.0 Port Routing Register (USB xHCI—D20:F0)

Address Offset: D0–D3h

Attribute:

R/W, RO

Default Value: 00000000h

Size:

32 bits

**Note:** Bits 3:0 are located in the Suspend Well.

Bit	Description
31:9	Reserved
8:0	<b>USB 2.0 Host Controller Selector (USB2HCSEL)</b> —R/W. Maps a USB 2.0 port to the xHC or EHC #1 host controller. When set to 0, this bit routes all the corresponding USB 2.0 port pins to the EHCI controller (D29:F0) and RMH #1. The USB 2.0 port is masked from the xHC and the USB 2.0 port's OC pin is routed to the EHCI controller (D29:F0). When set to 1, this bit routes all the corresponding USB 2.0 pins to the xHC controller. The USB 2.0 port is masked from the EHC and the USB 2.0 port's OC pin is routed to the xHC controller (D20:F0). Port to bit mapping is in one-hot encoding; that is, bit 0 controls port 1 and so on. Bit 0 = USB 2.0 Port 0 .... Bit 7 = USB 2.0 Port 7

### 13.1.34 XUSB2PRM—xHC USB 2.0 Port Routing Mask Register (USB xHCI—D20:F0)

Address Offset: D4–D7h      Attribute: R/WL, RO  
 Default Value: 00000000h      Size: 32 bits

**Note:** The R/WL property of this register is controlled by the ACCTRL bit (D20:F0:40h, bit 31).

Bit	Description
31:8	Reserved.
7:0	<b>USB 2.0 Host Controller Selector Mask (USB2HCSELM)</b> —R/WL. This bit field allows the BIOS to communicate to the OS which USB 2.0 ports can be switched from the EHCI controller to the xHC controller. When set to 1, the operating system may switch the USB 2.0 port between the EHCI and xHCI host controllers by modifying the corresponding USB2HCSEL bit (D20:F0:D0h, bit 3:0). When set to 0, The operating system shall not modify the corresponding USB2HCSEL bit. Port to bit mapping is in one-hot encoding; that is, bit 0 controls port 1 and so on. Bit 0 = USB 2.0 Port 0 .... Bit 7 = USB 2.0 Port 7

### 13.1.35 USB3\_PSSEN—USB3 Port SuperSpeed Enable Register (USB xHCI—D20:F0)

Address Offset: D8h–DBh      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

**Note:** Bits 3:0 are located in the Suspend Well.

Bit	Description
31:4	Reserved.
3:0	<b>USB3 Port SuperSpeed Enable (USB3PSSEN)</b> —R/W. This field controls whether SuperSpeed capability is enabled for a given USB 3.0 port. When set to 1, this bit enables the SuperSpeed terminations and allows the xHC to view the SuperSpeed connections on the USB port. Enables PORTSC to see the connects on the ports. When set to 0, the port's SuperSpeed capability is not visible to the xHC. Bit 0 = USB 3.0 Port 1 Bit 1 = USB 3.0 Port 2 Bit 2 = USB 3.0 Port 3 Bit 3 = USB 3.0 Port 4

### 13.1.36 USB3PRM—USB3 Port Routing Mask Register (USB xHCI—D20:F0)

Address Offset: DC-DFh  
Default Value: 00000000h  
Power Well: Core

Attribute: R/WL, RO  
Size: 32 bits

**Note:** The R/WL property of this register is controlled by the ACCTRL bit (D20:F0:40h, bit 31).

Bit	Description
31:4	Reserved.
3:0	<b>USB 2.0 Host Controller Selector Mask (USB2HCSELM)</b> —R/WL. This bit field allows the BIOS to communicate to the OS which USB 3.0 ports can have the SuperSpeed capabilities enabled. When set to 1, the OS may enable or disable the SuperSpeed capabilities by modifying the corresponding USB3PSEN bit (D20:F0:D8h, bit 3:0). When set to 0, the OS shall not modify the corresponding USB3PSEN bit. Bit 0 = USB 3.0 Port 1 Bit 1 = USB 3.0 Port 2 Bit 2 = USB 3.0 Port 3 Bit 3 = USB 3.0 Port 4

## 13.2 Memory-Mapped I/O Registers

The xHCI Memory-Mapped I/O space is composed of two sets of registers: Capability Registers and Operational Registers.

**Note:** The PCH xHC controller will not accept locked memory transactions (neither reads nor writes) as a target. The locked transactions should not be forwarded to PCI as the address space is known to be allocated to USB. Attempting to access the xHCI controller Memory-Mapped I/O space using locked memory transactions will result in undefined behavior.

**Note:** When the xHCI function is in the D3 PCIe\* power state, accesses to the xHCI memory range are ignored and result in a master abort. Similarly, if the Memory Space Enable (MSE) bit (D20:F0:04h, bit 1) is not set in the Command register in configuration space, the memory range will not be decoded by the PCH xHC. If the MSE bit is not set, the PCH must default to allowing any memory accesses for the range specified in the BAR to go to PCI. This is because the range may not be valid and, therefore, the cycle must be made available to any other targets that may be currently using that range.

### 13.2.1 Host Controller Capability Registers

These registers specify the limits, restrictions and capabilities of the host controller implementation.

**Table 13-2. Enhanced Host Controller Capability Registers**

MEM_BASE + Offset	Mnemonic	Register	Default	Type
00h	CAPLENGTH	Capabilities Registers Length	80h	RW/L
02h-03h	HCIVERSION	Host Controller Interface Version Number	0100h	RO
04h-07h	HCSPARAMS1	Host Controller Structural Parameters #1	0E000820h	RW/L
08h-0Bh	HCSPARAMS2	Host Controller Structural Parameters #2	84000054h	RW/L, RO
0Ch-0Fh	HCSPARAMS3	Host Controller Structural Parameters #3	00040001h	RW/L, RO
10h-13h	HCCPARAMS	Host Controller Capability Parameters	200071E9h	RW/L, R/W, RO
14h-17h	DBOFF	Doorbell Offset	00003000h	RO
18h-1Bh	RTSOFF	Runtime Register Space Offset	00002000h	RO

### 13.2.1.1 CAPLENGTH—Capability Registers Length Register

Offset: MEM\_BASE + 00h Attribute: R/W  
Default Value: 80h Size: 8 bits

Bit	Description
7:0	<b>Capability Register Length Value</b> —R/W. This register is used as an offset to add to the Memory Base register (D20:F0:10h) to find the beginning of the Operational Register Space. This register is modified and maintained by BIOS.

### 13.2.1.2 HCIVERSION—Host Controller Interface Version Number Register

Offset: MEM\_BASE + 02h–03h Attribute: RO  
Default Value: 0100h Size: 16 bits

Bit	Description
15:0	<b>Host Controller Interface Version Number</b> —RO. This is a two-byte register containing a BCD encoding of the version number of interface that this host controller interface conforms to.

### 13.2.1.3 HCSPARAMS1—Host Controller Structural Parameters #1 Register

Offset: MEM\_BASE + 04h–07h Attribute: RW/L, RO  
Default Value: 0E000820h Size: 32 bits

Bit	Description
31:24	<b>Number of Ports (MaxPorts)</b> —RW/L. This field specifies the number of port register sets that are addressable in the Operational Register Space. Default value = 0Eh
23:19	Reserved
18:8	<b>Number of Interrupters (MaxIntrs)</b> —RW/L. This field specifies the number of interrupters implemented on this host controller. Each interrupter is allocated to a vector of MSI and controls its generation and moderation.
7:0	<b>Number of Device Slots (MaxSlots)</b> —RW/L. This field specifies the number of Device Context Structures and Doorbell Array entries this host controller can support. Valid values are in the range of 1 to 255.

### 13.2.1.4 HCSPARAMS2—Host Controller Structural Parameters #2 Register

Offset: MEM\_BASE + 08h-0Bh Attribute: RW/L, RO  
 Default Value: 84000054h Size: 32 bits

Bit	Description
31:27	<b>Maximum Scratchpad Buffers (MaxScratchpadBufs)</b> —RW/L. Indicates the number of Scratchpad Buffers system software shall reserve for the xHC.
26	<b>Scratchpad Restore (SPR)</b> —RW/L 0 = Indicates the Scratchpad buffer space may be freed and reallocated between power events. 1 = Indicates that the xHC requires the integrity of the Scratchpad buffer space to be maintained across power events.
25:8	Reserved
7:4	<b>Event Ring Segment Table Maximum (ERSTMax)</b> —RW/L. This field determines the maximum value supported by the Event Ring Segment Table Base Size registers.
3:0	<b>Isochronous Scheduling Threshold (IST)</b> —RW/L. This field indicates to system software the minimum distance (in time) that it is required to stay ahead of the xHC while adding TRBs, in order to have the xHC process them at the correct time. The value is specified in the number of frames/microframes. If bit [3] of IST is cleared to 0b, software can add a TRB no later than IST [2:0] microframes before that TRB is scheduled to be executed. If bit [3] of IST is set to 1b, software can add a TRB no later than IST[2:0] frames before that TRB is scheduled to be executed.

### 13.2.1.5 HCSPARAMS3—Host Controller Structural Parameters #3 Register

Offset: MEM\_BASE + 0Ch-0Fh Attribute: RW/L, RO  
 Default Value: 00040001h Size: 32 bits

Bit	Description												
31:16	<b>U2 Device Exit Latency (U2DEL)</b> —RW/L. Indicates the worst case latency to transition from U2 to U0. Applies to all root hub ports. The following are permissible values: <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Zero</td> </tr> <tr> <td>01h</td> <td>Less than 1 <math>\mu</math>s</td> </tr> <tr> <td>02h</td> <td>Less than 2 <math>\mu</math>s</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>0Bh-FFh</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Description	00h	Zero	01h	Less than 1 $\mu$ s	02h	Less than 2 $\mu$ s	...		0Bh-FFh	Reserved
Value	Description												
00h	Zero												
01h	Less than 1 $\mu$ s												
02h	Less than 2 $\mu$ s												
...													
0Bh-FFh	Reserved												
15:8	Reserved												
7:0	<b>U1 Device Exit Latency (U1DEL)</b> —RW/L. Worst case latency to transition a root hub Port Link State (PLS) from U1 to U0. Applies to all root hub ports. The following are permissible values: <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Zero</td> </tr> <tr> <td>01h</td> <td>Less than 1 <math>\mu</math>s</td> </tr> <tr> <td>02h</td> <td>Less than 2 <math>\mu</math>s</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>0800h-FFFFh</td> <td>Reserved</td> </tr> </tbody> </table>	Value	Description	00h	Zero	01h	Less than 1 $\mu$ s	02h	Less than 2 $\mu$ s	...		0800h-FFFFh	Reserved
Value	Description												
00h	Zero												
01h	Less than 1 $\mu$ s												
02h	Less than 2 $\mu$ s												
...													
0800h-FFFFh	Reserved												

### 13.2.1.6 HCCPARAMS—Host Controller Capability Parameters Register

Offset: MEM\_BASE + 10h-13h Attribute: RW/L, R/W, RO  
Default Value: 200071C1h Size: 32 bits

Bit	Description
31:16	<b>xHCI Extended Capabilities Pointer (xECP)</b> —RW/L This field indicates the existence of a capabilities list. The value of this field indicates a relative offset, in 32-bit words, from Base to the beginning of the first extended capability.
15:12	<b>Maximum Primary Stream Array Size (MaxPSASize)</b> —RW/L. This field identifies the maximum size Primary Stream Array that the xHC supports. The Primary Stream Array size = $2^{\text{MaxPSASize}+1}$ . Valid MaxPSASize values are 1 to 15.
11	Reserved
10	<b>Stopped EDLTA Capability (SEC)</b> —R/W. This flag indicates that the host controller implementation Stream Context support a Stopped EDLTA field.
9	<b>Stopped-Short Packet Capability (SPC)</b> —R/W. This flag indicates that the host controller implementation is capable of generating a Stopped-Short Packet Completion Code.
8	Reserved
7	<b>No Secondary SID Support (NSS)</b> —RW/L. Hardwired to '0' indicating Secondary Stream ID decoding is supported.
6	<b>Latency Tolerance Messaging Capability (LTC)</b> —RW/L 0 = Latency Tolerance Messaging is not supported 1 = Latency Tolerance Messaging is supported
5	<b>Light HC Reset Capability (LHRC)</b> —RW/L 0 = Light Host Controller Reset is not supported 1 = Light Host Controller Reset is supported
4	<b>Port Indicators (PIND)</b> —RW/L. This bit indicates whether the xHC root hub ports support port indicator control. When this bit is a '1', the port status and control registers include a read/writeable field for controlling the state of the port indicator.
3	<b>Port Power Control (PPC)</b> —RO. This bit indicates whether the host controller implementation includes port power control. A, '1' in this bit indicates the ports have port power switches. A, '0' in this bit indicates the port do not have port power switches.
2	<b>Context Size (CSZ)</b> —RW/L. If this bit is set to '1', then the xHC uses 64 byte Context data structures. If this bit is cleared to '0', then the xHC uses 32 byte Context data structures.  <b>Note:</b> This flag does not apply to Stream Contexts.
1	<b>BW Negotiation Capability (BNC)</b> —RW/L 0 = Not capable of BW Negotiation 1 = Capable of BW Negotiation
0	<b>64-bit Addressing Capability (AC64)</b> —RW/L. This bit documents the addressing range capability of the xHC. The value of this flag determines whether the xHC has implemented the high order 32-bits of 64-bit register and data structure pointer fields. Values for this flag have the following interpretation: 0 = Supports 32-bit address memory pointers 1 = Supports 64-bit address memory pointers  If 32-bit address memory pointers are implemented, the xHC shall ignore the high order 32 bits of 64-bit data structure pointer fields, and system software shall ignore the high order 32- bits of 64-bit xHC registers.

### 13.2.1.7 DBOFF—Doorbell Offset Register

Offset: MEM\_BASE + 14h-17h Attribute: RO  
 Default Value: 00003000h Size: 32 bits

Bit	Description
31:2	<b>Doorbell Array Offset</b> —RO. This field defines the DWord offset of the Doorbell Array base address from the Base (for example, the base address of the xHCI Capability register address space).
1:0	Reserved

### 13.2.1.8 RTSOFF—Runtime Register Space Offset Register

Offset: MEM\_BASE + 18h-1Bh Attribute: RO  
 Default Value: 00002000h Size: 32 bits

Bit	Description
31:5	<b>Runtime Register Space Offset</b> —RO. This field defines the 32-byte offset of the xHCI Runtime Registers from the Base. That is, Runtime Register Base Address = Base + Runtime Register Set Offset.
4:0	Reserved

### 13.2.2 Host Controller Operational Registers

This section defines the xHC operational registers. These registers are located after the capabilities registers. The operational register base must be DWord aligned and is calculated by adding the value in the first capabilities register (CAPLENGTH) to the base address of the xHC register address space (MEM\_BASE). Since CAPLENGTH is always 80h, Table 13-3 already accounts for this offset. All registers are 32 bits in length.

**Table 13-3. Enhanced Host Controller Operational Register Address Map**

MEM_BASE + Offset	Mnemonic	Register Name	Default	Attribute
80h-83h	USB_CMD	USB Command	00000000h	R/W, RO
84h-87h	USB_STS	USB Status	00000001h	R/WC, RO
88h-8Bh	PAGESIZE	Page Size	00000001h	RO
94h-97h	DNCTRL	Device Notification Control	00000000h	R/W, RO
98h-9Bh	CRCRL	Command Ring Control Low	00000000h	R/W, RO
9Ch-9Fh	CRCRH	Command Ring Control High	00000000h	R/W
B0h-B3h	DCBAPL	Device Context Base Address Array Pointer Low	00000000h	R/W, RO
B4h-B7h	DCBAPH	Device Context Base Address Array Pointer High	00000000h	R/W
B8h-BBh	CONFIG	Configure	00000000h	R/W, RO
480h, 490h, 4A0h, 4B0h, 4C0h, 4D0h, 4E0h, 4F0h, 500h, 510h, 520h	PORTSCNUUSB2	Port N Status and Control USB2	000002A0h	R/W, R/WC, RO, R/WO,
484h, 494h, 4A4h, 4B4h, 4C4h, 4D4h, 4E4h, 4F4h, 504h, 514h, 524h	PORTPMSCNUUSB2	Port N Power Management Status and Control USB2	00000000h	R/W, RO
530h, 540h, 550h, 560h	PORTSCNUUSB3	Port N Status and Control USB3	000002A0h	R/W, RO, R/WO, RW/C
534h, 544h, 554h, 564h	PORTPMSCN	Port N Power Management Status and Control USB 3.0	00000000h	R/W, RO
578h, 588h, 598h, 5A8h	PORTLIX	Port X Link Info Register	00000000h	RO

**Note:** Software must read and write these registers using only DWord accesses.

### 13.2.2.1 USB\_CMD—USB Command Register

Offset: MEM\_BASE + 80h-83h Attribute: R/W, RO  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:12	Reserved
11	<b>Enable U3 MFINDEX Stop (EU3S)</b> —R/W. When set to 1b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the U3, Disconnected, Disabled, or Powered-off state. When cleared to 0b, the xHC may stop the MFINDEX counting action if all Root Hub ports are in the Disconnected, Disabled, or Powered-off state.
10	<b>Enable Wrap Event (EWE)</b> —R/W. When set to 1b, the xHC shall generate a MFINDEX Wrap Event every time the MFINDEX register transitions from 03FFFh to 0. When cleared to 0b, no MFINDEX Wrap Events are generated.
9	<b>Controller Restore State (CRS)</b> —R/W. When set to 1b, MEM_BASE+80h:bit 0= 0b, and MEM_BASE+80h:bit 8 = 1b, the xHC shall perform a Restore State operation and restore its internal state. When set to 1b and MEM_BASE+80h:bit 0= 1b <b>or</b> MEM_BASE+80h:bit 8 = 0b, or when cleared to 0, no Restore State operation shall be performed. <b>Note:</b> This flag always returns '0' when read.
8	<b>Controller Save State (CSS)</b> —R/W. When written by software with 1b and MEM_BASE+80h:bit 0= 0b, the xHC shall save any internal state that will be restored by a subsequent Restore State operation. When written by software with 1b and MEM_BASE+80h:bit 0= 1b, or written with 0, no Save State operation shall be performed. <b>Note:</b> This flag always returns '0' when read.
7	<b>Light Host Controller Reset (LHCRST)</b> —R/W. If the Light HC Reset Capability (LHRC) bit (MEM_BASE=10h:bit 5) is 1b, then setting this bit to 1b allows the driver to reset the xHC without affecting the state of the ports. A system software read of this bit as 0b indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the xHC. A software read of this bit as a 1b indicates the Light Host Controller Reset has not yet completed. <b>Note:</b> If Light HC Reset Capability is not implemented, a read of this flag will always return a 0b.
6:4	Reserved
3	<b>Host System Error Enable (HSEE)</b> —R/W. When this bit is set to 1b, and the HSE bit (MEM_BASE+84h:bit 2) is set to 1b, the xHC shall assert out-of-band error signaling to the host. The signaling is acknowledged by software clearing the HSE bit.
2	<b>Interrupter Enable (INTE)</b> —R/W. This bit provides system software with a means of enabling or disabling the host system interrupts generated by interrupters. When this bit is set to 1b, then Interrupter host system interrupt generation is allowed, for example, the xHC shall issue an interrupt at the next interrupt threshold if the host system interrupt mechanism (for example; MSI, MSIX, and so forth.) is enabled. The interrupt is acknowledged by a host system interrupt specific mechanism.
1	<b>Host Controller Reset (HCRST)</b> —R/W. This control bit is used by software to reset the host controller. When software sets this bit to 1b, the Host Controller resets its internal pipelines, timers, counters, state machines, and so forth, to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. PCI Configuration registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. <b>Notes:</b> <ol style="list-style-type: none"> <li>1. This bit is cleared to 0b by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a 0b to this bit and shall not write any xHC Operational or Runtime registers while HCRST is set to 1b.</li> <li>2. Software shall not set this bit to 1b when the HCHalted (HCH) bit (MEM_BASE+84h:bit 0) is set to 0b. Attempting to reset an actively running host controller will result in undefined behavior.</li> </ol>

Bit	Description
0	<p><b>Run/Stop (R/S)</b>—R/W. When set to 1b, the xHC proceeds with execution of the schedule. The xHC continues execution as long as this bit is set to 1b.</p> <p>When this bit is cleared to 0b, the xHC completes the current and any actively pipelined transactions on the USB and then halts. The xHC shall halt within 16 micro-frames after software clears the Run/Stop bit. The HCHalted (HCH) bit (MEM_BASE+84h:bit 0) indicates when the xHC has finished its pending pipelined transactions and has entered the stopped state. Software shall not write a '1' to this flag unless the xHC is in the Halted state (that is, HCH in the USBSTS register is '1'); doing so will yield undefined results.</p>

### 13.2.2.2 USB\_STS—USB Status Register

Offset: MEM\_BASE + 84h–87h Attribute: R/WC, RO  
 Default Value: 00000001h Size: 32 bits

This register indicates pending interrupts and various states of the Host controller. The status resulting from a transaction on the serial bus is not indicated in this register. See the Interrupts description in section 4 of the xHCI specification for additional information concerning interrupt conditions.

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 has no effect.

Bit	Description
31:13	Reserved.
12	<p><b>Host Controller Error (HCE)</b>—RO. This flag shall be set to indicate that an internal error condition has been detected which requires software to reset and re-initialize the xHC.</p> <p>0 = No internal xHC error conditions exist.    1 = Internal xHC error condition exists.</p>
11	<p><b>Controller Not Ready (CNR)</b>—RO.</p> <p>0 = Ready    1 = Not Ready</p> <p>Software shall not write any Doorbell or Operational register of the xHC, other than the USBSTS register, until CNR = 0b. This flag is set by the xHC after a Hardware Reset and cleared when the xHC is ready to begin accepting register writes. This flag shall remain cleared (0b) until the next Chip Hardware Reset.</p>
10	<p><b>Save/Restore Error (SRE)</b>—R/WC. If an error occurs during a Save or Restore operation, this bit shall be set to 1b. This bit shall be cleared to 0b when a Save or Restore operation is initiated or when written with 1b.</p>
9	<p><b>Restore State Status (RSS)</b>—RO. When the Controller Restore State (CRS) flag in the USB_CMD register is written with 1b, this bit shall be set to 1b and remain set while the xHC restores its internal state.</p> <p><b>Note:</b> When the Restore State operation is complete, this bit shall be cleared to 0b.</p>
8	<p><b>Save State Status (SSS)</b>—RO. When the Controller Save State (CSS) flag in the USB_CMD register is written with 1b, this bit shall be set to 1b and remain set while the xHC saves its internal state.</p> <p><b>Note:</b> When the Save State operation is complete, this bit shall be cleared to 0b.</p>
7:5	Reserved
4	<p><b>Port Change Detect (PCD)</b>—R/WC. This bit is allowed to be maintained in the Auxiliary power well. Alternatively, it is also acceptable that on a D3-to-D0 transition of the xHC, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, overcurrent change, enable/disable change and connect status change). Regardless of the implementation, when this bit is readable (that is, in the D0 state), it must provide a valid view of the Port Status registers.</p> <p>0 = No change bit transition from a 0 to 1 or No Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.    1 = The Host controller sets this bit to 1 when any port for which the Port Owner bit is set to 0 has a change bit transition from a 0 to 1 or a Force Port Resume bit transition from 0 to 1 as a result of a J-K transition detected on a suspended port.</p>

Bit	Description
3	<b>Event Interrupt (EINT)</b> —R/WC. The xHC sets this bit to 1b when the Interrupt Pending (IP) bit of any Interrupter transitions from 0b to 1b. Software that uses EINT shall clear it prior to clearing any IP flags. A race condition will occur if software clears the IP flags then clears the EINT flag, and between the operations another IP '0' to '1' transition occurs. In this case the new IP transition will be lost.
2	<b>Host System Error (HSE)</b> —R/WC. The xHC sets this bit to 1b when a serious error is detected, either internal to the xHC or during a host system access involving the xHC module. Conditions that set this bit to '1' include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the xHC clears the Run/Stop (R/S) bit in the USB_CMD register to prevent further execution of the scheduled TDs. If the HSEE bit in the USB_CMD register is 1b, the xHC shall also assert out-of-band error signaling to the host.
1	Reserved
0	<b>HCHalted (HCH)</b> —RO. This bit is a '0' whenever the Run/Stop (R/S) bit is set to 1b. The xHC sets this bit to 1b after it has stopped executing as a result of the Run/Stop (R/S) bit being cleared to 0b, either by software or by the xHC hardware (for example, internal error). If this bit is set to 1b, then SOFs, microSOFs, or Isochronous Timestamp Packets (ITP) shall not be generated by the xHC.

### 13.2.2.3 PAGESIZE—PAGESIZE Register

Offset: MEM\_BASE + 88h–8Bh Attribute: RO  
 Default Value: 00000001h Size: 32 bits

Bit	Description
31:16	Reserved
15:0	<b>Page Size</b> —RO. Hardwired to 1h to indicate support for 4 Kbyte page sizes.

### 13.2.2.4 DNCTRL—Device Notification Control Register

Offset: MEM\_BASE + 94h–97h Attribute: R/W, RO  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:16	Reserved
15:0	<b>Notification Enable</b> —R/W. When a Notification Enable bit is set, a Device Notification Event will be generated when a Device Notification Transaction Packet is received with the matching value in the Notification Type field. For example, setting N1 to '1' enables Device Notification Event generation if a Device Notification TP is received with its Notification Type field set to '1' (FUNCTION_WAKE), and so on Refer to the USB 3.0 Specification for more information on Notification Types.

### 13.2.2.5 CRCRL—Command Ring Control Low Register

Offset: MEM\_BASE + 98h–9Bh Attribute: R/W, RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:6	<p><b>Command Ring Pointer</b>—R/W. This field defines low-order bits of the initial value of the 64-bit Command Ring Dequeue Pointer.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>Writes to this field are ignored when Command Ring Running bit (CRR) = 1b.</li> <li>If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command.</li> <li>If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer.</li> <li>Reading this field always returns 0b.</li> </ol>
5:4	Reserved
3	<p><b>Command Ring Running (CRR)</b>—RO. This bit is set to 1b if the Run/Stop (R/S) bit is 1b and the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command. It is cleared to 0b when the Command Ring is stopped after writing a 1b to the Command Stop (CS) or Command Abort (CA) bits, or if the R/S bit is cleared to 0b.</p>
2	<p><b>Command Abort (CA)</b>—R/W. Writing a 1b to this bit shall immediately terminate the currently executing command, stop the Command Ring, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped.</p> <p>The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>Writes to this flag are ignored by the xHC if Command Ring Running (CRR) = 0b.</li> <li>Reading this bit always returns 0b.</li> </ol>
1	<p><b>Command Stop (CS)</b>—R/W. Writing a 1b to this bit shall stop the operation of the Command Ring after the completion of the currently executing command, and generate a Command Completion Event with the Completion Code set to Command Ring Stopped and the Command TRB Pointer set to the current value of the Command Ring Dequeue Pointer.</p> <p>The next write to the Host Controller Doorbell with DB Reason field set to Host Controller Command shall restart the Command Ring operation.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>Writes to this flag are ignored by the xHC if Command Ring Running (CRR) bit = 0b.</li> <li>Reading this bit always returns 0b.</li> </ol>
0	<p><b>Ring Cycle State (RCS)</b>—R/W. This bit identifies the value of the xHC Consumer Cycle State (CCS) flag for the TRB referenced by the Command Ring Pointer.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>Writes to this bit are ignored when the Command Ring Running (CRR) bit = 1b.</li> <li>If the CRCR register is written while the Command Ring is stopped (CCR = 0b), then the value of this flag shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command.</li> <li>If the CRCR register is not written while the Command Ring is stopped (CCR = 0b), then the Command Ring will begin fetching Command TRBs using the current value of the internal Command Ring CCS flag.</li> <li>Reading this flag always returns 0b.</li> </ol>

**Notes:**

- Setting the Command Stop (CS) or Command Abort (CA) flags while CRR = 1b shall generate a Command Ring Stopped Command Completion Event.
- Setting both the Command Stop (CS) and Command Abort (CA) flags with a single write to the CRCR register while CRR = '1' shall be interpreted as a Command Abort (CA) by the xHC.
- The values of the internal xHC Command Ring CCS flag and Dequeue Pointer are undefined after hardware reset, so these fields shall be initialized before setting USB\_CMD Run/Stop (R/S) bit (MEM\_BASE+80:bit 0) to 1b.



### 13.2.2.6 CRCRH—Command Ring Control High Register

Offset: MEM\_BASE + 9Ch–9Fh Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<p><b>Command Ring Pointer</b>—R/W. This field defines high order bits of the initial value of the 64-bit Command Ring Dequeue Pointer.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>Writes to this field are ignored when Command Ring Running bit (CRR) = 1b.</li> <li>If the CRCR register is written while the Command Ring is stopped (CRR = 0b), the value of this field shall be used to fetch the first Command TRB the next time the Host Controller Doorbell register is written with the DB Reason field set to Host Controller Command.</li> <li>If the CRCR register is not written while the Command Ring is stopped (CRR = 0b), then the Command Ring shall begin fetching Command TRBs at the current value of the internal xHC Command Ring Dequeue Pointer.</li> <li>Reading this field always returns 0b.</li> </ol>

### 13.2.2.7 DCBAAPL—Device Context Base Address Array Pointer Low Register

Offset: MEM\_BASE + B0h–B3h Attribute: R/W, RO  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:6	<b>Device Context Base Address Array Pointer</b> —R/W. This field defines low-order bits of the 64-bit base address of the Device Context Pointer Array table (a table of address pointers that reference Device Context structures for the devices attached to the host.)
5:0	Reserved

### 13.2.2.8 DCBAAPH—Device Context Base Address Array Pointer High Register

Offset: MEM\_BASE + B4h–B7h Attribute: R/W

Bit	Description
31:0	<b>Device Context Base Address Array Pointer</b> —R/W. This field defines high-order bits of the 64-bit base address of the Device Context Pointer Array table (a table of address pointers that reference Device Context structures for the devices attached to the host.)

### 13.2.2.9 CONFIG—Configure Register

Offset: MEM\_BASE + B8h–BBh Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Maximum Device Slots Enabled (MaxSlotsEn)</b>—R/W. This field specifies the maximum number of enabled Device Slots. Valid values are in the range of 0h to 20h. Enabled Devices Slots are allocated contiguously (for example, a value of 16 specifies that Device Slots 1 to 16 are active.) A value of '0' disables all Device Slots. A disabled Device Slot shall not respond to Doorbell Register references.</p> <p><b>Note:</b> This field shall not be modified if the xHC is running (Run/Stop (R/S) = '1').</p>

### 13.2.2.10 PORTSCNUSB2—Port N Status and Control USB2 Register

Offset: There are 11 USB2 PORTSC registers at offsets: 480h, 490h, 4A0h, 4B0h, 4C0h, 4D0h, 4E0h, 4F0h, 500h, 510h, 520h  
Attribute: R/W, R/WC, RO, R/WO  
Default Value: 000002A0h Size: 32 bits

A host controller must implement one or more port registers. Software uses the N\_Port information from the Structural Parameters Register to determine how many ports need to be serviced. All ports have the structure defined below. Software must not write to unreported Port Status and Control registers.

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No device connected
- Port disabled

When a device is attached, the port state transitions to the attached state and system software will process this as with any status change notification. Refer to Section 4 of the xHCI Specification for operational requirements for how change events interact with port suspend mode.

Bit	Description
31	<b>Warm Port Reset (WPR)</b> —R/WO. When software sets this bit to 1b, the Warm Reset sequence is initiated and the PR bit is set to 1b. Once initiated, the PR, PRC, and WRC bits shall reflect the progress of the Warm Reset sequence. This flag shall always return 0b when read. <b>Note:</b> This bit applies only to USB 3.0 capable ports. This bit is Reserved for USB 2.0 capable-only ports.
30	<b>Device Removable (DR)</b> —RO. This bit indicates if this port has a removable device attached. 0 = Device is removable. 1 = Device is non-removable.
29:28	Reserved.
27	<b>Wake on Over-current Enable (WOE)</b> —R/W 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to over-current conditions as system wake-up events.
26	<b>Wake on Disconnect Enable (WDE)</b> —R/W. 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.
25	<b>Wake on Connect Enable (WCE)</b> —R/W 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.
24	<b>Cold Attach Status (CAS)</b> —RO. This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1. <b>Note:</b> This bit is 0b if the PP bit is 0b or for USB 2.0 capable-only ports.
23	<b>Port Configuration Error Change (CEC)</b> —R/WC. This flag indicates that the port failed to configure its link partner. Software shall clear this bit by writing a 1 to it. This bit is bit is on the Suspend well. <b>Note:</b> This bit applies only to USB 3.0 capable ports. This bit is Reserved for USB 2.0 capable-only ports.



Bit	Description																					
22	<p><b>Port Link State Change (PLC)</b>—R/WC</p> <p>0 = No change 1 = Link Status Change</p> <p>This flag is set to '1' due to the following Port Link State (PLS) transitions:</p> <table> <thead> <tr> <th>Transition</th> <th>Condition</th> </tr> </thead> <tbody> <tr> <td>U3 -&gt; Resume</td> <td>Wakeup signaling from a device</td> </tr> <tr> <td>Resume -&gt; Recovery -&gt; U0</td> <td>Device Resume complete (USB 3.0 capable ports only)</td> </tr> <tr> <td>Resume -&gt; U0</td> <td>Device Resume complete (USB 2.0 capable-only ports)</td> </tr> <tr> <td>U3 -&gt; Recovery -&gt; U0</td> <td>Software Resume complete (USB 3.0 capable ports only)</td> </tr> <tr> <td>U3 -&gt; U0</td> <td>Software Resume complete (USB 2.0 capable-only ports)</td> </tr> <tr> <td>U2 -&gt; U0</td> <td>L1 Resume complete (USB 2.0 capable-only ports)</td> </tr> <tr> <td>U0 -&gt; U0</td> <td>L1 Entry Reject (USB 2.0 capable-only ports)</td> </tr> <tr> <td>U0 -&gt; Disabled</td> <td>L1 Entry Error (USB 2.0 capable-only ports)</td> </tr> <tr> <td>Any state -&gt; Inactive</td> <td>Error (USB 3.0 capable ports only)</td> </tr> </tbody> </table> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This bit shall not be set if the PLS transition was due to software setting the PP bit to 0b.</li> <li>2. Software shall clear this bit by writing a 1 to it.</li> </ol>	Transition	Condition	U3 -> Resume	Wakeup signaling from a device	Resume -> Recovery -> U0	Device Resume complete (USB 3.0 capable ports only)	Resume -> U0	Device Resume complete (USB 2.0 capable-only ports)	U3 -> Recovery -> U0	Software Resume complete (USB 3.0 capable ports only)	U3 -> U0	Software Resume complete (USB 2.0 capable-only ports)	U2 -> U0	L1 Resume complete (USB 2.0 capable-only ports)	U0 -> U0	L1 Entry Reject (USB 2.0 capable-only ports)	U0 -> Disabled	L1 Entry Error (USB 2.0 capable-only ports)	Any state -> Inactive	Error (USB 3.0 capable ports only)	
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19	<p><b>Warm Port Reset Change (WRC)</b>—R/WC. This bit is set when Warm Reset processing on this port completes.</p> <p>0 = No change (Default) 1 = Warm reset complete</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This bit shall not be set to 1b if the reset processing was forced to terminate due to software clearing the PP bit or PED bit to 0b.</li> <li>2. Software shall clear this bit by writing a 1 to it.</li> <li>3. This bit applies only to USB 3.0 capable ports. This bit is Reserved for USB 2.0 capable-only ports.</li> </ol>																					
18	<p><b>Port Enabled/Disabled Change (PEC)</b>—R/WC</p> <p>0 = No change. (Default) 1 = There is a change to PED bit.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This bit shall not be set if the PED transition was due to software setting the PP bit to 0.</li> <li>2. Software shall clear this bit by writing a 1 to it.</li> <li>3. For a USB 2.0-only port, this bit shall be set to 1 only when the port is disabled due to the appropriate conditions existing at the EOF2 point. (See Chapter 11 of the USB Specification for the definition of a port error).</li> <li>4. For a USB 3.0 port, this bit shall be set to '1' if an enabled port transitions to a Disabled state (that is, a 1-to-0 transition of PED). Refer to section 4 of the xHCI Specification for more information.</li> </ol>																					

Bit	Description								
17	<p><b>Connect Status Change (CSC)</b>—R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits.</p> <p>0 = No change (Default) 1 = There is a change to the CCS or CAS bit</p> <p>The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This bit shall not be set if the CCS transition was due to software setting the PP bit to 0b, or the CAS bit transition was due to software setting the WPR bit to 1b.</li> <li>2. Software shall clear this bit by writing a 1 to it.</li> </ol>								
16	<p><b>Port Link State Write Strobe (LWS)</b>—R/W</p> <p>0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field.</p> <p>Reads to this bit return '0'.</p>								
15:14	Reserved								
13:10	<p><b>Port Speed (Port_Speed)</b>. A device attached to this port operates at a speed defined by the following codes:</p> <table> <thead> <tr> <th>Value</th> <th>Speed</th> </tr> </thead> <tbody> <tr> <td>0001b</td> <td>Full-speed (12Mb/s)</td> </tr> <tr> <td>0010b</td> <td>Low-speed (1.5Mb/s)</td> </tr> <tr> <td>0011b</td> <td>High-speed (480Mb/s)</td> </tr> </tbody> </table> <p>All other values reserved. Refer to the <i>eXtensible Host Controller Interface for Universal Serial Bus Specification</i> for additional details.</p>	Value	Speed	0001b	Full-speed (12Mb/s)	0010b	Low-speed (1.5Mb/s)	0011b	High-speed (480Mb/s)
Value	Speed								
0001b	Full-speed (12Mb/s)								
0010b	Low-speed (1.5Mb/s)								
0011b	High-speed (480Mb/s)								
9	<b>Port Power (PP)</b> —RO. Read-only with a value of 1. This indicates that the port does have power.								



Bit	Description																																												
8:5	<p><b>Port Link State (PLS)</b>—R/W. This field is used to power manage the port and reflects its current link state. When the port is in the Enabled state, system software may set the link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port.</p> <table> <thead> <tr> <th>Write Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>The link shall transition to a U0 state from any of the U states.</td></tr> <tr> <td>2</td><td>USB 2.0 ports only. The link should transition to the U2 State.</td></tr> <tr> <td>3</td><td>The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port.</td></tr> <tr> <td>5</td><td>USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored.</td></tr> <tr> <td>15</td><td>USB 2.0 ports only. If the port is in the U3-state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3 Exit substate, else ignored.</td></tr> <tr> <td>All other values</td><td>Ignored</td></tr> </tbody> </table> <p><b>Note:</b> The Port Link State Write Strobe (LWS) shall be set to 1b to write this field.</p> <table> <thead> <tr> <th>Read Value</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>0</td><td>Link is in the U0 State</td></tr> <tr> <td>1</td><td>Link is in the U1 State</td></tr> <tr> <td>2</td><td>Link is in the U2 State</td></tr> <tr> <td>3</td><td>Link is in the U3 State (Device Suspended)</td></tr> <tr> <td>4</td><td>Link is in the Disabled State</td></tr> <tr> <td>5</td><td>Link is in the RxDetect State</td></tr> <tr> <td>6</td><td>Link is in the Inactive State</td></tr> <tr> <td>7</td><td>Link is in the Polling State</td></tr> <tr> <td>8</td><td>Link is in the Recovery State</td></tr> <tr> <td>9</td><td>Link is in the Hot Reset State</td></tr> <tr> <td>10</td><td>Link is in the Compliance Mode State</td></tr> <tr> <td>11</td><td>Link is in the Test Mode State</td></tr> <tr> <td>12–14</td><td>Reserved</td></tr> <tr> <td>15</td><td>Link is in the Resume State</td></tr> </tbody> </table> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This field is undefined if PP = 0.</li> <li>2. Transitions between different states are not reflected until the transition is complete.</li> </ol>	Write Value	Description	0	The link shall transition to a U0 state from any of the U states.	2	USB 2.0 ports only. The link should transition to the U2 State.	3	The link shall transition to a U3 state from any of the U states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port.	5	USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored.	15	USB 2.0 ports only. If the port is in the U3-state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3 Exit substate, else ignored.	All other values	Ignored	Read Value	Definition	0	Link is in the U0 State	1	Link is in the U1 State	2	Link is in the U2 State	3	Link is in the U3 State (Device Suspended)	4	Link is in the Disabled State	5	Link is in the RxDetect State	6	Link is in the Inactive State	7	Link is in the Polling State	8	Link is in the Recovery State	9	Link is in the Hot Reset State	10	Link is in the Compliance Mode State	11	Link is in the Test Mode State	12–14	Reserved	15	Link is in the Resume State
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4	<p><b>Port Reset (PR)</b>—R/W. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0. USB 3.0 ports shall execute the Hot Reset sequence as defined in the USB 3.0 Specification. PR remains set until reset signaling is completed by the root hub.</p> <p>1 = Port is in Reset. 0 = Port is not in Reset.</p>																																												
3	<p><b>Overcurrent Active (OCA)</b>—RO</p> <p>0 = This port does not have an overcurrent condition. (Default) 1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the over current condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.</p>																																												
2	Reserved.																																												

Bit	Description
1	<b>Port Enabled/Disabled</b> —R/W. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable 1 = Enable (Default)
0	<b>Current Connect Status</b> —RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

### 13.2.2.11 PORTPMSCNUSB2—xHCI Port N Power Management Status and Control USB2 Register

Offset: There are 11 USB2 PORTPMSC registers at offsets: 484h, 494h, 4A4h, 4B4h, 4C4h, 4D4h, 4E4h, 4F4h, 504h, 514h, 524h  
Attribute: R/W, RO  
Default Value: 00000000h Size: 32 bits

Bit	Description																		
31:28	<b>Port Test Control</b> —R/W. When this field is '0', the port is not operating in a test mode. (Default) A non-zero value indicates that the port is operating in test mode and the specific test mode is indicated by the specific value. A non-zero Port Test Control value is only valid to a port that is in the Disabled state. If the port is not in this state, the xHC shall respond with the Port Test Control field set to Port Test Control Error. The encoding of the Test Mode bits for a USB 2.0 port are:  <table> <thead> <tr> <th>Value</th> <th>Test Mode</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Test mode not enabled</td> </tr> <tr> <td>1h</td> <td>Test J_STATE</td> </tr> <tr> <td>2h</td> <td>Test K_STATE</td> </tr> <tr> <td>3h</td> <td>Test SE0_NAK</td> </tr> <tr> <td>4h</td> <td>Test Packet</td> </tr> <tr> <td>5h</td> <td>Test FORCE_ENABLE</td> </tr> <tr> <td>6h-14h</td> <td>Reserved.</td> </tr> <tr> <td>15</td> <td>Port Test Control Error</td> </tr> </tbody> </table> Refer to the sections 7.1.20 and 11.24.2.13 of the USB 2.0 Specification for more information on Test Modes.	Value	Test Mode	0h	Test mode not enabled	1h	Test J_STATE	2h	Test K_STATE	3h	Test SE0_NAK	4h	Test Packet	5h	Test FORCE_ENABLE	6h-14h	Reserved.	15	Port Test Control Error
Value	Test Mode																		
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4h	Test Packet																		
5h	Test FORCE_ENABLE																		
6h-14h	Reserved.																		
15	Port Test Control Error																		
27:17	Reserved.																		
16	<b>Hardware LPM Enable (HLE)</b> —R/W 0 = Disable. 1 = Enable. When this bit is a 1, hardware controlled LPM shall be enabled for this port. Refer to section 4 of the USB 2.0 LPM Specification for more information.																		
15:8	<b>L1 Device Slot</b> —R/W. System software sets this field to indicate the ID of the Device Slot associated with the device directly attached to the Root Hub port. A value of 0 indicates there is no device present.																		
7:4	<b>Host Initiated Resume Duration (HIRD)</b> —R/W. System software sets this field to indicate to the recipient device how long the xHC will drive resume if it (the xHC) initiates an exit from L1. The HIRD value is encoded as follows: The value of 0000b is interpreted as 50 $\mu$ s. Each incrementing value up adds 75 $\mu$ s to the previous value. For example, 0001b is 125 $\mu$ s, 0010b is 200 $\mu$ s and so on. Based on this rule, the maximum value resume drive time is at encoding value 1111b which represents 1.2 ms. Refer to section 4 of the USB 2.0 LPM Specification for more information.																		



Bit	Description
3	<b>Remote Wake Enable (RWE)</b> —R/W. The host system sets this flag to enable or disable the device for remote wake from L1. 0 = Disable (Default) 1 = Enable The value of this flag will temporarily (while in L1) override the current setting of the Remote Wake feature set by the standard Set/ClearFeature() commands defined in Universal Serial Bus Specification, Revision 2.0, Chapter 9.
2:0	L1 Status

### 13.2.2.12 PORTSCNUUSB3—xHCI USB3 Port N Status and Control Register

Offset: There are 4 USB3.0 PORTSC registers at offsets: 530h, 540h, 550h, 560h  
 Attribute: R/W, RO, R/WO, RW/C  
 Default Value: 000002A0h Size: 32 bits

A host controller must implement one or more port registers. Software uses the N\_Port information from the Structural Parameters Register to determine how many ports need to be serviced. All ports have the structure defined below. Software must not write to unreported Port Status and Control Registers.

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset. The initial conditions of a port are:

- No device connected
- Port disabled

When a device is attached, the port state transitions to the attached state and system software will process this as with any status change notification. Refer to Section 4 of the xHCI Specification for operational requirements for how change events interact with port suspend mode.

Bit	Description
31	<b>Warm Port Reset (WPR)</b> —R/WO. When software sets this bit to 1b, the Warm Reset sequence is initiated and the PR bit is set to 1b. Once initiated, the PR, PRC, and WRC bits shall reflect the progress of the Warm Reset sequence. This flag shall always return 0b when read.  <b>Note:</b> This bit applies only to USB 3.0 capable ports. This bit is Reserved for USB 2.0 capable-only ports.
30	<b>Device Removable (DR)</b> —RO. This bit indicates if this port has a removable device attached. 0 = Device is removable 1 = Device is non-removable
29:28	Reserved.
27	<b>Wake on Over-current Enable (WOE)</b> —R/W 0 = Disable (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to over-current conditions as system wake-up events.
26	<b>Wake on Disconnect Enable (WDE)</b> —R/W 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device disconnects as system wake-up events.

Bit	Description																				
25	<b>Wake on Connect Enable (WCE)</b> —R/W 0 = Disable. (Default) 1 = Enable. Writing this bit to a 1b enables the port to be sensitive to device connects as system wake-up events.																				
24	<b>Cold Attach Status (CAS)</b> —RO. This bit indicates that far-end terminations were detected in the Disconnected state and the Root Hub Port State Machine was unable to advance to the Enabled state. Software shall clear this bit by writing a 1b to the WPR bit or the xHC shall clear this bit if the CSS bit transitions to 1. <b>Note:</b> This bit is 0b if the PP bit is 0b or for USB 2.0 capable-only ports.																				
23	<b>Port Configuration Error Change (CEC)</b> —R/WC. This flag indicates that the port failed to configure its link partner. Software shall clear this bit by writing a 1 to it. <b>Note:</b> This bit applies only to USB 3.0 capable ports. This bit is Reserved for USB 2.0 capable-only ports.																				
22	<b>Port Link State Change (PLC)</b> —R/WC 0 = No change 1 = Link Status Change This flag is set to '1' due to the following Port Link State (PLS) transitions: <table> <thead> <tr> <th>Transition</th> <th>Condition</th> </tr> </thead> <tbody> <tr> <td>U3 -&gt; Resume</td> <td>Wakeup signaling from a device</td> </tr> <tr> <td>Resume -&gt; Recovery -&gt; U0</td> <td>Device Resume complete (USB 3.0 capable ports only)</td> </tr> <tr> <td>Resume -&gt; U0</td> <td>Device Resume complete (USB 2.0 capable-only ports)</td> </tr> <tr> <td>U3 -&gt; Recovery -&gt; U0</td> <td>Software Resume complete (USB 3.0 capable ports only)</td> </tr> <tr> <td>U3 -&gt; U0</td> <td>Software Resume complete (USB 2.0 capable-only ports)</td> </tr> <tr> <td>U2 -&gt; U0</td> <td>L1 Resume complete (USB 2.0 capable-only ports)</td> </tr> <tr> <td>U0 -&gt; U0</td> <td>L1 Entry Reject (USB 2.0 capable-only ports)</td> </tr> <tr> <td>U0 -&gt; Disabled</td> <td>L1 Entry Error (USB 2.0 capable-only ports)</td> </tr> <tr> <td>Any state -&gt; Inactive</td> <td>Error (USB 3.0 capable ports only)</td> </tr> </tbody> </table> <b>Notes:</b> 1. This bit shall not be set if the PLS transition was due to software setting the PP bit to 0b. 2. Software shall clear this bit by writing a 1 to it.	Transition	Condition	U3 -> Resume	Wakeup signaling from a device	Resume -> Recovery -> U0	Device Resume complete (USB 3.0 capable ports only)	Resume -> U0	Device Resume complete (USB 2.0 capable-only ports)	U3 -> Recovery -> U0	Software Resume complete (USB 3.0 capable ports only)	U3 -> U0	Software Resume complete (USB 2.0 capable-only ports)	U2 -> U0	L1 Resume complete (USB 2.0 capable-only ports)	U0 -> U0	L1 Entry Reject (USB 2.0 capable-only ports)	U0 -> Disabled	L1 Entry Error (USB 2.0 capable-only ports)	Any state -> Inactive	Error (USB 3.0 capable ports only)
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21	<b>Port Reset Change (PRC)</b> —R/WC. This flag is set to '1' due a '1'-to-'0' transition of Port Reset (PR); for example, when any reset processing on this port is complete. 0 = No change 1 = Reset Complete <b>Notes:</b> 1. This bit shall not be set to 1b if the reset processing was forced to terminate due to software clearing the PP bit or PED bit to 0b. 2. Software shall clear this bit by writing a 1 to it.																				
20	<b>Over-current Change (OCC)</b> —R/WC. The functionality of this bit is not dependent upon the port owner. Software clears this bit by writing a 1 to it. 0 = No change. (Default) 1 = There is a change to Overcurrent Active.																				
19	<b>Warm Port Reset Change (WRC)</b> —R/WC. This bit is set when Warm Reset processing on this port completes. 0 = No change. (Default) 1 = Warm reset complete. <b>Notes:</b> 1. This bit shall not be set to 1b if the reset processing was forced to terminate due to software clearing the PP bit or PED bit to 0b. 2. Software shall clear this bit by writing a 1 to it. 3. This bit applies only to USB 3.0 capable ports. This bit is Reserved for USB 2.0 capable-only ports.																				



Bit	Description				
18	<p><b>Port Enabled/Disabled Change (PEC)</b>—R/WC</p> <p>0 = No change. (Default) 1 = There is a change to PED bit.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This bit shall not be set if the PED transition was due to software setting the PP bit to 0.</li> <li>2. Software shall clear this bit by writing a 1 to it.</li> <li>3. For a USB 2.0-only port, this bit shall be set to 1 only when the port is disabled due to the appropriate conditions existing at the EOF2 point. (See Chapter 11 of the USB Specification for the definition of a port error).</li> <li>4. For a USB 3.0 port, this bit shall be set to '1' if an enabled port transitions to a Disabled state (that is, a '1'-to-'0' transition of PED). Refer to section 4 of the xHCI Specification for more information.</li> </ol>				
17	<p><b>Connect Status Change (CSC)</b>—R/WC. This flag indicates a change has occurred in the port's Current Connect Status (CCS) or Cold Attach Status (CAS) bits.</p> <p>0 = No change. (Default) 1 = There is a change to the CCS or CAS bit.</p> <p>The xHC sets this bit to 1b for all changes to the port device connect status, even if system software has not cleared an existing Connect Status Change. For example, the insertion status changes twice before system software has cleared the changed condition, root hub hardware will be "setting" an already-set bit (that is, the bit will remain 1b).</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This bit shall not be set if the CCS transition was due to software setting the PP bit to 0b, or the CAS bit transition was due to software setting the WPR bit to 1b.</li> <li>2. Software shall clear this bit by writing a 1 to it.</li> </ol>				
16	<p><b>Port Link State Write Strobe (LWS)</b>—R/W</p> <p>0 = When 0b, write data in PLS field is ignored. (Default) 1 = When this bit is set to 1b on a write reference to this register, this flag enables writes to the PLS field.</p> <p>Reads to this bit return '0'.</p>				
15:14	Reserved.				
13:10	<p><b>Port Speed (Port_Speed)</b>—RO</p> <p>A device attached to this port operates at a speed defined by the following codes:</p> <table> <thead> <tr> <th>Value</th> <th>Speed</th> </tr> </thead> <tbody> <tr> <td>0100b</td> <td>SuperSpeed (5Gb/s)</td> </tr> </tbody> </table> <p>All other values reserved. Refer to the <i>eXtensible Host Controller Interface for Universal Serial Bus Specification</i> for additional details.</p>	Value	Speed	0100b	SuperSpeed (5Gb/s)
Value	Speed				
0100b	SuperSpeed (5Gb/s)				
9	<b>Port Power (PP)</b> —RO. Read-only with a value of 1. This indicates that the port does have power.				

Bit	Description																																												
8:5	<p><b>Port Link State (PLS)</b>—R/W. This field is used to power manage the port and reflects its current link state.</p> <p>When the port is in the Enabled state, system software may set the link U-state by writing this field. System software may also write this field to force a Disabled to Disconnected state transition of the port.</p> <table> <thead> <tr> <th>Write Value</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0</td><td>The link shall transition to a U0 state from any of the U-states.</td></tr> <tr> <td>2</td><td>USB 2.0 ports only. The link should transition to the U2 State.</td></tr> <tr> <td>3</td><td>The link shall transition to a U3 state from any of the U-states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port.</td></tr> <tr> <td>5</td><td>USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored.</td></tr> <tr> <td>15</td><td>USB 2.0 ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored.</td></tr> <tr> <td>All other values</td><td>Ignored</td></tr> </tbody> </table> <p><b>Note:</b> The Port Link State Write Strobe (LWS) shall be set to 1b to write this field.</p> <table> <thead> <tr> <th>Read Value</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>0</td><td>Link is in the U0 State</td></tr> <tr> <td>1</td><td>Link is in the U1 State</td></tr> <tr> <td>2</td><td>Link is in the U2 State</td></tr> <tr> <td>3</td><td>Link is in the U3 State (Device Suspended)</td></tr> <tr> <td>4</td><td>Link is in the Disabled State</td></tr> <tr> <td>5</td><td>Link is in the RxDetect State</td></tr> <tr> <td>6</td><td>Link is in the Inactive State</td></tr> <tr> <td>7</td><td>Link is in the Polling State</td></tr> <tr> <td>8</td><td>Link is in the Recovery State</td></tr> <tr> <td>9</td><td>Link is in the Hot Reset State</td></tr> <tr> <td>10</td><td>Link is in the Compliance Mode State</td></tr> <tr> <td>11</td><td>Link is in the Test Mode State</td></tr> <tr> <td>12–14</td><td>Reserved</td></tr> <tr> <td>15</td><td>Link is in the Resume State</td></tr> </tbody> </table> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This field is undefined if PP = 0.</li> <li>2. Transitions between different states are not reflected until the transition is complete.</li> </ol>	Write Value	Description	0	The link shall transition to a U0 state from any of the U-states.	2	USB 2.0 ports only. The link should transition to the U2 State.	3	The link shall transition to a U3 state from any of the U-states. This action selectively suspends the device connected to this port. While the Port Link State = U3, the hub does not propagate downstream-directed traffic to this port, but the hub will respond to resume signaling from the port.	5	USB 3.0 ports only. If the port is in the Disabled state (PLS = Disabled, PP = 1), then the link shall transition to a RxDetect state and the port shall transition to the Disconnected state, else ignored.	15	USB 2.0 ports only. If the port is in the U3 state (PLS = U3), then the link shall remain in the U3 state and the port shall transition to the U3Exit substate, else ignored.	All other values	Ignored	Read Value	Definition	0	Link is in the U0 State	1	Link is in the U1 State	2	Link is in the U2 State	3	Link is in the U3 State (Device Suspended)	4	Link is in the Disabled State	5	Link is in the RxDetect State	6	Link is in the Inactive State	7	Link is in the Polling State	8	Link is in the Recovery State	9	Link is in the Hot Reset State	10	Link is in the Compliance Mode State	11	Link is in the Test Mode State	12–14	Reserved	15	Link is in the Resume State
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12–14	Reserved																																												
15	Link is in the Resume State																																												
4	<p><b>Port Reset (PR)</b>—R/W. When software writes a 1 to this bit (from a 0), the bus reset sequence as defined in the USB Specification, Revision 2.0 is started. Software writes a 0 to this bit to terminate the bus reset sequence. Software must keep this bit at a 1 long enough to ensure the reset sequence completes as specified in the USB Specification, Revision 2.0. USB 3.0 ports shall execute the Hot Reset sequence as defined in the USB 3.0 Specification. PR remains set until reset signaling is completed by the root hub.</p> <p>1 = Port is in Reset. 0 = Port is not in Reset.</p>																																												
3	<p><b>Overcurrent Active (OCA)</b>—RO.</p> <p>0 = This port does not have an overcurrent condition. (Default)</p> <p>1 = This port currently has an overcurrent condition. This bit will automatically transition from 1 to 0 when the overcurrent condition is removed. The PCH automatically disables the port when the overcurrent active bit is 1.</p>																																												
2	Reserved.																																												

Bit	Description
1	<b>Port Enabled/Disabled</b> —R/W. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this bit. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. 0 = Disable. 1 = Enable. (Default)
0	<b>Current Connect Status</b> —RO. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. 0 = No device is present. (Default) 1 = Device is present on port.

### 13.2.2.13 PORTPMSCN—Port N Power Management Status and Control USB3 Register

Offset: There are 4 USB 3.0 PORTPMSCN registers at offsets: 534h, 544h, 554h, 564h

Attribute: R/W, RO

Default Value: 00000000h

Size: 32 bits

Bit	Description																
31:17	Reserved																
16	<b>Force Link PM Accept (FLA)</b> —R/W. When this bit is set to '1', the port shall generate a Set Link Function LMP with the Force_LinkPM_Accept bit asserted. This bit shall be set to 0b by the assertion of PR to 1 or when CCS = transitions from 0 to 1. Writes to this flag have no affect if PP = 0b. The Set Link Function LMP is sent by the xHC to the device connected on this port when this bit transitions from 0 to 1. Refer to Sections 8.4.1, 10.4.2.2 and 10.4.2.9 of the USB 3.0 Specification for more details.																
15:8	<b>U2 Timeout</b> —R/W. Timeout value for U2 inactivity timer. If equal to FFh, the port is disabled from initiating U2 entry. This field shall be set to 0 by the assertion of PR to 1. Refer to section 4 of the xHCI Specification for more information on U2 Timeout operation. The following are permissible values: <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Zero (default)</td> </tr> <tr> <td>01h</td> <td>256 µs</td> </tr> <tr> <td>02h</td> <td>512 µs</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>FEh</td> <td>65.024 ms</td> </tr> <tr> <td>FFh</td> <td>Infinite</td> </tr> </tbody> </table>	Value	Description	00h	Zero (default)	01h	256 µs	02h	512 µs	...		FEh	65.024 ms	FFh	Infinite		
Value	Description																
00h	Zero (default)																
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02h	512 µs																
...																	
FEh	65.024 ms																
FFh	Infinite																
7:0	<b>U1 Timeout</b> —R/W. Timeout value for U1 inactivity timer. If equal to FFh, the port is disabled from initiating U1 entry. This field shall be set to 0 by the assertion of PR to 1. Refer to section 4 of the xHCI Specification for more information on U1 Timeout operation. The following are permissible values. <table> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Zero (default)</td> </tr> <tr> <td>01h</td> <td>1 µs</td> </tr> <tr> <td>02h</td> <td>2 µs</td> </tr> <tr> <td>...</td> <td></td> </tr> <tr> <td>7Fh</td> <td>127 µs</td> </tr> <tr> <td>80h-FEh</td> <td>Reserved</td> </tr> <tr> <td>FFh</td> <td>Infinite</td> </tr> </tbody> </table>	Value	Description	00h	Zero (default)	01h	1 µs	02h	2 µs	...		7Fh	127 µs	80h-FEh	Reserved	FFh	Infinite
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01h	1 µs																
02h	2 µs																
...																	
7Fh	127 µs																
80h-FEh	Reserved																
FFh	Infinite																

### 13.2.2.14 PORTLIX—USB 3.0 Port X Link Info Register

Offset: There are 4 USB3 PORTLIX registers at offsets: 578h, 588h, 598h, 5A8h  
Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:16	Reserved
15:0	<b>Link Error Count</b> —RO.

## 13.2.3 Host Controller Runtime Registers

This section defines the xHC runtime registers. The base address of this register space is referred to as Runtime Base. The Runtime Base shall be 32-byte aligned and is calculated by adding the value Runtime Register Space Offset register (MEM\_BASE+18h:bits 31:2) to the Capability Base address. All Runtime registers are multiples of 32 bits in length.

**Table 13-4. Host Controller Runtime Register Address Map**

Runtime Base + Offset	Mnemonic	Register Name	Default	Type
00h-03h	MFINDEX	Microframe Index	00000000h	RO
20h-23h	IMAN	Interrupter X Management	00000000h	RO, R/W, R/WC
24h-27h	IMOD	Interrupter X Moderation	00000FA0h	R/W
28h-2Bh	ERSTSZ	Event Ring Segment Table Size X	00000000h	R/W, RO
30h-33h	ERSTBAL	Event Ring Segment Table Base Address Low X	00000000h	R/W, RO
34h-37h	ERSTBAH	Event Ring Segment Table Base Address High X	00000000h	R/W
38h-3Bh	ERDPL	Event Ring Dequeue Pointer Low X	00000000h	R/W, R/WC
3Ch-3Fh	ERDPH	Event Ring Dequeue Pointer High X	00000000h	R/W

### 13.2.3.1 MFINDEX—Microframe Index Register

Offset: Runtime Base + 00h-03h Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:14	Reserved
13:0	<b>Microframe Index</b> —RO. The value in this register increments at the end of each micro-frame (for example, 125 µs). Bits 13:3 may be used to determine the current 1 ms. Frame Index.

### 13.2.3.2 IMAN—Interrupter X Management Register

Offset:                    Interrupter 1: Runtime Base + 20h-23h  
                           Interrupter 2: Runtime Base + 40h-43h  
                           Interrupter 3: Runtime Base + 60h-63h  
                           Interrupter 4: Runtime Base + 80h-83h  
                           Interrupter 5: Runtime Base + A0h-A3h  
                           Interrupter 6: Runtime Base + C0h-C3h  
                           Interrupter 7: Runtime Base + E0h-E3h  
                           Interrupter 8: Runtime Base + 100h-103h

Attribute:            RO, R/WC  
 Default Value:        00000000h                            Size:            32 bits

**Note:** The xHC implements up to 8 Interrupters. There are 8 IMAN registers, one for each Interrupter.

Bit	Description
31:2	Reserved.
1	<b>Interrupt Enable (IE)</b> —RO. This flag specifies whether the Interrupter is capable of generating an interrupt. 0 = The Interrupter is prohibited from generating interrupts. 1 = When this bit and the IP bit are set (1b), the Interrupter shall generate an interrupt when the Interrupter Moderation Counter reaches 0.
0	<b>Interrupt Pending (IP)</b> —R/WC. 0 = No interrupt is pending for the Interrupter. 1 = An interrupt is pending for this Interrupter. This bit is set to 1b when IE = 1, the IMODI Interrupt Moderation Counter field = 0b, the Event Ring associated with the Interrupter is not empty (or for the Primary Interrupter when the HCE flag is set to 1b), and EHB = 0. If MSI interrupts are enabled, this flag shall be cleared automatically when the PCI DWord write generated by the Interrupt assertion is complete. If PCI Pin Interrupts are enabled, this flag shall be cleared by software.

### 13.2.3.3 IMOD—Interrupter X Moderation Register

Offset:                    Interrupter 1: Runtime Base + 24h-27h  
                           Interrupter 2: Runtime Base + 44h-47h  
                           Interrupter 3: Runtime Base + 64h-67h  
                           Interrupter 4: Runtime Base + 84h-87h  
                           Interrupter 5: Runtime Base + A4h-A7h  
                           Interrupter 6: Runtime Base + C4h-C7h  
                           Interrupter 7: Runtime Base + E4h-E7h  
                           Interrupter 8: Runtime Base + 104h-107h

Attribute:            R/W  
                           Default Value: 00000FA0h                            Size: 32 bits

**Note:** The xHC implements up to 8 Interrupters. There are 8 IMOD registers, one for each Interrupter.

Bit	Description
31:16	<b>Interrupt Moderation Counter (IMODC)</b> —R/W. Down counter. Loaded with Interval Moderation value—value of bits 15:0, whenever the IP bit is cleared to 0b, counts down to '0', and stops. The associated interrupt shall be signaled whenever this counter is '0', the Event Ring is not empty, the IE and IP bits = 1, and EHB = 0. This counter may be directly written by software at any time to alter the interrupt rate.
15:0	<b>Interrupt Moderation Interval (IMODI)</b> —R/W. Minimum inter-interrupt interval. The interval is specified in 250 ns increments. A value of '0' disables interrupt throttling logic and interrupts shall be generated immediately if IP = 0, EHB = 0, and the Event Ring is not empty.

### 13.2.3.4 ERSTSZ—Event Ring Segment Table Size X Register

Offset:                    1: Runtime Base + 28h-2Bh  
                           2: Runtime Base + 48h-4Bh  
                           3: Runtime Base + 68h-6Bh  
                           4: Runtime Base + 88h-8Bh  
                           5: Runtime Base + A8h-ABh  
                           6: Runtime Base + C8h-CBh  
                           7: Runtime Base + E8h-EBh  
                           8: Runtime Base + 108h-10Bh

Attribute:            R/W, RO  
                           Default Value: 00000000h                            Size: 32 bits

**Note:** There are 8 ERSTSZ registers.

Bit	Description
31:16	Reserved
15:0	<b>Event Ring Segment Table Size</b> —R/W. This field identifies the number of valid Event Ring Segment Table entries in the Event Ring Segment Table pointed to by the Event Ring Segment Table Base Address register.

### 13.2.3.5 ERSTBAL—Event Ring Segment Table Base Address Low X Register

Offset:	1: Runtime Base + 30h-33h 2: Runtime Base + 50h-53h 3: Runtime Base + 70h-73h 4: Runtime Base + 90h-93h 5: Runtime Base + B0h-B3h 6: Runtime Base + D0h-D3h 7: Runtime Base + F0h-F3h 8: Runtime Base + 110h-113h
Attribute:	R/W, RO
Default Value:	00000000h
Size:	32 bits

**Note:** There are 8 ERSTBAL registers.

Bit	Description
31:6	<b>Event Ring Segment Table Base Address Register (ERSTBA_LO)</b> —R/W. This field defines the low-order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.
5:0	Reserved

### 13.2.3.6 ERSTBAH—Event Ring Segment Table Base Address High X Register

Offset:	1: Runtime Base + 34h-37h 2: Runtime Base + 54h-57h 3: Runtime Base + 74h-77h 4: Runtime Base + 94h-97h 5: Runtime Base + B4h-B7h 6: Runtime Base + D4h-D7h 7: Runtime Base + F4h-F7h 8: 1Runtime Base + 14h-117h
Attribute:	R/W
Default Value:	00000000h
Size:	32 bits

**Note:** There are 8 ERSTBAH registers.

Bit	Description
31:0	<b>Event Ring Segment Table Base Address Register (ERSTBA_HI)</b> —R/W. This field defines the low-order bits of the start address of the Event Ring Segment Table. This field shall not be modified if HCHalted (HCH) = 0.

### 13.2.3.7 ERDPL—Event Ring Dequeue Pointer Low X Register

Offset: 1: Runtime Base + 38h-3Bh  
2: Runtime Base + 58h-5Bh  
3: Runtime Base + 78h-7Bh  
4: Runtime Base + 98h-9Bh  
5: Runtime Base + B8h-BBh  
6: Runtime Base + D8h-DBh  
7: Runtime Base + F8h-FBh  
8: Runtime Base + 118h-11Bh

Attribute: R/W, R/WC  
Default Value: 00000000h Size: 32 bits

**Note:** There are 8 ERDPL registers.

Bit	Description
31:4	<b>Event Ring Dequeue Pointer</b> —R/W. This field defines the low-order bits of the 64-bit address of the current Event Ring Dequeue Pointer.
3	<b>Event Handler Busy (EHB)</b> —R/WC. This flag shall be set to '1' when the IP bit is set to '1' and cleared to '0' by software when the Dequeue Pointer register is written.
2:0	<b>Dequeue ERST Segment Index (DESI)</b> —R/W. This field may be used by the xHC to accelerate checking the Event Ring full condition. This field is written with the low-order 3 bits of the offset of the ERST entry that defines the Event Ring segment that Event Ring Dequeue Pointer resides in.

### 13.2.3.8 ERDPH—Event Ring Dequeue Pointer High X Register

Offset: 1: Runtime Base + 3Ch-3Fh  
2: Runtime Base + 5Ch-5Fh  
3: Runtime Base + 7Ch-7Fh  
4: Runtime Base + 9Ch-9Fh  
5: Runtime Base + BCh-BFh  
6: Runtime Base + DCh-DFh  
7: Runtime Base + FCh-FFh  
8: Runtime Base + 11Ch-11Fh

Attribute: R/W  
Default Value: 00000000h Size: 32 bits

**Note:** There are 8 ERDPH registers.

Bit	Description
31:0	<b>Event Ring Dequeue Pointer</b> —R/W. This field defines the low-order bits of the 64-bit address of the current Event Ring Dequeue Pointer.



## 13.2.4 Doorbell Registers

Door Bell registers are an array of 64 registers, with 0 to 32 being used by the xHC and the remainder being reserved. One 32-bit Doorbell Register is defined in the array for each Device Slot. System software uses the Doorbell Register to notify the xHC that it has Device Slot related work for the xHC to perform.

These registers are pointed to by the Doorbell Offset Register (DBOFF) in the xHC Capability register space. The Doorbell Array base address shall be DWord aligned and is calculated by adding the value in the DBOFF register (MEM\_BASE+14h-17h) to "Base" (the base address of the xHCI Capability register address space).

All registers are 32 bits in length. Software should read and write these registers using only DWord accesses.

### 13.2.4.1 DOORBELL—Doorbell X Register

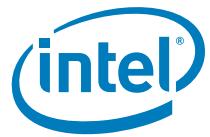
Offset:                   Doorbell 1: DBOFF + 00h-03h  
                          Doorbell 2: DBOFF + 04h-07h  
                          ....  
                          Doorbell 32: DBOFF + 7Ch-7Fh

Attribute:           R/W, RO  
                          Default Value: 00000000h                   Size: 32 bits

**Note:** There are 32 contiguous DOORBELL registers.

Bit	Description
31:16	<b>DB Stream ID</b> —R/W. If the endpoint of a Device Context Doorbell defines Streams, then this field shall be used to identify which Stream of the endpoint the doorbell reference is targeting. System software is responsible for ensuring that the value written to this field is valid. If the endpoint does not define Streams (MaxPStreams = 0) and a non-'0' value is written to this field, the doorbell reference shall be ignored. This field only applies to Device Context Doorbells and shall be cleared to '0' for Host Controller Commands. This field returns '0' when read.
15:8	Reserved
7:0	<b>DB Target</b> —R/W. This field defines the target of the doorbell reference. The table below defines the xHC notification that is generated by ringing the doorbell. Doorbell Register 0 is dedicated to Command Ring and decodes this field differently than the other Doorbell Registers. Refer to the xHCI Specification for definitions of the values.

§ §





# 14 Integrated Intel® High Definition Audio (Intel® HD Audio) Controller Registers

## 14.1 Intel® High Definition Audio (Intel® HD Audio) Controller Registers (D27:F0)

The Intel® High Definition Audio controller resides in PCI Device 27, Function 0 on bus 0. This function contains a set of DMA engines that are used to move samples of digitally encoded data between system memory and external codecs.

**Note:** All registers in this function (including memory-mapped registers) are addressable in byte, word, and DWord quantities. The software must always make register accesses on natural boundaries (that is, DWord accesses must be on DWord boundaries; word accesses—on word boundaries, and so on). Register accesses crossing the DWord boundary are ignored. In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the Intel® High Definition Audio memory-mapped space, the results are undefined.

**Note:** Users interested in providing feedback on the Intel® High Definition Audio specification or planning to implement the Intel® High Definition Audio specification into a future product will need to execute the *Intel® High Definition Audio Specification Developer's Agreement*. For more information, contact [nextgenaudio@intel.com](mailto:nextgenaudio@intel.com).

### 14.1.1 Intel® High Definition Audio (Intel® HD Audio) PCI Configuration Space (Intel® High Definition Audio—D27:F0)

**Note:** Address locations that are not shown should be treated as Reserved.

**Table 14-1. Intel® High Definition Audio (Intel® HD Audio) PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	03h	RO
0Bh	BCC	Base Class Code	04h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	LT	Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO

**Table 14-1. Intel® High Definition Audio (Intel® HD Audio) PCI Register Address Map (Intel® High Definition Audio D27:F0) (Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
10h-13h	HDBARL	Intel® High Definition Audio Lower Base Address (Memory)	00000004h	R/W, RO
14h-17h	HDBARU	Intel® High Definition Audio Upper Base Address (Memory)	00000000h	R/W
2Ch-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAPPTR	Capability List Pointer	50h	RO
3Ch	INTLN	Interrupt Line	00h	R/W
3Dh	INTPN	Interrupt Pin	See Register Description	RO
40h	HDCTL	Intel® High Definition Audio Control	01h	R/W, RO
4Ch	DCKCTL	Docking Control (Mobile Only)	00h	R/W, RO
4Dh	DCKSTS	Docking Status (Mobile Only)	80h	R/WO, RO
50h-51h	PID	PCI Power Management Capability ID	6001h	R/WO, RO
52h-53h	PC	Power Management Capabilities	C842h	RO
54h-57h	PCS	Power Management Control and Status	00000000h	R/W, RO, R/WC
60h-61h	MID	MSI Capability ID	7005h	RO
62h-63h	MMC	MSI Message Control	0080h	R/W, RO
64h-67h	MMLA	MSI Message Lower Address	00000000h	R/W, RO
68h-6Bh	MMUA	MSI Message Upper Address	00000000h	R/W
6Ch-6Dh	MMD	MSI Message Data	0000h	R/W
70h-71h	PXID	PCI Express® Capability Identifiers	0010h	RO
72h-73h	PXC	PCI Express® Capabilities	0091h	RO
74h-77h	DEVCAP	Device Capabilities	10000000h	RO, R/WO
78h-79h	DEVC	Device Control	0800h	R/W, RO
7Ah-7Bh	DEVS	Device Status	0010h	RO
100h-103h	VCCAP	Virtual Channel Enhanced Capability Header	13010002h	R/WO
104h-107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO
108h-10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10Ch-10D	PVCCTL	Port VC Control	0000h	RO
10Eh-10Fh	PVCSTS	Port VC Status	0000h	RO
110h-113h	VC0CAP	VC0 Resource Capability	00000000h	RO
114h-117h	VC0CTL	VC0 Resource Control	800000FFh	R/W, RO
11Ah-11Bh	VC0STS	VC0 Resource Status	0000h	RO
11Ch-11Fh	VCiCAP	VCi Resource Capability	00000000h	RO
120h-123h	VCiCTL	VCi Resource Control	00000000h	R/W, RO
126h-127h	VCiSTS	VCi Resource Status	0000h	RO
130h-133h	RCCAP	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
134h-137h	ESD	Element Self Description	0F000100h	RO
140h-143h	L1DESC	Link 1 Description	00000001h	RO
148h-14Bh	L1ADDL	Link 1 Lower Address	See Register Description	RO
14Ch-14Fh	L1ADDU	Link 1 Upper Address	00000000h	RO



#### 14.1.1.1 VID—Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0)

Offset: 00h–01h Attribute: RO  
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

#### 14.1.1.2 DID—Device Identification Register (Intel® High Definition Audio Controller—D27:F0)

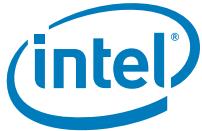
Offset Address: 02h–03h Attribute: RO  
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH's Intel® High Definition Audio controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

#### 14.1.1.3 PCICMD—PCI Command Register (Intel® High Definition Audio Controller—D27:F0)

Offset Address: 04h–05h Attribute: R/W, RO  
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable (ID)</b> —R/W 0 = The INTx# signals may be asserted. 1 = The Intel® High Definition Audio controller's INTx# signal will be de-asserted.  <b>Note:</b> This bit does not affect the generation of MSIs.
9	<b>Fast Back to Back Enable (FBE)</b> —RO. Hardwired to 0.
8	<b>SERR# Enable (SERR_EN)</b> —R/W. SERR# is not generated by the PCH Intel® High Definition Audio Controller.
7	<b>Wait Cycle Control (WCC)</b> —RO. Hardwired to 0.
6	<b>Parity Error Response (PER)</b> —R/W. PER functionality, not implemented.
5	<b>VGA Palette Snoop (VPS)</b> —RO. Hardwired to 0.
4	<b>Memory Write and Invalidate Enable (MWIE)</b> —RO. Hardwired to 0.
3	<b>Special Cycle Enable (SCE)</b> —RO. Hardwired to 0.
2	<b>Bus Master Enable (BME)</b> —R/W. Controls standard PCI Express* bus mastering capabilities for Memory and I/O, reads and writes. This bit also controls MSI generation since MSIs are essentially Memory writes. 0 = Disable 1 = Enable
1	<b>Memory Space Enable (MSE)</b> —R/W. Enables memory space addresses to the Intel® High Definition Audio controller. 0 = Disable 1 = Enable
0	<b>I/O Space Enable (IOSE)</b> —RO. Hardwired to 0 since the Intel® High Definition Audio controller does not implement I/O space.



#### 14.1.1.4 PCISTS—PCI Status Register (Intel® High Definition Audio Controller—D27:F0)

Offset Address: 06h–07h Attribute: RO, R/WC  
Default Value: 0010h Size: 16 bits

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —RO. Hardwired to 0.
14	<b>SERR# Status (SERRS)</b> —RO. Hardwired to 0.
13	<b>Received Master Abort (RMA)</b> —R/WC. Software clears this bit by writing a 1 to it. 0 = No master abort received. 1 = The Intel® High Definition Audio controller sets this bit when, as a bus master, it receives a master abort. When set, the Intel® High Definition Audio controller clears the run bit for the channel that received the abort.
12	<b>Received Target Abort (RTA)</b> —RO. Hardwired to 0.
11	<b>Signaled Target Abort (STA)</b> —RO. Hardwired to 0.
10:9	<b>DEVSEL# Timing Status (DEV_STS)</b> —RO. Hardwired to 0.
8	<b>Data Parity Error Detected (DPED)</b> —RO. Hardwired to 0.
7	<b>Fast Back to Back Capable (FB2BC)</b> —RO. Hardwired to 0.
6	Reserved
5	<b>66 MHz Capable (66 MHZ_CAP)</b> —RO. Hardwired to 0.
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 1. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	<b>Interrupt Status (IS)</b> —RO. 0 = This bit is 0 after the interrupt is cleared. 1 = This bit is 1 when the INTx# is asserted. This bit is not set by an MSI.
2:0	Reserved

#### 14.1.1.5 RID—Revision Identification Register (Intel® High Definition Audio Controller—D27:F0)

Offset: 08h Attribute: RO  
Default Value: See bit description Size: 8 Bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See Section 1.4 for the value of the RID Register.

#### 14.1.1.6 PI—Programming Interface Register (Intel® High Definition Audio Controller—D27:F0)

Offset: 09h Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Programming Interface</b> —RO

### 14.1.1.7 SCC—Sub Class Code Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Ah Attribute: RO  
Default Value: 03h Size: 8 bits

Bit	Description
7:0	<b>Sub Class Code (SCC)</b> —RO 03h = Audio Device

#### 14.1.1.8 BCC—Base Class Code Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Bh Attribute: RO  
Default Value: 04h Size: 8 bits

Bit	Description
7:0	<b>Base Class Code (BCC)</b> —RO 04h = Multi-media device

#### 14.1.1.9 CLS—Cache Line Size Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Ch Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Cache Line Size</b> —R/W. Implemented as R/W register, but has no functional impact to the PCH

#### 14.1.1.10 LT—Latency Timer Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Dh Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Latency Timer</b> —RO. Hardwired to 00

#### 14.1.1.11 HEADTYP—Header Type Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 0Eh Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Header Type</b> —RO. Hardwired to 00.

#### 14.1.1.12 HDBARL—Intel® High Definition Audio Lower Base Address Register (Intel® High Definition Audio—D27:F0)

Address Offset: 10h–13h      Attribute: R/W, RO  
 Default Value: 00000004h      Size: 32 bits

Bit	Description
31:14	<b>Lower Base Address (LBA)</b> —R/W. Base address for the Intel® High Definition Audio controller’s memory-mapped configuration registers. 16 Kbytes are requested by hardwiring bits 13:4 to 0s.
13:4	Reserved
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0 to indicate that this BAR is NOT prefetchable
2:1	<b>Address Range (ADDRNG)</b> —RO. Hardwired to 10b, indicating that this BAR can be located anywhere in 64-bit address space.
0	<b>Space Type (SPTYP)</b> —RO. Hardwired to 0. Indicates this BAR is located in memory space.

#### 14.1.1.13 HDBARU—Intel® High Definition Audio Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 14h–17h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Upper Base Address (UBA)</b> —R/W. Upper 32 bits of the Base address for the Intel® High Definition Audio controller’s memory-mapped configuration registers.

#### 14.1.1.14 SVID—Subsystem Vendor Identification Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 2Ch–2Dh      Attribute: R/WL  
 Default Value: 0000h      Size: 16 bits  
 Function Level Reset: No

The SVID register, in combination with the Subsystem ID register (D27:F0:2Eh), enable the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

Bit	Description
15:0	<b>Subsystem Vendor ID</b> —R/WL. Locked when HDCTL.BCLD = 1.



#### 14.1.1.15 SID—Subsystem Identification Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 2Eh–2Fh Attribute: R/WO  
 Default Value: 0000h Size: 16 bits  
 Function Level Reset: No

The SID register, in combination with the Subsystem Vendor ID register (D27:F0:2Ch) make it possible for the operating environment to distinguish one audio subsystem from the other(s).

This register is implemented as write-once register. Once a value is written to it, the value can be read back. Any subsequent writes will have no effect.

This register is not affected by the D3<sub>HOT</sub> to D0 transition.

Bit	Description
15:0	<b>Subsystem ID</b> —R/WL Locked when HDCTL.BCLD = 1.

#### 14.1.1.16 CAPPTR—Capabilities Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 34h Attribute: RO  
 Default Value: 50h Size: 8 bits

This register indicates the offset for the capability pointer.

Bit	Description
7:0	<b>Capabilities Pointer (CAP_PTR)</b> —RO. This field indicates that the first capability pointer offset is offset 50h (Power Management Capability).

#### 14.1.1.17 INTLN—Interrupt Line Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 3Ch Attribute: R/W  
 Default Value: 00h Size: 8 bits  
 Function Level Reset: No

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is used to communicate to software the interrupt line that the interrupt pin is connected to.



#### 14.1.1.18 INTPN—Interrupt Pin Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 3Dh Attribute: RO  
Default Value: See Description Size: 8 bits

Bit	Description
7:4	Reserved
3:0	<b>Interrupt Pin (IP)</b> —RO. This reflects the value of D27IP.ZIP (Chipset Configuration Registers:Offset 3110h:bits 3:0).

#### 14.1.1.19 HDCTL—Intel® High Definition Audio Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 40h Attribute: RO, R/WO  
Default Value: 01h Size: 8 bits

Bit	Description
7:2	Reserved
1	<b>BIOS Configuration Lock Down Bit (BCLD)</b> —R/WO. This bit being set is an indication that BIOS configuration is done and Intel® HD Audio Controller hardware can start operations using the defined configurations. Setting this bit also locks down the read only field that BIOS initialized.
0	<b>Intel® High Definition Signal Mode</b> —RO. This bit is hardwired to 1 (Intel High Definition Audio mode).

#### 14.1.1.20 DCKCTL—Docking Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 4Ch Attribute: R/W, RO  
Default Value: 00h Size: 8 bits  
Function Level Reset: No

Bit	Description
7:1	Reserved
0	<b>Dock Attach (DA)</b> —R/W/RO. Software writes a 1 to this bit to initiate the docking sequence on the HDA_DOCK_EN# and HDA_DOCK_RST# signals. When the docking sequence is complete, hardware will set the Dock Mated (GSTS.DM) status bit to 1. Software writes a 0 to this bit to initiate the undocking sequence on the HDA_DOCK_EN# and HDA_DOCK_RST# signals. When the undocking sequence is complete, hardware will set the Dock Mated (GSTS.DM) status bit to 0. Software must check the state of the Dock Mated (GSTS.DM) bit prior to writing to the Dock Attach bit. Software shall only change the DA bit from 0 to 1 when DM=0. Likewise, software shall only change the DA bit from 1 to 0 when DM=1. If these rules are violated, the results are undefined. This bit is read-only when the DCKSTS.DS bit = 0.



#### 14.1.1.21 DCKSTS—Docking Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 4Dh Attribute: R/WL, RO  
 Default Value: 80h Size: 8 bits  
 Function Level Reset: No

Bit	Description
7	<b>Docking Supported (DS)</b> —R/WL. A, 1 indicates that the PCH supports HD Audio Docking. The DCKCTL.DA bit is only writable when this DS bit is 1. ACPI BIOS software should only branch to the docking routine when this DS bit is 1. BIOS may clear this bit to 0 to prohibit the ACPI BIOS software from attempting to run the docking routines. This bit is reset to its default value only on a PLTRST#, but not on a CRST# or D3 <sub>HOT</sub> -to-D0 transition. Locked when HDCTL.BCLD = 1.
6:1	Reserved
0	<b>Dock Mated (DM)</b> —RO. This bit effectively communicates to software that an Intel® HD Audio docked codec is physically and electrically attached. Controller hardware sets this bit to 1 after the docking sequence triggered by writing a 1 to the Dock Attach (GCTL.DA) bit is completed (HDA_DOCK_RST# de-assertion). This bit indicates to software that the docked codec(s) may be discovered using the STATESTS register and then enumerated. Controller hardware sets this bit to 0 after the undocking sequence triggered by writing a 0 to the Dock Attach (GCTL.DA) bit is completed (HDA_DOCK_EN# de-asserted). This bit indicates to software that the docked codec(s) may be physically undocked.

#### 14.1.1.22 PID—PCI Power Management Capability ID Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 50h–51h Attribute: R/WL, RO  
 Default Value: 6001h Size: 16 bits  
 Function Level Reset: No (Bits 7:0 only)

Bit	Description
15:8	<b>Next Capability (Next)</b> —R/WL. Points to the next capability structure (MSI). Locked when HDCTL.BCLD = 1.
7:0	<b>Cap ID (CAP)</b> —RO. Hardwired to 01h. Indicates that this pointer is a PCI power management capability. These bits are not reset by Function Level Reset.

#### 14.1.1.23 PC—Power Management Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 52h–53h Attribute: RO  
 Default Value: C842h Size: 16 bits

Bit	Description
15:11	<b>PME Support</b> —RO. Hardwired to 11001b. Indicates PME# can be generated from D3 and D0 states.
10	<b>D2 Support</b> —RO. Hardwired to 0. Indicates that D2 state is not supported.
9	<b>D1 Support</b> —RO. Hardwired to 0. Indicates that D1 state is not supported.
8:6	<b>Aux Current</b> —RO. Hardwired to 001b. Reports 55mA maximum suspend well current required when in the D3 <sub>COLD</sub> state.
5	<b>Device Specific Initialization (DSI)</b> —RO. Hardwired to 0. Indicates that no device specific initialization is required.



Bit	Description
4	Reserved
3	<b>PME Clock (PMEC)</b> —RO. Does not apply. Hardwired to 0.
2:0	<b>Version</b> —RO. Hardwired to 010b. Indicates support for version 1.1 of the PCI Power Management Specification.

#### 14.1.1.24 PCS—Power Management Control and Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 54h–57h Attribute: RO, R/W, R/WC  
Default Value: 00000000h Size: 32 bits  
Function Level Reset: No

Bit	Description
31:24	<b>Data</b> —RO. Does not apply. Hardwired to 0.
23	<b>Bus Power/Clock Control Enable</b> —RO. Does not apply. Hardwired to 0.
22	<b>B2/B3 Support</b> —RO. Does not apply. Hardwired to 0.
21:16	Reserved
15	<b>PME Status (PMES)</b> —R/W. 0 = Software clears the bit by writing a 1 to it. 1 = This bit is set when the Intel® High Definition Audio controller would normally assert the PME# signal independent of the state of the PME_EN bit—bit 8 in this register. This bit is in the resume well and is cleared by a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
14:9	Reserved
8	<b>PME Enable (PMEE)</b> —R/W. 0 = Disable 1 = When set and if corresponding PMES also set, the Intel® High Definition Audio controller sets the PME_B0_STS bit in the GPE0_STS register (PMBASE +28h). This bit is in the resume well and is cleared on a power-on reset. Software must not make assumptions about the reset state of this bit and must set it appropriately.
7:2	Reserved
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the Intel® High Definition Audio controller and to set a new power state. 00 = D0 state 11 = D3 <sub>HOT</sub> state Others = reserved  <b>Notes:</b> <ol style="list-style-type: none"><li>If software attempts to write a value of 01b or 10b into this field, the write operation must complete normally; however, the data is discarded and no state change occurs.</li><li>When in the D3<sub>HOT</sub> states, the Intel® High Definition Audio controller's configuration space is available, but the I/O and memory space are not. Additionally, interrupts are blocked.</li><li>When software changes this value from D3<sub>HOT</sub> state to the D0 state, an internal warm (soft) reset is generated, and software must re-initialize the function.</li></ol>



#### 14.1.1.25 MID—Message Signal Interrupt (MSI) Capability ID Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 60h–61h      Attribute: RO  
 Default Value: 7005h      Size: 16 bits

Bit	Description
15:8	<b>Next Capability (Next)</b> —RO. Hardwired to 70h. Points to the PCI Express* capability structure.
7:0	<b>Cap ID (CAP)</b> —RO. Hardwired to 05h. Indicates that this pointer is a MSI capability.

#### 14.1.1.26 MMC—Message Signal Interrupt (MSI) Message Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 62h–63h      Attribute: RO, R/W  
 Default Value: 0080h      Size: 16 bits

Bit	Description
15:8	Reserved
7	<b>64b Address Capability (64ADD)</b> —RO. Hardwired to 1. Indicates the ability to generate a 64-bit message address.
6:4	<b>Multiple Message Enable (MME)</b> —RO. Normally this is a R/W register. However since only 1 message is supported, these bits are hardwired to 000 = 1 message.
3:1	<b>Multiple Message Capable (MMC)</b> —RO. Hardwired to 0 indicating request for 1 message.
0	<b>MSI Enable (ME)</b> —R/W 0 = an MSI may not be generated 1 = an MSI will be generated instead of an INTx signal.

**14.1.1.27 MMLA—Message Signal Interrupt (MSI) Message Lower Address Register (Intel® High Definition Audio Controller—D27:F0)**

Address Offset: 64h–67h      Attribute: RO, R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:2	<b>Message Lower Address (MLA)</b> —R/W. Lower address used for MSI message.
1:0	Reserved

**14.1.1.28 MMUA—Message Signal Interrupt (MSI) Message Upper Address Register (Intel® High Definition Audio Controller—D27:F0)**

Address Offset: 68h–6Bh      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Message Upper Address (MUA)</b> —R/W. Upper 32-bits of address used for MSI message.

**14.1.1.29 MMD—Message Signal Interrupt (MSI) Message Data Register (Intel® High Definition Audio Controller—D27:F0)**

Address Offset: 6Ch–6Dh      Attribute: R/W  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Message Data (MD)</b> —R/W. Data used for MSI message.

**14.1.1.30 PXID—PCI Express\* Capability ID Register (Intel® High Definition Audio Controller—D27:F0)**

Address Offset: 70h–71h      Attribute: RO  
Default Value: 0010h      Size: 16 bits

Bit	Description
15:8	<b>Next Capability (Next)</b> —RO. Hardwired to 0. Indicates that this is the last capability structure in the list.
7:0	<b>Cap ID (CAP)</b> —RO. Hardwired to 10h. Indicates that this pointer is a PCI Express* capability structure.



#### 14.1.1.31 PXC—PCI Express\* Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 72h–73h Attribute: RO  
Default Value: 0091h Size: 16 bits

Bit	Description
15:14	Reserved
13:9	<b>Interrupt Message Number (IMN)</b> —RO. Hardwired to 0.
8	<b>Slot Implemented (SI)</b> —RO. Hardwired to 0.
7:4	<b>Device/Port Type (DPT)</b> —RO. Hardwired to 1001b. Indicates that this is a Root Complex Integrated endpoint device.
3:0	<b>Capability Version (CV)</b> —RO. Hardwired to 0001b. Indicates version #1 PCI Express* capability

#### 14.1.1.32 DEVCAP—Device Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 74h–77h Attribute: R/WL, RO  
Default Value: 10000000h Size: 32 bits  
Function Level Reset: No

Bit	Description
31:29	Reserved
28	<b>Function Level Reset (FLR)</b> —R/WL. A, 1 indicates that the PCH HD Audio Controller supports the Function Level Reset Capability. Locked when HDCTL.BCLD = 1.
27:26	<b>Captured Slot Power Limit Scale (SPLS)</b> —RO. Hardwired to 0.
25:18	<b>Captured Slot Power Limit Value (SPLV)</b> —RO. Hardwired to 0.
17:15	Reserved
14	<b>Power Indicator Present</b> —RO. Hardwired to 0.
13	<b>Attention Indicator Present</b> —RO. Hardwired to 0.
12	<b>Attention Button Present</b> —RO. Hardwired to 0.
11:9	<b>Endpoint L1 Acceptable Latency</b> —R/WL. BIOS must write to this bit field during boot. Locked when HDCTL.BCLD = 1.
8:6	<b>Endpoint L0s Acceptable Latency</b> —R/WL. BIOS must write to this bit field during boot. Locked when HDCTL.BCLD = 1.
5	<b>Extended Tag Field Support</b> —RO. Hardwired to 0. Indicates 5-bit tag field support
4:3	<b>Phantom Functions Supported</b> —RO. Hardwired to 0. Indicates that phantom functions not supported.
2:0	<b>Maximum Payload Size Supported</b> —RO. Hardwired to 0. Indicates 128-B maximum payload size capability.



#### 14.1.1.33 DEVC—Device Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 78h–79h Attribute: R/W, RO  
Default Value: 0800h Size: 16 bits  
Function Level Reset: No (Bit 11 Only)

Bit	Description
15	<b>Initiate FLR (IF)</b> —R/W. This bit is used to initiate FLR transition. 1 = A write of 1 initiates FLR transition. Since hardware does not respond to any cycles until FLR completion, the read value by software from this bit is 0.
14:12	<b>Maximum Read Request Size</b> —RO. Hardwired to 0 enabling 128B maximum read request size.
11	<b>No Snoop Enable (NSNPEN)</b> —R/W 0 = The Intel® High Definition Audio controller will not set the No Snoop bit. In this case, isochronous transfers will not use VC1 (VCi) even if it is enabled since VC1 is never snooped. Isochronous transfers will use VC0. 1 = The Intel® High Definition Audio controller is permitted to set the No Snoop bit in the Requester Attributes of a bus master transaction. In this case, VC0 or VC1 may be used for isochronous transfers. <b>Note:</b> This bit is not reset on D3 <sub>HOT</sub> to D0 transition; however, it is reset by PLTRST#. This bit is not reset by Function Level Reset.
10	<b>Auxiliary Power Enable</b> —RO. Hardwired to 0, indicating that Intel® High Definition Audio device does not draw AUX power
9	<b>Phantom Function Enable</b> —RO. Hardwired to 0 disabling phantom functions.
8	<b>Extended Tag Field Enable</b> —RO. Hardwired to 0 enabling 5-bit tag.
7:5	<b>Maximum Payload Size</b> —RO. Hardwired to 0 indicating 128B.
4	<b>Enable Relaxed Ordering</b> —RO. Hardwired to 0 disabling relaxed ordering.
3	<b>Unsupported Request Reporting Enable</b> —R/W. Not implemented.
2	<b>Fatal Error Reporting Enable</b> —R/W. Not implemented.
1	<b>Non-Fatal Error Reporting Enable</b> —R/W. Not implemented.
0	<b>Correctable Error Reporting Enable</b> —R/W. Not implemented.



#### 14.1.1.34 DEVS—Device Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 7Ah–7Bh      Attribute: RO  
Default Value: 0010h      Size: 16 bits

Bit	Description
15:6	Reserved
5	<b>Transactions Pending</b> —RO. 0 = Indicates that completions for all non-posted requests have been received. 1 = Indicates that Intel® High Definition Audio controller has issued non-posted requests which have not been completed.
4	<b>AUX Power Detected</b> —RO. Hardwired to 1 indicating the device is connected to resume power
3	<b>Unsupported Request Detected</b> —RO. Not implemented. Hardwired to 0.
2	<b>Fatal Error Detected</b> —RO. Not implemented. Hardwired to 0.
1	<b>Non-Fatal Error Detected</b> —RO. Not implemented. Hardwired to 0.
0	<b>Correctable Error Detected</b> —RO. Not implemented. Hardwired to 0.

#### 14.1.1.35 VCCAP—Virtual Channel Enhanced Capability Header (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 100h–103h      Attribute: R/WL  
Default Value: 13010002h      Size: 32 bits

Bit	Description
31:20	<b>Next Capability Offset</b> —R/WL. Points to the next capability header. 130h = Root Complex Link Declaration Enhanced Capability Header 000h = Root Complex Link Declaration Enhanced Capability Header is not supported. Locked when HDCTL.BCLD = 1.
19:16	<b>Capability Version</b> —R/WL 0h = PCI Express* Virtual channel capability and the Root Complex Topology Capability structure are not supported. 1h = PCI Express* Virtual channel capability and the Root Complex Topology Capability structure are supported. Locked when HDCTL.BCLD = 1.
15:0	<b>PCI Express* Extended Capability</b> —R/WL 0000h = PCI Express* Virtual channel capability and the Root Complex Topology Capability structure are not supported. 0002h = PCI Express* Virtual channel capability and the Root Complex Topology Capability structure are supported. Locked when HDCTL.BCLD = 1.



#### 14.1.1.36 PVCCAP1—Port VC Capability Register 1 (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 104h-107h Attribute: RO  
Default Value: 00000001h Size: 32 bits

Bit	Description
31:12	Reserved
11:10	<b>Port Arbitration Table Entry Size</b> —RO. Hardwired to 0 since this is an endpoint device.
9:8	<b>Reference Clock</b> —RO. Hardwired to 0 since this is an endpoint device.
7	Reserved
6:4	<b>Low Priority Extended VC Count</b> —RO. Hardwired to 0. Indicates that only VC0 belongs to the low-priority VC group.
3	Reserved
2:0	<b>Extended VC Count</b> —RO. Hardwired to 001b. Indicates that 1 extended VC (in addition to VC0) is supported by the Intel® High Definition Audio controller.

#### 14.1.1.37 PVCCAP2—Port VC Capability Register 2 (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 108h-10Bh Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:24	<b>VC Arbitration Table Offset</b> —RO. Hardwired to 0 indicating that a VC arbitration table is not present.
23:8	Reserved
7:0	<b>VC Arbitration Capability</b> —RO. Hardwired to 0. These bits are not applicable since the Intel® High Definition Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register.

#### 14.1.1.38 PVCCTL—Port VC Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 10Ch-10Dh Attribute: RO  
Default Value: 0000h Size: 16 bits

Bit	Description
15:4	Reserved
3:1	<b>VC Arbitration Select</b> —RO. Hardwired to 0. Normally these bits are R/W. However, these bits are not applicable since the Intel® High Definition Audio controller reports a 0 in the Low Priority Extended VC Count bits in the PVCCAP1 register.
0	<b>Load VC Arbitration Table</b> —RO. Hardwired to 0 since an arbitration table is not present.



#### 14.1.1.39 PVCSTS—Port VC Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 10Eh–10Fh Attribute: RO  
Default Value: 0000h Size: 16 bits

Bit	Description
15:1	Reserved
0	<b>VC Arbitration Table Status</b> —RO. Hardwired to 0 since an arbitration table is not present.

#### 14.1.1.40 VC0CAP—VC0 Resource Capability Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 110h–113h Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:24	<b>Port Arbitration Table Offset</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices
23	Reserved
22:16	<b>Maximum Time Slots</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
15	<b>Reject Snoop Transactions</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
14	<b>Advanced Packet Switching</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
13:8	Reserved
7:0	<b>Port Arbitration Capability</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.

#### 14.1.1.41 VC0CTL—VC0 Resource Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 114h–117h Attribute: R/W, RO  
Default Value: 800000FFh Size: 32 bits  
Function Level Reset: No

Bit	Description
31	<b>VC0 Enable</b> —RO. Hardwired to 1 for VC0.
30:27	Reserved
26:24	<b>VC0 ID</b> —RO. Hardwired to 0 since the first VC is always assigned as VC0.
23:20	Reserved
19:17	<b>Port Arbitration Select</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
16	<b>Load Port Arbitration Table</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
15:8	Reserved
7:0	<b>TC/VC0 Map</b> —R/W, RO. Bit 0 is hardwired to 1 since TC0 is always mapped VC0. Bits 7:1 are implemented as R/W bits.



#### 14.1.1.42 VC0STS—VC0 Resource Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 11Ah-11Bh Attribute: RO  
Default Value: 0000h Size: 16 bits

Bit	Description
15:2	Reserved
1	<b>VC0 Negotiation Pending</b> —RO. Hardwired to 0 since this bit does not apply to the integrated Intel® High Definition Audio device.
0	<b>Port Arbitration Table Status</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.

#### 14.1.1.43 VCiCAP—VCi Resource Capability Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 11Ch-11Fh Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:24	<b>Port Arbitration Table Offset</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
23	Reserved
22:16	<b>Maximum Time Slots</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
15	<b>Reject Snoop Transactions</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
14	<b>Advanced Packet Switching</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
13:8	Reserved
7:0	<b>Port Arbitration Capability</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.

#### 14.1.1.44 VCiCTL—VCi Resource Control Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 120h-123h Attribute: R/W, RO  
Default Value: 00000000h Size: 32 bits  
Function Level Reset: No

Bit	Description
31	<b>VCi Enable</b> —R/W. 0 = VCi is disabled 1 = VCi is enabled  <b>Note:</b> This bit is not reset on D3 <sub>HOT</sub> to D0 transition; however, it is reset by PLTRST#.
30:27	Reserved
26:24	<b>VCi ID</b> —R/W. This field assigns a VC ID to the VCi resource. This field is not used by the PCH hardware, but it is R/W to avoid confusing software.
23:20	Reserved
19:17	<b>Port Arbitration Select</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
16	<b>Load Port Arbitration Table</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.
15:8	Reserved
7:0	<b>TC/VCi Map</b> —R/W, RO. This field indicates the TCs that are mapped to the VCi resource. Bit 0 is hardwired to 0 indicating that it cannot be mapped to VCi. Bits 7:1 are implemented as R/W bits. This field is not used by the PCH hardware, but it is R/W to avoid confusing software.



#### 14.1.1.45 VCiSTS—VCi Resource Status Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 126h–127h      Attribute: RO  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:2	Reserved
1	<b>VCi Negotiation Pending</b> —RO. Does not apply. Hardwired to 0.
0	<b>Port Arbitration Table Status</b> —RO. Hardwired to 0 since this field is not valid for endpoint devices.

#### 14.1.1.46 RCCAP—Root Complex Link Declaration Enhanced Capability Header Register (Intel® High Definition Audio Controller—D27:F0)

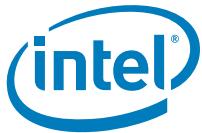
Address Offset: 130h–133h      Attribute: RO  
Default Value: 00010005h      Size: 32 bits

Bit	Description
31:20	<b>Next Capability Offset</b> —RO. Hardwired to 0 indicating this is the last capability.
19:16	<b>Capability Version</b> —RO. Hardwired to 1h.
15:0	<b>PCI Express* Extended Capability ID</b> —RO. Hardwired to 0005h.

#### 14.1.1.47 ESD—Element Self Description Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 134h–137h      Attribute: RO, RL  
Default Value: 0F000100h      Size: 32 bits

Bit	Description
31:24	<b>Port Number</b> —RO. Hardwired to 0Fh indicating that the Intel® High Definition Audio controller is assigned as Port #15d.
23:16	<b>Component ID</b> —RL. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS. Locked when HDCTL.BCLD = 1.
15:8	<b>Number of Link Entries</b> —RO. The Intel® High Definition Audio only connects to one device, the PCH egress port. Therefore, this field reports a value of 1h.
7:4	Reserved
3:0	<b>Element Type (ELTYP)</b> —RO. The Intel® High Definition Audio controller is an integrated Root Complex Device. Therefore, the field reports a value of 0h.



#### 14.1.1.48 L1DESC—Link 1 Description Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 140h–143h Attribute: RO  
Default Value: 00000001h Size: 32 bits

Bit	Description
31:24	<b>Target Port Number</b> —RO. The Intel® High Definition Audio controller targets PCH Port 0.
23:16	<b>Target Component ID</b> —RO. This field returns the value of the ESD.CID field of the chip configuration section. ESD.CID is programmed by BIOS.
15:2	Reserved
1	<b>Link Type</b> —RO. Hardwired to 0 indicating Type 0.
0	<b>Link Valid</b> —RO. Hardwired to 1.

#### 14.1.1.49 L1ADDL—Link 1 Lower Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 148h–14Bh Attribute: RO  
Default Value: See Register Description Size: 32 bits

Bit	Description
31:14	<b>Link 1 Lower Address</b> —RO. Hardwired to match the RCBA register value in the PCI-LPC bridge (D31:F0:F0h).
13:0	Reserved

#### 14.1.1.50 L1ADDU—Link 1 Upper Address Register (Intel® High Definition Audio Controller—D27:F0)

Address Offset: 14Ch–14Fh Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Link 1 Upper Address</b> —RO. Hardwired to 00000000h.



## 14.1.2 Intel® High Definition Audio (Intel® HD Audio) Memory Mapped Configuration Registers (Intel® High Definition Audio D27:F0)

The base memory location for these memory mapped configuration registers is specified in the HDBAR register (D27:F0:offset 10h and D27:F0:offset 14h). The individual registers are then accessible at HDBAR + Offset as indicated in [Table 14-2](#).

These memory mapped registers must be accessed in byte, word, or DWord quantities.

**Note:** Address locations that are not shown should be treated as Reserved.

**Table 14-2. Intel® High Definition Audio Memory Mapped Configuration Registers Address Map (Intel® High Definition Audio D27:F0) (Sheet 1 of 4)**

HDBAR + Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	GCAP	Global Capabilities	4401h	RO, R/WO
02h	VMIN	Minor Version	00h	RO
03h	VMAJ	Major Version	01h	RO
04h-05h	OUTPAY	Output Payload Capability	003Ch	RO
06h-07h	INPAY	Input Payload Capability	001Dh	RO
08h-0Bh	GCTL	Global Control	00000000h	R/W
0Ch-0Dh	WAKEEN	Wake Enable	0000h	R/W
0Eh-0Fh	STATESTS	State Change Status	0000h	R/WC
10h-11h	GSTS	Global Status	0000h	R/WC
12h-13h	GCAP2	Global Capabilities 2	0001h	R/WL
18h-19h	OUTSTRMPAY	Output Stream Payload Capability	0030h	RO
1Ah-1Bh	INSTRMPAY	Input Stream Payload Capability	0018h	RO
1Ch-1Fh	—	Reserved	00000000h	RO
20h-23h	INTCTL	Interrupt Control	00000000h	R/W
24h-27h	INTSTS	Interrupt Status	00000000h	RO
30h-33h	WALCLK	Wall Clock Counter	00000000h	RO
38h-3Bh	SSYNC	Stream Synchronization	00000000h	R/W
40h-43h	CORBLBASE	CORB Lower Base Address	00000000h	R/W, RO
44h-47h	CORBUBASE	CORB Upper Base Address	00000000h	R/W
48h-49h	CORBWP	CORB Write Pointer	0000h	R/W
4Ah-4Bh	CORB RP	CORB Read Pointer	0000h	R/W, RO
4Ch	CORB CTL	CORB Control	00h	R/W
4Dh	CORB ST	CORB Status	00h	R/WC
4Eh	CORB SIZE	CORB Size	42h	RO
50h-53h	RIRBLBASE	RIRB Lower Base Address	00000000h	R/W, RO
54h-57h	RIRBUBASE	RIRB Upper Base Address	00000000h	R/W
58h-59h	RIRB WP	RIRB Write Pointer	0000h	R/W, RO
5Ah-5Bh	RINTCNT	Response Interrupt Count	0000h	R/W
5Ch	RIRB CTL	RIRB Control	00h	R/W
5Dh	RIRBSTS	RIRB Status	00h	R/WC

**Table 14-2. Intel® High Definition Audio Memory Mapped Configuration Registers Address Map (Intel® High Definition Audio D27:F0) (Sheet 2 of 4)**

HDBAR + Offset	Mnemonic	Register Name	Default	Attribute
5Eh	RIRBSIZE	RIRB Size	42h	RO
60h-63h	IC	Immediate Command	00000000h	R/W
64h-67h	IR	Immediate Response	00000000h	RO
68h-69h	ICS	Immediate Command Status	0000h	R/W, R/WC
70h-73h	DPLBASE	DMA Position Lower Base Address	00000000h	R/W, RO
74h-77h	DPUBASE	DMA Position Upper Base Address	00000000h	R/W
80h-82h	ISD0CTL	Input Stream Descriptor Control	040000h	R/W, RO
83h	ISD0STS	ISD0 Status	00h	R/WC, RO
84h-87h	ISD0LPIB	ISD0 Link Position in Buffer	00000000h	RO
88h-8Bh	ISD0CBL	ISD0 Cyclic Buffer Length	00000000h	R/W
8Ch-8Dh	ISD0LVI	ISD0 Last Valid Index	0000h	R/W
8Eh-8F	ISD0FIFOW	ISD0 FIFO Watermark	0004h	R/W
90h-91h	ISD0FIFOS	ISD0 FIFO Size	0000h	R/W
92h-93h	ISD0FMT	ISD0 Format	0000h	R/W
98h-9Bh	ISD0BDPL	ISD0 Buffer Descriptor List Pointer –Lower Base Address	00000000h	R/W, RO
9Ch-9Fh	ISD0BDPU	ISD0 Buffer Description List Pointer –Upper Base Address	00000000h	R/W
A0h-A2h	ISD1CTL	Input Stream Descriptor 1(ISD1) Control	040000h	R/W, RO
A3h	ISD1STS	ISD1 Status	00h	R/WC, RO
A4h-A7h	ISD1LPIB	ISD1 Link Position in Buffer	00000000h	RO
A8h-ABh	ISD1CBL	ISD1 Cyclic Buffer Length	00000000h	R/W
ACh-ADh	ISD1LVI	ISD1 Last Valid Index	0000h	R/W
AEh-AFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W
B0h-B1h	ISD1FIFOS	ISD1 FIFO Size	0000h	R/W
B2h-B3h	ISD1FMT	ISD1 Format	0000h	R/W
B8h-BBh	ISD1BDPL	ISD1 Buffer Descriptor List Pointer –Lower Base Address	00000000h	R/W, RO
BCh-BFh	ISD1BDPU	ISD1 Buffer Description List Pointer –Upper Base Address	00000000h	R/W
C0h-C2h	ISD2CTL	Input Stream Descriptor 2 (ISD2) Control	040000h	R/W, RO
C3h	ISD2STS	ISD2 Status	00h	R/WC, RO
C4h-C7h	ISD2LPIB	ISD2 Link Position in Buffer	00000000h	RO
C8h-CBh	ISD2CBL	ISD2 Cyclic Buffer Length	00000000h	R/W
CCh-CDh	ISD2LVI	ISD2 Last Valid Index	0000h	R/W
CEh-CFh	ISD1FIFOW	ISD1 FIFO Watermark	0004h	R/W
D0h-D1h	ISD2FIFOS	ISD2 FIFO Size	0000h	R/W
D2h-D3h	ISD2FMT	ISD2 Format	0000h	R/W
D8h-DBh	ISD2BDPL	ISD2 Buffer Descriptor List Pointer –Lower Base Address	00000000h	R/W, RO
DCh-DFh	ISD2BDPU	ISD2 Buffer Description List Pointer –Upper Base Address	00000000h	R/W



**Table 14-2. Intel® High Definition Audio Memory Mapped Configuration Registers Address Map (Intel® High Definition Audio D27:F0) (Sheet 3 of 4)**

HDBAR + Offset	Mnemonic	Register Name	Default	Attribute
E0h-E2h	ISD3CTL	Input Stream Descriptor 3 (ISD3) Control	040000h	R/W, RO
E3h	ISD3STS	ISD3 Status	00h	R/WC, RO
E4h-E7h	ISD3LPIB	ISD3 Link Position in Buffer	00000000h	RO
E8h-EBh	ISD3CBL	ISD3 Cyclic Buffer Length	00000000h	R/W
EC'h-EDh	ISD3LVI	ISD3 Last Valid Index	0000h	R/W
EEh-EFh	ISD3FIFOW	ISD3 FIFO Watermark	0004h	R/W
F0h-F1h	ISD3FIFOS	ISD3 FIFO Size	0000h	R/W
F2h-F3h	ISD3FMT	ISD3 Format	0000h	R/W
F8h-FBh	ISD3BDPL	ISD3 Buffer Descriptor List Pointer – Lower Base Address	00000000h	R/W, RO
FCh-FFh	ISD3BDPU	ISD3 Buffer Description List Pointer – Upper Base Address	00000000h	R/W
100h-102h	OSD0CTL	Output Stream Descriptor 0 (OSD0) Control	040000h	R/W, RO
103h	OSD0STS	OSD0 Status	00h	R/WC, RO
104h-107h	OSD0LPIB	OSD0 Link Position in Buffer	00000000h	RO
108h-10Bh	OSD0CBL	OSD0 Cyclic Buffer Length	00000000h	R/W
10Ch-10Dh	OSD0LVI	OSD0 Last Valid Index	0000h	R/W
10Eh-10Fh	OSD0FIFOW	OSD0 FIFO Watermark	0004h	R/W
110h-111h	OSD0FIFOS	OSD0 FIFO Size	0000h	R/W
112h-113h	OSD0FMT	OSD0 Format	0000h	R/W
118h-11Bh	OSD0BDPL	OSD0 Buffer Descriptor List Pointer – Lower Base Address	00000000h	R/W, RO
11Ch-11Fh	OSD0BDPU	OSD0 Buffer Description List Pointer – Upper Base Address	00000000h	R/W
120h-122h	OSD1CTL	Output Stream Descriptor 1 (OSD1) Control	040000h	R/W, RO
123h	OSD1STS	OSD1 Status	00h	R/WC, RO
124h-127h	OSD1LPIB	OSD1 Link Position in Buffer	00000000h	RO
128h-12Bh	OSD1CBL	OSD1 Cyclic Buffer Length	00000000h	R/W
12Ch-12Dh	OSD1LVI	OSD1 Last Valid Index	0000h	R/W
12Eh-12Fh	OSD1FIFOW	OSD1 FIFO Watermark	0004h	R/W
130h-131h	OSD1FIFOS	OSD1 FIFO Size	0000h	R/W
132h-133h	OSD1FMT	OSD1 Format	0000h	R/W
138h-13Bh	OSD1BDPL	OSD1 Buffer Descriptor List Pointer – Lower Base Address	00000000h	R/W, RO
13Ch-13Fh	OSD1BDPU	OSD1 Buffer Description List Pointer – Upper Base Address	00000000h	R/W
140h-142h	OSD2CTL	Output Stream Descriptor 2 (OSD2) Control	040000h	R/W, RO
143h	OSD2STS	OSD2 Status	00h	R/WC, RO
144h-147h	OSD2LPIB	OSD2 Link Position in Buffer	00000000h	RO
148h-14Bh	OSD2CBL	OSD2 Cyclic Buffer Length	00000000h	R/W
14Ch-14Dh	OSD2LVI	OSD2 Last Valid Index	0000h	R/W
14Eh-14Fh	OSD2FIFOW	OSD2 FIFO Watermark	0004h	R/W

**Table 14-2. Intel® High Definition Audio Memory Mapped Configuration Registers Address Map (Intel® High Definition Audio D27:F0) (Sheet 4 of 4)**

HDBAR + Offset	Mnemonic	Register Name	Default	Attribute
150h-151h	OSD2FIFOS	OSD2 FIFO Size	0000h	R/W
152h-153h	OSD2FMT	OSD2 Format	0000h	R/W
158h-15Bh	OSD2BDPL	OSD2 Buffer Descriptor List Pointer – Lower Base Address	00000000h	R/W, RO
15Ch-15Fh	OSD2BDPU	OSD2 Buffer Description List Pointer – Upper Base Address	00000000h	R/W
160h-162h	OSD3CTL	Output Stream Descriptor 3 (OSD3) Control	040000h	R/W, RO
163h	OSD3STS	OSD3 Status	00h	R/WC, RO
164h-167h	OSD3LPIB	OSD3 Link Position in Buffer	00000000h	RO
168h-16Bh	OSD3CBL	OSD3 Cyclic Buffer Length	00000000h	R/W
16Ch-16Dh	OSD3LVI	OSD3 Last Valid Index	0000h	R/W
16Eh-16Fh	OSD3FIFOW	OSD3 FIFO Watermark	0004h	R/W
170h-171h	OSD3FIFOS	OSD3 FIFO Size	0000h	R/W
172h-173h	OSD3FMT	OSD3 Format	0000h	R/W
178h-17Bh	OSD3BDPL	OSD3 Buffer Descriptor List Pointer – Lower Base Address	00000000h	R/W, RO
17Ch-17Fh	OSD3BDPU	OSD3 Buffer Description List Pointer – Upper Base Address	00000000h	R/W



#### 14.1.2.1 GCAP—Global Capabilities Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 00h      Attribute: RO, R/WL  
Default Value: 4401h      Size: 16 bits

Bit	Description
15:12	<b>Number of Output Stream Supported</b> —R/WL. 0100b indicates that the PCH's Intel® High Definition Audio controller supports 4 output streams. Locked when HDCTL.BCLD = 1.
11:8	<b>Number of Input Stream Supported</b> —R/WL. 0100b indicates that the PCH's Intel® High Definition Audio controller supports 4 input streams. Locked when HDCTL.BCLD = 1.
7:3	<b>Number of Bidirectional Stream Supported</b> —RO. Hardwired to 0 indicating that the PCH's Intel® High Definition Audio controller supports 0 bidirectional stream.
2:1	<b>Number of Serial Data Out Signals</b> —RO. Hardwired to 0 indicating that the PCH's Intel® High Definition Audio controller supports 1 serial data output signal.
0	<b>64-bit Address Supported</b> —R/WL. 1b indicates that the PCH's Intel® High Definition Audio controller supports 64-bit addressing for BDL addresses, data buffer addressees, and command buffer addresses. Locked when HDCTL.BCLD = 1.

#### 14.1.2.2 VMIN—Minor Version Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 02h      Attribute: RO  
Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Minor Version</b> —RO. Hardwired to 0 indicating that the PCH supports minor revision number 00h of the Intel® High Definition Audio specification.

#### 14.1.2.3 VMAJ—Major Version Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 03h      Attribute: RO  
Default Value: 01h      Size: 8 bits

Bit	Description
7:0	<b>Major Version</b> —RO. Hardwired to 01h indicating that the PCH supports major revision number 1 of the Intel® High Definition Audio specification.



#### 14.1.2.4 OUTPAY—Output Payload Capability Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 04h  
Default Value: 003Ch

Attribute: RO  
Size: 16 bits

Bit	Description
15:7	Reserved
6:0	<b>Output Payload Capability</b> —RO. Hardwired to 3Ch indicating 60 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for command and control. This measurement is in 16-bit word quantities per 48 MHz frame. The default link clock of 24.000 MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits are used for command and control, leaving 60 words available for data payload. 00h = 0 word 01h = 1 word payload. ..... FFh = 256 word payload.

#### 14.1.2.5 INPAY—Input Payload Capability Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 06h  
Default Value: 001Dh

Attribute: RO  
Size: 16 bits

Bit	Description
15:7	Reserved
6:0	<b>Input Payload Capability</b> —RO. Hardwired to 1Dh indicating 29 word payload. This field indicates the total output payload available on the link. This does not include bandwidth used for response. This measurement is in 16-bit word quantities per 48 MHz frame. The default link clock of 24.000 MHz provides 500 bits per frame, or 31.25 words in total. 36 bits are used for response, leaving 29 words available for data payload. 00h = 0 word 01h = 1 word payload. ..... FFh = 256 word payload.



### 14.1.2.6 GCTL—Global Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 08h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:9	Reserved
8	<b>Accept Unsolicited Response Enable</b> —R/W. 0 = Unsolicited responses from the codecs are not accepted. 1 = Unsolicited response from the codecs are accepted by the controller and placed into the Response Input Ring Buffer.
7:2	Reserved
1	<b>Flush Control</b> —R/W. Writing a 1 to this bit initiates a flush. When the flush completion is received by the controller, hardware sets the Flush Status bit and clears this Flush Control bit. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 needs not be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be 0). When the flush is initiated, the controller will flush the pipelines to memory to ensure that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFOs is not critical.
0	<b>Controller Reset #</b> —R/W. 0 = Writing a 0 causes the Intel® High Definition Audio controller to be reset. All state machines, FIFOs, and non-resume well memory-mapped configuration registers (not PCI configuration registers) in the controller will be reset. The Intel® High Definition Audio link RESET# signal will be asserted, and all other link signals will be driven to their default values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a 0 from this bit to verify the controller is in reset. 1 = Writing a 1 causes the controller to exit its reset state and de-assert the Intel® High Definition Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum Intel® High Definition Audio link RESET# signal assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. This bit defaults to a 0 after Hardware reset; therefore, software needs to write a 1 to this bit to begin operation.

**Notes:**

1. The CORB/RIRB RUN bits and all stream RUN bits must be verified cleared to 0 before writing a 0 to this bit in order to assure a clean re-start.
2. When setting or clearing this bit, software must ensure that minimum link timing requirements (minimum RESET# assertion time, and so on) are met.
3. When this bit is 0 indicating that the controller is in reset, writes to all Intel® High Definition Audio memory-mapped registers are ignored as if the device is not present. The only exception is this register itself. The Global Control register is write-able as a DWord, Word, or Byte even when CRST# (this bit) is 0 if the byte enable for the byte containing the CRST# bit (Byte Enable 0) is active. If Byte Enable 0 is not active, writes to the Global Control register will be ignored when CRST# is 0. When CRST# is 0, reads to Intel High Definition Audio memory-mapped registers will return their default value except for registers that are not reset with PLTRST# or on a D3<sub>HOT</sub> to D0 transition.



#### 14.1.2.7 WAKEEN—Wake Enable Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 0Ch      Attribute: R/W  
Default Value: 0000h      Size: 16 bits  
Function Level Reset: No

Bit	Description
15:4	Reserved
3:0	<b>SDIN Wake Enable Flags</b> —R/W. These bits control which SDI signal(s) may generate a wake event. A, 1b in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. Bit 0 is used for SDI[0] Bit 1 is used for SDI[1] Bit 2 is used for SDI[2] Bit 3 is used for SDI[3] <b>Note:</b> These bits are in the resume well and only cleared on a power on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.

#### 14.1.2.8 STATESTS—State Change Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 0Eh      Attribute: R/WC  
Default Value: 0000h      Size: 16 bits  
Function Level Reset: No

Bit	Description
15:4	Reserved
3:0	<b>SDIN State Change Status Flags</b> —R/WC. Flag bits that indicate which SDI signal(s) received a state change event. The bits are cleared by writing 1s to them. Bit 0 = SDI[0] Bit 1 = SDI[1] Bit 2 = SDI[2] Bit 3 = SDI[3] These bits are in the resume well and only cleared on a power on reset. Software must not make assumptions about the reset state of these bits and must set them appropriately.



#### 14.1.2.9 GSTS—Global Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 10h      Attribute: R/WC  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:2	Reserved
1	<b>Flush Status</b> —R/WC. This bit is set to 1 by hardware to indicate that the flush cycle initiated when the Flush Control bit (HDBAR + 08h, bit 1) was set has completed. Software must write a 1 to clear this bit before the next time the Flush Control bit is set to clear the bit.
0	Reserved

#### 14.1.2.10 GCAP2 Global Capabilities 2 Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 12h      Attribute: R/WL  
Default Value: 0001h      Size: 16 bits

Bit	Description
15:1	Reserved
0	<b>Energy Efficient Audio Capability (EEAC)</b> —R/WL. Indicates whether the energy efficient audio with deeper buffering is supported or not. 0 = Not supported. 1 = Supported. Locked when HDCTL.BCLD = 1.

#### 14.1.2.11 OUTSTRMPAY—Output Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 18h      Attribute: RO  
Default Value: 0030h      Size: 16 bits

Bit	Description
15:8	Reserved
7:0	<b>Output Stream Payload Capability (OUTSTRMPAY)</b> —RO. Indicates maximum number of words per frame for any single output stream. This measurement is in 16-bit word quantities per 48 KHz frame. 48 Words (96B) is the maximum supported; therefore, a value of 30h is reported in this register. Software must ensure that a format that would cause more words per frame than indicated is not programmed into the Output Stream Descriptor register. 00h = 0 words 01h = 1 word payload ... FFh = 255h word payload



#### 14.1.2.12 INSTRMPAY—Input Stream Payload Capability (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 1Ah  
Default Value: 0018h

Attribute: RO  
Size: 16 bits

Bit	Description
15:8	Reserved
7:0	<b>Input Stream Payload Capability (INSTRMPAY)</b> —RO. Indicates maximum number of words per frame for any single input stream. This measurement is in 16-bit word quantities per 48 KHz frame. 24 Words (48B) is the maximum supported; therefore, a value of 18h is reported in this register. Software must ensure that a format that would cause more words per frame than indicated is not programmed into the Input Stream Descriptor register. 00h = 0 words 01h = 1 word payload ... FFh = 255h word payload

#### 14.1.2.13 INTCTL—Interrupt Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 20h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31	<b>Global Interrupt Enable (GIE)</b> —R/W. Global bit to enable device interrupt generation. 1 = When set to 1, the Intel® High Definition Audio function is enabled to generate an interrupt. This control is in addition to any bits in the bus specific address space, such as the Interrupt Enable bit in the PCI configuration space. <b>Note:</b> This bit is not affected by the D3 <sub>HOT</sub> to D0 transition.
30	<b>Controller Interrupt Enable (CIE)</b> —R/W. Enables the general interrupt for controller functions. 1 = When set to 1, the controller generates an interrupt when the corresponding status bit gets set due to a Response Interrupt, a Response Buffer Overrun, and State Change events. <b>Note:</b> This bit is not affected by the D3 <sub>HOT</sub> to D0 transition.
29:8	Reserved
7:0	<b>Stream Interrupt Enable (SIE)</b> —R/W. When set to 1, the individual streams are enabled to generate an interrupt when the corresponding status bits get set. A stream interrupt will be caused as a result of a buffer with IOC = 1 in the BDL entry being completed, or as a result of a FIFO error (underrun or overrun) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1 Bit 5 = output stream 2 Bit 6 = output stream 3 Bit 7 = output stream 4

#### 14.1.2.14 INTSTS—Interrupt Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 24h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31	<b>Global Interrupt Status (GIS)</b> —RO. This bit is an OR of all the interrupt status bits in this register. <b>Note:</b> This bit is not affected by the D3 <sub>HOT</sub> to D0 transition.
30	<b>Controller Interrupt Status (CIS)</b> —RO. Status of general controller interrupt. 1 = Interrupt condition occurred due to a Response Interrupt, a Response Buffer Overrun Interrupt, or a SDIN State Change event. The exact cause can be determined by interrogating other registers. This bit is an OR of all of the stated interrupt status bits for this register. <b>Notes:</b> <ol style="list-style-type: none"> <li>1. This bit is set regardless of the state of the corresponding interrupt enable bit, but a hardware interrupt will not be generated unless the corresponding enable bit is set.</li> <li>2. This bit is not affected by the D3<sub>HOT</sub> to D0 transition.</li> </ol>
29:8	Reserved
7:0	<b>Stream Interrupt Status (SIS)</b> —RO. 1 = Interrupt condition occurred on the corresponding stream. This bit is an OR of all of the stream's interrupt status bits. <b>Note:</b> These bits are set regardless of the state of the corresponding interrupt enable bits. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1 Bit 5 = output stream 2 Bit 6 = output stream 3 Bit 7 = output stream 4

#### 14.1.2.15 WALCLK—Wall Clock Counter Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 30h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:0	<b>Wall Clock Counter</b> —RO. A 32-bit counter that is incremented on each link Bit Clock period and rolls over from FFFF FFFFh to 0000 0000h. This counter will roll over to 0 with a period of approximately 179 seconds. This counter is enabled while the Bit Clock bit is set to 1. Software uses this counter to synchronize between multiple controllers. Will be reset on controller reset.



#### 14.1.2.16 SSYNC—Stream Synchronization Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 38h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Stream Synchronization (SSYNC)</b> —R/W. When set to 1, these bits block data from being sent on or received from the link. Each bit controls the associated stream descriptor (that is, bit 0 corresponds to the first stream descriptor, and so on) To synchronously start a set of DMA engines, these bits are first set to 1. The RUN bits for the associated stream descriptors are then set to 1 to start the DMA engines. When all streams are ready (FIFORDY =1), the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop the streams, first these bits are set, and then the individual RUN bits in the stream descriptor are cleared by software. If synchronization is not desired, these bits may be left as 0, and the stream will simply begin running normally when the stream's RUN bit is set. The streams are numbered and the SIE bits assigned sequentially, based on their order in the register set. Bit 0 = input stream 1 Bit 1 = input stream 2 Bit 2 = input stream 3 Bit 3 = input stream 4 Bit 4 = output stream 1 Bit 5 = output stream 2 Bit 6 = output stream 3 Bit 7 = output stream 4

#### 14.1.2.17 CORBLBASE—CORB Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 40h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:7	<b>CORB Lower Base Address</b> —R/W. Lower address of the Command Output Ring Buffer, allowing the CORB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	<b>CORB Lower Base Unimplemented Bits</b> —RO. Hardwired to 0. This required the CORB to be allocated with 128B granularity to allow for cache line fetch optimizations.



#### 14.1.2.18 CORBUBASE—CORB Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 44h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>CORB Upper Base Address</b> —R/W. Upper 32 bits of the address of the Command Output Ring buffer. This register must not be written when the DMA engine is running or the DMA transfer may be corrupted.

#### 14.1.2.19 CORBWP—CORB Write Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 48h      Attribute: R/W  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:8	Reserved
7:0	<b>CORB Write Pointer</b> —R/W. Software writes the last valid CORB entry offset into this field in DWord granularity. The DMA engine fetches commands from the CORB until the Read pointer matches the Write pointer. Supports 256 CORB entries (256x4B = 1KB). This register may be written when the DMA engine is running.

#### 14.1.2.20 CORBRP—CORB Read Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 4Ah      Attribute: R/W, RO  
Default Value: 0000h      Size: 16 bits

Bit	Description
15	<b>CORB Read Pointer Reset</b> —R/W. Software writes a 1 to this bit to reset the CORB Read Pointer to 0 and clear any residual prefetched commands in the CORB hardware buffer within the Intel® High Definition Audio controller. The hardware will physically update this bit to 1 when the CORB Pointer reset is complete. Software must read a 1 to verify that the reset completed correctly. Software must clear this bit back to 0 and read back the 0 to verify that the clear completed correctly. The CORB DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted.
14:8	Reserved
7:0	<b>CORB Read Pointer (CORBRP)</b> —RO. Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in DWord granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports 256 CORB entries (256 x 4B=1KB). This field may be read while the DMA engine is running.



#### 14.1.2.21 CORBCTL—CORB Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 4Ch Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:2	Reserved
1	<b>Enable CORB DMA Engine</b> —R/W 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	<b>CORB Memory Error Interrupt Enable</b> —R/W. If this bit is set, the controller will generate an interrupt if the CMEI status bit (HDBAR + 4Dh: bit 0) is set.

#### 14.1.2.22 CORBST—CORB Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 4Dh Attribute: R/WC  
Default Value: 00h Size: 8 bits

Bit	Description
7:1	Reserved
0	<b>CORB Memory Error Indication (CMEI)</b> —R/WC 1 = Controller detected an error in the path way between the controller and memory. This may be an ECC bit error or any other type of detectable data error that renders the command data fetched invalid. Software can clear this bit by writing a 1 to it. However, this type of error leaves the audio subsystem in an un-viable state and typically requires a controller reset by writing a 0 to the Controller Reset # bit (HDBAR + 08h: bit 0).

#### 14.1.2.23 CORBSIZE—CORB Size Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 4Eh Attribute: RO  
Default Value: 42h Size: 8 bits

Bit	Description
7:4	<b>CORB Size Capability</b> —RO. Hardwired to 0100b indicating that the PCH only supports a CORB size of 256 CORB entries (1024B)
3:2	Reserved
1:0	<b>CORB Size</b> —RO. Hardwired to 10b which sets the CORB size to 256 entries (1024B)



#### 14.1.2.24 RIRBLBASE—RIRB Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 50h      Attribute: R/W, RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:7	<b>RIRB Lower Base Address</b> —R/W. Lower address of the Response Input Ring Buffer, allowing the RIRB base address to be assigned on any 128-B boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	RIRB Lower Base Unimplemented Bits—RO. Hardwired to 0. This required the RIRB to be allocated with 128-B granularity to allow for cache line fetch optimizations.

#### 14.1.2.25 RIRBUBASE—RIRB Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 54h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>RIRB Upper Base Address</b> —R/W. Upper 32 bits of the address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

#### 14.1.2.26 RIRBWP—RIRB Write Pointer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: HDBAR + 58h      Attribute: R/W, RO  
Default Value: 0000h      Size: 16 bits

Bit	Description
15	<b>RIRB Write Pointer Reset</b> —R/W. Software writes a 1 to this bit to reset the RIRB Write Pointer to 0. The RIRB DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit is always read as 0.
14:8	Reserved
7:0	<b>RIRB Write Pointer (RIRBWP)</b> —RO. Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 DWord RIRB entry units (since each RIRB entry is 2 DWords long). Supports up to 256 RIRB entries (256 x 8 B = 2KB). This register may be written when the DMA engine is running.



#### 14.1.2.27 RINTCNT—Response Interrupt Count Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 5Ah  
Default Value: 0000hAttribute: R/W  
Size: 16 bits

Bit	Description
15:8	Reserved
7:0	<b>N Response Interrupt Count</b> —R/W 0000 0001b = 1 response sent to RIRB ..... 1111 1111b = 255 responses sent to RIRB 0000 0000b = 256 responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Each response occupies 2 DWords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one codec responds in one frame, then the count is increased by the number of responses received in the frame.

#### 14.1.2.28 RIRBCTL—RIRB Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 5Ch  
Default Value: 00hAttribute: R/W  
Size: 8 bits

Bit	Description
7:3	Reserved
2	<b>Response Overrun Interrupt Control</b> —R/W. If this bit is set, the hardware will generate an interrupt when the Response Overrun Interrupt Status bit (HDBAR + 5Dh: bit 2) is set.
1	<b>Enable RIRB DMA Engine</b> —R/W. 0 = DMA stop 1 = DMA run After software writes a 0 to this bit, the hardware may not stop immediately. The hardware will physically update the bit to 0 when the DMA engine is truly stopped. Software must read a 0 from this bit to verify that the DMA engine is truly stopped.
0	<b>Response Interrupt Control</b> —R/W. 0 = Disable Interrupt 1 = Generate an interrupt after N number of responses are sent to the RIRB buffer OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). The N counter is reset when the interrupt is generated.



#### 14.1.2.29 RIRBSTS—RIRB Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 5Dh  
Default Value: 00h

Attribute: R/WC  
Size: 8 bits

Bit	Description
7:3	Reserved
2	<b>Response Overrun Interrupt Status</b> —R/WC. 1 = Software sets this bit to 1 when the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming responses overrun the internal FIFO. When the overrun occurs, the hardware will drop the responses which overrun the buffer. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. This status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.
1	Reserved
0	<b>Response Interrupt</b> —R/WC. 1 = Hardware sets this bit to 1 when an interrupt has been generated after N number of Responses are sent to the RIRB buffer, OR when an empty Response slot is encountered on all SDI[x] inputs (whichever occurs first). This status bit is set even if an interrupt is not enabled for this event. Software clears this bit by writing a 1 to it.

#### 14.1.2.30 RIRBSIZE—RIRB Size Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 5Eh  
Default Value: 42h

Attribute: RO  
Size: 8 bits

Bit	Description
7:4	<b>RIRB Size Capability</b> —RO. Hardwired to 0100b indicating that the PCH only supports a RIRB size of 256 RIRB entries (2048B).
3:2	Reserved
1:0	<b>RIRB Size</b> —RO. Hardwired to 10b which sets the CORB size to 256 entries (2048B).

#### 14.1.2.31 IC—Immediate Command Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 60h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:0	<b>Immediate Command Write</b> —R/W. The command to be sent to the codec using the Immediate Command mechanism is written to this register. The command stored in this register is sent out over the link during the next available frame after a 1 is written to the ICB bit (HDBAR + 68h: bit 0).



#### 14.1.2.32 IR—Immediate Response Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 64h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:0	<b>Immediate Response Read (IRR)</b> —RO. This register contains the response received from a codec resulting from a command sent using the Immediate Command mechanism. If multiple codecs responded in the same time, there is no assurance as to which response will be latched. Therefore, broadcast-type commands must not be issued using the Immediate Command mechanism.

#### 14.1.2.33 ICS—Immediate Command Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 68h  
Default Value: 0000h

Attribute: R/W, R/WC  
Size: 16 bits

Bit	Description
15:2	Reserved
1	<b>Immediate Result Valid (IRV)</b> —R/WC. 1 = Set to 1 by hardware when a new response is latched into the Immediate Response register (HDBAR + 64). This is a status flag indicating that software may read the response from the Immediate Response register. Software must clear this bit by writing a 1 to it before issuing a new command so that the software may determine when a new response has arrived.
0	<b>Immediate Command Busy (ICB)</b> —R/W. When this bit is read as 0, it indicates that a new command may be issued using the Immediate Command mechanism. When this bit transitions from a 0 to a 1 (using software writing a 1), the controller issues the command currently stored in the Immediate Command register to the codec over the link. When the corresponding response is latched into the Immediate Response register, the controller hardware sets the IRV flag and clears the ICB bit back to 0. Software may write this bit to a 0 if the bit fails to return to 0 after a reasonable time out period. <b>Note:</b> An Immediate Command must not be issued while the CORB/RIRB mechanism is operating; otherwise, the responses conflict. This must be enforced by software.



#### 14.1.2.34 DPLBASE—DMA Position Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 70h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:7	<b>DMA Position Lower Base Address</b> —R/W. Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control and must be programmed with a valid value before the Flush Control bit (HDBAR+08h:bit 1) is set.
6:1	DMA Position Lower Base Unimplemented bits—RO. Hardwired to 0 to force the 128-byte buffer alignment for cache line write optimizations.
0	<b>DMA Position Buffer Enable</b> —R/W. 1 = Controller will write the DMA positions of each of the DMA engines to the buffer in the main memory periodically (typically, once per frame). Software can use this value to know what data in memory is valid data.

#### 14.1.2.35 DPUBASE—DMA Position Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address:HDBAR + 74h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>DMA Position Upper Base Address</b> —R/W. Upper 32 bits of the DMA Position Buffer Base Address. This register must not be written when any DMA engine is running or the DMA transfer may be corrupted.



#### 14.1.2.36 SDCTL—Stream Descriptor Control Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 80h      Attribute: R/W, RO  
Input Stream[1]: HDBAR + A0h  
Input Stream[2]: HDBAR + C0h  
Input Stream[3]: HDBAR + E0h  
Output Stream[0]: HDBAR + 100h  
Output Stream[1]: HDBAR + 120h  
Output Stream[2]: HDBAR + 140h  
Output Stream[3]: HDBAR + 160h

Default Value: 040000h      Size: 24 bits

Bit	Description
23:20	<b>Stream Number</b> —R/W. This value reflects the Tag associated with the data being transferred on the link. When data controlled by this descriptor is sent out over the link, it will have its stream number encoded on the SYNC signal. When an input stream is detected on any of the SDI signals that match this value, the data samples are loaded into FIFO associated with this descriptor. While a single SDI input may contain data from more than one stream number, two different SDI inputs may not be configured with the same stream number. 0000 = Reserved 0001 = Stream 1 ..... 1110 = Stream 14 1111 = Stream 15
19	<b>Bidirectional Direction Control</b> —RO. This bit is only meaningful for bidirectional streams; therefore, this bit is hardwired to 0.
18	<b>Traffic Priority</b> —RO. Hardwired to 1 indicating that all streams will use VC1 if it is enabled through the PCI Express* registers.
17:16	<b>Stripe Control</b> —RO. This bit is only meaningful for input streams; therefore, this bit is hardwired to 0.
15:5	Reserved
4	<b>Descriptor Error Interrupt Enable</b> —R/W 0 = Disable 1 = An interrupt is generated when the Descriptor Error Status bit is set.
3	<b>FIFO Error Interrupt Enable</b> —R/W. This bit controls whether the occurrence of a FIFO error (overrun for input or underrun for output) will cause an interrupt or not. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	<b>Interrupt on Completion Enable</b> —R/W. This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in its descriptor. If this bit is not set, bit 2 in the Status register will be set, but the interrupt will not occur.
1	<b>Stream Run (RUN)</b> —R/W 0 = DMA engine associated with this input stream will be disabled. The hardware will report a 0 in this bit when the DMA engine is actually stopped. Software must read a 0 from this bit before modifying related control registers or restarting the DMA engine. 1 = DMA engine associated with this input stream will be enabled to transfer data from the FIFO to the main memory. The SSYNC bit must also be cleared in order for the DMA engine to run. For output streams, the cadence generator is reset whenever the RUN bit is set.
0	<b>Stream Reset (SRST)</b> —R/W 0 = Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. 1 = Writing a 1 causes the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself) and FIFOs for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. The RUN bit must be cleared before SRST is asserted.



#### 14.1.2.37 SDSTS—Stream Descriptor Status Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 83h      Attribute: R/WC, RO  
                   Input Stream[1]: HDBAR + A3h  
                   Input Stream[2]: HDBAR + C3h  
                   Input Stream[3]: HDBAR + E3h  
                   Output Stream[0]: HDBAR + 103h  
                   Output Stream[1]: HDBAR + 123h  
                   Output Stream[2]: HDBAR + 143h  
                   Output Stream[3]: HDBAR + 163h  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:6	Reserved
5	<b>FIFO Ready (FIFORDY)</b> —RO. For output streams, the controller hardware will set this bit to 1 while the output DMA FIFO contains enough data to maintain the stream on the link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. For input streams, the controller hardware will set this bit to 1 when a valid descriptor is loaded and the engine is ready for the RUN bit to be set.
4	<b>Descriptor Error</b> —R/WC 1 = A serious error occurred during the fetch of a descriptor. This could be a result of a Master Abort, a parity or ECC error on the bus, or any other error that renders the current Buffer Descriptor or Buffer Descriptor list useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stopped. Software may attempt to restart the stream engine after addressing the cause of the error and writing a 1 to this bit to clear it.
3	<b>FIFO Error</b> —R/WC 1 = FIFO error occurred. This bit is set even if an interrupt is not enabled. The bit is cleared by writing a 1 to it. For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers do not increment and the incoming data is not written into the FIFO, thereby being lost. For an output stream, this indicates a FIFO underrun when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there is not valid data to send.
2	<b>Buffer Completion Interrupt Status</b> —R/WC. This bit is set to 1 by the hardware after the last sample of a buffer has been processed, AND if the Interrupt on Completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to it.
1:0	Reserved



#### 14.1.2.38 SDLPIB—Stream Descriptor Link Position in Buffer Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 84h      Attribute: RO

Input Stream[1]: HDBAR + A4h

Input Stream[2]: HDBAR + C4h

Input Stream[3]: HDBAR + E4h

Output Stream[0]: HDBAR + 104h

Output Stream[1]: HDBAR + 124h

Output Stream[2]: HDBAR + 144h

Output Stream[3]: HDBAR + 164h

Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Link Position in Buffer</b> —RO. Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register and then wrap to 0.

#### 14.1.2.39 SDCBL—Stream Descriptor Cyclic Buffer Length Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 88h      Attribute: R/W

Input Stream[1]: HDBAR + A8h

Input Stream[2]: HDBAR + C8h

Input Stream[3]: HDBAR + E8h

Output Stream[0]: HDBAR + 108h

Output Stream[1]: HDBAR + 128h

Output Stream[2]: HDBAR + 148h

Output Stream[3]: HDBAR + 168h

Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Cyclic Buffer Length</b> —R/W. Indicates the number of bytes in the complete cyclic buffer. This register represents an integer number of samples. Link Position in the Buffer will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. This value should only be modified when the RUN bit is 0. Once the RUN bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or transfer may be corrupted.



#### 14.1.2.40 SDLVI—Stream Descriptor Last Valid Index Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 8Ch      Attribute: R/W

Input Stream[1]: HDBAR + ACh  
 Input Stream[2]: HDBAR + CCh  
 Input Stream[3]: HDBAR + ECh  
 Output Stream[0]: HDBAR + 10Ch  
 Output Stream[1]: HDBAR + 12Ch  
 Output Stream[2]: HDBAR + 14Ch  
 Output Stream[3]: HDBAR + 16Ch

Default Value: 0000h      Size: 16 bits

Bit	Description
15:8	Reserved
7:0	<b>Last Valid Index</b> —R/W. The value written to this register indicates the index for the last valid Buffer Descriptor in BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list and continue processing. This field must be at least 1; that is, there must be at least 2 valid entries in the buffer descriptor list before DMA operations can begin. This value should only be modified when the RUN bit is 0.

#### 14.1.2.41 SDFIFOW—Stream Descriptor FIFO Watermark Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 8Eh      Attribute: RO

Input Stream[1]: HDBAR + AEh  
 Input Stream[2]: HDBAR + CEh  
 Input Stream[3]: HDBAR + EEh  
 Output Stream[0]: HDBAR + 10Eh  
 Output Stream[1]: HDBAR + 12Eh  
 Output Stream[2]: HDBAR + 14Eh  
 Output Stream[3]: HDBAR + 16Eh

Default Value: 0004h      Size: 16 bits

Bit	Description
15:3	Reserved
2:0	<b>FIFO Watermark (FIFOW)</b> —RO. Indicates the minimum number of bytes accumulated/free in the FIFO before the controller will start a fetch/eviction of data. The HD Audio Controller hardwires the FIFO Watermark to either 32 B or 64 B based on the number of bytes per frame for the configured input stream. 100 = 32 B (Default) 101 = 64 B Others = Unsupported <b>Note:</b> When the bit field is programmed to an unsupported size, the hardware sets itself to the default value. Software must read the bit field to test if the value is supported after setting the bit field.



#### 14.1.2.42 ISDFIFOS—Input Stream Descriptor FIFO Size Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 90h      Attribute: RW

Input Stream[1]: HDBAR + B0h

Input Stream[2]: HDBAR + D0h

Input Stream[3]: HDBAR + F0h

Output Stream[0]: HDBAR + 110h

Output Stream[1]: HDBAR + 130h

Output Stream[2]: HDBAR + 150h

Output Stream[3]: HDBAR + 170h

Default Value: 0000h

Size: 16 bits

Bit	Description
15:0	<p><b>FIFO Size</b> —RW. When GCAP2.EEACS = 0, it indicates the maximum number of bytes that could be evicted (for input) or fetched (for output) by the controller at one time. This is the maximum number of bytes that may have been received into the hardware buffer but not yet transferred out, and is also the maximum possible value that the PICB count will increase by at one time.</p> <p>The FIFO size is calculated based on factors including the stream format programmed in the SDFMT register. As the default value is zero, software must write to the respective SDFMT register to start the FIFO size calculation, and read back to find out the hardware allocated FIFO size.</p> <p>As the default value is zero, software must write to the &lt;I/O&gt;SD&lt;0:3&gt;FMT register to start the FIFO size calculation, and read back to find out the hardware allocated FIFO size.</p> <p>When GCAP2.EEACS = 1, this FIFO value represents the minimum FIFO size hardware required to operate efficiently. software can program FIFOL register to extend the effective FIFO size in hardware beyond this minimum value advertised. In this case, the maximum number.</p>



#### 14.1.2.43 SDFMT—Stream Descriptor Format Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 92h Attribute: R/W

Input Stream[1]: HDBAR + B2h

Input Stream[2]: HDBAR + D2h

Input Stream[3]: HDBAR + F2h

Output Stream[0]: HDBAR + 112h

Output Stream[1]: HDBAR + 132h

Output Stream[2]: HDBAR + 152h

Output Stream[3]: HDBAR + 172h

Default Value: 0000h

Size: 16 bits

Bit	Description
15	Reserved
14	<b>Sample Base Rate</b> —R/W 0 = 48 KHz 1 = 44.1 KHz
13:11	<b>Sample Base Rate Multiple</b> —R/W 000 = 48 KHz, 44.1 KHz or less 001 = x2 (96 KHz, 88.2 KHz, 32 KHz) 010 = x3 (144 KHz) 011 = x4 (192 KHz, 176.4 KHz) Others = Reserved.
10:8	<b>Sample Base Rate Devisor</b> —R/W 000 = Divide by 1 (48 KHz, 44.1 KHz) 001 = Divide by 2 (24 KHz, 22.05 KHz) 010 = Divide by 3 (16 KHz, 32 KHz) 011 = Divide by 4 (11.025 KHz) 100 = Divide by 5 (9.6 KHz) 101 = Divide by 6 (8 KHz) 110 = Divide by 7 111 = Divide by 8 (6 KHz)
7	Reserved
6:4	<b>Bits per Sample (BITS)</b> —R/W 000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries 001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries 100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries Others = Reserved.
3:0	<b>Number of Channels (CHAN)</b> —R/W. Indicates number of channels in each frame of the stream. 0000 = 1 0001 = 2 ..... 1111 = 16



#### 14.1.2.44 SDBDPL—Stream Descriptor Buffer Descriptor List Pointer Lower Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 98h Attribute: R/W, RO  
Input Stream[1]: HDBAR + B8h  
Input Stream[2]: HDBAR + D8h  
Input Stream[3]: HDBAR + F8h  
Output Stream[0]: HDBAR + 118h  
Output Stream[1]: HDBAR + 138h  
Output Stream[2]: HDBAR + 158h  
Output Stream[3]: HDBAR + 178h

Default Value: 00000000h Size: 32 bits

Bit	Description
31:7	<b>Buffer Descriptor List Pointer Lower Base Address</b> —R/W. Lower address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.
6:0	RO. Hardwired to 0 forcing alignment on 128 B boundaries.

#### 14.1.2.45 SDBDPU—Stream Descriptor Buffer Descriptor List Pointer Upper Base Address Register (Intel® High Definition Audio Controller—D27:F0)

Memory Address: Input Stream[0]: HDBAR + 9Ch Attribute: R/W  
Input Stream[1]: HDBAR + BCh  
Input Stream[2]: HDBAR + DCh  
Input Stream[3]: HDBAR + FCh  
Output Stream[0]: HDBAR + 11Ch  
Output Stream[1]: HDBAR + 13Ch  
Output Stream[2]: HDBAR + 15Ch  
Output Stream[3]: HDBAR + 17Ch

Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Buffer Descriptor List Pointer Upper Base Address</b> —R/W. Upper 32-bit address of the Buffer Descriptor List. This value should only be modified when the RUN bit is 0, or DMA transfer may be corrupted.

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# 15 SMBus Controller Registers (D31:F3)

## 15.1 PCI Configuration Registers (SMBus—D31:F3)

Table 15-1. SMBus Controller PCI Register Address Map (SMBus—D31:F3)

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	8086	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	0280h	RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	05h	RO
0Bh	BCC	Base Class Code	0Ch	RO
10h	SMBMBAR0	Memory Base Address Register 0 (Bit 31:0)	00000004h	R/W, RO
14h	SMBMBAR1	Memory Based Address Register 1 (Bit 63:32)	00000000h	R/W
20h-23h	SMB_BASE	SMBus Base Address	00000001h	R/W, RO
2Ch-2Dh	SVID	Subsystem Vendor Identification	0000h	RO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
40h	HOSTC	Host Configuration	00h	R/W, R/WO

**Note:** Registers that are not shown should be treated as Reserved (See [Section 7.2](#) for details).

### 15.1.1 VID—Vendor Identification Register (SMBus—D31:F3)

Address: 00h-01h  
Default Value: 8086h

Attribute: RO  
Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel.

### 15.1.2 DID—Device Identification Register (SMBus—D31:F3)

Address: 02h–03h      Attribute: RO  
 Default Value: See bit description      Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH SMBus controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

### 15.1.3 PCICMD—PCI Command Register (SMBus—D31:F3)

Address: 04h–05h      Attributes: RO, R/W  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable (IDE)</b> —R/W 0 = Enable 1 = Disables SMBus to assert its PIRQB# signal
9	<b>Fast Back to Back Enable (FBE)</b> —RO. Hardwired to 0.
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = Enables SERR# generation 1 = Disables SERR# generation
7	<b>Wait Cycle Control (WCC)</b> —RO. Hardwired to 0.
6	<b>Parity Error Response (PER)</b> —R/W 0 = Disable 1 = Sets Detected Parity Error bit (D31:F3:06, bit 15) when a parity error is detected.
5	<b>VGA Palette Snoop (VPS)</b> —RO. Hardwired to 0.
4	<b>Postable Memory Write Enable (PMWE)</b> —RO. Hardwired to 0.
3	<b>Special Cycle Enable (SCE)</b> —RO. Hardwired to 0.
2	<b>Bus Master Enable (BME)</b> —RO. Hardwired to 0.
1	<b>Memory Space Enable (MSE)</b> —R/W 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	<b>I/O Space Enable (IOSE)</b> —R/W 0 = Disable 1 = Enables access to the SMBus I/O space registers as defined by the Base Address Register.



### 15.1.4 PCISTS—PCI Status Register (SMBus—D31:F3)

Address: 06h–07h      Attributes: RO, R/WC  
 Default Value: 0280h      Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC 0 = No parity error detected. 1 = Parity error detected.
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No system error detected. 1 = System error detected.
13	<b>Received Master Abort (RMA)</b> —RO. Hardwired to 0.
12	<b>Received Target Abort (RTA)</b> —RO. Hardwired to 0.
11	<b>Signaled Target Abort (STA)</b> —RO. Hardwired to 0.
10:9	<b>DEVSEL# Timing Status (DEVT)</b> —RO. This 2-bit field defines the timing for DEVSEL# assertion for positive decode. 01 = Medium timing.
8	<b>Data Parity Error Detected (DPED)</b> —RO. Hardwired to 0.
7	<b>Fast Back to Back Capable (FB2BC)</b> —RO. Hardwired to 1.
6	<b>User Definable Features (UDF)</b> —RO. Hardwired to 0.
5	<b>66 MHz Capable (66 MHZ_CAP)</b> —RO. Hardwired to 0.
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 0 because there are no capability list structures in this function
3	<b>Interrupt Status (INTS)</b> —RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the PCI Command register.
2:0	Reserved

### 15.1.5 RID—Revision Identification Register (SMBus—D31:F3)

Offset Address: 08h      Attribute: RO  
 Default Value: See bit description      Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See <a href="#">Section 1.4</a> for the value of the RID register.



### 15.1.6 PI—Programming Interface Register (SMBus—D31:F3)

Offset Address: 09h  
Default Value: 00h

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	Reserved

### 15.1.7 SCC—Sub Class Code Register (SMBus—D31:F3)

Address Offset: 0Ah  
Default Value: 05h

Attributes: RO  
Size: 8 bits

Bit	Description
7:0	<b>Sub Class Code (SCC)</b> —RO 05h = SMBus serial controller

### 15.1.8 BCC—Base Class Code Register (SMBus—D31:F3)

Address Offset: 0Bh  
Default Value: 0Ch

Attributes: RO  
Size: 8 bits

Bit	Description
7:0	<b>Base Class Code</b> (BCC)—RO 0Ch = Serial controller.

## 15.1.9 SMBMBAR0—D31\_F3\_SMBus Memory Base Address 0 Register (SMBus—D31:F3)

Address Offset: 10-13h  
Default Value: 00000004h

Attributes: R/W, RO  
Size: 32 bits

Bit	Description
31:8	<b>Base Address</b> —R/W. Provides the 32 byte system memory base address for the PCH SMBus logic.
7:4	Reserved
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that SMBMBAR is not prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO. Indicates that this SMBMBAR can be located anywhere in 64-bit address space. Hardwired to 10b.
0	<b>Memory Space Indicator</b> —RO. This read-only bit is always 0, indicating that the SMBus logic is Memory mapped.

### 15.1.10 SMBMBAR1—D31\_F3\_SMBus Memory Base Address 1 Register (SMBus—D31:F3)

Address Offset: 14h–17h      Attributes: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Base Address</b> —R/W. Provides bits 63:32 system memory base address for the PCH SMBus logic.

### 15.1.11 SMB\_BASE—SMBus Base Address Register (SMBus—D31:F3)

Address Offset: 20–23h      Attribute: R/W, RO  
 Default Value: 00000001h      Size: 32 bits

Bit	Description
31:16	Reserved—RO
15:5	<b>Base Address</b> —R/W. This field provides the 32-byte system I/O base address for the PCH's SMBus logic.
4:1	Reserved—RO
0	I/O Space Indicator—RO. Hardwired to 1 indicating that the SMBus logic is I/O mapped.

### 15.1.12 SVID—Subsystem Vendor Identification Register (SMBus—D31:F2/F4)

Address Offset: 2Ch–2Dh      Attribute: RO  
 Default Value: 0000h      Size: 16 bits  
 Lockable: No      Power Well: Core

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —RO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE SVID register.  <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 15.1.13 SID—Subsystem Identification Register (SMBus—D31:F2/F4)

Address Offset: 2Eh–2Fh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits  
 Lockable: No      Power Well: Core

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. The value returned by reads to this register is the same as that which was written by BIOS into the IDE SID register. <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 15.1.14 INT\_LN—Interrupt Line Register (SMBus—D31:F3)

Address Offset: 3Ch      Attributes: R/W  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is to communicate to software the interrupt line that the interrupt pin is connected to PIRQB#.

### 15.1.15 INT\_PN—Interrupt Pin Register (SMBus—D31:F3)

Address Offset: 3Dh      Attributes: RO  
 Default Value: See description      Size: 8 bits

Bit	Description
7:0	<b>Interrupt PIN (INT_PN)</b> —RO. This reflects the value of D31IP.SMIP in Chipset configuration space.

### 15.1.16 HOSTC—Host Configuration Register (SMBus—D31:F3)

Address Offset: 40h  
Default Value: 00h

Attribute: R/W, R/WO  
Size: 8 bits

Bit	Description
7:5	Reserved
4	<p><b>SPD Write Disable</b>—R/W 0 = SPD write enabled. 1 = SPD write disabled. Writes to SMBus addresses 50h – 57h are disabled.</p> <p><b>Note:</b> This bit is R/WO and will be reset on PLTRST# assertion. This bit should be set by BIOS to '1'. Software can only program this bit when both the START bit (SMB_BASE + 02h, bit 6) and Host Busy bit (SMB_BASE + 00h, bit 0) are '0'; otherwise, the write may result in undefined behavior.</p>
3	<p><b>Soft SMBus Reset (SSRESET)</b>—R/W 0 = The hardware will reset this bit to 0 when SMBus reset operation is completed. 1 = The SMBus state machine and logic in the PCH is reset.</p>
2	<p><b>I<sup>2</sup>C_EN</b>—R/W 0 = SMBus behavior. 1 = The PCH is enabled to communicate with I<sup>2</sup>C devices. This will change the formatting of some commands.</p>
1	<p><b>SMB_SMI_EN</b>—R/W 0 = SMBus interrupts will not generate an SMI#. 1 = Any source of an SMBus interrupt will instead be routed to generate an SMI#. Refer to <a href="#">Section 5.21.4 (Interrupts/SMI#)</a>. This bit needs to be set for SMBALERT# to be enabled.</p>
0	<p><b>SMBus Host Enable (HST_EN)</b>—R/W 0 = Disable the SMBus Host controller. 1 = Enable. The SMBus Host controller interface is enabled to execute commands. The INTREN bit (offset SMB_BASE + 02h, bit 0) needs to be enabled for the SMBus Host controller to interrupt or SMI#. The SMBus Host controller will not respond to any new requests until all interrupt requests have been cleared.</p>

## 15.2 SMBus I/O and Memory Mapped I/O Registers

The SMBus registers (see Table 15-2) can be accessed through I/O BAR or Memory BAR registers in PCI configuration space. The offsets are the same for both I/O and Memory Mapped I/O registers.

**Table 15-2. SMBus I/O and Memory Mapped I/O Register Address Map**

SMB_BASE + Offset	Mnemonic	Register Name	Default	Attribute
00h	HST_STS	Host Status	00h	R/WC, RO
02h	HST_CNT	Host Control	00h	R/W, WO
03h	HST_CMD	Host Command	00h	R/W
04h	XMIT_SLVA	Transmit Slave Address	00h	R/W
05h	HST_D0	Host Data 0	00h	R/W
06h	HST_D1	Host Data 1	00h	R/W
07h	HOST_BLOCK_DB	Host Block Data Byte	00h	R/W
08h	PEC	Packet Error Check	00h	R/W
09h	RCV_SLVA	Receive Slave Address	44h	R/W
0Ah-0Bh	SLV_DATA	Receive Slave Data	0000h	RO
0Ch	AUX_STS	Auxiliary Status	00h	R/WC, RO
0Dh	AUX_CTL	Auxiliary Control	00h	R/W
0Eh	SMLINK_PIN_CTL	SMLink Pin Control (TCO Compatible Mode)	See register description	R/W, RO
0Fh	SMBus_PIN_CTL	SMBus Pin Control	See register description	R/W, RO
10h	SLV_STS	Slave Status	00h	R/WC
11h	SLV_CMD	Slave Command	00h	R/W
14h	NOTIFY_DADDR	Notify Device Address	00h	RO
16h	NOTIFY_DLLOW	Notify Data Low Byte	00h	RO
17h	NOTIFY_DHIGH	Notify Data High Byte	00h	RO

## 15.2.1 HST\_STS—Host Status Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 00h      Attribute: R/WC, RO  
 Default Value: 00h      Size: 8-bits

All status bits are set by hardware and cleared by the software writing a one to the particular bit position. Writing a 0 to any bit position has no effect.

Bit	Description
7	<p><b>Byte Done Status (DS)</b>—R/WC            0 = Software can clear this by writing a 1 to it.            1 = Host controller received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands) when the 32-byte buffer is not being used. This bit will be set, even on the last byte of the transfer. This bit is not set when transmission is due to the LAN interface heartbeat.            This bit has no meaning for block transfers when the 32-byte buffer is enabled.</p> <p><b>Note:</b> When the last byte of a block message is received, the host controller will set this bit. However, it will not immediately set the INTR bit—bit 1 in this register. When the interrupt handler clears the DS bit, the message is considered complete, and the host controller will then set the INTR bit (and generate another interrupt). Thus, for a block message of n bytes, the PCH will generate n+1 interrupts. The interrupt handler needs to be implemented to handle these cases. When not using the 32-Byte Buffer, hardware will drive the SMBCLK signal low when the DS bit is set until software clears the bit. This includes the last byte of a transfer. Software must clear the DS bit before it can clear the BUSY bit.</p>
6	<p><b>INUSE_STS</b>—R/W. This bit is used as a semaphore among various independent software threads that may need to use the PCH's SMBus logic, and has no other effect on hardware.            0 = After a full PCI reset, a read to this bit returns a 0.            1 = After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the host controller.</p>
5	<p><b>SMBALERT_STS</b>—R/WC            0 = Interrupt or SMI# was not generated by SMBALERT#. Software clears this bit by writing a 1 to it.            1 = The source of the interrupt or SMI# was the SMBALERT# signal. This bit is only cleared by software writing a 1 to the bit position or by RSMRST# going low.            If the signal is programmed as a GPIO, then this bit will never be set.</p>
4	<p><b>FAILED</b>—R/WC            0 = Software clears this bit by writing a 1 to it.            1 = The source of the interrupt or SMI# was a failed bus transaction. This bit is set in response to the KILL bit being set to terminate the host transaction.</p>
3	<p><b>BUS_ERR</b>—R/WC            0 = Software clears this bit by writing a 1 to it.            1 = The source of the interrupt or SMI# was a transaction collision.</p>
2	<p><b>DEV_ERR</b>—R/WC            0 = Software clears this bit by writing a 1 to it. The PCH will then de-assert the interrupt or SMI#.            1 = The source of the interrupt or SMI# was due to one of the following:            — Invalid Command Field,            — Unclaimed Cycle (host initiated),            — Host Device Timeout Error.</p>
1	<p><b>INTR</b>—R/WC. This bit can only be set by termination of a command. INTR is not dependent on the INTREN bit (offset SMB_BASE + 02h, bit 0) of the Host controller register (offset 02h). It is only dependent on the termination of the command. If the INTREN bit is not set, then the INTR bit will be set; although, the interrupt will not be generated. Software can poll the INTR bit in this non-interrupt case.            0 = Software clears this bit by writing a 1 to it. The PCH then de-asserts the interrupt or SMI#.            1 = The source of the interrupt or SMI# was the successful completion of its last command.</p>
0	<p><b>HOST_BUSY</b>—R/WC            0 = Cleared by the PCH when the current transaction is completed.            1 = Indicates that the PCH is running a command from the host interface. No SMBus registers should be accessed while this bit is set, except the BLOCK DATA BYTE register. The BLOCK DATA BYTE register can be accessed when this bit is set only when the SMB_CMD bits in the Host Control register are programmed for Block command or I<sup>2</sup>C Read command. This is necessary in order to check the DONE_STS bit.</p>

## 15.2.2 HST\_CNT—Host Control Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 02h      Attribute: R/W, WO  
 Default Value: 00h      Size: 8 bits

**Note:** A read to this register will clear the byte pointer of the 32-byte buffer.

Bit	Description
7	<b>PEC_EN</b> —R/W 0 = SMBus host controller does not perform the transaction with the PEC phase appended. 1 = Causes the host controller to perform the SMBus transaction with the Packet Error Checking phase appended. For writes, the value of the PEC byte is transferred from the PEC register. For reads, the PEC byte is loaded in to the PEC register. This bit must be written prior to the write in which the <b>START</b> bit is set.
6	<b>START</b> —WO 0 = This bit will always return 0 on reads. The HOST_BUSY bit in the Host Status register (offset 00h) can be used to identify when the PCH has finished the command. 1 = Writing a 1 to this bit initiates the command described in the SMB_CMD field. All registers should be setup prior to writing a 1 to this bit position.
5	<b>LAST_BYTE</b> —WO. This bit is used for Block Read commands. 1 = Software sets this bit to indicate that the next byte will be the last byte to be received for the block. This causes the PCH to send a NACK (instead of an ACK) after receiving the last byte.  <b>Note:</b> Once the SECOND_TO_STS bit in TCO2_STS register (D31:F0, TCOBASE+6h, bit 1) is set, the LAST_BYTE bit also gets set. While the SECOND_TO_STS bit is set, the LAST_BYTE bit cannot be cleared. This prevents the PCH from running some of the SMBus commands (Block Read/Write, I <sup>2</sup> C Read, Block I <sup>2</sup> C Write).
4:2	<b>SMB_CMD</b> —R/W. The bit encoding below indicates which command the PCH is to perform. If enabled, the PCH will generate an interrupt or SMI# when the command has completed. If the value is for a non-supported or reserved command, the PCH will set the device error (DEV_ERR) status bit (offset SMB_BASE + 00h, bit 2) and generate an interrupt when the START bit is set. The PCH will perform no command, and will not operate until DEV_ERR is cleared.  000 = <b>Quick</b> : The slave address and read/write value (bit 0) are stored in the transmit slave address register. 001 = <b>Byte</b> : This command uses the transmit slave address and command registers. Bit 0 of the slave address register determines if this is a read or write command. 010 = <b>Byte Data</b> : This command uses the transmit slave address, command, and DATA0 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, the DATA0 register will contain the read data. 011 = <b>Word Data</b> : This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. If it is a read, after the command completes, the DATA0 and DATA1 registers will contain the read data. 100 = <b>Process Call</b> : This command uses the transmit slave address, command, DATA0 and DATA1 registers. Bit 0 of the slave address register determines if this is a read or write command. After the command completes, the DATA0 and DATA1 registers will contain the read data. 101 = <b>Block</b> : This command uses the transmit slave address, command, DATA0 registers, and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block reads, the count is received and stored in the DATA0 register. Bit 0 of the slave address register selects if this is a read or write command. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register. 110 = <b>I<sup>2</sup>C Read</b> : This command uses the transmit slave address, command, DATA0, DATA1 registers, and the Block Data Byte register. The read data is stored in the Block Data Byte register. The PCH continues reading data until the NAK is received. 111 = <b>Block Process</b> : This command uses the transmit slave address, command, DATA0 and the Block Data Byte register. For block write, the count is stored in the DATA0 register and indicates how many bytes of data will be transferred. For block read, the count is received and stored in the DATA0 register. Bit 0 of the slave address register always indicate a write command. For writes, data is retrieved from the first m (where m is equal to the specified count) addresses of the SRAM array. For reads, the data is stored in the Block Data Byte register.  <b>Note:</b> E32B bit in the Auxiliary Control register must be set for this command to work.



Bit	Description
1	<b>KILL</b> —R/W 0 = Normal SMBus host controller functionality. 1 = Kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#). This bit, once set, must be cleared by software to allow the SMBus host controller to function normally.
0	<b>INTREN</b> —R/W 0 = Disable. 1 = Enable the generation of an interrupt or SMI# upon the completion of the command.

### 15.2.3 HST\_CMD—Host Command Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 03h      Attribute: R/W  
Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>HST_CMD</b> – R/W. This 8-bit field is transmitted by the host controller in the command field of the SMBus protocol during the execution of any command.

### 15.2.4 XMIT\_SLVA—Transmit Slave Address Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 04h      Attribute: R/W  
Default Value: 00h      Size: 8 bits

This register is transmitted by the host controller in the slave address field of the SMBus protocol.

Bit	Description
7:1	<b>Address</b> —R/W. This field provides a 7-bit address of the targeted slave.
0	<b>RW</b> —R/W. Direction of the host transfer. 0 = Write 1 = Read <b>Note:</b> Writes to SMBus addresses 50h - 57h are disabled depending on the setting of bit 4 in HOSTC register (D31:F3:Offset 40h).

### 15.2.5 HST\_D0—Host Data 0 Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 05h      Attribute: R/W  
Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Data0/Count</b> —R/W. This field contains the 8-bit data sent in the DATA0 field of the SMBus protocol. For block write commands, this register reflects the number of bytes to transfer. This register should be programmed to a value between 1 and 32 for block counts. A count of 0 or a count above 32 will result in unpredictable behavior. The host controller does not check or log invalid block counts.

### 15.2.6 HST\_D1—Host Data 1 Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 06h      Attribute: R/W  
Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Data1</b> —R/W. This 8-bit register is transmitted in the DATA1 field of the SMBus protocol during the execution of any command.

### 15.2.7 Host\_BLOCK\_DB—Host Block Data Byte Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 07h      Attribute: R/W  
Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Block Data (BDTA)</b> —R/W. This is either a register, or a pointer into a 32-byte block array, depending upon whether the E32B bit is set in the Auxiliary Control register. When the E32B bit (offset SMB_BASE + 0Dh, bit 1) is cleared, this is a register containing a byte of data to be sent on a block write or read from on a block read. When the E32B bit is set, reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array, which is reset to 0 by reading the HCTL register (offset 02h). The index pointer then increments automatically upon each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0. When the E2B bit is set, for writes, software will write up to 32-bytes to this register as part of the setup for the command. After the Host controller has sent the Address, Command, and Byte Count fields, it will send the bytes in the SRAM pointed to by this register. When the E2B bit is cleared for writes, software will place a single byte in this register. After the host controller has sent the address, command, and byte count fields, it will send the byte in this register. If there is more data to send, software will write the next series of bytes to the SRAM pointed to by this register and clear the DONE_STS bit. The controller will then send the next byte. During the time between the last byte being transmitted to the next byte being transmitted, the controller will insert wait-states on the interface. When the E2B bit is set for reads, after receiving the byte count into the Data0 register, the first series of data bytes go into the SRAM pointed to by this register. If the byte count has been exhausted or the 32-byte SRAM has been filled, the controller will generate an SMI# or interrupt (depending on configuration) and set the DONE_STS bit. Software will then read the data. During the time between when the last byte is read from the SRAM to when the DONE_STS bit is cleared, the controller will insert wait-states on the interface.

### 15.2.8 PEC—Packet Error Check (PEC) Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 08h      Attribute: R/W  
Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>PEC_DATA</b> —R/W. This 8-bit register is written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software. Software must ensure that the INUSE_STS bit is properly maintained to avoid having this field over-written by a write transaction following a read transaction.



### 15.2.9 RCV\_SLVA—Receive Slave Address Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 09h      Attribute: R/W  
 Default Value: 44h      Size: 8 bits  
 Lockable: No      Power Well: Resume

Bit	Description
7	Reserved
6:0	<b>SLAVE_ADDR</b> —R/W. This field is the slave address that the PCH decodes for read and write cycles. The default is not 0, so the SMBus Slave Interface can respond even before the processor comes up (or if the processor is dead). This register is cleared by RSMRST#, but not by PLTRST#.

### 15.2.10 SLV\_DATA—Receive Slave Data Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 0Ah–0Bh      Attribute: RO  
 Default Value: 0000h      Size: 16 bits  
 Lockable: No      Power Well: Resume

This register contains the 16-bit data value written by the external SMBus master. The processor can then read the value from this register. This register is reset by RSMRST#, but not PLTRST#.

Bit	Description
15:8	<b>Data Message Byte 1 (DATA_MSG1)</b> —RO. See <a href="#">Section 5.21.7</a> for a discussion of this field.
7:0	<b>Data Message Byte 0 (DATA_MSG0)</b> —RO. See <a href="#">Section 5.21.7</a> for a discussion of this field.

### 15.2.11 AUX\_STS—Auxiliary Status Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 0Ch      Attribute: R/WC, RO  
 Default Value: 00h      Size: 8 bits  
 Lockable: No      Power Well: Resume

Bit	Description
7:2	Reserved
1	<b>SMBus TCO Mode (STCO)</b> —RO. This bit reflects the strap setting of TCO compatible mode versus Advanced TCO mode. 0 = The PCH is in the compatible TCO mode. 1 = The PCH is in the advanced TCO mode.
0	<b>CRC Error (CRCE)</b> —R/WC. 0 = Software clears this bit by writing a 1 to it. 1 = This bit is set if a received message contained a CRC error. When this bit is set, the DERR bit of the host status register will also be set. This bit will be set by the controller if a software abort occurs in the middle of the CRC portion of the cycle or an abort happens after the PCH has received the final data bit transmitted by an external slave.

### 15.2.12 AUX\_CTL—Auxiliary Control Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 0Dh      Attribute: R/W  
 Default Value: 00h      Size: 8 bits  
 Lockable: No      Power Well: Resume

Bit	Description
7:2	Reserved
1	<b>Enable 32-Byte Buffer (E32B)</b> —R/W 0 = Disable. 1 = Enable. When set, the Host Block Data register is a pointer into a 32-byte buffer, as opposed to a single register. This enables the block commands to transfer or receive up to 32-bytes before the PCH generates an interrupt.
0	<b>Automatically Append CRC (AAC)</b> —R/W 0 = The PCH will Not automatically append the CRC. 1 = The PCH will automatically append the CRC. This bit must not be changed during SMBus transactions or undetermined behavior will result. It should be programmed only once during the lifetime of the function.

### 15.2.13 SMLINK\_PIN\_CTL—SMLink Pin Control Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 0Eh      Attribute: R/W, RO  
 Default Value: See below      Size: 8 bits

**Note:** This register is in the resume well and is reset by RSMRST#.

This register is only applicable in the TCO compatible mode.

Bit	Description
7:3	Reserved
2	<b>SMLINK_CLK_CTL</b> —R/W. 0 = The PCH will drive the SMLink0 pin low, independent of what the other SMLink logic would otherwise indicate for the SMLink0 pin. 1 = The SMLink0 pin is <b>not</b> overdriven low. The other SMLink logic controls the state of the pin. (Default)
1	<b>SMLINK1_CUR_STS</b> —RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMLink1 pin. This allows software to read the current state of the pin. 0 = Low 1 = High
0	<b>SMLINK0_CUR_STS</b> —RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMLink0 pin. This allows software to read the current state of the pin. 0 = Low 1 = High

### 15.2.14 SMBus\_PIN\_CTL—SMBus Pin Control Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 0Fh Attribute: R/W, RO  
 Default Value: See below Size: 8 bits

**Note:** This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:3	Reserved
2	<b>SMBCLK_CTL</b> —R/W 1 = The SMBCLK pin is <b>not</b> overdriven low. The other SMBus logic controls the state of the pin. 0 = The PCH drives the SMBCLK pin low, independent of what the other SMBus logic would otherwise indicate for the SMBCLK pin. (Default)
1	<b>SMBDATA_CUR_STS</b> —RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBDATA pin. This allows software to read the current state of the pin. 0 = Low 1 = High
0	<b>SMBCLK_CUR_STS</b> —RO. This read-only bit has a default value that is dependent on an external signal level. This pin returns the value on the SMBCLK pin. This allows software to read the current state of the pin. 0 = Low 1 = High

### 15.2.15 SLV\_STS—Slave Status Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 10h Attribute: R/WC  
 Default Value: 00h Size: 8 bits

**Note:** This register is in the resume well and is reset by RSMRST#.

All bits in this register are implemented in the 64 KHz clock domain. Therefore, software must poll this register until a write takes effect before assuming that a write has completed internally.

Bit	Description
7:1	Reserved
0	<b>HOST_NOTIFY_STS</b> —R/WC. The PCH sets this bit to a 1 when it has completely received a successful Host Notify Command on the SMBus pins. Software reads this bit to determine that the source of the interrupt or SMI# was the reception of the Host Notify Command. Software clears this bit after reading any information needed from the Notify address and data registers by writing a 1 to this bit. The PCH will allow the Notify Address and Data registers to be over-written once this bit has been cleared. When this bit is 1, the PCH will NACK the first byte (host address) of any new "Host Notify" commands on the SMBus pins. Writing a 0 to this bit has no effect.

### 15.2.16 SLV\_CMD—Slave Command Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 11h      Attribute: R/W  
 Default Value: 00h      Size: 8 bits

**Note:** This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:2	Reserved
2	<b>SMBALERT_DIS</b> —R/W 0 = Allows the generation of the interrupt or SMI#. 1 = Software sets this bit to block the generation of the interrupt or SMI# due to the SMBALERT# source. This bit is logically inverted and ANDed with the SMBALERT_STS bit (offset SMB_BASE + 00h, bit 5). The resulting signal is distributed to the SMI# and/or interrupt generation logic. This bit does not effect the wake logic.
1	<b>HOST_NOTIFY_WKEN</b> —R/W. Software sets this bit to 1 to enable the reception of a Host Notify command as a wake event. When enabled, this event is "OR'd" in with the other SMBus wake events and is reflected in the SMB_WAK_STS bit of the General Purpose Event 0 Status register. 0 = Disable 1 = Enable
0	<b>HOST_NOTIFY_INTREN</b> —R/W. Software sets this bit to 1 to enable the generation of interrupt or SMI# when HOST_NOTIFY_STS (offset SMB_BASE + 10h, bit 0) is 1. This enable does not affect the setting of the HOST_NOTIFY_STS bit. When the interrupt is generated, either PIRQB# or SMI# is generated, depending on the value of the SMB_SMI_EN bit (D31:F3:40h, bit 1). If the HOST_NOTIFY_STS bit is set when this bit is written to a 1, then the interrupt (or SMI#) will be generated. The interrupt (or SMI#) is logically generated by AND'ing the STS and INTREN bits. 0 = Disable 1 = Enable

### 15.2.17 NOTIFY\_DADDR—Notify Device Address Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 14h      Attribute: RO  
 Default Value: 00h      Size: 8 bits

**Note:** This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:1	<b>DEVICE_ADDRESS</b> —RO. This field contains the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 Specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMB_BASE + 10, bit 0) is set to 1.
0	Reserved



### 15.2.18 NOTIFY\_DLOW—Notify Data Low Byte Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 16h      Attribute: RO  
 Default Value: 00h      Size: 8 bits

**Note:** This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	<b>DATA_LOW_BYTE</b> —RO. This field contains the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMB_BASE +10, bit 0) is set to 1.

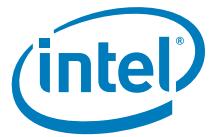
### 15.2.19 NOTIFY\_DHIGH—Notify Data High Byte Register (SMBus—D31:F3)

Register Offset: SMB\_BASE + 17h      Attribute: RO  
 Default Value: 00h      Size: 8 bits

**Note:** This register is in the resume well and is reset by RSMRST#.

Bit	Description
7:0	<b>DATA_HIGH_BYTE</b> —RO. This field contains the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 specification. Software should only consider this field valid when the HOST_NOTIFY_STS bit (D31:F3:SMB_BASE +10, bit 0) is set to 1.

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# 16 High Precision Event Timer Registers

The timer registers are memory-mapped in a non-indexed scheme. This allows the processor to directly access each register without having to use an index register. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. There are four possible memory address ranges beginning at 1) FED0\_0000h, 2) FED0\_1000h, 3) FED0\_2000h, 4) FED0\_3000h. The choice of address range will be selected by configuration bits in the High Precision Timer Configuration Register (Chipset Configuration Registers:Offset 3404h).

Behavioral Rules:

1. Software must not attempt to read or write across register boundaries. For example, a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. Any accesses to these offsets will result in an unexpected behavior, and may result in a master abort. However, these accesses should not result in system hangs. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.

## 16.1 Memory Mapped Registers

**Table 16-1. Memory-Mapped Register Address Map (Sheet 1 of 2)**

Offset	Mnemonic	Register	Default	Attribute
000h-007h	GCAP_ID	General Capabilities and Identification	0429B17F8086 A201h	RO
008h-00Fh	—	Reserved	—	—
010h-017h	GEN_CONF	General Configuration	000000000000 0000h	R/W
018h-01Fh	—	Reserved	—	—
020h-027h	GINTR_STA	General Interrupt Status	000000000000 0000h	R/WC
028h-0EFh	—	Reserved	—	—
0F0h-0F7h	MAIN_CNT	Main Counter Value	N/A	R/W
0F8h-0FFh	—	Reserved	—	—
100h-107h	TIM0_CONF	Timer 0 Configuration and Capabilities	N/A	R/W, RO
108h-10Fh	TIM0_COMP	Timer 0 Comparator Value	N/A	R/W
110h-11Fh	—	Reserved	—	—
120h-127h	TIM1_CONF	Timer 1 Configuration and Capabilities	N/A	R/W, RO
128h-12Fh	TIM1_COMP	Timer 1 Comparator Value	N/A	R/W
130h-13Fh	—	Reserved	—	—
140h-147h	TIM2_CONF	Timer 2 Configuration and Capabilities	N/A	R/W, RO

**Table 16-1. Memory-Mapped Register Address Map (Sheet 2 of 2)**

Offset	Mnemonic	Register	Default	Attribute
148h-14Fh	TIM2_COMP	Timer 2 Comparator Value	N/A	R/W
150h-15Fh	—	Reserved	—	—
160h-167h	TIM3_CONG	Timer 3 Configuration and Capabilities	N/A	R/W, RO
168h-16Fh	TIM3_COMP	Timer 3 Comparator Value	N/A	R/W
180h-187h	TIM4_CONG	Timer 4 Configuration and Capabilities	N/A	R/W, RO
188h-18Fh	TIM4_COMP	Timer 4 Comparator Value	N/A	R/W
190h-19Fh	—	Reserved	—	—
1A0h-1A7h	TIM5_CONG	Timer 5 Configuration and Capabilities	N/A	R/W, RO
1A8h-1AFh	TIM5_COMP	Timer 5 Comparator Value	N/A	R/W
1B0h-1BFh	—	Reserved	—	—
1C0h-1C7h	TIM6_CONG	Timer 6 Configuration and Capabilities	N/A	R/W, RO
1C8h-1CFh	TIM6_COMP	Timer 6 Comparator Value	N/A	R/W
1D0h-1DFh	—	Reserved	—	—
1E0h-1E7h	TIM7_CONG	Timer 7 Configuration and Capabilities	N/A	R/W, RO
1E8h-1EFh	TIM7_COMP	Timer 7 Comparator Value	N/A	R/W
1F0h-19Fh	—	Reserved	—	—
200h-3FFh	—	Reserved	—	—

**NOTES:**

1. Reads to reserved registers or bits will return a value of 0.
2. Software must not attempt locks to the memory-mapped I/O ranges for High Precision Event Timers. If attempted, the lock is not honored, which means potential deadlock conditions may occur.

### 16.1.1 GCAP\_ID—General Capabilities and Identification Register

Address Offset: 00h Attribute: RO  
 Default Value: 0429B17F8086A201h Size: 64 bits

Bit	Description
63:32	<b>Main Counter Tick Period (COUNTER_CLK_PER_CAP)</b> —RO. This field indicates the period at which the counter increments in femtoseconds ( $10^{-15}$ seconds). This will return 0429B17Fh when read. This indicates a period of 69841279 fs (69.841279 ns).
31:16	<b>Vendor ID Capability (VENDOR_ID_CAP)</b> —RO. This is a 16-bit value assigned to Intel.
15	<b>Legacy Replacement Rout Capable (LEG_RT_CAP)</b> —RO. Hardwired to 1. Legacy Replacement Interrupt Rout option is supported.
14	Reserved. This bit returns 0 when read.
13	<b>Counter Size Capability (COUNT_SIZE_CAP)</b> —RO. Hardwired to 1. Counter is 64-bit wide.
12:8	<b>Number of Timer Capability (NUM_TIM_CAP)</b> —RO. This field indicates the number of timers in this block. 07h = Eight timers.
7:0	<b>Revision Identification (REV_ID)</b> —RO. This field indicates which revision of the function is implemented. Default value will be 01h.

### 16.1.2 GEN\_CONF—General Configuration Register

Address Offset: 010h Attribute: R/W  
 Default Value: 00000000 00000000h Size: 64 bits

Bit	Description
63:2	Reserved. These bits return 0 when read.
1	<b>Legacy Replacement Rout (LEG_RT_CNF)</b> —R/W. If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, the interrupts will be routed as follows: <ul style="list-style-type: none"> <li>• Timer 0 is routed to IRQ0 in 8259 or IRQ2 in the I/O APIC</li> <li>• Timer 1 is routed to IRQ8 in 8259 or IRQ8 in the I/O APIC</li> <li>• Timer 2-n is routed as per the routing in the timer n Configuration registers.</li> <li>• If the Legacy Replacement Rout bit is set, the individual routing bits for Timers 0 and 1 (APIC) will have no impact.</li> <li>• If the Legacy Replacement Rout bit is not set, the individual routing bits for each of the timers are used.</li> <li>• This bit will default to 0. BIOS can set it to 1 to enable the legacy replacement routing, or 0 to disable the legacy replacement routing.</li> </ul>
0	<b>Overall Enable (ENABLE_CNF)</b> —R/W. This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers. For level-triggered interrupts, if an interrupt is pending when the ENABLE_CNF bit is changed from 1 to 0, the interrupt status indications (in the various Txx_INT_STS bits) will not be cleared. Software must write to the Txx_INT_STS bits to clear the interrupts. <b>NOTE:</b> This bit will default to 0. BIOS can set it to 1 or 0.

### 16.1.3 GINTR\_STA—General Interrupt Status Register

Address Offset: 020h Attribute: R/WC  
 Default Value: 00000000 00000000h Size: 64 bits

Bit	Description
63:8	Reserved. These bits will return 0 when read.
7	<b>Timer 7 Interrupt Active (T07_INT_STS)</b> —R/WC. Same functionality as Timer 0.
6	<b>Timer 6 Interrupt Active (T06_INT_STS)</b> —R/WC. Same functionality as Timer 0.
5	<b>Timer 5 Interrupt Active (T05_INT_STS)</b> —R/WC. Same functionality as Timer 0.
4	<b>Timer 4 Interrupt Active (T04_INT_STS)</b> —R/WC. Same functionality as Timer 0.
3	<b>Timer 3 Interrupt Active (T03_INT_STS)</b> —R/WC. Same functionality as Timer 0.
2	<b>Timer 2 Interrupt Active (T02_INT_STS)</b> —R/WC. Same functionality as Timer 0.
1	<b>Timer 1 Interrupt Active (T01_INT_STS)</b> —R/WC. Same functionality as Timer 0.
0	<p><b>Timer 0 Interrupt Active (T00_INT_STS)</b>—R/WC. The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer.          (default = 0)</p> <p>If set to level-triggered mode:          This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. Writes of 0 to this bit will have no effect.</p> <p>If set to edge-triggered mode:          This bit should be ignored by software. Software should always write 0 to this bit.</p> <p><b>NOTE:</b> Defaults to 0. In edge triggered mode, this bit will always read as 0 and writes will have no effect.</p>

### 16.1.4 MAIN\_CNT—Main Counter Value Register

Address Offset: 0F0h Attribute: R/W  
 Default Value: N/A Size: 64 bits

Bit	Description
63:0	<p><b>Counter Value (COUNTER_VAL[63:0])</b>—R/W. Reads return the current value of the counter.          Writes load the new value to the counter.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>1. Writes to this register should only be done while the counter is halted.</li> <li>2. Reads to this register return the current value of the main counter.</li> <li>3. 32-bit counters will always return 0 for the upper 32-bits of this register.</li> <li>4. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this delays the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode.</li> <li>5. Reads to this register are monotonic. No two consecutive reads return the same value. The second of two reads always returns a larger value (unless the timer has rolled over to 0).</li> </ol>



## 16.1.5 TIM<sub>n</sub>\_CONF—Timer n Configuration and Capabilities Register

Address Offset: Timer 0: 100–107h, Attribute: RO, R/W  
 Timer 1: 120–127h,  
 Timer 2: 140–147h,  
 Timer 3: 160–167h,  
 Timer 4: 180–187h,  
 Timer 5: 1A0–1A7h,  
 Timer 6: 1C0–1C7h,  
 Timer 7: 1E0–1E7h,  
 Default Value: N/A Size: 64 bit

**Note:** The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7.

Bit	Description
63:56	Reserved. These bits will return 0 when read.
55:52, 44, 43	<p><b>Timer Interrupt Rout Capability (TIMER<sub>n</sub>_INT_ROUT_CAP)</b>—RO            Timer 0, 1: Bits 52, 53, 54, and 55 in this field (corresponding to IRQ 20, 21, 22, and 23) have a value of 1. Writes will have no effect.            Timer 2: Bits 43, 52, 53, 54, and 55 in this field (corresponding to IRQ 11, 20, 21, 22, and 23) have a value of 1. Writes will have no effect.            Timer 3: Bits 44, 52, 53, 54, and 55 in this field (corresponding to IRQ 11, 20, 21, 22, and 23) have a value of 1. Writes will have no effect.            Timer 4, 5, 6, 7: This field is always 0 as interrupts from these timers can only be delivered using direct processor interrupt messages.</p> <p><b>NOTE:</b> If IRQ 11 is used for HPET #2, software should ensure IRQ 11 is not shared with any other devices to ensure the proper operation of HPET #2.</p> <p><b>NOTE:</b> If IRQ 12 is used for HPET #3, software should ensure IRQ 12 is not shared with any other devices to ensure the proper operation of HPET #3.</p>
51:45, 42:16	Reserved. These bits return 0 when read.
15	<b>Timer n Processor Message Interrupt Delivery (Tn_PROCMSG_INT_DEL_CAP)</b> —RO This bit is always read as '1', since the PCH HPET implementation supports the direct processor interrupt delivery.
14	<p><b>Timer n Processor Message Interrupt Enable (Tn_PROCMSG_EN_CNF)</b>—R/W/RO. If the Tn_PROCMSG_INT_DEL_CAP bit is set for this timer, then the software can set the Tn_PROCMSG_EN_CNF bit to force the interrupts to be delivered directly as processor messages, rather than using the 8259 or I/O (x) APIC. In this case, the Tn_INT_ROUT_CNF field in this register will be ignored. The Tn_PROCMSG_ROUT register will be used instead.</p> <p>Timer 0, 1, 2, 3 Specific: This bit is a read/write bit.            Timer 4, 5, 6, 7 Specific: This bit is always Read Only '1' as interrupt from these timers can only be delivered using direct processor interrupt messages.</p>
13:9	<p><b>Timer n Interrupt Rout (Tn_INT_ROUT_CNF)</b>—R/W/RO. This 5-bit field indicates the routing for the interrupt to the 8259 or I/O (x) APIC. Software writes to this field to select which interrupt in the 8259 or I/O (x) will be used for this timer's interrupt. If the value is not supported by this particular timer, then the value read back will not match what is written. The software must only write valid values.</p> <p>Timer 4, 5, 6, 7: This field is read-only and reads will return 0.</p> <p><b>NOTES:</b></p> <ol style="list-style-type: none"> <li>If the interrupt is handled using the 8259, only interrupts 0–15 are applicable and valid. Software must not program any value other than 0–15 in this field.</li> <li>If the Legacy Replacement Rout bit is set, then Timers 0 and 1 will have a different routing, and this bit field has no effect for those two timers.</li> <li>Timer 0,1: Software is responsible to make sure it programs a valid value (20, 21, 22, or 23) for this field. The PCH logic does not check the validity of the value written.</li> <li>Timer 2: Software is responsible to make sure it programs a valid value (11, 20, 21, 22, or 23) for this field. The PCH logic does not check the validity of the value written.</li> <li>Timer 3: Software is responsible to make sure it programs a valid value (12, 20, 21, 22, or 23) for this field. The PCH logic does not check the validity of the value written.</li> <li>Timers 4, 5, 6, 7: This field is always Read Only 0 as interrupts from these timers can only be delivered using direct processor interrupt messages.</li> </ol>

Bit	Description
8	<b>Timer n 32-bit Mode (TIMERn_32MODE_CNF)</b> —R/W or RO. Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. Timer 0: Bit is read/write (default to 0). 0 = 64 bit; 1 = 32 bits Timers 1, 2, 3, 4, 5, 6, 7: Hardwired to 0. Writes have no effect (since these seven timers are 32 bits). <b>NOTE:</b> When this bit is set to 1, the hardware counter will do a 32-bit operation on comparator match and rollovers; thus, the upper 32-bit of the Timer 0 Comparator Value register is ignored. The upper 32-bit of the main counter is not involved in any rollover from lower 32-bit of the main counter and becomes all zeros.
7	Reserved. This bit returns 0 when read.
6	<b>Timer n Value Set (TIMERn_VAL_SET_CNF)</b> —R/W. Software uses this bit only for Timer 0 if it has been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timer's accumulator. Software does <b>not</b> have to write this bit back to 1 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode. <b>NOTE:</b> This bit will return 0 when read. Writes will only have an effect for Timer 0 if it is set to periodic mode. Writes will have no effect for Timers 1, 2, 3, 4, 5, 6, 7.
5	<b>Timer n Size (TIMERn_SIZE_CAP)</b> —RO. This read only field indicates the size of the timer. Timer 0: Value is 1 (64-bits). Timers 1, 2, 3, 4, 5, 6, 7: Value is 0 (32 bits).
4	<b>Periodic Interrupt Capable (TIMERn_PER_INT_CAP)</b> —RO. If this bit is 1, the hardware supports a periodic mode for this timer's interrupt. Timer 0: Hardwired to 1 (supports the periodic interrupt). Timers 1, 2, 3, 4, 5, 6, 7: Hardwired to 0 (does not support periodic interrupt).
3	<b>Timer n Type (TIMERn_TYPE_CNF)</b> —R/W or RO. Timer 0: Bit is read/write. 0 = Disable timer to generate periodic interrupt; 1 = Enable timer to generate a periodic interrupt. Timers 1, 2, 3, 4, 5, 6, 7: Hardwired to 0. Writes have no affect.
2	<b>Timer n Interrupt Enable (TIMERn_INT_ENB_CNF)</b> —R/W. This bit must be set to enable timer n to cause an interrupt when it times out. 0 = Disable (Default). The timer can still count and generate appropriate status bits, but will not cause an interrupt. 1 = Enable.
1	<b>Timer Interrupt Type (TIMERn_INT_TYPE_CNF)</b> —R/W. 0 = The timer interrupt is edge triggered. This means that an edge-type interrupt is generated. If another interrupt occurs, another edge will be generated. 1 = The timer interrupt is level triggered. This means that a level-triggered interrupt is generated. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active. Timer 4, 5, 6, 7: This bit is Read Only, and will return 0 when read
0	Reserved. These bits will return 0 when read.

**NOTE:** Reads or writes to unimplemented timers should not be attempted. Read from any unimplemented registers will return an undetermined value.

## 16.1.6 **TIM<sub>n</sub>\_COMP**—Timer n Comparator Value Register

Address Offset: Timer 0: 108h-10Fh,  
 Timer 1: 128h-12Fh,  
 Timer 2: 148h-14Fh,  
 Timer 3: 168h-16Fh,  
 Timer 4: 188h-18Fh,  
 Timer 5: 1A8h-1AFh,  
 Timer 6: 1C8h-1CFh,  
 Timer 7: 1E8h-1EFh

Default Value: N/A      Attribute: R/W  
                             Size: 64 bit

Bit	Description
63:0	<p><b>Timer Compare Value</b>—R/W. Reads to this register return the current value of the comparator</p> <p>If Timer n is configured to non-periodic mode:    Writes to this register load the value against which the main counter should be compared for this timer.</p> <ul style="list-style-type: none"> <li>When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled).</li> <li>The value in this register does not change based on the interrupt being generated.</li> </ul> <p>If Timer 0 is configured to periodic mode:</p> <ul style="list-style-type: none"> <li>When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled).</li> <li>After the main counter equals the value in this register, the value in this register is increased by the value last written to the register.</li> </ul> <p>For example, if the value written to the register is 00000123h, then</p> <ol style="list-style-type: none"> <li>An interrupt will be generated when the main counter reaches 00000123h.</li> <li>The value in this register will then be adjusted by the hardware to 00000246h.</li> <li>Another interrupt will be generated when the main counter reaches 00000246h</li> <li>The value in this register will then be adjusted by the hardware to 00000369h</li> </ol> <ul style="list-style-type: none"> <li>As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000h, then after the next interrupt the value will change to 00010000h</li> </ul> <p>Default value for each timer is all 1s for the bits that are implemented. For example, a 32-bit timer has a default value of 00000000FFFFFFFFFFh. A 64-bit timer has a default value of FFFFFFFFFFFFFFh.</p>

### 16.1.7 **TIMERn\_PROCMMSG\_ROUT—Timer n Processor Message Interrupt Rout Register**

Address Offset: Timer 0: 110–117h, Attribute: R/W  
Timer 1: 130–137h,  
Timer 2: 150–157h,  
Timer 3: 170–177h,  
Timer 4: 190–197h,  
Timer 5: 1B0–1B7h,  
Timer 6: 1D0–1D7h,  
Timer 7: 1F0–1F7h,  
Default Value: N/A Size: 64 bit

**Note:** The letter n can be 0, 1, 2, 3, 4, 5, 6, or 7 referring to Timer 0, 1, 2, 3, 4, 5, 6, or 7.

Software can access the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses can be done to offset 1x0h or 1x4h. 64-bit accesses can be done to 1x0h. 32-bit accesses must not be done to offsets 1x1h, 1x2h, 1x3h, 1x5h, 1x6h, or 1x7h.

Bit	Description
63:32	<b>Tn_PROCMMSG_INT_ADDR</b> —R/W. Software sets this 32-bit field to indicate the location that the direct processor interrupt message should be written. <b>NOTE:</b> Bits 33:32 are read-only of '00'.
31:0	<b>Tn_PROCMMSG_INT_VAL</b> —R/W. Software sets this 32-bit field to indicate that value that is written during the direct processor interrupt message.

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# 17 PCI Express\* Configuration Registers

## 17.1 PCI Express\* Configuration Registers (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

**Note:** This section assumes the default PCI Express\* Function Number-to-Root Port mapping is used. Function numbers for a given root port are assignable through the Root Port Function Number and Hide for PCI Express\* Root Ports register (RCBA+0238h).

**Note:** Register address locations that are not shown in [Table 17-1](#), should be treated as Reserved.

**Table 17-1. PCI Express\* Configuration Registers Address Map (PCI Express\*—D28:F0/F1/F2/F3/F4/F5) (Sheet 1 of 3)**

Offset	Mnemonic	Register Name	Function 0–7 Default	Attribute
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	R/WC, RO
08h	RID	Revision Identification	See register description	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	04h	RO
0Bh	BCC	Base Class Code	06h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary Latency Timer	00h	RO
0Eh	HEADTYP	Header Type	81h	RO
18h–1Ah	BNUM	Bus Number	000000h	R/W
1Bh	SLT	Secondary Latency Timer	00h	RO
1Ch–1Dh	IOBL	I/O Base and Limit	0000h	R/W, RO
1Eh–1Fh	SSTS	Secondary Status Register	0000h	R/WC
20h–23h	MBL	Memory Base and Limit	00000000h	R/W
24h–27h	PMBL	Prefetchable Memory Base and Limit	00010001h	R/W, RO
28h–2Bh	PMBU32	Prefetchable Memory Base Upper 32 Bits	00000000h	R/W
2Ch–2Fh	PMLU32	Prefetchable Memory Limit Upper 32 Bits	00000000h	R/W
34h	CAPP	Capabilities List Pointer	40h	RO
3Ch–3Dh	INTR	Interrupt Information	See bit description	R/W, RO
3Eh–3Fh	BCTRL	Bridge Control Register	0000h	R/W
40h–41h	CLIST	Capabilities List	8010h	RO
42h–43h	XCAP	PCI Express* Capabilities	0042h	R/WO, RO
44h–47h	DCAP	Device Capabilities	00008000h	RO
48h–49h	DCTL	Device Control	0000h	R/W, RO

**Table 17-1. PCI Express\* Configuration Registers Address Map  
(PCI Express\*-D28:F0/F1/F2/F3/F4/F5) (Sheet 2 of 3)**

Offset	Mnemonic	Register Name	Function 0-7 Default	Attribute
4Ah-4Bh	DSTS	Device Status	0010h	R/WC, RO
4Ch-4Fh	LCAP	Link Capabilities	See bit description	RO, R/WO
50h-51h	LCTL	Link Control	0000h	R/W, RO
52h-53h	LSTS	Link Status	See bit description	RO
54h-57h	SLCAP	Slot Capabilities Register	00060060h	R/WO, RO
58h-59h	SLCTL	Slot Control	0000h	R/W, RO
5Ah-5Bh	SLSTS	Slot Status	0000h	R/WC, RO
5Ch-5Dh	RCTL	Root Control	0000h	R/W
60h-63h	RSTS	Root Status	00000000h	R/WC, RO
64h-67h	DCAP2	Device Capabilities 2 Register	00080816h	R/WO, RO
68h-69h	DCTL2	Device Control 2 Register	0000h	R/W, RO
70h-71h	LCTL2	Link Control 2 Register	0002h	R/W
72h-73h	LSTS2	Link Status 2 Register	0000h	RO
80h-81h	MID	Message Signaled Interrupt Identifiers	9005h	RO
82h-83h	MC	Message Signaled Interrupt Message Control	0000h	R/W, RO
84h-87h	MA	Message Signaled Interrupt Message Address	00000000h	R/W
88h-89h	MD	Message Signaled Interrupt Message Data	0000h	R/W
90h-91h	SVCAP	Subsystem Vendor Capability	A00Dh	R/WO, RO
94h-97h	SVID	Subsystem Vendor Identification	00000000h	R/WO
A0h-A1h	PMCAP	Power Management Capability	0001h	RO
A2h-A3h	PMC	PCI Power Management Capability	C803h	RO
A4h-A7h	PMCS	PCI Power Management Control and Status	00000000h	R/W, RO
D4h-D7h	MPC2	Miscellaneous Port Configuration 2	00000800h	R/W, RO
D8h-DBh	MPC	Miscellaneous Port Configuration	09110000h	R/W, RO, R/WO
DCh-DFh	SMSCS	SMI/SCI Status Register	00000000h	R/WC
E1h	RPDCGEN	Root Port Dynamic Clock Gating Enable	00h	R/W
E2h	RPPGEN	Root Port Power Gating Enable	00h	R/WS, RO
ECh-EFh	PECR3	PCI Express* Configuration Register 3	00000000h	R/W
FCh-FFh	PECR4	PCI Express* Configuration Register 4	00000000h	R/W
104h-107h	UES	Uncorrectable Error Status	See bit description	R/WC, RO
108h-10Bh	UEM	Uncorrectable Error Mask	00000000h	R/WO, RO
10Ch-10Fh	UEV	Uncorrectable Error Severity	00060011h	RO
110h-113h	CES	Correctable Error Status	00000000h	R/WC
114h-117h	CEM	Correctable Error Mask	00000000h	R/WO
118h-11Bh	AECC	Advanced Error Capabilities and Control	00000000h	RO
130h-133h	RES	Root Error Status	00000000h	R/WC, RO
200h-203h	L1SECH	L1 Sub-States Extended Capability Header	00010000h	R/WO
204h-207h	L1SCAP	L1 Sub-States Capabilities	0028281Fh	R/WO, RO
208h-20Bh	L1SCTL1	L1 Sub-States Control 1	00000010h	R/W, RO

**Table 17-1. PCI Express\* Configuration Registers Address Map (PCI Express\*-D28:F0/F1/F2/F3/F4/F5) (Sheet 3 of 3)**

Offset	Mnemonic	Register Name	Function 0-7 Default	Attribute
20Ch-20Fh	L1SCTL2	L1 Sub-States Control 2	00000028h	R/W, RO
320h-323h	PECR2	PCI Express* Configuration Register 2	0004b05bh	R/W
324h-327h	PEETM	PCI Express* Extended Test Mode Register	See bit description	RO
330h-333h	PEC1	PCI Express* Configuration Register 1	28000016h	RO, R/W
408h-40Bh	PEC4	PCI Express* Configuration Register 4	04011420h	RO, R/W
418h-41Bh	PEC2	PCI Express* Configuration Register 2	00000930h	RO, R/W
420h-423h	PEC3	PCI Express* Configuration Register 3	0028E8146h	RO, R/W

## 17.1.1 VID—Vendor Identification Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 00h-01h  
Default Value: 8086h

Attribute: RO  
Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

## 17.1.2 DID—Device Identification Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 02h-03h  
Default Value: Port 1= E  
Port 2= E  
Port 3= E  
Port 4= E  
Port 5= E  
Port 6= E  
Port 7= E  
Port 8= E

Attribute: RO  
Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH's PCI Express* controller. See Section 1.4 for the value of the DID Register.

### 17.1.3 PCICMD—PCI Command Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 04h–05h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable</b> —R/W. This disables pin-based INTx# interrupts on enabled hot-plug and power management events. This bit has no effect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for hot-plug or power management and MSI is not enabled. 1 = Internal INTx# messages will not be generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages will still be forwarded to the internal interrupt controllers if this bit is set.
9	Fast Back to Back Enable (FBE)—Reserved per the <i>PCI Express* Base Specification</i> .
8	<b>SERR# Enable (SEE)</b> —R/W. 0 = Disable. 1 = Enables the root port to generate an SERR# message when PSTS.SSE is set.
7	Wait Cycle Control (WCC)—Reserved per the <i>PCI Express* Base Specification</i> .
6	<b>Parity Error Response (PER)</b> —R/W. 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	VGA Palette Snoop (VPS)—Reserved per the <i>PCI Express* Base Specification</i> .
4	Postable Memory Write Enable (PMWE)—Reserved per the <i>PCI Express* Base Specification</i> .
3	Special Cycle Enable (SCE)—Reserved per the <i>PCI Express* Base Specification</i> .
2	<b>Bus Master Enable (BME)</b> —R/W. 0 = Disable. Memory and I/O requests received at a Root Port must be handled as Unsupported Requests. 1 = Enable. Allows the root port to forward Memory and I/O Read/Write cycles onto the backbone from a PCI Express* device. <b>Note:</b> This bit does not affect forwarding of completions in either upstream or downstream direction nor controls forwarding of requests other than memory or I/O
1	<b>Memory Space Enable (MSE)</b> —R/W. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI Express* device.
0	<b>I/O Space Enable (IOSE)</b> —R/W. This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI Express* device.

### 17.1.4 PCISTS—PCI Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 06h–07h  
Default Value: 0010h

Attribute: R/WC, RO  
Size: 16 bits

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC. 0 = No parity error detected. 1 = Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER (D28:F0/F1/F2/F3:04, bit 6) is not set.
14	<b>Signaled System Error (SSE)</b> —R/WC. 0 = No system error signaled. 1 = Set when the root port signals a system error to the internal SERR# logic.
13	<b>Received Master Abort (RMA)</b> —R/WC. 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the root port receives a completion with unsupported request status from the backbone.
12	<b>Received Target Abort (RTA)</b> —R/WC. 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the root port receives a completion with completer abort from the backbone.
11	<b>Signaled Target Abort (STA)</b> —R/WC. 0 = No target abort received. 1 = Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
10:9	DEVSEL# Timing Status (DEV_STS)—Reserved per the <i>PCI Express* Base Specification</i> .
8	<b>Master Data Parity Error Detected (DPED)</b> —R/WC. 0 = No data parity error received. 1 = Set when the root port receives a completion with a data parity error on the backbone and PCIMD.PER (D28:F0/F1/F2/F3:04, bit 6) is set.
7	<b>Fast Back to Back Capable (FB2BC)</b> —Reserved per the <i>PCI Express* Base Specification</i> .
6	Reserved
5	66 MHz Capable—Reserved per the <i>PCI Express* Base Specification</i> .
4	<b>Capabilities List</b> —RO. Hardwired to 1. Indicates the presence of a capabilities list.
3	<b>Interrupt Status</b> —RO. Indicates status of hot-plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit (D28:F0/F1/F2/F3/F4/F5:04h:bit 10).
2:0	Reserved

### 17.1.5 RID—Revision Identification Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Offset Address: 08h Attribute: RO  
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See Section 1.4 for the value of the RID Register.

### 17.1.6 PI—Programming Interface Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 09h Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Programming Interface</b> —RO. 00h = No specific register level programming interface defined.

### 17.1.7 SCC—Sub Class Code Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Ah Attribute: RO  
Default Value: 04h Size: 8 bits

Bit	Description
7:0	<b>Sub Class Code (SCC)</b> —RO. This field is determined by bit 2 of the MPC register (D28:F0-5:Offset D8h, bit 2). 04h = PCI-to-PCI bridge. 00h = Host Bridge.

### 17.1.8 BCC—Base Class Code Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Bh Attribute: RO  
Default Value: 06h Size: 8 bits

Bit	Description
7:0	<b>Base Class Code (BCC)</b> —RO. 06h = Indicates the device is a bridge device.

### 17.1.9 CLS—Cache Line Size Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Ch Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Cache Line Size (CLS)</b> —R/W. This is read/write but contains no functionality, per the <i>PCI Express* Base Specification</i> .

### 17.1.10 PLT—Primary Latency Timer Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Dh Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:3	<b>Latency Count</b> —RO. Reserved per the <i>PCI Express* Base Specification</i> .
2:0	Reserved

### 17.1.11 HEADTYP—Header Type Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 0Eh Attribute: RO  
Default Value: 81h Size: 8 bits

Bit	Description
7	<b>Multi-Function Device</b> —RO. 0 = Single-function device. 1 = Multi-function device.
6:0	<b>Configuration Layout</b> —RO. This field is determined by bit 2 of the MPC register (D28:F0-5:Offset D8h, bit 2). 00h = Indicates a Host Bridge. 01h = Indicates a PCI-to-PCI bridge.

### 17.1.12 BNUM—Bus Number Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 18-1Ah  
Default Value: 000000h

Attribute: R/W  
Size: 24 bits

Bit	Description
23:16	<b>Subordinate Bus Number (SBBN)</b> —R/W. Indicates the highest PCI bus number below the bridge.
15:8	<b>Secondary Bus Number (SCBN)</b> —R/W. Indicates the bus number the port.
7:0	<b>Primary Bus Number (PBN)</b> —R/W. Indicates the bus number of the backbone.

### 17.1.13 SLT—Secondary Latency Timer Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 1Bh  
Default Value: 00h

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	<b>Secondary Latency Timer</b> —RO. Reserved for a Root Port per the <i>PCI Express* Base Specification</i> .

### 17.1.14 IOBL—I/O Base and Limit Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 1Ch-1Dh  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:12	<b>I/O Limit Address (IOLA)</b> —R/W. I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to FFFh.
11:8	<b>I/O Limit Address Capability (IOLC)</b> —RO. Indicates that the bridge does not support 32-bit I/O addressing.
7:4	<b>I/O Base Address (IOBA)</b> —R/W. I/O Base bits corresponding to address lines 15:12 for 4KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	<b>I/O Base Address Capability (IOBC)</b> —RO. Indicates that the bridge does not support 32-bit I/O addressing.

### 17.1.15 SSTS—Secondary Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 1Eh–1Fh  
Default Value: 0000h

Attribute: R/WC  
Size: 16 bits

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC. 0 = No error. 1 = The port received a poisoned TLP.
14	<b>Received System Error (RSE)</b> —R/WC. 0 = No error. 1 = The port received an ERR_FATAL or ERR_NONFATAL message from the device.
13	<b>Received Master Abort (RMA)</b> —R/WC. 0 = Unsupported Request not received. 1 = The port received a completion with "Unsupported Request" status from the device.
12	<b>Received Target Abort (RTA)</b> —R/WC. 0 = Completion Abort not received. 1 = The port received a completion with "Completion Abort" status from the device.
11	<b>Signaled Target Abort (STA)</b> —R/WC. 0 = Completion Abort not sent. 1 = The port generated a completion with "Completion Abort" status to the device.
10:9	Secondary DEVSEL# Timing Status (SDTS): Reserved per <i>PCI Express* Base Specification</i> .
8	<b>Data Parity Error Detected (DPD)</b> —R/WC. 0 = Conditions below did not occur. 1 = Set when the BCTRL.PERE (D28:FO/F1/F2/F3/F4/F5:3E: bit 0) is set, and either of the following two conditions occurs: — Port receives completion marked poisoned. — Port poisons a write request to the secondary side.
7	Secondary Fast Back to Back Capable (SFBC): Reserved per <i>PCI Express* Base Specification</i> .
6	Reserved
5	<b>Secondary 66 MHz Capable (SC66)</b> —R/WC. Reserved per <i>PCI Express* Base Specification</i> .
4:0	Reserved

### 17.1.16 MBL—Memory Base and Limit Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 20h–23h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Accesses that are within the ranges specified in this register will be sent to the attached device if CMD.MSE (D28:F0/F1/F2/F3/F4/F5:04:bit 1) is set. Accesses from the attached device that are outside the ranges specified will be forwarded to the backbone if CMD.BME (D28:F0/F1/F2/F3/F4/F5:04:bit 2) is set. The comparison performed is  $MB \geq AD[31:20] \leq ML$ .

Bit	Description
31:20	<b>Memory Limit (ML)</b> —R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	Reserved
15:4	<b>Memory Base (MB)</b> —R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	Reserved

### 17.1.17 PMBL—Prefetchable Memory Base and Limit Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 24h–27h  
Default Value: 00010001h

Attribute: R/W, RO  
Size: 32 bits

Accesses that are within the ranges specified in this register will be sent to the device if CMD.MSE (D28:F0/F1/F2/F3/F4/F5:04, bit 1) is set. Accesses from the device that are outside the ranges specified will be forwarded to the backbone if CMD.BME (D28:F0/F1/F2/F3/F4/F5:04, bit 2) is set. The comparison performed is  $PMBU32:PMB \geq AD[63:32]:AD[31:20] \leq PMLU32:PML$ .

Bit	Description
31:20	<b>Prefetchable Memory Limit (PML)</b> —R/W. These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the range.
19:16	<b>64-bit Indicator (I64L)</b> —RO. Indicates support for 64-bit addressing
15:4	<b>Prefetchable Memory Base (PMB)</b> —R/W. These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the range.
3:0	<b>64-bit Indicator (I64B)</b> —RO. Indicates support for 64-bit addressing



### 17.1.18 PMBU32—Prefetchable Memory Base Upper 32-Bit Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 28h–2Bh      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Prefetchable Memory Base Upper Portion (PMBU)</b> —R/W. Upper 32-bits of the prefetchable address base.

### 17.1.19 PMLU32—Prefetchable Memory Limit Upper 32-Bit Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 2Ch–2Fh      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Prefetchable Memory Limit Upper Portion (PMLU)</b> —R/W. Upper 32-bits of the prefetchable address limit.

### 17.1.20 CAPP—Capabilities List Pointer Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 34h      Attribute: RO  
 Default Value: 40h      Size: 8 bits

Bit	Description
7:0	<b>Capabilities Pointer (PTR)</b> —RO. Indicates that the pointer for the first entry in the capabilities list is at 40h in configuration space.

### 17.1.21 INTR—Interrupt Information Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 3Ch–3Dh Attribute: R/W, RO  
Default Value: See bit description Size: 16 bits  
Function Level Reset: No (Bits 7:0 only)

Bit	Description																			
15:8	<p><b>Interrupt Pin (IPIN)</b>—RO. Indicates the interrupt pin driven by the root port. At reset, this register takes on the following values that reflect the reset state of the D28IP register in Chipset Configuration space:</p> <table><thead><tr><th>Port</th><th>Reset Value</th></tr></thead><tbody><tr><td>1</td><td>D28IP.P1IP</td></tr><tr><td>2</td><td>D28IP.P2IP</td></tr><tr><td>3</td><td>D28IP.P3IP</td></tr><tr><td>4</td><td>D28IP.P4IP</td></tr><tr><td>5</td><td>D28IP.P5IP</td></tr><tr><td>6</td><td>D28IP.P6IP</td></tr><tr><td>7</td><td>D28IP.P7IP</td></tr><tr><td>8</td><td>D28IP.P8IP</td></tr></tbody></table> <p><b>Note:</b> The value that is programmed into D28IP is always reflected in this register.</p>		Port	Reset Value	1	D28IP.P1IP	2	D28IP.P2IP	3	D28IP.P3IP	4	D28IP.P4IP	5	D28IP.P5IP	6	D28IP.P6IP	7	D28IP.P7IP	8	D28IP.P8IP
Port	Reset Value																			
1	D28IP.P1IP																			
2	D28IP.P2IP																			
3	D28IP.P3IP																			
4	D28IP.P4IP																			
5	D28IP.P5IP																			
6	D28IP.P6IP																			
7	D28IP.P7IP																			
8	D28IP.P8IP																			
7:0	<p><b>Interrupt Line (ILINE)</b>—R/W. Default = 00h. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. These bits are not reset by FLR.</p>																			



### 17.1.22 BCTRL—Bridge Control Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 3Eh–3Fh  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:12	Reserved
11	Discard Timer SERR# Enable (DTSE): Reserved per <i>PCI Express* Base Specification</i> , Revision 1.0a
10	Discard Timer Status (DTS): Reserved per <i>PCI Express* Base Specification</i> , Revision 1.0a.
9	Secondary Discard Timer (SDT): Reserved per <i>PCI Express* Base Specification</i> , Revision 1.0a.
8	Primary Discard Timer (PDT): Reserved per <i>PCI Express* Base Specification</i> , Revision 1.0a.
7	Fast Back to Back Enable (FBE): Reserved per <i>PCI Express* Base Specification</i> , Revision 1.0a.
6	<b>Secondary Bus Reset (SBR)</b> —R/W. Triggers a hot reset on the PCI Express* port.
5	Master Abort Mode (MAM): Reserved per Express specification.
4	<b>VGA 16-Bit Decode (V16)</b> —R/W. 0 = VGA range is enabled. 1 = The I/O aliases of the VGA range (see BCTRL:VE definition below), are not enabled, and only the base I/O ranges can be decoded.
3	<b>VGA Enable (VE)</b> —R/W. 0 = The ranges below will not be claimed off the backbone by the root port. 1 = The following ranges will be claimed off the backbone by the root port: <ul style="list-style-type: none"><li>• Memory ranges A0000h–BFFFFh</li><li>• I/O ranges 3B0h – 3BBh and 3C0h – 3DFh, and all aliases of bits 15:10 in any combination of 1s</li></ul>
2	<b>ISA Enable (IE)</b> —R/W. This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64KB of PCI I/O space. 0 = The root port will not block any forwarding from the backbone as described below. 1 = The root port will block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1KB block (offsets 100h to 3FFh).
1	<b>SERR# Enable (SE)</b> —R/W. 0 = The messages described below are not forwarded to the backbone. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone.
0	<b>Parity Error Response Enable (PERE)</b> —R/W. When set, 0 = Poisoned write TLPs and completions indicating poisoned TLPs will not set the SSTS.DPD (D28:F0/F1/F2/F3/F4/F5:1E, bit 8). 1 = Poisoned write TLPs and completions indicating poisoned TLPs will set the SSTS.DPD (D28:F0/F1/F2/F3/F4/F5:1E, bit 8).

### 17.1.23 CLIST—Capabilities List Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 40–41h  
Default Value: 8010h

Attribute: RO  
Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —RO. Value of 80h indicates the location of the next pointer.
7:0	<b>Capability ID (CID)</b> —RO. Indicates this is a PCI Express* capability.

### 17.1.24 XCAP—PCI Express\* Capabilities Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 42h–43h  
 Default Value: 0042h

Attribute: R/WO, RO  
 Size: 16 bits

Bit	Description
15:14	Reserved
13:9	<b>Interrupt Message Number (IMN)</b> —RO. The PCH does not have multiple MSI interrupt numbers.
8	<b>Slot Implemented (SI)</b> —R/WO. Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
7:4	<b>Device/Port Type (DT)</b> —RO. Indicates this is a PCI Express* root port.
3:0	<b>Capability Version (CV)</b> —RO. Indicates PCI Express 2.0.

### 17.1.25 DCAP—Device Capabilities Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 44h–47h  
 Default Value: 00008000h

Attribute: RO  
 Size: 32 bits

Bit	Description
31:28	Reserved
27:26	<b>Captured Slot Power Limit Scale (CSPS)</b> —RO. Not supported.
25:18	<b>Captured Slot Power Limit Value (CSPV)</b> —RO. Not supported.
17:16	Reserved
15	<b>Role Based Error Reporting (RBER)</b> —RO. Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express* 2.0 specification.
14:12	Reserved
11:9	<b>Endpoint L1 Acceptable Latency (E1AL)</b> —RO. This field is reserved with a setting of 000b for devices other than Endpoints, per the PCI Express* 2.0 specification.
8:6	<b>Endpoint L0s Acceptable Latency (E0AL)</b> —RO. This field is reserved with a setting of 000b for devices other than Endpoints, per the PCI Express* 2.0 specification.
5	<b>Extended Tag Field Supported (ETFS)</b> —RO. Indicates that 8-bit tag fields are supported.
4:3	<b>Phantom Functions Supported (PFS)</b> —RO. No phantom functions supported.
2:0	<b>Maximum Payload Size Supported (MPS)</b> —RO. Indicates the maximum payload size supported is 128B.

### 17.1.26 DCTL—Device Control Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 48h–49h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15	Reserved
14:12	<b>Maximum Read Request Size (MRRS)</b> —RO. Hardwired to 0.
11	<b>Enable No Snoop (ENS)</b> —RO. Not supported. The root port will never issue non-snoop requests.
10	<b>Aux Power PM Enable (APME)</b> —R/W. The OS will set this bit to 1 if the device connected has detected aux power. It has no effect on the root port otherwise.
9	<b>Phantom Functions Enable (PFE)</b> —RO. Not supported.
8	<b>Extended Tag Field Enable (ETFE)</b> —RO. Not supported.
7:5	<b>Maximum Payload Size (MPS)</b> —R/W. The root port only supports 128-B payloads, regardless of the programming of this field.
4	<b>Enable Relaxed Ordering (ERO)</b> —RO. Not supported.
3	<b>Unsupported Request Reporting Enable (URE)</b> —R/W. 0 = The root port will ignore unsupported request errors. 1 = Allows signaling of ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_, or NONFATAL, is sent to the Root Control register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	<b>Fatal Error Reporting Enable (FEE)</b> —R/W. 0 = The root port will ignore fatal errors. 1 = Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	<b>Non-Fatal Error Reporting Enable (NFE)</b> —R/W. 0 = The root port will ignore non-fatal errors. 1 = Enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	<b>Correctable Error Reporting Enable (CEE)</b> —R/W. 0 = The root port will ignore correctable errors. 1 = Enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

### 17.1.27 DSTS—Device Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 4Ah–4Bh  
Default Value: 0010h

Attribute: R/WC, RO  
Size: 16 bits

Bit	Description
15:6	Reserved
5	<b>Transactions Pending (TDP)</b> —RO. This bit has no meaning for the root port since only one transaction may be pending to the PCH, so a read of this bit cannot occur until it has already returned to 0.
4	<b>AUX Power Detected (APD)</b> —RO. The root port contains AUX power for wakeup.
3	<b>Unsupported Request Detected (URD)</b> —R/WC. Indicates an unsupported request was detected.
2	<b>Fatal Error Detected (FED)</b> —R/WC. Indicates a fatal error was detected. 0 = Fatal has not occurred. 1 = A fatal error occurred from a data link protocol error, link training error, buffer overflow, or malformed TLP.
1	<b>Non-Fatal Error Detected (NFED)</b> —R/WC. Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout.
0	<b>Correctable Error Detected (CED)</b> —R/WC. Indicates a correctable error was detected. 0 = Correctable error has not occurred. 1 = The port received an internal correctable error from receiver errors/framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

### 17.1.28 LCAP—Link Capabilities Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 4Ch–4Fh Attribute: R/WO, RO  
Default Value: See bit description Size: 32 bits

Bit	Description																													
31:24	<b>Port Number (PN)</b> —RO. Indicates the port number for the root port. This value is different for each implemented port: <table> <thead> <tr> <th>Function</th><th>Port #</th><th>Value of PN Field</th></tr> </thead> <tbody> <tr><td>D28:F0</td><td>1</td><td>01h</td></tr> <tr><td>D28:F1</td><td>2</td><td>02h</td></tr> <tr><td>D28:F2</td><td>3</td><td>03h</td></tr> <tr><td>D28:F3</td><td>4</td><td>04h</td></tr> <tr><td>D28:F4</td><td>5</td><td>05h</td></tr> <tr><td>D28:F5</td><td>6</td><td>06h</td></tr> <tr><td>D28:F6</td><td>7</td><td>07h</td></tr> <tr><td>D28:F7</td><td>8</td><td>08h</td></tr> </tbody> </table>			Function	Port #	Value of PN Field	D28:F0	1	01h	D28:F1	2	02h	D28:F2	3	03h	D28:F3	4	04h	D28:F4	5	05h	D28:F5	6	06h	D28:F6	7	07h	D28:F7	8	08h
Function	Port #	Value of PN Field																												
D28:F0	1	01h																												
D28:F1	2	02h																												
D28:F2	3	03h																												
D28:F3	4	04h																												
D28:F4	5	05h																												
D28:F5	6	06h																												
D28:F6	7	07h																												
D28:F7	8	08h																												
23:22	Reserved																													
21	<b>Link Bandwidth Notification Capability (LBNC)</b> —RO. This port supports Link Bandwidth Notification status and interrupt mechanisms.																													
20	<b>Link Active Reporting Capable (LARC)</b> —RO. Hardwired to 1 to indicate that this port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.																													
19	Reserved																													
18	<b>Clock Power Management (CPM)</b> —RO. 0 = PCH root ports do not support CLKREQ# mechanism. 1 = PCH root ports support the CLKREQ# mechanism.																													
17:15	<b>L1 Exit Latency (EL1)</b> —R/WO. 000b = Less than 1us 001b = 1 us to less than 2 $\mu$ s 010b = 2 us to less than 4 $\mu$ s 011b = 4 us to less than 8 $\mu$ s 100b = 8 us to less than 16 $\mu$ s 101b = 16 us to less than 32 $\mu$ s 110b = 32 us to 64 $\mu$ s 111b = more than 64 $\mu$ s																													
	<b>Note:</b> If PXP PLL shutdown is enabled, BIOS should program this latency to comprehend PLL lock latency.																													
14:12	<b>L0s Exit Latency (EL0)</b> —RO/V. Indicates as exit latency based upon common-clock configuration.																													
	<table> <thead> <tr> <th>LCLT.CCC</th><th>Value of EL0 (these bits)</th></tr> </thead> <tbody> <tr><td>0</td><td>MPC.UCEL (D28:F0/F1/F2/F3:D8h:bits20:18)</td></tr> <tr><td>1</td><td>MPC.CCEL (D28:F0/F1/F2/F3:D8h:bits17:15)</td></tr> </tbody> </table>			LCLT.CCC	Value of EL0 (these bits)	0	MPC.UCEL (D28:F0/F1/F2/F3:D8h:bits20:18)	1	MPC.CCEL (D28:F0/F1/F2/F3:D8h:bits17:15)																					
LCLT.CCC	Value of EL0 (these bits)																													
0	MPC.UCEL (D28:F0/F1/F2/F3:D8h:bits20:18)																													
1	MPC.CCEL (D28:F0/F1/F2/F3:D8h:bits17:15)																													
	<b>Note:</b> LCLT.CCC is at D28:F0/F1/F2/F3/F4/F5:50h:bit 6																													

Bit	Description																																																															
11:10	<p><b>Active State Link PM Support (APMS)</b>—R/WO. Indicates what level of active state link power management is supported on the root port.</p> <table> <thead> <tr> <th data-bbox="551 382 600 403">Bits</th> <th data-bbox="665 382 780 403">Definition</th> </tr> </thead> <tbody> <tr> <td data-bbox="551 418 600 439">00b</td> <td data-bbox="665 418 992 439">Neither L0s nor L1 are supported</td> </tr> <tr> <td data-bbox="551 454 600 475">01b</td> <td data-bbox="665 454 878 475">L0s Entry Supported</td> </tr> <tr> <td data-bbox="551 489 600 511">10b</td> <td data-bbox="665 489 861 511">L1 Entry Supported</td> </tr> <tr> <td data-bbox="551 528 600 549">11b</td> <td data-bbox="665 528 992 549">Both L0s and L1 Entry Supported</td> </tr> </tbody> </table>	Bits	Definition	00b	Neither L0s nor L1 are supported	01b	L0s Entry Supported	10b	L1 Entry Supported	11b	Both L0s and L1 Entry Supported																																																					
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9:4	<p><b>Maximum Link Width (MLW)</b>—RO. For the root ports, several values can be taken, based upon the value of the Chipset Configuration register field RPC.PC1 (Chipset Configuration Registers:Offset 0224h:bits1:0) for Ports 1-4 and RPC.PC2 (Chipset Configuration Registers:Offset 0224h:bits1:0) for Ports 5 and 6</p> <table> <thead> <tr> <th data-bbox="551 720 698 762">Value of MLW Field</th> <th data-bbox="584 741 682 762"></th> <th data-bbox="747 783 910 804">Port #</th> <th data-bbox="747 783 910 804">RPC.PC1=00b</th> <th data-bbox="975 783 1024 804">01b</th> <th data-bbox="1090 783 1139 804">10b</th> <th data-bbox="1237 783 1286 804">11b</th> </tr> </thead> <tbody> <tr> <td data-bbox="616 819 633 840">1</td> <td data-bbox="780 819 812 840"></td> <td data-bbox="845 819 878 840">01h</td> <td data-bbox="943 819 992 840"></td> <td data-bbox="1024 819 1073 840">02h</td> <td data-bbox="1106 819 1155 840">02h</td> <td data-bbox="1253 819 1302 840">04h</td> </tr> <tr> <td data-bbox="616 855 633 876">2</td> <td data-bbox="780 855 812 876"></td> <td data-bbox="845 855 878 876">01h</td> <td data-bbox="943 855 992 876"></td> <td data-bbox="1024 855 1073 876">01h</td> <td data-bbox="1106 855 1155 876">01h</td> <td data-bbox="1253 855 1302 876">01h</td> </tr> <tr> <td data-bbox="616 891 633 912">3</td> <td data-bbox="780 891 812 912"></td> <td data-bbox="845 891 878 912">01h</td> <td data-bbox="943 891 992 912"></td> <td data-bbox="1024 891 1073 912">01h</td> <td data-bbox="1106 891 1155 912">02h</td> <td data-bbox="1253 891 1302 912">01h</td> </tr> <tr> <td data-bbox="616 927 633 948">4</td> <td data-bbox="780 927 812 948"></td> <td data-bbox="845 927 878 948">01h</td> <td data-bbox="943 927 992 948"></td> <td data-bbox="1024 927 1073 948">01h</td> <td data-bbox="1106 927 1155 948">01h</td> <td data-bbox="1253 927 1302 948">01h</td> </tr> <tr> <td data-bbox="616 963 633 984">Port #</td> <td data-bbox="780 963 910 984">RPC.PC2=00b</td> <td data-bbox="975 963 1024 984"></td> <td data-bbox="1090 963 1139 984"><b>01b</b></td> <td data-bbox="1237 963 1286 984"><b>10b</b></td> <td data-bbox="1253 963 1302 984"><b>11b</b></td> <td data-bbox="1253 963 1302 984"></td> </tr> <tr> <td data-bbox="616 998 633 1020">5</td> <td data-bbox="780 998 812 1020"></td> <td data-bbox="845 998 878 1020">01h</td> <td data-bbox="943 998 992 1020"></td> <td data-bbox="1024 998 1073 1020">02h</td> <td data-bbox="1106 998 1155 1020">02h</td> <td data-bbox="1253 998 1302 1020">04h</td> </tr> <tr> <td data-bbox="616 1034 633 1056">Port #</td> <td data-bbox="780 1034 910 1056">RPC.PC3=00b</td> <td data-bbox="975 1034 1024 1056"></td> <td data-bbox="1090 1034 1139 1056">01b</td> <td data-bbox="1237 1034 1286 1056">10b</td> <td data-bbox="1253 1034 1302 1056">11b</td> <td data-bbox="1253 1034 1302 1056"></td> </tr> <tr> <td data-bbox="616 1070 633 1091">6</td> <td data-bbox="780 1070 812 1091"></td> <td data-bbox="845 1070 878 1091">01h</td> <td data-bbox="943 1070 992 1091"></td> <td data-bbox="1024 1070 1073 1091">02h</td> <td data-bbox="1106 1070 1155 1091">02h</td> <td data-bbox="1253 1070 1302 1091">04h</td> </tr> </tbody> </table>	Value of MLW Field		Port #	RPC.PC1=00b	01b	10b	11b	1		01h		02h	02h	04h	2		01h		01h	01h	01h	3		01h		01h	02h	01h	4		01h		01h	01h	01h	Port #	RPC.PC2=00b		<b>01b</b>	<b>10b</b>	<b>11b</b>		5		01h		02h	02h	04h	Port #	RPC.PC3=00b		01b	10b	11b		6		01h		02h	02h	04h
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1		01h		02h	02h	04h																																																										
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Port #	RPC.PC3=00b		01b	10b	11b																																																											
6		01h		02h	02h	04h																																																										
3:0	<p><b>Maximum Link Speed (MLS)</b>—RO.</p> <p>0001b = indicates the link speed is 2.5Gb/s      0010b = 5.0Gb/s and 2.5Gb/s link speeds supported      These bits report a value of 0001b if Gen 2 disable bit 14 is set in the MPC register; otherwise, the value reported is 0010b.</p>																																																															

### 17.1.29 LCTL—Link Control Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 50h–51h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:10	Reserved
9	<b>Hardware Autonomous Width Disable</b> —RO. Hardware never attempts to change the link width except when attempting to correct unreliable Link operation.
8	Reserved
7	<b>Extended Synch (ES)</b> —R/W. 0 = Extended sync disabled. 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	<b>Common Clock Configuration (CCC)</b> —R/W. 0 = The PCH and device are not using a common reference clock. 1 = The PCH and device are operating with a distributed common reference clock.  <b>Note:</b> Non-Common Clock without Spread Spectrum Clocking (also known as, PCIe* SRNS mode, with 600 ppm jitter tolerance) is <b>not</b> supported. <b>Note:</b> Non-Common Clock with Spread Spectrum Clocking (also known as, PCIe* SRIS mode, with 5600 ppm jitter tolerance) is <b>not</b> supported.
5	<b>Retrain Link (RL)</b> —R/W. 0 = This bit always returns 0 when read. 1 = The root port will train its downstream link.  <b>Note:</b> Software uses LSTS.LT (D28:F0/F1/F2/F3/F4/F5:52, bit 11) to check the status of training. <b>Note:</b> It is permitted to write 1b to this bit while simultaneously writing modified values to other fields in this register. If the LTSSM is not already in Recovery or Configuration, the resulting Link training must use the modified values. If the LTSSM is already in Recovery or Configuration, the modified values are not required to affect the Link training that is already in progress.
4	<b>Link Disable (LD)</b> —R/W. 0 = Link enabled. 1 = The root port will disable the link.
3	<b>Read Completion Boundary Control (RCBC)</b> —RO. Indicates the read completion boundary is 64 bytes.
2	Reserved
1:0	<b>Active State Link PM Control (ASPM)</b> —R/W. Indicates whether the root port should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled

### 17.1.30 LSTS—Link Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 52h–53h      Attribute: RO  
 Default Value: See bit description      Size: 16 bits

Bit	Description																		
15:14	Reserved																		
13	<b>Data Link Layer Active (DLA)</b> —RO. Default value is 0b. 0 = Data Link Control and Management State Machine is not in the DL_Active state 1 = Data Link Control and Management State Machine is in the DL_Active state																		
12	<b>Slot Clock Configuration (SCC)</b> —RO. Set to 1b to indicate that the PCH uses the same reference clock as on the platform and does not generate its own clock.																		
11	<b>Link Training (LT)</b> —RO. Default value is 0b. 0 = Link training completed. 1 = Link training is occurring.																		
10	<b>Link Training Error (LTE)</b> —RO. Not supported. Set value is 0b.																		
9:4	<b>Negotiated Link Width (NLW)</b> —RO. This field indicates the negotiated width of the given PCI Express* link. The contents of this NLW field is undefined if the link has not successfully trained. <table border="1" data-bbox="551 903 959 1220"> <thead> <tr> <th>Port #</th><th>Possible Values</th></tr> </thead> <tbody> <tr> <td>1</td><td>000001b, 000010b, 000100b</td></tr> <tr> <td>2</td><td>000001b</td></tr> <tr> <td>3</td><td>000001b, 000010b</td></tr> <tr> <td>4</td><td>000001b</td></tr> <tr> <td>5</td><td>000001b, 000010b, 000100b</td></tr> <tr> <td>6</td><td>000001b</td></tr> <tr> <td>7</td><td>000001b, 000010b</td></tr> <tr> <td>8</td><td>000001b</td></tr> </tbody> </table> <p><b>Note:</b> 000001b = x1 link width, 000010b = x2 linkwidth, 000100b = x4 linkwidth</p>	Port #	Possible Values	1	000001b, 000010b, 000100b	2	000001b	3	000001b, 000010b	4	000001b	5	000001b, 000010b, 000100b	6	000001b	7	000001b, 000010b	8	000001b
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1	000001b, 000010b, 000100b																		
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5	000001b, 000010b, 000100b																		
6	000001b																		
7	000001b, 000010b																		
8	000001b																		
3:0	<b>Link Speed (LS)</b> —RO. This field indicates the negotiated Link speed of the given PCI Express* link. 0001b = Link is 2.5Gb/s 0010b = Link is 5.0Gb/s																		

### 17.1.31 SLCAP—Slot Capabilities Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 54h–57h      Attribute: R/WO, RO  
 Default Value: 00060060h      Size: 32 bits

Bit	Description
31:19	<b>Physical Slot Number (PSN)</b> —R/WO. This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18:17	Reserved
16:15	<b>Slot Power Limit Scale (SLS)</b> —R/WO. Specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:7	<b>Slot Power Limit Value (SLV)</b> —R/WO. Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	<b>Hot-Plug Capable (HPC)</b> —R/WO 1b = Indicates that hot-plug is supported.
5	<b>Hot-Plug Surprise (HPS)</b> —R/WO 1b = Indicates the device may be removed from the slot without prior notification.
4	<b>Power Indicator Present (PIP)</b> —RO 0b = Indicates that a power indicator LED is not present for this slot.
3	<b>Attention Indicator Present (AIP)</b> —RO 0b = Indicates that an attention indicator LED is not present for this slot.
2	<b>MRL Sensor Present (MSP)</b> —RO 0b = Indicates that an MRL sensor is not present.
1	<b>Power Controller Present (PCP)</b> —RO 0b = Indicates that a power controller is not implemented for this slot.
0	<b>Attention Button Present (ABP)</b> —RO 0b = Indicates that an attention button is not implemented for this slot.

### 17.1.32 SLCTL—Slot Control Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 58h–59h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:13	Reserved
12	<b>Link Active Changed Enable (LACE)</b> —R/W. When set, this field enables generation of a hot-plug interrupt when the Data Link Layer Link Active field (D28:F0/F1/F2/F3/F4/F5:52h:bit 13) is changed.
11	Reserved
10	<b>Power Controller Control (PCC)</b> —RO. This bit has no meaning for module-based hot-plug.
9:6	Reserved
5	<b>Hot-Plug Interrupt Enable (HPE)</b> —R/W. 0 = Hot-Plug interrupts based on hot-plug events is disabled. 1 = Enables generation of a hot-plug interrupt on enabled hot-plug events.
4	Reserved
3	<b>Presence Detect Changed Enable (PDE)</b> —R/W. 0 = Hot-Plug interrupts based on presence detect logic changes is disabled. 1 = Enables the generation of a hot-plug interrupt or wake message when the presence detect logic changes state.
2:0	Reserved

### 17.1.33 SLSTS—Slot Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 5Ah–5Bh  
Default Value: 0000h

Attribute: R/WC, RO  
Size: 16 bits

Bit	Description
15:9	Reserved
8	<b>Link Active State Changed (LASC)</b> —R/WC 1 = This bit is set when the value reported in Data Link Layer Link Active field of the Link Status register (D28:F0/F1/F2/F3/F4/F5:52h:bit 13) is changed. In response to a Data Link Layer State Changed event, software must read Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot-plugged device.
7	Reserved
6	<b>Presence Detect State (PDS)</b> —RO. If XCAP.SI (D28:F0/F1/F2/F3/F4/F5:42h:bit 8) is set (indicating that this root port spawns a slot), then this bit: 0 = Indicates the slot is empty. 1 = Indicates the slot has a device connected. Otherwise, if XCAP.SI is cleared, this bit is always set (1).
5	MRL Sensor State (MS)—Reserved as the MRL sensor is not implemented.
4	Reserved
3	<b>Presence Detect Changed (PDC)</b> —R/WC 0 = No change in the PDS bit. 1 = The PDS bit changed states.
2	<b>MRL Sensor Changed (MSC)</b> —Reserved as the MRL sensor is not implemented.
1	<b>Power Fault Detected (PFD)</b> —Reserved as a power controller is not implemented.
0	Reserved

### 17.1.34 RCTL—Root Control Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 5Ch–5Dh  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:4	Reserved
3	<b>PME Interrupt Enable (PIE)</b> —R/W 0 = Interrupt generation disabled. 1 = Interrupt generation enabled when PCISTS.Inerrupt Status (D28:F0/F1/F2/F3/F4/F5:60h, bit 16) is in a set state (either due to a 0 to 1 transition, or due to this bit being set with RSTS.IS already set).
2	<b>System Error on Fatal Error Enable (SFE)</b> —R/W 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5:04, bit 8) is set, if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port.
1	<b>System Error on Non-Fatal Error Enable (SNE)</b> —R/W 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5:04, bit 8) is set, if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port.
0	<b>System Error on Correctable Error Enable (SCE)</b> —R/W 0 = An SERR# will not be generated. 1 = An SERR# will be generated, assuming CMD.SEE (D28:F0/F1/F2/F3/F4/F5:04, bit 8) if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port.

### 17.1.35 RSTS—Root Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 60h–63h  
Default Value: 00000000h

Attribute: R/WC, RO  
Size: 32 bits

Bit	Description
31:18	Reserved
17	<b>PME Pending (PP)</b> —RO 0 = When the original PME is cleared by software, it will be set again, the requestor ID will be updated, and this bit will be cleared. 1 = Indicates another PME is pending when the PME status bit is set.
16	<b>PME Status (PS)</b> —R/WC 0 = PME was not asserted. 1 = Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	<b>PME Requestor ID (RID)</b> —RO. Indicates the PCI requestor ID of the last PME requestor. Valid only when PS is set.

### 17.1.36 DCAP2—Device Capabilities 2 Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 64h–67h  
Default Value: 00080816h

Attribute: RO, RWO  
Size: 32 bits

Bit	Description
31:12	Reserved
11	<b>LTR Mechanism Supported (LTRMS)</b> —RWO. A value of 1b indicates support for the optional Latency Tolerance Reporting (LTR) mechanism capability. BIOS must write this register bit with either a '1' or '0' to enable/disable the root port from declaring support for the LTR capability.
10:5	Reserved
4	<b>Completion Timeout Disable Supported (CTDS)</b> —RO. A value of 1b indicates support for the Completion Timeout Disable mechanism.
3:0	<b>Completion Timeout Ranges Supported (CTRS)</b> —RO. This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is hardwired to support 10 ms to 250 ms and 250 ms to 4 sec.

### 17.1.37 DCTL2—Device Control 2 Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 68h–69h  
Default Value: 0000h

Attribute: RO, R/W  
Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>LTR Mechanism Enable (LTREN)</b> —RW. When set to 1b, this bit enables the Latency Tolerance Reporting (LTR) mechanism. If DCAP2.LTRMS is clear, programming this field to any non-zero value will have no effect.
9:5	Reserved
4	<b>Completion Timeout Disable (CTD)</b> —R/W. When set to 1b, this bit disables the Completion Timeout mechanism. If there are outstanding requests when the bit is cleared, it is permitted but not required for hardware to apply the completion timeout mechanism to the outstanding requests. If this is accomplished, it is permitted to base the start time for each request on either the time this bit was cleared or the time each request was issued.
3:0	<b>Completion Timeout Value (CTV)</b> —R/W. This field allows system software to modify the Completion Timeout value. 0000b = Default range: 40 – 50 ms (specification range 50 µs to 50 ms) 0101b = 40 – 50 ms (specification range is 16 – 55 ms) 0110b = 160 – 170 ms (specification range is 65 – 210 ms) 1001b = 400 – 500 ms (specification range is 260 – 900 ms) 1010b = 1.6 – 1.7 sec., (specification range is 1 – 3.5 sec.) All other values are Reserved.  <b>Note:</b> Software is permitted to change the value in this field at any time. For requests already pending when the Completion Timeout Value is changed, hardware is permitted to use either the new or the old value for the outstanding requests, and is permitted to base the start time for each request either on when this value was changed or on when each request was issued.

### 17.1.38 LCTL2—Link Control 2 Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 70h–71h  
Default Value: 0002h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:13	Reserved
12	<b>Compliance De-Emphasis (CD)</b> —R/W. This bit sets the de-emphasis level in Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. Encodings: 0 = -6 dB 1 = -3.5 dB When the Link is operating at 2.5 GT/s, the setting of this bit has no effect. The default value of this bit is 0b. This bit is intended for debug, compliance testing purposes. System firmware and software are allowed to modify this bit only during debug or compliance testing.
11	<b>Compliance SOS (CSOS)</b> —R/W. When set to 1b, the LTSSM is required to send SKP Ordered Sets periodically in between the (modified) compliance patterns. The default value of this bit is 0b.
10	<b>Enter Modified Compliance (EMC)</b> —R/W. When this bit is set to 1b, the device transmits Modified Compliance Pattern if the LTSSM enters Polling.Compliance substrate. This register is intended for debug, compliance testing purposes only and the system must ensure it is set to the default value during normal operation. The default value of this bit is 0b.
9:7	<b>Transmit Margin (TM)</b> —R/W. This field controls the value of the non-de-emphasized voltage level at the Transmitter pins. This field is reset to 000b on entry to the LTSSM Polling. Configuration substrate (see PCI Express* Chapter 4 for details of how the Transmitter voltage level is determined in various states). Encodings: <b>000b</b> = Normal operating range <b>001b</b> = 800 – 1200mV for full swing and 400 – 700mV for half-swing <b>010b – (n-1)</b> = Values must be monotonic with a non-zero slope. The value of n must be greater than 3 and less than 7. At least two of these must be below the normal operating range of n: 200 – 400mV for full-swing and 100 – 200mV for half-swing <b>n - 111b</b> = Reserved For a multi-function device associated with an Upstream Port, the field in Function 0 is of type RWS, and only Function 0 controls the component's Link behavior. In all other Functions of that device, this field is of type Reserved. Default value of this field is 000b. Components that support only the 2.5 GT/s speed are permitted to hard wire this bit to 000b. This register is intended for debug, compliance testing purposes only and the system must ensure it is set to the default value during normal operation.
6	<b>Selectable De-emphasis (SD)</b> —R/W. When the Link is operating at 5.0 GT/s speed, this bit selects the level of de-emphasis for an Upstream component. Encodings: 1b = -3.5 dB 0b = -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	Reserved
4	<b>Enter Compliance (EC)</b> —R/W. Software is permitted to force a Link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a Link and then initiating a hot reset on the Link.
3:0	<b>Target Link Speed (TLS)</b> —R/W. This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. 0001b = 2.5 GT/s Target Link Speed 0010b = 5.0 GT/s and 2.5 GT/s Target Link Speeds All other values reserved.

### 17.1.39 LSTS2—Link Status 2 Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 72h–73h  
Default Value: 0000h

Attribute: RO  
Size: 16 bits

Bit	Description
15:1	Reserved
0	<b>Current De-emphasis Level (CDL)</b> —RO. When the Link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. Encodings: 0 = -6 dB 1 = -3.5 dB The value in this bit is undefined when the Link is operating at 2.5 GT/s speed.

### 17.1.40 MID—Message Signaled Interrupt Identifiers Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 80h–81h  
Default Value: 9005h

Attribute: RO  
Size: 16 bits

Bit	Description
15:8	<b>Next Pointer (NEXT)</b> —RO. Indicates the location of the next pointer in the list.
7:0	<b>Capability ID (CID)</b> —RO. Capabilities ID indicates MSI.

### 17.1.41 MC—Message Signaled Interrupt Message Control Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 82–83h      Attribute: R/W, RO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:8	Reserved
7	<b>64-bit Address Capable (C64)</b> —RO. Capable of generating a 32-bit message only.
6:4	<b>Multiple Message Enable (MME)</b> —R/W. These bits are R/W for software compatibility, but only one message is ever sent by the root port.
3:1	<b>Multiple Message Capable (MMC)</b> —RO. Only one message is required.
0	<b>MSI Enable (MSIE)</b> —R/W. 0 = MSI is disabled. 1 = MSI is enabled and traditional interrupt pins are not used to generate interrupts. <b>Note:</b> CMD.BME (D28:F0/F1/F2/F3/F4/F5/F6/F7:04h:bit 2) must be set for an MSI to be generated. If CMD.BME is cleared, and this bit is set, no interrupts (not even pin based) are generated.

### 17.1.42 MA—Message Signaled Interrupt (MSI) Message Address Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 84h–87h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:2	<b>Address (ADDR)</b> —R/W. Lower 32 bits of the system specified message address, always DWord aligned.
1:0	Reserved

### 17.1.43 MD—Message Signaled Interrupt (MSI) Message Data Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 88h–89h      Attribute: R/W  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Data (DATA)</b> —R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

### 17.1.44 SVCAP—Subsystem Vendor Capability Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 90h–91h  
Default Value: A00Dh

Attribute: R/WO, RO  
Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —R/WO. Indicates the location of the next pointer in the list. As this register is R/WO, BIOS must write a value to this register, even if it is to re-write the default value.
7:0	<b>Capability Identifier (CID)</b> —RO. Value of 0Dh indicates this is a PCI bridge subsystem vendor capability.

### 17.1.45 SVID—Subsystem Vendor Identification Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 94h–97h  
Default Value: 00000000h

Attribute: R/WO  
Size: 32 bits

Bit	Description
31:16	<b>Subsystem Identifier (SID)</b> —R/WO. Indicates the subsystem as identified by the vendor. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).
15:0	<b>Subsystem Vendor Identifier (SVID)</b> —R/WO. Indicates the manufacturer of the subsystem. This field is write once and is locked down until a bridge reset occurs (not the PCI bus reset).

### 17.1.46 PMCAP—Power Management Capability Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: A0h–A1h  
Default Value: 0001h

Attribute: RO  
Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —RO. Indicates this is the last item in the list.
7:0	<b>Capability Identifier (CID)</b> —RO. Value of 01h indicates this is a PCI power management capability.

### 17.1.47 PMC—PCI Power Management Capabilities Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: A2h–A3h  
Default Value: C803h

Attribute: RO  
Size: 16 bits

Bit	Description
15:11	<b>PME_Support (PMES)</b> —RO. Indicates PME# is supported for states D0, D3 <sub>HOT</sub> , and D3 <sub>COLD</sub> . The root port does not generate PME#, but reporting that it does is necessary for some legacy operating systems to enable PME# in devices connected behind this root port.
10	D2_Support (D2S)—RO. The D2 state is not supported.
9	D1_Support (D1S)—RO. The D1 state is not supported.
8:6	<b>Aux_Current (AC)</b> —RO. Reports 375mA maximum suspend well current required when in the D3 <sub>COLD</sub> state.
5	<b>Device Specific Initialization (DSI)</b> —RO. 1 = Indicates that no device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PMEC)</b> —RO. 1 = Indicates that 24-MHz clock is not required to generate PME#.
2:0	<b>Version (VS)</b> —RO. Indicates support for <i>Revision 1.2 of the PCI Power Management Specification</i> .

### 17.1.48 PMCS—PCI Power Management Control and Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: A4h–A7h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:24	Reserved
23	<b>Bus Power/Clock Control Enable (BPCE)</b> —Reserved per <i>PCI Express* Base Specification, Revision 1.0a</i> .
22	B2/B3 Support (B23S)—Reserved per <i>PCI Express* Base Specification, Revision 1.0a</i> .
21:16	Reserved
15	<b>PME Status (PMES)</b> —RO 1 = Indicates a PME was received on the downstream link.
14:9	Reserved
8	<b>PME Enable (PMEE)</b> —R/W 1 = Indicates PME is enabled. The root port takes no action on this bit, but it must be R/W for some legacy operating systems to enable PME# on devices connected to this root port. This bit is sticky and resides in the resume well. The reset for this bit is RSMRST# which is not asserted during a warm reset.
7:2	Reserved
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 = D0 state 11 = D3 <sub>HOT</sub> state  <b>Note:</b> When in the D3 <sub>HOT</sub> state, the controller's configuration space is available, but the I/O and memory spaces are not. Type 1 configuration cycles are also not accepted. Interrupts are not required to be blocked as software will disable interrupts prior to placing the port into D3 <sub>HOT</sub> . If software attempts to write a '10' or '01' to these bits, the write will be ignored.

### 17.1.49 MPC2—Miscellaneous Port Configuration Register 2 (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: D4h-D7h  
Default Value: 00000800h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:5	Reserved
4	<b>ASPM Control Override Enable (ASPMCOEN)</b> —R/W 1 = Root port will use the values in the ASPM Control Override registers 0 = Root port will use the ASPM Registers in the Link Control register.  <b>Notes:</b> This register allows BIOS to control the root port ASPM settings instead of the operating system.
3:2	<b>ASPM Control Override (ASPMO)</b> —R/W. Provides BIOS control of whether root port should enter L0s or L1 or both. 00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled.
1	<b>EOI Forwarding Disable (EOIFD)</b> —R/W. When set, EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe* link. 0 = Broadcast EOI messages that are sent on the backbone are claimed by this port and forwarded across the PCIe* link. 1 = Broadcast EOI messages are not claimed on the backbone by this port and will not be forwarded across the PCIe* Link.
0	<b>L1 Completion Timeout Mode (LICTM)</b> —R/W 0 = PCI Express* Specification Compliant. Completion timeout is disabled during software initiated L1, and enabled during ASPM initiate L1. 1 = Completion timeout is enabled during L1, regardless of how L1 entry was initiated.

### 17.1.50 MPC—Miscellaneous Port Configuration Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: D8h–DBh      Attribute: R/W, R/WO  
 Default Value: 09110000h      Size: 32 bits

Bit	Description
31	<b>Power Management SCI Enable (PMCE)</b> —R/W. 0 = SCI generation based on a power management event is disabled. 1 = Enables the root port to generate SCI whenever a power management event is detected.
30	<b>Hot-Plug SCI Enable (HPCE)</b> —R/W. 0 = SCI generation based on a hot-plug event is disabled. 1 = Enables the root port to generate SCI whenever a hot-plug event is detected.
29	<b>Link Hold Off (LHO)</b> —R/W. 1 = Port will not take any TLP. This is used during loopback mode to fill up the downstream queue.
28	<b>Address Translator Enable (ATE)</b> —R/W. This bit is used to enable address translation using the AT bits in this register during loopback mode. 0 = Disable 1 = Enable
27	Reserved
26	<b>Invalid Receive Bus Number Check Enable (IRBNCE)</b> —R/W. When set, the receive transaction layer will signal an error if the bus number of a memory request does not fall within the range between SCBN and SBBN. If this check is enabled and the request is a memory write, it is treated as an Unsupported Request. If this check is enabled and the request is a non-posted memory read request, the request is considered a Malformed TLP and a fatal error. Messages, I/O, Configuration, and Completions are never checked for valid bus number.
25	<b>Invalid Receive Range Check Enable (IRRCE)</b> —R/W. When set, the receive transaction layer will treat the TLP as an Unsupported Request error if the address range of a memory request does not fall outside the range between prefetchable and non-prefetchable base and limit. Messages, I/O, Configuration, and Completions are never checked for valid address ranges.
24	<b>BME Receive Check Enable (BMERCE)</b> —R/W. When set, the receive transaction layer will treat the TLP as an Unsupported Request error if a memory read or write request is received and the Bus Master Enable bit is not set. Messages, I/O, Configuration, and Completions are never checked for BME.
23	Reserved
22	<b>Detect Override (FORCEDDET)</b> —R/W. 0 = Normal operation. Detected output from AFE is sampled for presence detection. 1 = Override mode. Ignores AFE detect output and link training proceeds as if a device were detected.
21	<b>Flow Control During L1 Entry (FCDL1E)</b> —R/W. 0 = No flow control update DLLPs sent during L1 Ack transmission. 1 = Flow control update DLLPs sent during L1 Ack transmission as required to meet the 30 µs periodic flow control update.
20:18	<b>Unique Clock Exit Latency (UCEL)</b> —R/W. This value represents the L0s Exit Latency for unique-clock configurations (LCTL.CCC = 0) (D28:F0/F1/F2/F3/F4/F5:Offset 50h:bit 6). It defaults to 512 ns to less than 1 µs, but may be overridden by BIOS.
17:15	<b>Common Clock Exit Latency (CCEL)</b> —R/W. This value represents the L0s Exit Latency for common-clock configurations (LCTL.CCC = 1) (D28:F0/F1/F2/F3/F4/F5:Offset 50h:bit 6). It defaults to 128 ns to less than 256 ns, but may be overridden by BIOS.
14	<b>PCIe* Gen2 Speed Disable</b> —R/W. 0 = PCIe* supported data rate is defined as set through Supported Link Speed and Target Link Speed settings. 1 = PCIe* supported data rate is limited to 2.5 GT/s (Gen 1). Supported Link Speed register bits will reflect "0001b" when this bit is set. When this bit is changed, link retrain needs to be performed for the change to be effective.
13:8	Reserved

Bit	Description																		
7	<p><b>Port I/OxAPIC Enable (PAE)</b>—R/W.            0 = Hole is disabled.            1 = A range is opened through the bridge for the following memory addresses:</p> <table> <thead> <tr> <th data-bbox="649 409 719 430">Port #</th> <th data-bbox="904 409 990 430">Address</th> </tr> </thead> <tbody> <tr> <td data-bbox="682 451 698 473">1</td> <td data-bbox="817 451 1078 473">FEC1_0000h – FEC1_7FFFh</td> </tr> <tr> <td data-bbox="682 487 698 508">2</td> <td data-bbox="817 487 1078 508">FEC1_8000h – FEC1_FFFFh</td> </tr> <tr> <td data-bbox="682 523 698 544">3</td> <td data-bbox="817 523 1078 544">FEC2_0000h – FEC2_7FFFh</td> </tr> <tr> <td data-bbox="682 559 698 580">4</td> <td data-bbox="817 559 1078 580">FEC2_8000h – FEC2_FFFFh</td> </tr> <tr> <td data-bbox="682 595 698 616">5</td> <td data-bbox="817 595 1078 616">FEC3_0000h – FEC3_7FFFh</td> </tr> <tr> <td data-bbox="682 631 698 652">6</td> <td data-bbox="817 631 1078 652">FEC3_8000h – FEC3_FFFFh</td> </tr> <tr> <td data-bbox="682 667 698 688">7</td> <td data-bbox="817 667 1078 688">FEC4_0000h – FEC4_7FFFh</td> </tr> <tr> <td data-bbox="682 703 698 724">8</td> <td data-bbox="817 703 1078 724">FEC4_8000h – FEC4_FFFFh</td> </tr> </tbody> </table>	Port #	Address	1	FEC1_0000h – FEC1_7FFFh	2	FEC1_8000h – FEC1_FFFFh	3	FEC2_0000h – FEC2_7FFFh	4	FEC2_8000h – FEC2_FFFFh	5	FEC3_0000h – FEC3_7FFFh	6	FEC3_8000h – FEC3_FFFFh	7	FEC4_0000h – FEC4_7FFFh	8	FEC4_8000h – FEC4_FFFFh
Port #	Address																		
1	FEC1_0000h – FEC1_7FFFh																		
2	FEC1_8000h – FEC1_FFFFh																		
3	FEC2_0000h – FEC2_7FFFh																		
4	FEC2_8000h – FEC2_FFFFh																		
5	FEC3_0000h – FEC3_7FFFh																		
6	FEC3_8000h – FEC3_FFFFh																		
7	FEC4_0000h – FEC4_7FFFh																		
8	FEC4_8000h – FEC4_FFFFh																		
6:3	Reserved																		
2	<p><b>Bridge Type (BT)</b>—R/WO. This register can be used to modify the Base Class and Header Type fields from the default PCI-to-PCI bridge to a Host Bridge. Having the root port appear as a Host Bridge is useful in some server configurations.            0 = The root port bridge type is a PCI-to-PCI Bridge, Header Sub-Class = 04h, and Header Type = Type 1.            1 = The root port bridge type is a PCI-to-PCI Bridge, Header Sub-Class = 00h, and Header Type = Type 0.</p>																		
1	<p><b>Hot-Plug SMI Enable (HPME)</b>—R/W.            0 = SMI generation based on a hot-plug event is disabled.            1 = Enables the root port to generate SMI whenever a hot-plug event is detected.</p>																		
0	<p><b>Power Management SMI Enable (PMME)</b>—R/W.            0 = SMI generation based on a power management event is disabled.            1 = Enables the root port to generate SMI whenever a power management event is detected.</p>																		

### 17.1.51 SMSCS—SMI/SCI Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: DCh–DFh Attribute: R/WC  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31	<b>Power Management SMI Status (PMCS)</b> —R/WC 1 = PME control logic needs to generate an interrupt, and this interrupt has been routed to generate an SCI.
30	<b>Hot-Plug SCI Status (HPCS)</b> —R/WC 1 = Hot-Plug controller needs to generate an interrupt, and has this interrupt been routed to generate an SCI.
29:5	Reserved
4	<b>Hot-Plug Link Active State Changed SMI Status (HPLAS)</b> —R/WC 1 = SLSTS.LASC (D28:F0/F1/F2/F3/F4/F5:5Ah, bit 8) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5:D8h, bit 1) is set. When this bit is set, an SMI# will be generated.
3:2	Reserved
1	<b>Hot-Plug Presence Detect SMI Status (HPPDM)</b> —R/WC 1 = SLSTS.PDC (D28:F0/F1/F2/F3/F4/F5:5Ah, bit 3) transitioned from 0-to-1, and MPC.HPME (D28:F0/F1/F2/F3/F4/F5:D8h, bit 1) is set. When this bit is set, an SMI# will be generated.
0	<b>Power Management SMI Status (PMMS)</b> —R/WC 1 = RSTS.PS (D28:F0/F1/F2/F3/F4/F5:60h, bit 16) transitioned from 0-to-1, and MPC.PMME (D28:F0/F1/F2/F3/F4/F5:D8h, bit 1) is set.

### 17.1.52 RPDCGEN—Root Port Dynamic Clock Gating Enable Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: E1h Attribute: R/W  
 Default Value: 00h Size: 8-bits

Bits	Description
7	<b>PCIe* Root Port Static Clock Gate Enable (RPSCGEN)</b> —R/W. 0 = Static Clock Gating is disabled for the PCIe* Root Port 1 = Static Clock Gating is enabled for the PCIe Root Port when the corresponding port is disabled in the function disable register.  <b>Note:</b> Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for ports 5–8.
6	<b>Partition Oscillator Clock Gate Enable (POCGE)</b> —R/W. 0 = The oscillator clock gating at the platform level is disabled 1 = Allows the oscillator clock to be gated at the partition level when conditions are met.  <b>Note:</b> This power saving mode can only be if all PCIe* ports has a dedicated CLKREQ# pin.
5	<b>PCIe* Link CLKREQ Enable (PCIELCLKREQEN)</b> —R/W. 0 = PCIe* port must never de-assert the link CLKREQ 1 = Allows the PCIe* port to de-assert the link CLKREQ.  <b>Note:</b> Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for port 5. Only the value from Port 6 is used for port 6.
4	<b>PCIe* CLKREQ Enable (PCIEBBCLKREQEN)</b> —R/W. 0 = PCIe* port must never de-assert the primary interface CLKREQ 1 = Allows the PCIe* port to de-assert the primary CLKREQ.
	 <b>Note:</b> Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for port 5. Only the value from Port 6 is used for port 6.

Bits	Description
3	<b>Shared Resource Dynamic Link Clock Gating Enable (SRDLCGEN)</b> —R/W 0 = Disables dynamic clock gating of the shared resource link clock domain. 1 = Enables dynamic clock gating on the root port shared resource link clock domain. <b>Note:</b> Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for ports 5–8.
2	<b>Shared Resource Dynamic Backbone Clock Gate Enable (SRDBCGEN)</b> —R/W 0 = Disables dynamic clock gating of the shared resource backbone clock domain. 1 = Enables dynamic clock gating on the root port shared resource backbone clock domain. <b>Note:</b> Only the value from Port 1 is used for ports 1–4. Only the value from Port 5 is used for ports 5–8.
1	<b>Root Port Dynamic Link Clock Gate Enable (RPDLCGEN)</b> —R/W 0 = Disables dynamic clock gating of the root port link clock domain. 1 = Enables dynamic clock gating on the root port link clock domain.
0	<b>Root Port Dynamic Backbone Clock Gate Enable (RPDBCGEN)</b> —R/W 0 = Disables dynamic clock gating of the root port backbone clock domain. 1 = Enables dynamic clock gating on the root port backbone clock domain.

### 17.1.53 RPPGE—Root Port Power Gating Enable Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: E2h  
Default Value: 00h

Attribute: R/WS  
Size: 8-bits

Bits	Description
7:4	Reserved
3	<b>L23_Rdy to Detect Transition (L23R2DT)</b> —R/WS. When set by software, the link moves from L23_Rdy to Detect state. This bit is cleared by hardware once the link has successfully transitioned to Detect state. <b>Note:</b> The HSIO power and clocks needed to enable this transition to Detect state is brought up in response to this bit being set by software. <b>Note:</b> If the link is not in L23_Rdy when this bit is set, the bit is cleared immediately by hardware.
2	<b>L23_Rdy Entry Request (L23ER)</b> —R/WS. When set by software, the corresponding PCIe* root port will initiate the sequence to put the link into L2/L3 Ready state. PME_Turn_Off message will be sent and the corresponding PME_TO_Ack response will be returned by the device. Once the link enters L23_Rdy, this bit will be cleared by hardware. Alternatively, this bit will be cleared by hardware when PME_Turn_Off timer Timeout.
1:0	Reserved

### 17.1.54 PECR3—PCI Express\* Configuration Register 3 (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: ECh–EFh Attribute: R/W  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:2	Reserved
1	<b>Subtractive Decode Compatibility Device ID (SDCIDID)</b> —R/W. 0 = This function reports the device Device ID value assigned to the PCI Express Root Ports. See for the value of the DID Register. 1 = This function reports a Device ID of 2448h for mobile.  <b>Note:</b> If subtractive decode (SDE) is enabled, having this bit as '0' allows the function to present a Device ID that is recognized by the operating system.
0	<b>Subtractive Decode Enable (SDE)</b> —R/W. 0 = Subtractive decode is disabled. This function will only claim transactions positively. 1 = This port will subtractively forward transactions across the PCIe link downstream memory and I/O transactions that are not positively claimed by any internal device or bridge.  <b>Note:</b> Software must ensure that only one PCH device is enabled for Subtractive decode at a time.

### 17.1.55 PECR4—PCI Express\* Configuration Register 4 (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: FCh–FFh Attribute: R/W  
Default Value: See Below Size: 32 bits

Bit	Description
31:30	<b>USB 3.0 PCIe* Port 2 Mode Strap (USB3_PCIE_PORT2_MODE_STRAP)</b> —RO 00 = Root Port 2 is statically assigned to PCI Express* (or GbE) (Default) 01 = Root Port 2 is statically assigned to USB 3.0 10 = Reserved 11 = Reserved  <b>Note:</b> Only the value from Port 1 is used.
29:24	Reserved
23:22	<b>SATA Port 3 PCIe* Port 6 Lane 0 Mode Strap (SATAP3_PCIEP6L0_MODE_STRAP)</b> —RO 00 = Statically assigned to SATA Port 3 01 = Statically assigned to PCIe* Port 6 Lane 0 10 = Reserved 11 = Assigned based on the native mode of GPIO37 pin. If the native GPIO37 pin is a 1, then it is assigned to SATA Port 3; otherwise, it is assigned to PCIe* Port 6 Lane 0  <b>Note:</b> If this soft strap is set to 11 then GPIO37 native mode is SATAP3_PCIEP6L0#; otherwise, the native mode is SATAP3GP. <b>Note:</b> This soft strap only has effect if it is allowed by the SATAP3_PCIEP6L0_Mode (bits 13:12 in this register). <b>Note:</b> Only the value from Port 1 is used.

Bit	Description
21:20	<p><b>SATA Port 2 PCIe* Port 6 Lane 1 Mode Strap (SATAP2_PCIEP6L1_MODE_STRAP)</b>—RO</p> <p>00 = Statically assigned to SATA Port 2 01 = Statically assigned to PCIe* Port 6 Lane 1 10 = Reserved 11 = Assigned based on the native mode of GPIO36 pin. If the native GPIO36 pin is a '1', then it is assigned to SATA Port 2, else it is assigned to PCIe* Port 6 Lane 1</p> <p><b>Note:</b> If this soft strap is set to 11, then GPIO36 native mode is SATA2_PCIE6L1#; otherwise, the native mode is SATA2GP. <b>Note:</b> This soft strap only has effect if it is allowed by the SATAP2_PCIE6L1_Mode (bits 11:10 in this register). <b>Note:</b> Only the value from Port 1 is used.</p>
19	<p><b>GbE Over PCI Express Port Enable Strap (GBE_PCIE_PEN_STRAP)</b>—RO.</p> <p>0 = GbE MAC/PHY port communication is not enabled over PCI Express. 1 = The PCI Express port selected by the GBE_PCIEPORTSEL_STRAP (bits 18:16 in this register) will be used for GbE MAC/PHY over PCI Express communication.</p> <p>This strap defines the GbE port.</p> <p><b>Note:</b> The value of this register, not the soft strap, should be used by GbE and PCI Express*. <b>Note:</b> Only the value from Port 1 is used by the lane multiplexing logic.</p>
18:16	<p><b>GbE PCIe* Port Select Strap (GBE_PCIEPORTSEL_STRAP)</b>—RO. Used to determine which PCIe* port to use for GbE MAC/PHY over PCI Express communication.</p> <p>000 = Port 3 001 = Port 4 010 = Port 5 Lane 0 011 = Port 5 Lane 1 100 = Port 5 Lane 2 101 = Port 5 Lane 3 110 – 111 = Reserved</p> <p><b>Note:</b> The value of this register, not the soft strap, should be used by GbE and PCI Express*. <b>Note:</b> Only the value from Port 1 is used by the lane multiplexing logic.</p>
15:14	<p><b>Root Port Configuration Strap (RPC_STRAP)</b>—RO</p> <p><b>For Port 1:</b> 11 = 1x4 Port 1 (x4), Ports 2–4 (Disabled) 10 = 2x2 Port 1 (x2), Port 3 (x2), Ports 2, 4 (Disabled) 01 = 1x2, 2x1 Port 1 (x2), Port 2 (Disabled), Ports 3, 4 (x1) 00 = 4x1 Ports 1–4 (x1)</p> <p><b>For Port 5 and Port 6:</b> 11 = 1x4 10 = 1x2 01 = Reserved 00 = 1x1</p> <p><b>Note:</b> Only the value from Port 1 is used for Ports 1–4. The values from Port 5 and Port 6 are used for the respective ports.</p>
13:12	<p><b>SATA Port 3 PCIe* Port 6 Lane 0 Mode (SATAP3_PCIEP6L0_MODE)</b>—RO</p> <p>00 = Root Port 1 is statically assigned to SATA Port 3 01 = Root Port 1 is statically assigned to PCIe* Port 6 Lane 0 10 = Assigned based on the SATAP3_PCIEP6L0_MODE_STRAP (bits 23:22 in this register) 11 = Reserved</p> <p><b>Note:</b> Only the value from Port 1 is used.</p>

Bit	Description
11:10	<p><b>SATA Port 2 PCIe* Port 6 Lane 1 Mode (SATAP2_PCIEP6L1_MODE)</b>—RO</p> <p>00 = Root Port 1 is statically assigned to SATA Port 2      01 = Root Port 1 is statically assigned to PCIe* Port 6 Lane 1      10 = Assigned based on SATAP2_PCIEP6L1_MODE_STRAP (bits 21:20 in this register)      11 = Reserved</p> <p><b>Note:</b> Only the value from Port 1 is used.</p>
9:2	Reserved
1:0	<p><b>USB 3.0 PCIe* Port 1 Mode Strap (USB3_PCIE_PORT1_MODE)</b>—RO</p> <p>00 = Root Port 1 is statically assigned to PCI Express (or GbE)      01 = Root Port 1 is statically assigned to USB 3.0      10 = Reserved      11 = Reserved</p> <p><b>Note:</b> Only the value from Port 1 is used.</p>

### 17.1.56 UES—Uncorrectable Error Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 104h–107h Attribute: R/WC, RO  
Default Value: 0000000000000xxx0x0x00000000x0000b Size: 32 bits

This register maintains its state through a platform reset. It loses its state upon suspend.

Bit	Description
31:21	Reserved
20	<b>Unsupported Request Error Status (URE)</b> —R/WC. Indicates an unsupported request was received.
19	<b>ECRC Error Status (EE)</b> —RO. ECRC is not supported.
18	<b>Malformed TLP Status (MT)</b> —R/WC. Indicates a malformed TLP was received.
17	<b>Receiver Overflow Status (RO)</b> —R/WC. Indicates a receiver overflow occurred.
16	<b>Unexpected Completion Status (UC)</b> —R/WC. Indicates an unexpected completion was received.
15	<b>Completion Abort Status (CA)</b> —R/WC. Indicates a completer abort was received.
14	<b>Completion Timeout Status (CT)</b> —R/WC. Indicates a completion timed out. This bit is set if Completion Timeout is enabled and a completion is not returned within the time specified by the Completion Timeout Value.
13	<b>Flow Control Protocol Error Status (FCPE)</b> —RO. Flow Control Protocol Errors not supported.
12	<b>Poisoned TLP Status (PT)</b> —R/WC. Indicates a poisoned TLP was received.
11:5	Reserved
4	<b>Data Link Protocol Error Status (DLPE)</b> —R/WC. Indicates a data link protocol error occurred.
3:0	Reserved

### 17.1.57 UEM—Uncorrectable Error Mask Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 108h–10Bh Attribute: R/WO, RO  
Default Value: 00000000h Size: 32 bits

When set, the corresponding error in the UES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:21	Reserved
20	<b>Unsupported Request Error Mask (URE)</b> —R/WO 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
19	ECRC Error Mask (EE)—RO. ECRC is not supported.
18	<b>Malformed TLP Mask (MT)</b> —R/WO 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
17	<b>Receiver Overflow Mask (RO)</b> —R/WO 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
16	<b>Unexpected Completion Mask (UC)</b> —R/WO 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
15	<b>Completion Abort Mask (CA)</b> —R/WO 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
14	<b>Completion Timeout Mask (CT)</b> —R/WO 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
13	Reserved.
12	<b>Poisoned TLP Mask (PT)</b> —R/WO 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
11:5	Reserved
4	<b>Data Link Protocol Error Mask (DLPE)</b> —R/WO 0 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is enabled. 1 = The corresponding error in the UES register (D28:F0/F1/F2/F3/F4/F5:144) is masked.
3:1	Reserved
0	<b>Training Error Mask (TE)</b> —RO. Training Errors not supported

### 17.1.58 UEV—Uncorrectable Error Severity Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 10Ch-10Fh  
Default Value: 00060011h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31:21	Reserved
20	<b>Unsupported Request Error Severity (URE)</b> —R/W 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
19	<b>ECRC Error Severity (EE)</b> —RO. ECRC is not supported.
18	<b>Malformed TLP Severity (MT)</b> —R/W 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
17	<b>Receiver Overflow Severity (RO)</b> —R/W 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
16	Reserved
15	<b>Completion Abort Severity (CA)</b> —R/W 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
14	Reserved
13	<b>Flow Control Protocol Error Severity (FCPE)</b> —RO. Flow Control Protocol Errors not supported.
12	<b>Poisoned TLP Severity (PT)</b> —R/W 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
11:5	Reserved
4	<b>Data Link Protocol Error Severity (DLPE)</b> —R/W 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
3:1	Reserved
0	<b>Training Error Severity (TE)</b> —R/W. TE is not supported.

### 17.1.59 CES—Correctable Error Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 110h–113h      Attribute: R/WC  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:14	Reserved
13	<b>Advisory Non-Fatal Error Status (ANFES)</b> —R/WC 0 = Advisory Non-Fatal Error did not occur. 1 = Advisory Non-Fatal Error did occur.
12	<b>Replay Timer Timeout Status (RTT)</b> —R/WC. Indicates the replay timer timed out.
11:9	Reserved
8	<b>Replay Number Rollover Status (RNR)</b> —R/WC. Indicates the replay number rolled over.
7	<b>Bad DLLP Status (BD)</b> —R/WC. Indicates a bad DLLP was received.
6	<b>Bad TLP Status (BT)</b> —R/WC. Indicates a bad TLP was received.
5:1	Reserved
0	<b>Receiver Error Status (RE)</b> —R/WC. Indicates a receiver error occurred.

### 17.1.60 CEM—Correctable Error Mask Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 114h–117h      Attribute: R/WO  
Default Value: 00002000h      Size: 32 bits

When set, the corresponding error in the CES register is masked, and the logged error will cause no action. When cleared, the corresponding error is enabled.

Bit	Description
31:14	Reserved
13	<b>Advisory Non-Fatal Error Mask (ANFEM)</b> —R/WO. 0 = Does not mask Advisory Non-Fatal errors. 1 = Masks Advisory Non-Fatal errors from a) signaling ERR_COR to the device control register and b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. <b>Note:</b> The correctable error detected bit in the device status register is set whenever the Advisory Non-Fatal error is detected, independent of this mask bit.
12	<b>Replay Timer Timeout Mask (RTT)</b> —R/WO. Mask for replay timer timeout.
11:9	Reserved
8	<b>Replay Number Rollover Mask (RNR)</b> —R/WO. Mask for replay number rollover.
7	<b>Bad DLLP Mask (BD)</b> —R/WO. Mask for bad DLLP reception.
6	<b>Bad TLP Mask (BT)</b> —R/WO. Mask for bad TLP reception.
5:1	Reserved
0	<b>Receiver Error Mask (RE)</b> —R/WO. Mask for receiver errors.

### 17.1.61 AECC—Advanced Error Capabilities and Control Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 118h–11Bh  
 Default Value: 00000000h

Attribute: RO  
 Size: 32 bits

Bit	Description
31:9	Reserved
8	<b>ECRC Check Enable (ECE)</b> —RO. ECRC is not supported.
7	<b>ECRC Check Capable (ECC)</b> —RO. ECRC is not supported.
6	<b>ECRC Generation Enable (EGE)</b> —RO. ECRC is not supported.
5	<b>ECRC Generation Capable (EGC)</b> —RO. ECRC is not supported.
4:0	<b>First Error Pointer (FEP)</b> —RO. Identifies the bit position of the last error reported in the Uncorrectable Error Status Register.

### 17.1.62 RES—Root Error Status Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 130h–133h  
 Default Value: 00000000h

Attribute: R/WC, RO  
 Size: 32 bits

Bit	Description
31:27	<b>Advanced Error Interrupt Message Number (AEMN)</b> —RO. There is only one error interrupt allocated.
26:7	Reserved
6	<b>Fatal Error Messages Received (FEMR)</b> —RO. This bit is set when one or more Fatal Uncorrectable Error Messages have been received.
5	<b>Non-Fatal Error Messages Received (NFEMR)</b> —RO. This bit is set when one or more Non-Fatal Uncorrectable error messages have been received
4	<b>First Uncorrectable Fatal (FUF)</b> —RO. This bit is set when the first Uncorrectable Error message received is for a fatal error.
3	<b>Multiple ERR_FATAL/NONFATAL Received (MENR)</b> —RO. For the PCH, only one error will be captured.
2	<b>ERR_FATAL/NONFATAL Received (ENR)</b> —R/WC 0 = No error message received. 1 = Either a fatal or a non-fatal error message is received.
1	<b>Multiple ERR_COR Received (MCR)</b> —RO. For the PCH, only one error will be captured.
0	<b>ERR_COR Received (CR)</b> —R/WC 0 = No error message received. 1 = A correctable error message is received.

### 17.1.63 L1SECH—L1 Sub-States Extended Capability Header Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 200h–203h Attribute: R/WO, RO  
 Default Value: 00010000h Size: 32 bits

Bit	Description
31:20	<b>Next Capability Offset (NCO)</b> —R/WO. This field contains the offset to the next PCI Express* Capability structure or 00h if no other items exists in the linked list of Capabilities. For Extended Capabilities implemented in Configuration Space, this offset is relative to the beginning of PCI compatible configuration space and, thus, must always be either 00h (for terminating list of capabilities) or greater than OFFh. The bottom 2 bits of this offset are Reserved and must be implemented as 00b; software must mask them to allow for future use of these bits.
19:16	<b>Capability Version (CV)</b> —RO. This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. Must be 1h for this version of the specification.
15:0	<b>PCI Express Extended Capability ID (PCIEEC)</b> —RO. This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability.

### 17.1.64 L1SCAP—L1 Sub-States Capabilities Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 204h–207h Attribute: R/WO, RO  
 Default Value: 0028281Fh Size: 32 bits

Bit	Description
31:24	Reserved
23:19	<b>Port Tpower on Value (PTV)</b> —R/WO. Along with the Port Tpower on Scale field in the L1 Sub-States Capabilities register, sets the time (in us) that this port requires the port on the opposite side of Link to wait in L1.OFF exit after sampling CLKREQ# asserted before actively driving the interface. Port Tpower on is calculated by multiplying the value in this field by the value in the Port Tpower on scale field in the L1 Sub-States capabilities 2 register. Required for all Ports that support L1.OFF.
18	Reserved
17:16	<b>Port Tpower on Scale (PTPOS)</b> —R/WO. Specifies the scale used for Tpower on value field in the L1 Sub-States capabilities register. 00 = 2 $\mu$ s 01 = 10 $\mu$ s 10 = 100 $\mu$ s 11 = Reserved Required for all ports that support L1.OFF.
15:8	<b>Port Common Mode Restore Time (PCMRT)</b> —R/WO. This is the time (in us) required for this port to re-establish common mode. Required for all ports that support L1.OFF.
7:6	Reserved
5	<b>LFAS L1 Sub-States Supported (LFASL1SS)</b> —RO. When set, this bit indicates that this port supports the LFAS mechanism. Required for both upstream and downstream ports.

Bit	Description
4	<b>CLKREQ# L1 Sub-States Supported (CKRQL1SS)</b> —RO. When set, this bit indicates that this port supports the CLKREQ# out-of-band wake mechanism. Required for both upstream and downstream ports. This field must be programmed prior to enabling ASPM.
3	<b>ASPM L1 Sub-States Supported (AL1SS)</b> —R/WO. When set, this bit indicates that this port supports L1 Sub-States for ASPM L1. Required for both upstream and downstream ports. This field must be programmed prior to enabling ASPM.
2	<b>PCI-PM L1 Sub-States Supported (PL1SS)</b> —R/WO. When set, this bit indicates that this port supports L1 Sub-States for PCI-PM. Required for both upstream and downstream ports. This field must be programmed prior to enabling ASPM.
1	<b>L1.SNOOZ Supported (L1SS)</b> —R/WO. When set, this bit indicates that L1.SNOOZ sub-state is supported and this bit must be set by all ports implementing L1 Sub-States. A port that supports L1.OFF must support L1.SNOOZ. Required for both upstream and downstream ports. This field must be programmed prior to enabling ASPM.
0	<b>L1.OFF Supported (L1OS)</b> —R/WO. When set, this bit indicates that L1.OFF power management feature is supported. Required for both upstream and downstream ports. This field must be programmed prior to enabling ASPM.



### 17.1.65 L1SCTL1—L1 Sub-States Control 1 Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 208h–20Bh  
Default Value: 00000010h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:29	<p><b>L1.OFF LTR Threshold Latency Scale Value (L1OFFLRTTLSV)</b>—R/W. This field contains the L1.OFF LTR Threshold Latency Scale Value for this particular PCIe* root port. The value in this field, together with L1OFFLRTLV, is compared against both the snoop and non-snoop LTR values of the device.</p> <p>000 = L1OFFLRTTLSV * 1 ns 001 = L1OFFLRTTLSV * 32 ns 010 = L1OFFLRTTLSV * 1024 ns 011 = L1OFFLRTTLSV * 32768 ns 100 = L1OFFLRTTLSV * 1048576 ns 101 = L1OFFLRTTLSV * 33554432 ns Others = Not Permitted.</p> <p>This field must be programmed prior to enabling L1.OFF.</p>
28:26	Reserved
25:16	<p><b>L1.OFF LTR Threshold Latency Value (L1OFFLRTTLV)</b>—R/W. This field contains the L1.OFF LTR Threshold Latency Value for this particular PCIe* root port. The value in this field, together with L1OFFLRTTLSV, is compared against both the snoop and non-snoop LTR values of the device.</p> <p>This field must be programmed prior to enabling L1.OFF.</p>
15:8	<p><b>Common Mode Restore Time (CMRT)</b>—RW. This is the Tcommon_mode time the PCIe* root port needs to continue sending TS1 and refrain from sending TS2 in Recovery state to allow the TX common mode to be established prior to sending TS2. The timer starts from the time when the first TS1 has been sent and the receiver has detected un-squelch. The value in this field defines the time in micro-seconds.</p> <p>This field must be programmed prior to enabling L1.OFF.</p>
7:5	Reserved
4	<p><b>Select L1 Sub-States Mechanism (SLSM)</b>—RO. When set, this bit indicates that this Port must use the CLKREQ# based mechanism. When clear, the LFSAS mechanism must be used.</p> <p>Ports that support only one mechanism for L1 Sub-States are permitted to implement this bit as RO/ Hardware Initiated and the value of this bit must reflect the supported mechanism.</p>
3	<p><b>ASPM L1 Sub-States Enabled (AL1SE)</b>—RW. When set, this bit indicates that L1 Sub-States are enabled for ASPM.</p> <p>Required for both upstream and downstream ports.</p>
2	<p><b>PCI-PM L1 Sub-States Enabled (PPL1SE)</b>—R/W. When set, this bit indicates that L1 Sub-States are enabled for PCI-PM.</p> <p>Required for both upstream and downstream ports.</p>
1	<p><b>L1.SNOOZ Enable (L1SE)</b>—R/W. When set, this bit indicates that L1.SNOOZ power management feature is enabled. If L1.OFF is enabled, L1.SNOOZ must also be enabled.</p> <p>This field must be programmed prior to enabling ASPM L1.</p>
0	<p><b>L1.OFF Enable (L1OE)</b>—R/W. When set, this bit indicates that L1.OFF power management feature is enabled. L1.OFF can only be enabled if platform supports bi-directional CLKREQPLUS#.</p> <p>This field must be programmed prior to enabling ASPM L1.</p> <p>Ports that support L1.OFF shall support Latency Tolerance Reporting.</p>

### 17.1.66 L1SCTL2—L1 Sub-States Control 2 Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 20Ch–20Fh  
Default Value: 00000028h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:8	Reserved
7:3	<b>Power On Wait Time (POWT)</b> —R/W. Along with the Tpower on Scale sets the minimum amount of time (in us) that the Port must wait in L1.OFF EXIT after sampling CLKREQPLUS# asserted before actively driving the interface. The timer starts counting when CLKREQPLUS# asserts in L1.OFF state. This field must be programmed prior to enabling L1.OFF.
2	Reserved
1:0	<b>Tpower on Scale (TPOS)</b> —R/W. Specifies the scale used for Tpower on value. 00 = 2 µs 01 = 10 µs 10 = 100 µs 11 = Reserved Required for all ports that support L1.OFF.

### 17.1.67 PECR2—PCI Express\* Configuration Register 2 (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 320–323h Attribute: R/W  
Default Value: 0004b05bh Size: 32 bits

Bit	Description
31:20	Reserved
21	<b>PECR2 Field 1</b> —R/W. BIOS must set this bit to 1b.
20:0	Reserved

### 17.1.68 PEETM—PCI Express\* Extended Test Mode Register (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 324h–327h Attribute: RO, R/W  
Default Value: See Description Size: 32 bits

Bit	Description
31:5	Reserved
4	<b>Lane Reversal (LR)</b> —RO. This register reads the setting of the PCIELR1 soft strap for port 1 and the PCIELR2 soft strap for port 5. 0 = No Lane reversal (default). 1 = PCI Express* lanes 0 – 3 (register in port 1) or lanes 4 – 7 (register in port 5) are reversed. <b>Notes:</b> 1. The port configuration straps must be set such that Port 1 or Port 5 is configured as a x4 port using lanes 0 – 3, or 4 – 7 when Lane Reversal is enabled. x2 lane reversal is not supported. 2. This register is only valid on port 1 (for ports 1 – 4) or port 5 (for ports 5 – 8).
3	Reserved
2	<b>Scrambler Bypass Mode (BAU)</b> —R/W 0 = Normal operation. Scrambler and descrambler are used. 1 = Bypasses the data scrambler in the transmit direction and the data de-scrambler in the receive direction. <b>Note:</b> This functionality intended for debug/testing only. <b>Note:</b> If bypassing scrambler with the PCH root port 1 in x4 configuration, each PCH root port must have this bit set.
1:0	Reserved

### 17.1.69 PEC1—PCI Express\* Configuration Register 1 (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 330h–333h Attribute: RO, R/W  
Default Value: 28000016h Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>PEC1 Field 1</b> —R/W. BIOS must program this field to 40h.

### 17.1.70 PEC4—PCI Express\* Configuration Register 4 (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 408h–40Bh  
Default Value: 0h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31:28	Reserved
27	<b>Squelch Disable (SQDIS)</b> —R/W. When set, this bit disables the squelch circuitry for all the lanes owned by this port. This bit is used to shut-off the squelch circuitry when the port, which owns a number of lanes, is being functionally disabled.
26:0	Reserved

### 17.1.71 PEC2—PCI Express\* Configuration Register 2 (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 418h–41Bh  
Default Value: 00000930h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31:16	<b>PEC2A</b> —R/W. BIOS may program this field
15:12	Reserved – RO. 00b
11:4	<b>PEC2B</b> —R/W. BIOS may program this field
3:2	Reserved – RO. 00b
1:0	<b>Dynamic Throttling Enable (DPLTE)</b> —R/W. 00 = Disabled 01 = Reserved 10 = Reserved 11 = Enabled

### 17.1.72 PEC3—PCI Express\* Configuration Register 3 (PCI Express\*—D28:F0/F1/F2/F3/F4/F5)

Address Offset: 420h–423h  
Default Value: 028E8746h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>PEC3 Field 1</b> —R/W. BIOS may set this bit to 1b.

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# 18 Serial Peripheral Interface (SPI)

The Serial Peripheral Interface resides in memory-mapped space. This function contains registers that allow for the setup and programming of devices that reside on the SPI interface.

**Note:** All registers in this function (including memory-mapped registers) must be addressable in byte, word, and DWord quantities. The software must always make register accesses on natural boundaries (that is, DWord accesses must be on DWord boundaries; word accesses on word boundaries, and so on). In addition, the memory-mapped register space must not be accessed with the LOCK semantic exclusive-access mechanism. If software attempts exclusive-access mechanisms to the SPI memory-mapped space, the results are undefined.

## 18.1 Serial Peripheral Interface Memory Mapped Configuration Registers

The SPI Host Interface registers are memory-mapped in the RCRB (Root Complex Register Block) Chipset Register Space with a base address (SPIBAR) of 3800h and are located within the range of 3800h to 39FFh. The address for RCRB can be found in RCBA Register see [Section 10.1.40](#). The individual registers are then accessible at SPIBAR + Offset as indicated in the following table.

These memory mapped registers must be accessed in byte, word, or DWord quantities.

**Table 18-1. Serial Peripheral Interface (SPI) Register Address Map (SPI Memory Mapped Configuration Registers) (Sheet 1 of 2)**

SPIBAR + Offset	Mnemonic	Register Name	Default
00h-03h	BFPR	BIOS Flash Primary Region	00000000h
04h-05h	HSFS	Hardware Sequencing Flash Status	0000h
06h-07h	HSFC	Hardware Sequencing Flash Control	0000h
08h-0Bh	FADDR	Flash Address	00000000h
0Ch-0Fh	—	Reserved	00000000h
10h-13h	FDATA0	Flash Data 0	00000000h
14h-4Fh	FDATAN	Flash Data N	00000000h
50h-53h	FRAP	Flash Region Access Permissions	00000202h
54h-57h	FREG0	Flash Region 0	00000000h
58h-5Bh	FREG1	Flash Region 1	00000000h
5Ch-5Fh	FREG2	Flash Region 2	00000000h
60h-63h	FREG3	Flash Region 3	00000000h
64h-67h	FREG4	Flash Region 4	00000000h
67h-73h	—	Reserved for Future Flash Regions	
74h-77h	PRO	Flash Protected Range 0	00000000h

**Table 18-1. Serial Peripheral Interface (SPI) Register Address Map  
(SPI Memory Mapped Configuration Registers) (Sheet 2 of 2)**

SPIBAR + Offset	Mnemonic	Register Name	Default
78h-7Bh	PR1	Flash Protected Range 1	00000000h
7Ch-7Fh	PR2	Flash Protected Range 2	00000000h
80h-83h	PR3	Flash Protected Range 3	00000000h
84h-87h	PR4	Flash Protected Range 4	00000000h
88h-8Fh	—	Reserved	—
90h	SSFS	Software Sequencing Flash Status	00h
91h-93h	SSFC	Software Sequencing Flash Control	0000h
94h-95h	PREOP	Prefix Opcode Configuration	0000h
96h-97h	OPTYPE	Opcode Type Configuration	0000h
98h-9Fh	OPMENU	Opcode Menu Configuration	0000000000000h
A0h	BBAR	BIOS Base Address Configuration	00000000h
B0h-B3h	FDOC	Flash Descriptor Observability Control	00000000h
B4h-B7h	FDOD	Flash Descriptor Observability Data	00000000h
B8h-C3h	—	Reserved	—
C0h-C3h	AFC	Additional Flash Control	00000000h
C4h-C7h	LVSCC	Host Lower Vendor Specific Component Capabilities	00000000h
C8h-C11h	UVSCC	Host Upper Vendor Specific Component Capabilities	00000000h
CC-CFh	PTINX	Parameter Table Index	00000000h
D0h-D3h	PTDATA	Parameter Table Data	00000000h
F0h-F3h	SRDL	Soft Reset Data Lock	00000000h
F4h-F7h	SRDC	Soft Reset Data Control	00000000h
F8h-FBh	SRD	Soft Reset Data	00000000h

### 18.1.1 BFPR—BIOS Flash Primary Region Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 00h Attribute: RO  
 Default Value: 00000000h Size: 32 bits

**Note:** This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	<b>BIOS Flash Primary Region Limit (PRL)</b> —RO. This specifies address bits 24:12 for the Primary Region Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15:13	Reserved
12:0	<b>BIOS Flash Primary Region Base (PRB)</b> —RO. This specifies address bits 24:12 for the Primary Region Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base

### 18.1.2 HSFS—Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 04h Attribute: RO, R/W/L, R/C/W  
 Default Value: 0000h Size: 16 bits

Bit	Description
15	<b>Flash Configuration Lock-Down (FLOCKDN)</b> —R/W/L. When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset due to a global reset or host partition reset in an Intel® ME enabled system.
14	<b>Flash Descriptor Valid (FDV)</b> —RO. This bit is set to a 1 if the Flash Controller reads the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1, software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	<b>Flash Descriptor Override Pin Strap Status (FDOPSS)</b> —RO. This bit indicates the condition of the Flash Descriptor Security Override/Intel® ME Debug Mode pin strap. 0 = The Flash Descriptor Security Override/Intel® ME Debug Mode strap is set using an external pull-up on HDA_SDO 1 = No override
12:6	Reserved
5	<b>SPI Cycle In Progress (SCIP)</b> —RO. Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.  <b>Note:</b> This field is only applicable when in Descriptor mode and Hardware sequencing is being used.

Bit	Description
4:3	<b>Block/Sector Erase Size (BERASE)</b> —RO. This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 = 256 Byte 01 = 4KB 10 = 8KB 11 = 64KB If the FLA is less than FLCOMP.CODEN then this field reflects the Component 0 Block/Sector Erase Size (BES). Otherwise it reflects the Component 1 BES. If SFDPn is valid and advertises 4KB erase capability, then BES is taken from the SFDPn table, otherwise it is taken from the BIOS VSCC table. <b>Note:</b> If SFDPn is the BES source, then '11' means "not 4KB" erase.
2	<b>Access Error Log (AEL)</b> —R/W/C. Hardware sets this bit to a 1 when an attempt was made to access the GbE region using the direct access method or an access to the GbE Program Registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a 1. <b>Note:</b> This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
1	<b>Flash Cycle Error (FCERR)</b> —R/W/C. Hardware sets this bit to 1 when a program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until a hardware reset occurs due to a global reset or host partition reset in an Intel® ME enabled system. Software must clear this bit before setting the FLASH Cycle GO bit in this register. <b>Note:</b> This field is only applicable when in Descriptor mode and Hardware sequencing is being used.
0	<b>Flash Cycle Done (FDONE)</b> —R/W/C. The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access. <b>Note:</b> This field is only applicable when in Descriptor mode and Hardware sequencing is being used.

### 18.1.3 HSFC—Hardware Sequencing Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 06h Attribute: R/W, R/W/S  
 Default Value: 0000h Size: 16 bits

**Note:** This register is only applicable when SPI device is in Descriptor mode.

Bit	Description
15	<b>Flash SPI SMI# Enable (FSMIE)</b> —R/W. When set to 1, the SPI asserts an SMI# request whenever the Flash Cycle Done bit is 1.
14	Reserved
13:8	<b>Flash Data Byte Count (FDBC)</b> —R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based with 0b representing 1 byte and 111111b representing 64 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	Reserved
2:1	<b>FLASH Cycle (FCYCLE)</b> —R/W. This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 = Read (1 up to 64 bytes by setting FDBC) 01 = Reserved 10 = Write (1 up to 64 bytes by setting FDBC) 11 = Block Erase
0	<b>Flash Cycle Go (FGO)</b> —R/W/S. A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

### 18.1.4 FADDR—Flash Address Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 08h Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:25	Reserved
24:0	<b>Flash Linear Address (FLA)</b> —R/W. The FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which GbE has access permissions. Hardware must convert the FLA into a Flash Physical Address (FPA) before running this cycle on the SPI bus.

### 18.1.5 FDAT0—Flash Data 0 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 10h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<p><b>Flash Data 0 (FD0)</b>—R/W. This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle.</p> <p>This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle.</p> <p>The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, and so on. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-...-8-23-22-...-16-31...24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address.</p> <p>The data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.</p>

### 18.1.6 FDATAN—Flash Data [N] Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 14h      Attribute: R/W

SPIBAR + 18h  
 SPIBAR + 1Ch  
 SPIBAR + 20h  
 SPIBAR + 24h  
 SPIBAR + 28h  
 SPIBAR + 2Ch  
 SPIBAR + 30h  
 SPIBAR + 34h  
 SPIBAR + 38h  
 SPIBAR + 3Ch  
 SPIBAR + 40h  
 SPIBAR + 44h  
 SPIBAR + 48h  
 SPIBAR + 4Ch

Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Flash Data N (FD[N])</b> —R/W. Similar definition as Flash Data 0. However, this register does not begin shifting until FD[N-1] has completely shifted in/out.

### 18.1.7 FRAP—Flash Regions Access Permissions Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 50h Attribute: RO, R/W  
 Default Value: 00000202h Size: 32 bits

**Note:** This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:24	<b>BIOS Master Write Access Grant (BMWAG)</b> —R/W. Each bit [31:29] corresponds to Master[7:0]. BIOS can grant one or more masters write access to the BIOS region 1 overriding the permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel® Management Engine, Master[3] is Host processor/GbE. Master[0] and Master[7:4] are reserved. The contents of this register field are locked by the FLOCKDN bit.
23:16	<b>BIOS Master Read Access Grant (BMRAG)</b> —R/W. Each bit [28:16] corresponds to Master[7:0]. BIOS can grant one or more masters read access to the BIOS region 1 overriding the read permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel® Management Engine, Master[3] is Host processor/GbE. Master[0] and Master[7:4] are reserved. The contents of this register field are locked by the FLOCKDN bit.
15:8	<b>BIOS Region Write Access (BRWA)</b> —RO. Each bit [15:8] corresponds to Regions [7:0]. If the bit is set, this master can erase and write that particular region through register accesses.
7:0	<b>BIOS Region Read Access (BRRA)</b> —RO. Each bit [7:0] corresponds to Regions [7:0]. If the bit is set, this master can read that particular region through register accesses.

### 18.1.8 FREG0—Flash Region 0 (Flash Descriptor) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 54h Attribute: RO  
 Default Value: 00000000h Size: 32 bits

**Note:** This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)/Flash Descriptor Base Address Region (FDBAR)</b> —RO. This specifies address bits 24:12 for the Region 0 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base.

### 18.1.9 FREG1—Flash Region 1 (BIOS Descriptor) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 58h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

**Note:** This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)</b> —RO. This specifies address bits 24:12 for the Region 1 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

### 18.1.10 FREG2—Flash Region 2 (Intel® ME) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 5Ch      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

**Note:** This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This field specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)</b> —RO. This field specifies address bits 24:12 for the Region 2 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base

### 18.1.11 FREG3—Flash Region 3 (GbE) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 60h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

**Note:** This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This field specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)</b> —RO. This field specifies address bits 24:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

### 18.1.12 FREG4—Flash Region 4 (Platform Data) Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 64h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

**Note:** This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This field specifies address bits 24:12 for the Region 4 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)</b> —RO. This field specifies address bits 24:12 for the Region 4 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG4.Region Base.

### 18.1.13 PR0—Protected Range 0 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 74h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

**Note:** This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	<b>Write Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	<b>Protected Range Limit</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	<b>Read Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that reads directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	<b>Protected Range Base</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

### 18.1.14 PR1—Protected Range 1 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 78h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

**Note:** This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	<b>Write Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	<b>Protected Range Limit</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	<b>Read Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	<b>Protected Range Base</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

### 18.1.15 PR2—Protected Range 2 Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 7Ch      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

**Note:** This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	<b>Write Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	<b>Protected Range Limit</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	<b>Read Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	<b>Protected Range Base</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

### 18.1.16 PR3—Protected Range 3 Register (SPI Memory Mapped Configuration Registers)

See Protected Range 0 for the detailed description.

### 18.1.17 PR4—Protected Range 4 Register (SPI Memory Mapped Configuration Registers)

See Protected Range 0 for the detailed description.

### 18.1.18 SSFS—Software Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 90h      Attribute: RO, R/WC  
Default Value: 00h      Size: 8 bits

**Note:** The Software Sequencing Control and Status registers are reserved if the Hardware Sequencing Control and Status registers are used.

Bit	Description
7:5	Reserved
4	<b>Access Error Log (AEL)</b> —RO. This bit reflects the value of the Hardware Sequencing Status AEL register.
3	<b>Flash Cycle Error (FCERR)</b> —R/WC. Hardware sets this bit to 1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system.
2	<b>Cycle Done Status</b> —R/WC. The PCH sets this bit to 1 when the SPI cycle completes (that is, SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	Reserved
0	<b>SPI Cycle In Progress (SCIP)</b> —RO. Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.

### 18.1.19 SSFC—Software Sequencing Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 91h      Attribute: R/W, R/WS  
Default Value: F80000h      Size: 24 bits

Bit	Description
23:19	Reserved – BIOS must set this field to '11111'b
18:16	<b>SPI Cycle Frequency (SCF)</b> —R/W. This register sets the frequency to use for all SPI software sequencing cycles (write, erase, fast read, read status, and so on) except for the read cycle which always run at 20 MHz. 000 = 20 MHz 001 = 33 MHz 100 = 50 MHz All other values reserved. This register field is locked when the SPI Configuration Lock-Down bit is set.
15	<b>SPI SMI# Enable (SME)</b> —R/W. When set to 1, the SPI asserts an SMI# request whenever the Cycle Done Status bit is 1.
14	<b>Data Cycle (DS)</b> —R/W. When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are don't cares.
13:8	<b>Data Byte Count (DBC)</b> —R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. When this field is 00_0000b, there is 1 byte to transfer; 11_1111b means there are 64 bytes to transfer.
7	Reserved
6:4	<b>Cycle Opcode Pointer (COP)</b> —R/W. This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	<b>Sequence Prefix Opcode Pointer (SPOP)</b> —R/W. This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the PCH supports flash devices that have different opcodes for enabling writes to the data space versus status register.
2	<b>Atomic Cycle Sequence (ACS)</b> —R/W. When set to 1 along with the SCGO assertion, the PCH will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of: <ul style="list-style-type: none"> <li>Atomic Sequence Prefix Command (8-bit opcode only)</li> <li>Primary Command specified below by software (can include address and data)</li> <li>Polling the Flash Status Register (opcode 05h) until bit 0 becomes 0b.</li> </ul> The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
1	<b>SPI Cycle Go (SCGO)</b> —R/WS. This bit always returns 0 on reads. However, a write to this register with a 1 in this bit starts the SPI cycle defined by the other bits of this register. The "SPI Cycle in Progress" (SCIP) bit gets set by this action. Hardware must ignore writes to this bit while the Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write.
0	Reserved

### 18.1.20 PREOP—Prefix Opcode Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 94h      Attribute: R/W  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:8	<b>Prefix Opcode 1</b> —R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	<b>Prefix Opcode 0</b> —R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

**Note:** This register is not writable when the Flash Configuration Lock-Down bit (SPIBAR + 04h:15) is set.

### 18.1.21 OPTYPE—Opcode Type Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 96h      Attribute: R/W  
 Default Value: 0000h      Size: 16 bits

Entries in this register correspond to the entries in the Opcode Menu Configuration register.

**Note:** The definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, “Chip Erase” and “Auto-Address Increment Byte Program”).

Bit	Description
15:14	<b>Opcode Type 7</b> —R/W. See the description for bits 1:0
13:12	<b>Opcode Type 6</b> —R/W. See the description for bits 1:0
11:10	<b>Opcode Type 5</b> —R/W. See the description for bits 1:0
9:8	<b>Opcode Type 4</b> —R/W. See the description for bits 1:0
7:6	<b>Opcode Type 3</b> —R/W. See the description for bits 1:0
5:4	<b>Opcode Type 2</b> —R/W. See the description for bits 1:0
3:2	<b>Opcode Type 1</b> —R/W. See the description for bits 1:0
1:0	<b>Opcode Type 0</b> —R/W. This field specifies information about the corresponding Opcode 0. This information allows the hardware to: 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The encoding of the two bits is: 00 = No address associated with this Opcode; Read cycle type 01 = No address associated with this Opcode; Write cycle type 10 = Address required; Read cycle type 11 = Address required; Write cycle type

**Note:** This register is not writable when the SPI Configuration Lock-Down bit (SPIBAR + 00h:15) is set.

### 18.1.22 OPMENU—Opcode Menu Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + 98h Attribute: R/W  
Default Value: 0000000000000000h Size: 64 bits

Eight entries are available in this register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

**Note:** It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Bit	Description
63:56	<b>Allowable Opcode 7</b> —R/W. See the description for bits 7:0
55:48	<b>Allowable Opcode 6</b> —R/W. See the description for bits 7:0
47:40	<b>Allowable Opcode 5</b> —R/W. See the description for bits 7:0
39:32	<b>Allowable Opcode 4</b> —R/W. See the description for bits 7:0
31:24	<b>Allowable Opcode 3</b> —R/W. See the description for bits 7:0
23:16	<b>Allowable Opcode 2</b> —R/W. See the description for bits 7:0
15:8	<b>Allowable Opcode 1</b> —R/W. See the description for bits 7:0
7:0	<b>Allowable Opcode 0</b> —R/W. Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

This register is not writable when the SPI Configuration Lock-Down bit (SPIBAR + 00h:15) is set.

### 18.1.23 BBAR—BIOS Base Address Configuration Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + A0h Attribute: R/W  
Default Value: 00000000h Size: 32 bits

Eight entries are available in this register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

Bit	Description
31:24	Reserved
23:8	<b>Bottom of System Flash</b> —R/W. This field determines the bottom of the System BIOS. The PCH will not run programmed commands nor memory reads whose address field is less than this value. This field corresponds to bits 23:8 of the 3-byte address; bits 7:0 are assumed to be 00h for this vector when comparing to a potential SPI address.  <b>Note:</b> The SPI host controller prevents any programmed cycle using the address register with an address less than the value in this register. Some flash devices specify that the Read ID command must have an address of 0000h or 0001h. If this command must be supported with these devices, it must be performed with the BIOS BAR.
7:0	Reserved

### 18.1.24 FDOC—Flash Descriptor Observability Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + B0h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

**Note:** This register can be used to observe the contents of the Flash Descriptor that is stored in the PCH Flash Controller. This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:15	Reserved
14:12	<b>Flash Descriptor Section Select (FDSS)</b> —R/W. Selects which section within the loaded Flash Descriptor to observe. 000 = Flash Signature and Descriptor Map 001 = Component 010 = Region 011 = Master 111 = Reserved
11:2	<b>Flash Descriptor Section Index (FDSI)</b> —R/W. Selects the DWord offset within the Flash Descriptor Section to observe.
1:0	Reserved

### 18.1.25 FDOD—Flash Descriptor Observability Data Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + B4h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

**Note:** This register can be used to observe the contents of the Flash Descriptor that is stored in the PCH Flash Controller.

Bit	Description
31:0	<b>Flash Descriptor Section Data (FDSD)</b> —RO. Returns the DWord of data to observe as selected in the Flash Descriptor Observability Control.

### 18.1.26 AFC—Additional Flash Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + C0h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits.

Bit	Description
31:3	Reserved
2:1	<b>Flash Controller Interface Dynamic Clock Gating Enable</b> —R/W. 00 = Flash Controller Interface Dynamic Clock Gating is Disabled 11 = Flash Controller Interface Dynamic Clock Gating is Enabled Other encodings are Reserved.
0	<b>Flash Controller Core Dynamic Clock Gating Enable</b> —R/W. 0 = Flash Controller Core Dynamic Clock Gating is Disabled 1 = Flash Controller Core Dynamic Clock Gating is Enabled

### 18.1.27 LVSCC—Host Lower Vendor Specific Component Capabilities Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + C4h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

**Note:** All attributes described in LVSCC must apply to all flash space below the FPBA, even if it spans between two separate flash parts. This register is only applicable when an SPI device is in descriptor mode.

Bit	Description
31:24	Reserved
23	<b>Vendor Component Lock (LVCL)</b> —R/W. This register bit locks itself when set. 0 = The lock bit is not set 1 = The Vendor Component Lock bit is set.  <b>Note:</b> This bit applies to both UVS CC and LVSCC registers.
22:16	Reserved
15:8	<b>Lower Erase Opcode (LEO)</b> —R/W. This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. This register field is locked by the Vendor Component Lock (LVCL) bit.
7:5	Reserved
4	<b>Write Enable on Write Status (LWEWS)</b> —R/W. This bit is locked by the Vendor Component Lock (LVCL) bit. 0 = No automatic write of 00h will be made to the SPI flash's status register 1 = A write of 00h to the SPI flash's Status register will be sent on EVERY write and erase to the SPI flash. 06h 01h 00h is the opcode sequence used to unlock the Status register.  <b>Notes:</b> 1. This bit should not be set to 1 if there are non-volatile bits in the SPI flash's Status register. This may lead to premature flash wear out. 2. This is not an atomic sequence. If the SPI component's Status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. Bit 3 and bit 4 should NOT be both set to 1.

Bit	Description
3	<p><b>Lower Write Status Required (LWSR)</b>—R/W. This register bit is locked by the Vendor Component Lock (LVCL) bit.</p> <p>0 = No automatic write of 00h will be made to the SPI flash's Status register</p> <p>1 = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash. 50h 01h 00h is the opcode sequence used to unlock the Status register.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. This bit should not be set to 1 if there are non volatile bits in the SPI flash's Status register. This may lead to premature flash wear out.</li> <li>2. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part.</li> <li>3. Bit 3 and bit 4 should NOT be both set to 1.</li> </ol>
2	<p><b>Lower Write Granularity (LWG)</b>—R/W. This register bit is locked by the Vendor Component Lock (LVCL) bit.</p> <p>0 = 1 Byte</p> <p>1 = 64 Byte</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components.</li> <li>2. If using 64 Byte write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a feature page writable SPI flash.</li> </ol>
1:0	<p><b>Lower Block/Sector Erase Size (LBES)</b>—R/W. This field identifies the erasable sector size for all Flash components.</p> <p>00 = 256 Byte</p> <p>01 = 4KB</p> <p>10 = 8KB</p> <p>11 = 64KB</p> <p>This register field is locked by the Vendor Component Lock (LVCL) bit.</p> <p>Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is less than FPBA.</p>

### 18.1.28 UVSCC—Host Upper Vendor Specific Component Capabilities Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + C8h Attribute: R/W  
Default Value: 00000000h Size: 32 bits

**Note:** All attributes described in UVSCC must apply to all flash space equal to or above the FPBA, even if it spans between two separate flash parts. This register is only applicable when SPI device is in descriptor mode.

**Note:** To prevent this register from being modified the LVSCC.VCL bit must be used.

Bit	Description
31:16	Reserved
15:8	<b>Upper Erase Opcode (UEO)</b> —R/W. This register is programmed with the Flash erase instruction opcode required by the vendor's Flash component. This register field is locked by the Vendor Component Lock (UVCL) bit.
7:5	Reserved
4	<b>Write Enable on Write Status (UWEWS)</b> —R/W. This register bit is locked by the Vendor Component Lock (UVCL) bit. 0 = No automatic write of 00h will be made to the SPI flash's Status register 1 = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash. 06h 01h 00h is the opcode sequence used to unlock the Status register. <b>Notes:</b> 1. This bit should not be set to 1 if there are non volatile bits in the SPI flash's Status register. This may lead to premature flash wear out. 2. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. Bit 3 and bit 4 should NOT be both set to 1.
3	<b>Upper Write Status Required (UWSR)</b> —R/W. This register bit is locked by the Vendor Component Lock (UVCL) bit. 0 = No automatic write of 00h will be made to the SPI flash's status register 1 = A write of 00h to the SPI flash's status register will be sent on EVERY write and erase to the SPI flash. 50h 01h 00h is the opcode sequence used to unlock the Status register. <b>Notes:</b> 1. This bit should not be set to '1' if there are non volatile bits in the SPI flash's Status register. This may lead to premature flash wear out. 2. This is not an atomic sequence. If the SPI component's status register is non-volatile, then BIOS should issue an atomic software sequence cycle to unlock the flash part. 3. Bit 3 and bit 4 should NOT be both set to 1.
2	<b>Upper Write Granularity (UWG)</b> —R/W. This register bit is locked by the Vendor Component Lock (UVCL) bit. 0 = 1 Byte 1 = 64 Byte <b>Notes:</b> 1. If more than one Flash component exists, this field must be set to the lowest common write granularity of the different Flash components. 2. If using 64 B write, BIOS must ensure that multiple byte writes do not occur over 256 B boundaries. This will lead to corruption as the write will wrap around the page boundary on the SPI flash part. This is a a feature page writable SPI flash.
1:0	<b>Upper Block/Sector Erase Size (UBES)</b> —R/W. This field identifies the erasable sector size for all Flash components. Valid Bit Settings: 00 = 256 Byte 01 = 4KB 10 = 8KB 11 = 64KB This register field is locked by the Vendor Component Lock (UVCL) bit. Hardware takes no action based on the value of this register. The contents of this register are to be used only by software and can be read in the HSFSTS.BERASE register in both the BIOS and the GbE program registers if FLA is greater or equal to FPBA.

### 18.1.29 PTINX—Parameter Table Index Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + CCh Attribute: R/W  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:16	Reserved
15:14	<b>Supported Parameter Table (SPT)</b> —R/W. Selects which supported parameter table to observe. 00 = Component 0 Property Parameter Table 01 = Component 1 Property Parameter Table 10-11 = Reserved
13:12	<b>Header or Data (HORD)</b> —R/W. Select parameter table header DWord versus Data DWord. 00 = SFDP Header 01 = Parameter Table Header 10 = Data 11 = Reserved
11:2	<b>Parameter Table DW Index (PTDWI)</b> —R/W. Selects the DWord offset within the parameter table to observe.
1:0	Reserved

### 18.1.30 PTDATA—Parameter Table Data Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + D0h Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Parameter Table DW (PTDWD)</b> —RO. Returns the DWord of data to observe as selected in the Parameter Table Index register.  <b>Note:</b> The returned value of reserved fields in the SFDP header or table must be ignored by software. The flash controller may return either 0 or 1 for these fields.

### 18.1.31 FPB—Flash Partition Boundary Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + D0h Attribute: RO  
Default Value: 00000000h Size: 32 bits

**Note:** This register is only applicable when SPI device is in descriptor mode.

Bit	Description
31:13	Reserved
12:0	<b>Flash Partition Boundary Address (FPBA)</b> —RO. This register reflects the value of Flash Descriptor Component FPBA field.

### 18.1.32 SRDL—Soft Reset Data Lock Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + F0h Attribute: R/WL  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Set_Strip Lock (SSL)</b> —R/WL. 0 = The SRDL (this register), SRDC (SPIBAR+F4h), and SRD (SPIBAR+F4h) registers are writeable. 1 = The SRDL (this register), SRDC (SPIBAR+F4h), and SRD (SPIBAR+F4h) registers are locked. <b>Note:</b> That this bit is reset to '0' on CF9h resets.

### 18.1.33 SRDC—Soft Reset Data Control Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + F4h Attribute: R/WL  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Soft Reset Data Select (SRDS)</b> —R/WL. 0 = The Set_Strip data sends the default processor configuration data. 1 = The Set_Strip message bits come from the Set_Strip Msg Data register. <b>Notes:</b> 1. This bit is reset by the RSMRST# or when the Resume well loses power. 2. This bit is locked by the SSL bit (SPIBAR+F0h:bit 0).

### 18.1.34 SRD—Soft Reset Data Register (SPI Memory Mapped Configuration Registers)

Memory Address: SPIBAR + F8h      Attribute: R/WL  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:14	Reserved
13:0	<b>Set_Strip Data (SSD)—R/WL.</b> <b>Notes:</b> <ol style="list-style-type: none"> <li>These bits are reset by the RSMRST#, or when the Resume well loses power.</li> <li>These bits are locked by the SSL bit (SPIBAR+F0h:bit 0).</li> </ol>

## 18.2 Flash Descriptor Records

The following sections describe the data structure of the Flash Descriptor on the SPI device. These are not registers within the PCH.

### 18.3 OEM Section

Memory Address: F00h      Default Value:      Size: 256 Bytes

256 Bytes are reserved at the top of the Flash Descriptor for use by the OEM. The information stored by the OEM can only be written during the manufacturing process as the Flash Descriptor read/write permissions must be set to read-only when the computer leaves the manufacturing floor. The PCH Flash controller does not read this information. FFh is suggested to reduce programming time.

## 18.4 GbE SPI Flash Program Registers

The GbE Flash registers are memory-mapped with a base address MBARB found in the GbE LAN register chapter Device 25: Function 0: Offset 14h. The individual registers are then accessible at MBARB + Offset as indicated in the following table.

These memory mapped registers must be accessed in byte, word, or DWord quantities.

**Note:** These register are only applicable when SPI flash is used in descriptor mode.

**Table 18-2. Gigabit LAN SPI Flash Program Register Address Map (GbE LAN Memory Mapped Configuration Registers)**

MBARB + Offset	Mnemonic	Register Name	Default	Attribute
00h-03h	GLFPR	Gigabit LAN Flash Primary Region	00000000h	RO
04h-05h	HSFS	Hardware Sequencing Flash Status	0000h	RO, R/WC, R/W
06h-07h	HSFC	Hardware Sequencing Flash Control	0000h	R/W, R/WS
08h-0Bh	FADDR	Flash Address	00000000h	R/W
0Ch-0Fh	—	Reserved	00000000h	—
10h-13h	FDATA0	Flash Data 0	00000000h	R/W
14h-4Fh	—	Reserved	00000000h	—
50h-53h	FRAP	Flash Region Access Permissions	00000000h	RO, R/W
54h-57h	FREG0	Flash Region 0	00000000h	RO
58h-5Bh	FREG1	Flash Region 1	00000000h	RO
5Ch-5F	FREG2	Flash Region 2	00000000h	RO
60h-63h	FREG3	Flash Region 3	00000000h	RO
64h-73h	—	Reserved for Future Flash Regions	—	—
74h-77h	PRO	Flash Protected Range 0	00000000h	R/W
78h-7Bh	PR1	Flash Protected Range 1	00000000h	R/W
7Ch-8Fh	—	Reserved	—	—
90h	SSFS	Software Sequencing Flash Status	00h	RO, R/WC
91h-93h	SSFC	Software Sequencing Flash Control	000000h	R/W
94h-95h	PREOP	Prefix Opcode Configuration	0000h	R/W
96h-97h	OPTYPE	Opcode Type Configuration	0000h	R/W
98h-9Fh	OPMENU	Opcode Menu Configuration	0000000000000000h	R/W
A0h-DFh	—	Reserved	—	—

### 18.4.1 GLFPR—Gigabit LAN Flash Primary Region Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 00h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:29	Reserved
28:16	<b>GbE Flash Primary Region Limit (PRL)</b> —RO. This specifies address bits 24:12 for the Primary Region Limit. The value in this register loaded from the contents in the Flash Descriptor.FLREG3.Region Limit
15:13	Reserved
12:0	<b>GbE Flash Primary Region Base (PRB)</b> —RO. This specifies address bits 24:12 for the Primary Region Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base

### 18.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 04h      Attribute: RO, R/W/C, R/W  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15	<b>Flash Configuration Lock-Down (FLOCKDN)</b> —R/W. When set to 1, those Flash Program Registers that are locked down by this FLOCKDN bit cannot be written. Once set to 1, this bit can only be cleared by a hardware reset due to a global reset or host partition reset in an Intel® ME enabled system.
14	<b>Flash Descriptor Valid (FDV)</b> —RO. This bit is set to a 1 if the Flash Controller reads the correct Flash Descriptor Signature. If the Flash Descriptor Valid bit is not 1, software cannot use the Hardware Sequencing registers, but must use the software sequencing registers. Any attempt to use the Hardware Sequencing registers will result in the FCERR bit being set.
13	<b>Flash Descriptor Override Pin Strap Status (FDOPSS)</b> —RO. This bit indicates the condition of the Flash Descriptor Security Override/Intel® ME Debug Mode pin strap. 0 = The Flash Descriptor Security Override/Intel® ME Debug Mode strap is set using external pull-up on HDA_SDO 1 = No override
12:6	Reserved
5	<b>SPI Cycle In Progress (SCIP)</b> —RO. Hardware sets this bit when software sets the Flash Cycle Go (FGO) bit in the Hardware Sequencing Flash Control register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.
4:3	<b>Block/Sector Erase Size (BERASE)</b> —RO. This field identifies the erasable sector size for all Flash components. 00 = 256 Byte 01 = 4KB 10 = 8KB 11 = 64KB If the Flash Linear Address is less than FPBA, then this field reflects the value in the LVSCL.BES register. If the Flash Linear Address is greater or equal to FPBA, then this field reflects the value in the UVSCC.UBES register.

Bit	Description
2	<b>Access Error Log (AEL)</b> —R/W/C. Hardware sets this bit to a 1 when an attempt was made to access the BIOS region using the direct access method or an access to the BIOS Program registers that violated the security restrictions. This bit is simply a log of an access security violation. This bit is cleared by software writing a 1.
1	<b>Flash Cycle Error (FCERR)</b> —R/W/C. Hardware sets this bit to 1 when a program register access is blocked to the FLASH due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or until hardware reset occurs due to a global reset or host partition reset in an Intel® ME enabled system. Software must clear this bit before setting the FLASH Cycle GO bit in this register.
0	<b>Flash Cycle Done (FDONE)</b> —R/W/C. The PCH sets this bit to 1 when the SPI Cycle completes after software previously set the FGO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.

### 18.4.3 HSFC—Hardware Sequencing Flash Control Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 06h      Attribute: R/W, R/W/S  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:10	Reserved
9:8	<b>Flash Data Byte Count (FDBC)</b> —R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The contents of this register are 0s based on 0b representing 1 byte and 11b representing 4 bytes. The number of bytes transferred is the value of this field plus 1. This field is ignored for the Block Erase command.
7:3	Reserved
2:1	<b>FLASH Cycle (FCYCLE)</b> —R/W. This field defines the Flash SPI cycle type generated to the FLASH when the FGO bit is set as defined below: 00 = Read (1 up to 4 bytes by setting FDBC) 01 = Reserved 10 = Write (1 up to 4 bytes by setting FDBC) 11 = Block Erase
0	<b>Flash Cycle Go (FGO)</b> —R/W/S. A write to this register with a 1 in this bit initiates a request to the Flash SPI Arbiter to start a cycle. This register is cleared by hardware when the cycle is granted by the SPI arbiter to run the cycle on the SPI bus. When the cycle is complete, the FDONE bit is set. Software is forbidden to write to any register in the HSFLCTL register between the FGO bit getting set and the FDONE bit being cleared. Any attempt to violate this rule will be ignored by hardware. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write. This bit always returns 0 on reads.

#### 18.4.4 FADDR—Flash Address Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 08h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:25	Reserved
24:0	<b>Flash Linear Address (FLA)</b> —R/W. FLA is the starting byte linear address of a SPI Read or Write cycle or an address within a Block for the Block Erase command. The Flash Linear Address must fall within a region for which BIOS has access permissions.

#### 18.4.5 FDATA0—Flash Data 0 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 10h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Flash Data 0 (FDO)</b> —R/W. This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, and so on. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-...8-23-22-...16-31...24. Bit 24 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. The data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

#### 18.4.6 FRAP—Flash Regions Access Permissions Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 50h      Attribute: RO, R/W  
Default Value: 00000808h      Size: 32 bits

Bit	Description
31:28	Reserved
27:25	<b>GbE Master Write Access Grant (GMWAG)</b> —R/W. Each bit 27:25 corresponds to Master[3:1]. GbE can grant one or more masters write access to the GbE region 3 overriding the permissions in the Flash Descriptor. Master[1] is Host Processor/BIOS, Master[2] is Intel® Management Engine, Master[3] is Host processor/GbE. The content of this register field is locked by the FLOCKDN bit.
24:20	Reserved
19:17	<b>GbE Master Read Access Grant (GMRAG)</b> —R/W. Each bit 19:17 corresponds to Master[3:1]. GbE can grant one or more masters read access to the GbE region 3 overriding the read permissions in the Flash Descriptor. Master[1] is Host processor/BIOS, Master[2] is Intel® Management Engine, Master[3] is GbE. The content of this register field is locked by the FLOCKDN bit
16:12	Reserved
11:8	<b>GbE Region Write Access (GRWA)</b> —RO. Each bit 11:8 corresponds to Regions 3:0. If the bit is set, this master can erase and write that particular region through register accesses.
7:4	Reserved
3:0	<b>GbE Region Read Access (GRRA)</b> —RO. Each bit 3:0 corresponds to Regions 3:0. If the bit is set, this master can read that particular region through register accesses.

#### 18.4.7 FREG0—Flash Region 0 (Flash Descriptor) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 54h      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This specifies address bits 24:12 for the Region 0 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)</b> —RO. This specifies address bits 24:12 for the Region 0 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG0.Region Base.

#### 18.4.8 FREG1—Flash Region 1 (BIOS Descriptor) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 58h      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This specifies address bits 24:12 for the Region 1 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)</b> —RO. This specifies address bits 24:12 for the Region 1 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG1.Region Base.

#### 18.4.9 FREG2—Flash Region 2 (Intel® ME) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 5Ch      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This specifies address bits 24:12 for the Region 2 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)</b> —RO. This specifies address bits 24:12 for the Region 2 Base The value in this register is loaded from the contents in the Flash Descriptor.FLREG2.Region Base.

### 18.4.10 FREG3—Flash Region 3 (GbE) Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 60h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:29	Reserved
28:16	<b>Region Limit (RL)</b> —RO. This specifies address bits 24:12 for the Region 3 Limit. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Limit.
15:13	Reserved
12:0	<b>Region Base (RB)</b> —RO. This specifies address bits 24:12 for the Region 3 Base. The value in this register is loaded from the contents in the Flash Descriptor.FLREG3.Region Base.

### 18.4.11 PR0—Protected Range 0 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 74h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

**Note:** This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	<b>Write Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	<b>Protected Range Limit</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	<b>Read Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	<b>Protected Range Base</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

### 18.4.12 PR1—Protected Range 1 Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 78h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

**Note:** This register can not be written when the FLOCKDN bit is set to 1.

Bit	Description
31	<b>Write Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that writes and erases directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:29	Reserved
28:16	<b>Protected Range Limit</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
15	<b>Read Protection Enable</b> —R/W. When set, this bit indicates that the Base and Limit fields in this register are valid and that read directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
14:13	Reserved
12:0	<b>Protected Range Base</b> —R/W. This field corresponds to FLA address bits 24:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

### 18.4.13 SSFS—Software Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 90h      Attribute: RO, R/WC  
Default Value: 00h      Size: 8 bits

**Note:** The Software Sequencing Control and Status registers are reserved if the Hardware Sequencing Control and Status registers are used.

Bit	Description
7:5	Reserved
4	<b>Access Error Log (AEL)</b> —RO. This bit reflects the value of the Hardware Sequencing Status AEL register.
3	<b>Flash Cycle Error (FCERR)</b> —R/WC. Hardware sets this bit to 1 when a programmed access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system.
2	<b>Cycle Done Status</b> —R/WC. The PCH sets this bit to 1 when the SPI Cycle completes (that is, SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset due to a global reset or host partition reset in an Intel® ME enabled system. When this bit is set and the SPI SMI# Enable bit is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access.
1	Reserved
0	<b>SPI Cycle In Progress (SCIP)</b> —RO. Hardware sets this bit when software sets the SPI Cycle Go bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0.

### 18.4.14 SSFC—Software Sequencing Flash Control Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 91h      Attribute: R/W  
 Default Value: 000000h      Size: 24 bits

Bit	Description
23:19	Reserved
18:16	<b>SPI Cycle Frequency (SCF)</b> —R/W. This register sets the frequency to use for all SPI software sequencing cycles (write, erase, fast read, read status, and so on), except for the read cycle which always run at 20 MHz. 000 = 20 MHz 001 = 33 MHz 100 = 50 MHz All other values = Reserved. This register field is locked when the SPI Configuration Lock-Down bit is set.
15	Reserved
14	<b>Data Cycle (DS)</b> —R/W. When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are don't cares.
13:8	<b>Data Byte Count (DBC)</b> —R/W. This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 3. The number of bytes transferred is the value of this field plus 1. When this field is 00b, there is 1 byte to transfer and that 11b means there are 4 bytes to transfer.
7	Reserved
6:4	<b>Cycle Opcode Pointer (COP)</b> —R/W. This field selects one of the programmed opcodes in the Opcode Menu to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	<b>Sequence Prefix Opcode Pointer (SPOP)</b> —R/W. This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Prefix Opcodes register. By making this programmable, the PCH supports flash devices that have different opcodes for enabling writes to the data space versus status register.
2	<b>Atomic Cycle Sequence (ACS)</b> —R/W. When set to 1 along with the SCGO assertion, the PCH will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles. The sequence is composed of: <ul style="list-style-type: none"> <li>• Atomic Sequence Prefix Command (8-bit opcode only)</li> <li>• Primary Command specified below by software (can include address and data)</li> <li>• Polling the Flash Status Register (opcode 05h) until bit 0 becomes 0b.</li> </ul> The SPI Cycle in Progress bit remains set and the Cycle Done Status bit remains unset until the Busy bit in the Flash Status Register returns 0.
1	Reserved
0	Reserved

### 18.4.15 PREOP—Prefix Opcode Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 94h      Attribute: R/W  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:8	<b>Prefix Opcode 1</b> —R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	<b>Prefix Opcode 0</b> —R/W. Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

**Note:** This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

### 18.4.16 OPTYPE—Opcode Type Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 96h      Attribute: R/W  
Default Value: 0000h      Size: 16 bits

Entries in this register correspond to the entries in the Opcode Menu Configuration register.

**Note:** The definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address should be avoided (for example, “Chip Erase” and “Auto-Address Increment Byte Program”).

Bit	Description
15:14	<b>Opcode Type 7</b> —R/W. See the description for bits 1:0
13:12	<b>Opcode Type 6</b> —R/W. See the description for bits 1:0
11:10	<b>Opcode Type 5</b> —R/W. See the description for bits 1:0
9:8	<b>Opcode Type 4</b> —R/W. See the description for bits 1:0
7:6	<b>Opcode Type 3</b> —R/W. See the description for bits 1:0
5:4	<b>Opcode Type 2</b> —R/W. See the description for bits 1:0
3:2	<b>Opcode Type 1</b> —R/W. See the description for bits 1:0
1:0	<b>Opcode Type 0</b> —R/W. This field specifies information about the corresponding Opcode 0. This information allows the hardware to 1) know whether to use the address field and 2) provide BIOS and Shared Flash protection capabilities. The encoding of the two bits is: 00 = No address associated with this Opcode; Read cycle type 01 = No address associated with this Opcode; Write cycle type 10 = Address required; Read cycle type 11 = Address required; Write cycle type

**Note:** This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

### 18.4.17 OPMENU—Opcode Menu Configuration Register (GbE LAN Memory Mapped Configuration Registers)

Memory Address: MBARB + 98h      Attribute: R/W  
 Default Value: 0000000000000000h      Size: 64 bits

Eight entries are available in this register to give GbE a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

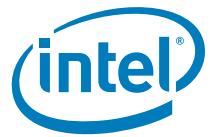
**Note:**

It is recommended that GbE avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. This could cause functional failures in a shared flash environment. Write Enable opcodes should only be programmed in the Prefix Opcodes.

Bit	Description
63:56	<b>Allowable Opcode 7</b> —R/W. See the description for bits 7:0
55:48	<b>Allowable Opcode 6</b> —R/W. See the description for bits 7:0
47:40	<b>Allowable Opcode 5</b> —R/W. See the description for bits 7:0
39:32	<b>Allowable Opcode 4</b> —R/W. See the description for bits 7:0
31:24	<b>Allowable Opcode 3</b> —R/W. See the description for bits 7:0
23:16	<b>Allowable Opcode 2</b> —R/W. See the description for bits 7:0
15:8	<b>Allowable Opcode 1</b> —R/W. See the description for bits 7:0
7:0	<b>Allowable Opcode 0</b> —R/W. Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

This register is not writable when the SPI Configuration Lock-Down bit (MBARB + 00h:15) is set.

§ §



***Serial Peripheral Interface (SPI)***

# 19 Thermal Sensor Registers (D31:F6)

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## 19.1 PCI Space Configuration Registers

Table 19-1. Thermal Sensor Register Address Map

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	8086h	RO
02h-03h	DID	Device Identification	3A32h	RO
04h-05h	CMD	Command Register	0000h	R/W, RO
06h-07h	STS	Device Status	0010h	R/WC, RO
08h	RID	Revision ID	00h	RO
09h	PI	Programming Interface	00h	RO
0Ah	SCC	Sub Class Code	80h	RO
0Bh	BCC	Base Class Code	11h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	LT	Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
10h-13h	TBAR	Thermal Base Address	00000004h	R/W, RO
14h-17h	TBARTH	Thermal Base Address High DWord	00000000h	RO
2Ch-2Dh	SVID	Subsystem Vendor Identifier	0000h	R/WO
2Eh-2Fh	SID	Subsystem Identifier	0000h	R/WO
34h	CAP_PTR	Capabilities Pointer	50h	RO
3Ch	INTLN	Interrupt Line	00h	R/W
3Dh	INTPN	Interrupt Pin	See Description	RO
40h-43h	TBARB	BIOS Assigned Thermal Base Address	00000004h	R/W, RO
44h-47h	TBARBH	BIOS Assigned Thermal Base High DWord	00000000h	R/W
50h-51h	PID	PCI Power Management Capability ID	0001h	RO
52h-53h	PC	Power Management Capabilities	0023h	RO
54h-57h	PCS	Power Management Control and Status	0000h	R/W, RO

### 19.1.1 VID—Vendor Identification Register

Offset Address:	00h–01h	Attribute:	RO
Default Value:	8086h	Size:	16 bits
Lockable:	No	Power Well:	Core

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h

### 19.1.2 DID—Device Identification Register

Offset Address:	02h–03h	Attribute:	RO
Default Value:	3A32h	Size:	16 bits

Bit	Description
15:0	<b>Device ID (DID)</b> —RO. Indicates the device number assigned by the SIG.

### 19.1.3 CMD—Command Register

Address Offset:	04h–05h	Attribute:	RO, R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable (ID)</b> —R/W. Enables the device to assert an INTx#. 0 = When cleared, the INTx# signal may be asserted. 1 = When set, the Thermal logic's INTx# signal will be de-asserted.
9	<b>FBE (Fast Back to Back Enable)</b> —RO. Hardwired to 0.
8	<b>SEN (SERR Enable)</b> —RO. Hardwired to 0.
7	<b>WCC (Wait Cycle Control)</b> —RO. Hardwired to 0.
6	<b>PER (Parity Error Response)</b> —RO. Hardwired to 0.
5	<b>VPS (VGA Palette Snoop)</b> —RO. Hardwired to 0.
4	<b>MWI (Memory Write and Invalidate Enable)</b> —RO. Hardwired to 0.
3	<b>SCE (Special Cycle Enable)</b> —RO. Hardwired to 0.
2	<b>BME (Bus Master Enable)</b> —R/W. 0 = Function disabled as bus master. 1 = Function enabled as bus master.
1	<b>Memory Space Enable (MSE)</b> —R/W. 0 = Disable 1 = Enable. Enables memory space accesses to the Thermal registers.
0	<b>IOS (I/O Space)</b> —RO. The Thermal logic does not implement I/O Space; therefore, this bit is hardwired to 0.

### 19.1.4 STS—Status Register

Address Offset: 06h–07h      Attribute: R/WC, RO  
 Default Value: 0010h      Size: 16 bits

Bit	Description
15	<b>Detected Parity Error (DPE)</b> —R/WC. This bit is set whenever a parity error is seen on the internal interface for this function, regardless of the setting of bit 6 in the Command register. Software clears this bit by writing a 1 to this bit location.
14	<b>SERR# Status (SERRS)</b> —RO. Hardwired to 0.
13	<b>Received Master Abort (RMA)</b> —RO. Hardwired to 0.
12	<b>Received Target Abort (RTA)</b> —RO. Hardwired to 0.
11	<b>Signaled Target-Abort (STA)</b> —RO. Hardwired to 0.
10:9	<b>DEVSEL# Timing Status (DEVT)</b> —RO. Hardwired to 0.
8	<b>Master Data Parity Error (MDPE)</b> —RO. Hardwired to 0.
7	<b>Fast Back to Back Capable (FBC)</b> —RO. Hardwired to 0.
6	Reserved
5	<b>66 MHz Capable (C66)</b> —RO. Hardwired to 0.
4	<b>Capabilities List Exists (CLIST)</b> —RO. Indicates that the controller contains a capabilities pointer list. The first item is pointed to by looking at configuration offset 34h.
3	<b>Interrupt Status (IS)</b> —RO. Reflects the state of the INTx# signal at the input of the enable/disable circuit. This bit is a 1 when the INTx# is asserted. This bit is a 0 after the interrupt is cleared (independent of the state of the Interrupt Disable bit in the command register).
2:0	Reserved

### 19.1.5 RID—Revision Identification Register

Address Offset: 08h      Attribute: RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Revision ID (RID)</b> —RO. Indicates the device specific revision identifier.

### 19.1.6 PI—Programming Interface Register

Address Offset: 09h      Attribute: RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Programming Interface (PI)</b> —RO. The PCH Thermal logic has no standard programming interface.

### 19.1.7 SCC—Sub Class Code Register

Address Offset: 0Ah Attribute: RO  
 Default Value: 80h Size: 8 bits

Bit	Description
7:0	<b>Sub Class Code (SCC)</b> —RO. Value assigned to the PCH Thermal logic.

### 19.1.8 BCC—Base Class Code Register

Address Offset: 0Bh Attribute: RO  
 Default Value: 11h Size: 8 bits

Bit	Description
7:0	<b>Base Class Code (BCC)</b> —RO. Value assigned to the PCH Thermal logic.

### 19.1.9 CLS—Cache Line Size Register

Address Offset: 0Ch Attribute: RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Cache Line Size (CLS)</b> —RO. Does not apply to PCI Bus Target-only devices.

### 19.1.10 LT—Latency Timer Register

Address Offset: 0Dh Attribute: RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Latency Timer (LT)</b> —RO. Does not apply to PCI Bus Target-only devices.

### 19.1.11 HTYPE—Header Type Register

Address Offset: 0Eh Attribute: RO  
 Default Value: 00h Size: 8 bits

Bit	Description
7	<b>Multi-Function Device (MFD)</b> —RO. This bit is 0 because a multi-function device only needs to be marked as such in Function 0, and the Thermal registers are not in Function 0.
6:0	<b>Header Type (HTYPE)</b> —RO. Implements Type 0 Configuration header.

### 19.1.12 TBAR—Thermal Base Register

Address Offset: 10h–13h      Attribute: R/W, RO  
 Default Value: 00000004h      Size: 32 bits

This BAR creates 4KB of memory space to signify the base address of Thermal memory mapped configuration registers. This memory space is active when the Command (CMD) register Memory Space Enable (MSE) bit is set and either TBAR[31:12] or TBARH are programmed to a non-zero address. This BAR is owned by the operating system, and allows the operating system to locate the Thermal registers in system memory space.

Bit	Description
31:12	<b>Thermal Base Address (TBA)</b> —R/W. This field provides the base address for the Thermal logic memory-mapped configuration registers. 4KB are requested by hardwiring bits 11:4 to 0s.
11:4	Reserved
3	<b>Prefetchable (PREF)</b> —RO. Indicates that this BAR is NOT prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO. Indicates that this BAR can be located anywhere in 64-bit address space.
0	<b>Space Type (SPTYP)</b> —RO. Indicates that this BAR is located in memory space.

### 19.1.13 TBARH—Thermal Base High DWord Register

Address Offset: 14h–17h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

This BAR extension holds the high 32 bits of the 64-bit TBAR. In conjunction with TBAR, it creates 4KB of memory space to signify the base address of Thermal memory-mapped configuration registers.

Bit	Description
31:0	<b>Thermal Base Address High (TBAH)</b> —R/W. TBAR bits 63:32.

### 19.1.14 SVID—Subsystem Vendor ID Register

Address Offset: 2Ch–2Dh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

This register should be implemented for any function that could be instantiated more than once in a given system. The SVID register, in combination with the Subsystem ID register, enables the operating environment to distinguish one subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SID to create one 32-bit write. This register is not affected by D3HOT to D0 reset.

Bit	Description
15:0	<b>SVID (SVID)</b> —R/WO. These R/WO bits have no PCH functionality.

### 19.1.15 SID—Subsystem ID Register

Address Offset: 2Eh–2Fh	Attribute: R/WO
Default Value: 0000h	Size: 16 bits

This register should be implemented for any function that could be instantiated more than once in a given system. The SID register, in combination with the Subsystem Vendor ID register make it possible for the operating environment to distinguish one subsystem from the other(s).

Software (BIOS) will write the value to this register. After that, the value can be read, but writes to the register will have no effect. The write to this register should be combined with the write to the SVID to create one 32-bit write. This register is not affected by D3<sub>HOT</sub> to D0 reset.

Bit	Description
15:0	<b>SID (SAID)</b> —R/WO. These R/WO bits have no PCH functionality.

### 19.1.16 CAP\_PTR—Capabilities Pointer Register

Address Offset: 34h	Attribute: RO
Default Value: 50h	Size: 8 bits

Bit	Description
7:0	<b>Capability Pointer (CP)</b> —RO. Indicates that the first capability pointer offset is offset 50h (Power Management Capability).

### 19.1.17 INTLN—Interrupt Line Register

Address Offset: 3Ch	Attribute: R/W
Default Value: 00h	Size: 8 bits

Bit	Description
7:0	<b>Interrupt Line</b> —R/W. PCH hardware does not use this field directly. It is used to communicate to software the interrupt line that the interrupt pin is connected to.

### 19.1.18 INTPN—Interrupt Pin Register

Address Offset: 3Dh	Attribute: RO
Default Value: See description	Size: 8 bits

Bit	Description
7:4	Reserved
3:0	<b>Interrupt Pin</b> —RO. This field reflects the value of the Device 31 interrupt pin bits 27:24 (TTIP) in Chipset configuration space.

### 19.1.19 TBARB—BIOS Assigned Thermal Base Address Register

Address Offset: 40h–43h Attribute: R/W, RO  
 Default Value: 00000004h Size: 32 bits

This BAR creates 4KB of memory space to signify the base address of Thermal memory-mapped configuration registers. This memory space is active when TBARB.SPTYPEN is asserted. This BAR is owned by the BIOS, and allows the BIOS to locate the Thermal registers in system memory space. If both TBAR and TBARB are programmed, then the operating system and BIOS each have their own independent “view” of the Thermal registers, and must use the TSIU register to denote Thermal registers ownership/availability.

Bit	Description
31:12	<b>Thermal Base Address (TBA)</b> —R/W. This field provides the base address for the Thermal logic memory mapped configuration registers. 4KB are requested by hardwiring bits 11:4 to 0s.
11:4	Reserved
3	<b>Prefetchable (PREF)</b> —RO. Indicates that this BAR is NOT prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO. Indicates that this BAR can be located anywhere in 64-bit address space.
0	<b>Space Type Enable (SPTYPEN)</b> —R/W. 0 = Disable. 1 = Enable. When set to 1b by software, enables the decode of this memory BAR.

### 19.1.20 TBARBH—BIOS Assigned Thermal Base High DWord Register

Address Offset: 44h–47h Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

This BAR extension holds the high 32- bits of the 64-bit TBARB.

Bit	Description
31:0	<b>Thermal Base Address High (TBAH)</b> —R/W. TBAR bits 61:32.

### 19.1.21 PID—PCI Power Management Capability ID Register

Address Offset: 50h–51h Attribute: RO  
 Default Value: 0001h Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —RO. Indicates that this is the last capability structure in the list.
7:0	<b>Cap ID (CAP)</b> —RO. Indicates that this pointer is a PCI power management capability

### 19.1.22 PC—Power Management Capabilities Register

Address Offset: 52h–53h  
 Default Value: 0023h

Attribute: RO  
 Size: 16 bits

Bit	Description
15:11	<b>PME_Support</b> —RO. Indicates PME# is not supported
10	<b>D2_Support</b> —RO. The D2 state is not supported.
9	<b>D1_Support</b> —RO. The D1 state is not supported.
8:6	<b>Aux_Current</b> —RO. PME# from D3 <sub>COLD</sub> state is not supported, therefore this field is 000b.
5	<b>Device Specific Initialization (DSI)</b> —RO. Indicates that device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PMEC)</b> —RO. Does not apply. Hardwired to 0.
2:0	<b>Version (VS)</b> —RO. Indicates support for Revision 1.2 of the <i>PCI Power Management Specification</i> .

### 19.1.23 PCS—Power Management Control And Status Register

Address Offset: 54h–57h  
 Default Value: 0008h

Attribute: R/W, RO  
 Size: 32 bits

Bit	Description
31:24	<b>Data</b> —RO. Does not apply. Hardwired to 0s.
23	<b>Bus Power/Clock Control Enable (BPCCE)</b> —RO. Hardwired to 0.
22	<b>B2/B3 Support (B23)</b> —RO. Does not apply. Hardwired to 0.
21:16	Reserved
15	<b>PME Status (PMES)</b> —RO. This bit is always 0, since this PCI Function does not generate PME#.
14:9	<b>Reserved</b>
8	<b>PME Enable (PMEE)</b> —RO. This bit is always zero, since this PCI Function does not generate PME#.
7:4	Reserved
3	<b>No Soft Reset</b> —RO. When set to 1, this bit indicates that devices transitioning from D3 <sub>HOT</sub> to D0 because of PowerState commands do not perform an internal reset. Configuration context is preserved. Upon transition from D3 <sub>HOT</sub> to D0 initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	Reserved
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the Thermal controller and to set a new power state. The values are: 00 = D0 state 11 = D3 <sub>HOT</sub> state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in the D3 <sub>HOT</sub> states, the Thermal controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. When software changes this value from the D3 <sub>HOT</sub> state to the D0 state, no internal warm (soft) reset is generated.

## 19.2 Thermal Memory Mapped Configuration Registers (Thermal Sensor—D31:F26)

The base memory for these thermal memory mapped configuration registers is specified in the TBARB (D31:F6:Offset 40h). The individual registers are then accessible at TBARB + Offset.

All registers are located in Core well.

**Table 19-2. Thermal Memory Mapped Configuration Register Address Map**

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	TEMP	Temperature	0000h	RO
04h	TSC	Thermal Sensor Control	00h	RO, R/W
06h	TSS	Thermal Sensor Status	00h	RO, R/W, R/RC
08h	TSEL	Thermal Sensor Enable and Lock	00h	RO, R/W
0Ah	TSREL	Thermal Sensor Report Enable and Lock	00h	RO, R/W
0Ch	TSMIC	Thermal Sensor SMI Control	00h	RO, R/W
10h-11h	CTT	Catastrophic Trip Point	01FFh	RO, R/W
14h-15h	TAHV	Thermal Alert High Value	0000h	RO, R/W
18h-19h	TALV	Thermal Alert Low Value	0000h	RO, R/W
1Ch-1Dh	TSPM	Thermal Sensor Power Management	0400h	RO, R/W
40h-43h	TL	Throttle Levels	00000000h	RO, R/W
60h-61h	PHL	PCH Hot Level	0000h	RO, R/W
62h	PHLC	PHL Control	00h	RO, R/W
80h	TAS	Thermal Alert Status	00h	RO, R/W, R/RC
82h	TSPIEN	PCI Interrupt Event Enables	00h	RO, R/W
84h	TSGPEN	General Purpose Event Enables	00h	RO, R/W

### 19.2.1 TEMP—Temperature Register

Offset Address: TBARB+00h      Attribute: RO  
 Default Value: 00h      Size: 16 bits

Bit	Description
15:9	Reserved
8:0	<b>TS Reading (TSR)</b> —RO. The die temperature with resolution of 1/2 °C and an offset of -50 °C. To calculate the die temperature, convert the raw 9-bit value to decimal, divide by two and subtract 50. For example, if the value read is 0x121, then the temperature is calculated as $(289/2) - 50$ which results in 94.5 °C.

### 19.2.2 TSC—Thermal Sensor Control Register

Offset Address: TBARB+04h      Attribute: R/W  
 Default Value: 00h      Size: 8 bit

This register controls the operation of the thermal sensor.

Bit	Description
7	<b>Policy Lock-Down Bit</b> —R/W. When written to 1, this bit prevents any more writes to the register (offset 04h) and to CTT (offset 10h)
6:1	Reserved
0	<b>Catastrophic Power-Down Enable</b> —R/W. When set to 1, the power management logic (PMC) transitions to the S5 state when a catastrophic temperature is detected by the sensor. The transition to the S5 state must be unconditional (like the Power Button Override Function).  <b>Note:</b> The thermal sensor and response logic is in the core/main power well; therefore, detection of a catastrophic temperature is limited to times when this well is powered and out of reset.

### 19.2.3 TSS—Thermal Sensor Status Register

Offset Address: TBARB+06h      Attribute: RO, R/WC  
 Default Value: 00h      Size: 8 bit

This register provides statuses of the thermal sensor.

Bit	Description
7:5	Reserved
4	<b>Thermal Sensor Dynamic Shutdown Status (TSDSS)</b> —RO. This bit indicates the status of the thermal sensor circuit when TSEL.ETS=1. 1 = thermal sensor is fully operational 0 = thermal sensor is in a dynamic shutdown state
3	<b>GPE Status (GPES)</b> —R/WC. Set when GPE is enabled for a trip event. Software must write a '1' to this bit to clear the GPE status. GPE can be configured to cause an SMI or SCI. As long as this bit is set, the GPE indication to the global GPE logic is asserted.
2	<b>SMI Status (SMIS)</b> —R/WC. Set when SMI is enabled for a trip event. Software must write a '1' to this bit to clear the SMI status. As long as this bit is set, the SMI indication to the global SMI logic is asserted.
1:0	Reserved

## 19.2.4 TSEL—Thermal Sensor Enable and Lock Register

Offset Address: TBARB+08h Attribute: RO, R/W  
 Default Value: 00h Size: 8 bit

This register controls the operation of the thermal sensor.

Bit	Description
7	<b>Policy Lock-Down Bit</b> —R/W. When written to 1, this bit prevents any more writes to this register.
6:1	Reserved
0	<b>Enable TS (ETS)</b> —R/W. 1 = Enables the thermal sensor. Until this bit is set, no thermometer readings or trip events will occur. If software reads the TEMP register before the sensor is enabled, it will read 0x0. The value of this bit is sent to the thermal sensor. <b>Note:</b> if the sensor is running and valid temperatures have been captured in TEMP and then ETS is cleared, TEMP will retain its old value. Clearing ETS does not force TEMP to 0x0. 0 = Disables the sensor.

## 19.2.5 TSREL—Thermal Sensor Reporting Enable and Lock Register

Offset Address: TBARB+0Ah Attribute: R/W  
 Default Value: 00h Size: 8 bit

Bit	Description
7	<b>Policy Lock-Down Bit</b> —R/W. When written to 1, this bit prevents anymore writes to this register.
6:1	Reserved
0	<b>Enable SMBus Temperature Reporting</b> —R/W. 1 = Enables the reporting of the PCH temperature to the SMBus and PMC. This must also be set if Intel® ME needs access to the PCH temperature. Once enabled, this bit should not be cleared by software. If it is cleared, then the EC may get an undefined value. Software has no need to dynamically disable and then re-enable this bit. 0 = Disables temperature reporting.

## 19.2.6 TSMIC—Thermal Sensor SMI Control Register

Offset Address:	TBARB+0Ch	Attribute:	R/W
Default Value:	00h	Size:	8 bit

Bit	Description
7	<b>Policy Lock-Down Bit</b> —R/W. When written to 1, this bit prevents more writes to this register.
6:1	Reserved
0	<b>SMI Enable on Alert Thermal Sensor Trip</b> —R/W. 1 = Enables SMI# assertions on alert thermal sensor events for either low-to-high or high-to-low events. Both edges are enabled by this one bit. 0 = Disables SMI# assertions for alert thermal events.

## 19.2.7 CTT—Catastrophic Trip Point Register

Offset Address:	TBARB+10h	Attribute:	R/W
Default Value:	01FFh	Size:	16 bits

Bit	Description
15:9	Reserved
8:0	<b>Catastrophic Temperature TRIP (CTRIP)</b> —R/W. When the current temperature reading is greater than or equal to the value in this register, a catastrophic trip event is signaled. This register field is locked by TSC[7].

## 19.2.8 TAHV—Thermal Alert High Value Register

Offset Address:	TBARB+14h	Attribute:	R/W
Default Value:	0000h	Size:	16 bits

Bit	Description
15:9	Reserved
8:0	<b>Alert High (AH)</b> —R/W. Sets the high value for the alert indication. See the later section for usage. <b>Note:</b> It is invalid for software to program AH to a value less than TALV.AL. This register is not lockable, so that software can change the values during runtime.

### 19.2.9 TALV—Thermal Alert Low Value Register

Offset Address: TBARB+18h      Attribute: R/W  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:9	Reserved
8:0	<b>Alert Low (AL)</b> —R/W. Sets the low value for the alert indication. See the later section for usage. This register is not lockable, so that software can change the values during runtime.

### 19.2.10 TSPM—Thermal Sensor Power Management Register

Offset Address: TBARB+1Ch      Attribute: R/W  
 Default Value: 0400h      Size: 16 bits

Bit	Description
15	<b>Thermal Sensor Power Management Lock (TSPMLOCK)</b> —R/W. Setting this bit to a 1 causes bits 15:9 in this register to be locked.
14	<b>Dynamic Thermal Sensor Shutdown in S0 idle Enable (DTSSSOEN)</b> —R/W 1 = Dynamic thermal sensor shutdown in S0 idle is enabled. When set to 1, the power management logic shuts down the thermal sensor when the TEMP.TSR $\leq$ TSPM.LTT and the system is idle as indicated by processor C-State if TSPM.DTSSICO = 0. When the sensor is disabled, the last value of TEMP.TSR is preserved. Upon re-enabling, the TEMP.TSR will be updated with the latest temperature as reported by the sensor. 0 = Dynamic thermal sensor shutdown in S0 idle is disabled
13	<b>Dynamic Thermal Sensor Shutdown in C0 Allowed (DTSSICO)</b> —R/W. 0 = Processor must be in a non-C0 state to allow PCH thermal sensor shutdown 1 = Processor can be in a C0 or non-C0 state to allow PCH thermal sensor shutdown.
12	Reserved
11:9	<b>Maximum Thermal Sensor Shutdown Time (MAXSST)</b> —R/W. Sets the maximum time that the thermal sensor will be held in a shutdown state assuming no other wake conditions. This register field is used to set the expiration time of a timer that is used to wake up the thermal sensor on expiration. 000 = 1 s 001 = 2 s 010 = 4 s 011 = 8 s 100 = 16 s 101-111 = Reserved
8:0	<b>Low Temp Threshold (LTT)</b> —R/W. Sets the low maximum temp value used for dynamic thermal sensor shutdown consideration. See DTSSSOEN for details. This register field is not lockable, so that software can change the values during runtime.

### 19.2.11 TL—Throttle Levels Register

Offset Address: TBARB+40h  
 Default Value: 00000000h

Attribute: R/W  
 Size: 32 bit

Bit	Description
31	<b>TT.Lock</b> —R/W. When set to '1', this entire register (TL) is locked and remains locked until the next platform reset.
30	<b>TT.State13 Enable (TT13EN)</b> —R/W. When set to '1' and the programmed GPIO pin is a 1, then PMSync state 13 will force at least T2 state.
29	<b>TT Enable (TTEN)</b> —R/W. When set the thermal throttling states are enabled. At reset, BIOS must set bits 28:0 and then do a separate write to set bit 29 to enable throttling. Software may set bit 31 at the same time it sets bit 29 if it wishes to lock the register. If software wants to change the values of 28:0, it must first clear the TTEN bit, then change the values in 28:0, and then re-enable TTEN. It is valid to set bits 31, 30, and 29 with the same write. This bit must not be set by software until software has already enabled the thermal sensor (TSEL.ETS = 1). If TTEN is written to 0, after having been enabled, then the PCH may stay in the throttling state it was in at the moment TTEN is disabled. There is no intent that the sensor be enabled for a while and then disabled and left off. It may be disabled temporarily while changing the register values, but it should not be left in the disabled state.
28:20	<b>T2 Level (T2L)</b> —R/W. When TTEN = 1 AND TSE = '1' AND (T2L $\geq$ TSR[8:0] > T1L), then the system is in T2 state. When TTEN = 1 AND TSE = '1' AND (TSR[8:0] > T2L), then the system is in T3 state. <b>Note:</b> The T3 condition overrides PMSync[13] and forces the system to T3 if both cases are true. <b>Software Note:</b> T2L must be programmed to a value greater than T1L if TTEN='1'
19	Reserved
18:10	<b>T1 Level (T1L)</b> —R/W. When TTEN = 1 AND TSE = 1 AND (T1L $\geq$ TSR[8:0] > T0L), then the system is in T1 state. <b>Software Note:</b> T1L must be programmed to a value greater than T0L if TTEN='1'
9	Reserved
8:0	<b>T0 Level (T0L)</b> —R/W. When TEMP.TSR[8:0] $\leq$ T0L OR TT.Enable is '0' OR TSE = '0', then the system is in T0 state.

### 19.2.12 TL2—Throttle Levels 2 Register

Offset Address: TBARB+50h  
 Default Value: 00000000h

Attribute: R/W  
 Size: 32 bits

Bit	Description
15	<b>TL2.Lock</b> —R/WL. When set to '1', this entire register (TL2) is locked and remains locked until the next platform reset.
14	<b>PMC Throttling Enable (PMCTEN)</b> —R/WL. When set to '1' and the PMC is requesting throttling, force at least the T-state that PMC is requesting.
13:0	Reserved

### 19.2.13 PHL—PCH Hot Level Register

Offset Address: TBARB+60h      Attribute: R/W  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15	<b>PHL Enable (PHLE)</b> —R/W. When set and the current temperature reading, TSR, is greater than PHLL, then the PCHHOT# pin will be asserted (active low).
14:9	Reserved
8:0	<b>PHL Level (PHLL)</b> —R/W. Temperature value used for PCHHOT# pin.

### 19.2.14 PHLC—PHL Control Register

Offset Address: TBARB+62h      Attribute: R/W  
 Default Value: 00h      Size: 8 bit

Bit	Description
7:1	Reserved
0	<b>PHL Lock</b> —R/W. When written to a '1', then both PHL and PHLC are locked

### 19.2.15 TAS—Thermal Alert Status Register

Offset Address: TBARB+80h      Attribute: R/W  
 Default Value: 00h      Size: 8 bit

Bit	Description
7:2	Reserved
1	<b>Alert High-to-Low Event (AHLE)</b> —R/WC. 1 = Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0 = No trip for this event Software must write a 1 to clear this status bit.
0	<b>Alert Low-to-High Event (ALHE)</b> —R/WC. 1 = Indicates that an Aux Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0 = No trip for this event Software must write a 1 to clear this status bit. <b>Note:</b> AHLE will not be set until there has been one occurrence of a Low-to-High event (ALHE must have been set once). This prevents the case where the system power up at a reasonably high temperature and starts to cool off while booting and causing an interrupt before there is software loaded to handle it.

### 19.2.16 TSPIEN—PCI Interrupt Event Enables Register

Offset Address: TBARB+82h      Attribute: R/W  
Default Value: 00h      Size: 8 bit

Bit	Description
7:2	Reserved
1	<b>Alert High-to-Low Enable</b> —R/W. When set to 1, the thermal sensor logic asserts the Thermal logic PCI INTx signal when the corresponding status bit is set in the Thermal Error Status register. When cleared, the corresponding status bit does not result in PCI INTx.
0	<b>Alert Low-to-High Enable</b> —R/W. See the description for bit 1

### 19.2.17 TSGPEN—General Purpose Event Enables Register

Offset Address: TBARB+84h      Attribute: R/W  
Default Value: 00h      Size: 8 bit

Bit	Description
7:2	Reserved
1	<b>Alert High-to-Low Enable</b> —R/W. When set to 1, the thermal sensor logic asserts its General Purpose Event signal to the GPE block when the corresponding status bit is set in the Thermal Error Status register. When cleared, the corresponding status bit does not result in the GPE signal assertion.
0	<b>Alert Low-to-High Enable</b> —R/W. See the description for bit 1.

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# 20 Intel® Management Engine (Intel® ME) Subsystem Registers (D22:F[3:0])

## 20.1 First Intel® Management Engine Interface (Intel® MEI) Configuration Registers (Intel® MEI 1—D22:F0)

### 20.1.1 PCI Configuration Registers (Intel® MEI 1—D22:F0)

**Table 20-1. Intel® MEI 1 Configuration Registers Address Map (Intel® MEI 1—D22:F0) (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	8086h	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	0010h	RO
08h	RID	Revision Identification	See register description	RO
09h-0Bh	CC	Class Code	078000h	RO
0Eh	HTYPE	Header Type	80h	RO
10h-17h	MEI0_MBAR	Intel® MEI 1 MMIO Base Address	0000000000000004h	R/W, RO
2Ch-2Dh	SVID	Subsystem Vendor ID	0000h	R/WO
2Eh-2Fh	SID	Subsystem ID	0000h	R/WO
34h	CAPP	Capabilities List Pointer	50h	RO
3Ch-3Dh	INTR	Interrupt Information	0100h	R/W, RO
40h-43h	HFSTS#1	Host Firmware Status Register #1	00000000h	RO
44h-47h	ME_UMA	Management Engine UMA Register	10000000h	RO
48h-4Bh	HFSTS#2	Host Firmware Status Register #2	00000000h	RO
4Ch-4Fh	H_GS	Host General Status	00000000h	R/W
50h-51h	PID	PCI Power Management Capability ID	8C01h	RO
52h-53h	PC	PCI Power Management Capabilities	C803h	RO
54h-55h	PMCS	PCI Power Management Control and Status	0008h	R/WC, R/W, RO
60h-63h	HFSTS#3	Host Firmware Status Register #3	00000000h	RO
64h-67h	HFSTS#4	Host Firmware Status Register #4	00000000h	RO
68h-6Bh	HFSTS#5	Host Firmware Status Register #5	00000000h	RO
6Ch-6Fh	GMES5	General Intel® ME Status 5	00000000h	RO

**Table 20-1. Intel® MEI 1 Configuration Registers Address Map (Intel® MEI 1—D22:F0) (Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
70h-73h	H_GS2	Host General Status 2	00000000h	RW
74h-77h	H_GS3	Host General Status 3	00000000h	RW
8Ch-8Dh	MID	Message Signaled Interrupt Identifiers	0005h	RO
8Eh-8Fh	MC	Message Signaled Interrupt Message Control	0080h	R/W, RO
90h-93h	MA	Message Signaled Interrupt Message Address	00000000h	R/W, RO
94h-97h	MUA	Message Signaled Interrupt Upper Address	00000000h	R/W
98h-99h	MD	Message Signaled Interrupt Message Data	0000h	R/W
A0h	HIDM	Intel MEI Interrupt Delivery Mode	00h	R/W
BCh-BFh	HERES	Intel MEI Extended Register Status	40000000h	RO
C0h-DFh	HER[1:8]	Intel MEI Extended Register DW[1:8]	00000000h	RO

#### 20.1.1.1 VID—Vendor Identification Register (Intel® MEI 1—D22:F0)

Address Offset: 00h-01h Attribute: RO  
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	<b>Vendor ID (VID)</b> —RO. This is a 16-bit value assigned to Intel.

#### 20.1.1.2 DID—Device Identification Register (Intel® MEI 1—D22:F0)

Address Offset: 02h-03h Attribute: RO  
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	<b>Device ID (DID)</b> —RO. This is a 16-bit value assigned to the Intel® Management Engine Interface controller. See <a href="#">Section 1.4</a> for the value of the DID Register.



### 20.1.1.3 PCICMD—PCI Command Register (Intel® MEI 1—D22:F0)

Address Offset: 04h–05h  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

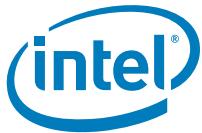
Bit	Description
15:11	Reserved
10	<b>Interrupt Disable (ID)</b> —R/W. Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9:3	Reserved
2	<b>Bus Master Enable (BME)</b> —R/W. Controls the Intel® MEI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, Intel® ME bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an Intel® ME MSI. When this bit is 0, Intel® MEI is blocked from generating MSI to the host processor.  <b>Note:</b> This bit does not block Intel® MEI accesses to Intel® ME UMA; that is, writes or reads to the host and Intel® ME circular buffers through the read window and write window registers still cause Intel® ME backbone transactions to Intel® ME UMA.
1	<b>Memory Space Enable (MSE)</b> —R/W. Controls access to the Intel® ME's memory-mapped register space. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers accepted.
0	Reserved

### 20.1.1.4 PCISTS—PCI Status Register (Intel® MEI 1—D22:F0)

Address Offset: 06h–07h  
Default Value: 0010h

Attribute: RO  
Size: 16 bits

Bit	Description
15:5	<b>Reserved</b>
4	Capabilities List (CL)—RO. Indicates the presence of a capabilities list, hardwired to 1.
3	<b>Interrupt Status (IS)</b> —RO. Indicates the interrupt status of the device. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted.
2:0	Reserved



#### 20.1.1.5 RID—Revision Identification Register (Intel® MEI 1—D22:F0)

Offset Address: 08h Attribute: RO  
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See Section 1.4 for the value of the RID Register.

#### 20.1.1.6 CC—Class Code Register (Intel® MEI 1—D22:F0)

Address Offset: 09h–0Bh Attribute: RO  
Default Value: 078000h Size: 24 bits

Bit	Description
23:16	<b>Base Class Code (BCC)</b> —RO. Indicates the base class code of the Intel® MEI device.
15:8	<b>Sub Class Code (SCC)</b> —RO. Indicates the sub class code of the Intel® MEI device.
7:0	<b>Programming Interface (PI)</b> —RO. Indicates the programming interface of the Intel® MEI device.

#### 20.1.1.7 HTYPE—Header Type Register (Intel® MEI 1—D22:F0)

Address Offset: 0Eh Attribute: RO  
Default Value: 80h Size: 8 bits

Bit	Description
7	<b>Multi-Function Device (MFD)</b> —RO. Indicates the Intel® MEI host controller is part of a multifunction device.
6:0	<b>Header Layout (HL)</b> —RO. Indicates that the Intel® MEI uses a target device layout.

#### 20.1.1.8 MEIO\_MBAR—Intel® MEI 1 MMIO Base Address Register (Intel® MEI 1—D22:F0)

Address Offset: 10h–17h Attribute: R/W, RO  
Default Value: 0000000000000004h Size: 64 bits

This register allocates space for the MEIO memory mapped registers.

Bit	Description
63:4	<b>Base Address (BA)</b> —R/W. Software programs this field with the base address of this region.
3	<b>Prefetchable Memory (PM)</b> —RO. Indicates that this range is not prefetchable.
2:1	<b>Type (TP)</b> —RO. Set to 10b to indicate that this range can be mapped anywhere in 64-bit address space.
0	<b>Resource Type Indicator (RTE)</b> —RO. Indicates a request for register memory space.



### 20.1.1.9 SVID—Subsystem Vendor ID Register (Intel® MEI 1—D22:F0)

Address Offset: 2Ch–2Dh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<p><b>Subsystem Vendor ID (SSVID)</b>—R/WO. Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes read-only. This field can only be cleared by PLTRST#.</p> <p><b>Note:</b> Register must be written as a Word write or as a DWord write with SVID register.</p>

### 20.1.1.10 SID—Subsystem ID Register (Intel® MEI 1—D22:F0)

Address Offset: 2Eh–2Fh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<p><b>Subsystem ID (SSID)</b>—R/WO. Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.</p> <p><b>Note:</b> Register must be written as a Word write or as a DWord write with SVID register.</p>

### 20.1.1.11 CAPP—Capabilities List Pointer Register (Intel® MEI 1—D22:F0)

Address Offset: 34h      Attribute: RO  
 Default Value: 50h      Size: 8 bits

Bit	Description
7:0	<b>Capabilities Pointer (PTR)</b> —RO. Indicates that the pointer for the first entry in the capabilities list is at 50h in configuration space.

### 20.1.1.12 INTR—Interrupt Information Register (Intel® MEI 1—D22:F0)

Address Offset: 3Ch–3Dh      Attribute: R/W, RO  
 Default Value: 0100h      Size: 16 bits

Bit	Description
15:8	<b>Interrupt Pin (IPIN)</b> —RO. This field indicates the interrupt pin the Intel® MEI host controller uses. A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. The upper 4 bits are hardwired to 0 and the lower 4 bits are programmed by the MEI1IP bits (RCBA+3124:bits 3:0).
7:0	<b>Interrupt Line (ILINE)</b> —R/W. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.



#### 20.1.1.13 HFSTS#1—Host Firmware Status Register #1 (Intel® MEI 1—D22:F0)

Address Offset: 40h–43h      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Firmware Status Register #1 (HFSTS#1)</b> —RO. This register field is used by Firmware to reflect the operating environment to the host.

#### 20.1.1.14 ME\_UMA—Intel® Management Engine UMA Register (Intel® MEI 1—D22:F0)

Address Offset: 44h–47h      Attribute: RO  
Default Value: 80000000h      Size: 32 bits

Bit	Description
31	Reserved—RO. Hardwired to 1. Can be used by host software to discover that this register is valid.
30:7	Reserved
16	<b>Intel® ME UMA Size Valid</b> —RO. This bit indicates that firmware has written to the MUSZ field.
15:6	Reserved
5:0	<b>Intel® ME UMA Size (MUSZ)</b> —RO. This field reflect Intel® ME Firmware’s desired size of Intel® ME UMA memory region. This field is set by Intel® ME firmware prior to core power bring up allowing BIOS to initialize memory. 000000b = 0MB, No memory allocated to Intel® ME UMA 000001b = 1MB 000010b = 2MB 000100b = 4MB 001000b = 8MB 010000b = 16MB 100000b = 32MB

#### 20.1.1.15 HFSTS#2—Host Firmware Status Register #2 (Intel® MEI 1—D22:F0)

Address Offset: 48h–4Bh      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Firmware Status Register #2(HFSTS#2)</b> —RO. This field is populated by Intel® ME.



### 20.1.1.16 H\_GS—Host General Status Register (Intel® MEI 1—D22:F0)

Address Offset: 4Ch–4Fh Attribute: R/W  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Host General Status(H_GS)</b> —R/W. General Status of Host, this field is not used by Hardware

### 20.1.1.17 PID—PCI Power Management Capability ID Register (Intel® MEI 1—D22:F0)

Address Offset: 50h–51h Attribute: RO  
Default Value: 8C01h Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —RO. Value of 8Ch indicates the location of the next pointer.
7:0	<b>Capability ID (CID)</b> —RO. Indicates the linked list item is a PCI Power Management Register.

### 20.1.1.18 PC—PCI Power Management Capabilities Register (Intel® MEI 1—D22:F0)

Address Offset: 52h–53h Attribute: RO  
Default Value: C803h Size: 16 bits

Bit	Description
15:11	<b>PME_Support (PSUP)</b> —RO. This five-bit field indicates the power states in which the function may assert PME#. Intel® MEI can assert PME# from any D-state except D1 or D2 which are not supported by Intel® MEI.
10:9	Reserved
8:6	<b>Aux_Current (AC)</b> —RO. Reports the maximum Suspend well current required when in the D3COLD state. Value of 00b is reported.
5	<b>Device Specific Initialization (DSI)</b> —RO. Indicates whether device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PMEC)</b> —RO. Indicates that 24-MHz clock is not required to generate PME#.
2:0	<b>Version (VS)</b> —RO. Hardwired to 011b to indicate support for <i>Revision 1.2 of the PCI Power Management Specification</i> .



### 20.1.1.19 PMCS—PCI Power Management Control and Status Register (Intel® MEI 1—D22:F0)

Address Offset: 54h–55h      Attribute: R/WC, R/W, RO  
Default Value: 0008h      Size: 16 bits

Bit	Description
15	<b>PME Status (PMES)</b> —R/WC. This bit is set by Intel® ME Firmware. Host software clears this bit by writing 1 to bit. This bit is reset when CL_RST# asserted.
14:9	Reserved
8	<b>PME Enable (PMEE)</b> —R/W. This bit is read/write and is under the control of host software. It does not directly have an effect on PME events. However, this bit is shadowed so Intel® ME firmware can monitor it. Intel® ME firmware will not cause the PMES bit to transition to 1 while the PMEE bit is 0, indicating that host software had disabled PME. This bit is reset when PLTRST# asserted.
7:4	Reserved
3	<b>No_Soft_Reset (NSR)</b> —RO. This bit indicates that when the Intel® MEI host controller is transitioning from D3 <sub>hot</sub> to D0 due to a power state command, it does not perform an internal reset. Configuration context is preserved.
2	Reserved
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the Intel® MEI host controller and to set a new power state. The values are: 00 = D0 state (default) 11 = D3 <sub>hot</sub> state The D1 and D2 states are not supported for the Intel® MEI host controller. When in the D3 <sub>hot</sub> state, the Intel® ME's configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked.

### 20.1.1.20 HFSTS#3—Host Firmware Status Register #3 (Intel® MEI 1—D22:F0)

Address Offset: 60h–63h      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Firmware Status #3(HFSTS#3)</b> —RO. This field is populated by Intel® ME.

### 20.1.1.21 HFSTS#4—Host Firmware Status Register #4 (Intel® MEI 1—D22:F0)

Address Offset: 64h–67h      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Firmware Status #4(HFSTS#4)</b> —RO. This field is populated by Intel® ME.



### 20.1.1.22 HFSTS#5—Host Firmware Status Register #5 (Intel® MEI 1—D22:F0)

Address Offset: 68h–6Bh      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Firmware Status #5(HFSTS#5)</b> —RO. This field is populated by Intel® ME.

### 20.1.1.23 HFSTS#6—Host Firmware Status Register #6 (Intel® MEI 1—D22:F0)

Address Offset: 6Ch–6Fh      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Firmware Status #6(HFSTS#6)</b> —RO. This field is populated by Intel® ME.

### 20.1.1.24 H\_GS2—Host General Status Register 2 (Intel® MEI 1—D22:F0)

Address Offset: 70h–73h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host General Status 2(H_GS 2)</b> —R/W. General Status of Host, this field is not used by Hardware

### 20.1.1.25 H\_GS3—Host General Status Register 3 (Intel® MEI 1—D22:F0)

Address Offset: 74h–77h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host General Status 3(H_GS3)</b> —R/W. General Status of Host, this field is not used by Hardware

### 20.1.1.26 MID—Message Signaled Interrupt (MSI) Identifiers Register (Intel® MEI 1—D22:F0)

Address Offset: 8Ch–8Dh      Attribute: RO  
Default Value: 0005h      Size: 16 bits

Bit	Description
15:8	<b>Next Pointer (NEXT)</b> —RO. Value of 00h indicates that this is the last item in the list.
7:0	<b>Capability ID (CID)</b> —RO. Capabilities ID indicates MSI.

**20.1.1.27 MC—Message Signaled Interrupt (MSI) Message Control Register (Intel® MEI 1—D22:F0)**

Address Offset: 8Eh–8Fh      Attribute: R/W, RO  
Default Value: 0080h      Size: 16 bits

Bit	Description
15:8	Reserved
7	<b>64-bit Address Capable (C64)</b> —RO. Specifies that function is capable of generating 64-bit messages.
6:1	Reserved
0	<b>MSI Enable (MSIE)</b> —R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

**20.1.1.28 MA—Message Signaled Interrupt (MSI) Message Address Register (Intel® MEI 1—D22:F0)**

Address Offset: 90h–93h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:2	<b>Address (ADDR)</b> —R/W. Lower 32 bits of the system specified message address, always DW aligned.
1:0	Reserved

**20.1.1.29 MUA—Message Signaled Interrupt Upper Address Register (Intel® MEI 1—D22:F0)**

Address Offset: 94h–97h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Upper Address (UADDR)</b> —R/W. Upper 32 bits of the system specified message address, always DW aligned.

**20.1.1.30 MD—Message Signaled Interrupt (MSI) Message Data Register (Intel® MEI 1—D22:F0)**

Address Offset: 98h–99h      Attribute: R/W  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Data (DATA)</b> —R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven during the data phase of the MSI memory write transaction.



### 20.1.1.31 HIDM—MEI Interrupt Delivery Mode Register (Intel® MEI 1—D22:F0)

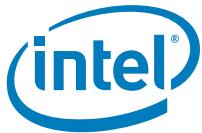
Address Offset: A0h Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:2	Reserved
1:0	<b>Intel® MEI Interrupt Delivery Mode (HIDM)</b> —R/W. These bits control what type of interrupt the Intel® MEI will send the host. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI

### 20.1.1.32 HERES—Intel® MEI Extend Register Status (Intel® MEI 1—D22:F0)

Address Offset: BCh–BFh Attribute: RO  
Default Value: 40000000h Size: 32 bits

Bit	Description
31	<b>Extend Register Valid (ERV)</b> —RO. Set by hardware after all firmware has been loaded. If the ERA field is SHA-1, the result of the extend operation is in HER:5–1. If the ERA field is SHA-256, the result of the extend operation is in HER:8–1.
30	<b>Extend Feature Present (EFP)</b> —RO. This bit is hardwired to 1 to allow driver software to easily detect the Chipset supports the Extend register firmware measurement feature.
29:4	Reserved
3:0	<b>Extend Register Algorithm (ERA)</b> —RO. This field indicates the hash algorithm used in the firmware measurement extend operations. Encodings are: 0h = SHA-1 2h = SHA-256 Other values = Reserved.



### 20.1.1.33 HERX—Intel® MEI Extend Register DWX (Intel® MEI 1—D22:F0)

Address Offset: HER1: C0h-C3h      Attribute: RO  
HER2: C4h-C7h  
HER3: C8h-CBh  
HER4: CCh-CFh  
HER5: D0h-D3h  
HER6: D4h-D7h  
HER7: D8h-DBh  
HER8: DCh-DFh  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Extend Register DWX (ERDWX)—RO.</b> Xth DWord result of the extend operation. <b>Note:</b> Extend Operation is HER[5:1] if using SHA-1. If using SHA-256 then Extend Operation is HER[8:1]

## 20.1.2 MEI0\_MBAR—Intel® MEI 1 MMIO Registers

These MMIO registers are accessible starting at the Intel® MEI 1 MMIO Base Address (MEI0\_MBAR) that gets programmed into D22:F0:Offset 10-17h. These registers are reset by PLTRST# unless otherwise noted.

**Table 20-2. Intel® MEI 1 MMIO Register Address Map**

MEI0_MBAR+Offset	Mnemonic	Register Name	Default	Attribute
00-03h	H_CB_WW	Host Circular Buffer Write Window	00000000h	WO
04h-07h	H_CSR	Host Control Status	02000040h	RO, R/W, R/WC
08h-0Bh	ME_CB_RW	Intel ME Circular Buffer Read Window	FFFFFFFh	RO
0Ch-0Fh	ME_CSR_HA	Intel ME Control Status Host Access	02000040h	RO
10h-13h	H_HPG_CSR	Host MEI0 Power Gating Control Status	00000000h	RO, R/WS

### 20.1.2.1 H\_CB\_WW—Host Circular Buffer Write Window Register (Intel® MEI 1 MMIO Register)

Address Offset: MEI0\_MBAR + 00h      Attribute: WO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Circular Buffer Write Window Field (H_CB_WWF)—WO.</b> This bit field is for host to write into its circular buffer. The host's circular buffer is located at the Intel ME subsystem address specified in the Host CB Base Address register. This field is write only, reads will return arbitrary data. Writes to this register will increment the H_CBWP as long as ME_RDY is 1. When ME_RDY is 0, writes to this register have no effect and are not delivered to the H_CB, nor is H_CBWP incremented.



### 20.1.2.2 H\_CSR—Host Control Status Register (Intel® MEI 1 MMIO Register)

Address Offset: MEI0\_MBAR + 04h Attribute: RO, R/W, R/WC  
 Default Value: 02000000h Size: 32 bits

Bit	Description
31:24	<b>Host Circular Buffer Depth (H_CBD)</b> —RO. This field indicates the maximum number of 32-bit entries available in the host circular buffer (H_CB). Host software uses this field, along with the H_CBRP and H_CBWP fields, to calculate the number of valid entries in the H_CB to read or # of entries available for write.  This field is implemented with a “1-hot” scheme. Only one bit will be set to a 1 at a time. Each bit position represents the value n of a buffer depth of $(2^n)$ . For example, when bit# 1 is 1, the buffer depth is 2; when bit#2 is 1, the buffer depth is 4, and so on. The allowed buffer depth values are 2, 4, 8, 16, 32, 64, and 128.
23:16	<b>Host CB Write Pointer (H_CBWP)</b> —RO. Points to next location in the H_CB for host to write the data. Software uses this field along with H_CBRP and H_CBD fields to calculate the number of valid entries in the H_CB to read or number of entries available for write.
15:8	<b>Host CB Read Pointer (H_CBRP)</b> —RO. Points to next location in the H_CB where a valid data is available for embedded controller to read. Software uses this field along with H_CBWR and H_CBD fields to calculate the number of valid entries in the host CB to read or number of entries available for write.
7:5	Reserved <b>Note:</b> For writes to this register, these bits shall be written as 000b.
4	<b>Host Reset (H_RST)</b> —R/W. Setting this bit to 1 will initiate an Intel® MEI reset sequence to get the circular buffers into a known good state for host and Intel® ME communication. When this bit transitions from 0 to 1, hardware will clear the H_RDY and ME_RDY bits.
3	<b>Host Ready (H_RDY)</b> —R/W. This bit indicates that the host is ready to process messages.
2	<b>Host Interrupt Generate (H_IG)</b> —R/W. Once message(s) are written into its CB, the host sets this bit to one for the hardware to set the ME_IS bit in the ME_CSR and to generate an interrupt message to Intel® ME. Hardware will send the interrupt message to Intel® ME only if the ME_IE is enabled. Hardware then clears this bit to 0.
1	<b>Host Interrupt Status (H_IS)</b> —R/WC. Hardware sets this bit to 1 when ME_IG bit is set to 1. Host clears this bit to 0 by writing a 1 to this bit position. H_IE has no effect on this bit.
0	<b>Host Interrupt Enable (H_IE)</b> —R/W. Host sets this bit to 1 to enable the host interrupt (INTR# or MSI) to be asserted when H_IS is set to 1.

### 20.1.2.3 ME\_CB\_RW—Intel® ME Circular Buffer Read Window Register (Intel® MEI 1 MMIO Register)

Address Offset: MEI0\_MBAR + 08h Attribute: RO  
 Default Value: FFFFFFFFh Size: 32 bits

Bit	Description
31:0	<b>Intel® ME Circular Buffer Read Window Field (ME_CB_RWF)</b> —RO. This bit field is for the host to read from the Intel® ME Circular Buffer. The Intel® ME's circular buffer is located at the Intel® ME subsystem address specified in the Intel® ME CB Base Address register. This field is read-only, writes have no effect. Reads to this register will increment the ME_CBRP as long as ME_RDY is 1. When ME_RDY is 0, reads to this register have no effect; all 1s are returned, and ME_CBRP is not incremented.



#### 20.1.2.4 ME\_CSR\_HA—Intel® ME Control Status Host Access Register (Intel® MEI 1 MMIO Register)

Address Offset: MEI0\_MBAR + 0Ch Attribute: RO  
Default Value: 02000040h Size: 32 bits

Bit	Description
31:24	<b>Intel® ME Circular Buffer Depth Host Read Access (ME_CBD_HRA)</b> —RO. Host read only access to ME_CBD.
23:16	<b>Intel® ME CB Write Pointer Host Read Access (ME_CBWP_HRA)</b> —RO. Host read only access to ME_CBWP.
15:8	<b>Intel® ME CB Read Pointer Host Read Access (ME_CBRP_HRA)</b> —RO. Host read only access to ME_CBRP.
7:5	Reserved
4	<b>Intel® ME Reset Host Read Access (ME_RST_HRA)</b> —RO. Host read access to ME_RST.
3	<b>Intel® ME Ready Host Read Access (ME_RDY_HRA)</b> —RO. Host read access to ME_RDY.
2	<b>Intel® ME Interrupt Generate Host Read Access (ME_IG_HRA)</b> —RO. Host read only access to ME_IG.
1	<b>Intel® ME Interrupt Status Host Read Access (ME_IS_HRA)</b> —RO. Host read only access to ME_IS.
0	<b>Intel® ME Interrupt Enable Host Read Access (ME_IE_HRA)</b> —RO. Host read only access to ME_IE.

#### 20.1.2.5 H\_HPG\_CSR—Host MEI0 Power Gating Control Register (Intel® MEI 1 MMIO Register)

Address Offset: MEI0\_MBAR + 10h Attribute: RO, R/W  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:2	Reserved
1	<b>Power Gate Isolated (PGI)</b> 1 = The MEI interface is in the Power Gate Isolated state. 0 = The MEI interface is in the Power Gate Un-isolated state.
0	<b>Power Gate Isolated Host Exit Request Status (PGIHEXRS)</b> 1 = The host software has made a request to place the MEI interface in the Power Gate Isolated state. 0 = The request to place the MEI interface in the Power Gate Un-isolated state has been serviced.



## 20.2 Second Intel® Management Engine Interface (Intel® MEI 2) Configuration Registers (Intel® MEI 2—D22:F1)

### 20.2.1 PCI Configuration Registers (Intel® MEI 2—D22:F1)

**Table 20-3. Intel® MEI 2 Configuration Registers Address Map (Intel® MEI 2—D22:F1) (Sheet 1 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	See register description	RO
04h–05h	PCICMD	PCI Command	0000h	R/W, RO
06h–07h	PCISTS	PCI Status	0010h	RO
08h	RID	Revision Identification	See register description	RO
09h–0Bh	CC	Class Code	078000h	RO
0Eh	HTYPE	Header Type	80h	RO
10h–17h	MEI1_MBAR	Intel® MEI 2 MMIO Base Address	0000000000000000 004h	R/W, RO
2Ch–2Dh	SVID	Subsystem Vendor ID	0000h	R/WO
2Eh–2Fh	SID	Subsystem ID	0000h	R/WO
34h	CAPP	Capabilities List Pointer	50h	RO
3Ch–3Dh	INTR	Interrupt Information	0200h	R/W, RO
40h–43h	HFS	Host Firmware Status	00000000h	RO
48h–4Bh	GMES	General Intel ME Status	00000000h	RO
4Ch–4Fh	H_GS	Host General Status	00000000h	R/W
50h–51h	PID	PCI Power Management Capability ID	8C01h	RO
52h–53h	PC	PCI Power Management Capabilities	C803h	RO
54h–55h	PMCS	PCI Power Management Control and Status	0008h	R/WC, R/W, RO
60h–63h	GMES2	General Intel ME Status 2	00000000h	RO
64h–67h	GMES3	General Intel ME Status 3	00000000h	RO
68h–6Bh	GMES4	General Intel ME Status 4	00000000h	RO
6Ch–6Fh	GMES5	General Intel ME Status 5	00000000h	RO
70h–73h	H_GS2	Host General Status 2	00000000h	RW
74h–77h	H_GS3	Host General Status 3	00000000h	RW
8Ch–8Dh	MID	Message Signaled Interrupt Identifiers	0005h	RO
8Eh–8Fh	MC	Message Signaled Interrupt Message Control	0080h	R/W, RO
90h–93h	MA	Message Signaled Interrupt Message Address	00000000h	R/W, RO
94h–97h	MUA	Message Signaled Interrupt Upper Address	00000000h	R/W
98h–99h	MD	Message Signaled Interrupt Message Data	0000h	R/W



**Table 20-3. Intel® MEI 2 Configuration Registers Address Map (Intel® MEI 2—D22:F1) (Sheet 2 of 2)**

Offset	Mnemonic	Register Name	Default	Attribute
A0h	HIDM	Intel® MEI Interrupt Delivery Mode	00h	R/W
BC-BFh	HERES	Intel® MEI Extended Register Status	40000000h	RO
C0-DFh	HER[1:8]	Intel® MEI Extended Register DW[1:8]	00000000h	RO

### 20.2.1.1 VID—Vendor Identification Register (Intel® MEI 2—D22:F1)

Address Offset: 00h-01h Attribute: RO  
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	<b>Vendor ID (VID)</b> —RO. This is a 16-bit value assigned to Intel.

## 20.2.1.2 DID—Device Identification Register (Intel® MEI 2—D22:F1)

Address Offset: 02h-03h Attribute: RO  
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	<b>Device ID (DID)</b> —RO. This is a 16-bit value assigned to the Intel® Management Engine Interface controller. See <a href="#">Section 1.4</a> for the value of the DID Register.



### 20.2.1.3 PCICMD—PCI Command Register (Intel® MEI 2—D22:F1)

Address Offset: 04h–05h      Attribute: R/W, RO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable (ID)</b> —R/W. Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9:3	Reserved
2	<b>Bus Master Enable (BME)</b> —R/W. Controls the Intel® MEI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, Intel® MEI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an Intel® ME MSI. When this bit is 0, Intel® MEI is blocked from generating MSI to the host processor.  <b>Note:</b> This bit does not block Intel® MEI accesses to Intel® ME UMA; that is, writes or reads to the host and Intel® ME circular buffers through the read window and write window registers still cause Intel® ME backbone transactions to Intel® ME UMA.
1	<b>Memory Space Enable (MSE)</b> —R/W. Controls access to the Intel® ME memory mapped register space. 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers accepted.
0	Reserved

### 20.2.1.4 PCISTS—PCI Status Register (Intel® MEI 2—D22:F1)

Address Offset: 06h–07h      Attribute: RO  
 Default Value: 0010h      Size: 16 bits

Bit	Description
15:5	<b>Reserved</b>
4	Capabilities List (CL)—RO. Indicates the presence of a capabilities list, hardwired to 1.
3	<b>Interrupt Status</b> —RO. Indicates the interrupt status of the device. 0 = Interrupt is de-asserted. 1 = Interrupt is asserted.
2:0	Reserved



#### 20.2.1.5 RID—Revision Identification Register (Intel® MEI 2—D22:F1)

Offset Address: 08h Attribute: RO  
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See Section 1.4 the value of the RID Register.

#### 20.2.1.6 CC—Class Code Register (Intel® MEI 2—D22:F1)

Address Offset: 09h–0Bh Attribute: RO  
Default Value: 078000h Size: 24 bits

Bit	Description
23:16	<b>Base Class Code (BCC)</b> —RO. Indicates the base class code of the Intel® MEI device.
15:8	<b>Sub Class Code (SCC)</b> —RO. Indicates the sub class code of the Intel® MEI device.
7:0	<b>Programming Interface (PI)</b> —RO. Indicates the programming interface of the Intel® MEI device.

#### 20.2.1.7 HTYPE—Header Type Register (Intel® MEI 2—D22:F1)

Address Offset: 0Eh Attribute: RO  
Default Value: 80h Size: 8 bits

Bit	Description
7	<b>Multi-Function Device (MFD)</b> —RO. Indicates the Intel® MEI host controller is part of a multifunction device.
6:0	<b>Header Layout (HL)</b> —RO. Indicates that the Intel® MEI uses a target device layout.

#### 20.2.1.8 MEI1\_MBAR—Intel® MEI 2 MMIO Base Address Register (Intel® MEI 2—D22:F1)

Address Offset: 10h–17h Attribute: R/W, RO  
Default Value: 0000000000000004h Size: 64 bits

This register allocates space for the Intel® MEI memory mapped registers.

Bit	Description
63:4	<b>Base Address (BA)</b> —R/W. Software programs this field with the base address of this region.
3	<b>Prefetchable Memory (PM)</b> —RO. Indicates that this range is not prefetchable.
2:1	<b>Type (TP)</b> —RO. Set to 10b to indicate that this range can be mapped anywhere in 64-bit address space.
0	<b>Resource Type Indicator (RTE)</b> —RO. Indicates a request for register memory space.



### 20.2.1.9 SVID—Subsystem Vendor ID Register (Intel® MEI 2—D22:F1)

Address Offset: 2Ch–2Dh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<p><b>Subsystem Vendor ID (SSVID)</b>—R/WO. Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes read-only. This field can only be cleared by PLTRST#.</p> <p><b>Note:</b> Register must be written as a Word write or as a DWord write with SVID register.</p>

### 20.2.1.10 SID—Subsystem ID Register (Intel® MEI 2—D22:F1)

Address Offset: 2Eh–2Fh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<p><b>Subsystem ID (SSID)</b>—R/WO. Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes read-only. This field can only be cleared by PLTRST#.</p> <p><b>Note:</b> Register must be written as a Word write or as a DWord write with SVID register.</p>

### 20.2.1.11 CAPP—Capabilities List Pointer Register (Intel® MEI 2—D22:F1)

Address Offset: 34h      Attribute: RO  
 Default Value: 50h      Size: 8 bits

Bit	Description
7:0	<b>Capabilities Pointer (PTR)</b> —RO. Indicates that the pointer for the first entry in the capabilities list is at 50h in configuration space.

### 20.2.1.12 INTR—Interrupt Information Register (Intel® MEI 2—D22:F1)

Address Offset: 3Ch–3Dh      Attribute: R/W, RO  
 Default Value: 0200h      Size: 16 bits

Bit	Description
15:8	<b>Interrupt Pin (IPIN)</b> —RO. This field indicates the interrupt pin the Intel® MEI host controller uses. A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. The upper 4 bits are hardwired to 0 and the lower 4 bits are programmed by the MEI2IP bits (RCBA+3124:bits 7:4).
7:0	<b>Interrupt Line (ILINE)</b> —R/W. Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.



#### 20.2.1.13 HFS—Host Firmware Status Register (Intel® MEI 2—D22:F1)

Address Offset: 40h–43h      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Firmware Status (HFS)</b> —RO. This register field is used by firmware to reflect the operating environment to the host.

#### 20.2.1.14 GMES—General Intel® ME Status Register (Intel® MEI 2—D22:F1)

Address Offset: 48h–4Bh      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>General Intel® ME Status (ME_GS)</b> —RO. This field is populated by Intel® ME.

#### 20.2.1.15 H\_GS—Host General Status Register (Intel® MEI 2—D22:F1)

Address Offset: 4Ch–4Fh      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host General Status(H_GS)</b> —R/W. General Status of Host; this field is not used by Hardware

#### 20.2.1.16 PID—PCI Power Management Capability ID Register (Intel® MEI 2—D22:F1)

Address Offset: 50h–51h      Attribute: RO  
Default Value: 8C01h      Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —RO. Value of 8Ch indicates the location of the next pointer.
7:0	<b>Capability ID (CID)</b> —RO. Indicates the linked list item is a PCI Power Management Register.



### 20.2.1.17 PC—PCI Power Management Capabilities Register (Intel® MEI 2—D22:F1)

Address Offset: 52h–53h      Attribute: RO  
 Default Value: C803h      Size: 16 bits

Bit	Description
15:11	<b>PME_Support (PSUP)</b> —RO. This five-bit field indicates the power states in which the function may assert PME#. Intel® MEI can assert PME# from any D-state except D1 or D2, which are not supported by Intel® MEI.
10:9	Reserved
8:6	<b>Aux_Current (AC)</b> —RO. Reports the maximum Suspend well current required when in the D3 <sub>COLD</sub> state. Value of 00b is reported.
5	<b>Device Specific Initialization (DSI)</b> —RO. Indicates whether device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PMEC)</b> —RO. Indicates that 24-MHz clock is not required to generate PME#.
2:0	<b>Version (VS)</b> —RO. Hardwired to 011b to indicate support for <i>Revision 1.2 of the PCI Power Management Specification</i> .

### 20.2.1.18 PMCS—PCI Power Management Control and Status Register (Intel® MEI 2—D22:F1)

Address Offset: 54h–55h      Attribute: R/WC, R/W, RO  
 Default Value: 0008h      Size: 16 bits

Bit	Description
15	<b>PME Status (PMES)</b> —R/WC. Bit is set by Intel® ME Firmware. Host software clears bit by writing 1 to bit. This bit is reset when CL_RST# is asserted.
14:9	Reserved
8	<b>PME Enable (PMEE)</b> —R/W. This bit is read/write and is under the control of host software. It does not directly have an effect on PME events. However, this bit is shadowed so Intel® ME firmware can monitor it. Intel® ME firmware will not cause the PMES bit to transition to 1 while the PMEE bit is 0, indicating that host software had disabled PME. This bit is reset when PLTRST# asserted.
7:4	Reserved
3	<b>No_Soft_Reset (NSR)</b> —RO. This bit indicates that when the Intel® MEI host controller is transitioning from D3 <sub>hot</sub> to D0 due to a power state command, it does not perform an internal reset. Configuration context is preserved.
2	Reserved
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the Intel® MEI host controller and to set a new power state. The values are: 00 = D0 state (default) 11 = D3 <sub>hot</sub> state The D1 and D2 states are not supported for the Intel® MEI host controller. When in the D3 <sub>hot</sub> state, the Intel® ME's configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked.



### 20.2.1.19 GMES2—General Intel® ME Status Register 2 (Intel® MEI 2—D22:F1)

Address Offset: 60h–63h      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>General Intel® ME Status 2 (ME_GS 2)</b> —RO. This field is populated by Intel® ME.

### 20.2.1.20 GMES3—General Intel® ME Status Register 3 (Intel® MEI 2—D22:F1)

Address Offset: 64h–67h      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>General Intel® ME Status 3 (ME_GS 3)</b> —RO. This field is populated by Intel® ME.

### 20.2.1.21 GMES4—General Intel® ME Status Register 4 (Intel® MEI 2—D22:F1)

Address Offset: 68h–6Bh      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>General Intel® ME Status 4(ME_GS 4)</b> —RO. This field is populated by Intel® ME.

### 20.2.1.22 GMES5—General Intel® ME Status Register 5 (Intel® MEI 2—D22:F1)

Address Offset: 6Ch–6Fh      Attribute: RO  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>General Intel® ME Status 5(ME_GS 5)</b> —RO. This field is populated by Intel® ME.

### 20.2.1.23 H\_GS2—Host General Status Register 2 (Intel® MEI 2—D22:F1)

Address Offset: 70h–73h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host General Status 2(H_GS 2)</b> —R/W. General Status of Host; this field is not used by Hardware

### 20.2.1.24 H\_GS3—Host General Status Register 3 (Intel® MEI 2—D22:F1)

Address Offset: 74h–77h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host General Status 3(H_GS3)</b> —R/W. General Status of Host; this field is not used by Hardware



### 20.2.1.25 MID—Message Signaled Interrupt (MSI) Identifiers Register (Intel® MEI 2—D22:F1)

Address Offset: 8Ch-8Dh      Attribute: RO  
 Default Value: 0005h      Size: 16 bits

Bit	Description
15:8	<b>Next Pointer (NEXT)</b> —RO. Value of 00h indicates that this is the last item in the list.
7:0	<b>Capability ID (CID)</b> —RO. Capabilities ID indicates MSI.

### 20.2.1.26 MC—Message Signaled Interrupt (MSI) Message Control Register (Intel® MEI 2—D22:F1)

Address Offset: 8Eh-8Fh      Attribute: R/W, RO  
 Default Value: 0080h      Size: 16 bits

Bit	Description
15:8	Reserved
7	<b>64-bit Address Capable (C64)</b> —RO. Specifies that function is capable of generating 64-bit messages.
6:1	Reserved
0	<b>MSI Enable (MSIE)</b> —R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

### 20.2.1.27 MA—Message Signaled Interrupt Message (MSI) Address Register (Intel® MEI 2—D22:F1)

Address Offset: 90h-93h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:2	<b>Address (ADDR)</b> —R/W. Lower 32 bits of the system specified message address; always DWord aligned.
1:0	Reserved

### 20.2.1.28 MUA—Message Signaled Interrupt Upper Address Register (Intel® MEI 2—D22:F1)

Address Offset: 94h-97h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Upper Address (UADDR)</b> —R/W. Upper 32 bits of the system specified message address; always DWord aligned.



### 20.2.1.29 MD—Message Signaled Interrupt (MSI) Message Data Register (Intel® MEI 2—D22:F1)

Address Offset: 98h–99h      Attribute: R/W  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Data (DATA)</b> —R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven during the data phase of the MSI memory write transaction.

### 20.2.1.30 HIDM—Intel® MEI Interrupt Delivery Mode Register (Intel® MEI 2—D22:F1)

Address Offset: A0h      Attribute: R/W  
Default Value: 00h      Size: 8 bits

Bit	Description
7:2	Reserved
1:0	<b>Intel® MEI Interrupt Delivery Mode (HIDM)</b> —R/W. These bits control what type of interrupt the Intel® MEI will send the host. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI

### 20.2.1.31 HERES—Intel® MEI Extend Register Status (Intel® MEI 2—D22:F1)

Address Offset: BCh–BFh      Attribute: RO  
Default Value: 00h      Size: 32 bits

Bit	Description
31	<b>Extend Register Valid (ERV)</b> —RO. Set by hardware after all firmware has been loaded. If the ERA field is SHA-1, the result of the extend operation is in HER:5–1. If the ERA field is SHA-256, the result of the extend operation is in HER:8–1.
30	<b>Extend Feature Present (EFP)</b> —RO. This bit is hardwired to 1 to allow driver software to easily detect the Chipset supports the Extend Register firmware measurement feature.
29:4	Reserved
3:0	<b>Extend Register Algorithm (ERA)</b> —RO. This field indicates the hash algorithm used in the firmware measurement extend operations. Encodings are: 0h = SHA-1 2h = SHA-256 Other values = Reserved



### 20.2.1.32 HERX—Intel® MEI Extend Register DWX (Intel® MEI 2—D22:F1)

Address Offset: HER1: C0h–C3h      Attribute: RO  
                   HER2: C4h–C7h  
                   HER3: C8h–CBh  
                   HER4: CCh–CFh  
                   HER5: D0h–D3h  
                   HER6: D4h–D7h  
                   HER7: D8h–DBh  
                   HER8: DCh–DFh  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	Extend Register DWX (ERDWX): Xth DWord result of the extend operation.  <b>Note:</b> Extend Operation is HER[5:1] if using SHA-1. If using SHA-256, then Extend Operation is HER[8:1].

## 20.2.2 MEI1\_MBAR—Intel® MEI 2 MMIO Registers

These MMIO registers are accessible starting at the Intel® MEI 2 MMIO Base Address (MEI1\_MBAR) which gets programmed into D22:F1:Offset 10–17h. These registers are reset by PLTRST# unless otherwise noted.

**Table 20-4. Intel® MEI 2 MMIO Register Address Map**

MEI1_MBAR+Offset	Mnemonic	Register Name	Default	Attribute
00–03h	H_CB_WW	Host Circular Buffer Write Window	00000000h	W
04h–07h	H_CSR	Host Control Status	02000000h	R/W, R/WC, RO
08h–0Bh	ME_CB_RW	Intel ME Circular Buffer Read Window	FFFFFFFFFFh	RO
0Ch–0Fh	ME_CSR_HA	Intel ME Control Status Host Access	02000040h	RO
10h–13h	H_HPG_CSR	Host MEI1 Power Gating Control Status	00000000h	RO, R/WS

### 20.2.2.1 H\_CB\_WW—Host Circular Buffer Write Window (Intel® MEI 2 MMIO Register)

Address Offset: MEI1\_MBAR + 00h      Attribute: W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Host Circular Buffer Write Window Field (H_CB_WWF)</b> —W. This bit field is for host to write into its circular buffer. The host's circular buffer is located at the Intel® ME subsystem address specified in the Host CB Base Address register. This field is write only, reads will return arbitrary data. Writes to this register will increment the H_CBWP as long as ME_RDY is 1. When ME_RDY is 0, writes to this register have no effect and are not delivered to the H_CB, nor is H_CBWP incremented.



### 20.2.2.2 H\_CSR—Host Control Status Register (Intel® MEI 2 MMIO Register)

Address Offset: MEI1\_MBAR + 04h Attribute: RO, R/W, R/WC  
Default Value: 02000000h Size: 32 bits

Bit	Description
31:24	<b>Host Circular Buffer Depth (H_CBD)</b> —RO. This field indicates the maximum number of 32-bit entries available in the host circular buffer (H_CB). Host software uses this field, along with the H_CBRP and H_CBWP fields, to calculate the number of valid entries in the H_CB to read or # of entries available for write. This field is implemented with a “1-hot” scheme. Only one bit will be set to a ‘1’ at a time. Each bit position represents the value n of a buffer depth of $(2^n)$ . For example, when bit #1 is 1, the buffer depth is 2; when bit #2 is 1, the buffer depth is 4, and so on. The allowed buffer depth values are 2, 4, 8, 16, 32, 64, and 128.
23:16	<b>Host CB Write Pointer (H_CBWP)</b> —RO. Points to next location in the H_CB for host to write the data. Software uses this field along with H_CBRP and H_CBD fields to calculate the number of valid entries in the H_CB to read or number of entries available for write.
15:8	<b>Host CB Read Pointer (H_CBRP)</b> —RO. Points to next location in the H_CB where a valid data is available for embedded controller to read. Software uses this field along with H_CBWR and H_CBD fields to calculate the number of valid entries in the host CB to read or number of entries available for write.
7:5	Reserved <b>Note:</b> For writes to this register, these bits shall be written as 000b.
4	<b>Host Reset (H_RST)</b> —R/W. Setting this bit to 1 will initiate a Intel® MEI reset sequence to get the circular buffers into a known good state for host and Intel® ME communication. When this bit transitions from 0 to 1, hardware will clear the H_RDY and ME_RDY bits.
3	<b>Host Ready (H_RDY)</b> —R/W. This bit indicates that the host is ready to process messages.
2	<b>Host Interrupt Generate (H_IG)</b> —R/W. Once message(s) are written into its CB, the host sets this bit to one for the hardware to set the ME_IS bit in the ME_CSR and to generate an interrupt message to Intel® ME. Hardware will send the interrupt message to Intel® ME only if the ME_IE is enabled. Hardware then clears this bit to 0.
1	<b>Host Interrupt Status (H_IS)</b> —R/WC. Hardware sets this bit to 1 when ME_IG bit is set to 1. Host clears this bit to 0 by writing a 1 to this bit position. H_IE has no effect on this bit.
0	<b>Host Interrupt Enable (H_IE)</b> —R/W. Host sets this bit to 1 to enable the host interrupt (INTR# or MSI) to be asserted when H_IS is set to 1.

### 20.2.2.3 ME\_CB\_RW—Intel® ME Circular Buffer Read Window Register (Intel® MEI 2 MMIO Register)

Address Offset: MEI1\_MBAR + 08h Attribute: RO  
Default Value: FFFFFFFFh Size: 32 bits

Bit	Description
31:0	<b>Intel® ME Circular Buffer Read Window Field (ME_CB_RWF)</b> . This bit field is for the host to read from the Intel® ME Circular Buffer. The Intel® ME’s circular buffer is located at the Intel® ME subsystem address specified in the Intel® ME CB Base Address register. This field is read-only, writes have no effect. Reads to this register will increment the ME_CBRP as long as ME_RDY is 1. When ME_RDY is 0, reads to this register have no effect; all 1s are returned, and ME_CBRP is not incremented.



#### 20.2.2.4 ME\_CSR\_HA—Intel® ME Control Status Host Access Register (Intel® MEI 2 MMIO Register)

Address Offset: MEI1\_MBAR + 0Ch Attribute: RO  
 Default Value: 02000040h Size: 32 bits

Bit	Description
31:24	Intel® ME Circular Buffer Depth Host Read Access (ME_CBD_HRA). Host read only access to ME_CBD.
23:16	Intel® ME CB Write Pointer Host Read Access (ME_CBWP_HRA). Host read only access to ME_CBWP.
15:8	Intel® ME CB Read Pointer Host Read Access (ME_CBRP_HRA). Host read only access to ME_CBRP.
7:5	Reserved
4	Intel® ME Reset Host Read Access (ME_RST_HRA). Host read access to ME_RST.
3	Intel® ME Ready Host Read Access (ME_RDY_HRA). Host read access to ME_RDY.
2	Intel® ME Interrupt Generate Host Read Access (ME_IG_HRA). Host read only access to ME_IG.
1	Intel® ME Interrupt Status Host Read Access (ME_IS_HRA). Host read only access to ME_IS.
0	Intel® ME Interrupt Enable Host Read Access (ME_IE_HRA). Host read only access to ME_IE.

#### 20.2.2.5 H\_HPG\_CSR—Host MEI1 Power Gating Control Status (Intel® MEI 2 MMIO Register)

Address Offset: MEI1\_MBAR + 10h Attribute: RO, RW  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:2	Reserved
1	Power Gate Isolated (PGI) 1 = The MEI interface is in the Power Gate Isolated state. 0 = The MEI interface is in the Power Gate Un-isolated state.
0	Power Gate Isolated Host Exit Request Status (PGIHEXRS) 1 = The host software has made a request to place the MEI interface in the Power Gate Isolated state. 0 = The request to place the MEI interface in the Power Gate Un-isolated state has been serviced.

## 20.3 IDE Redirect IDER Registers (IDER—D22:F2)

### 20.3.1 PCI Configuration Registers (IDER—D22:F2)

**Table 20-5. IDE Redirect Function IDER Register Address Map**

Address Offset	Register Symbol	Register Name	Default Value	Attribute
00h-01h	VID	Vendor Identification	8086h	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	RO, R/W
06h-07h	PCISTS	PCI Status	00B0h	RO
08h	RID	Revision ID	See register description	RO
09h-0Bh	CC	Class Codes	010185h	RO
0Ch	CLS	Cache Line Size	00h	RO
10h-13h	PCMDBA	Primary Command Block I/O Bar	00000001h	RO, R/W
14h-17h	PCTLBA	Primary Control Block Base Address	00000001h	RO, R/W
18h-1Bh	SCMDBA	Secondary Command Block Base Address	00000001h	RO, R/W
1Ch-1Fh	SCTLBA	Secondary Control Block base Address	00000001h	RO, R/W
20h-23h	LBAR	Legacy Bus Master Base Address	00000001h	RO, R/W
2Ch-2Dh	SVID	Subsystem Vendor ID	0000h	R/WO
2Eh-2Fh	SID	Subsystem ID	8086h	R/WO
34h	CAPP	Capabilities Pointer	C8h	RO
3Ch-3Dh	INTR	Interrupt Information	0300h	R/W, RO
C8h-C9h	PID	PCI Power Management Capability ID	D001h	RO
CAh-CBh	PC	PCI Power Management Capabilities	0023h	RO
CCh-CFh	PMCS	PCI Power Management Control and Status	00000000h	RO, R/W, RO/V
D0h-D1h	MID	Message Signaled Interrupt Capability ID	0005h	RO
D2h-D3h	MC	Message Signaled Interrupt Message Control	0080h	RO, R/W
D4h-D7h	MA	Message Signaled Interrupt Message Address	00000000h	R/W, RO
D8h-DBh	MAU	Message Signaled Interrupt Message Upper Address	00000000h	RO, R/W
DC-DDh	MD	Message Signaled Interrupt Message Data	0000h	R/W

#### 20.3.1.1 VID—Vendor Identification Register (IDER—D22:F2)

Address Offset: 00-01h  
Default Value: 8086h

Attribute: RO  
Size: 16 bits

Bit	Description
15:0	<b>Vendor ID (VID)</b> —RO. This is a 16-bit value assigned by Intel.



### 20.3.1.2 DID—Device Identification Register (IDER—D22:F2)

Address Offset: 02–03h Attribute: RO  
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	<b>Device ID (DID)</b> —RO. This is a 16-bit value assigned to the PCH IDER controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

### 20.3.1.3 PCICMD—PCI Command Register (IDER—D22:F2)

Address Offset: 04–05h Attribute: RO, R/W  
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable (ID)</b> —R/W. This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt <b>and</b> MSI is not enabled.
9:3	Reserved
2	<b>Bus Master Enable (BME)</b> —RO. This bit controls the PT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands.
1	<b>Memory Space Enable (MSE)</b> —RO. PT function does not contain target memory space.
0	<b>I/O Space enable (IOSE)</b> —RO. This bit controls access to the PT function's target I/O space.

### 20.3.1.4 PCISTS—PCI Device Status Register (IDER—D22:F2)

Address Offset: 06–07h Attribute: RO  
Default Value: 00B0h Size: 16 bits

Bit	Description
15:11	Reserved
10:9	<b>DEVSEL# Timing Status (DEVT)</b> —RO. This bit controls the device select time for the PT function's PCI interface.
8:5	Reserved
4	<b>Capabilities List (CL)</b> —RO. This bit indicates that there is a capabilities pointer implemented in the device.
3	<b>Interrupt Status (IS)</b> —RO. This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTc interrupt asserted to the Host.
2:0	Reserved

### 20.3.1.5 RID—Revision Identification Register (IDER—D22:F2)

Address Offset: 08h Attribute: RO  
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See <a href="#">Section 1.4</a> for the value of the RID Register.



### 20.3.1.6 CC—Class Codes Register (IDER—D22:F2)

Address Offset: 09–0Bh      Attribute: RO  
Default Value: 010185h      Size: 24 bits

Bit	Description
23:16	<b>Base Class Code (BCC)</b> —RO. This field indicates the base class code of the IDER host controller device.
15:8	<b>Sub Class Code (SCC)</b> —RO. This field indicates the sub class code of the IDER host controller device.
7:0	<b>Programming Interface (PI)</b> —RO. This field indicates the programming interface of the IDER host controller device.

### 20.3.1.7 CLS—Cache Line Size Register (IDER—D22:F2)

Address Offset: 0Ch      Attribute: RO  
Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Cache Line Size (CLS)</b> —RO. All writes to system memory are Memory Writes.

### 20.3.1.8 PCMDBA—Primary Command Block I/O Bar Register (IDER—D22:F2)

Address Offset: 10–13h      Attribute: RO, R/W  
Default Value: 00000001h      Size: 32 bits

Bit	Description
31:16	Reserved
15:3	<b>Base Address (BAR)</b> —R/W. Base Address of the BAR0 I/O space (8 consecutive I/O locations).
2:1	Reserved
0	<b>Resource Type Indicator (RTE)</b> —RO. This bit indicates a request for I/O space.

### 20.3.1.9 PCTLBA—Primary Control Block Base Address Register (IDER—D22:F2)

Address Offset: 14–17h      Attribute: RO, R/W  
Default Value: 00000001h      Size: 32 bits

Bit	Description
31:16	Reserved
15:2	<b>Base Address (BAR)</b> —R/W. Base Address of the BAR1 I/O space (4 consecutive I/O locations).
1	Reserved
0	<b>Resource Type Indicator (RTE)</b> —RO. This bit indicates a request for I/O space.



### 20.3.1.10 SCMDBA—Secondary Command Block Base Address Register (IDER—D22:F2)

Address Offset: 18–1Bh      Attribute: RO, R/W  
 Default Value: 00000001h      Size: 32 bits

Bit	Description
31:16	Reserved
15:3	<b>Base Address (BAR)</b> —R/W. Base Address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	<b>Resource Type Indicator (RTE)</b> —RO. This bit indicates a request for I/O space.

### 20.3.1.11 SCTLBA—Secondary Control Block Base Address Register (IDER—D22:F2)

Address Offset: 1C–1Fh      Attribute: RO, R/W  
 Default Value: 00000001h1      Size: 32 bits

Bit	Description
31:16	Reserved
15:2	<b>Base Address (BAR)</b> —R/W. Base Address of the I/O space (4 consecutive I/O locations).
1	Reserved
0	<b>Resource Type Indicator (RTE)</b> —RO. This bit indicates a request for I/O space.

### 20.3.1.12 LBAR—Legacy Bus Master Base Address Register (IDER—D22:F2)

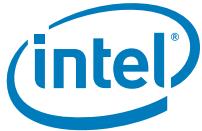
Address Offset: 20–23h      Attribute: RO, R/W  
 Default Value: 00000001h      Size: 32 bits

Bit	Description
31:16	Reserved
15:4	<b>Base Address (BA)</b> —R/W. Base Address of the I/O space (16 consecutive I/O locations).
3:1	Reserved
0	<b>Resource Type Indicator (RTE)</b> —RO. This bit indicates a request for I/O space.

### 20.3.1.13 SVID—Subsystem Vendor ID Register (IDER—D22:F2)

Address Offset: 2Ch–2Dh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (SSVID)</b> —R/WO. Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes read-only. This field can only be cleared by PLTRST#. <b>Note:</b> Register must be written as a DWord write with SID register.



#### 20.3.1.14 SID—Subsystem ID Register (IDER—D22:F2)

Address Offset: 2Eh–2Fh Attribute: R/WO  
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (SSID)</b> —R/WO. Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes read-only. This field can only be cleared by PLTRST#.  <b>Note:</b> Register must be written as a DWord write with SVID register.

#### 20.3.1.15 CAPP—Capabilities List Pointer Register (IDER—D22:F2)

Address Offset: 34h Attribute: R/WO  
Default Value: C8h Size: 8 bits

Bit	Description
7:0	<b>Capability Pointer (CP)</b> —R/WO. This field indicates that the first capability pointer is offset C8h (the power management capability).

#### 20.3.1.16 INTR—Interrupt Information Register (IDER—D22:F2)

Address Offset: 3C–3Dh Attribute: R/W, RO  
Default Value: 0300h Size: 16 bits

Bit	Description
15:8	<b>Interrupt Pin (IPIN)</b> —RO. A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. The upper 4 bits are hardwired to 0 and the lower 4 bits are programmed by the IDERIP bits (RCBA+3124:bits 11:8).
7:0	<b>Interrupt Line (ILINE)</b> —R/W. The value written in this register indicates which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the operating system and the device driver, and has no affect on the hardware.

#### 20.3.1.17 PID—PCI Power Management Capability ID Register (IDER—D22:F2)

Address Offset: C8–C9h Attribute: RO  
Default Value: D001h Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —RO. Its value of D0h points to the MSI capability.
7:0	<b>Cap ID (CID)</b> —RO. This field indicates that this pointer is a PCI power management.



### 20.3.1.18 PC—PCI Power Management Capabilities Register (IDER—D22:F2)

Address Offset: CA-CBh      Attribute: RO  
 Default Value: 0023h      Size: 16 bits

Bit	Description
15:11	<b>PME_Support (PSUP)</b> —RO. This five-bit field indicates the power states in which the function may assert PME#. IDER can assert PME# from any D-state except D1 or D2 that are not supported by IDER.
10:9	Reserved
8:6	<b>Aux_Current (AC)</b> —RO. Reports the maximum Suspend well current required when in the D3 <sub>COLD</sub> state. Value of 000b is reported.
5	<b>Device Specific Initialization (DSI)</b> —RO. Indicates whether device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PMEC)</b> —RO. Indicates that 24-MHz clock is not required to generate PME#.
2:0	<b>Version (VS)</b> —RO. Hardwired to 011b to indicate support for <i>Revision 1.2 of the PCI Power Management Specification</i> .

### 20.3.1.19 PMCS—PCI Power Management Control and Status Register (IDER—D22:F2)

Address Offset: CC-CFh      Attribute: RO, R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:4	Reserved
3	<b>No Soft Reset (NSR)</b> —RO. 0 = Devices do perform an internal reset upon transitioning from D3hot to D0 using software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full re-initialization sequence is needed to return the device to D0 Initialized. 1 = Devices do not perform an internal reset upon transitioning from D3hot to D0. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits.
2	Reserved
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the PT function and to set a new power state. The values are: 00 = D0 state 11 = D3 <sub>HOT</sub> state When in the D3 <sub>HOT</sub> state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a '10' or '01' to these bits, the write will be ignored.



#### 20.3.1.20 MID—Message Signaled Interrupt (MSI) Capability ID Register (IDER—D22:F2)

Address Offset: D0–D1h Attribute: RO  
Default Value: 0005h Size: 16 bits

Bit	Description
15:8	<b>Next Pointer (NEXT)</b> —RO. This value indicates this is the last item in the capabilities list.
7:0	<b>Capability ID (CID)</b> —RO. The Capabilities ID value indicates device is capable of generating an MSI.

#### 20.3.1.21 MC—Message Signaled Interrupt (MSI) Message Control Register (IDER—D22:F2)

Address Offset: D2–D3h Attribute: RO, R/W  
Default Value: 0080h Size: 16 bits

Bit	Description
15:8	Reserved
7	<b>64-bit Address Capable (C64)</b> —RO. Capable of generating 64-bit and 32-bit messages.
6:4	<b>Multiple Message Enable (MME)</b> —R/W. These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	<b>Multiple Message Capable (MMC)</b> —RO. Only one message is required.
0	<b>MSI Enable (MSIE)</b> —R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

#### 20.3.1.22 MA—Message Signaled Interrupt Message Address Register (IDER—D22:F2)

Address Offset: D4–D7h Attribute: R/W  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:2	<b>Address (ADDR)</b> —R/W. This field contains the Lower 32 bits of the system specified message address, always DWord aligned
1:0	Reserved

#### 20.3.1.23 MAU—Message Signaled Interrupt Message Upper Address Register (IDER—D22:F2)

Address Offset: D8–DBh Attribute: R/W  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:4	Reserved
3:0	<b>Address (ADDR)</b> —R/W. This field contains the Upper 4 bits of the system specified message address.



### 20.3.1.24 MD—Message Signaled Interrupt (MSI) Message Data Register (IDER—D22:F2)

Address Offset: DC-DDh  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:0	<b>Data (DATA)</b> —R/W. This content is driven onto the lower word of the data bus of the MSI memory write transaction.

## 20.3.2 IDER BAR0 Registers

**Table 20-6. IDER BAR0 Register Address Map**

Address Offset	Register Symbol	Register Name	Default Value	Attribute
0h	IDEDETA	IDE Data Register	00h	R/W
1h	IDEERD1	IDE Error Register DEV1	00h	R/W
1h	IDEERD0	IDE Error Register DEV0	00h	R/W
1h	IDEFR	IDE Features Register	00h	R/W
2h	IDESCIR	IDE Sector Count In Register	00h	R/W
2h	IDESCOR1	IDE Sector Count Out Register Device 1	00h	R/W
2h	IDESCOR0	IDE Sector Count Out Register Device 0	00h	R/W
3h	IDESNOR0	IDE Sector Number Out Register Device 0	00h	R/W
3h	IDESNOR1	IDE Sector Number Out Register Device 1	00h	R/W
3h	IDESNIR	IDE Sector Number In Register	00h	R/W
4h	IDECLIR	IDE Cylinder Low In Register	00h	R/W
4h	IDCLOR1	IDE Cylinder Low Out Register Device 1	00h	R/W
4h	IDCLOR0	IDE Cylinder Low Out Register Device 0	00h	R/W
5h	IDCHOR0	IDE Cylinder High Out Register Device 0	00h	R/W
5h	IDCHOR1	IDE Cylinder High Out Register Device 1	00h	R/W
5h	IDECHIR	IDE Cylinder High In Register	00h	R/W
6h	IDEHIR	IDE Drive/Head In Register	00h	R/W
6h	IDDHOR1	IDE Drive Head Out Register Device 1	00h	R/W
6h	IDDHOR0	IDE Drive Head Out Register Device 0	00h	R/W
7h	IDESD0R	IDE Status Device 0 Register	80h	R/W
7h	IDESD1R	IDE Status Device 1 Register	80h	R/W
7h	IDECR	IDE Command Register	00h	R/W



### 20.3.2.1 IDEDATA—IDE Data Register (IDER—D22:F2)

Address Offset: 0h  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

The IDE data interface is a special interface that is implemented in the hardware. This data interface is mapped to I/O space from the host and takes read and write cycles from the host targeting master or slave device.

Writes from host to this register result in the data being written to Intel® ME memory.

Reads from host to this register result in the data being fetched from Intel® ME memory.

Data is typically written/ read in WORDs. Intel® ME firmware must enable hardware to allow it to accept Host initiated Read/ Write cycles, else the cycles are dropped.

Bit	Description
7:0	<b>IDE Data Register (IDEDR)</b> —R/W. Data Register implements the data interface for IDE. All writes and reads to this register translate into one or more corresponding write/reads to Intel® ME memory.

### 20.3.2.2 IDEERD1—IDE Error Register DEV1 (IDER—D22:F2)

Address Offset: 01h  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

This register implements the Error register of the command block of the IDE function. This register is read-only by the Host interface when DEV = 1 (slave device).

Bit	Description
7:0	<b>IDE Error Data (IDEED)</b> —R/W. Drive reflects its error/ diagnostic code to the host using this register at different times.



### 20.3.2.3 IDEERD0—IDE Error Register DEV0 (IDER—D22:F2)

Address Offset: 01h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the Error register of the command block of the IDE function. This register is read-only by the Host interface when DEV = 0 (master device).

Bit	Description
7:0	<b>IDE Error Data (IDEED)</b> —R/W. Drive reflects its error/ diagnostic code to the host using this register at different times.

### 20.3.2.4 IDEFR—IDE Features Register (IDER—D22:F2)

Address Offset: 01h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the Feature register of the command block of the IDE function. This register can be written only by the Host.

When the Host reads the same address, it reads the Error register of Device 0 or Device 1 depending on the device\_select bit—(bit 4 of the drive/head register).

Bit	Description
7:0	<b>IDE Feature Data (IDEFD)</b> —R/W. IDE drive specific data written by the Host

### 20.3.2.5 IDESCIR—IDE Sector Count In Register (IDER—D22:F2)

Address Offset: 02h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the Sector Count register of the command block of the IDE function. This register can be written only by the Host. When the host writes to this register, all three registers (IDESCR, IDESCOR0, and IDESCOR1) are updated with the written value.

A host read to this register address reads the IDE Sector Count Out Register IDESCOR0 if DEV=0 or IDESCOR1 if DEV=1.

Bit	Description
7:0	<b>IDE Sector Count Data (IDESCD)</b> —R/W. Host writes the number of sectors to be read or written.



### 20.3.2.6 IDESCOR1—IDE Sector Count Out Register Device 1 Register (IDER—D22:F2)

Address Offset: 02h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read by the HOST interface if DEV = 1. Intel® ME Firmware writes to this register at the end of a command of the selected device.

When the host writes to this address, the IDE Sector Count In Register (IDESCIR), this register is updated.

Bit	Description
7:0	<b>IDE Sector Count Out Dev1 (ISCOD1)</b> —R/W. Sector Count register for Slave Device (that is, Device 1)

### 20.3.2.7 IDESCOR0—IDE Sector Count Out Register Device 0 Register (IDER—D22:F2)

Address Offset: 02h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read by the HOST interface if DEV = 0. Intel® ME Firmware writes to this register at the end of a command of the selected device.

When the host writes to this address, the IDE Sector Count In Register (IDESCIR), this register is updated.

Bit	Description
7:0	<b>IDE Sector Count Out Dev0 (ISCOD0)</b> —R/W. Sector Count register for Master Device (that is, Device 0).

### 20.3.2.8 IDESNOR0—IDE Sector Number Out Register Device 0 Register (IDER—D22:F2)

Address Offset: 03h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read by the Host if DEV = 0. Intel® ME Firmware writes to this register at the end of a command of the selected device.

When the host writes to the IDE Sector Number In Register (IDESNIR), this register is updated with that value.

Bit	Description
7:0	<b>IDE Sector Number Out DEV 0 (IDESNO0)</b> —R/W. Sector Number Out register for Master device.



### 20.3.2.9 IDESNOR1—IDE Sector Number Out Register Device 1 Register (IDER—D22:F2)

Address Offset: 03h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read by the Host if DEV = 1. Intel® ME Firmware writes to this register at the end of a command of the selected device.

When the host writes to the IDE Sector Number In Register (IDESNIR), this register is updated with that value.

Bit	Description
7:0	<b>IDE Sector Number Out DEV 1 (IDESNO1)</b> —R/W. Sector Number Out register for Slave device.

### 20.3.2.10 IDESNIR—IDE Sector Number In Register (IDER—D22:F2)

Address Offset: 03h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the Sector Number register of the command block of the IDE function. This register can be written only by the Host. When the host writes to this register, all three registers (IDESNIR, IDESNOR0, IDESNOR1) are updated with the written value.

Host read to this register address reads the IDE Sector Number Out Register IDESNOR0 if DEV=0 or IDESNOR1 if DEV=1.

Bit	Description
7:0	<b>IDE Sector Number Data (IDESND)</b> —R/W. This register contains the number of the first sector to be transferred.

### 20.3.2.11 IDECLIR—IDE Cylinder Low In Register (IDER—D22:F2)

Address Offset: 04h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the Cylinder Low register of the command block of the IDE function. This register can be written only by the Host. When the host writes to this register, all three registers (IDECLIR, IDECLOR0, IDECLOR1) are updated with the written value.

Host read to this register address reads the IDE Cylinder Low Out Register IDECLOR0 if DEV=0 or IDECLOR1 if DEV=1.

Bit	Description
7:0	<b>IDE Cylinder Low Data (IDECLD)</b> —R/W. Cylinder Low register of the command block of the IDE function.



### 20.3.2.12 IDCLOR1—IDE Cylinder Low Out Register Device 1 Register (IDER—D22:F2)

Address Offset: 04h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read by the Host if DEV = 1. Intel® ME Firmware writes to this register at the end of a command of the selected device. When the host writes to the IDE Cylinder Low In Register (IDECLIR), this register is updated with that value.

Bit	Description
7:0	<b>IDE Cylinder Low Out DEV 1. (IDECLO1)</b> —R/W. Cylinder Low Out Register for Slave Device.

### 20.3.2.13 IDCLOR0—IDE Cylinder Low Out Register Device 0 Register (IDER—D22:F2)

Address Offset: 04h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read by the Host if DEV = 0. Intel® ME Firmware writes to this register at the end of a command of the selected device. When the host writes to the IDE Cylinder Low In Register (IDECLIR), this register is updated with that value.

Bit	Description
7:0	<b>IDE Cylinder Low Out DEV 0. (IDECLO0)</b> —R/W. Cylinder Low Out Register for Master Device.

### 20.3.2.14 IDCHOR0—IDE Cylinder High Out Register Device 0 Register (IDER—D22:F2)

Address Offset: 05h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read by the Host if Device = 0. Intel® ME Firmware writes to this register at the end of a command of the selected device. When the host writes to the IDE Cylinder High In Register (IDECHIR), this register is updated with that value.

Bit	Description
7:0	<b>IDE Cylinder High Out DEV 0 (IDECHO0)</b> —R/W. Cylinder High out register for Master device.



### 20.3.2.15 IDCHOR1—IDE Cylinder High Out Register Device 1 Register (IDER—D22:F2)

Address Offset: 05h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read by the Host if Device = 1. Intel® ME Firmware writes to this register at the end of a command of the selected device. When the host writes to the IDE Cylinder High In Register (IDECHIR), this register is updated with that value.

Bit	Description
7:0	<b>IDE Cylinder High Out DEV 1 (IDECHO1)</b> —R/W. Cylinder High out register for Slave device.

### 20.3.2.16 IDECHIR—IDE Cylinder High In Register (IDER—D22:F2)

Address Offset: 05h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the Cylinder High register of the command block of the IDE function. This register can be written only by the Host. When the host writes to this register, all three registers (IDECHIR, IDECHOR0, IDECHOR1) are updated with the written value.

Host read to this register address reads the IDE Cylinder High Out Register IDECHOR0 if DEV=0 or IDECHOR1 if DEV=1.

Bit	Description
7:0	<b>IDE Cylinder High Data (IDECHD)</b> —R/W. Cylinder High data register for IDE command block.

### 20.3.2.17 IDEDHIR—IDE Drive/Head In Register (IDER—D22:F2)

Address Offset: 06h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the Drive/Head register of the command block of the IDE. This register can be written only by the Host. When the host writes to this register, all three registers (IDEDHIR, IDEDHOR0, IDEDHOR1) are updated with the written value.

Host read to this register address reads the IDE Drive/Head Out Register (IDEDHOR0) if DEV=0 or IDEDHOR1 if DEV=1.

Bit 4 of this register is the DEV (master/slave) bit. This bit is cleared by hardware on IDE software reset (S\_RST toggles to '1') in addition to Host system reset and D3->D0 transition of the function.

Bit	Description
7:0	<b>IDE Drive/Head Data (IDEDHD)</b> —R/W. Register defines the drive number, head number, and addressing mode.



### 20.3.2.18 IDDHOR1—IDE Drive Head Out Register Device 1 Register (IDER—D22:F2)

Address Offset: 06h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read only by the Host. Host read to this Drive/head In register address reads the IDE Drive/Head Out Register (IDEDHOR0) if DEV=1

Bit 4 of this register is the DEV (master/slave) bit. This bit is cleared by hardware on IDE software reset (S\_RST toggles to '1') in addition to the Host system reset and D3 to D0 transition of the IDE function.

When the host writes to this address, it updates the value of the IDEDHIR register.

Bit	Description
7:0	<b>IDE Drive Head Out DEV 1 (IDEDHO1)</b> —R/W. Drive/Head Out register of Slave device.

### 20.3.2.19 IDDHOR0—IDE Drive Head Out Register Device 0 Register (IDER—D22:F2)

Address Offset: 06h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register is read only by the Host. Host read to this Drive/head In register address reads the IDE Drive/Head Out Register (IDEDHOR0) if DEV=0.

Bit 4 of this register is the DEV (master/slave) bit. This bit is cleared by hardware on IDE software reset (S\_RST toggles to 1) in addition to the Host system reset and D3 to D0 transition of the IDE function.

When the host writes to this address, it updates the value of the IDEDHIR register.

Bit	Description
7:0	<b>IDE Drive Head Out DEV 0 (IDEDHO0)</b> —R/W. Drive/Head Out register of Master device.



### 20.3.2.20 IDESD0R—IDE Status Device 0 Register (IDER—D22:F2)

Address Offset: 07h  
Default Value: 80h

Attribute: R/W  
Size: 8 bits

This register implements the status register of the Master device (DEV = 0). This register is read-only by the Host. Host read of this register clears the Master device's interrupt.

When the HOST writes to the same address, it writes to the command register.

The bits description is for ATA mode.

Bit	Description
7	<b>Busy (BSY)</b> —R/W. This bit is set by hardware when the IDECR is being written and DEV=0, or when SRST bit is asserted by Host or host system reset or D3-to-D0 transition of the IDE function. This bit is cleared by firmware write of 0.
6	<b>Drive Ready (DRDY)</b> —R/W. When set, this bit indicates drive is ready for command.
5	<b>Drive Fault (DF)</b> —R/W. Indicates Error on the drive.
4	<b>Drive Seek Complete (DSC)</b> —R/W. Indicates Heads are positioned over the desired cylinder.
3	<b>Data Request (DRQ)</b> —R/W. Set when, the drive wants to exchange data with the Host using the data register.
2	<b>Corrected Data (CORR)</b> —R/W. When set, this bit indicates a correctable read error has occurred.
1	<b>Index (IDX)</b> —R/W. This bit is set once per rotation of the medium when the index mark passes under the read/write head.
0	<b>Error (ERR)</b> —R/W. When set, this bit indicates an error occurred in the process of executing the previous command. The Error register of the selected device contains the error information.



### 20.3.2.21 IDESD1R—IDE Status Device 1 Register (IDER—D22:F2)

Address Offset: 07h Attribute: R/W  
Default Value: 80h Size: 8 bits

This register implements the status register of the slave device (DEV = 1). This register is read-only by the Host. Host read of this register clears the slave device's interrupt.

When the Host writes to the same address, it writes to the command register.

The bits description is for ATA mode.

Bit	Description
7	<b>Busy (BSY)</b> —R/W. This bit is set by hardware when the IDECR is being written and DEV=0, or when SRST bit is asserted by the Host or host system reset or D3-to-D0 transition of the IDE function. This bit is cleared by firmware write of 0.
6	<b>Drive Ready (DRDY)</b> —R/W. When set, indicates drive is ready for command.
5	<b>Drive Fault (DF)</b> —R/W. Indicates Error on the drive.
4	<b>Drive Seek Complete (DSC)</b> —R/W. Indicates Heads are positioned over the desired cylinder.
3	<b>Data Request (DRQ)</b> —R/W. Set when the drive wants to exchange data with the Host using the data register.
2	<b>Corrected Data (CORR)</b> —R/W. When set indicates a correctable read error has occurred.
1	<b>Index (IDX)</b> —R/W. This bit is set once per rotation of the medium when the index mark passes under the read/write head.
0	<b>Error (ERR)</b> —R/W. When set, this bit indicates an error occurred in the process of executing the previous command. The Error Register of the selected device contains the error information

### 20.3.2.22 IDECR—IDE Command Register (IDER—D22:F2)

Address Offset: 07h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the Command register of the command block of the IDE function. This register can be written only by the Host.

When the Host reads the same address, it reads the Status register DEV0 if DEV=0 or Status Register DEV1 if DEV=1 (Drive/Head register bit [4]).

Bit	Description
7:0	<b>IDE Command Data (IDECD)</b> —R/W. Host sends the commands (read/ write, and so forth) to the drive using this register.



### 20.3.3 IDER BAR1 Registers

**Table 20-7. IDER BAR1 Register Address Map**

Address Offset	Register Symbol	Register Name	Default Value	Attribute
2h	IDDCR	IDE Device Control Register	00h	RO, WO
2h	IDASR	IDE Alternate status Register	00h	RO

#### 20.3.3.1 IDDCR—IDE Device Control Register (IDER—D22:F2)

Address Offset: 2h Attribute: WO  
Default Value: 00h Size: 8 bits

This register implements the Device Control register of the Control block of the IDE function. This register is write only by the Host.

When the Host reads to the same address, it reads the Alternate Status register.

Bit	Description
7:3	Reserved
2	<b>Software reset (S_RST)</b> —WO. When this bit is set by the Host, it forces a reset to the device.
1	<b>Host interrupt Disable (nIEN)</b> —WO. When set, this bit disables hardware from sending interrupt to the Host.
0	Reserved

#### 20.3.3.2 IDASR—IDE Alternate Status Register (IDER—D22:F2)

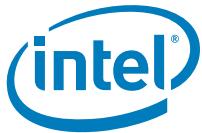
Address Offset: 2h Attribute: RO  
Default Value: 00h Size: 8 bits

This register implements the Alternate Status register of the Control block of the IDE function. This register is a mirror register to the status register in the command block. Reading this register by the Host does not clear the IDE interrupt of the DEV selected device.

Host read of this register when DEV=0 (Master); Host gets the mirrored data of IDESD0R register.

Host read of this register when DEV=1 (Slave); host gets the mirrored data of IDESD1R register.

Bit	Description
7:0	<b>IDE Alternate Status Register (IDEASR)</b> —RO. This field mirrors the value of the DEV0/ DEV1 status register, depending on the state of the DEV bit on Host reads.



## 20.3.4 IDER BAR4 Registers

Table 20-8. IDER BAR4 Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Attribute
0h	IDEPBMR	IDE Primary Bus Master Command Register	00h	RO, R/W
1h	IDEPBMDS0R	IDE Primary Bus Master Device Specific 0 Register	00h	R/W
2h	IDEPBMSR	IDE Primary Bus Master Status Register	80h	RO, R/W
3h	IDEPBMDS1R	IDE Primary Bus Master Device Specific 1 Register	00h	R/W
4h	IDEPBMDTPR0	IDE Primary Bus Master Descriptor Table Pointer Register Byte 0	00h	R/W
5h	IDEPBMDTPR1	IDE Primary Bus Master Descriptor Table Pointer Register Byte 1	00h	R/W
6h	IDEPBMDTPR2	IDE Primary Bus Master Descriptor Table Pointer Register Byte 2	00h	R/W
7h	IDEPBMDTPR3	IDE Primary Bus Master Descriptor Table Pointer Register Byte 3	00h	R/W
8h	IDESBMR	IDE Secondary Bus Master Command Register	00h	RO, R/W
9h	IDESBMDS0R	IDE Secondary Bus Master Device Specific 0 Register	00h	R/W
Ah	IDESBMSR	IDE Secondary Bus Master Status Register	00h	R/W, RO
Bh	IDESBMDS1R	IDE Secondary Bus Master Device Specific 1 Register	00h	R/W
Ch	IDESBMDTPR0	IDE Secondary Bus Master Descriptor Table Pointer Register Byte 0	00h	R/W
Dh	IDESBMDTPR1	IDE Secondary Bus Master Descriptor Table Pointer Register Byte 1	00h	R/W
Eh	IDESBMDTPR2	IDE Secondary Bus Master Descriptor Table Pointer Register Byte 2	00h	R/W
Fh	IDESBMDTPR3	IDE Secondary Bus Master Descriptor Table Pointer Register Byte 3	00h	R/W



#### 20.3.4.1 IDEPBMCR—IDE Primary Bus Master Command Register (IDER—D22:F2)

Address Offset: 00h Attribute: R/W  
 Default Value: 00h Size: 8 bits

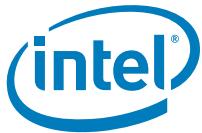
This register implements the bus master command register of the primary channel. This register is programmed by the Host.

Bit	Description
7:4	Reserved
3	<b>Read Write Command (RWC)</b> —R/W. This bit sets the direction of bus master transfer. 0 = Reads are performed from system memory 1 = Writes are performed to System Memory. This bit should not be changed when the bus master function is active.
2:1	Reserved
0	<b>Start/Stop Bus Master (SSBM)</b> —R/W. This bit gates the bus master operation of IDE function when 0. Writing 1 enables the bus master operation. Bus master operation can be halted by writing a 0 to this bit. Operation cannot be stopped and resumed. This bit is cleared after data transfer is complete as indicated by either the BMIA bit or the INT bit of the Bus Master status register is set or both are set.

#### 20.3.4.2 IDEPBMD0R—IDE Primary Bus Master Device Specific 0 Register (IDER—D22:F2)

Address Offset: 01h Attribute: R/W  
 Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Device Specific Data0 (DSD0)</b> —R/W. Device Specific



#### 20.3.4.3 IDEPBMSR—IDE Primary Bus Master Status Register (IDER—D22:F2)

Address Offset: 02h Attribute: RO, R/W  
Default Value: 80h Size: 8 bits

Bit	Description
7	<b>Simplex Only (SO)</b> —RO. Value indicates whether both Bus Master Channels can be operated at the same time or not. 0 = Both can be operated independently 1 = Only one can be operated at a time.
6	<b>Drive 1 DMA Capable (D1DC)</b> —R/W. This bit is read/write by the host (not write 1 clear).
5	<b>Drive 0 DMA Capable (D0DC)</b> —R/W. This bit is read/write by the host (not write 1 clear).
4:3	Reserved
2	<b>Interrupt (INT)</b> —R/W. This bit is set by the hardware when it detects a positive transition in the interrupt logic. The hardware will clear this bit when the Host software writes 1 to it.
1	<b>Error (ER)</b> —R/W. Bit is typically set by firmware. Hardware will clear this bit when the Host software writes 1 to it.
0	<b>Bus Master IDE Active (BMIA)</b> —RO. This bit is set by hardware when SSBM register is set to 1 by the Host. When the bus master operation ends (for the whole command) this bit is cleared by firmware. This bit is not cleared when the HOST writes 1 to it.

#### 20.3.4.4 IDEPBMDS1R—IDE Primary Bus Master Device Specific 1 Register (IDER—D22:F2)

Address Offset: 03h Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Device Specific Data1 (DSD1)</b> —R/W. Device Specific Data

#### 20.3.4.5 IDEPBMDTPRO—IDE Primary Bus Master Descriptor Table Pointer Byte 0 Register (IDER—D22:F2)

Address Offset: 04h Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Descriptor Table Pointer Byte 0 (DTPBO)</b> —R/W. This register implements the Byte 0 (1 of 4 bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the primary channel. This register is read/write by the HOST interface.



#### 20.3.4.6 IDEPBMDTPR1—IDE Primary Bus Master Descriptor Table Pointer Byte 1 Register (IDER—D22:F2)

Address Offset: 05h Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Descriptor Table Pointer Byte 1 (DTPB1)</b> —R/W. This register implements the Byte 1 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the primary channel. This register is programmed by the Host.

#### 20.3.4.7 IDEPBMDTPR2—IDE Primary Bus Master Descriptor Table Pointer Byte 2 Register (IDER—D22:F2)

Address Offset: 06h Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Descriptor Table Pointer Byte 2 (DTPB2)</b> —R/W. This register implements the Byte 2 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the primary channel. This register is programmed by the Host.

#### 20.3.4.8 IDEPBMDTPR3—IDE Primary Bus Master Descriptor Table Pointer Byte 3 Register (IDER—D22:F2)

Address Offset: 07h Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Descriptor Table Pointer Byte 3 (DTPB3)</b> —R/W. This register implements the Byte 3 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the primary channel. This register is programmed by the Host.

#### 20.3.4.9 IDESBMCR—IDE Secondary Bus Master Command Register (IDER—D22:F2)

Address Offset: 08h Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:4	Reserved
3	<b>Read Write Command (RWC)</b> —R/W. This bit sets the direction of bus master transfer. When 0, reads are performed from system memory; when 1, writes are performed to system memory. This bit should not be changed when the bus master function is active.
2:1	Reserved
0	<b>Start/Stop Bus Master (SSBM)</b> —R/W. This bit gates the bus master operation of IDE function when zero. Writing 1 enables the bus master operation. Bus master operation can be halted by writing a 0 to this bit. Operation cannot be stopped and resumed. This bit is cleared after data transfer is complete as indicated by either the BMIA bit or the INT bit of the Bus Master status register is set or both are set.



#### 20.3.4.10 IDESBMDS0R—IDE Secondary Bus Master Device Specific 0 Register (IDER—D22:F2)

Address Offset: 09h Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Device Specific Data0 (DSD0)</b> —R/W. This register implements the bus master Device Specific 1 register of the secondary channel. This register is programmed by the Host.

#### 20.3.4.11 IDESBMSR—IDE Secondary Bus Master Status Register (IDER—D22:F2)

Address Offset: 0Ah Attribute: R/W  
Default Value: 80h Size: 8 bits

Bit	Description
7	<b>Simplex Only (SO)</b> —R/W. This bit indicates whether both Bus Master Channels can be operated at the same time or not. 0 = Both can be operated independently 1 = Only one can be operated at a time.
6	<b>Drive 1 DMA Capable (D1DC)</b> —R/W. This bit is read/write by the host.
5	<b>Drive 0 DMA Capable (D0DC)</b> —R/W. This bit is read/write by the host.
4:0	Reserved

#### 20.3.4.12 IDESBMDS1R—IDE Secondary Bus Master Device Specific 1 Register (IDER—D22:F2)

Address Offset: 0Bh Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Device Specific Data1 (DSD1)</b> —R/W. This register implements the bus master Device Specific 1 register of the secondary channel. This register is programmed by the Host for device specific data if any.

#### 20.3.4.13 IDESBMDTPR0—IDE Secondary Bus Master Descriptor Table Pointer Byte 0 Register (IDER—D22:F2)

Address Offset: 0Ch Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Descriptor Table Pointer Byte 0 (DTPB0)</b> —R/W. This register implements the Byte 0 (1 of 4 bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the secondary channel. This register is read/write by the HOST interface.

#### 20.3.4.14 IDESBMDTPR1—IDE Secondary Bus Master Descriptor Table Pointer Byte 1 Register (IDER—D22:F2)

Address Offset: 0Dh Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Descriptor Table Pointer Byte 1 (DTPB1)</b> —R/W. This register implements the Byte 1 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the secondary channel. This register is programmed by the Host.

#### 20.3.4.15 IDESBMDPTR2—IDE Secondary Bus Master Descriptor Table Pointer Byte 2 Register (IDER—D22:F2)

Address Offset: 0Eh Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Descriptor Table Pointer Byte 2 (DTPB2)</b> —R/W. This register implements the Byte 2 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the secondary channel. This register is programmed by the Host.

### 20.3.4.16 IDESBMDPTR3—IDE Secondary Bus Master Descriptor Table Pointer Byte 3 Register (IDER—D22:F2)

Address Offset: 0Fh Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Descriptor Table Pointer Byte 3 (DTPB3)</b> —R/W. This register implements the Byte 3 (of four bytes) of the descriptor table Pointer (four I/O byte addresses) for bus master operation of the secondary channel. This register is programmed by the Host.

## 20.4 Serial Port for Remote Keyboard and Text (KT) Redirection (KT—D22:F3)

### 20.4.1 PCI Configuration Registers (KT—D22:F3)

**Table 20-9. Serial Port for Remote Keyboard and Text (KT) Redirection Register Address Map**

Address Offset	Register Symbol	Register Name	Default Value	Attribute
00h-01h	VID	Vendor Identification	8086h	RO
02h-03h	DID	Device Identification	See Register description	RO
04h-05h	CMD	Command Register	0000h	RO, R/W
06h-07h	STS	Device Status	00B0h	RO
08h	RID	Revision ID	See Register description	RO
09h-0Bh	CC	Class Codes	070002h	RO
0Ch	CLS	Cache Line Size	00h	RO
10h-13h	KTIBA	KT I/O Block Base Address	00000001h	RO, R/W
14h-17h	KTMBA	KT Memory Block Base Address	00000000h	RO, R/W
2Ch-2Dh	SVID	Subsystem Vendor ID	0000h	R/WO
2Eh-2Fh	SID	Subsystem ID	8086h	R/WO
34h	CAP	Capabilities Pointer	C8h	RO
3Ch-3Dh	INTR	Interrupt Information	0200h	R/W, RO
C8h-C9h	PID	PCI Power Management Capability ID	D001h	RO
CAh-CBh	PC	PCI Power Management Capabilities	0023h	RO
D0h-D1h	MID	Message Signaled Interrupt Capability ID	0005h	RO
D2h-D3h	MC	Message Signaled Interrupt Message Control	0080h	RO, R/W
D4h-D7h	MA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
D8h-DBh	MAU	Message Signaled Interrupt Message Upper Address	00000000h	RO, R/W
DCh-DDh	MD	Message Signaled Interrupt Message Data	0000h	R/W



#### 20.4.1.1 VID—Vendor Identification Register (KT—D22:F3)

Address Offset: 00–01h Attribute: RO  
Default Value: 8086h Size: 16 bits

Bit	Description
15:0	<b>Vendor ID (VID)</b> —RO. This is a 16-bit value assigned by Intel.

#### 20.4.1.2 DID—Device Identification Register (KT—D22:F3)

Address Offset: 02–03h Attribute: RO  
Default Value: See bit description Size: 16 bits

Bit	Description
15:0	<b>Device ID (DID)</b> —RO. This is a 16-bit value assigned to the PCH KT controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

#### 20.4.1.3 CMD—Command Register (KT—D22:F3)

Address Offset: 04–05h Attribute: R/W  
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable (ID)</b> —R/W. This bit disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 1 = Internal INTx# messages will not be generated. 0 = Internal INTx# messages are generated if there is an interrupt <b>and</b> MSI is not enabled.
9:3	Reserved
2	<b>Bus Master Enable (BME)</b> —R/W. This bit controls the KT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands. For KT, the only bus mastering activity is MSI generation.
1	<b>Memory Space Enable (MSE)</b> —R/W. This bit controls Access to the PT function's target memory space.
0	<b>I/O Space enable (IOSE)</b> —R/W. This bit controls access to the PT function's target I/O space.



#### 20.4.1.4 STS—Device Status Register (KT—D22:F3)

Address Offset: 06–07h Attribute: RO  
Default Value: 00B0h Size: 16 bits

Bit	Description
15:11	Reserved
10:9	<b>DEVSEL# Timing Status (DEVT)</b> —RO. This field controls the device select time for the PT function's PCI interface.
8:5	Reserved
4	<b>Capabilities List (CL)</b> —RO. This bit indicates that there is a capabilities pointer implemented in the device.
3	<b>Interrupt Status (IS)</b> —RO. This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTB interrupt asserted to the Host.
2:0	Reserved

#### 20.4.1.5 RID—Revision ID Register (KT—D22:F3)

Address Offset: 08h Attribute: RO  
Default Value: See bit description Size: 8 bits

Bit	Description
7:0	<b>Revision ID</b> —RO. See Section 1.4 for the value of the RID Register.

#### 20.4.1.6 CC—Class Codes Register (KT—D22:F3)

Address Offset: 09–0Bh Attribute: RO  
Default Value: 070002h Size: 24 bits

Bit	Description
23:16	<b>Base Class Code (BCC)</b> —RO. This field indicates the base class code of the KT host controller device.
15:8	<b>Sub Class Code (SCC)</b> —RO. This field indicates the sub class code of the KT host controller device.
7:0	<b>Programming Interface (PI)</b> —RO. This field indicates the programming interface of the KT host controller device.



#### 20.4.1.7 CLS—Cache Line Size Register (KT—D22:F3)

Address Offset: 0Ch Attribute: RO  
Default Value: 00h Size: 8 bits

This register defines the system cache line size in DWord increments. Mandatory for master that use the Memory-Write and Invalidate command.

Bit	Description
7:0	<b>Cache Line Size (CLS)</b> —RO. All writes to system memory are Memory Writes.

#### 20.4.1.8 KTIBA—KT I/O Block Base Address Register (KT—D22:F3)

Address Offset: 10–13h Attribute: RO, R/W  
Default Value: 00000001h Size: 32 bits

Bit	Description
31:16	Reserved
15:3	<b>Base Address (BAR)</b> —R/W. This field provides the base address of the I/O space (8 consecutive I/O locations).
2:1	Reserved
0	<b>Resource Type Indicator (RTE)</b> —RO. This bit indicates a request for I/O space

#### 20.4.1.9 KTMBA—KT Memory Block Base Address Register (KT—D22:F3)

Address Offset: 14–17h Attribute: RO, R/W  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:12	<b>Base Address (BAR)</b> —R/W. This field provides the base address for Memory Mapped I/O BAR. Bits 31:12 correspond to address signals 31:12.
11:4	Reserved
3	<b>Prefetchable (PF)</b> —RO. This bit indicates that this range is not prefetchable.
2:1	<b>Type (TP)</b> —RO. This field indicates that this range can be mapped anywhere in 32-bit address space.
0	<b>Resource Type Indicator (RTE)</b> —RO. This bit indicates a request for register memory space.



#### 20.4.1.10 SVID—Subsystem Vendor ID Register (KT—D22:F3)

Address Offset: 2Ch–2Dh      Attribute: R/WO  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (SSVID)</b> —R/WO. Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes read-only. This field can only be cleared by PLTRST#. <b>Note:</b> Register must be written as a DWord write with SVID register.

#### 20.4.1.11 SID—Subsystem ID Register (KT—D22:F3)

Address Offset: 2Eh–2Fh      Attribute: R/WO  
Default Value: 8086h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (SSID)</b> —R/WO. Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes read-only. This field can only be cleared by PLTRST#. <b>Note:</b> Register must be written as a DWord write with SVID register.

#### 20.4.1.12 CAP—Capabilities Pointer Register (KT—D22:F3)

Address Offset: 34h      Attribute: RO  
Default Value: C8h      Size: 8 bits

This optional register is used to point to a linked list of new capabilities implemented by the device.

Bit	Description
7:0	<b>Capability Pointer (CP)</b> —RO. This field indicates that the first capability pointer is offset C8h (the power management capability).

#### 20.4.1.13 INTR—Interrupt Information Register (KT—D22:F3)

Address Offset: 3C–3Dh      Attribute: R/W, RO  
Default Value: 0200h      Size: 16 bits

Bit	Description
15:8	<b>Interrupt Pin (IPIN)</b> —RO. A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. The upper 4 bits are hardwired to 0 and the lower 4 bits are programmed by the KTIP bits (RCBA+3124:bits 15:12).
7:0	<b>Interrupt Line (ILINE)</b> —R/W. The value written in this register tells which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the operating system and the device driver, and has no affect on the hardware.



#### 20.4.1.14 PID—PCI Power Management Capability ID Register (KT—D22:F3)

Address Offset: C8—C9h      Attribute: RO  
 Default Value: D001h      Size: 16 bits

Bit	Description
15:8	<b>Next Capability (NEXT)</b> —RO. A value of D0h points to the MSI capability.
7:0	<b>Cap ID (CID)</b> —RO. This field indicates that this pointer is a PCI power management.

#### 20.4.1.15 PC—PCI Power Management Capabilities ID Register (KT—D22:F3)

Address Offset: CA—CBh      Attribute: RO  
 Default Value: 0023h      Size: 16 bits

Bit	Description
15:11	<b>PME Support (PME)</b> —RO. This field indicates no PME# in the PT function.
10:6	Reserved
5	<b>Device Specific Initialization (DSI)</b> —RO. This bit indicates that no device-specific initialization is required.
4	Reserved
3	<b>PME Clock (PMEC)</b> —RO. This bit indicates that 24-MHz clock is not required to generate PME#
2:0	<b>Version (VS)</b> —RO. This field indicates support for the <i>PCI Power Management Specification, Revision 1.2</i> .



#### 20.4.1.16 MID—Message Signaled Interrupt (MSI) Capability ID Register (KT—D22:F3)

Address Offset: D0–D1h Attribute: RO  
Default Value: 0005h Size: 16 bits

Message Signaled Interrupt is a feature that allows the device/function to generate an interrupt to the host by performing a DWord memory write to a system specified address with system specified data. This register is used to identify and configure an MSI capable device.

Bit	Description
15:8	<b>Next Pointer (NEXT)</b> —RO. This value indicates this is the last item in the list.
7:0	<b>Capability ID (CID)</b> —RO. This field value of Capabilities ID indicates device is capable of generating MSI.

#### 20.4.1.17 MC—Message Signaled Interrupt (MSI) Message Control Register (KT—D22:F3)

Address Offset: D2–D3h Attribute: RO, R/W  
Default Value: 0080h Size: 16 bits

Bit	Description
15:8	Reserved
7	<b>64-bit Address Capable (C64)</b> —RO. Capable of generating 64-bit and 32-bit messages.
6:4	<b>Multiple Message Enable (MME)</b> —R/W. These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	<b>Multiple Message Capable (MMC)</b> —RO. Only one message is required.
0	<b>MSI Enable (MSIE)</b> —R/W. If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

#### 20.4.1.18 MA—Message Signaled Interrupt (MSI) Message Address Register (KT—D22:F3)

Address Offset: D4–D7h Attribute: R/W  
Default Value: 00000000h Size: 32 bits

This register specifies the DWord aligned address programmed by system software for sending MSI.

Bit	Description
31:2	<b>Address (ADDR)</b> —R/W. Lower 32 bits of the system specified message address; always DWord aligned.
1:0	Reserved



#### 20.4.1.19 MAU—Message Signaled Interrupt Message Upper Address Register (KT—D22:F3)

Address Offset: D8–DBh      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:4	Reserved
3:0	<b>Address (ADDR)</b> —R/W. Upper 4 bits of the system specified message address.

#### 20.4.1.20 MD—Message Signaled Interrupt (MSI) Message Data Register (KT—D22:F3)

Address Offset: DC–DDh      Attribute: R/W  
 Default Value: 0000h      Size: 16 bits

This 16-bit field is programmed by system software if MSI is enabled.

Bit	Description
15:0	<b>Data (DATA)</b> —R/W. This MSI data is driven onto the lower word of the data bus of the MSI memory write transaction.

### 20.4.2 KT I/O Memory Mapped Device Registers

**Table 20-10. KT I/O Memory Mapped Device Register Address Map**

Address Offset	Register Symbol	Register Name	Default Value	Attribute
0h	KTRxBR	KT Receive Buffer Register	00h	RO
0h	KTTHR	KT Transmit Holding Register	00h	WO
0h	KTDLLR	KT Divisor Latch LSB Register	00h	R/W
1h	KTIER	KT Interrupt Enable register	00h	R/W, RO
1h	KTDLMR	KT Divisor Latch MSB Register	00h	R/W
2h	KTIIR	KT Interrupt Identification register	01h	RO
2h	KTFCR	KT FIFO Control register	00h	WO
3h	KTLCR	KT Line Control register	03h	R/W
4h	KTMCR	KT Modem Control register	00h	RO, R/W
5h	KTLSR	KT Line Status register	00h	RO
6h	KTMSR	KT Modem Status register	00h	RO



#### 20.4.2.1 KTRxBR—KT Receive Buffer Register (KT—D22:F3)

Address Offset: 00h Attribute: RO  
Default Value: 00h Size: 8 bits

This register implements the KT Receiver Data register. Host access to this address, depends on the state of the DLAB bit (KTLCR[7]). It must be 0 to access the KTRxBR.

##### RxBR

Host reads this register when firmware provides it the receive data in non-FIFO mode. In FIFO mode, host reads to this register translate into a read from Intel® ME memory (RBR FIFO).

Bit	Description
7:0	<b>Receiver Buffer Register (RBR)</b> —RO. Implements the Data register of the Serial Interface. If the Host does a read, it reads from the Receive Data Buffer.

#### 20.4.2.2 KTTHR—KT Transmit Holding Register (KT—D22:F3)

Address Offset: 00h Attribute: WO  
Default Value: 00h Size: 8 bits

This register implements the KT Transmit Data register. Host access to this address, depends on the state of the DLAB bit (KTLCR[7]). It must be 0 to access the KTTHR.

##### THR

When host wants to transmit data in the non-FIFO mode, it writes to this register. In FIFO mode, writes by host to this address cause the data byte to be written by hardware to Intel® ME memory (THR FIFO).

Bit	Description
7:0	<b>Transmit Holding Register (THR)</b> —WO. Implements the Transmit Data register of the Serial Interface. If the Host does a write, it writes to the Transmit Holding Register.

#### 20.4.2.3 KTDLLR—KT Divisor Latch LSB Register (KT—D22:F3)

Address Offset: 00h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the KT DLL register. Host can Read/Write to this register only when the DLAB bit (KTLCR[7]) is 1. When this bit is 0, Host accesses the KTTHR or the KTRBR depending on Read or Write.

This is the standard Serial Port Divisor Latch register. This register is only for software compatibility and does not affect performance of the hardware.

Bit	Description
7:0	<b>Divisor Latch LSB (DLL)</b> —R/W. Implements the DLL register of the Serial Interface.



#### 20.4.2.4 KTIER—KT Interrupt Enable Register (KT—D22:F3)

Address Offset: 01h Attribute: R/W  
Default Value: 00h Size: 8 bits

This register implements the KT Interrupt Enable register. Host access to this address, depends on the state of the DLAB bit (KTLCR[7]). It must be '0' to access this register. The bits enable specific events to interrupt the Host.

Bit	Description
7:4	Reserved
3	<b>MSR (IER2)</b> —R/W. When set, this bit enables bits in the Modem Status register to cause an interrupt to the host.
2	<b>LSR (IER1)</b> —R/W. When set, this bit enables bits in the Receiver Line Status register to cause an interrupt to the Host.
1	<b>THR (IER1)</b> —R/W. When set, this bit enables an interrupt to be sent to the Host when the transmit Holding register is empty.
0	<b>DR (IER0)</b> —R/W. When set, the Received Data Ready (or Receive FIFO Timeout) interrupts are enabled to be sent to Host.

#### 20.4.2.5 KTDLMR—KT Divisor Latch MSB Register (KT—D22:F3)

Address Offset: 01h Attribute: R/W  
Default Value: 00h Size: 8 bits

Host can Read/Write to this register only when the DLAB bit (KTLCR[7]) is 1. When this bit is 0, Host accesses the KTIER.

This is the standard Serial interface's Divisor Latch register's MSB. This register is only for software compatibility and does not affect performance of the hardware.

Bit	Description
7:0	<b>Divisor Latch MSB (DLM)</b> —R/W. Implements the Divisor Latch MSB register of the Serial Interface.

#### 20.4.2.6 KTIIR—KT Interrupt Identification Register (KT—D22:F3)

Address Offset: 02h Attribute: RO  
Default Value: 00h Size: 8 bits

The KT IIR register prioritizes the interrupts from the function into 4 levels and records them in the IIR\_STAT field of the register. When Host accesses the IIR, hardware freezes all interrupts and provides the priority to the Host. Hardware continues to monitor the interrupts but does not change its current indication until the Host read is over. Table in the Host Interrupt Generation section shows the contents.

Bit	Description
7	<b>FIFO Enable (FIEN1)</b> —RO. This bit is connected by hardware to bit 0 in the FCR register.
6	<b>FIFO Enable (FIENO)</b> —RO. This bit is connected by hardware to bit 0 in the FCR register.
5:4	Reserved

Bit	Description
3:1	<b>IIR STATUS (IIRSTS)</b> —RO. These bits are asserted by the hardware according to the source of the interrupt and the priority level.
0	<b>Interrupt Status (INTSTS)</b> —RO. 0 = Pending interrupt to Host 1 = No pending interrupt to Host

### 20.4.2.7 KTFCR—KT FIFO Control Register (KT—D22:F3)

Address Offset: 02h Attribute: WO  
Default Value: 00h Size: 8 bits

When Host writes to this address, it writes to the KTFCR. The FIFO Control register of the serial interface is used to enable the FIFOs, set the receiver FIFO trigger level, and clear FIFOs under the direction of the Host.

When Host reads from this address, it reads the KTIIR.

Bit	Description
7:6	<b>Receiver Trigger Level (RTL)</b> —WO. Trigger level in bytes for the RCV FIFO. Once the trigger level number of bytes is reached, an interrupt is sent to the Host. 00 = 01 01 = 04 10 = 08 11 = 14
5:3	Reserved
2	<b>XMT FIFO Clear (XFIC)</b> —WO. When the Host writes 1 to this bit, the hardware will clear the XMT FIFO. This bit is self-cleared by hardware.
1	<b>RCV FIFO Clear (RFIC)</b> —WO. When the Host writes 1 to this bit, the hardware will clear the RCV FIFO. This bit is self-cleared by hardware.
0	<b>FIFO Enable (FIE)</b> —WO. When set to 1, this bit indicates that the KT interface is working in FIFO mode. When this bit value is changed the RCV and XMT FIFO are cleared by hardware.

#### 20.4.2.8 KTLCR—KT Line Control Register (KT—D22:F3)

Address Offset: 03h Attribute: R/W  
Default Value: 03h Size: 8 bits

The line control register specifies the format of the asynchronous data communications exchange and sets the DLAB bit. Most bits in this register have no affect on hardware and are only used by the firmware.

Bit	Description
7	<b>Divisor Latch Address Bit (DLAB)</b> —R/W. This bit is set when the Host wants to read/write the Divisor Latch LSB and MSB registers. This bit is cleared when the Host wants to access the Receive Buffer register or the Transmit Holding register or the Interrupt Enable register.
6	<b>Break Control (BC)</b> —R/W. This bit has no affect on hardware.
5:4	<b>Parity Bit Mode (PBM)</b> —R/W. This bit has no affect on hardware.
3	<b>Parity Enable (PE)</b> —R/W. This bit has no affect on hardware.
2	<b>Stop Bit Select (SBS)</b> —R/W. This bit has no affect on hardware.
1:0	<b>Word Select Byte (WSB)</b> —R/W. This bit has no affect on hardware.



#### 20.4.2.9 KTMCR—KT Modem Control Register (KT—D22:F3)

Address Offset: 04h Attribute: R/W  
Default Value: 00h Size: 8 bits

The Modem Control register controls the interface with the modem. Since the firmware emulates the modem, the Host communicates to the firmware using this register. The register has impact on hardware when the Loopback mode is on.

Bit	Description
7:5	Reserved
4	<b>Loop Back Mode (LBM)</b> —R/W. When set by the Host, this bit indicates that the serial port is in loop Back mode. This means that the data that is transmitted by the host should be received. Helps in debug of the interface.
3	<b>Output 2 (OUT2)</b> —R/W. This bit has no affect on hardware in normal mode. In Loop Back mode the value of this bit is written by hardware to the Modem Status register bit 7.
2	<b>Output 1 (OUT1)</b> —R/W. This bit has no affect on hardware in normal mode. In Loop Back mode the value of this bit is written by hardware to Modem Status register bit 6.
1	<b>Request to Send Out (RTSO)</b> —R/W. This bit has no affect on hardware in normal mode. In Loop Back mode, the value of this bit is written by hardware to Modem Status register bit 4.
0	<b>Data Terminal Ready Out (DRT0)</b> —R/W. This bit has no affect on hardware in normal mode. In Loop Back mode, the value in this bit is written by hardware to Modem Status register Bit 5.

#### 20.4.2.10 KTLSR—KT Line Status Register (KT—D22:F3)

Address Offset: 05h Attribute: RO  
Default Value: 00h Size: 8 bits

This register provides status information of the data transfer to the Host. Error indication, and so forth are provided by the hardware/firmware to the host using this register.

Bit	Description
7	<b>RX FIFO Error (RXFER)</b> —RO. This bit is cleared in Non-FIFO mode. This bit is connected to the BI bit in FIFO mode.
6	<b>Transmit Shift Register Empty (TEMT)</b> —RO. This bit is connected by hardware to bit 5 (THRE) of this register.
5	<b>Transmit Holding Register Empty (THRE)</b> —RO. This bit is always set when the mode (FIFO/ Non-FIFO) is changed by the Host. This bit is active only when the THR operation is enabled by the firmware. This bit has acts differently in the different modes: <b>Non-FIFO:</b> This bit is cleared by hardware when the Host writes to the THR registers and set by hardware when the firmware reads the THR register. <b>FIFO mode:</b> This bit is set by hardware when the THR FIFO is empty, and cleared by hardware when the THR FIFO is not empty. This bit is reset on Host system reset or D3->D0 transition.
4	<b>Break Interrupt (BI)</b> —RO. This bit is cleared by hardware when the LSR register is being read by the Host.
3:2	Reserved
1	<b>Overrun Error (OE)</b> —RO. This bit is cleared by hardware when the LSR register is being read by the Host. The firmware typically sets this bit, but it is cleared by hardware when the host reads the LSR.
0	<b>Data Ready (DR)</b> —RO. <b>Non-FIFO Mode:</b> This bit is set when the firmware writes to the RBR register and cleared by hardware when the RBR register is being Read by the Host. <b>FIFO Mode:</b> This bit is set by hardware when the RBR FIFO is not empty and cleared by hardware when the RBR FIFO is empty. This bit is reset on Host System Reset or D3->D0 transition.



#### 20.4.2.11 KTMSR—KT Modem Status Register (KT—D22:F3)

Address Offset: 06h  
Default Value: 00h

Attribute: RO  
Size: 8 bits

The functionality of the Modem is emulated by the firmware. This register provides the status of the current state of the control lines from the modem.

Bit	Description
7	<b>Data Carrier Detect (DCD)</b> —RO. In Loop Back mode this bit is connected by hardware to the value of MCR bit 3.
6	<b>Ring Indicator (RI)</b> —RO. In Loop Back mode this bit is connected by hardware to the value of MCR bit 2.
5	<b>Data Set Ready (DSR)</b> —RO. In Loop Back mode this bit is connected by hardware to the value of MCR bit 0.
4	<b>Clear To Send (CTS)</b> —RO. In Loop Back mode this bit is connected by hardware to the value of MCR bit 1.
3	<b>Delta Data Carrier Detect (DDCD)</b> —RO. This bit is set when bit 7 is changed. This bit is cleared by hardware when the MSR register is being read by the HOST driver.
2	<b>Trailing Edge of Read Detector (TERI)</b> —RO. This bit is set when bit 6 is changed from 1 to 0. This bit is cleared by hardware when the MSR register is being read by the Host driver.
1	<b>Delta Data Set Ready (DDSR)</b> —RO. This bit is set when bit 5 is changed. This bit is cleared by hardware when the MSR register is being read by the Host driver.
0	<b>Delta Clear To Send (DCTS)</b> —RO. This bit is set when bit 4 is changed. This bit is cleared by hardware when the MSR register is being read by the Host driver.

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# 21 Intel® Serial I/O DMA Controller Registers (D21:F0)

## 21.1 PCI Configuration Registers (DMA—D21:F0)

**Table 21-1. DMA Controller PCI Register Address Map (DMA—D21:F0)**

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	8086	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	0010h	R/W, R/WC, RO
08h-0Bh	RID	Revision Identification and Class Code	0C800000h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h-13h	BAR0	Memory Base Address 0 Register	00000000h	R/W, RO
14h-17h	BAR1	Memory Based Address 1 Register	00000000h	R/WO
2Ch-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAPPTR	Capability Pointer	00h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	01	RO
80h-83h	PWRCAPID	Power Management Capability ID	00030001h	R/W, R/WO
84h-87h	PPCS	Power Management control and Status	00000008h	R/W, R/WC, RO

**Note:** Registers that are not shown should be treated as Reserved (See [Section 7.2](#) for details).

### 21.1.1 VID—Vendor Identification Register (DMA—D21:F0)

Address: 00h-01h Attribute: RO  
 Default Value: 8086h Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO. this is a 16-bit value assigned to Intel. Intel VID = 8086h.



### 21.1.2 DID—Device Identification Register (DMA—D21:F0)

Address: 02h–03h Attribute: RO  
Default Value: 9C60h Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the DMA controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

### 21.1.3 PCICMD—PCI Command Register (DMA—D21:F0)

Address: 04h–05h Attributes: R/W  
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable</b> —R/W 0 = Enable 1 = Disable. Setting this bit disables INTx assertion. The interrupt disabled is legacy INTx# interrupts.
9	Reserved
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7:3	Reserved
2	<b>Bus Master Enable (BME)</b> —R/W
1	<b>Memory Space Enable (MSE)</b> —R/W 0 = Disables memory mapped configuration space. 1 = Enables memory mapped configuration space.
0	Reserved

#### 21.1.4 PCISTS—PCI Status Register (DMA—D21:F0)

Address: 06h–07h      Attributes: RO, R/WC  
 Default Value: 0010h      Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Reserved
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No system error detected 1 = System error detected
13	<b>Received Master Abort (RMA)</b> —R/WC
12	<b>Received Target Abort (RTA)</b> —R/WC
11	<b>Signaled Target Abort (STA)</b> —R/WC
10:5	Reserved
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 1 to indicate there are capability list structures in this function
3	<b>Interrupt Status (INTS)</b> —RO. This bit reflects state of interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the device's/function's INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit reflects Legacy interrupt status.
2:0	Reserved

#### 21.1.5 RID—Revision Identification and Class Code Register (DMA—D21:F0)

Offset Address: 08h–0Bh      Attribute: RO  
 Default Value: 0C800000h      Size: 32 bits

Bit	Description
31:8	<b>Class Code</b> —RO. Hardwired to 080102h
7:0	<b>Revision ID</b> —RO. See <a href="#">Section 1.4</a> for the value of the RID Register.



### 21.1.6 CLS—Cache Line Size Register (DMA—D21:F0)

Address Offset: 0Ch Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Cache Line Size (CLS)</b> —R/W

### 21.1.7 PLT—Primary Latency Timer Register (DMA—D21:F0)

Address Offset: 0Dh Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Latency Count</b> —RO

### 21.1.8 HEADTYP—Header Type Register (DMA—D21:F0)

Address Offset: 0Eh Attribute: RO  
Default Value: 80h Size: 8 bits

Bit	Description
7	<b>Multi-Function Device</b> —RO 0 = Single-function device. 1 = Multi-function device.
6:0	<b>Header Type</b> —RO 00h = Indicates a Host Bridge

### 21.1.9 BAR0—Memory Base Address 0 Register (DMA—D21:F0)

Address Offset: 10–13h Attributes: R/W, RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:12	<b>Base Address 0</b> —R/W. Provides system memory base address for the Intel Serial I/O logic.
11:4	<b>Size Indicator</b> —RO
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that BAR0 is not prefetchable.
2:1	<b>Type</b> —RO.
0	<b>Message Space</b> —RO. This read-only bit always is 0, indicating that the DMA logic is Memory mapped.



### 21.1.10 BAR1—Memory Base Address 1 Register (DMA—D21:F0)

Address Offset: 14h–17h      Attributes: RO, R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:12	<b>Base Address 1</b> —R/W. Provides system memory base address for the Intel Serial I/O DMA logic.
11:4	<b>Size Indicator 1</b> —RO.
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that BAR1 is not prefetchable.
2:1	<b>Type 1</b> —RO.
0	<b>Message Space 1</b> —RO. This read-only bit always is 0, indicating that the DMA logic is Memory mapped.

### 21.1.11 SVID—Subsystem Vendor Identification Register (DMA—D21:F0)

Address Offset: 2Ch–2Dh      Attribute: R/WO  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —R/WO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 21.1.12 SID—Subsystem Identification Register (DMA—D21:F0)

Address Offset: 2Eh–2Fh      Attribute: R/WO  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other. <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 21.1.13 CAPPTR—Capabilities Pointer Register (DMA—D21:F0)

Address Offset: 34h      Attribute: RO  
Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Power Capabilities Pointer (CAPPTR_POWER)</b> —RO



### 21.1.14 INT\_LN—Interrupt Line Register (DMA—D21:F0)

Address Offset: 3Ch  
Default Value: 00h

Attributes: R/W  
Size: 8 bits

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is to communicate to software the interrupt line that the interrupt pin is connected to.

### 21.1.15 INT\_PN—Interrupt Pin Register (DMA—D21:F0)

Address Offset: 3Dh  
Default Value: 01h

Attributes: RO  
Size: 8 bits

Bit	Description
7:4	Reserved
3:0	<b>Interrupt PIN (INT_PN)</b> —RO. Hardwired to 1

### 21.1.16 PWRCAPID—Power Management Capability ID Register (DMA—D21:F0)

Address Offset: 80h-83h  
Default Value: 00030001h

Attributes: RO  
Size: 32 bits

Bit	Description
31:27	<b>PME Support</b> —RO
26:19	Reserved
18:16	<b>Version</b> —RO. Hardwired to 03h.
15:8	<b>next Capability (NEXT_CAP)</b> —RO
7:0	<b>Power Management Cap ID (PW_CAP)</b> —RO. Hardwired to 1. Indicates that this pointer is a PCI power management capability.

### 21.1.17 PPCS—Power Management Control and Status Register (DMA—D21:F0)

Address Offset: 84-87h  
Default Value: 00000008h

Attributes: RO, R/W, R/WC  
Size: 32 bits

Bit	Description
31:16	Reserved
15	<b>PME Status (PMES)</b> —R/WC
14:9	Reserved
8	<b>PME Enable (PMEE)</b> —R/W
7:4	Reserved
3	<b>No Soft Reset</b> —RO
2	Reserved
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the DMA controller and to set a new power state.

## 21.2 Memory Mapped I/O Registers

The DMA MMIO registers (see Table 21-2) can be accessed through BAR0 in PCI mode or through BAR1 when in ACPI mode (that is, when PCI configuration space is hidden). BAR0 and BAR1 are located in PCI configuration space.

**Note:** Only 32-bit operation is supported. Memory reads to DMA MMIO range offset 0x400h and greater will return the last value read from a valid MMIO register. The cycles to MMIO offset 400h and greater do not return Unsupported Request.

**Table 21-2. DMA I/O and Memory Mapped I/O Register Address Map (Sheet 1 of 4)**

BAR + Offset	Mnemonic	Register Name	Default	Attribute
00h	SAR	Source Address (Channel 0)	00000000h	R/W
08h	DAR	Destination Address (Channel 0)	00000000h	R/W
10h	LLP	Linked List Pointer (Channel 0)	00000000h	R/W
18h	CTL_LO	Channel Control Register - Lower 32 bits (Channel 0)	00304825h	R/W, RO
1Ch	CTL_HI	Channel Control Register - Higher 32 bits (Channel 0)	00000002h	R/W, RO
40h	CFG_LO	Configuration - Lower 32 bits (Channel 0)	00000E00h	R/W
44h	CFG_HI	Configuration - Higher 32 bits (Channel 0)	00000004h	R/W
48h	SGA	Source Gather (Channel 0)	00000000h	R/W
50h	DSR	Destination Scatter (Channel 0)	00000000h	R/W
58h	SAR	Source Address (Channel 1)	00000000h	R/W
60h	DAR	Destination Address (Channel 1)	00000000h	R/W
68h	LLP	Linked List Pointer (Channel 1)	00000000h	R/W
70h	CTL_LO	Channel Control Register - Lower 32 bits (Channel 1)	00304825h	R/W, RO
74h	CTL_HI	Channel Control Register - Higher 32 bits (Channel 1)	00000002h	R/W, RO
98h	CFG_LO	Configuration - Lower 32 bits (Channel 1)	00000E00h	R/W, RO
9Ch	CFG_HI	Configuration - Higher 32 bits (Channel 1)	00000004h	R/W
A0h	SGA	Source Gather (Channel 1)	00000000h	R/W
A8h	DSR	Destination Scatter (Channel 1)	00000000h	R/W
B0h	SAR	Source Address (Channel 2)	00000000h	R/W
B8h	DAR	Destination Address (Channel 2)	00000000h	R/W
C0h	LLP	Linked List Pointer (Channel 2)	00000000h	R/W
C8h	CTL_LO	Channel Control Register - Lower 32 bits (Channel 2)	00304825h	R/W, RO
CCh	CTL_HI	Channel Control Register - Higher 32 bits (Channel 2)	00000002h	R/W, RO
F0h	CFG_LO	Configuration - Lower 32 bits (Channel 2)	00000E00h	R/W, RO
F4h	CFG_HI	Configuration - Higher 32 bits (Channel 2)	00000004h	R/W
F8h	SGA	Source Gather (Channel 2)	00000000h	R/W
100h	DSR	Destination Scatter (Channel 2)	00000000h	R/W
108hh	SAR	Source Address (Channel 3)	00000000h	R/W
110h	DAR	Destination Address (Channel 3)	00000000h	R/W



Table 21-2. DMA I/O and Memory Mapped I/O Register Address Map (Sheet 2 of 4)

BAR + Offset	Mnemonic	Register Name	Default	Attribute
118h	LLP	Linked List Pointer (Channel 3)	00000000h	R/W
120h	CTL_LO	Channel Control Register - Lower 32 bits (Channel 3)	00304825h	R/W, RO
124h	CTL_HI	Channel Control Register - Higher 32 bits (Channel 3)	00000002h	R/W, RO
148h	CFG_LO	Configuration - Lower 32 bits (Channel 3)	00000E00h	R/W, RO
14Ch	CFG_HI	Configuration - Higher 32 bits (Channel 3)	00000004h	R/W
150h	SGA	Source Gather (Channel 3)	00000000h	R/W
158h	DSR	Destination Scatter (Channel 3)	00000000h	R/W
160h	SAR	Source Address (Channel 4)	00000000h	R/W
168h	DAR	Destination Address (Channel 4)	00000000h	R/W
170h	LLP	Linked List Pointer (Channel 4)	00000000h	R/W
178h	CTL_LO	Channel Control Register - Lower 32 bits (Channel 4)	00304825h	R/W, RO
17Ch	CTL_HI	Channel Control Register - Higher 32 bits (Channel 4)	00000002h	R/W, RO
1A0h	CFG_LO	Configuration - Lower 32 bits (Channel 4)	00000E00h	R/W, RO
1A4h	CFG_HI	Configuration - Higher 32 bits (Channel 4)	00000004h	R/W
1A8h	SGA	Source Gather (Channel 4)	00000000h	R/W
<b>1B0h</b>	DSR	Destination Scatter (Channel 4)	00000000h	R/W
1B8h	SAR	Source Address (Channel 5)	00000000h	R/W
1C0h	DAR	Destination Address (Channel 5)	00000000h	R/W
1C8h	LLP	Linked List Pointer (Channel 5)	00000000h	R/W
1D0h	CTL_LO	Channel Control Register - Lower 32 bits (Channel 5)	00304825h	R/W, RO
1D4h	CTL_HI	Channel Control Register - Higher 32 bits (Channel 5)	00000002h	R/W, RO
1F8h	CFG_LO	Configuration - Lower 32 bits (Channel 5)	00000E00h	R/W, RO
1FCh	CFG_HI	Configuration - Higher 32 bits (Channel 5)	00000004h	R/W
200h	SGA	Source Gather (Channel 5)	00000000h	R/W
208h	DSR	Destination Scatter (Channel 5)	00000000h	R/W
210h	SAR	Source Address (Channel 6)	00000000h	R/W
218h	DAR	Destination Address (Channel 6)	00000000h	R/W
220h	LLP	Linked List Pointer (Channel 6)	00000000h	R/W
228h	CTL_LO	Channel Control Register - Lower 32 bits (Channel 6)	00304825h	R/W, RO
22Ch	CTL_HI	Channel Control Register - Higher 32 bits (Channel 6)	00000002h	R/W, RO
250h	CFG_LO	Configuration - Lower 32 bits (Channel 6)	00000E00h	R/W, RO
254h	CFG_HI	Configuration - Higher 32 bits (Channel 6)	00000004h	R/W
258h	SGA	Source Gather (Channel 6)	00000000h	R/W
260h	DSR	Destination Scatter (Channel 6)	00000000h	R/W
268h	SAR	Source Address (Channel 7)	00000000h	R/W
270h	DAR	Destination Address (Channel 7)	00000000h	R/W

**Table 21-2. DMA I/O and Memory Mapped I/O Register Address Map (Sheet 3 of 4)**

BAR + Offset	Mnemonic	Register Name	Default	Attribute
278h	LLP	Linked List Pointer (Channel 7)	00000000h	R/W
280h	CTL_LO	Channel Control Register - Lower 32 bits (Channel 7)	00304825h	R/W, RO
284h	CTL_HI	Channel Control Register - Higher 32 bits (Channel 7)	00000002h	R/W, RO
2A8h	CFG_LO	Configuration - Lower 32 bits (Channel 7)	00000E00h	R/W, RO
2ACh	CFG_HI	Configuration - Higher 32 bits (Channel 7)	00000004h	R/W
2B0h	SGA	Source Gather (Channel 7)	00000000h	R/W
2B8h	DSR	Destination Scatter (Channel 7)	00000000h	R/W
2C0h	RAWTFR	Raw DMA Transfer Complete Interrupt Status	00000000h	R/W, RO
2C8h	RAWBLOCK	Raw Block Transfer Complete Interrupt Status	00000000h	R/W, RO
2D0h	RAWSCRTRAN	Raw Source Transaction Complete Interrupt Status	00000000h	R/W, RO
2D8h	RAWDSTTRAN	Raw Destination Transaction Complete Interrupt Status	00000000h	R/W, RO
2E0h	RAWERR	Raw Error Interrupt Status	00000000h	R/W, RO
2E8	STATUSTFR	DMA Transfer Complete Interrupt Status	00000000h	RO
2F0h	STATUSBLOCK	Block Transfer Complete Interrupt Status	00000000h	RO
2F8h	STATUSRCTRAN	Source Transaction Complete Interrupt Status	00000000h	RO
300h	STATUSDSTTRAN	Destination Transaction Complete Interrupt Status	00000000h	RO
308h	STATUSERR	Error Interrupt Status	00000000h	RO
310h	MASKTFR	DMA Transfer Complete Interrupt Mask	00000000h	R/W, RO, WO
318h	MASKBLOCK	Block Transfer Complete Interrupt Mask	00000000h	R/W, RO, WO
320h	MASKSCRTRAN	Source Transaction Complete Interrupt Mask	00000000h	R/W, RO, WO
328h	MASKDSTTRAN	Destination Transaction Complete Interrupt Mask	00000000h	R/W, RO, WO
330h	MASKERR	Raw Error Interrupt Mask	00000000h	R/W, RO, WO
338h	CLEARTFR	DMA Transfer Complete Interrupt Clear	00000000h	WO, RO
344hh	CLEARBLOCK	Block Transfer Complete Interrupt Clear	00000000h	WO, RO
348h	CLEARSCRTRAN	Interrupt Clear Source Transfer	00000000h	WO, RO
350h	CLEARDSTTRAN	Destination Transaction Complete Interrupt Clear	00000000h	WO, RO
358h	CLEARERR	Error Interrupt Clear	00000000h	WO, RO
360hh	STATUSINT	Combined Interrupt Status	00000000h	RO
368h	REQSRCREG	Source software Transaction Request	00000000h	R/W, RO, WO
370h	REQDSTREQ	Destination software Transaction Request	00000000h	R/W, RO, WO
378h	REQSRCSSGL	Source software Transaction Request	00000000h	R/W, RO, WO

**Table 21-2. DMA I/O and Memory Mapped I/O Register Address Map (Sheet 4 of 4)**

BAR + Offset	Mnemonic	Register Name	Default	Attribute
380h	REQDSTSGL	Destination software Transaction Request	00000000h	R/W, RO, WO
398h	DMACFGREG	DMA Configuration	00000000h	R/W, RO
3A0h	CHANENREG	DMA Channel Enable	00000000h	R/W, RO, WO
3B0	DMATESTREG	DMA Test	00000000	R/W, RO
3CCh	DMAPARAMS7	Configuration Parameter Channel 7	38220B00h	RO
3D0h	DMAPARAMS6	Configuration Parameter Channel 6	38220B00h	RO
3D4h	DMAPARAMS5	Configuration Parameter Channel 5	38220B00h	RO
3D8h	DMAPARAMS4	Configuration Parameter Channel 4	38220B00h	RO
3DCh	DMAPARAMS3	Configuration Parameter Channel 3	38220B00h	RO
3E0h	DMAPARAMS2	Configuration Parameter Channel 2	38220B00h	RO
3E4h	DMAPARAMS1	Configuration Parameter Channel 1	38220B00h	RO
3E8h	DMAPARAMS0	Configuration Parameter Channel 0	38220B00h	RO
3EcH	DMA_COMP_PAR_2	DMA Component Parameter 2	00000000h	RO
3F0h	DMA_COMP_PAR_1_LO	DMA Component Parameter 1 - Lower	AAAAAAAAh	RO
3F4h	DMA_COMP_PAR_1_HI	DMA Component Parameter 1 - Higher	36000F04h	RO

### 21.2.1 SAR—Source Address Register (DMA—D21:F0)

Register Offset: Channel 0: BAR + 00h      Attribute: R/W  
 Channel 1: BAR + 58h  
 Channel 2: BAR + B0h  
 Channel 3: BAR + 108h  
 Channel 4: BAR + 160h  
 Channel 5: BAR + 1B8h  
 Channel 6: BAR + 210h  
 Channel 7: BAR + 268h

Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Current Destination Address (SAR)</b> —R/W. Current destination address of DMA transfer. Updated after each destination transfer. The DINC field in the CTL register determines whether the address increments, decrements, or is left unchanged on every destination transfer throughout the block transfer.



## 21.2.2 DAR—Destination Address Register (DMA—D21:F0)

Register Offset: Channel 0: BAR + 08h Attribute: R/W

Channel 1: BAR + 60h

Channel 2: BAR + B8h

Channel 3: BAR + 110h

Channel 4: BAR + 168h

Channel 5: BAR + 1C0h

Channel 6: BAR + 218h

Channel 7: BAR + 270h

Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Current Destination Address (SAR)</b> —R/W. Current destination address of DMA transfer. Updated after each source transfer. The DINC field in the CTL register determines whether the address increments, decrements, or is left unchanged on every transfer throughout the block transfer.

## 21.2.3 LLP—Linked List Pointer Register (DMA—D21:F0)

Register Offset: Channel 0: BAR + 10h Attribute: R/W

Channel 1: BAR + 68h

Channel 2: BAR + C0h

Channel 3: BAR + 118h

Channel 4: BAR + 170h

Channel 5: BAR + 1C8h

Channel 6: BAR + 220h

Channel 7: BAR + 278h

Default Value: 00000000h Size: 32 bits

Bit	Description
31:2	<b>LOC</b> —R/W. Starting address in memory of next LLI if block chaining is enabled.
1:0	<b>List Master Select (LMS)</b> —RO. Identifies the controller layer/interface where the memory device that stores the next linked list item resides. Hard coded 00 = AHB master 1

## 21.2.4 CTL\_LO—Channel Control Register—Lower 32 Bits (DMA—D21:F0)

Register Offset: Channel 0: BAR + 18h      Attribute: R/W, RO  
 Channel 1: BAR + 70h  
 Channel 2: BAR + C8h  
 Channel 3: BAR + 120h  
 Channel 4: BAR + 178h  
 Channel 5: BAR + 1D0h  
 Channel 6: BAR + 228h  
 Channel 7: BAR + 280h

Default Value: 00304825h      Size: 32 bits

Bit	Description
31:29	Reserved
28	<b>LLP_SCR_EN—R/W.</b> Block chaining is enabled on the source side only if this field is set and LLP.LOC is non-zero. 0 = Disable 1 = Enable
27	<b>LLP_DST_EN—R/W.</b> Block chaining is enabled on the destination side only if this field is set and LLP.LOC is non-zero. 0 = Disable 1 = Enable
26:25	<b>Source Master Select (SMS)—R/W.</b> Identifies the Master Interface layer from which the source device (peripheral or memory) is accessed. 00 = AHB master 1 01 = AHB master 2 Other values are reserved. The maximum value of this field that can be read back is 1.
24:23	<b>Destination Master Select (DMS)—R/W.</b> Identifies the Master Interface layer where the destination device (peripheral or memory) resides. 00 = AHB master 1 01 = AHB master 2 Other values are reserved. The maximum value of this field that can be read back is 1
22:20	<b>Transfer Type and Flow Control (TT_FC)—R/W.</b> 000 = Reserved 001 = Memory to Peripheral 010 = Peripheral to Memory 011 = Reserved
19	Reserved.
18	<b>Destination Scatter Enable (DST_SCATTER_EN)—R/W.</b> Scatter on the destination side is applicable only when the CTL.DINC bit indicates an incrementing or decrementing address control. 0 = Disabled 1 = Enabled
17	<b>Source Gather Enable (SRC_GATHER_EN)—R/W.</b> Gather on the source side is applicable only when the CTL.SINC bit indicates an incrementing or decrementing address control. 0 = Disabled 1 = Enabled



Bit	Description
16:14	<p><b>Source Burst Transaction Length (SRC_MSIZE)</b>—R/W. Number of data items, each of width CTL.SRC_TR_WIDTH, to be read from the source every time a source burst transaction request is made from either the corresponding hardware or software handshaking interface.</p> <p>000 = 1 001 = 4 010 = 8 011 = 16 100 = 32 101 = 64 110 = 128 111 = 256</p> <p><b>Note:</b> This value is not related to the AHB bus master HBURST bus</p>
13:11	<p><b>Destination Burst Transaction Length (DEST_MSIZE)</b>—R/W. Number of data items, each of width CTL.DST_TR_WIDTH, to be written to the destination every time a destination burst transaction request is made from either the corresponding hardware or software handshaking interface.</p> <p>000 = 1 001 = 4 010 = 8 011 = 16 100 = 32 101 = 64 110 = 128 111 = 256</p> <p><b>Note:</b> This value is not related to the AHB bus master HBURST bus</p>
10:9	<p><b>Source Address Increment (SINC)</b>—R/W. Indicates whether to increment or decrement the source address on every source transfer. If the device is fetching data from a source peripheral FIFO with a fixed address, then set this field to "No change."</p> <p>00 = Increment 01 = Decrement 1x = No change</p> <p><b>Note:</b> Incrementing or decrementing is done for alignment to the next CTL.SRC_TR_WIDTH boundary</p>
8:7	<p><b>Destination Address Increment (DINC)</b>—R/W. Indicates whether to increment or decrement the destination address on every destination transfer. If the device is writing data to a destination peripheral FIFO with a fixed address, then set this field to "No change."</p> <p>00 = Increment 01 = Decrement 1x = No change</p> <p><b>Note:</b> Incrementing or decrementing is done for alignment to the next CTL.DST_TR_WIDTH boundary.</p>
6:4	<p><b>Source Transfer Width (SRC_TR_WIDTH)</b>—R/W.</p> <p>000 = 8 001 = 16 010 = 32 011 – 111 = invalid</p>
3:1	<p><b>Destination Transfer Width (DST_TR_WIDTH)</b>—R/W.</p> <p>000 = 8 001 = 16 010 = 32 011 – 111 = invalid</p>
0	<p><b>Interrupt Enable (INT_EN)</b>—R/W. If set, then all interrupt-generating sources are enabled. Functions as a global mask bit for all interrupts for the channel; raw interrupt registers still assert if CTL.INT_EN = 0</p>



## 21.2.5 CTL\_HI—Channel Control Register—Higher 32 Bits (DMA—D21:F0)

Register Offset: Channel 0: BAR + 1Ch      Attribute: R/W, RO

Channel 1: BAR + 74h  
Channel 2: BAR + CCh  
Channel 3: BAR + 124h  
Channel 4: BAR + 17Ch  
Channel 5: BAR + 1D4h  
Channel 6: BAR + 22Ch  
Channel 7: BAR + 284h

Default Value: 00000002h

Size: 32 bits

Bit	Description
31:13	Reserved
12	<b>Done Bit (DONE)</b> —R/W. Software can poll the LLI CTLx.DONE bit to see when a block transfer is complete. The LLI CTL.DONE bit should be cleared when the linked lists are set up in memory prior to enabling the channel. 0 = Cleared 1 = Done
11:0	<b>Block Transfer Size (BLOCK_TS)</b> —R/W. This field is written before the channel is enabled in order to indicate the block size. The number programmed into BLOCK_TS indicates the total number of single transactions to perform for every block transfer; a single transaction is mapped to a single AMBA beat. Width: The width of the single transaction is determined by CTL.SRC_TR_WIDTH. Once the transfer starts, the read-back value is the total number of data items already read from the source peripheral.

## 21.2.6 CFG\_LO—Configuration Register—Lower 32 Bits (DMA—D21:F0)

Register Offset: Channel 0: BAR + 40h      Attribute: R/W

Channel 1: BAR + 98h  
 Channel 2: BAR + F0h  
 Channel 3: BAR + 148h  
 Channel 4: BAR + 1A0h  
 Channel 5: BAR + 1F8h  
 Channel 6: BAR + 250h  
 Channel 7: BAR + 2A8h

Default Value: 00000E00h      Size: 32 bits

Bit	Description
31	<b>Automatic Destination Reload (RELOAD_DST)</b> —R/W. The DAR register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. 0 = Disabled 1 = Enabled
30	<b>Automatic Source Reload (RELOAD_SRC)</b> —R/W. The SAR register can be automatically reloaded from its initial value at the end of every block for multi-block transfers. 0 = Disabled 1 = Enabled
29:20	<b>Reserved</b>
19	<b>Source Handshaking Interface Polarity (SRC_HS_POL)</b> —R/W 0 = Active high 1 = Active low
18	<b>Destination Handshaking Interface Polarity (DST_HS_POL)</b> —R/W 0 = Active high 1 = Active low
17:12	Reserved
11	<b>Source Software or Hardware Handshaking Select (HW_SEL_SRC)</b> —R/W 0 = Hardware handshaking interface. Software-initiated transaction requests are ignored. 1 = Software handshaking interface. Hardware-initiated transaction requests are ignored. If the source peripheral is memory, then this bit is ignored.
10	<b>Destination Software or Hardware Handshaking Select (HW_SEL_DST)</b> —R/W 0 = Hardware handshaking interface. Software-initiated transaction requests are ignored. 1 = Software handshaking interface. Hardware-initiated transaction requests are ignored. If the source peripheral is memory, then this bit is ignored.
9	<b>FIFO Empty (FIFO_EMPTY)</b> —RO. Indicates if there is data left in the channel FIFO. 0 = Channel FIFO not empty 1 = Channel FIFO empty
8	<b>Channel Suspend (CH_SUSP)</b> —R/W. Suspend all DMA transfers from source until this bit is cleared. There is no guarantee that the current transaction will complete. Can also be used in conjunction with CFG.FIFO_EMPTY to cleanly disable a channel without losing any data. 0 = Not suspended. 1 = Suspend DMA transfer from the source.

Bit	Description
7:5	<b>Channel Priority (CH_PRIOR)</b> —R/W 111 = Priority of 7 is the highest priority 110 = Priority 6 101 = Priority 5 100 = Priority 4 011 = Priority 3 010 = Priority 2 0 01 = Priority 1 000 = lowest priority
4:0	Reserved

### 21.2.7 CFG\_HI—Configuration Register—Higher 32 Bits (DMA—D21:F0)

Register Offset: Channel 0: BAR + 44h      Attribute: R/W, RO  
 Channel 1: BAR + 9Ch  
 Channel 2: BAR + F4h  
 Channel 3: BAR + 14Ch  
 Channel 4: BAR + 1A4h  
 Channel 5: BAR + 1FCCh  
 Channel 6: BAR + 254h  
 Channel 7: BAR + 2ACh

Default Value: 00000004h      Size: 32 bits

Bit	Description
31:15	Reserved.
14:11	<b>DEST_PER</b> —R/W. Assigns a hardware handshaking interface (0-11) to the destination of channel x if the CFGx.HS_SEL_DST field is 0; otherwise, this field is ignored. 0 = SPI1 Tx Request. 1 = SPI1 Rx Request 2 = SPI0 Tx Request 3 = SPI0 Rx Request 4 = UART0 Tx Request 5 = UART0 Rx Request 6 = UART1 Tx Request 7 = UART1 Rx Request 8 = I2C0 Tx Request 9 = I2C0 Rx Request 10 = I2C1 Tx Request 11 = I2C1 Rx Request
10:7	<b>SRC_PER</b> —R/W. Assigns a hardware Handshaking interface (0-11) to the source of channel x if the CFGx.HS_SEL_SRC field is 0; otherwise, this field is ignored. 0 = SPI1 Tx Request. 1 = SPI1 Rx Request 2 = SPI0 Tx Request 3 = SPI0 Rx Request 4 = UART0 Tx Request 5 = UART0 Rx Request 6 = UART1 Tx Request 7 = UART1 Rx Request 8 = I2C0 Tx Request 9 = I2C0 Rx Request 10 = I2C1 Tx Request 11 = I2C1 Rx Request



Bit	Description
6:5	Reserved
4:2	<b>Protection Control (PROTCTL)</b> —R/W. Used to drive the AHB HPROT[3:1] bus. The AMBA Specification recommends that the default value of HPROT indicates a non-cached, non-buffered, privileged data access. The reset value is used to indicate such an access. HPROT[0] is tied high because all transfers are data accesses, as there are no opcode fetches. There is a one-to-one mapping of these register bits to the HPROT[3:1] master interface signals. 1'b1: HPROT[0] CFGx.PROTCTL[1]: HPROT[1] CFGx.PROTCTL[2]: HPROT[2] CFGx.PROTCTL[3]: HPROT[3]
1	<b>FIFO Mode Select (FIFO_MODE)</b> —R/W. Determines how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0 = Space/data available for single AHB transfer of the specified transfer width. 1 = Data available is greater than or equal to half the FIFO depth for destination transfers and space available is greater than half the FIFO depth for source.
0	<b>Flow Control Mode (FCMODE)</b> —R/W. Determines when source transaction requests are serviced when the destination peripheral is the flow controller. 0 = Source transaction requests are serviced when they occur. Data prefetching is enabled. 1 = Source transaction requests are not serviced until a destination transaction request occurs. <b>Note:</b> Channel Flow Control is fixed by Hardware Parameter to DMA Flow control Only

## 21.2.8 SGR—Source Gather Register (DMA—D21:F0)

Register Offset: Channel 0: BAR + 48h      Attribute: R/W

Channel 1: BAR + A0h

Channel 2: BAR + F8h

Channel 3: BAR + 150h

Channel 4: BAR + 1A8h

Channel 5: BAR + 200h

Channel 6: BAR + 258h

Channel 7: BAR + 2B0h

Default Value: 00000000h      Size: 32 bits

Bit	Description
31:20	<b>Source Gather Count (SGC)</b> —R/W. Specifies the number of contiguous source transfers of CTL.SRC_TR_WIDTH between successive gather intervals. This is defined as a gather boundary.
19:0	<b>Source Gather Interval (SGI)</b> —R/W. Specifies the source address increment/decrement in multiples of CTL.SRC_TR_WIDTH on a gather boundary when gather mode is enabled for the source transfer. The CTL.SINC field controls whether the address increments or decrements. When the CTL.SINC field indicates a fixed-address control, then the address remains constant throughout the transfer and the SGR register is ignored.



### 21.2.9 DSR—Destination Scatter Register (DMA—D21:F0)

Register Offset: Channel 0: BAR + 50h Attribute: R/W

Channel 1: BAR + A8h

Channel 2: BAR + 100h

Channel 3: BAR + 158h

Channel 4: BAR + 1B0h

Channel 5: BAR + 208h

Channel 6: BAR + 260h

Channel 7: BAR + 2B8h

Default Value: 00000000h Size: 32 bits

Bit	Description
31:20	<b>Destination Scatter Count (DSG)</b> —R/W. Specifies the number of contiguous destination transfers of CTL.DST_TR_WIDTH between successive scatter boundaries.
19:0	<b>Destination Scatter Interval (DSI)</b> —R/W. Specifies the destination address increment/decrement in multiples of CTL.DST_TR_WIDTH on a scatter boundary when scatter mode is enabled for the destination transfer. The CTL.DINC field controls whether the address increments or decrements. When the CTL.DINC field indicates a fixed address control, then the address remains constant throughout the transfer and the DSR register is ignored.

### 21.2.10 RAWTFR—Raw DMA Transfer Complete Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 2C0h Attribute: R/W

Default Value: 00000000h Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Raw DMA Transfer Complete Interrupt Status (RAWTFR)</b> —R/W. This interrupt is generated on DMA transfer completion to the destination peripheral. Interrupt events are stored in this Raw Interrupt Status registers before masking. Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARTFR register. Write access is available to this registers for software testing purposes only. Under normal operation, writes to these registers are not recommended. For interrupts to propagate past the RAWTFR interrupt register stage, CTL.INT_EN must be set to 1, and the relevant interrupt must be unmasked in the MASKTFR interrupt register. There is a bit allocated per channel for each RAWTFR. 00000000 = Ch0 RAWTFR 00000010 = Ch1 RAWTFR 00000100 = Ch2 RAWTFR 00001000 = Ch3 RAWTFR 00010000 = Ch4 RAWTFR 00100000 = Ch5 RAWTFR 01000000 = Ch6 RAWTFR 10000000 = Ch7 RAWTFR  0 = Cleared 1 = Active

### 21.2.11 RAWBLOCK—Raw Block Transfer Complete Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 2C8h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Raw Block Transfer Complete Interrupt Status (RAWBLOCK)</b>—R/W. This interrupt is generated on DMA block transfer completion to the destination peripheral. Interrupt events are stored in this Raw Interrupt Status registers before masking. Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARBLOCK register. Write access is available to this register for software testing purposes only. Under normal operation, writes to these registers are not recommended.</p> <p>For interrupts to propagate past the RAWBLOCK interrupt register stage, CTL.INT_EN must be set to 1, and the relevant interrupt must be unmasked in the MASKBLOCK interrupt register. There is a bit allocated per channel for each RAWBLOCK.</p> <p>00000000 = Ch0 RAWBLOCK    00000010 = Ch1 RAWBLOCK    00000100 = Ch2 RAWBLOCK    00001000 = Ch3 RAWBLOCK    00010000 = Ch4 RAWBLOCK    00100000 = Ch5 RAWBLOCK    01000000 = Ch6 RAWBLOCK    10000000 = Ch7 RAWBLOCK</p> <p>0 = Cleared    1 = Active</p>

## 21.2.12 RAWSRCTRAN—Raw Source Transaction Complete Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 2D0h  
 Default Value: 00000000h

Attribute: R/W, RO  
 Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Raw Source Transaction Complete Interrupt Status (RAWSRCTRAN)</b>—R/W.    This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the source side.</p> <p><b>Note:</b> If the source or destination is memory, then INTSRCTRAN/INTDSTTRAN interrupts should be ignored, as there is no concept of a "DMA transaction level" for memory.</p> <p>Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARSRCTRAN register.</p> <p>Write access is available to this registers for software testing purposes only. Under normal operation, writes to these registers are not recommended.</p> <p>For interrupts to propagate past the RAWSRCTRAN interrupt register stage, CTL.INT_EN must be set to 1, and the relevant interrupt must be unmasked in the MASKBLOCK interrupt register.</p> <p>There is a bit allocated per channel for each RAWSRCTRAN.</p> <p>00000000 = Ch0 RAWSRCTRAN    00000010 = Ch1 RAWSRCTRAN    00000100 = Ch2 RAWSRCTRAN    00001000 = Ch3 RAWSRCTRAN    00010000 = Ch4 RAWSRCTRAN    00100000 = Ch5 RAWSRCTRAN    01000000 = Ch6 RAWSRCTRAN    10000000 = Ch7 RAWSRCTRAN</p> <p>0 = Cleared    1 = Active</p>

### 21.2.13 RAWDSTTRAN—Raw Destination Transaction Complete Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 2D8h  
 Default Value: 00000000h

Attribute: R/W  
 Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Raw Destination Complete Transaction Interrupt Status (RAW)</b>—R/W</p> <p>This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the source side.</p> <p><b>Note:</b> If the source or destination is memory, then that channel will never generate the INTDSTTRAN interrupt. Because of this, the corresponding bit in this field will not be set. Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARDSTTRAN register.</p> <p>Write access is available to this registers for software testing purposes only. Under normal operation, writes to these registers are not recommended.</p> <p>For interrupts to propagate past the RAWDSTTRAN interrupt register stage, CTL.INT_EN must be set to 1, and the relevant interrupt must be unmasked in the MASKBLOCK interrupt register.</p> <p>There is a bit allocated per channel for each RAWDSTTRAN.</p> <p>00000000 = Ch0 RAWDSTTRAN    00000010 = Ch1 RAWDSTTRAN    00000100 = Ch2 RAWDSTTRAN    00001000 = Ch3 RAWDSTTRAN    00010000 = Ch4 RAWDSTTRAN    00100000 = Ch5 RAWDSTTRAN    01000000 = Ch6 RAWDSTTRAN    10000000 = Ch7 RAWDSTTRAN</p> <p>0 = Cleared    1 = Active</p>



### 21.2.14 RAWERR—Raw Error Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 2E0h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Raw Error Interrupt Status (RAW)</b> —R/W This interrupt is generated when an ERROR response is received from an AHB slave on the HRESP bus during a DMA transfer. In addition, the DMA transfer is cancelled and the channel is disabled. Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARERR register. Write access is available to this registers for software testing purposes only. Under normal operation, writes to these registers are not recommended. For interrupts to propagate past the RAWERR interrupt register stage, CTLx.INT_EN must be set to 1'b1, and the relevant interrupt must be unmasked in the MaskBlock interrupt register. There is a bit allocated per channel for each RAWERR. 00000000 = Ch0 RAWERR 00000010 = Ch1 RAWERR 00000100 = Ch2 RAWERR 00001000 = Ch3 RAWERR 00010000 = Ch4 RAWERR 00100000 = Ch5 RAWERR 01000000 = Ch6 RAWERR 10000000 = Ch7 RAWERR  0 = Cleared 1 = Active

## 21.2.15 STATUSTFR—DMA Transfer Complete Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 2E8h  
 Default Value: 00000000h

Attribute: RO  
 Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>DMA Transfer Complete Interrupt Status (STATUS)</b>—RO</p> <p>This interrupt is generated on DMA transfer completion to the destination peripheral.</p> <p>Interrupt events are stored in this Status Interrupt Status register before masking.</p> <p>Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARTFR register.</p> <p>The contents of these registers are used to generate the interrupt signals (INT or INT_N bus, depending on interrupt polarity) leaving the DMA controller.</p> <p>There is a bit allocated per channel for each STATUSTFR.</p> <p>00000000 = Ch0 STATUSTFR    00000010 = Ch1 STATUSTFR    00000100 = Ch2 STATUSTFR    00001000 = Ch3 STATUSTFR    00010000 = Ch4 STATUSTFR    00100000 = Ch5 STATUSTFR    01000000 = Ch6 STATUSTFR    10000000 = Ch7 STATUSTFR</p> <p>0 = Cleared    1 = Active</p>

## 21.2.16 STATUSBLOCK—Block Transfer Complete Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 2F0h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Block Transfer Complete Interrupt Status (STATUSBLOCK)</b> —RO. This interrupt is generated on DMA block transfer completion to the destination peripheral. Interrupt events are stored in this Status Interrupt Status register before masking. Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARBLOCK. The contents of these registers are used to generate the interrupt signals (INT or INT_N bus, depending on interrupt polarity) leaving the DMA controller. There is a bit allocated per channel for each STATUSBLOCK. 00000000 = Ch0 STATUSBLOCK 00000010 = Ch1 STATUSBLOCK 00000100 = Ch2 STATUSBLOCK 00001000 = Ch3 STATUSBLOCK 00010000 = Ch4 STATUSBLOCK 00100000 = Ch5 STATUSBLOCK 01000000 = Ch6 STATUSBLOCK 10000000 = Ch7 STATUSBLOCK  0 = Cleared 1 = Active

## 21.2.17 STATUSRCTRAN—Source Transaction Complete Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 2F8h  
 Default Value: 00000000h

Attribute: RO  
 Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Source Transaction Complete Interrupt Status (STATUSRCTRAN)</b>—RO</p> <p>This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the source side.</p> <p><b>Note:</b> If the source or destination is memory, then INTSRCTRAN/INTDSTTRAN interrupts should be ignored, as there is no concept of a "DMA transaction level" for memory.</p> <p>Interrupt events are stored in this Status Interrupt Status register before masking.</p> <p>Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEAESRCTRAN. The contents of these registers are used to generate the interrupt signals (INT or INT_N bus, depending on interrupt polarity) leaving the DMA controller.</p> <p>There is a bit allocated per channel for each STATUSRCTRAN.</p> <p>00000000 = Ch0 STATUSRCTRAN    00000010 = Ch1 STATUSRCTRAN    00000100 = Ch2 STATUSRCTRAN    00001000 = Ch3 STATUSRCTRAN    00010000 = Ch4 STATUSRCTRAN    00100000 = Ch5 STATUSRCTRAN    01000000 = Ch6 STATUSRCTRAN    10000000 = Ch7 STATUSRCTRAN</p> <p>0 = Cleared    1 = Active</p>

## 21.2.18 STATUSDSTTRAN—Destination Transaction Complete Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 300h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Destination Transaction Complete Interrupt Status (STATUSDSTTRAN)</b> —RO This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the destination side.  <b>Note:</b> If the destination for a channel is memory, then that channel will never generate the INTDSTTRAN interrupt. Because of this, the corresponding bit in this field will not be set. Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARDSTTRAN. The contents of these registers are used to generate the interrupt signals (INT or INT_N bus, depending on interrupt polarity) leaving the DMA controller. There is a bit allocated per channel for each STATUSDSTTRAN. 00000000 = Ch0 STATUSDSTTRAN 00000010 = Ch1 STATUSDSTTRAN 00000100 = Ch2 STATUSDSTTRAN 00001000 = Ch3 STATUSDSTTRAN 00010000 = Ch4 STATUSDSTTRAN 00100000 = Ch5 STATUSDSTTRAN 01000000 = Ch6 STATUSDSTTRAN 10000000 = Ch7 STATUSDSTTRAN  0 = Cleared 1 = Active

## 21.2.19 STATUSERR—Error Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 308h  
 Default Value: 00000000h

Attribute: RO  
 Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Error Interrupt Status (STATUSERR)</b>—RO</p> <p>This interrupt is generated when an ERROR response is received from an AHB slave on the HRESP bus during a DMA transfer. In addition, the DMA transfer is cancelled and the channel is disabled. Each bit in this register is cleared by writing a 1 to the corresponding location in the CLEARERR register.</p> <p>The contents of these registers are used to generate the interrupt signals (INT or INT_N bus, depending on interrupt polarity) leaving the DMA controller.</p> <p>There is a bit allocated per channel for each STATUSERR.</p> <p>00000000 = Ch0 STATUSERR    00000010 = Ch1 STATUSERR    00000100 = Ch2 STATUSERR    00001000 = Ch3 STATUSERR    00010000 = Ch4 STATUSERR    00100000 = Ch5 STATUSERR    01000000 = Ch6 STATUSERR    10000000 = Ch7 STATUSERR</p> <p>0 = Cleared    1 = Active</p>

## 21.2.20 MASKTFR—DMA Transfer Complete Interrupt Mask Register (DMA—D21:F0)

Register Offset: BAR + 310h  
Default Value: 00000000h

Attribute: R/W, WO  
Size: 32 bits

The contents of the RAWTFR Status registers are masked with the contents of the MASKTFR Mask registers. This Interrupt Mask register has a bit allocated per channel; for example, MASKTFR[2] is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel  $i$  is memory, then the source transaction complete interrupt, MASKTFR[ $i$ ], must be masked to prevent an erroneous triggering of an interrupt on the int\_combined signal. Similarly, when the destination peripheral of DMA channel  $i$  is memory, then the destination transaction complete interrupt, MASKTFR[ $i$ ], must be masked to prevent an erroneous triggering of an interrupt on the int\_combined(\_n) signal. A channel INT\_MASK bit will be written only if the corresponding mask write enable bit in the INT\_MASK\_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MASKTFR register writes a 1 into MASKTFR[0], while MASKTFR[7:1] remains unchanged. Writing hex 00xx leaves MASKTFR[7:0] unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt; thus, allowing the DMA controller to set the appropriate bit in the Status registers and int\_\* port signals.

Bit	Description
31:16	Reserved
15:8	<p><b>Interrupt Mask Write Enable (INT_MASK_WE)</b>—WO</p> <p>0 = Write disabled  1 = Write enabled</p> <p>There is a bit allocated per channel for each INT_MASK_WE.</p> <p>00000000 = Ch0 INT_MASK_WE  00000010 = Ch1 INT_MASK_WE  00000100 = Ch2 INT_MASK_WE  00001000 = Ch3 INT_MASK_WE  00010000 = Ch4 INT_MASK_WE  00100000 = Ch5 INT_MASK_WE  01000000 = Ch6 INT_MASK_WE  10000000 = Ch7 INT_MASK_WE</p>
7:0	<p><b>Interrupt Mask (INT_MASK)</b>—R/W</p> <p>0 = Masked  1 = Unmasked</p> <p>There is a bit allocated per channel for each INT_MASK.</p> <p>00000000 = Ch0 INT_MASK  00000010 = Ch1 INT_MASK  00000100 = Ch2 INT_MASK  00001000 = Ch3 INT_MASK  00010000 = Ch4 INT_MASK  00100000 = Ch5 INT_MASK  01000000 = Ch6 INT_MASK  10000000 = Ch7 INT_MASK</p>

## 21.2.21 MASKBLOCK—Block Transfer Complete Interrupt Mask Register (DMA—D21:F0)

Register Offset: BAR + 318h      Attribute: R/W, WO  
 Default Value: 00000000h      Size: 32 bits

This interrupt is generated on DMA block transfer completion to the destination peripheral. The contents of the RAWBLOCK Status registers are masked with the contents of the MASKBLOCK Mask registers. This Interrupt Mask register has a bit allocated per channel; for example, MASKBLOCK[2] is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel  $i$  is memory, then the source transaction complete interrupt, MASKBLOCK[ $i$ ], must be masked to prevent an erroneous triggering of an interrupt on the int\_combined signal. Similarly, when the destination peripheral of DMA channel  $i$  is memory, then the destination transaction complete interrupt, MASKBLOCK[ $i$ ], must be masked to prevent an erroneous triggering of an interrupt on the int\_combined(\_n) signal. A channel INT\_MASK bit will be written only if the corresponding mask write enable bit in the INT\_MASK\_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MASKBLOCK register writes a 1 into MASKBLOCK[0], while MASKBLOCK[7:1] remains unchanged. Writing hex 00xx leaves MASKBLOCK[7:0] unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt; thus, allowing the DMA controller to set the appropriate bit in the Status registers and int\_\* port signals.

Bit	Description
31:16	Reserved
15:8	<p><b>Interrupt Mask Write Enable (INT_MASK_WE)</b>—WO</p> <p>0 = Write disabled    1 = Write enabled</p> <p>There is a bit allocated per channel for each INT_MASK_WE.</p> <p>00000000 = Ch0 INT_MASK_WE    00000010 = Ch1 INT_MASK_WE    00000100 = Ch2 INT_MASK_WE    00001000 = Ch3 INT_MASK_WE    00010000 = Ch4 INT_MASK_WE    00100000 = Ch5 INT_MASK_WE    01000000 = Ch6 INT_MASK_WE    10000000 = Ch7 INT_MASK_WE</p>
7:0	<p><b>Interrupt Mask (INT_MASK)</b>—R/W</p> <p>0 = Masked    1 = Unmasked</p> <p>There is a bit allocated per channel for each INT_MASK.</p> <p>00000000 = Ch0 INT_MASK    00000010 = Ch1 INT_MASK    00000100 = Ch2 INT_MASK    00001000 = Ch3 INT_MASK    00010000 = Ch4 INT_MASK    00100000 = Ch5 INT_MASK    01000000 = Ch6 INT_MASK    10000000 = Ch7 INT_MASK</p>

## 21.2.22 MASKSRCTRAN—Source Transaction Complete Interrupt Mask Register (DMA—D21:F0)

Register Offset: BAR + 320h  
Default Value: 00000000h

Attribute: R/W, WO  
Size: 32 bits

This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the source side. The contents of the RAWSRCTRAN Status registers are masked with the contents of the MASKDRCTRAN Mask registers. This Interrupt Mask register has a bit allocated per channel; for example, MASKSRCTRAN[2] is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel  $i$  is memory, then the source transaction complete interrupt, MASKSRCTRAN[ $i$ ], must be masked to prevent an erroneous triggering of an interrupt on the int\_combined signal. Similarly, when the destination peripheral of DMA channel  $i$  is memory, then the destination transaction complete interrupt, MASKSRCTRAN asked to prevent an erroneous triggering of an interrupt on the int\_combined(\_n) signal. A channel INT\_MASK bit will be written only if the corresponding mask write enable bit in the INT\_MASK\_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MASKSRCTRAN register writes a 1 into MASKSRCTRAN[0], while MASKSRCTRAN[7:1] remains unchanged. Writing hex 00xx leaves MASKSRCTRAN[7:0] unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt; thus, allowing the DMA controller to set the appropriate bit in the Status registers and int\_\* port signals.

Bit	Description
31:16	Reserved
15:8	<p><b>Interrupt Mask Write Enable (INT_MASK_WE)</b>—WO</p> <p>0 = Write disabled  1 = Write enabled</p> <p>There is a bit allocated per channel for each INT_MASK_WE.</p> <p>00000000 = Ch0 INT_MASK_WE  00000010 = Ch1 INT_MASK_WE  00000100 = Ch2 INT_MASK_WE  00001000 = Ch3 INT_MASK_WE  00010000 = Ch4 INT_MASK_WE  00100000 = Ch5 INT_MASK_WE  01000000 = Ch6 INT_MASK_WE  10000000 = Ch7 INT_MASK_WE</p>
7:0	<p><b>Interrupt Mask (INT_MASK)</b>—R/W</p> <p>0 = Masked  1 = Unmasked</p> <p>There is a bit allocated per channel for each INT_MASK.</p> <p>00000000 = Ch0 INT_MASK  00000010 = Ch1 INT_MASK  00000100 = Ch2 INT_MASK  00001000 = Ch3 INT_MASK  00010000 = Ch4 INT_MASK  00100000 = Ch5 INT_MASK  01000000 = Ch6 INT_MASK  10000000 = Ch7 INT_MASK</p>

### 21.2.23 MASKDSTTRAN—Destination Transaction Complete Interrupt Mask Register (DMA—D21:F0)

Register Offset: BAR + 328h  
Default Value: 00000000h

Attribute: R/W, WO, RO  
Size: 32 bits

This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the destination side.

The contents of the RAWDSTTRAN Status registers are masked with the contents of the MASKDSTTRAN Mask registers. This Interrupt Mask register has a bit allocated per channel; for example, MASKDSTTRAN[2] is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel  $i$  is memory, then the source transaction complete interrupt, MASKDSTTRAN[ $i$ ], must be masked to prevent an erroneous triggering of an interrupt on the int\_combined signal. Similarly, when the destination peripheral of DMA channel  $i$  is memory, then the destination transaction complete interrupt, MASKDSTTRAN asked to prevent an erroneous triggering of an interrupt on the int\_combined(\_n) signal. A channel INT\_MASK bit will be written only if the corresponding mask write enable bit in the INT\_MASK\_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MASKDSTTRAN register writes a 1 into MASKDSTTRAN[0], while MASKDSTTRAN[7:1] remains unchanged. Writing hex 00xx leaves MASKDSTTRAN[7:0] unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt; thus, allowing the DMA controller to set the appropriate bit in the Status registers and int\_\* port signals.

Bit	Description
31:16	Reserved
15:8	<p><b>Interrupt Mask Write Enable (INT_MASK_WE)</b>—WO</p> <p>0 = Write disabled 1 = Write enabled</p> <p>There is a bit allocated per channel for each INT_MASK_WE.</p> <p>00000000 = Ch0 INT_MASK_WE 00000010 = Ch1 INT_MASK_WE 00000100 = Ch2 INT_MASK_WE 00001000 = Ch3 INT_MASK_WE 00010000 = Ch4 INT_MASK_WE 00100000 = Ch5 INT_MASK_WE 01000000 = Ch6 INT_MASK_WE 10000000 = Ch7 INT_MASK_WE</p>
7:0	<p><b>Interrupt Mask (INT_MASK)</b>—R/W</p> <p>0 = Masked 1 = Unmasked</p> <p>There is a bit allocated per channel for each INT_MASK.</p> <p>00000000 = Ch0 INT_MASK 00000010 = Ch1 INT_MASK 00000100 = Ch2 INT_MASK 00001000 = Ch3 INT_MASK 00010000 = Ch4 INT_MASK 00100000 = Ch5 INT_MASK 01000000 = Ch6 INT_MASK 10000000 = Ch7 INT_MASK</p>

## 21.2.24 MASKERR—Raw Error Interrupt Mask Register (DMA—D21:F0)

Register Offset: BAR + 330h  
Default Value: 00000000h

Attribute: R/W, WO  
Size: 32 bits

This interrupt is generated when an ERROR response is received from an AHB slave on the HRESP bus during a DMA transfer. In addition, the DMA transfer is cancelled and the channel is disabled.

The contents of the RAWERR Status registers are masked with the contents of the MASKERR Mask registers. This Interrupt Mask register has a bit allocated per channel; for example, MASKERR[2] is the mask bit for the Channel 2 transfer complete interrupt. When the source peripheral of DMA channel  $i$  is memory, then the source transaction complete interrupt, MASKERR[ $i$ ], must be masked to prevent an erroneous triggering of an interrupt on the int\_combined signal. Similarly, when the destination peripheral of DMA channel  $i$  is memory, then the destination transaction complete interrupt, MASKERR asked to prevent an erroneous triggering of an interrupt on the int\_combined(\_ $n$ ) signal. A channel INT\_MASK bit will be written only if the corresponding mask write enable bit in the INT\_MASK\_WE field is asserted on the same AHB write transfer. This allows software to set a mask bit without performing a read-modified write operation. For example, writing hex 01x1 to the MASKERR register writes a 1 into MASKERR[0], while MASKERR[7:1] remains unchanged. Writing hex 00xx leaves MASKERR[7:0] unchanged. Writing a 1 to any bit in these registers unmasks the corresponding interrupt; thus, allowing the DMA controller to set the appropriate bit in the Status registers and int\_\* port signals.

Bit	Description
31:16	Reserved
15:8	<p><b>Interrupt Mask Write Enable (INT_MASK_WE)</b>—WO</p> <p>0 = Write disabled  1 = Write enabled</p> <p>There is a bit allocated per channel for each INT_MASK_WE.</p> <p>00000000 = Ch0 INT_MASK_WE  00000010 = Ch1 INT_MASK_WE  00000100 = Ch2 INT_MASK_WE  00001000 = Ch3 INT_MASK_WE  00010000 = Ch4 INT_MASK_WE  00100000 = Ch5 INT_MASK_WE  01000000 = Ch6 INT_MASK_WE  10000000 = Ch7 INT_MASK_WE</p>
7:0	<p><b>Interrupt Mask (INT_MASK)</b>—R/W</p> <p>0 = Masked  1 = Unmasked</p> <p>There is a bit allocated per channel for each INT_MASK.</p> <p>00000000 = Ch0 INT_MASK  00000010 = Ch1 INT_MASK  00000100 = Ch2 INT_MASK  00001000 = Ch3 INT_MASK  00010000 = Ch4 INT_MASK  00100000 = Ch5 INT_MASK  01000000 = Ch6 INT_MASK  10000000 = Ch7 INT_MASK</p>

## 21.2.25 CLEARTFR—DMA Transfer Complete Interrupt Clear Register (DMA—D21:F0)

Register Offset: BAR + 338h      Attribute: WO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Clear Interrupt Status (CLEAR)</b>—WO</p> <p>Clear interrupt status for DMA complete interrupt. This interrupt is generated on DMA transfer completion to the destination peripheral.</p> <p>Each bit in the TFR Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear register.</p> <p>Writing a 0 has no effect. These registers are not readable.</p> <p>There is a bit allocated per channel for each CLEARTFR.</p> <p>00000000 = Ch0 CLEARTFR    00000010 = Ch1 CLEARTFR    00000100 = Ch2 CLEARTFR    00001000 = Ch3 CLEARTFR    00010000 = Ch4 CLEARTFR    00100000 = Ch5 CLEARTFR    01000000 = Ch6 CLEARTFR    10000000 = Ch7 CLEARTFR</p> <p>0 = No effect    1 = Clear interrupt</p>

## 21.2.26 CLEARBLOCK—Block Transfer Complete Interrupt Clear Register (DMA—D21:F0)

Register Offset: BAR + 344h      Attribute: WO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Clear Interrupt Status (CLEAR)</b>—WO</p> <p>Clear interrupt status for block transfer complete interrupt. This interrupt is generated on DMA block transfer completion to the destination peripheral.</p> <p>Each bit in the Block Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear register.</p> <p>Writing a 0 has no effect. These registers are not readable.</p> <p>There is a bit allocated per channel for each CLEARBLOCK.</p> <p>00000000 = Ch0 CLEARBLOCK    00000010 = Ch1 CLEARBLOCK    00000100 = Ch2 CLEARBLOCK    00001000 = Ch3 CLEARBLOCK    00010000 = Ch4 CLEARBLOCK    00100000 = Ch5 CLEARBLOCK    01000000 = Ch6 CLEARBLOCK    10000000 = Ch7 CLEARBLOCK</p> <p>0 = No effect    1 = Clear interrupt</p>

### 21.2.27 CLEARSRCTRAN—Interrupt Clear Source Transfer Register (DMA—D21:F0)

Register Offset: BAR + 348h  
Default Value: 00000000h

Attribute: WO  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Clear Interrupt Status (CLEAR)—WO</b> Clear interrupt status for source transaction complete interrupt. This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the source side. <b>Note:</b> If the source or destination is memory, then INTSRCTRAN/INTDSTTRAN interrupts should be ignored, as there is no concept of a "DMA transaction level" for memory. Each bit in the SrcTran Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear register. Writing a 0 has no effect. These registers are not readable There is a bit allocated per channel for each CLEARSRCTRAN. 00000000 = Ch0 CLEARSRCTRAN 00000010 = Ch1 CLEARSRCTRAN 00000100 = Ch2 CLEARSRCTRAN 00001000 = Ch3 CLEARSRCTRAN 00010000 = Ch4 CLEARSRCTRAN 00100000 = Ch5 CLEARSRCTRAN 01000000 = Ch6 CLEARSRCTRAN 10000000 = Ch7 CLEARSRCTRAN  0 = No effect 1 = Clear interrupt



## 21.2.28 CLEARDSTTRAN—Destination Transaction Complete Interrupt Clear Register (DMA—D21:F0)

Register Offset: BAR + 350h  
Default Value: 00000000h

Attribute: WO  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Clear Interrupt Status (CLEAR)</b>—WO</p> <p>Clear interrupt status for destination transaction complete interrupt. This interrupt is generated after completion of the last AHB transfer of the requested single/burst transaction from the handshaking interface (either the hardware or software handshaking interface) on the destination side.</p> <p><b>Note:</b> If the destination for a channel is memory, then that channel will never generate the INTDSTTRAN interrupt. Because of this, the corresponding bit in this field will not be set.</p> <p>Each bit in the DstTran Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear register.</p> <p>There is a bit allocated per channel for each CLEARDSTTRAN.</p> <p>00000000 = Ch0 CLEARDSTTRAN 00000010 = Ch1 CLEARDSTTRAN 00000100 = Ch2 CLEARDSTTRAN 00001000 = Ch3 CLEARDSTTRAN 00010000 = Ch4 CLEARDSTTRAN 00100000 = Ch5 CLEARDSTTRAN 01000000 = Ch6 CLEARDSTTRAN 10000000 = Ch7 CLEARDSTTRAN</p> <p>0 = No effect 1 = Clear interrupt</p>

## 21.2.29 CLEARERR—Error Interrupt Clear Register (DMA—D21:F0)

Register Offset: BAR + 358h  
Default Value: 00000000h

Attribute: WO  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Clear Interrupt Status (CLEAR)</b>—WO</p> <p>Clear interrupt status for error interrupt. This interrupt is generated when an ERROR response is received from an AHB slave on the HRESP bus during a DMA transfer. In addition, the DMA transfer is cancelled and the channel is disabled.</p> <p>Each bit in the Err Raw Status and Status registers is cleared on the same cycle by writing a 1 to the corresponding location in the Clear register.</p> <p>Writing a 0 has no effect. These registers are not readable</p> <p>There is a bit allocated per channel for each CLEARERR.</p> <p>00000000 = Ch0 CLEARERR 00000010 = Ch1 CLEARERR 00000100 = Ch2 CLEARERR 00001000 = Ch3 CLEARERR 00010000 = Ch4 CLEARERR 00100000 = Ch5 CLEARERR 01000000 = Ch6 CLEARERR 10000000 = Ch7 CLEARERR</p> <p>0 = No effect 1 = Clear interrupt</p>



### 21.2.30 STATUSINT—Combined Interrupt Status Register (DMA—D21:F0)

Register Offset: BAR + 360h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:5	Reserved
4	<b>ERR—RO.</b> OR the contents of STATUSERR register.
3	<b>DSTT—RO.</b> OR the contents of STATUSDSTTRAN register.
2	<b>SRCT—RO.</b> OR the contents of STATUSSRCTTRAN register.
1	<b>BLOCK—RO.</b> OR the contents of STATUSBLOCK register.
0	<b>TFR—RO.</b> OR the contents of STATUSTFR register.

### 21.2.31 REQSRCREG—Source Software Transaction Request Register (DMA—D21:F0)

Register Offset: BAR + 368h  
Default Value: 00000000h

Attribute: R/W, WO  
Size: 32 bits

The registers that comprise the software handshaking registers allow software to initiate single or burst transaction requests in the same way that handshaking interface signals do in hardware.

Setting CFGx.HS\_SEL\_SRC to 1 enables software handshaking on the source of channel x. Setting CFGx.HS\_SEL\_DST to 1 enables software handshaking on the destination of channel x.

A channel SRC\_REQ bit is written only if the corresponding channel write enable bit in the SRC\_REQ\_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register. For example, writing hex 0101 writes a 1 into ReqSrcReg[0], while ReqSrcReg[7:1] remains unchanged. Writing hex 00xx leaves REQSRCREG[7:0] unchanged. This allows software to set a bit in the REQSRCREG register without performing a read-modified write operation.

Bit	Description
31:16	Reserved
15:8	<b>Source Request Write Enable (SRC_REQ_WE)—WO</b> 0 = Write disabled 1 = Write enabled There is a bit allocated per channel for each SRC_REQ_WE 00000000 = Ch0 SRC_REQ_WE 00000010 = Ch1 SRC_REQ_WE 00000100 = Ch2 SRC_REQ_WE 00001000 = Ch3 SRC_REQ_WE 00010000 = Ch4 SRC_REQ_WE 00100000 = Ch5 SRC_REQ_WE 01000000 = Ch6 SRC_REQ_WE 10000000 = Ch7 SRC_REQ_WE

Bit	Description
7:0	<p><b>Source Request (SRC_REQ)</b>—R/W</p> <p>0 = Clear 1 = Active</p> <p>There is a bit allocated per channel for each SRC_REQ.</p> <p>00000000 = Ch0 SRC_REQ 00000010 = Ch1 SRC_REQ 00000100 = Ch2 SRC_REQ 00001000 = Ch3 SRC_REQ 00010000 = Ch4 SRC_REQ 00100000 = Ch5 SRC_REQ 01000000 = Ch6 SRC_REQ 10000000 = Ch7 SRC_REQ</p>

### 21.2.32 REQDSTREQ—Destination Transaction Request Register (DMA—D21:F0)

Register Offset: BAR + 370h  
Default Value: 00000000h

Attribute: R/W, WO  
Size: 32 bits

Bit	Description
31:16	Reserved
15:8	<p><b>Destination Request Write Enable (DST_REQ_WE)</b>—WO</p> <p>0 = Write disabled 1 = Write enabled</p> <p>There is a bit allocated per channel for each DST_REQ_WE.</p> <p>00000000 = Ch0 DST_REQ_WE 00000010 = Ch1 DST_REQ_WE 00000100 = Ch2 DST_REQ_WE 00001000 = Ch3 DST_REQ_WE 00010000 = Ch4 DST_REQ_WE 00100000 = Ch5 DST_REQ_WE 01000000 = Ch6 DST_REQ_WE 10000000 = Ch7 DST_REQ_WE</p>
7:0	<p><b>Destination Request (DST_REQ)</b>—R/W</p> <p>0 = Clear 1 = Active</p> <p>There is a bit allocated per channel for each DST_REQ.</p> <p>00000000 = Ch0 DST_REQ 00000010 = Ch1 DST_REQ 00000100 = Ch2 DST_REQ 00001000 = Ch3 DST_REQ 00010000 = Ch4 DST_REQ 00100000 = Ch5 DST_REQ 01000000 = Ch6 DST_REQ 10000000 = Ch7 DST_REQ</p>

### 21.2.33 REQSRC SGL—Source Software Transaction Request Register 1 (DMA—D21:F0)

Register Offset: BAR + 378h  
 Default Value: 00000000h

Attribute: R/W, WO  
 Size: 32 bits

The registers that comprise the software handshaking registers allow software to initiate single or burst transaction requests in the same way that handshaking interface signals do in hardware.

Setting CFGx.HS\_SEL\_SRC to 1 enables software handshaking on the source of channel x. Setting CFGx.HS\_SEL\_DST to 1 enables software handshaking on the destination of channel x.

A channel SRC\_SGLREQ bit is written only if the corresponding channel write enable bit in the SRC\_SGLREQ\_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

Bit	Description
31:16	Reserved
15:8	<p><b>Source Request Write Enable (SRC_SGLREQ_WE)—WO</b>            0 = Write disabled            1 = Write enabled            There is a bit allocated per channel for each SRC_SGLREQ_WE.            00000000 = Ch0 SRC_SGLREQ_WE            00000010 = Ch1 SRC_SGLREQ_WE            00000100 = Ch2 SRC_SGLREQ_WE            00001000 = Ch3 SRC_SGLREQ_WE            00010000 = Ch4 SRC_SGLREQ_WE            00100000 = Ch5 SRC_SGLREQ_WE            01000000 = Ch6 SRC_SGLREQ_WE            10000000 = Ch7 SRC_SGLREQ_WE</p>
7:0	<p><b>Source Request (SRC_SGLREQ)—R/W</b>            0 = clear            1 = Active            There is a bit allocated per channel for each SRC_SGLREQ.            00000000 = Ch0 SRC_SGLREQ            00000010 = Ch1 SRC_SGLREQ            00000100 = Ch2 SRC_SGLREQ            00001000 = Ch3 SRC_SGLREQ            00010000 = Ch4 SRC_SGLREQ            00100000 = Ch5 SRC_SGLREQ            01000000 = Ch6 SRC_SGLREQ            10000000 = Ch7 SRC_SGLREQ</p>

## 21.2.34 REQDSTSGL—Destination Software Transaction Request Register 1 (DMA—D21:F0)

Register Offset: BAR + 380h Attribute: R/W, WO  
 Default Value: 00000000h Size: 32 bits

The registers that comprise the software handshaking registers allow software to initiate single or burst transaction requests in the same way that handshaking interface signals do in hardware.

Setting CFGx.HS\_SEL\_SRC to 1 enables software handshaking on the source of channel x. Setting CFGx.HS\_SEL\_DST to 1 enables software handshaking on the destination of channel x.

A channel DST\_SGLREQ bit is written only if the corresponding channel write enable bit in the DST\_SGLREQ\_WE field is asserted on the same AHB write transfer, and if the channel is enabled in the ChEnReg register.

Bit	Description
31:16	Reserved
15:8	<p><b>Destination Request Write Enable (DST_SGLREQ_WE)</b>—WO</p> <p>0 = Write disabled    1 = Write enabled</p> <p>There is a bit allocated per channel for each DST_SGLREQ_WE.</p> <p>00000000 = Ch0 DST_SGLREQ_WE    00000010 = Ch1 DST_SGLREQ_WE    00000100 = Ch2 DST_SGLREQ_WE    00001000 = Ch3 DST_SGLREQ_WE    00010000 = Ch4 DST_SGLREQ_WE    00100000 = Ch5 DST_SGLREQ_WE    01000000 = Ch6 DST_SGLREQ_WE    10000000 = Ch7 DST_SGLREQ_WE</p>
7:0	<p><b>Destination Request (DST_SGLREQ)</b>—R/W</p> <p>0 = Clear    1 = Active</p> <p>There is a bit allocated per channel for each DST_SGLREQ.</p> <p>00000000 = Ch0 DST_SGLREQ    00000010 = Ch1 DST_SGLREQ    00000100 = Ch2 DST_SGLREQ    00001000 = Ch3 DST_SGLREQ    00010000 = Ch4 DST_SGLREQ    00100000 = Ch5 DST_SGLREQ    01000000 = Ch6 DST_SGLREQ    10000000 = Ch7 DST_SGLREQ</p>

### 21.2.35 DMACFGREG—DMA Configuration Register (DMA—D21:F0)

Register Offset: BAR + 398h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>DMA Controller Enable (DMA_EN)</b> —R/W. Used to enable the DMA controller, which must be done before any channel activity can begin. If the global channel enable bit is cleared while any channel is still active, then this bit still returns 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which point the bit returns 0. 0 = Disabled. 1 = Enabled.

### 21.2.36 CHANENREG—DMA Channel Enable Register (DMA—D21:F0)

Register Offset: BAR + 3A0h  
Default Value: 00000000h

Attribute: R/W, WO  
Size: 32 bits

This is the DMA Channel Enable Register. If software needs to set up a new channel, then it can read this register in order to find out which channels are currently inactive; it can then enable an inactive channel with the required priority.

All bits of this register are cleared to 0 when the global DMA channel enable bit, DmaCfgReg[0], is 0. When the global channel enable bit is 0, then a write to the ChEnReg register is ignored and a read will always read back 0. The channel enable bit, ChEnReg.CH\_EN, is written only if the corresponding channel write enable bit, ChEnReg.CH\_EN\_WE, is asserted on the same AHB write transfer. For example, writing hex 01x1 writes a 1 into ChEnReg[0], while ChEnReg[7:1] remains unchanged. Writing hex 00xx leaves ChEnReg[7:0] unchanged. A read-modified write is not required.

32-Bit Addressing Example:

CH\_IE register contain 8-bit (0:7) mask for channel enable/disable and 8-bit (8:15) for indicating which bits in the first part are valid (write enable).

When reading this register as 32 bit—the part (8:15) is not cleared. For example:

- Enable channel 0 -> write 0x00000101
- Enable channel 1 -> write 0x00000202
- Disable channel 0 -> write 0x00000100
- Disable channel 1 -> write 0x00000200

**Warning:** CANNOT do step c) as a read-modify-write as it will read 0x00000303 (the upper part is WRITE ONLY).

Bit	Description
31:16	Reserved
15:8	<b>Channel Enable Write Enable (LSTDST_WE)</b> —WO 0 = Write disabled 1 = Write enabled
7:0	<b>Channel Enable (CH_EN)</b> —R/W. The bit is automatically cleared by hardware to disable the channel after the last AMBA transfer of the DMA transfer to the destination has completed. Software can therefore poll this bit to determine when this channel is free for a new DMA transfer. 0 = Disable the channel 1 = Enable the channel



### 21.2.37 DMATESTREG—DMA Test Register (DMA—D21:F0)

Register Offset: BAR + 3B0h Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

This register is used to put the AHB slave interface into test mode, during which the readback value of the writable registers match the value written, assuming the DMAC configuration has not optimized the same registers. In normal operation, the readback value of some registers is a function of the DMAC state and does not match the value written.

Bit	Description
31:1	Reserved
0	<b>Test SLV Interface</b> —R/W. Places the slave interface into test mode. In this mode, the read back value of the writable registers always matches the value written. This bit does not allow writing to read-only registers. 0 = Normal mode 1 = Test mode

### 21.2.38 DMAPARAMS—Configuration Parameter Register (DMA—D21:F0)

Register Offset: Channel 0: BAR + 3E8h Attribute: RO  
 Channel 1: BAR + 3E4h  
 Channel 2: BAR + 3E0h  
 Channel 3: BAR + 3DCh  
 Channel 4: BAR + 3D8h  
 Channel 5: BAR + 3D4h  
 Channel 6: BAR + 3D0h  
 Channel 7: BAR + 3CCh

Default Value: 38220B00h Size: 32 bits

Bit	Description
31	Reserved
30:28	<b>CHx_FIFO_DEPTH</b> —RO 0x3 = Channel x FIFO depth equal to 64 bytes
27:25	<b>CHx_SMS</b> —RO Hardcode the Master interface attached to the Source of Channel x. 0x4 = not hardcoded, then software can program the destination of Channel x to be attached to any of the configured layers.
24:22	<b>CHx_LMS</b> —RO Hardcode the Master interface attached to the Linked List Pointer (LLP) peripheral of Channel x. 0x0 = not hardcoded, then software can program the LLP peripheral of Channel x to be attached to any of the configured layers.
21:19	<b>CHx_DMS</b> —RO Hardcode the Master interface attached to the destination of Channel x. 0x4 = not hardcoded, then software can program the destination of Channel x to be attached to any of the configured layers
18:16	<b>CHx_MAX_MULT_SIZE</b> —RO Maximum value of burst transaction size that can be programmed for Channel x. 0x2 = 16 bytes Programming either of the ctl0.src_msiz or ctl0.dest_msiz registers to a value greater than this parameter will result in erroneous behavior.

Bit	Description
15:14	<b>CHx_FC</b> —RO. Channel x Flow Control 0x0 = DMA flow control only
13	<b>CHx_HC_LPP</b> —RO. Channel x Hard Code Linked List Pointer (LLP) 0x0 = No hardcoding of LPP
12	<b>CHx_CTL_WB_EN</b> —RO. Channel x Writeback Enable 0x0 = Disable writeback of the control register at the end of every block transfer
11	<b>CHx_MULTI_BLK_EN</b> —RO. Channel x Multi-block Enable 0x1 = Enable multi-block DMA transfers on Channel x.
10	<b>CHx_LOCK_EN</b> —RO. Channel x Lock Enable 0x0 = exclude logic to enable channel or bus level locking on Channel x.
9	<b>CHx_SCR_GAT_EN</b> —RO. Channel x Source Scatter Enable 0x1 = Enable the 'scatter' feature on channel x.
8	<b>CHx_DST_SCA_EN</b> —RO. Channel x Destination Scatter Enable 0x1 = Enable the 'scatter' feature on channel x.
7	<b>CHx_STAT_SCR</b> —RO. Status Register from the source peripheral of Channel x 0x0 = exclude logic to fetch a status register from the source peripheral of Channel x and write this status information to system memory at the end of each block transfer
6	<b>CHx_STAT_DST</b> —RO. Status Register from the destination peripheral of Channel x 0x0 = exclude logic to fetch a status register from the source peripheral of Channel x and write this status information to system memory at the end of each block transfer.
5:3	<b>CHx_STW</b> —RO. Channel x Source Transfer Width 0x0 = No hardcoding of the Source transfer width for transfers from the destination of Channel x. Software can program the destination transfer width for Channel x.
2:0	<b>CHx_DTW</b> —RO. Channel x Destination Transfer Width 0x0 = No hardcoding of the destination transfer width for transfers from the destination of Channel x. Software can program the destination transfer width for Channel x.

### 21.2.39 DMA\_COMP\_PAR\_2—DMA Component Parameter 2 Register (DMA—D21:F0)

Register Offset: BAR + 3ECh  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:28	<b>CH7_MULTI_BLK_TYPE</b> —RO. Channel 7 Multi-block Type 0x0 = No hardcode; allow all types of multi-block support (see <b>Note</b> below table)
27:24	<b>CH6_MULTI_BLK_TYPE</b> —RO. Channel 6 Multi-block Type 0x0 = No hardcode; allow all types of multi-block support (see <b>Note</b> below table)
23:20	<b>CH5_MULTI_BLK_TYPE</b> —RO. Channel 5 Multi-block Type 0x0 = No hardcode; allow all types of multi-block support (see <b>Note</b> below table)
19:16	<b>CH4_MULTI_BLK_TYPE</b> —RO. Channel 4 Multi-block Type 0x0 = No hardcode; allow all types of multi-block support (see <b>Note</b> below table)
15:12	<b>CH3_MULTI_BLK_TYPE</b> —RO. Channel 3 Multi-block Type 0x0 = No hardcode; allow all types of multi-block support (see <b>Note</b> below table)



Bit	Description
11:8	<b>CH2_MULTI_BLK_TYPE</b> —RO. Channel 2 Multi-block Type 0x0 = No hardcode; allow all types of multi-block support (see <b>Note</b> below table)
7:4	<b>CH1_MULTI_BLK_TYPE</b> —RO. Channel 1 Multi-block Type 0x0 = No hardcode; allow all types of multi-block support (see <b>Note</b> below table)
3:0	<b>CH0_MULTI_BLK_TYPE</b> —RO. Channel 0 Multi-block Type 0x0 = No hardcode; allow all types of multi-block support (see <b>Note</b> below table)

**Note:** Multi-block support:

CONT\_RELOAD: Allow multi-block transfers where SAR1 is contiguous, DAR1 and CTL1 are reloaded from their initial values

RELOAD\_CONT: Allow multi-block transfers where SAR1 and CTL1 are reloaded from their initial values, DAR1 is contiguous

RELOAD\_RELOAD: Allow multi-block transfers where SAR1, DAR1 and CTL1 are reloaded from their initial values

CONT\_LL\_P: Allow multi-block transfers where SAR1 is contiguous, DAR1, CTL1 and LLP1 are loaded from the next Linked List Item

RELOAD\_LL\_P: Allow multi-block transfers where SAR1 is reloaded from its initial value, DAR1, CTL1 and LLP1 are loaded from the next Linked List Item

LLP\_CONT: Allow multi-block transfers where SAR1, CTL1 and LLP1 are loaded from the next Linked List Item, DAR1 is contiguous

LLP\_RELOAD: Allow multi-block transfers where SAR1, CTL1 and LLP1 are loaded from the next Linked List Item, DAR1 is reloaded from its initial values

LLP\_LL\_P: Allow multi-block transfers where SAR1, DAR1, CTL1 and LLP1 are loaded from the next Linked list Item

## 21.2.40 DMA\_COMP\_PAR\_1\_LO— DMA Component Parameter 1 Lower Register (DMA—D21:F0)

Register Offset: BAR + 3F0h  
Default Value: AAAAAAAAh

Attribute: RO  
Size: 32 bits

Bit	Description
31:28	<b>CH7_MAX_BLK_TYPE</b> —RO CH7 Maximum block size 0xA = 4095 bytes
27:24	<b>CH6_MAX_BLK_TYPE</b> —RO CH6 Maximum block size 0xA = 4095 bytes
23:20	<b>CH5_MAX_BLK_TYPE</b> —RO CH5 Maximum block size 0xA = 4095 bytes
19:16	<b>CH4_MAX_BLK_TYPE</b> —RO CH4 Maximum block size 0xA = 4095 bytes
15:12	<b>CH3_MAX_BLK_TYPE</b> —RO CH3 Maximum block size 0xA = 4095 bytes
11:8	<b>CH2_MAX_BLK_TYPE</b> —RO CH2 Maximum block size 0xA = 4095 bytes
7:4	<b>CH1_MAX_BLK_TYPE</b> —RO CH1 Maximum block size 0xA = 4095 bytes
3:0	<b>CH0_MAX_BLK_TYPE</b> —RO CH0 Maximum block size 0xA = 4095 bytes

### 21.2.41 DMA\_COMP\_PAR\_1\_HIGH—DMA Component Parameter 1 Higher Register (DMA—D21:F0)

Register Offset: BAR + 3F4h  
Default Value: 36000F04h

Attribute: RO  
Size: 32 bits

Bit	Description
31:30	Reserved
29	<b>STATIC_ENDIAN_SELECT</b> —RO. The endianness of the DMA controller is configured statically through RTL parameter (BIG_ENDIAN) that controls the endianness of all AHB master interfaces and the AHB slave interface. 0x1 = Static
28	<b>ADD_ENCODED_PARAMS</b> —RO. Adding the encoded parameters gives firmware an easy and quick way of identifying the DesignWare component within an I/O memory map. Some critical design-time options determine how a driver should interact with the peripheral. There is a minimal area overhead when you include these parameters. Additionally, this option allows a self-configurable single driver to be developed for each component. 0x1 = true
27:23	<b>NUM_HS_INT</b> —RO. Number of handshaking interfaces. Each channel's source and destination can be assigned a handshaking interface. This is under software control. If 0 is selected, then no hardware handshaking interface signals will be present on the I/O. 0xC = 12 Handshaking Interfaces
22:19	Reserved.
18:17	<b>M2_HDATA_WIDTH</b> —RO. Master 2 interface data bus width. 0x0 = 32 Bits
16:15	<b>M1_HDATA_WIDTH</b> —RO. Master 1 interface data bus width. 0x0 = 32 Bits
14:13	<b>S_HDATA_WIDTH</b> —RO. Master interface system address bus width. All AHB layers are assumed to have the same haddr bus width. 0x0 = 32 bits
12:11	<b>NUM_MASTER_INT</b> —RO. Number of AHB master interfaces. A channel's source and destination device can be programmed to be on any of the configured AHB layer's attached to the AHB Master interfaces. This setting determines if a master interface's signal set is present on the I/O or not. AHB master 1 interface signals are always present. 0x1 = 2 AHB master Interfaces
10:8	<b>NUM_CHANNELS</b> —RO. Number Of DMA channels. Each channel is uni-directional and transfers data from the channel's source to the channel's destination. The channel's source and destination AHB layer, system address and handshaking interface are under software control. 0x7 = 8 Channels
7:4	Reserved
3	<b>MABRST</b> —RO. This is a global parameter for all of the configured master interfaces. 0x0 = software cannot limit the maximum AMBA burst length. The maximum possible AMBA burst length in this case will be determined by the depth of the channel FIFO's (64 Bytes) as the DMA controller may try to fill/empty the channel FIFO in a single AMBA burst.
2:1	<b>INTR_IO</b> —RO. Selects which interrupt related pins appear as outputs of the design. 0x2 = Combined - Bit wise OR of all bits of int_flag(_n) bus is driven onto the int_combined(_n) single bit output port
0	<b>BIG_ENDIAN</b> —RO. The AHB master interfaces and the AHB slave interface can be configured to exist in either a big or little endian system. All master interfaces and the AHB slave interface have the same endianness. 0 = all configured AHB master interfaces and the AHB slave interface will be configured to be little endian

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## 22 Intel® Serial I/O I<sup>2</sup>C\* Controller Registers (D21:F1/F2)

### 22.1 PCI Configuration Registers (I<sup>2</sup>C—D21:F1/F2)

Table 22-1. I<sup>2</sup>C\* Controller PCI Register Address Map (I<sup>2</sup>C—D21:F1/F2)

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	8086	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	0010h	R/W, R/WC, RO
08h-0Bh	RID	Revision Identification and Class Code	0C800000h	RO
0Ch	CLS	Cache Line Size	00h	R/W
0Dh	PLT	Primary latency Timer	00h	RO
0Eh	HEADTYP	Header Type	00h	RO
10h-13h	BAR0	Memory Base Address 0 Register	00000000h	R/W, RO
14h-17h	BAR1	Memory Based Address 1 Register	00000000h	R/WO
2Ch-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
34h	CAPPTR	Capability Pointer	00h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	See register description	RO
80h-83h	PWRCAPID	Power Management Capability ID	00030001h	R/W, R/WO
84h-87h	PCS	Power Management control and Status	00000008h	R/W, R/WC, RO

**Note:** Registers that are not shown should be treated as Reserved (See [Section 7.2](#) for details).

#### 22.1.1 VID—Vendor Identification Register (I<sup>2</sup>C—D21:F1/F2)

Address: 00h-01h  
Default Value: 8086h

Attribute: RO  
Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO. This is a 16-bit value assigned to Intel. Intel VID = 8086h.



## 22.1.2 DID—Device Identification Register (I<sup>2</sup>C—D21:F1/F2)

Address: 02h–03h Attribute: RO  
Default Value: 9CE1h Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH I <sup>2</sup> C controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

## 22.1.3 PCICMD—PCI Command Register (I<sup>2</sup>C—D21:F1/F2)

Address: 04h–05h Attributes: R/W  
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable</b> —R/W 0 = Enable 1 = Disables I <sup>2</sup> C to assert its interrupt signal.
9	Reserved
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7:3	Reserved
2	Bus Master Enable (BME)—R/W
1	<b>Memory Space Enable (MSE)</b> —R/W 0 = Disables memory mapped configuration space. 1 = Enables memory mapped configuration space.
0	Reserved

## 22.1.4 PCISTS—PCI Status Register (I<sup>2</sup>C—D21:F1/F2)

Address: 06h–07h      Attributes: RO, R/WC  
 Default Value: 0010h      Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Reserved
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No system error detected. 1 = System error detected.
13	<b>Received Master Abort (RMA)</b> —R/WC
12	<b>Received Target Abort (RTA)</b> —R/WC
11	<b>Signaled Target Abort (STA)</b> —R/WC
10:5	Reserved
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 1 to indicate there are capability list structures in this function.
3	<b>Interrupt Status (INTS)</b> —RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the PCI Command register.
2:0	Reserved

## 22.1.5 RID—Revision Identification and Class Code Register (I<sup>2</sup>C—D21:F1/F2)

Offset Address: 08h–0Bh      Attribute: RO  
 Default Value: 0C800000h      Size: 32 bits

Bit	Description
31:8	<b>Class Code</b> —RO. Hardwired to 0C8000h
7:0	<b>Revision ID</b> —RO. See <a href="#">Section 1.4</a> for the value of the RID Register.

### 22.1.6 CLS—Cache Line Size Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 0Ch Attribute: R/W  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Cache Line Size (CLS)</b> —R/W

### 22.1.7 PLT—Primary Latency Timer Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 0Dh Attribute: RO  
Default Value: 00h Size: 8 bits

Bit	Description
7:0	<b>Latency Count</b> —RO

### 22.1.8 HEADTYP—Header Type Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 0Eh Attribute: RO  
Default Value: 80h Size: 8 bits

Bit	Description
7	<b>Multi-Function Device</b> —RO 0 = Single-function device. 1 = Multi-function device.
6:0	<b>Header Type</b> —RO 00h = Indicates a Host Bridge.

### 22.1.9 BAR0—Memory Base Address 0 Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 10–13h Attributes: R/W, RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:12	<b>Base Address 0</b> —R/W. Provides system memory base address for the I <sup>2</sup> C logic.
11:4	<b>Size Indicator</b> —RO
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that I2CMBAR0 is not prefetchable.
2:1	<b>Type</b> —RO
0	<b>Message Space</b> —RO. This read-only bit always is 0, indicating that the I <sup>2</sup> C logic is Memory mapped.



## 22.1.10 BAR1—Memory Base Address 1 Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 14h–17h      Attributes: RO, R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:12	<b>Base Address 1</b> —R/W. Provides system memory base address for the PCH I <sup>2</sup> C logic.
11:4	<b>Size Indicator 1</b> —RO
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that I2CMBAR1 is not prefetchable.
2:1	<b>Type 1</b> —RO
0	<b>Message Space 1</b> —RO. This read-only bit always is 0, indicating that the I <sup>2</sup> C logic is Memory mapped.

## 22.1.11 SVID—Subsystem Vendor Identification Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 2Ch–2Dh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —R/WO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other.  <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

## 22.1.12 SID—Subsystem Identification Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 2Eh–2Fh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other.  <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

## 22.1.13 CAPPTR—Capabilities Pointer Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 34h      Attribute: RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Power Capabilities Pointer (CAPPTR_POWER)</b> —RO

### 22.1.14 INT\_LN—Interrupt Line Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 3Ch  
Default Value: 00h

Attributes: R/W  
Size: 8 bits

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is to communicate to software the interrupt line that the interrupt pin is connected to.

### 22.1.15 INT\_PN—Interrupt Pin Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 3Dh  
Default Value: 01h

Attributes: RO  
Size: 8 bits

Bit	Description
7:4	Reserved
3:0	<b>Interrupt PIN (INT_PN)</b> —RO. Hardwired to 1

### 22.1.16 PWRCAPID—Power Management Capability ID Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 80h-83h  
Default Value: 00030001h

Attributes: RO  
Size: 32 bits

Bit	Description
31:27	<b>PME Support</b> —RO
26:19	Reserved
18:16	<b>Version</b> —RO. Hardwired to 03h
15:8	<b>Next Capability (NEXT_CAP)</b> —RO
7:0	<b>Power Management Cap ID (PW_CAP)</b> —RO. Hardwired to 1. Indicates that this pointer is a PCI power management capability.

### 22.1.17 PCS—Power Management Control and Status Register (I<sup>2</sup>C—D21:F1/F2)

Address Offset: 84-87h  
Default Value: 00000008h

Attributes: RO, R/W, R/WC  
Size: 32 bits

Bit	Description
31:16	Reserved
15	<b>PME Status (PMES)</b> —R/WC
14:9	Reserved
8	<b>PME Enable (PMEE)</b> —R/W
7:4	Reserved
3	<b>No Soft Reset</b> —RO
2	Reserved
1:0	<b>Power State (PS)</b> —R/W. This field is used both to determine the current power state of the I <sup>2</sup> C controller and to set a new power state.



## 22.2 I<sup>2</sup>C Memory Mapped I/O Registers

The I<sup>2</sup>C MMIO registers (see Table 22-2) can be accessed through BAR0 in PCI mode or through BAR1 when in ACPI mode (for example, when PCI configuration space is hidden). BAR0 and BAR1 are located in PCI configuration space.

**Note:** Only 32-bit operation is supported.

**Table 22-2. I<sup>2</sup>C I/O and Memory Mapped I/O Register Address Map (Sheet 1 of 2)**

BAR + Offset	Mnemonic	Register Name	Default	Attribute
00h-03h	CTL	Control Register	00000000h	R/W, RO
04h-07h	TAR_ADD	Target Address	00000055h	R/W, RO
10h-13h	DATA_CMD	Data Buffer and Command	00000000h	R/W
14h-17h	SS_SCL_HCNT	Standard Speed Clock High Count	00000264h	R/W, RO
18h-1Bh	SS_SCL_LCNT	Standard Speed Clock Low Count	000002C2h	R/W, RO
1Ch-1Fh	FS_SCL_HCNT	Fast Speed Clock High Count	0000006Eh	R/W, RO
20h-23h	FS_SCL_LCNT	Fast Speed Clock Low Count	000000CFh	R/W, RO
2Ch-2Fh	INTR_STAT	Interrupt Status	00000000h	RO
30h-33h	INTR_MASK	Interrupt Mask	000008FFh	R/W, RO
34h-37h	RAW_INTR_STAT	Raw Interrupt Status	00000000h	RO
38h-3Bh	RX_TL	Receive FIFO Threshold	00000000h	R/W, RO
3Ch-3Fh	TX_TL	Transmit FIFO Threshold	00000000h	R/W, RO
40h-43h	CLR_INTR	Clear Interrupt	00000000h	RO
44h-47h	CLR_RX_UNDER	Clear Rx_Under Interrupt	00000000h	RO
48h-4Bh	CLR_RX_OVER	Clear Tx_Over Interrupt	00000000h	RO
4Ch-4Fh	CLR_TX_OVER	Clear Tx_Over Interrupt	00000000h	RO
54h-57h	CLR_TX_ABORT	Clear Tx_Abort Interrupt	00000000h	RO
5Ch-5Fh	CLR_ACTIVITY	clear Activity Interrupt	00000000h	RO
60h-63h	CLR_STOP_DET	Clear STOP Detection Interrupt	00000000h	RO
64h-67h	CLR_START_DET	Clear START Detection Interrupt	00000000h	RO
68h-6Bh	CLR_GEN_CALL	Clear General Call Interrupt	00000000h	RO
6Ch-6Fh	I2C_EN	I <sup>2</sup> C Enable	00000000h	R/W, RO
70h-73h	I2C_STA	I <sup>2</sup> C Status	00000006h	RO
74h-77h	TXFLR	Transmit FIFO Level	00000000h	RO
78h-7Bh	RXFLR	Receive FIFO Level	00000000h	RO
7Ch-7Fh	SDA_HOLD	SDA Hold Time Length	00000001h	R/W, RO
80h-83h	TX_ABRT_SOURCE	Transmit Abort Source	00000000h	RO
84h-87h	SLV_DATA_NACK	Generate Slave Data NACK	00000000h	R/W, RO
88h-8Bh	DMA_CTRL	DMA Control	00000000h	R/W, RO
8Ch-8Fh	DMA_TDLR	DMA Transmit Data Level	00000000h	R/W, RO
90h-93h	DMA_RDLR	DMA Receive Data Level	00000000h	R/W, RO
94h-97h	SDA_SETUP	SDA Setup	00000064h	R/W, RO
98h-9Bh	ACK_GEN_CALL	I <sup>2</sup> C ACK General Call	00000001h	RW, RO
9Ch-9Fh	ENABLE_STATUS	Enable Status	00000000h	RO

**Table 22-2. I<sup>2</sup>C I/O and Memory Mapped I/O Register Address Map (Sheet 2 of 2)**

BAR + Offset	Mnemonic	Register Name	Default	Attribute
F4h-F7h	COMP_PARAM1	Component Parameter	00FFFF6Eh	RO
F8h-FBh	COMP_VER	Component Version	3131352Ah	RO
804h-807h	RESETS	Reset Register	00000000h	R/W, RO
808h-80Bh	GENERAL	General Register	00000000h	R/W, RO
810h-813h	SW_LTR_VALUE	Software LTR Value	00000800h	R/W, RO
814h-817h	AUTO_LTR_VALUE	Auto LTR Value	00000800h	R/W, RO



## 22.2.1 CTL—Control Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 00h  
Default Value: 0000007Fh

Attribute: R/W  
Size: 32 bits

This register contains the physical system memory address used for DMA transfer.

Bit	Description
31:7	Reserved
6	<p><b>Slave Disable</b>—R/W. This bit controls whether I<sup>2</sup>C has its slave disabled. If this bit is set (slave is disabled), the function only works as a master and does not perform any action that requires a slave.</p> <p>0 = Reserved 1 = Slave is disabled (Default)</p> <p><b>Note:</b> For Master Device Configuration Software must ensure that this bit is set to 1, and bit 0 must also be set to 1. Otherwise, this will result in configuration error.</p>
5	<p><b>Restart Enable</b>—R/W. Determines whether RESTART conditions may be sent when I<sup>2</sup>C is acting as a master.</p> <p>0 = Restart Disable 1 = Restart Enable.</p> <p>When the RESTART is disabled, the controller is incapable of performing the following functions:</p> <ul style="list-style-type: none"> <li>• Sending a START BYTE</li> <li>• Performing any high-speed mode operation</li> <li>• Performing direction changes in combined format mode</li> <li>• Performing a read operation with a 10-bit address</li> </ul> <p>By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple transfers. If the above operations are performed, it will result in setting bit 6 (TX_ABRT) of the RAW_INTR_STAT register.</p>
4	<p><b>Addressing Mode</b>—R/W. Controls whether the controller operates in 7- or 10-bit addressing mode.</p> <p>0 = 7-bit addressing 1 = 10-bit addressing</p>
3	Reserved
2:1	<p><b>Speed</b>—R/W. These bits control at which speed I<sup>2</sup>C operates. Its setting is relevant only if I<sup>2</sup>C is operating in master mode.</p> <p>00 = Standard Mode (0 to 100 kbytes/s) 10 = Fast Mode (<math>\leq</math> 400 kbytes/s) 11 = Reserved (Default)</p>
0	<p><b>Master Mode</b>—R/W. This bit controls whether I<sup>2</sup>C master is enabled.</p> <p>0 = Reserved 1 = Master Enabled (Default)</p> <p><b>Note:</b> For Master Device Configuration Software must ensure that this bit is set to 1, and bit 6 must also be set to 1. Otherwise, this will result in configuration error.</p>



## 22.2.2 TAR\_ADD—Target Address Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 04h  
Default Value: 00000055h

Attribute: R/W, RO  
Size: 32 bits

The register should only be updated when the I<sup>2</sup>C is disabled (I2C\_ENABLE = 0).

Bit	Description
31:13	Reserved
12	<b>10-bit Address</b> —R/W. This bit controls whether the controller starts its transfers in 7- or 10-bit addressing mode. 0 = 7-bit addressing 1 = 10-bit addressing
11	<b>Special (SPECIAL)</b> —R/W. This bit indicates whether software performs a General Call or START BYTE command. 0 = Ignore bit 10 in this register (General Call or Start) and use TAR Address normally. 1 = Perform special I <sup>2</sup> C command as specified in bit 10 in this register.
10	<b>General Call or Start (GC_OR_START)</b> —R/W. If bit 11 in this register is set to 1, then this bit indicates whether the controller performs a General Call or START byte command. 0 = General Call Address. After issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (IX_ABRT) of the RAW_INTR_STAT register. The I <sup>2</sup> C controller remains in General Call mode until bit 11 (SPECIAL) is cleared. 1 = Start Byte
9:0	<b>Target Address (IC_TAR)</b> —R/W. When transmitting a General Call, these bits are ignored. To generate a START BYTE, the address needs to be written into these bits once.

### 22.2.3 DATA\_CMD—Data Buffer and Command Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BASE + 10h Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

This register is used by the processor to write to when filling the Tx FIFO and to read from when retrieving bytes from Tx FIFO. In order for the I<sup>2</sup>C controller to continue acknowledging reads, a read command should be written for every byte that is to be received; otherwise, the controller will stop acknowledging.

Bit	Description
31:11	Reserved
10	<b>Restart (RESTART)</b> —R/W. This bit controls whether a RESTART is issued before the byte is sent or received. 0 = A RESTART is issued only if the transfer direction is changing from the previous command. 1 = A RESTART is issued before the data is sent/received (according to the value of the CMD), regardless of whether or not the transfer direction is changing from the previous command.
9	<b>Stop (STOP)</b> —R/W. This bit controls whether a STOP is issued after the byte is sent or received. 0 = STOP is not issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master continues the current transfer by sending/receiving data bytes according to the value of the CMD bit. If the Tx FIFO is empty, the master holds the SCL line low and stalls the bus until a new command is available in the Tx FIFO. 1 = STOP is issued after this byte, regardless of whether or not the Tx FIFO is empty. If the Tx FIFO is not empty, the master immediately tries to start a new transfer by issuing a START and arbitrating for the bus.
8	<b>Command (CMD)</b> —R/W. This bit controls whether a read or a write is performed. 0 = Write. 1 = Read.
7:0	<b>Data (DAT)</b> —R/W. This register contains the data to be transmitted or received on the I <sup>2</sup> C bus. If data is written into this register and a read is performed, these bits are ignored by the controller. These bits return the value of data received on the I <sup>2</sup> C interface when a read is performed to this field.

### 22.2.4 SS\_SCL\_HCNT—Standard Speed Clock High Count Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 14h Attribute: R/W, RO  
 Default Value: 00000264h Size: 32 bits

This register can be written only when the I<sup>2</sup>C interface is disabled, which corresponds to the I2C\_EN register being set to 0. Writes at other times have no effect.

Bit	Description
31:16	Reserved
15:0	<b>Standard Speed I2C Clock High Count</b> —R/W. This register sets the I <sup>2</sup> C clock high period count for standard speed. The value of the register should be within the range of 6 to 65525.



## 22.2.5 SS\_SCL\_LCNT—Standard Speed Clock Low Count Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 18h  
Default Value: 000002C2h

Attribute: R/W, RO  
Size: 32 bits

This register can be written only when the I<sup>2</sup>C interface is disabled, which corresponds to the I<sup>2</sup>C ENABLE bit being set to 0. Writes at other times have no effect.

Bit	Description
31:16	Reserved
15:0	<b>Standard Speed I<sup>2</sup>C Clock Low Count</b> —R/W. This register sets the I <sup>2</sup> C clock low period count for standard speed. The minimum value to be programmed into this field is 8.

## 22.2.6 FS\_SCL\_HCNT—Fast Speed Clock High Count Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 1Ch  
Default Value: 0000006Eh

Attribute: R/W, RO  
Size: 32 bits

This register can be written only when the I<sup>2</sup>C interface is disabled, which corresponds to the ENABLE bit being set to 0. Writes at other times have no effect.

Bit	Description
31:16	Reserved
15:0	<b>Fast Speed I<sup>2</sup>C Clock High Count</b> —R/W. This register sets the I <sup>2</sup> C clock high period count for fast speed. The minimum value to be programmed to this field is 6.

## 22.2.7 FS\_SCL\_LCNT—Fast Speed Clock Low Count Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 20h  
Default Value: 000000CFh

Attribute: R/W  
Size: 32 bits

This register must be set before any I<sup>2</sup>C bus transaction can take place to ensure proper I/O timing.

Bit	Description
31:16	Reserved
15:0	<b>Fast Speed I<sup>2</sup>C Clock Low Count</b> —R/W. This register sets the I <sup>2</sup> C clock low period count for fast speed. The minimum value to be programmed into this field is 8.



## 22.2.8 INTR\_STAT—Interrupt Status Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 2Ch  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Each bit in this register has a corresponding mask bit in the INTR\_MASK register. These bits are cleared by reading the matching interrupt clear register.

Bit	Description
31:12	Reserved
11	<b>General Call (R_GEN_CALL)</b> —RO. Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the controller or when the processor reads bit 0 of the CLR_GEN_CALL register.
10	<b>START Detection (R_START_DET)</b> —RO. Indicates whether a START or RESTART condition has occurred on the I <sup>2</sup> C interface.
9	<b>STOP Detection (R_STOP_DET)</b> —RO. Indicates whether a STOP condition has occurred on the I <sup>2</sup> C interface.
8	<b>Activity (R_ACTIVITY)</b> —RO. This bit captures the controller activity and stays set until it is cleared. There are four ways to clear it: <ul style="list-style-type: none"> <li>Disabling the controller,</li> <li>Reading the CLR_ACTIVITY register</li> <li>Reading the CLR_INTR register</li> <li>System reset.</li> </ul> <b>Note:</b> Once this bit is set, it stays set unless one of the four methods is used to clear it
7	Reserved
6	<b>Tx Abort (R_TX_ABRT)</b> —RO. This bit indicates if the controller, as an I <sup>2</sup> C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO. <b>Note:</b> The controller flushes/resets/empties the Tx FIFO whenever this bit is set. The Tx FIFO remains in this flushed state until the register CLR_TX_ABRT is read. Once this read is performed, the Tx FIFO is then ready to accept more data bytes for transmitting.
5	Reserved
4	<b>Tx Empty (R_TX_EMPTY)</b> —RO. Set to 1 when the transmit buffer is at or below the threshold value set in the TX_TL register. It is automatically cleared by hardware when the buffer level goes above the threshold.
3	<b>Tx Over (R_TX_OVER)</b> —RO. Set during transmit if the transmit buffer is filled to TX_BUFFER_DEPTH and the processor attempts to issue another I <sup>2</sup> C command by writing to the DATA_CMD register.
2	<b>Rx Full (R_RX_FULL)</b> —RO. Set when the receive buffer reaches or goes above the RX_TL threshold in the RX_TL register. It is automatically cleared by hardware when buffer level goes below the threshold.
1	<b>Rx Over (R_RX_OVER)</b> —RO. Set if the receive buffer is completely filled to RX_BUFFER_DEPTH and an additional byte is received from an external I <sup>2</sup> C device. The controller acknowledges this, but any data bytes received after the FIFO is full are lost.
0	<b>Rx Under (R_RX_UNDER)</b> —RO. Set if the processor attempts to read the receive buffer, by reading from the DATA_CMD register, when it is empty.

## 22.2.9 INTR\_MASK—Interrupt Mask Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 30h  
Default Value: 000008FFh

Attribute: R/W  
Size: 32 bits

The bits in this register mask the corresponding interrupt status bits in the INTR\_STAT register.

Bit	Description
31:12	Reserved
11	<b>General Call</b> —R/W
10	<b>START Detection Mask</b> —R/W
9	<b>STOP Detection Mask</b> —R/W
8	<b>Activity Mask</b> —R/W
7	<b>Reserved</b>
6	<b>Tx Abort Mask</b> —R/W
5	<b>Reserved</b>
4	<b>Tx Empty Mask</b> —R/W
3	<b>Tx Over Mask</b> —R/W
2	<b>Rx Full Mask</b> —R/W
1	<b>Rx Over Mask</b> —R/W
0	<b>Rx Under Mask</b> —R/W

## 22.2.10 RAW\_INTR\_STAT—Raw Interrupt Status Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 34h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:12	Reserved
11	<b>General Call</b> —RO. Set only when a General Call address is received and it is acknowledged. It stays set until it is cleared either by disabling the controller or when the processor reads bit 0 of the CLR_GEN_CALL register.
10	<b>START Detection</b> —RO. Indicates whether a START or RESTART condition has occurred on the I <sup>2</sup> C interface.
9	<b>STOP Detection</b> —RO. Indicates whether a STOP condition has occurred on the I <sup>2</sup> C interface.
8	<b>Activity</b> —RO. This bit captures the controller activity and stays set until it is cleared. There are four ways to clear it – disabling the controller, reading the CLR_ACTIVITY register, reading the CLR_INTR register, and system reset.
7	Reserved
6	<b>Tx Abort</b> —RO. This bit indicates if the controller, as an I <sup>2</sup> C transmitter, is unable to complete the intended actions on the contents of the transmit FIFO.
5	Reserved
4	<b>Tx Empty</b> —RO. Set to 1 when the transmit buffer is at or below the threshold value set in the TX_TL register.
3	<b>Tx Over</b> —RO. Set during transmit if the transmit buffer is filled to TX_BUFFER_DEPTH and the processor attempts to issue another I <sup>2</sup> C command by writing to the DATA_CMD register.



Bit	Description
2	<b>Rx Full</b> —RO. Set when the receive buffer reaches or goes above the RX_TL threshold in the RX_TL register.
1	<b>Rx Over</b> —RO. Set if the receive buffer is completely filled to RX_BUFFER_DEPTH and an additional byte is received from an external I <sup>2</sup> C device.
0	<b>Rx Under</b> —RO. Set if the processor attempts to read the receive buffer, by reading from the DATA_CMD register, when it is empty.

## 22.2.11 RX\_TL—Receive FIFO Threshold Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 38h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Receive FIFO Threshold Level (RX_TL)</b> —R/W. Controls the level of entries (or above) that triggers the RX_FULL interrupt (bit 2 in RAW_INTR_STAT register). The valid range is 0–0xF. If values are greater than 0xF, the actual value set will be the maximum depth of the buffer.

## 22.2.12 TX\_TL—Transmit FIFO Threshold Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 3Ch  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

The host driver can get status of the host controller from this register.

Bit	Description
31:8	Reserved
7:0	<b>Transmit FIFO Threshold Level</b> —R/W. Controls the level of entries (or below) that trigger the TX_EMPTY interrupt (bit 4 in RAW_INTR_STAT register). The valid range is 0–0xF. If values are greater than 0xF, the actual value set will be the maximum depth of the buffer.

## 22.2.13 CLR\_INTR—Clear Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 40h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear Interrupt</b> —RO. Read this register to clear the combined interrupt, all individual interrupts, and the TX_ABRT_SOURCE register. This bit does not clear hardware clearable interrupts; only software clearable interrupts can be cleared.

### 22.2.14 CLR\_RX\_UNDER—Clear Rx\_UNDER Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 44h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear Rx_Under Interrupt</b> —RO. Read this register to clear the RX_UNDER interrupt (bit 0) of the RAW_INTR_STAT register.

### 22.2.15 CLR\_RX\_OVER—Clear Rx\_Over Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 48h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear Rx_Over Interrupt</b> —RO. Read this register to clear the RX_OVER interrupt (bit 1) of the RAW_INTR_STAT register.

### 22.2.16 CLR\_TX\_OVER—Clear Tx\_Over Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 4Ch  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear Tx_Over Interrupt</b> —RO. Read this register to clear the TX_OVER interrupt (bit 3) of the RAW_INTR_STAT register.

### 22.2.17 CLR\_TX\_ABORT—Clear Tx\_Abort Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 54h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear Tx_Abort Interrupt</b> —RO. Read this register to clear the TX_ABRT interrupt (bit 6) of the RAW_INTR_STAT register, and the TX_ABRT_SOURCE register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO.



## 22.2.18 CLR\_ACTIVITY—Clear Activity Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 5Ch Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear Activity Interrupt</b> —RO. Reading this register clears the ACTIVITY interrupt if the I <sup>2</sup> C is not active anymore. If the I <sup>2</sup> C module is still active on the bus, the ACTIVITY interrupt bit continues to be set. It is automatically cleared by hardware if the module is disabled and if there is no further activity on the bus. The value read from this register reflect the status of the ACTIVITY interrupt (bit 8) of the RAW_INTR_STAT register.

## 22.2.19 CLR\_STOP\_DET—Clear STOP Detection Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 60h Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear STOP Detection Interrupt</b> —RO. Read this register to clear the STOP_DET interrupt (bit 9) of the RAW_INTR_STAT register.

## 22.2.20 CLR\_START\_DET—Clear START Detection Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 64h Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear START Detection Interrupt</b> —RO. Read this register to clear the START_DET interrupt (bit 10) of the RAW_INTR_STAT register.

## 22.2.21 CLR\_GEN\_CALL—Clear General Call Interrupt Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 68h Attribute: RO  
Default Value: 00000000h Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Clear General Call Interrupt</b> —RO. Read this register to clear the General Call interrupt (bit 11) of the RAW_INTR_STAT register.



## 22.2.22 I2C\_EN—I<sup>2</sup>C Enable Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 6Ch  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:2	Reserved
1	<b>ABORT</b> —R/W. Software can abort I <sup>2</sup> C transfer by setting this bit. This bit can only be set when I2C ENABLE = 1. Hardware will clear the bit once the STOP has been detected.
0	<b>I2C Enable</b> —R/W 0 = I <sup>2</sup> C controller disabled. 1 = I <sup>2</sup> C controller enabled.

## 22.2.23 I2C\_STA—I<sup>2</sup>C Status Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 70h  
Default Value: 00000006h

Attribute: RO  
Size: 32 bits

Bit	Description
31:6	Reserved
5	<b>Controller Activity Status</b> —RO 0 = The controller is in idle state. 1 = The controller is not in idle state.
4	<b>Receive FIFO Completely Full</b> —RO 0 = The receive FIFO contains one or more empty location. 1 = The receive FIFO is completely full.
3	<b>Receive FIFO Not Empty</b> —RO 0 = The receive FIFO is empty. 1 = The receive FIFO contains one or more entries.
2	<b>Transmit FIFO Completely Empty</b> —RO 0 = The transmit FIFO contains one or more valid entries. 1 = The transmit FIFO is completely empty.
1	<b>Transmit FIFO Not Full</b> —RO 0 = The transmit FIFO is full. 1 = The transmit FIFO contains one or more empty locations.
0	<b>Activity</b> —RO. Indicates I <sup>2</sup> C activity status.

## 22.2.24 TXFLR—Transmit FIFO Level Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 74h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:9	Reserved
8:0	<b>Transmit FIFO Level</b> —RO. Contains the number of valid data entries in the transmit FIFO.

## 22.2.25 RXFLR—Receive FIFO Level Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 78h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:9	Reserved
8:0	<b>Receive FIFO Level</b> —RO. Contains the number of valid data entries in the receive FIFO.

## 22.2.26 SDA\_HOLD—SDA Hold Time Length Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 7Ch      Attribute: R/W  
 Default Value: 00000001h      Size: 32 bits

Bit	Description
31:16	Reserved
15:0	<b>SDA Hold Time</b> —R/W. This bit sets the required SDA hold time in units of I <sup>2</sup> C clock period (100 MHz).

## 22.2.27 TX\_ABRT\_SOURCE—Transmit Abort Source Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 80h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:17	Reserved
16	<b>Transfer Abort</b> —RO. When set to 1, this bit indicates that the a transfer abort is initiated by the user (I2C_EN[1]).
15:13	Reserved
12	<b>Arbitration Lost</b> —RO. When set to 1, this bit indicates that the master (the controller) has lost arbitration.
11	Reserved
10	<b>Abort 10-bit Read no RESTART</b> —RO. When set to 1, the bit indicates that the RESTART is disabled (RESTART_EN bit =0) and the controller sends a read command in 10-bit addressing mode.
9	<b>Abort START Byte no RESTART</b> —RO. When set to 1, the bit indicates that the RESTART is disabled (RESTART_EN bit =0) and a START byte is being tried.
8	Reserved
7	<b>Abort START Byte Ack Detection</b> —RO. When set to 1, the bit indicates that the controller has sent a START byte and the START byte was acknowledged (wrong behavior).
6	Reserved
5	<b>Abort General Call No Ack</b> —RO. When set to 1, the bit indicates that the controller has sent a General Call but software programmed the byte following the General Call to be a read from the bus (DATA_CMD[9] is set to 1).
4	<b>Abort General Call Read</b> —RO. When set to 1, the bit indicates that the controller has sent a General Call but there was no acknowledge from any device
3	<b>Abort Tx Data No Ack</b> —RO. When set to 1, the bit indicates that the controller has received an acknowledgement for the address; but when it sent data byte(s) following the address, it did not receive an acknowledge from the device.

Bit	Description
2	<b>Abort 10b Address2 No Ack</b> —RO. When set to 1, the bit indicates that the second 10-bit address byte sent was not acknowledged by any device.
1	<b>Abort 10b Address1 No Ack</b> —RO. When set to 1, the bit indicates that the first 10-bit address byte sent was not acknowledged by any device.
0	<b>Abort 7b Address No Ack</b> —RO. When set to 1, the bit indicates that the 7-bit address sent was not acknowledged by any device.

## 22.2.28 SLV\_DATA\_NACK—Generate Slave DATA NACK Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 84h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Generate NACK</b> —R/W. This NACK generation only occurs when the controller is a receiver. 0 = Generate NACK/ACK normally. 1 = Generate NACK after data byte received. If this register is set to 1, it can only generate a NACK after a data byte is received; hence, the data transfer is aborted and the data received is not pushed to the receive buffer. When the register is set to 0, it generates NACK/ACK, depending on normal criteria.

## 22.2.29 DMA\_CTRL—DMA Control Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 88h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:1	Reserved
1	<b>Transmit DMA Enable</b> —R/W. This bit enables/disables the transmit FIFO DMA channel. 0 = Transmit DMA disabled. 1 = Transmit DMA enabled.
0	<b>Receive DMA Enable</b> —R/W. This bit enables/disables the receive FIFO DMA channel. 0 = Receive DMA disabled. 1 = Receive DMA enabled.



### 22.2.30 DMA\_TDRL—DMA Transmit Data Level Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 8Ch      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Transmit Data Level</b> —R/W. This bit field controls the level at which a DMA request is made by the transmit logic. It is equal to the watermark level; that is, the DMA Transmit Request signal is generated when the number of valid data entries in the transmit FIFO is equal to or below this field value, and Transmit DMA Enable bit = 1.

### 22.2.31 DMA\_RDLR—DMA Receive Data Level Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 90h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Receive Data Level</b> —R/W. This bit field controls the level at which a DMA request is made by the transmit logic. The watermark level = this field +1; that is, the DMA Receive Request signal is generated when the number of valid data entries in the receive FIFO is equal to or more than this field value +1, and Receive DMA Enable bit = 1.

### 22.2.32 ACK\_GEN\_CALL—I<sup>2</sup>C ACK General Call Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 98h      Attribute: R/W  
 Default Value: 00000001h      Size: 32 bits

This register controls whether the controller responds with a ACK or NACK when it receives an I<sup>2</sup>C General Call address.

Bit	Description
31:1	Reserved
0	<b>ACK General Call (ACK_GEN_CALL)</b> —R/W. When set to 1, the controller responds with an ACK when it receives a General Call. When set to 0, the controller does not generate General Call interrupts.

### 22.2.33 ENABLE\_STATUS—I<sup>2</sup>C Enable Status Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 9Ch  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:3	Reserved
2	<b>Slave-Receiver Data Lost</b> —RO. This bit indicates if a slave-Receiver operation has been aborted with at least one data byte received from a transfer due to the setting of I2C ENABLE from 1 to 0.
1	Reserved
0	<b>I2C_EN Status</b> —RO. 0 = I <sup>2</sup> C controller is disabled. 1 = I <sup>2</sup> C controller is enabled.

### 22.2.34 COMP\_PARAM1—Component Parameter Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + F4h  
Default Value: 00FFFF6Eh

Attribute: RO  
Size: 32 bits

Bit	Description
31:24	Reserved
23:16	<b>Transmit Buffer Depth</b> —RO. Indicates TX FIFO_DEPTH
15:8	<b>Receive Buffer Depth</b> —RO. Indicates RX FIFO_DEPTH = 32
7	<b>Add Encoder Parameters</b> —RO. The register allows software to read the encoded configuration information.
6	<b>HAS DMA</b> —RO. Value of 1 indicates that the I <sup>2</sup> C has DMA.
5	<b>INTR_IO</b> —RO. Indicates if each interrupt is presented as separate or all interrupts are combined to generate one interrupt. 0 = Individual 1 = Combined
4	<b>HC Count Value</b> —RO. Indicates if *CNT registers are writable or read only. The *CNT registers are always readable and have reset values from the corresponding *COUNT configuration parameters, which may be user defined or derived. 0 = Not Writable 1 = Writable
3:2	<b>Maximum Speed Mode</b> —RO. Identifies the Maximum speed supported 00 = reserved 01 = Standard 10 = Fast 11 = Reserved
1:0	<b>Data Width</b> —RO. Indicates the internal bus width 00 = 8 bits 01 = 16 bits 10 = 32 bits 11 = Reserved



## 22.2.35 COMP\_VER—Component Version Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + F8h  
Default Value: 3131352Ah

Attribute: RO  
Size: 32 bits

Bit	Description
31:0	Component Version—RO

## 22.2.36 RESETS—Reset Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 804h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:2	Reserved
1:0	<b>I<sup>2</sup>C Host Controller Reset (RESET_I2C)</b> —R/W. Used to reset the I <sup>2</sup> C host controller by software control. All I <sup>2</sup> C configuration state and operational state will be forced to the default state. There is no timing requirement (software can assert and de-assert in back to back transactions). Driver should re-initialize registers related to Driver context following an I <sup>2</sup> C host controller reset. 00 = I <sup>2</sup> C Host Controller is NOT at reset (Reset released) 11 = I <sup>2</sup> C Host Controller is in reset (Reset asserted) Other values are reserved.

## 22.2.37 GENERAL—General Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 808h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:4	Reserved
3	<b>I/O Voltage Select</b> —R/W 0 = 3.3V 1 = 1.8V
2	<b>LTR Mode</b> —R/W 0 = Auto mode. 1 = Software mode. In the auto mode, the BIOS will write to the host controllers Auto LTR Value register (offset 814h) with the active state LTR value and software LTR Value register (offset 810h) with idle state LTR value. In the software mode, the software will write to the host controller software LTR Value (offset 810h). It is the software responsibility to update the LTR with the appropriate value.
1:0	Reserved



### 22.2.38 SW\_LTR\_VALUE—Software LTR Value Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 810h  
Default Value: 00000800h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31	<b>Non Snoop Requirement</b> —RO
30:29	Reserved
28:26	<b>Non Snoop Latency Scale</b> —RO 010 = 1 µs. 011 = 32 µs Other values are Reserved
25:16	<b>Non Snoop Value</b> —RO 10-bit latency value.
15	<b>Snoop Requirement</b> —R/W. If this bit is clear, that indicates that the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely).
14:13	Reserved
12:10	<b>Snoop Latency Scale</b> —R/W 010 = 1 µs. 011 = 32 µs Other values are Reserved Write to this field with reserved values will be dropped completely.
9:0	<b>Snoop Value</b> —R/W. 10-bit latency value. If 0, it indicates that the device cannot tolerate any delay and needs the best possible service/response time.

### 22.2.39 Auto\_LTR\_VALUE—Auto LTR Value Register (I<sup>2</sup>C—D21:F1/2)

Register Offset: BAR + 814h  
Default Value: 00000800h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31	<b>Non Snoop Requirement</b> —RO
30:29	Reserved
28:26	<b>Non Snoop Latency Scale</b> —RO 010 = 1 µs 011 = 32 µs Other values are Reserved
25:16	<b>Non Snoop Value</b> —RO 10-bit latency value.
15	<b>Snoop Requirement</b> —R/W. If this bit is clear, that indicates that the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely).
14:13	Reserved
12:10	<b>Snoop Latency Scale</b> —R/W 010 = 1 µs. 011 = 32 µs Other values are Reserved Write to this field with reserved values will be dropped completely.
9:0	<b>Snoop Value</b> —R/W. 10-bit latency value. If 0, it indicates that the device cannot tolerate any delay and needs the best possible service/response time.

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## 23 Intel® Serial I/O Generic SPI (GSPI) Controller Registers (D21:F3/F4)

### 23.1 PCI Configuration Registers (GSPI—D21:F3/F4)

Table 23-1. GSPI Controller PCI Register Address Map (GSPI—D21:F1/F4)

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	0000	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	0010h	RO, R/WC
08h-0Bh	RID	Revision Identification	See register description	RO
0Ch-0Fh	CLLH	Cache Line Latency Header	00800000h	R/W, RO
10h-13h	BAR0	Memory Base Address 0	00000000h	RO, R/W
14h-17h	BAR1	Memory Base Address 1	00000000h	RO, R/W
2Ch-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
34h-35h	CAPPTR	Capabilities Pointer	00h	RO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	01h	RO
80h-83h	PWR_CAP	Power Capability	00030001h	RO
84h-87h	PME_CTRL_STA	PME Control and Status	00000008h	RO, R/W, R/WC

**Note:** Registers that are not shown should be treated as Reserved.

#### 23.1.1 VID—Vendor Identification Register (GSPI—D21:F3/F4)

Address: 00h-01h  
Default Value: 8086h

Attribute: RO  
Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO



### 23.1.2 DID—Device Identification Register (GSPI—D21:F3/F4)

Address: 02h–03h Attribute: RO  
Default Value: 9CE5h Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

### 23.1.3 PCICMD—PCI Command Register (GSPI—D21:F3/F4)

Address: 04h–05h Attributes: R/W  
Default Value: 0000h Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable</b> —R/W 0 = Enable 1 = Disable
9	Reserved
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7:3	Reserved
2	<b>Bus Master Enable (BME)</b> —R/W
1	<b>Memory Space Enable (MSE)</b> —R/W 0 = Disables memory mapped configuration space. 1 = Enables memory mapped configuration space.
0	Reserved



### 23.1.4 PCISTS—PCI Status Register (GSPI—D21:F3/F4)

Address: 06h-07h      Attributes: RO, R/WC  
 Default Value: 0010h      Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Reserved.
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No system error detected. 1 = System error detected.
13	<b>Received Master Abort (RMA)</b> —R/WC
12	<b>Received Target Abort (RTA)</b> —R/WC
11	<b>Signaled Target Abort (STA)</b> —R/WC
10:5	Reserved
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 1 to indicate there are capability list structures in this function.
3	<b>Interrupt Status (INTS)</b> —RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the PCI Command register.
2:0	Reserved

### 23.1.5 RID—Revision Identification and Class Code Register (GSPI—D21:F3/F4)

Offset Address: 08h-0Bh      Attribute: RO  
 Default Value: See bit description      Size: 32 bits

Bit	Description
31:8	<b>Class Code</b> —RO. Hardwired to 0C8000h
7:0	<b>Revision ID</b> —RO. See Section 1.4 for the value of the RID Register.

### 23.1.6 CLLH—Cache Line Latency Header Register (GSPI—D21:F3/F4)

Offset Address: 0Ch-0Fh      Attribute: R/W, RO  
 Default Value: 00800000h      Size: 32 bits

Bit	Description
31:24	Reserved
23	<b>Multi-Function Device</b> —RO
22:16	<b>Header Type</b> —RO
15:8	<b>Latency Timer</b> —RO
7:0	<b>Cache Line Size</b> —R/W



### 23.1.7 BAR0—Memory Base Address 0 Register (GSPI—D21:F3/F4)

Address Offset: 10–13h  
Default Value: 00000000h

Attributes: R/W, RO  
Size: 32 bits

Bit	Description
31:12	<b>Base Address 0</b> —R/W. Provides system memory base address for the SPI logic.
11:4	<b>Size Indicator</b> —RO
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that BAR0 is not prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO
0	<b>Memory Space Indicator</b> —RO. This read-only bit always is 0, indicating that the SPI logic is Memory mapped.

### 23.1.8 BAR1—Memory Base Address 1 Register (GSPI—D21:F3/F4)

Address Offset: 14h–17h  
Default Value: 00000000h

Attributes: RO, R/W  
Size: 32 bits

Bit	Description
31:12	<b>Base Address 1</b> —R/W. Provides system memory base address for the SPI logic.
11:4	<b>Size Indicator</b> —RO
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that BAR1 is not prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO
0	<b>Memory Space Indicator 1</b> —RO. This read-only bit always is 0, indicating that the SPI logic is Memory mapped.

### 23.1.9 SVID—Subsystem Vendor Identification Register (GSPI—D21:F3/F4)

Address Offset: 2Ch–2Dh  
Default Value: 0000h

Attribute: R/WO  
Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —R/WO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 23.1.10 SID—Subsystem Identification Register (GSPI—D21:F3/F4)

Address Offset: 2Eh–2Fh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other.  <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 23.1.11 CAPPTR—Capabilities Pointer Register (GSPI—D21:F3/F4)

Address Offset: 34h–35h      Attribute: RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Power Capabilities (CAPPTR_POWER)</b> —RO

### 23.1.12 INT\_LN—Interrupt Line Register (GSPI—D21:F3/F4)

Address Offset: 3Ch      Attributes: R/W  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is to communicate to software the interrupt line that the interrupt pin is connected to.

### 23.1.13 INT\_PN—Interrupt Pin Register (GSPI—D21:F3/F4)

Address Offset: 3Dh      Attributes: RO  
 Default Value: 01h      Size: 8 bits

Bit	Description
7:4	Reserved
3:0	<b>Interrupt PIN (INT_PN)</b> —RO.



### 23.1.14 PWR\_CAP—Power Capability Register (GSPI—D21:F3/F4)

Address Offset: 80h-83h  
Default Value: 00030001h

Attributes: RO  
Size: 32 bits

Bit	Description
31:27	<b>PME Support</b> —RO
26:16	Reserved
15:8	<b>Next Capability (NXT_CAP)</b> —RO
7:0	<b>Power Capabilities (PWR_CAP)</b> —RO. Hardwired to 01h.

### 23.1.15 PME\_CTRL\_STA—PME Control and Status Register (GSPI—D21:F3/F4)

Address Offset: 84h-87h  
Default Value: 00000008h

Attributes: RO, R/W, R/WC  
Size: 32 bits

Bit	Description
31:16	Reserved
15	<b>PME Status (PME_STA)</b> —R/WC
14:9	Reserved
8	<b>PME Enable (PME_EN)</b> —R/W
7:4	Reserved
3	<b>No Soft Reset</b> —RO. Hardwired to 1.
2	Reserved
1:0	<b>Power State (PWR_STATE)</b> —R/W

## 23.2 GSPI Memory Mapped I/O Registers

The GSPI MMIO registers (see Table 23-2) can be accessed through BAR0 or through BAR1 when in ACPI mode (when PCI Configuration space is hidden). BAR0 and BAR1 are located in PCI configuration space.

**Note:** Only 32-bit operation is supported.

**Table 23-2. GSPI Memory Mapped I/O Register Address Map**

BAR + Offset	Mnemonic	Register Name	Default	Attribute
00h	SSCR0	SSP Control Register 0	00000000h	RO, R/W
04h	SSCR1	SSP Control Register 1	00000000h	RO, R/W
08h	SSSR	Controller Status	0000F004h	RO, R/WC
10h	SSDR	Data Register	00000000h	RO
0Eh	CMD	Command	0000h	R/W, RO
10h	RESP0	Respond 0	00000000h	RO
28h	SSTO	Timeout Register	00000000h	RO, R/W
44h	SITF	SPI Transmit FIFO	00000000h	RO, R/W
48h	SIRF	SPI Receive FIFO	00000000h	RO, R/W
800h	CLK_PARM	Clock Parameter	00000000h	R/W
804h	RESET	Reset Register	00000000h	R/W, RO
808h	GEN	General Register	00000000h	R/W, RO
810h	SW_LTR_VAL	Software LTR Value	00000800h	R/W, RO
814h	AUTO_LTR_VAL	Auto LTR Value	00000800h	R/W, RO
818h	SPI_CS_CONTROL	SPI Chip Select Control	00000000h	R/W, RO



### 23.2.1 SSCR0—SSP Control Register 0 (GSPI—D21:F3/F4)

Register Offset: BAR + 00h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

The Enhanced SSP Control 0 registers contain twelve different bit fields that control various functions within the Enhanced SSP. All bits must be set to the preferred value before enabling the Enhanced SSP. Writes to reserved bits must be zeroes, and Read values of these bits are undetermined.

Bit	Description
31	<b>Mode (MOD)</b> —R/W 0 = Normal SSP Mode. Full Duplex Serial Peripheral Interface 1 = Reserved
30	<b>Audio Clock Select (ACS)</b> —R/W 0 = Clock selection is determined by the NCS and ECS bits in this register 1 = Reserved
29:27	Reserved
26:24	<b>Frame Rate Divider Control (FRDC)</b> —R/W. Value 0–7 indicates the number of time slots per frame when in network mode (the actual number of time slots is FRDC+1, so 1 to 8 time slots).
23	<b>Transmit Under Run Interrupt Mask (TIM)</b> —R/W. When set, this bit will mask the Transmit FIFO Under Run (TUR) event from generating an SSP interrupt. The SSSR status register will still indicate that an TUR event has occurred. This bit can be written to at any time (before or after SSP is enabled). 0 = Transmit FIFO Under Run (TUR) events will generate an SSP interrupt 1 = TUR events will be masked
22	<b>Receive Over Run Interrupt Mask (RIM)</b> —R/W. When set, this bit will mask the Receive FIFO Over Run (ROR) event from generating an SSP interrupt. The SSSR status register will still indicate that an ROR event has occurred. This bit can be written to at any time (before or after SSP is enabled) 0 = Receive FIFO Over Run (ROR) events will generate an SSP interrupt 1 = ROR events will be masked
21	<b>Network Clock Select (NCS)</b> —R/W. The SSCR0.NCS bit in conjunction with SSCR0.ECS determines which clock is used. 0 = Clock selection is determined by ECS bit 1 = Reserved
20	<b>Extended Data Size Select (EDSS)</b> —R/W. The 1-bit extended field is used in conjunction with the data size select SSCR0.DSS bits to select the size of the data transmitted and received by the Enhanced SSP. 0 = A zero is pre-appended to the DSS value which sets the DSS range from 4–16 bits 1 = A one is pre-appended to the DSS value which sets the DSS range from 17–32 bits
19:8	<b>Serial Clock Rate Value (SCR)</b> —R/W. The 12-bit Serial Clock Rate SSCR0.SCR bit field selects the baud or bit rate of the Enhanced SSP when in Master mode with respect to the SSPSCLK as defined by the SSCR1.SCLKDIR bit. Many different bit rates can be selected to a maximum of 25Mbps. The serial-clock generator uses the clock selected by the SSCR0.ECS and SSCR0.NCS bits divided by the programmable SSCR0.SCR value (3 to 99 <sup>1</sup> ) to generate the serial clock (SSPSCLK). The resultant clock is driven on the SSPSCLK pin and is used by the Enhanced SSP Transmit logic to drive data on the SSPTXD pin, and to latch data on the SSPRXD pin. Depending on the frame format selected, each transmitted bit is driven on either the rising or falling edge of SSPSCLK, and is sampled on the opposite clock edge. Software should take care not to change these bits when the SSPSCLK is enabled through use of the SSPSCLKEN pin or SSPCR1.ECRA or SPCR1.ECRB bits as this will cause the SPSCLK frequency to immediately change. <b>Note:</b> SSP_Clock = 100 MHz, See PRV_CLOCK_PARAMS.N_VAL and PRV_CLOCK_PARAMS.M_VAL SCR is decimal integer. SCR = Serial bit rate = (SSP Clock/SPI_Frequency) – 1 <b>Note:</b> SSP_Clock = 100 MHz, See PRV_CLOCK_PARAMS.N_VAL and PRV_CLOCK_PARAMS.M_VAL SPI Frequency ≤ 25 MHz Valid SCR values = 3 through 99 = 1 – 25 MHz



Bit	Description
7	<p><b>Synchronous Serial Port Enable (SSE)</b>—R/W. The SSP enable bit, SSCR0.SSE, enables and disables all SSP operations.</p> <p>When SSCR0.SSE=0, the Enhanced SSP is disabled; when SSCR0.SSE=1, it is enabled. When the Enhanced SSP is disabled, all of its clocks can be stopped by programmers to minimize power consumption. On reset, the Enhanced SSP is disabled.</p> <p>When the SSCR0.SSE bit is cleared during active operation, the Enhanced SSP is disabled immediately, terminating the current frame being transmitted or received. Clearing SSCR0.SSE resets the Enhanced SSP FIFOs and the Enhanced SSP status bits; however, the Enhanced SSP Control registers are not reset.</p> <p><b>Note:</b> After reset or after clearing the SSCR0.SSE, users must ensure that the SSCR1, SSITR, SSTO, and SSPSP control registers are properly re-configured and that the SSSR register is reset before re-enabling the Enhanced SSP with the SSCR0.SSE. Also, the SSCR0.SSE bit must be cleared before reconfiguring the SSCR0, SSCR1, or SSPSP registers; other control bits in SSCR0 can be written at the same time as the SSCR0.SSE. When any SSP is disabled, its five pins can be used as GPIOs.</p> <p>0 = - SSP operation disabled 1 = - SSP operation enabled</p>
6	<p><b>External Clock Select (ECS)</b>—R/W</p> <p>0 = Use on-chip 100 MHz clock to produce the SSP's serial clock (Using the output of the M/N divider (offset 800h, CLOCK_PARAMS) to create the SSP's serial clock) 1 = Reserved</p>
5:4	<p><b>Frame Format (FRF)</b>—R/W. Only Motorola interface supported.</p> <p>00 = Motorola Serial Peripheral Interface (SPI) Other values are reserved.</p>
3:0	<p><b>Data Size Select (DSS)</b>—R/W. Data Size Select With EDSS as MSB.</p> <p>The processor or DMA access data through the Enhanced SSP Port's Transmit and Receive FIFOs. A processor access takes the form of programmed I/O, transferring one FIFO entry per access. Processor accesses would normally be triggered off of an SSSR Interrupt and must always be 32-bits wide.</p> <p>Processor Writes to the FIFOs are 32-bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (EDSS/DSS value). Processor Reads to the FIFOs are also 32-bits wide, but the Receive data written into the RX FIFO (from the RXD line) is stored with zeroes in the MSBs down to the programmed data size.</p> <p>The FIFOs can also be accessed by DMA bursts, which must be in multiples of 1, 2, or 4 bytes, depending upon the EDSS value, and must also transfer one FIFO entry per access. When the SSCR0.EDSS bit is set, DMA bursts must be in multiples of 4 bytes (the DMA must have the Enhanced SSP configured as a 32-bit peripheral). The DMA's DCMD.width register must be at least the SSP data size programmed into the SSP control registers EDSS and DSS. The FIFO is seen as one 32-bit location by the processor. For Writes, the Enhanced SSP port takes the data from the Transmit FIFO, serializes it, and sends it over the serial wire (SSPTXD) to the external peripheral. Receive data from the external peripheral (on SSPRXD) is converted to parallel words and stored in the Receive FIFO.</p> <p>A programmable FIFO trigger threshold, when exceeded, generates an Interrupt or DMA service request that, if enabled, signals the processor or DMA respectively to empty the Receive FIFO or to refill the Transmit FIFO.</p> <p>The Transmit and Receive FIFOs are differentiated by whether the access is a Read or a Write transfer. Reads automatically target the Receive FIFO, while Writes will write data to the Transmit FIFO. From a memory-map perspective, they are at the same address. FIFOs are 256 samples deep by 32-bits wide. Each read or write is to 1 SSP sample.</p> <p>The 4-bit Data Size Select SSCR0.DSS field is used in conjunction with the extended data size select SSCR0.EDSS bit to select the size of the data transmitted and received by the Enhanced SSP. The concatenated 5-bit value of SSCR0.EDSS and SSCR0.DSS provides a data range from 4- to 32-bits in length.</p> <p><b>Note:</b> When data is programmed to be less than 32 bits, the FIFO should be programmed right-justified. Although it is possible to program data sizes of 1, 2, and 3 bits, these sizes are reserved and produce unpredictable results in the Enhanced SSP.</p> <p>0011 = 4 bits 0111 = 8 bits 1111 = 16, 32 bits</p> <p><b>Note:</b> To differentiate between 16 bits and 32 bits check the EDSS bit, for 32-bit data EDSS = 1.</p>



### 23.2.2 SSCR1—SSP Control Register 1 (GSPI—D21:F3/F4)

Register Offset: BAR + 04h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

The Enhanced SSP Control 1 registers contain bit fields that control various SSP functions. Bits must be set to the preferred value before enabling the Enhanced SSP.

**Note:** Writes to reserved bits must be zeroes, and Read values of these bits is undetermined.

Bit	Description
31	<b>TXD Tri-state Enable on Last Phase (TTELP)</b> —R/W. This bit is used in conjunction with the TTE bit. When set, this bit will cause the SSPTXD line to be tri-stated 1/2 phase later than that specified in the TTE bit description under either of the following two conditions: 1. The format is TI SSP 2. The format is PSP and the Enhanced SSP is a slave to frame (SFRMDIR=1). For example, when in TI SSP format, with the TTELP and TTE bits set, the SSPTXD line will tri-state on the next rising edge after the lsb was to have been flopped 0 = TXD line will be tri-stated on same clock edge as TXD is to be flopped 1 = TXD line will be tri-stated ½ clock phase after TXD is to be flopped
30	<b>TXD Tri-state Enable (TTE)</b> —R/W. If this bit is cleared, the SSPTXD line will always be driven. When set, however, this bit will cause the SSPTXD line to be tri-stated when the Enhanced SSP is not transmitting data. The timing for the tri-state enable/disable varies according to the different serial formats and frame direction. For Motorola SPI format, the SSPTXD line is tri-stated whenever SSPSFRM (frame signal) is de-asserted (at logic 1). 0 = TXD line will not be tri-stated 1 = TXD line will be tri-stated when no transmitting data
29:24	Reserved
23	<b>Receive With Out Transmit (RWOT)</b> —R/W. The SSCR1.RWOT bit is a read-write bit used to put the Enhanced SSP into a mode similar to half duplex. When the Enhanced SSP is in Transmit/Receive mode as determined SSCR1.RWOT=0, the Enhanced SSP simultaneously transmits and receives data (as supported by the individual protocols; that is, normally all modes are full duplex except microwire) and the serial clock SSPSCLK only toggles while an active data transfer is underway. When in Receive-without-Transmit mode as determined by SSCR1.RWOT=1, the Enhanced SSP will continue to clock in receive data despite data existing or not in the Transmit FIFO. Data is sent/received according to the selected format immediately after the Enhanced SSP enable bit (SSCR0.SSE) is set. This allows the Enhanced SSP to receive data without transmitting data (half-duplex only). During this mode, if there is no data to send, programmers should disable the DMA service requests and Interrupts for the Transmit FIFO (clear the SSCR1.TSRE and SSCR1.TIE bits). If the Transmit FIFO is empty, the SSPTXD line will be driven to 0. The Transmit FIFO under run condition will not occur when SSCR1.RWOT=1. When RWOT is enabled, the SSSR.BUSY bit will remain active (set to 1) until software clears the RWOT bit. If the Enhanced SSP has been in RWOT mode, and software disables this by clearing the RWOT bit, an extra frame cycle may occur due to the synchronization between clock domains. This bit must not be used when the SSCR0.MOD bit is set. 0 = Transmit/Receive mode 1 = Receive without transmit mode <b>Warning:</b> When RWOT =1, the first entry of the TX FIFO must be initialized with all zeros.



Bit	Description
22	<p><b>Trailing Byte (TRAIL)</b>—R/W. When the number of samples in the Receive FIFO is less than its FIFO trigger threshold level, and no additional data is received, the remaining bytes are called trailing bytes. Trailing bytes can be handled by either the DMA or the processor, as indicated by the SSCR1.TRAILING bit. Trailing bytes are identified by means of a Timeout mechanism and the existence of data within the Receive FIFO.</p> <p><b>Timeout:</b> A Timeout condition exists when the Receive FIFO has been idle for a period of time (in bus clocks) defined by the value programmed within the Timeout register (SSTO). When a Timeout occurs, the receiver Timeout interrupt SSSR.TINT bit will be set to a 1, and if the Timeout Interrupt is enabled SSCR1.TINTE=1, a Timeout Interrupt will occur. The Timeout timer is reset after a new sample is received. Once the SSSR.TINT bit is set, it must be cleared by programmers by writing a 1 to it. Clearing this bit also causes the Timeout Interrupt, if enabled, to be de-asserted.</p> <p><b>Peripheral Trailing Byte Interrupt:</b> It is possible for the DMA to reach the end of its Descriptor chain while removing Receive FIFO data. When this happens, the processor is forced to take over because the DMA can no longer service the Enhanced SSP request until a new chain is linked. When the DMA has reached the end of its Descriptor chain, and there is data in the receive FIFO, the Enhanced SSP will do the following:</p> <ul style="list-style-type: none"> <li>• Sets the peripheral trailing byte interrupt SSSR.PINT bit to 1;</li> <li>• Asserts the Enhanced SSP Interrupt to signal to the processor that a Peripheral Trailing Byte Interrupt condition has occurred (if SSCR1.PINTE=1 to enable the interrupt).</li> <li>• Sets the SSSR.EOC status bit which must be cleared by software. If more data is received after the EOC bit was set (and EOC bit is still set), then the SSSR.PINT bit will be set to a 1. Once the SSSR.PINT bit is set, it must be cleared by programmers by writing a 1 to it. Clearing the SSSR.PINT bit also de-asserts the Peripheral Interrupt if it has been enabled (SSCR1.PINTE=1).</li> </ul> <p><b>Removing Trailing Bytes:</b></p> <p><b>Processor Based (SSCR1.TRAILING = 0):</b> This is the default method indicated by a zero in the SSCR1.TRAILING bit. In this case, no Receive DMA service request is generated. To read out the trailing bytes, software should wait for the Timeout Interrupt and then read all remaining entries as indicated by the SSSR.RFL and SSSR.RNE bits within the Enhanced SSP Status register (SSSR).</p> <p><b>Note:</b> To use the Trailing bytes feature through the processor, the Timeout Interrupt must be enabled by setting SSCR1.TINTE=1 (to enable the interrupt).</p> <p><b>DMA Based (SSCR1.TRAILING = 1):</b> When the DMA is to handle trailing bytes (SSCR1.TRAILING = 1), a DMA service request is automatically issued for the remaining number of samples left in the Receive buffer. The DMA will then empty the contents of the Receive buffer unless the DMA reaches the end of its Descriptor. If a Timeout occurs, the processor is only interrupted by means of a Timeout Interrupt if it has been enabled by setting SSCR1.TINTE=1.</p> <p>When handling trailing bytes by means of the DMA, if a timeout occurs and the receive FIFO is empty, an End-of-Receive (EOR) will be sent to the DMA Controller. If an EOC occurs at the time that the last sample is read out of the FIFO (the DMA descriptor chain was just exactly long enough), and the timeout counter is still running (that is, a time out has not occurred and the SSTO register is non-zero), then, when the time out does occur, the Enhanced SSP will generate a DMA request which will create an RAS interrupt from the DMA.</p> <p>0 = Processor based, trailing bytes are handled by processor 1 = DMA based, trailing bytes are handled by DMA</p>
21	<p><b>Transmit Service Request Enable (TSRE)</b>—R/W. This bit enables the Transmit FIFO DMA Service Request. When SSCR1.TSRE=0, the DMA Service Request is masked, and the state of the transmit FIFO service request (SSSR.TFS) bit within the Enhanced SSP Status register is ignored. When SSCR1.TSRE=1, the DMA Service Request is enabled, and whenever SSSR.TFS is set to one, a DMA Service Request is made to the DMA. Programming SSCR1.TSRE=0 does not affect the current state of SSSR.TFS or the ability of the Transmit FIFO logic to set and clear SSSR.TFS—it only blocks the generation of the DMA Service Request. Also, the state of SSCR1.TSRE does not affect the generation of the Interrupt, which is asserted whenever the SSSR.TFS is set to 1.</p> <p><b>Note:</b> TSRE and RSRE is automatically cleared by hardware when DMA transaction if finished.</p> <p>0 = DMA Service Request is disabled 1 = DMA Service Request is enabled</p>



Bit	Description
20	<b>Receive Service Request Enable (RSRE)</b> —R/W. This bit enables the Receive FIFO DMA Service Request. When SSCR1.RSRE=0, the DMA Service Request is masked, and the state of the receive FIFO service request SSSR.RFS bit within the Enhanced SSP Status register is ignored. When SSCR1.RSRE=1, the DMA Service Request is enabled, and whenever SSSR.RFS is set to one, a DMA Service Request is made to the DMA. Programming SSCR1.RSRE=0 does not affect the current state of SSSR.RFS or the ability of the Receive FIFO logic to set and clear SSSR.RFS—it only blocks the generation of the DMA Service Request. Also, the state of SSCR1.RFRS does not affect the generation of the Interrupt, which is asserted whenever the SSSR.RFS is set to 1. 0 = DMA Service Request is disabled 1 = DMA Service Request is enabled
19	<b>Receiver Timeout Interrupt Enable (TINTE)</b> —R/W. This bit is used to mask or enable the Receiver Timeout Interrupt. When SSCR1.TINTE=0, the Interrupt is masked and the state of the SSSR.TINT bit is ignored by the Interrupt controller. When SSCR1.TINTE=1, the Interrupt is enabled, and whenever the SSSR.TINT bit is set to one an Interrupt request is made to the Interrupt controller. Programming SSCR1.TINTE=0 does not affect the current state of the SSSR.TINT or the ability of logic to set and clear the SSSR.TINT; it only blocks the generation of the Interrupt request. 0 = Receiver Timeout interrupts are disabled 1 = Receiver Timeout interrupts are enabled
18	<b>Peripheral Trailing Byte Interrupts Enable (PINTE)</b> —R/W. This bit is used to enable the Peripheral Trailing Byte Interrupt. When SSCR1.PINTE=0, the Interrupt is masked and the state of the SSSR.PINT bit is ignored by the Interrupt controller. When SSCR1.PINTE=1, the Interrupt is enabled, and whenever the SSSR.PINT bit is set to 1, an Interrupt request is made to the Interrupt controller. Programming SSCR1.PINTE=0 does not affect the current state of the SSSR.PINT or the ability of logic to set and clear the SSSR.PINT; it only blocks the generation of the Interrupt request. 0 = Peripheral Trailing Byte Interrupts are disabled 1 = Peripheral Trailing Byte Interrupts are enabled
17	Reserved
16	<b>Invert Frame Signal (IFS)</b> —R/W. This bit (when set) will invert the frame signal coming into or going out of the Enhanced SSP. <b>Note:</b> Changing polarity here does not affect software override reg_SPI_CS_CONTROL 0 = Frame polarity is determined by SSP format and PSP polarity bits 1 = Frame signal will be inverted from the normal SSP frame signal
15:5	Reserved
4	<b>Motorola SPI CLK phase setting (SPH)</b> —R/W. This bit determines the phase relationship between the SSPSCLK and the serial frame (SSPSFRM) pins when the Motorola* SPI format is selected (SSCR0.FRF=00). When SSCR1.SPH=0, SSPSCLK remains in its Inactive/Idle state (as determined by the SSCR1.SPO setting) for one full cycle after SSPSFRM is asserted low at the beginning of a frame. SSPSCLK continues to transition for the rest of the frame and is then held in its Inactive state for one-half of an SSPSCLK period before SSPSFRM is de-asserted high at the end of the frame. When SSCR1.SPH=1, SSPSCLK remains in its Inactive/Idle state (as determined by the SSCR1.SPO setting) for one-half cycle after SSPSFRM is asserted low at the beginning of a frame. SSPSCLK continues to transition for the remainder of the frame, and is then held in its Inactive state for one full SSPSCLK period before SSPSFRM is de-asserted high at the end of the frame. The combination of the SSCR1.SPO and SSCR1.SPH settings determines when SSPSCLK is active during the assertion of SSPSFRM, and which SSPSCLK edge transmits and receives data on the SSPTXD and SSPRXD pins. When SSCR1.SPO and SSCR1.SPH are programmed to the same value (both 0 or both 1), Transmit data is driven on the falling edge of SSPSCLK, and Receive data is latched on the rising edge of SSPSCLK. When SSCR1.SPO and SSCR1.SPH are programmed to opposite values (one 0 and the other 1), Transmit data is driven on the rising edge of SSPSCLK, and Receive data is latched on the falling edge of SSPSCLK. <b>Note:</b> The SSCR1.SPH is ignored for all data frame formats except for the Motorola* SPI format (SSCR0.FRF=00). 0 = SSPSCLK is inactive one cycle at the start of a frame and cycle at the end of a frame 1 = SSPSCLK is inactive for one half cycle at the start of a frame and one cycle at the end of a frame



Bit	Description
3	<b>Motorola SPI polarity setting (SPO)</b> —R/W. This bit selects the polarity of the inactive state of the SSPSCLK pin when the Motorola* SPI format is selected (SSCR0.FRF=00). For SSCR1.SPO=0, the SSPSCLK is held low in the Inactive or Idle state when the Enhanced SSP is not transmitting/receiving data. For SSCR1.SPO=1, the SSPSCLK is held high during the Inactive/Idle state. The programmed setting of the SSCR1.SPO alone does not determine which SSPSCLK edge transmits or receives data—the SSCR1.SPO setting in combination with the SSPSCLK phase bit SSCR1.SPH does. 0 = The inactive or idle state of SSPSCLK is low 1 = The inactive or idle state of SSPSCLK is high
2	Reserved
1	<b>Transmit FIFO Interrupt Enable (TIE)</b> —R/W. This bit enables the Transmit FIFO Service Request Interrupt. When SSCR1.TIE=0, the Interrupt is masked, and the state of the transmit FIFO service request (SSSR.TFS) bit within the Enhanced SSP Status register is ignored. When SSCR1.TIE=1, the Interrupt is enabled, and whenever SSSR.TFS is set to one, an Interrupt request is made to the Interrupt controller. Programming SSCR1.TIE=0 does not affect the current state of SSSR.TFS or the ability of the Transmit FIFO logic to set and clear SSSR.TFS; it only blocks the generation of the Interrupt request. Also, the state of SSCR1.TIE does not affect the generation of the Transmit FIFO DMA service request, which is asserted whenever the SSSR.TFS is set to 1. 0 = Transmit FIFO level interrupt is disabled 1 = Transmit FIFO level interrupt is enabled
0	<b>Receive FIFO Interrupt Enable (RIE)</b> —R/W. This bit enables the Receive FIFO Service Request Interrupt. When SSCR1.RIE=0, the Interrupt is masked, and the state of the receive FIFO service request SSSR.RFS bit within the Enhanced SSP Status register is ignored. When SSCR1.RIE=1, the Interrupt is enabled, and whenever SSSR.RFS is set to one, an Interrupt request is made to the Interrupt controller. Programming SSCR1.RIE=0 does not affect the current state of SSSR.RFS or the ability of the Receive FIFO logic to set and clear SSSR.RFS—it only blocks the generation of the Interrupt request. Also, the state of SSCR1.RIE does not affect the generation of the Receive FIFO DMA service request, which is asserted whenever the SSSR.RFS bit is set to 1. 0 = Receive FIFO level interrupt is disabled 1 = Receive FIFO level interrupt is enabled

### 23.2.3 SSSR—Controller Status Register (GSPI—D21:F3/F4)

Register Offset: BAR + 08h  
Default Value: 0000F004h

Attribute: RO, R/WC  
Size: 32 bits

Bit	Description
31:22	Reserved
21	<b>Transmit FIFO Under Run (TUR)</b> —R/WC. This bit indicates that the transmitter tried to send data from the Transmit FIFO when the Transmit FIFO was empty. When the SSSR.TUR bit is set, an Interrupt is generated to the processor that can be locally masked by the SSCR0.TIM bit. The setting of the SSSR.TUR bit does not, however, generate any DMA service request. The SSSR.TUR bit remains set until cleared by software writing a 1 to this bit which will also reset its Interrupt request; writing a 0 to this bit does not affect SSSR.TUR status. This bit can only be set when the Enhanced SSP is a slave to the FRAME signal (SSCR1.SFRMDIR = 1), or if the Enhanced SSP is a master to the FRAME signal and the Enhanced SSP is in Network mode, and will not be set if the Enhanced SSP is in Receive-Without-Transmit mode (SSCR1.RWOT = 1). 0 = Transmit FIFO has not experienced an under run 1 = Attempted read from the transmit FIFO when the FIFO was empty, request interrupt
20	<b>End of Chain (EOC)</b> End of Chain—R/WC. This bit indicates that the DMA has signaled an end of chain. The SSSR.EOC=1 indicates that the DMA has signaled an end of chain. The SSSR.EOC=0 indicates that the DMA has not signaled an end-of-chain condition. The SSSR.EOC bit is cleared by programmers by writing a 1 to it. The end-of-chain event indicates that the DMA descriptor for the Receive FIFO is ending and is described in more detail in the DMA chapter. This event will require software intervention if data remains in the Receive FIFO. 0 = DMA has not signaled an end of chain condition 1 = DMA has signaled an end of chain condition



Bit	Description
19	<b>Receiver Timeout Interrupt (TINT)</b> —R/WC. This bit is set to 1 when the Receive FIFO has been idle (no samples received) for a period of time defined by the value programmed within the Timeout register (SSTO). This interrupt can be masked by the SSCR1.TINTE bit. The SSSR.TINT bit is cleared by programmers by writing a 1 to it. 0 = No receiver Timeout pending. 1 = Receiver Timeout pending Receive FIFO has been idle for period defined by SSTO
18	<b>Peripheral Trailing Byte Interrupt (PINT)</b> —R/WC. 0 = No peripheral trailing byte interrupt pending 1 = Peripheral trailing byte interrupt pending
17:8	Reserved
7	<b>Receive FIFO Overrun (ROR)</b> —R/WC. This bit is set when the Receive logic attempts to place data into the Receive FIFO after it has been completely filled. If the Receive FIFO is full and new data is received, the SSSR.ROR bit is set, and the newly received data is discarded. This process is repeated for each new data.chunk received until at least one empty FIFO entry exists. When the SSSR.ROR bit is set, an Interrupt is generated to the processor that can be locally masked by the SSCR0.RIM bit. The setting of the SSSR.ROR bit does not, however, generate any DMA service request. The SSSR.ROR bit remains set until cleared by software writing a 1 to this bit which will also reset its Interrupt request; writing a 0 to this bit does not affect SSSR.ROR status. 0 = Receive FIFO has not experienced an overrun 1 = Attempted data write to full receive FIFO, request interrupt
6	<b>Receive FIFO Service Request (RFS)</b> —RO. This bit is a read-only bit that is set to generate an Interrupt when the Receive FIFO requires service to prevent an overrun. SSSR.RFS is set any time the Receive FIFO has more entries of valid data than the number indicated by the Receive FIFO Trigger threshold, and it is cleared when it has the same or fewer entries than the threshold value. When the SSSR.RFS bit is set, an Interrupt is generated unless the receive FIFO interrupt request enable (SSCR1.RIE) bit is cleared. Also, the setting of the SSSR.RFS bit will signal a DMA service request if the SSCR1.RSRE bit is set. After the processor or DMA reads the FIFO such that it has the same or fewer entries than the SSCR1.RFT value, the SSSR.RFS flag (and the service request and/or Interrupt) is automatically cleared. Software should not set both the SSCR1.RSRE and the SSCR1.RIE bits. 0 = Receive FIFO level is at or below RFT threshold (RFT), or controller disabled 1 = Receive FIFO level exceeds RFT threshold (RFT), request interrupt
5	<b>Transmit FIFO Service Request (TFS)</b> —RO. The transmit FIFO service request flag SSSR.TFS is a read-only bit that is set to generate an Interrupt when the Transmit FIFO requires service to prevent an underrun. SSSR.TFS is set any time the Transmit FIFO has the same or fewer entries of valid data than indicated by the Transmit FIFO Trigger threshold, and it is cleared when it has more entries of valid data than the threshold value (the service request is triggered when the number of FIFO entries is less than or equal to 1 + TFT). When the SSSR.TFS bit is set, an Interrupt is generated unless the transmit FIFO interrupt request enable (SSCR1.TIE) bit is cleared. Also, the setting of the SSSR.TFS bit will generate a DMA service request if the SSCR1.TSRE bit was set. After the processor or the DMA fills the FIFO such that it exceeds the threshold, the SSSR.TFS flag (and the service request and/or Interrupt) is automatically cleared. If the threshold has not been exceeded, another request will be made. Software should not set both the SSCR1.TSRE and the SSCR1.TIE bits. 0 = Transmit FIFO level exceeds the TFT threshold (TFT), or controller disabled 1 = Transmit FIFO level is at or below TFT threshold (TFT), request interrupt
4	<b>SSP Busy (BSY)</b> —RO. This is a read-only bit that is set when the SSP is actively transmitting and/or receiving data, and is cleared when the SSP is idle or disabled (SSCR0.SSE=0). This bit does not generate an Interrupt. 0 = Controller is idle or disabled 1 = Controller currently transmitting or receiving a frame
3	<b>Receive FIFO Not Empty (RNE)</b> —RO. The bit is a read-only bit that is set whenever the Receive FIFO contains one or more entries of valid data, and is cleared when it no longer contains any valid data. This bit can be polled when using programmed I/O to remove remaining bytes of data from the Receive FIFO since processor Interrupt requests are made only when the Receive FIFO Trigger threshold has been met or exceeded. This bit does not generate an Interrupt. 0 = Receive FIFO is empty 1 = Receive FIFO is not empty



Bit	Description
2	<b>Transmit FIFO Not Full (TNF)</b> —RO. This bit is a read-only bit that is set whenever the Receive FIFO contains one or more entries of valid data, and is cleared when it no longer contains any valid data. This bit can be polled when using programmed I/O to remove remaining bytes of data from the Receive FIFO since processor Interrupt requests are made only when the Receive FIFO Trigger threshold has been met or exceeded. This bit does not generate an Interrupt. 0 = Transmit FIFO is full 1 = Transmit FIFO is not full
1:0	Reserved

### 23.2.4 SSDR—Data Register (GSPI—D21:F3/F4)

Register Offset: BAR + 10h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

The Enhanced SSP Data registers are single address locations that Read-Write data transfers can access. The SSDR represents two physical registers: the first is temporary storage for data on its way out through the Transmit FIFO; the other is temporary storage for data coming in through the Receive FIFO. As the system accesses the register, FIFO Control logic transfers data automatically between register and FIFO as fast as the system moves it. Data in the FIFO shifts up or down to accommodate the new word (unless it's an attempted Write to a full Transmit FIFO). Status bits (such as SSSR.RNE, and SSSR.TNF) show users whether the FIFO is full, above/below a programmable FIFO trigger threshold, or empty. For Transmit data transfers (Write from system to SSP peripheral), the register can be loaded (written) by the system processor anytime it falls below its threshold level when using programmed I/O. When a data size of less than 32 bits is selected, users should not left-justify data written to the Transmit FIFO. Transmit logic left-justifies the data and ignores any unused bits. Received data of less than 32 bits is automatically right-justified in the Receive FIFO.

Bit	Description
31:0	<b>Data (DAT)</b> —RO Data word to be written to/read from transmit/receive FIFO.

### 23.2.5 SSTO—Timeout Register (GSPI—D21:F3/F4)

Register Offset: BAR + 28h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

The Enhanced SSP Timeout registers have single bit fields that specify the Timeout value used to signal a period of inactivity within the Receive FIFO. Writes to reserved bits must be zeroes, and Read value of these bits is undetermined.

Bit	Description
31:24	Reserved
23:0	<b>Timeout (TIMEOUT)</b> —R/W. Timeout Value Is the value that defines the timeout interval for the Receive FIFO, interval is given by given by TIMEOUT/Peripheral Clock Frequency. For Example: This value needs to be set in case the MSize of the DMA is not equal to the Threshold of the FIFO. In such a case we calculate the TIMEOUT value to be the time to transfer the smallest size of data, which is 24'h00029. The value need to be optimum (not to small or too large).



### 23.2.6 SITF—SPI Transmit FIFO Register (GSPI—D21:F3/F4)

Register Offset: BAR + 44h  
Default Value: 00000000h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31:25	Reserved
24:16	<b>SPI Transmit FIFO Level (SITFL)</b> —RO Number of entries in SPI Transmit FIFO.
15:8	<b>Low Water Mark Transmit FIFO (LWMTF)</b> —R/W Sets the low water mark of the SPI transmit FIFO.  00000000'b = 1 entry ..... 11111111'b = 255 entries
7:0	<b>High Water Mark Transmit FIFO (HWMTF)</b> —R/W Sets the water mark of the SPI transmit FIFO.  00000000'b = 1 entry ..... 11111111'b = 255 entries

### 23.2.7 SIRF—SPI Receive FIFO Register (GSPI—D21:F3/F4)

Register Offset: BAR + 48h  
Default Value: 00000000h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31:17	Reserved
16:8	<b>SPI Receive FIFO Level (SIRFL)</b> —RO Number of entries in SPI receive FIFO.
7:0	<b>Water Mark Receive FIFO (WMRF)</b> —R/W Sets the high water mark of the SPI receive FIFO  00000000'b = 1 entry ..... 11111111'b = 255 entries

### 23.2.8 CLK\_PARM—Clock Parameter Register (GSPI—D21:F3/F4)

Register Offset: BAR + 800h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31	<b>Clock Update (CLK_UPDATE)</b> —R/W 0 = No M/N clock update 1 = M/N clock gets updated with N-VAL and M-VAL
30:16	<b>N_VAL</b> —R/W. This is the denominator value for the M over N divider logic that creates the SPI_CLK_OUT for the SSP. (M/N value used to generate input clk to SSP).  <b>Note:</b> The M/N is set to pass through (100 MHz) by software and the internal SSP divider is used. M=N=9154. SSP SSCR0 (MBAR0+0x0), Bits 8:19, SCR = 3 for 25 MHz operation
15:1	<b>M_VAL</b> —R/W. The numerator value for the M over N divider logic that creates the SPI_CLK_OUT for the SSP.  <b>Note:</b> The M/N is set to pass through (100 MHz) by the software and the internal SSP divider is used. M=N=9154. SSP SSCR0 (MBAR0+0x0), Bits 8:19, SCR = 3 for 25 MHz operation:
0	<b>Clock Enable (LTR_EN)</b> —R/W 0 = M/N clock disabled 1 = M/N clock enabled

### 23.2.9 RESET—Reset Register (GSPI—D21:F3/F4)

Register Offset: BAR + 804h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:2	Reserved
1:0	<b>Reset SSP (RESET_SSP)</b> —R/W. This field is used to reset the SSP Host Controller by software control. All SSP Configuration State and Operational State will be forced to the Default state. There is no timing requirement (software can assert and de-assert in back to back transactions). This reset does NOT impact the LPSS cluster level settings by BIOS, the PCI configuration header information, DMA channel configuration, and interrupt assignment/mapping/and so forth. Driver should re-initialize registers related to Driver context following an SSP host controller reset. 00 = SSP Host Controller is NOT at reset (Reset Released) 01 = Reserved 10 = Reserved 11 = SSP Host Controller is in reset (Reset Asserted)



### 23.2.10 GEN—General Register (GSPI—D21:F3/F4)

Register Offset: BAR + 808h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:26	Reserved
25	<b>Terminate TX on RX Full Disable</b> —R/W. Allows the synchronization of the TX FIFO to the RX FIFO. In Full duplex operation prevents an RX FIFO overrun condition.  <b>Note:</b> If it is desired to operate transmit without reading from the RX FIFO then this feature must be disabled. 0= Enabled TXFIFO to RXFIFO Sync 1= Disabled TXFIFO to RXFIFO Sync
24:3	Reserved
2	<b>LTR Mode (LTR_MODE)</b> —R/W 0 = Auto Mode 1 = Software Mode  In the auto mode, the BIOS will write to the "host controllers Auto LTR register (offset 0x814) with the active state LTR value and Software LTR register (offset 0x810) with the idle state LTR value. When the host controller goes active, the reported LTR value forwarded to the coalescing logic (see below) will be the value in the Auto LTR register. When the host controller goes inactive (Idle), the reported LTR value will be taken from the Software LTR register (offset 0x810).  In software mode the software will write to the host controllers Software LTR register (offset 0x810). The value will then be forwarded to the hardware coalescing logic (see below). It is the responsibility of software to update the LTR with the appropriate value.  <b>Note:</b> If software does not update the Software LTR register, no LTR value will be forwarded to the coalescing logic (see below), effectively disabling LTR generation for this module. Hardware coalescing logic is used to reduce the six LTR values that are generated from the various Intel® Serial Interface modules (2xI2C, 2xSPI, 2xUART) to a single message. The 6 to 1 reduction is achieved by hardware selecting the lowest LTR value at the time of each update.
1:0	Reserved



### 23.2.11 SW\_LTR\_VAL—Software LTR Value Register (GSPI—D21:F3/F4)

Register Offset: BAR + 810h  
Default Value: 00000800h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31	<b>Non Snoop Requirement (NON_SNOOP_REQUIREMENT)</b> —RO. If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (that is, it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	Reserved
28:26	<b>Non Snoop Latency Scale (NON_SNOOP_LATENCY_SCALE)</b> —RO. Support for codes 010 (1 µs) or 011 (32 µs) for Snoop Latency Scale (1 µs – 32 ms total span) only. Writes to this field that do not match those values will be dropped completely; next read will return previous value.
25:16	<b>Non Snoop Value (NON_SNOOP_VALUE)</b> —RO. 10-bit latency value
15	<b>Snoop Requirement (SNOOP_REQUIREMENT)</b> —R/W. If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (that is, it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	Reserved
12:10	<b>Snoop Latency Scale (SNOOP_LATENCY_SCALE)</b> —R/W. Support for codes 010 (1 µs) or 011 (32 µs) for Snoop Latency Scale (1 µs – 32 ms total span) only. Writes to this field that do not match those values will be dropped completely; next read will return previous value.
9:0	<b>Snoop Value (SNOOP_VALUE)</b> —R/W. 10-bit latency value

### 23.2.12 AUTO\_LTR\_VAL—Auto LTR Value Register (GSPI—D21:F3/F4)

Register Offset: BAR + 814h  
Default Value: 00000800h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31	<b>Non Snoop Requirement (NON_SNOOP_REQUIREMENT)</b> —RO. If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (that is, it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	Reserved
28:26	<b>Non Snoop Latency Scale (NON_SNOOP_LATENCY_SCALE)</b> —RO. Support for codes 010 (1 µs) or 011 (32 µs) for Snoop Latency Scale (1 µs – 32 ms total span) only. Writes to this field that do not match those values will be dropped completely; next read will return previous value.
25:16	<b>Non Snoop Value (NON_SNOOP_VALUE)</b> —RO. 10-bit latency value
15	<b>Snoop Requirement (SNOOP_REQUIREMENT)</b> —R/W. If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (that is, it can wait for service indefinitely). If the 10-bit latency value is zero, it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	Reserved
12:10	<b>Snoop Latency Scale (SNOOP_LATENCY_SCALE)</b> —R/W. Support for codes 010 (1 µs) or 011 (32 µs) for Snoop Latency Scale (1 µs – 32 ms total span) only. Writes to this field that do not match those values will be dropped completely; next read will return previous value.
9:0	<b>Snoop Value (SNOOP_VALUE)</b> —R/W. 10-bit latency value



### 23.2.13 SPI\_CS\_CONTROL—SPI Chip Select Control Register (GSPI—D21:F3/F4)

Register Offset: BAR + 818h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:2	Reserved
1	<b>SPI Chip Select Software Control (CS_STATE)</b> —R/W. Manual software control of SPI Chip Select. 0 = HCS is set to low 1 = CS is set to high
0	<b>SPI Chip Select Mode Selection (CS_MODE)</b> —R/W. 0 = Hardware Mode. CS is under SSP control. 1 = Software Mode. CS is under software control using CS_STATE bit

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# 24 Intel® Serial I/O SDIO Controller Registers (D23:F0)

## 24.1 PCI Configuration Registers (SDIO—D23:F0)

Table 24-1. SDIO Controller PCI Register Address Map (SDIO—D23:F0)

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	0000	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	0010h	RO, R/WC
08h-0Bh	RID	Revision Identification	See register description	RO
13h-10h	SDIOMBAR0	SDIO Memory Base Address 0	00000000h	RO, R/W
17h-14h	SDIOMBAR1	SDIO Memory Base Address 1	00000000h	RO, R/W
2Ch-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
34h-35h	PWRCAPTR	Power Capabilities Pointer	80h	RO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	01h	RO

**Note:** Registers that are not shown should be treated as Reserved.

### 24.1.1 VID—Vendor Identification Register (SDIO—D23:F0)

Address: 00h-01h Attribute: RO  
 Default Value: 0000h Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO

### 24.1.2 DID—Device Identification Register (SDIO—D23:F0)

Address: 02h–03h      Attribute: RO  
Default Value: 9CB5h      Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the PCH SDIO controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

### 24.1.3 PCICMD—PCI Command Register (SDIO—D23:F0)

Address: 04h–05h      Attributes: R/W  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable</b> —R/W 0 = Enable 1 = Disables SMBus to assert its PIRQB# signal.
9	Reserved
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7:3	Reserved
2	<b>Bus Master Enable (BME)</b> —R/W
1	<b>Memory Space Enable (MSE)</b> —R/W 0 = Disables memory mapped configuration space. 1 = Enables memory mapped configuration space.
0	Reserved

#### 24.1.4 PCISTS—PCI Status Register (SDIO—D23:F0)

Address: 06h–07h      Attributes: RO, R/WC  
 Default Value: 0010h      Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Reserved.
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No system error detected. 1 = System error detected.
13	<b>Received Master Abort (RMA)</b> —R/WC
12	<b>Received Target Abort (RTA)</b> —R/WC
11	<b>Signaled Target Abort (STA)</b> —R/WC
10:5	Reserved
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 1 to indicate there are capability list structures in this function.
3	<b>Interrupt Status (INTS)</b> —RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the PCI Command register.
2:0	Reserved

#### 24.1.5 RID—Revision Identification and Class Code Register (SDIO—D23:F0)

Offset Address: 08h–0Bh      Attribute: RO  
 Default Value: See bit description      Size: 32 bits

Bit	Description
31:8	<b>Class Code</b> —RO. Hardwired to 080501h
7:0	<b>Revision ID</b> —RO. See <a href="#">Section 1.4</a> for the value of the RID Register.

#### 24.1.6 SDIOMBAR0—SDIO Memory Base Address 0 Register (SDIO—D33:F0)

Address Offset: 10–13h      Attributes: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:12	<b>Base Address 0</b> —R/W. Provides system memory base address for the SDIO logic.
11:4	Reserved
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that SDIOMBAR0 is not prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO.
0	<b>Memory Space Indicator</b> —RO. This read-only bit always is 0, indicating that the SDIO logic is Memory mapped.

### 24.1.7 SMBMBAR1—SDIO Memory Base Address 1 Register (SDIO—D23:F0)

Address Offset: 14h–17h  
Default Value: 00000000h

Attributes: RO, R/W  
Size: 32 bits

Bit	Description
31:12	<b>Base Address 1</b> —R/W. Provides system memory base address for the PCH SDIO logic.
11:4	Reserved
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that SDIOMBAR1 is not prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO.
0	<b>Memory Space Indicator 1</b> —RO. This read-only bit always is 0, indicating that the SDIO logic is Memory mapped.

### 24.1.8 SVID—Subsystem Vendor Identification Register (SDIO—D23:F0)

Address Offset: 2Ch–2Dh  
Default Value: 0000h

Attribute: R/WO  
Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —R/WO. The SVID register, in combination with the Subsystem ID (SID) register, enables the Operating System (OS) to distinguish subsystems from each other.  <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 24.1.9 SID—Subsystem Identification Register (SDIO—D23:F0)

Address Offset: 2Eh–2Fh  
Default Value: 0000h

Attribute: R/WO  
Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other.  <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 24.1.10 PWRCAPPTR—Power Capabilities Pointer Register (SDIO—D23:F0)

Address Offset: 34h–35h  
Default Value: 80h

Attribute: RO  
Size: 8 bits

Bit	Description
7:0	<b>Power Capabilities (CAPPTR_POWER)</b> —RO

### 24.1.11 INT\_LN—Interrupt Line Register (SDIO—D23:F0)

Address Offset: 3Ch  
Default Value: 00h

Attributes: R/W  
Size: 8 bits

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is to communicate to software the interrupt line that the interrupt pin is connected to.

### 24.1.12 INT\_PN—Interrupt Pin Register (SMBus—D31:F3)

Address Offset: 3Dh  
Default Value: 01h

Attributes: RO  
Size: 8 bits

Bit	Description
7:4	Reserved
3:0	<b>Interrupt PIN (INT_PN)</b> —RO

## 24.2 SDIO Memory Mapped I/O Registers

The SDIO MMIO registers (see Table 24-2) can be accessed through BAR0 or through BAR1 when in ACPI mode (when PCI Configuration space is hidden). BAR0 and BAR1 are located in PCI configuration space.

**Note:** Only 32-bit operation is supported.

**Note:** The registers documented in this section are common registers for SDIO interface. As the PCH SDIO only supports Wi-Fi implementation (for example, the interface is not intended for general-purpose connections, such as SD cards), certain registers may not apply to the functionality that the PCH SDIO supports.

**Table 24-2. SDIO Memory Mapped I/O Register Address Map (Sheet 1 of 2)**

BAR + Offset	Mnemonic	Register Name	Default	Attribute
00h	SYS_ADR	SDMA System Address	00000000h	R/W
04h	BLK_SIZE	Block Size	0000h	R/W
06h	BLK_CNT	Block Count	0000h	R/W
08h	ARGUMENT	Argument	00000000h	R/W
0Ch	TX_MODE	Transfer Mode	0000h	R/W, RO
0Eh	CMD	Command	0000h	R/W, RO
10h	RESP0	Respond 0	00000000h	RO
14h	RESP1	Respond 1	00000000h	RO
18h	RESP2	Respond 2	00000000h	RO
1Ch	RESP3	Respond 3	00000000h	RO
20h	BUF_DATA_PORT	Buffer Data Port	00000000h	R/W
24h	PRE_STATE	Present State	1FFF0000h	RO
28h	HOST_CTRL	Host Control	00h	R/W
29h	PWR_CTRL	Power Control	00h	R/W, RO
2Ah	BLK_GAP_CTRL	Block Gap Control	00h	R/W, RO
2Bh	WAKEUP_CTRL	Wakeup Control	00h	R/W, RO
2Ch	CLK_CTRL	Clock Control	0000h	R/W, RO
2Eh	TIMEOUT_CTRL	Timeout Control	00h	R/W, RO
2Fh	SW_RST	Software Reset	00h	R/W, R/ WC, RO
30h	NML_INT_STAT	Normal Interrupt Status	0000h	R/ WC, RO
32h	ERR_INT_STAT	Error Interrupt Status	0000h	R/ WC, RO
34h	NML_INT_STAT_EN	Normal Interrupt Status Enable	0000h	R/W, RO
36h	ERR_INT_STAT_EN	Error Interrupt Status Enable	0000h	R/W, RO
38h	NML_INT_SIG_EN	Normal Interrupt Signal Enable	0000h	R/W, RO
3Ah	ERR_INT_SIG_EN	Error Interrupt Signal Enable	0000h	R/W, RO
3Ch	CMD12_EER_STAT	Auto CMD12 Error Status	0000h	RO
3E	HOST_CTL_2	Host Controller 2	0000	R/W, RO
40h	CAP	Capabilities	Hardware INIT	RO

**Table 24-2. SDIO Memory Mapped I/O Register Address Map (Sheet 2 of 2)**

BAR + Offset	Mnemonic	Register Name	Default	Attribute
44h	CAP2	Capabilities 2	Hardware INIT	RO
48h	MAX_CUR_CAP	Maximum Current Capabilities	00000000h	RO
50h	FORCE_EVENT_CMD_12_ERR_STAT	Force Event for Auto CMD12 Error Status	0000h	R/W, RO
52h	FORCE_EVENT_ERR_INT_STAT	Force Event for Error Interrupt Status	0000h	R/W, RO
54h	ADMA_ERR_STAT	ADMA Error Status	00h	RO
58h	ADMA_SYS_ADDR	System Address	00000000h	R/W
60h	RESET_VAL	Preset Values 0	0002h	RO
70h	BOOT_TO_CTRL	Boot Timeout Control	00000000h	R/W
0E0h	SHARED-BUS	Shared Bus Control Register	00000000	R/W, RO
0F0h	SPI_INT_SUP	SPI Interrupt Support	00h	R/W
0FCh	SLOT_INT_STAT	Slot Interrupt Status	0000	RO
1008h	GEN	General	00000000h	R/W, RO
1010h	SW_LTR_VAL	Software LTR Value	00000800h	R/W, RO
1014h	AUTO_LTR_VAL	Auto LTR Value	00000800h	R/W, RO
102Ch	RX_DELAY_SDR_MODE	Receive Delay for Default Mode and SDR25	00000204h	WO, RO
1034h	RX_DELAY_DDR50_MODE	Receive Delay for DDR50	0000030Eh	WO, RO



### 24.2.1 SYS\_ADR—SDMA System Address Register (SDIO—D23:F0)

Register Offset: BAR + 00h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

This register contains the physical system memory address used for DMA transfer.

Bit	Description
31:0	<p><b>SYS_ADR</b>—R/W. This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23.</p> <p>1. <b>SDMA System Address</b> This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (for example, after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates a DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (003h) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register</p> <p>2. <b>Argument 2</b> This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without ADMA, the available block count value is limited by the Block Count register. 65535 blocks is the maximum value in this case.</p>

## 24.2.2 BLK\_SIZE—Block Size Register (SDIO—D23:F0)

Register Offset: BAR + 04h  
Default Value: 0000h

Attribute: R/W  
Size: 16-bits

Bit	Description
15	Reserved
14:12	<b>HOST SDMA BUFFER SIZE</b> —R/W. To perform long DMA transfers, the System Address register shall be updated at every system boundary during the DMA transfer. These bits specify the size of contiguous buffer in the system memory. The DMA transfer shall wait at the every boundary specified by these fields and the host controller generates the DMA Interrupt to request the host driver to update the System Address register. These bits shall support when the DMA Support in the Capabilities register is set to 1 and this function is active when the DMA Enable in the Transfer Mode register is set to 1. 000b = 4KB (Detects A11 Carry out) 001b = 8KB (Detects A12 Carry out) 010b = 16KB (Detects A13 Carry out) 011b = 32KB (Detects A14 Carry out) 100b = 64KB (Detects A15 Carry out) 101b = 128KB (Detects A16 Carry out) 110b = 256KB (Detects A17 Carry out) 111b = 512KB (Detects A18 Carry out)
11:0	<b>TRANSFER BLOCK SIZE (TR_BLK_SIZE)</b> —R/W. This register specifies the block size of data transfers for CMD17, CMD18, CMD24, CMD25, and CMD53. It can be accessed only if no transaction is executing (for example, after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. 0000h = No Data Transfer 0001h; 1 Byte 0002h = 2 Bytes 0003h = 3 Bytes 0004h = 4 Bytes ..... 01FFh = 511 Bytes 0200h = 512 Bytes 0800h = 2048 Bytes

## 24.2.3 BLK\_CNT—Block Count Register (SDIO—D23:F0)

Register Offset: BAR + 06h  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:0	<b>Block Count</b> —R/W. This register is enabled when Block Count Enable in the Transfer Mode register is set to 1 and is valid only for multiple block transfers. The HC decrements the block count after each block transfer and stops when the count reaches zero. It can be accessed only if no transaction is executing (that is, after a transaction has stopped). Read operations during transfer return an invalid value and write operations shall be ignored. When saving transfer context as a result of Suspend command, the number of blocks yet to be transferred can be determined by reading this register. When restoring transfer context prior to issuing a Resume command, the host driver shall restore the previously save block count. 0000h = Stop Count 0001h = 1 block 0002h = 2 blocks ..... FFFFh = 65535 blocks



#### 24.2.4 ARGUMENT—Argument Register (SDIO—D23:F0)

Register Offset: BAR + 08h      Attribute: R/W  
Default Value: 00000000h      Size: 32 bits

Bit	Description
31:0	<b>Command Argument</b> —R/W. This register contains the Command Argument.

#### 24.2.5 TX\_MODE—Transfer Mode Register (SDIO—D23:F0)

Register Offset: BAR + 0Ch      Attribute: R/W  
Default Value: 0000h      Size: 16 bits

Bit	Description
15:6	Reserved
5	<b>Block Select (BLK_SEL)</b> —R/W 0 = Single Block 1 = Multiple Block
4	<b>Data Transfer Direction Select (DATA_TR_DIR)</b> —R/W. This bit defines the direction of DAT line data transfers. 0 = Write (Host to Card) 1 = Read (Card to Host)
3:2	<b>Auto CMD Enable (BLK_CNT_EN)</b> —R/W. This field determines use of auto command functions. 00b = Auto Command Disabled 01b = Auto CMD12 Enable 10b = Auto CMD23 Enable 11b = Reserved
1	<b>Block Count Enable (BLK_CNT_EN)</b> —R/W. This bit is used to enable the Clock Count register, which is only relevant for multiple block transfers. 0 = Disable 1 = Enable
0	<b>DMA Enable (DMA_EN)</b> —R/W. DMA can be enabled only if the DMA Support bit in the Capabilities register is set. If this bit is set to 1, a DMA operation shall begin when the host driver writes to the upper byte of Command register (00Fh). 0 = Disable 1 = Enable

## 24.2.6 CMD—Command Register (SDIO—D23:F0)

Register Offset: BAR + 0Eh  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:14	Reserved
13:8	<b>Command Index (CMD_INDEX)</b> —R/W. These bits shall be set to the command number (CMD0-63, ACMD0-63) that is specified in bits 45-40 of the command format.
7:6	<b>Command Type (CMD_TYPE)</b> —R/W. There are three types of special commands: Suspend, Resume, and Abort. These bits shall be set to 00b for all other commands. <b>Suspend Command</b> If the Suspend command succeeds, the host controller shall assume the SD Bus has been released and that it is possible to issue the next command which uses the DAT line. The host controller shall de-assert Read Wait for read transactions and stop checking busy for write transactions. The Interrupt cycle shall start, in 4-bit mode. If the Suspend command fails, the host controller shall maintain its current state and the host driver shall restart the transfer by setting continue Request in Resume Command the Block Gap Control register. The host driver re-starts the data transfer by restoring the registers in the range of 000-00Dh. The HC shall check for busy before starting write transfers. <b>Abort Command</b> If this command is set when executing a read transfer, the HC shall stop reads to the buffer. If this command is set when executing a write transfer, the HC shall stop driving the DAT line. After issuing the Abort command, the host driver should issue a software reset. 00b = Normal 01b = Suspend 10b = Resume 11b = Abort
5	<b>Data Present Select (DATA_PR_SEL)</b> —R/W 0 = No data present. 1 = Data present. This bit is set to 1 to indicate that data is present and shall be transferred using the DAT line. It is set to 0 for the following: 1. Commands using only CMD line (for example, CMD52) 2. Commands with no data transfer but using busy signal on DAT0 line 3. Resume command
4	<b>Command Index Check Enable (CMD_INDEX_CHK_EN)</b> —R/W 0 = Disable. The Index field is not checked 1 = Enable. The host controller shall check the Index field in the response to see if it has the same value as the command index. If it is not, it is reported as a Command Index Error.
3	<b>Command CRC Check Enable (CMD_CRC_CHK_EN)</b> —R/W 0 = Disable. The CRC field is not checked. 1 = Enable. The host controller shall check the CRC field in the response. If an error is detected, it is reported as a Command CRC Error.
2	Reserved
1:0	<b>Responsive Type Select (RESP_TYPE_SEL)</b> —R/W 00 = No Response 01 = Response length 136 10 = Response length 48 11 = Response length 48; check Busy after response

### 24.2.7 RESP0—Response Register 0 (SDIO—D23:F0)

Register Offset: BAR + 10h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:0	<p><b>Command Response 0 (CMD_RESP0)</b>—RO. The Command Response is a 128-bit register field composed of CMD_RESP0 (LSB), CMD_RESP1, CMD_RESP2, CMD_RESP3 (MSB). CMD_RESP0 contains bits 31 to 0 of the Command Response. The following table describes the mapping of command responses from the SD Bus to this register for each response type. In the table, R[] refers to a bit range within the response data as transmitted on the SD Bus, REP[] refers to a bit range within the Response register.</p> <p>The following information describes the relation between the parameters and name: Response Type, Index Check Enable, CRC Check Enable, Name of Response Type</p> <p>00, 0, 0, No Response  01, 0, 1, R2  10, 0, 0, R3, R4  10, 1, 1, R1, R6, R5, R7  11, 1, 1, R1b, R5b</p> <p>The following information defines each response type  Kind of Response, Meaning of Response, Response Field, Response Register  R1, R1b (normal response), Card Status, R[39:8], REP[31:0]  R1b (Auto CMD12 response), Card Status for Auto CMD12, R[39:8], REP[127:96]  R1 (Auto CMD23 response), Card Status for Auto CMD23, R[39:8], REP [127:96]  R2 (CID, CSD Register), CID or CSD register including, R[127:8], REP[119:0]  R3 (OCR Register), OCR register for memory, R[39:8], REP[31:0]</p> <p>The following information shows the Response bit definition for each response type:  Kind of Response, Meaning of Response, Response Field, Response Register  R4 (OCR Register), OCR Register for I/O and so on, R[39:8], REP[31:0]  R5, R5b, SDIO Response, R[39:8], REP[31:0]  R6 (Published RCA response), New published RCA[31:16] and so on, R[39:8], REP[31:0]</p>

### 24.2.8 RESP1—Response Register 1 (SDIO—D23:F0)

Register Offset: BAR + 14h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:0	<b>Command Response 1(CMD_RESP1)</b> —RO. This field contains bits 63-32 of the Command Response.

### 24.2.9 RESP2—Response Register 2 (SDIO—D23:F0)

Register Offset: BAR + 18h Attribute: RO  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Command Response 2 (CMD_RESP2)</b> —RO. This field contains bits 95–64 of the Command Response.

### 24.2.10 RESP3—Response Register 3 (SDIO—D23:F0)

Register Offset: BAR + 1Ch Attribute: RO  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Command Response 3(CMD_RESP3)</b> —RO. This field contains bits 127–96 of the Command Response.

### 24.2.11 BUF\_DATA\_PORT—Buffer Data Port Register (SDIO—D23:F0)

Register Offset: BAR + 20h Attribute: R/W  
 Default Value: 00000000h Size: 32 bits

Bit	Description
31:0	<b>Buffer Data (BUF_DATA)</b> —R/W. The host controller buffer can be accessed through this Data Port register.

### 24.2.12 PRE\_STATE—Present State Register (SDIO—D23:F0)

Register Offset: BAR + 24h Attribute: RO  
 Default Value: 1FFF0000h Size: 32 bits

The host driver can get status of the host controller from this register.

Bit	Description
31:12	Reserved
11	<b>Buffer Read Enable (BUF_RD_EN)</b> —RO. This status is used for non-DMA read transfers. This read only flag indicates that valid data exists in the host side buffer status. If this bit is 1, readable data exists in the buffer. A change of this bit from 1 to 0 occurs when all the block data is read from the buffer. A change of this bit from 0 to 1 occurs when all the block data is ready in the buffer and generates the Buffer Read Ready Interrupt. 0 = Read Disable 1 = Read Enable
10	<b>Buffer Write Enable (BUF_WR_EN)</b> —RO. This status is used for non-DMA write transfers. This read-only flag indicates if space is available for write data. If this bit is 1, data can be written to the buffer. A change of this bit from 1 to 0 occurs when all the block data is written to the buffer. A change of this bit from 0 to 1 occurs when top of block data can be written to the buffer and generates the Buffer Write Ready Interrupt. 0 = Write Disable 1 = Write Enable.

Bit	Description
9	<p><b>Read Transfer Active (RD_TX_ACTIVE)</b>—RO. This status is used for detecting completion of a read transfer. This bit is set to 1 for either of the following conditions:</p> <ul style="list-style-type: none"> <li>• After the end bit of the read command</li> <li>• When writing a 1 to Continue Request in the Block Gap Control register to restart a read transfer</li> </ul> <p>This bit is cleared to 0 for either of the following conditions:</p> <ul style="list-style-type: none"> <li>• When the last data block as specified by block length is transferred to the system.</li> <li>• When all valid data blocks have been transferred to the system and no current block transfers are being sent as a result of the Stop At Block Gap Request set to 1. A transfer complete interrupt is generated when this bit changes to 0.</li> </ul> <p>0 = No valid data 1 = Transferring data</p>
8	<p><b>Write Transfer Active (WR_TX_ACTIVE)</b>—RO. This status indicates a write transfer is active. If this bit is 0, it means no valid write data exists in the HC. This bit is set in either of the following cases:</p> <ul style="list-style-type: none"> <li>• After the end bit of the write command.</li> <li>• When writing a 1 to Continue Request in the Block Gap Control register to restart a write transfer.</li> </ul> <p>This bit is cleared in either of the following cases:</p> <ul style="list-style-type: none"> <li>• After getting the CRC status of the last data block as specified by the transfer count (Single or Multiple)</li> <li>• After getting a CRC status of any block where data transmission is about to be stopped by a Stop At Block Gap Request.</li> </ul> <p>During a write transaction, a Block Gap Event interrupt is generated when this bit is changed to 0, as a result of the Stop At Block Gap Request being set. This status is useful for the host driver in determining when to issue commands during write busy.</p> <p>0 = No valid data 1 = Transferring data</p>
7:3	Reserved
2	<p><b>DAT Line Active (DAT_LN_ACTIVE)</b>—RO. This bit indicates whether one of the DAT lines on SD bus is in use.</p> <p>0 = DAT line inactive 1 = DAT line active</p>
1	<p><b>Command Inhibit Data (CMD_INHIBIT_DAT)</b>—RO. This status bit is generated if either the DAT Line Active or the Read transfer Active is set to 1. If this bit is 0, it indicates the HC can issue the next SD command. Commands with busy signal belong to Command Inhibit (DAT) (ex. R1b, R5b type).</p> <p>Changing from 1 to 0 generates a Transfer Complete interrupt in the Normal interrupt status register.</p> <p><b>Note:</b> The SD Host Driver can save registers in the range of 000-00Dh for a suspend transaction after this bit has changed from 1 to 0.</p> <p>1 = Cannot issue command which uses the DAT line 0 = Can issue command which uses the DAT line</p>
0	<p><b>Command Inhibit Command (CMD_INHIBIT_CMD)</b>—RO. If this bit is 0, it indicates the CMD line is not in use and the HC can issue a SD command using the CMD line. This bit is set immediately after the Command register (00Fh) is written. This bit is cleared when the command response is received.</p> <p>Even if the Command Inhibit (DAT) is set to 1, Commands using only the CMD line can be issued if this bit is 0. Changing from 1 to 0 generates a Command complete interrupt in the Normal Interrupt Status register. If the HC cannot issue the command because of a command conflict error or because of Command Not Issued By Auto CMD12 Error, this bit shall remain 1 and the Command Complete is not set. Status issuing Auto CMD12 is not read from this bit.</p> <p>Auto CMD12 and Auto CMD23 consist of two responses. In this case, this bit is not cleared by the response of CMD12 or CMD23 but cleared by the response of a read/write command. Status issuing Auto CMD12 is not read from this bit. So if a command is issued during Auto CMD12 operation, Host Controller shall manage to issue two commands: CMD12 and a command set by Command register.</p>

### 24.2.13 HOST\_CTRL—Host Control Register (SDIO—D23:F0)

Register Offset: BAR + 28h  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

Bit	Description
7:4	Reserved
5	<b>Extended Data Transfer Width (EXT_DATA_XFER_WIDTH)</b> —R/W. This bit controls 8-bit bus width mode for embedded device. Support of this function is indicated in 8-bit Support for Embedded Device in the Capabilities register. If a device supports 8-bit bus mode, this bit may be set to 1. If this bit is 0, bus width is controlled by Data Transfer Width in the Host Control 1 register. This bit is not effective when multiple devices are installed on a bus slot (Slot Type is set to 10b in the Capabilities register). In this case, each device bus width is controlled by Bus Width Preset field in the Shared Bus register. 0 = Bus Width is Selected by Data Transfer Width 1 = 8-bit Bus Width
4:3	<b>DMA Select (DMA_SEL)</b> —R/W. One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. 00 = SDMA is selected 01 = 32-bit Address ADMA1 is selected 10 = 32-bit Address ADMA2 is selected 11 = 64-bit Address ADMA2 is selected
2	<b>High Speed Enable (HI_SPD_EN)</b> —R/W. This bit is optional. Before setting this bit, the host driver shall check the High Speed Support in the capabilities register. If this bit is set to 0 (default), the HC outputs CMD line and DAT lines at the falling edge of the SD clock (up to 25 MHz/20 MHz for MMC). If this bit is set to 1, the HC outputs CMD line and DAT lines at the rising edge of the SD clock (up to 50 MHz). If Preset Value Enable in the Host Control 2 register is set to 1, the Host Driver needs to reset the SD Clock Enable before changing this field to avoid generating clock glitches. After setting this field, the Host Driver sets SD Clock Enable again 0 = Normal Speed Mode 1 = High Speed Mode
1	<b>Data Transfer Width (DATA_TX_WIDTH)</b> —R/W. This bit selects the data width of the HC. The HD shall select it to match the data width of the SD card. 0 = 1-bit mode 1 = 4-bit mode
0	Reserved

### 24.2.14 PWR\_CTRL—Power Control Register (SDIO—D23:F0)

Register Offset: BAR + 29h  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

Bit	Description
7:5	Reserved
4	<b>Hardware Reset (HW_RST)</b> —R/W. Hardware reset signal is generated for e-MMC* 4.41 card when this bit is set. 0 = De-assert the hardware reset pin 1 = Drives the hardware reset pin as ZERO (Active LOW to e-MMC* card)
3:0	Reserved

## 24.2.15 BLK\_GAP\_CTRL—Block Gap Control Register (SDIO—D23:F0)

Register Offset: BAR + 2Ah  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

Bit	Description
7:4	Reserved
3	<b>Interrupt at Block Gap (INT_BLK_GAP)</b> —R/W. This bit is valid only in 4-bit mode of the SDIO card and selects a sample point in the interrupt cycle. Setting to 1 enables interrupt detection at the block gap for a multiple block transfer. If the SD card cannot signal an interrupt during a multiple block transfer, this bit should be set to 0. When the host driver detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card
2	<b>Read Wait Control (RD_WAIT_CTL)</b> —R/W. The read wait function is optional for SDIO cards. If the card supports read wait, set this bit to enable use of the read wait protocol to stop read data using DAT[2] line. Otherwise, the HC has to stop the SD clock to hold read data, which restricts commands generation. When the HD detects an SD card insertion, it shall set this bit according to the CCCR of the SDIO card. If the card does not support read wait, this bit shall never be set to 1; otherwise, DAT line conflict may occur. If this bit is set to 0, Suspend/Resume cannot be supported 0 = Disable Read Wait Control 1 = Enable Read Wait Control
1	<b>Continue Request (CONT_REQ)</b> —R/W. This bit is used to restart a transaction that was stopped using the Stop At Block Gap Request. To cancel stop at the block gap, set Stop At block Gap Request to 0 and set this bit to restart the transfer. The HC automatically clears this bit in either of the following cases: 1. In the case of a read transaction, the DAT Line Active changes from 0 to 1 as a read transaction restarts. 2. In the case of a write transaction, the Write transfer active changes from 0 to 1 as the write transaction restarts. Therefore, it is not necessary for the Host driver to set this bit to 0. If Stop At Block Gap Request is set to 1, any write to this bit is ignored. 0 = Ignored 1 = Restart
0	<b>Stop At Block Gap Request (STP_BLK_GAP_REQ)</b> —R/W. This bit is used to stop executing a transaction at the next block gap for non- DMA, SDMA and ADMA transfers. Until the transfer complete is set to 1, indicating a transfer completion the HD shall leave this bit set to 1. Clearing both the Stop At Block Gap Request and Continue Request shall not cause the transaction to restart. Read Wait is used to stop the read transaction at the block gap. The HC shall honour Stop At Block Gap Request for write transfers; but for read transfers, it requires that the SD card support Read Wait. Therefore, the HD shall not set this bit during read transfers unless the SD card supports Read Wait and has set Read Wait Control to 1. In case of write transfers in which the HD writes data to the Buffer Data Port register, the HD shall set this bit after all block data is written. If this bit is set to 1, the host driver shall not write data to Buffer data port register. This bit affects Read Transfer Active, Write Transfer Active, DAT line active and Command Inhibit (DAT) in the Present State register. 0 = Transfer 1 = Stop

## 24.2.16 WAKEUP\_CTRL—Wakeup Control Register (SDIO—D23:F0)

Register Offset: BAR + 2Bh  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

Bit	Description
7:3	Reserved
2	<b>Wakeup Event Enable on Card Removal (WAKEUP_EN_RM)</b> —R/W. This bit enables wakeup event by means of Card Removal assertion in the Normal Interrupt Status register. FN_WUS (Wake up Support) in CIS does not affect this bit. 0 = Disable 1 = Enable
1	<b>Wakeup Event Enable on Card Insertion (WAKEUP_EN_INS)</b> —R/W. This bit enables wakeup event by means of Card Insertion assertion in the Normal Interrupt Status register. FN_WUS (Wake up Support) in CIS does not affect this bit. 0 = Disable 1 = Enable
0	<b>Wakeup Event Enable on Card Interrupt (WAKEUP_EN_INT)</b> —R/W. This bit enables wakeup event by means of Card Interrupt assertion in the Interrupt Normal Interrupt Status register. This bit can be set to 1 if FN_WUS (Wake Up Support) in CIS is set to 1. 0 = Disable 1 = Enable



## 24.2.17 CLK\_CTRL—Clock Control Register (SDIO—D23:F0)

Register Offset: BAR + 2Ch  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15:8	<p><b>Clock Frequency Select (SDCLK_FREQ_SEL)</b>—R/W. This register is used to select the frequency of the SDCLK pin. The frequency is not programmed directly; rather, this register holds the divisor of the Base Clock Frequency For SD clock in the capabilities register. Only the following settings are allowed.</p> <p><b>(1) 8-bit Divided Clock Mode</b></p> <p>80h - base clock divided by 256 40h - base clock divided by 128 20h - base clock divided by 64 10h - base clock divided by 32 08h - base clock divided by 16 04h - base clock divided by 8 02h - base clock divided by 4 01h - base clock divided by 2 00h - base clock (10 – 63 MHz)</p> <p>Setting 00h specifies the highest frequency of the SD Clock. When setting multiple bits, the most significant bit is used as the divisor. But multiple bits should not be set. The two default divider values can be calculated by the frequency that is defined by the Base Clock Frequency For SD Clock in the Capabilities register.</p> <ul style="list-style-type: none"><li>- 25 MHz divider value</li><li>- 400 KHz divider value</li></ul> <p>The frequency of the SDCLK is set by the following formula:</p> <p>Clock Frequency = (Base clock)/divisor.</p> <p>Thus, choose the smallest possible divisor that results in a clock frequency that is less than or equal to the target frequency.</p> <p>Maximum Frequency for SD = 50 MHz (base clock) Maximum Frequency for MMC = 52 MHz (base clock) Minimum Frequency = 195.3125 KHz (50 MHz/256), same calculation for MMC also</p> <p><b>(2) 10-bit Divided Clock Mode</b></p> <p>Host Controller Version 3.00 supports this mandatory mode instead of the 8-bit Divided Clock Mode. The length of divider is extended to 10 bits and all divider values shall be supported.</p> <p>3FFh -- 1/2046 Divided Clock N --1/2N Divided Clock (Duty 50%) 002h -- 1/4 Divided Clock 001h -- 1/2 Divided Clock 000h -- Base Clock (10 – 254 MHz)</p>
7:3	Reserved
2	<p><b>Clock Enable (SD_CLK_EN)</b>—R/W</p>
1	<p><b>Internal Clock Stable (INT_CLK_STABLE)</b>—RO. This bit is set to 1 when the SD clock is stable after writing to Internal Clock Enable in this register to 1. The SD Host Driver shall wait to set SD Clock Enable until this bit is set to 1.</p> <p><b>Note:</b> This is useful when using PLL for a clock oscillator that requires setup time.</p> <p>0 = Not Ready 1 = Ready</p>
0	<p><b>Internal Clock Enable (INT_CLK_EN)</b>—R/W. This bit is set to 0 when the host driver is not using the HC or the HC awaits a wakeup event.</p> <p>The HC should stop its internal clock to go to a very low power state. Still, registers shall be able to be read and written. Clock starts to oscillate when this bit is set to 1. When clock oscillation is stable, the HC shall set Internal Clock Stable in this register to 1. This bit shall not affect card detection.</p> <p>0 = Stop 1 = Oscillate</p>

## 24.2.18 TIMEOUT\_CTRL—Timeout Control Register (SDIO—D23:F0)

Register Offset: BAR + 2Eh      Attribute: R/W  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:4	Reserved
3:0	<p><b>Data Timeout Counter Value (DATA_TIMEOUT_CNT_VAL)</b>—R/W. This value determines the interval by which DAT line Timeouts are detected.</p> <p>Refer to the Data Timeout Error in the Error Interrupt Status register for information on factors that dictate Timeout generation. Timeout clock frequency will be generated by dividing the sdclock TMCLK by this value.</p> <p>When setting this register, prevent inadvertent Timeout events by clearing the Data Timeout Error Status Enable (in the Error Interrupt Status Enable register)</p> <p>1111 = Reserved    1110 = TMCLK * 2<sup>27</sup>    -----    0001 = TMCLK * 2<sup>14</sup>    0000 = TMCLK * 2<sup>13</sup></p>

## 24.2.19 SW\_RST—Software Reset Register

Register Offset: BAR + 2Fh      Attribute: R/WC  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:3	Reserved
2	<p><b>Software Reset for Data Line (SW_RST_DAT_LN)</b>—R/WC. Only part of data circuit is reset. The following registers and bits are cleared by this bit:</p> <ul style="list-style-type: none"> <li>• Buffer Data Port register: Buffer is cleared and Initialized.</li> <li>• Present State register: Buffer read Enable, Buffer write Enable, Read Transfer Active, Write Transfer Active, DAT Line Active, Command Inhibit (DAT)</li> <li>• Block Gap Control register: Continue Request, Stop At Block Gap Request</li> <li>• Normal Interrupt Status register: Buffer Read Ready, Buffer Write Ready, Block Gap Event Transfer Complete</li> </ul> <p>0 = Work    1 = Reset</p>
1	<p><b>Software Reset for CMD Line (SW_RST_CMD_LN)</b>—R/WC. Only part of command circuit is reset. The following registers and bits are cleared by this bit: Present State register, Command Inhibit (CMD), Normal Interrupt Status register, Command Complete</p> <p>0 = Work    1 = Reset</p>
0	<p><b>Software Reset for All (SW_RST_ALL)</b>—R/WC. This reset affects the entire HC except for the card detection circuit. Register bits of type ROC, RW, RWC are cleared to 0. During its initialization, the host driver shall set this bit to 1 to reset the HC.</p> <p>The HC shall reset this bit to 0 when capabilities registers are valid and the host driver can read them. Additional use of Software Reset for All may not affect the value of the Capabilities registers. If this bit is set to 1, the SD card shall reset itself and must be re initialized by the host driver.</p> <p>0 = Work    1 = Reset</p>



## 24.2.20 NML\_INT\_STAT—Normal Interrupt Status Register

Register Offset: BAR + 30h  
Default Value: 0000h

Attribute: R/WC, RO  
Size: 16 bits

Bit	Description
15	<b>Error Interrupt (ERR_INT)</b> —RO. If any of the bits in the Error Interrupt Status register are set, then this bit is set. Therefore, the host driver can test for an error by checking this bit first. 0 = No Error. 1 = Error.
14	<b>Boot Terminate Interrupt (BOOT_TER_INT)</b> —R/WC. This status is set if the boot operation gets terminated 0 = Boot operation is not terminated. 1 = Boot operation is terminated
13	<b>Boot Ack Received (BOOT_CK_RCV)</b> —R/WC. This status is set if the boot acknowledge is received from device. 0 = Boot ack is not received. 1 = Boot ack is received.
12	<b>Retuning Event (RE_TUNE)</b> —RO. This status is set if Re-Tuning Request in the Present State register changes from 0 to 1. Host Controller requests Host Driver to perform re-tuning for next data transfer. Current data transfer (not large block count) can be completed without re-tuning. 0 = Re-Tuning is not required 1 = Re-Tuning should be performed
11	<b>INTC (INT_C)</b> —RO. This status is set if INT_C is enabled and INT_C# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_C interrupt factor.
10	<b>INTB (INT_B)</b> —RO. This status is set if INT_B is enabled and INT_B# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_B interrupt factor.
9	<b>INTA (INT_A)</b> —RO. This status is set if INT_A is enabled and INT_A# pin is in low level. Writing this bit to 1 does not clear this bit. It is cleared by resetting the INT_A interrupt factor.
8:7	Reserved
6	<b>Card Insertion (CRD_INS)</b> —R/WC. This status is set if the Card Inserted in the Present State register changes from 0 to 1. When the host driver writes this bit to 1 to clear this status, the status of the Card Inserted in the Present State register should be confirmed. Because the card detect may possibly be changed when the HD clears this bit an Interrupt event may not be generated. 0 = Card State Stable or Debouncing 1 = Card Inserted
5	<b>Buffer Read Ready (BUF_RD_RDY)</b> —R/WC. This status is set if the Buffer Read Enable changes from 0 to 1. Buffer Read Ready is set to 1 for every CMD19 execution in tuning procedure. 0 = Not Ready to read Buffer. 1 = Ready to read Buffer.
4	<b>Buffer Write Ready (BUF_WR_RDY)</b> —R/WC. This status is set if the Buffer Write Enable changes from 0 to 1. 0 = Not Ready to Write Buffer. 1 = Ready to Write Buffer.
3	<b>DMA Interrupt (DMA_INT)</b> —R/WC. This status is set if the HC detects the Host DMA Buffer Boundary in the Block Size register. 0 = No DMA Interrupt 1 = DMA Interrupt is Generated



Bit	Description
2	<b>Block Gap Event (BLK_GAP_EVENT)</b> —R/WC. If the Stop At Block Gap Request in the Block Gap Control Register is set, this bit is set.
1	<b>Transfer Complete (TX_COMP)</b> —R/WC. This bit is set when a read/write transaction is completed.
0	<b>Command Complete (CMD_COMP)</b> —R/WC. This bit is set when the end bit of the command response (Except Auto CMD12 and Auto CMD23) is received.  <b>Note:</b> Command Timeout Error has higher priority than Command Complete. If both are set to 1, it can be considered that the response was not received correctly.  0 = No Command Complete 1 = Command Complete

## 24.2.21 ERR\_INT\_STAT—Error Interrupt Status Register

Register Offset: BAR + 32h  
Default Value: 0000h

Attribute: R/WC  
Size: 16 bits

Status defined in this register can be enabled by the Error Interrupt Status Enable register, but not by the Error Interrupt Signal Enable register. The Interrupt is generated when the Error Interrupt Signal Enable is enabled and at least one of the statuses is set to 1. Writing to 1 clears the bit and writing to 0 keeps the bit unchanged. More than one status can be cleared at the one register write.

Bit	Description
15:13	Reserved
12	<b>TGT_RSP_ERR</b> —R/WC. Occurs when detecting error in DMA transaction.
11:10	Reserved
9	<b>ADMA Error (ADMA_ERR)</b> —R/WC. This bit is set when the Host Controller detects errors during ADMA-based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. 0 = No error 1 = Error
8	<b>Auto CMD12 Error (CMD12_ERR)</b> —R/WC. Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that one of the bits D00 015–D04 in Auto CMD Error Status register has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error. 0 = No Error 1 = Error
7	<b>Current Limit Error (CUR_LIMIT_ERR)</b> —R/WC. By setting the SD Bus Power bit in the Power Control register, the HC is requested to supply power for the SD Bus. If the HC supports the Current Limit Function, it can be protected from an Illegal card by stopping the power supply to the card in which case this bit indicates a failure status. Reading 1 means the HC is not supplying power to SD card due to some failure. Reading 0 means that the HC is supplying power and no error has occurred. This bit shall always set to be 0, if the HC does not support this function. 0 = No Error 1 = Power Fail
6	<b>Data End Bit Error (DATA_END_BIT_ERR)</b> —R/WC. Occurs when detecting 0 at the end bit position of read data which uses the DAT line or the end bit position of the CRC status. 0 = No Error 1 = Error
5	<b>Data CRC Error (DATA_CRC_ERR)</b> —R/WC. Occurs when detecting CRC error when transferring read data which uses the DAT line or when detecting the Write CRC Status having a value of other than “010”. 0 = No Error 1 = Error

Bit	Description
4	<b>Data Timeout Error (DATA_TIMEOUT_ERR)</b> —R/WC. Occurs when detecting one of following timeout conditions. 1. Busy Timeout for R1b, R5b type. 2. Busy Timeout after Write CRC status 3. Write CRC status Timeout 4. Read Data Timeout 0 = No Error 1 = Timeout
3	<b>Command Index Error (CMD_INDEX_ERR)</b> —R/WC. Command Index Error. Occurs if a Command Index error occurs in the Command Response. 0 = No Error 1 = Error
2	<b>Command End Bit Error (CMD_END_BIT_ERR)</b> —R/WC. Occurs when detecting that the end bit of a command response is 0. 0 = No Error 1 = Error
1	<b>Command CRC Error (CMD_CRC_ERR)</b> —R/WC. Command CRC Error is generated in two cases. 1. If a response is returned and the Command Timeout Error is set to 0, this bit is set to 1 when detecting a CRT error in the command response. 2. The HC detects a CMD line conflict by monitoring the CMD line when a command is issued. If the HC drives the CMD line to 1 level, but detects 0 level on the CMD line at the next SDCLK edge, then the HC shall abort the command (Stop driving CMD line) and set this bit to 1. The Command Timeout Error shall also be set to 1 to distinguish CMD line conflict. 0 = No Error 1 = CRC Error Generated
0	<b>Command Timeout Error (CMD_TIMEOUT_ERR)</b> —R/WC. Occurs only if the no response is returned within 64 SDCLK cycles from the end bit of the command. If the HC detects a CMD line conflict, in which case Command CRC Error shall also be set. This bit shall be set without waiting for 64 SDCLK cycles because the command will be aborted by the HC. 0 = No Error 1 = Timeout

#### 24.2.22 NML\_INT\_STAT\_EN—Normal Interrupt Status Enable Register

Register Offset: BAR + 34h  
Default Value: 0000h

Attribute: R/W, RO  
Size: 16 bits

Bit	Description
15	Fixed to 0 (FIXED_0)—RO. The host controller shall control error interrupts using the Error Interrupt Status Enable Register
14	Boot Terminate Interrupt Enable (BOOT_TERM_INT_EN)—R/W 0 = Masked 1 = Enabled
13	Boot Acknowledge Received Enable (BOOT_ACK_RCV_EN)—R/W 0 = Masked 1 = Enabled
12	Re-Tuning Event Status Enable (RE_TUN_STATUS_EN)—R/W 0 = Masked 1 = Enabled
11	<b>INT_C Status Enable (INT_C_STATUS_EN)</b> —R/W. If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_C and may set this bit again after all interrupt requests to INT_C pin are cleared to prevent inadvertent interrupts.



Bit	Description
10	<b>INT_B Status Enable (INT_B_STATUS_EN)</b> —R/W. If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_B and may set this bit again after all interrupt requests to INT_B pin are cleared to prevent inadvertent interrupts.
9	<b>INT_A Status Enable (INT_A_STATUS_EN)</b> —R/W. If this bit is set to 0, the Host Controller shall clear the interrupt request to the System. The Host Driver may clear this bit before servicing the INT_A and may set this bit again after all interrupt requests to INT_A pin are cleared to prevent inadvertent interrupts.
8	<b>Card Interrupt Status Enable (CRD_INT_STAT_EN)</b> —R/W. If this bit is set to 0, the HC shall clear Interrupt request to the System. The Card Interrupt detection is stopped when this bit is cleared and restarted when this bit is set to 1. The HD may clear the Card Interrupt Status Enable before servicing the Card Interrupt and may set this bit again after all Interrupt requests from the card are cleared to prevent inadvertent Interrupts. 0 = Masked 1 = Enabled
7	<b>Card Removal Status Enable (CRD_RM_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled
6	<b>Card Insertion Status Enable (CRD_INS_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled
5	<b>Buffer Read Ready Status Enable (BUF_RD_RDY_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled
4	<b>Buffer Write Ready Status Enable (BUF_WR_RDY_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled
3	<b>DMA Interrupt Status Enable (DMA_INT_STA_EN)</b> —R/W. 0 = Masked 1 = Enabled
2	<b>Block Gap Event Status Enable (BLK_GAP_EVENT_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled
1	<b>Transfer Complete Status Enable (TX_COMP_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled
0	<b>Command Complete Status Enable (CMD_COMP_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled

### 24.2.23 ERR\_INT\_STAT\_EN—Error Interrupt Status Enable Register

Register Offset: BAR + 36h  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:13	Reserved.
12	<b>TGT_RSP_ERR_EN</b> —R/W. 0 = Masked 1 = Enabled
11	Reserved.
10	<b>TUNE Error Status Enable (TUNE_ERR_STAT_EN)</b> —R/W 0 = Masked 1 = Enabled
9	<b>ADMA Error Status Enable (ADMA_ERR)</b> —R/W 0 = Masked 1 = Enabled
8	<b>Auto CMD12 Error Status Enable (CMD12_ERR)</b> —R/W. 0 = Masked 1 = Enabled
7	<b>Current Limit Error Status Enable (CUR_LIMIT_ERR)</b> —R/W. 0 = Masked 1 = Enabled
6	<b>Data End Bit Error Status Enable (DATA_END_BIT_ERR)</b> —R/W. 0 = Masked 1 = Enabled
5	<b>Data CRC Error Status Enable (DATA_CRC_ERR)</b> —R/W. 0 = Masked 1 = Enabled
4	<b>Data Timeout Error Status Enable (DATA_TIMEOUT_ERR)</b> —R/W. 0 = Masked 1 = Enabled
3	<b>Command Index Error Status Enable (CMD_INDEX_ERR)</b> —R/W. 0 = Masked 1 = Enabled
2	<b>Command End Bit Error Status Enable (CMD_END_BIT_ERR_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled
1	<b>Command CRC Error Status Enable (CMD_CRC_ERR_STAT_EN)</b> —R/W. 0 = Masked 1 = Enabled
0	<b>Command Timeout Error Status Enable</b> —R/W. 0 = Masked 1 = Enabled

## 24.2.24 NML\_INT\_SIG\_EN—Normal Interrupt Signal Enable Register

Register Offset: BAR + 38h      Attribute: R/W, RO  
 Default Value: 0000h      Size: 16 bits

This register is used to select which interrupt status is indicated to the Host System as the Interrupt. These status bits all share the sample 1-bit interrupt line. Setting any of these bits to 1 enables Interrupt generation.

Bit	Description
15	Fixed to 0 (FIXED_0)—RO. The host controller shall control error interrupts using the Error Interrupt Status Enable register
14	<b>Boot Terminate Interrupt Signal Enable (BOOT_TERM_INT_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
13	<b>Boot Acknowledge Received Signal Enable (BOOT_ACK_RCV_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
12	<b>Re-tuning Signal Enable (RE_TUN_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
11	<b>INT_C Signal Enable (INT_C_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
10	<b>INT_B Signal Enable (INT_B_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
9	<b>INT_A Signal Enable (INT_A_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
8	<b>Card Interrupt Signal Enable (CRD_INT_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
7	<b>Card Removal Signal Enable (CRD_RM_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
6	<b>Card Insertion Signal Enable (CRD_INS_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
5	<b>Buffer Read Ready Signal Enable (BUF_RD_RDY_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
4	<b>Buffer Write Ready Signal Enable (BUF_WR_RDY_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
3	<b>DMA Interrupt Signal Enable (DMA_INT_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
2	<b>Block Gap Event Signal Enable (BLK_GAP_EVENT_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
1	<b>Transfer Complete Signal Enable (TX_COMP_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
0	<b>Command Complete Signal Enable (CMD_COMP_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled

## 24.2.25 ERR\_INT\_SIG\_EN—Error Interrupt Signal Enable Register

Register Offset: BAR + 3Ah  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:13	Reserved
12	<b>TGT_RSP_ERR_SIG_EN</b> —R/W. 0 = Masked 1 = Enabled
11	Reserved
10	<b>TUNE_ERR_SIG_EN</b> —R/W. 0 = Masked 1 = Enabled
9	<b>ADMA Error Signal Enable (ADMA_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
8	<b>Auto CMD12 Error Signal Enable (CMD12_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
7	<b>Current Limit Error Signal Enable (CUR_LIMIT_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
6	<b>Data End Bit Error Signal Enable (DATA_END_BIT_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
5	<b>Data CRC Error Signal Enable (DATA_CRC_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
4	<b>Data Timeout Error Signal Enable (DATA_TIMEOUT_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
3	<b>Command Index Error Signal Enable (CMD_INDEX_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
2	<b>Command End Bit Error Signal Enable (CMD_END_BIT_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
1	<b>Command CRC Error Signal Enable (CMD_CRC_ERR_SIG_EN)</b> —R/W. 0 = Masked 1 = Enabled
0	<b>Command Timeout Error Signal Enable</b> —R/W. 0 = Masked 1 = Enabled

## 24.2.26 CMD12\_ERR\_STAT—Auto CMD12 Error Status

Register Offset: BAR + 3Ch  
Default Value: 0000h

Attribute: RO  
Size: 16 bits

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD23. The Host driver can determine what kind of Auto CMD12/CMD23 errors occur by this register. Auto CMD23 errors are indicated in bit 04-01. This register is valid only when the Auto CMD Error is set.

Bit	Description
15:8	Reserved
7	<b>Command Not Issued By Auto CMD12 Error (CMD_NOT_ISS_CMD12_ERR)</b> —RO. Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 error (D04 – D01) in this register. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23 0 = No Error 1 = Not Issued
6:5	Reserved
4	<b>Auto CMD Index Error (CMD_IND_ERR)</b> —RO. Occurs if the Command Index error occurs in response to a command. 0 = No error 1 = Error
3	<b>Auto CMD End Bit Error (CMD_END_BIT_ERR)</b> —RO. Occurs when detecting that the end bit of command response is 0. 0 = No error 1 = End bit error generated
2	<b>Auto CMD CRC Error (CMD_CRC_ERR)</b> —RO. Occurs when detecting a CRC error in the command response. 0 = No error 1 = CRC error generated
1	<b>Auto CMD Timeout Error (CMD_TIMEOUT_ERR)</b> —RO. Occurs when detecting a CRC error in the command response. 0 = No error 1 = CRC error generated
0	<b>Auto CMD Not Executed (CMD_NOT_EXE)</b> —RO. If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the HC cannot issue Auto CMD12 to stop memory multiple block transfer due to some error. If this bit is set to 1, other error status bits (D04 – D01) are meaningless. This bit is set to 0 when Auto CMD Error is generated by Auto CMD23. 0 = Executed 1 = Not Executed



## 24.2.27 HOST\_CTL\_2—Host Controller 2 Register

Register Offset: BAR + 3Eh  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15	<b>Preset Value (PRESET_VALUE)</b> —R/W. Host Controller Version 3.00 supports this bit. As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set to automatic, this bit enables the functions defined in the PresetValue registers. 1 = Automatic Selection by Preset Value are Enabled 0 = SDCLK and Driver Strength are controlled by Host Driver. If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver. If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.
14	<b>Asynchronous Interrupt (ASYNC_INT)</b> —R/W. This bit can be set to 1 if a card supports asynchronous interrupt and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode (and zero is set to Interrupt Pin Select in the Shared Bus Control register). If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver Card Interrupt to the host when it is asserted by the Card. 0 = Disabled 1 = Enabled
13:8	Reserved.
7	<b>Sampling Clock (SAMPLING_CLOCK)</b> —R/W. This bit is set by tuning procedure when Execute Tuning is cleared. Writing 1 to this bit is meaningless and ignored. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is cleared by writing 0. Change of this bit is not allowed while the Host Controller is receiving response or a read data block. 0 = Fixed clock is used to sample data 1 = Tuned clock is used to sample data
6	<b>Execute Tuning (EXECUTE_TUNING)</b> —R/W. This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by writing 0 for more detail about tuning procedure. 0 = Not Tuned or Tuning Completed 1 = Execute Tuning
5:4	<b>Driver Strength (TIMEOUT_CLK_UNIT)</b> —R/W. Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C, and D support bits in the Capabilities register. This bit depends on setting of Preset Value Enable. If Preset Value Enable = 0, this field is set by Host Driver. If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers. 00b = Driver Type B is Selected (Default) 01b Driver Type A is Selected 10b = Driver Type C is Selected 11b Driver Type D is Selected.
3	<b>1.8V Signalling Enable (DRIVER_STRENGTH)</b> —R/W. This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage. Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5 ms. Host Controller clears this bit if switching to 1.8V signaling fails. Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5 ms. Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling (One of support bits is set to 1: SDR50, SDR104 or DDR50 in the Capabilities register) and the card or device supports UHS- I 0 = 3.3V Signaling 1 = 1.8V Signaling

Bit	Description
2:0	<p><b>UHS Mode (UHS_MODE)</b>—R/W. This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1.</p> <p>If Preset Value Enable in the Host Control 2 register is set to 1, Host Controller sets SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again.</p> <p>000b = SDR12 001b - SDR25 010b = SDR50 011b - SDR104 100b = DDR50 101b - 111 Reserved</p> <p>When SDR50, SDR104, or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes.</p> <p>Refer to the SDIO Specification Version 3.00 for more detail</p>

## 24.2.28 CAP—Capabilities Register

Register Offset: BAR + 40h  
Default Value: Hardware INIT

Attribute: RO  
Size: 32 bits

Bit	Description
31:30	<p><b>Slot Type</b>—RO. This field indicates usage of a slot by a specific Host System. (A host controller register set is defined per slot.) Embedded slot for one device (01b) means that only one non-removable device is connected to a SD bus slot. Shared Bus Slot (10b) can be set if Host Controller supports the Shared Bus Control register.</p> <p>The Standard Host Driver controls only a removable card or one embedded device is connected to a SD bus slot. If a slot is configured for shared bus (10b), the Standard Host Driver does not control embedded devices connected to a shared bus. Shared bus slot is controlled by a specific host driver developed by a Host System.</p> <p>00b = Removable Card Slot 01b = Embedded Slot for One Device 10b = Shared Bus Slot 11b = Reserved</p>
29	<b>Asynchronous Interrupt Support (ASYNC_INT)</b> —RO
28	<b>64-bit System Bus Support (SYS_BUS64)</b> —RO 0 = Does not support 64-bit system address 1 = supports 64-bit system address
27	Reserved.
26	<b>Voltage Support 1.8v (VOLT_18)</b> —RO 0 = 1.8V not supported 1 = 1.8V supported
25	<b>Voltage Support 3.0v (VOLT_30)</b> —RO 0 = 3.0V not supported 1 = 3.0V supported
24	<b>Voltage Support 3.3v (VOLT_33)</b> —RO 0 = 3.3V not supported 1 = 3.3V supported
23	<b>Suspend Resume Support (SUSP_RES)</b> —RO. This bit indicates whether the HC supports Suspend/Resume functionality. If this bit is 0, the Suspend and Resume mechanisms are not supported and the HD shall not issue either Suspend/Resume commands.
22	<b>SDMA Support (SDMA)</b> —RO. This bit indicates whether the HC is capable of using DMA to transfer data between system memory and the HC directly.
	0 = SDMA Not Supported 1 = SDMA Supported.



Bit	Description
21	<b>High Speed Support (HIGH_SPEED)</b> —RO. This bit indicates whether the HC and the Host System support High Speed mode and they can supply SD Clock frequency from 25 – 50 MHz (for SD)/20 – 52 MHz (for MMC). 0 = High Speed Not Supported 1 = High Speed Supported
20	Reserved
19	<b>ADMA2 Support (ADMA2)</b> —RO 0 = ADMA2 not supported 1 = ADMA2 supported
18	<b>Extended Media Bus Support (EXT_MEDIA_BUS)</b> —RO. This bit indicates whether the Host Controller is capable of using 8-bit bus width mode. This bit is not effective when Slot Type is set to 10b. In this case, refer to Bus Width Preset in the Shared Bus register. 0 = Extended Media Bus not Supported 1 = Extended Media Bus Supported
17:16	<b>Maximum Block Length (MAX_BLK_LEN)</b> —RO. This value indicates the maximum block size that the host driver can read and write to the buffer in the HC. The buffer shall transfer this block size without wait cycles. Three sizes can be defined as indicated below. 00 = 512 byte 01 = 1024 byte 10 = 2048 byte 11 = 4096 byte
15:8	<b>Base Clock Frequency for SD Clock (BASE_CLK_FREQ)</b> —RO <b>(1) 6-bit Base Clock Frequency</b> This mode is supported by the Host Controller Version 1.00 and 2.00. Upper 2-bit is not effective and always 0. Unit values are 1 MHz. The supported clock range is 10 – 63 MHz. 11xx xxxx b = Not supported 0011 1111 b = 63 MHz 0000 0010 b = 2 MHz 0000 0001 b = 1 MHz 0000 0000 b = Get information by means of another method <b>(2) 8-bit Base Clock Frequency</b> This mode is supported by the Host Controller Version 3.00. Unit values are 1 MHz. The supported clock range is 10 – 255 MHz. FFh = 255 MHz 02h = 2 MHz 01h = 1 MHz 00h = Get information by means of another method If the real frequency is 16.5 MHz, the larger value shall be set 0001 0001b (17 MHz) because the Host Driver uses this value to calculate the clock divider value (Refer to the SDCLK Frequency Select in the Clock Control register.) and it shall not exceed upper limit of the SD Clock frequency. If these bits are all 0, the Host system has to get information by means of another method.
7	<b>Timeout Clock Unit (TIMEOUT_CLK_UNIT)</b> —RO. This bit shows the unit of base clock frequency used to detect Data Timeout Error. 0 = KHz 1 = MHz
6	Reserved.
5:0	<b>Timeout Clock Frequency (TIMEOUT_CLK_FREQ)</b> —RO. This bit shows the base clock frequency used to detect Data Timeout Error A non-zero value indicates 1 kHz to 63 kHz or 1 MHz to 63 MHz. 0 = Get information by means of another method

## 24.2.29 CAP2—Capabilities 2 Register

Register Offset: BAR + 44h  
Default Value: Hardware INIT

Attribute: RO  
Size: 32 bits

Bit	Description
31:26	Reserved
25	<b>SPI Block Mode</b> —RO 0 = Not supported 1 = Supported
24	<b>SPI Mode</b> —RO 0 = Not supported 1 = Supported
23:16	<b>Clock Multiplier</b> —RO. This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator. FFh = Clock Multiplier M = 256 .... 02h = Clock Multiplier M = 3 01h = Clock Multiplier M = 2 00h = Clock Multiplier is Not Supported
15:14	<b>Retuning Modes</b> —RO. This field defines the re-tuning capability of a Host Controller and how to manage the data transfer length and a Re-Tuning Timer by the Host Driver. 00 = Mode1 01 = Mode2 10 = Mode3 11 = Reserved There are two re-tuning timings: Re-Tuning Request and expiration of a Re-Tuning Timer. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue
13	<b>Tuning for SDR50</b> —RO. If this bit is set to 1, this Host Controller requires tuning to operate SDR50. (Tuning is always required to operate SDR104.) 0 = SDR50 does not require tuning 1 = SDR50 requires tuning
12	Reserved
11:8	<b>Timer Count for Retuning</b> —RO. This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. 0h - Get information by means of other source 1h = 1 seconds 2h = 2 seconds 3h = 4 seconds 4h = 8 seconds ..... n = 2(n-1) seconds ..... Bh = 1024 seconds Fh - Ch = Reserved
7	Reserved
6	<b>Driver Type D Support</b> —RO. This bit indicates support of Driver Type D for 1.8 signaling. 0 = Driver Type D is not supported 1 = Driver Type D is supported
5	<b>Driver Type C Support</b> —RO. This bit indicates support of Driver Type C for 1.8 signaling. 0 = Driver Type C is not supported 1 = Driver Type C is supported

Bit	Description
4	<b>Driver Type A Support</b> —RO. This bit indicates support of Driver Type A for 1.8 signaling. 0 = Driver Type A is not supported 1 = Driver Type A is supported
3	Reserved
2	<b>DDR50 Support</b> —RO 0 = DDR50 is not supported 1 = DDR50 is supported
1	<b>SDR104 Support</b> —RO. SDR104 requires tuning. 0 = SDR104 is not supported 1 = SDR104 is supported
0	<b>SDR50 Support</b> —RO. If SDR 104 is supported, this bit shall be set to 1. Bit 40 indicates whether SDR50 requires tuning or not. 0 = SDR50 is not supported 1 = SDR50 is supported

### 24.2.30 MAX\_CUR\_CAP—Maximum Current Capabilities Register

Register Offset: BAR + 48h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:24	Reserved
23:16	<b>Maximum Current for 1.8V (MAX_CUR_1p8V)</b> —RO. Maximum Current for 1.8V Register Value, Current Value 0 = Get Information by means of another method 1 = 4mA 2 = 8mA 3 = 12mA ----- 255 = 1020mA
15:8	<b>Maximum Current for 3.0V (MAX_CUR_3p0V)</b> —RO
7:0	<b>Maximum Current for 3.3V (MAX_CUR_3p3V)</b> —RO

### 24.2.31 FORCE\_EVENT\_CMD12\_ERR\_STAT—Force Event Register for Auto CMD12 Error Status

Register Offset: BAR + 50h  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:8	Reserved.
7	<b>Force Event for Command Not Issued By Auto CMD12 Error (NON_CMD12_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
6:5	Reserved
4	<b>Force Event for Auto CMD12 Index Error (CMD12_IND_ERR)</b> —R/W
3	<b>Force Event for Auto CMD12 End Bit Error (CMD12_END_BIT_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
2	<b>Force Event for Auto CMD12 CRC Error (CMD12_CRC_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
1	<b>Force Event for Auto CMD12 Timeout Error (CMD12_TIMEOUT_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
0	<b>Force Event for Auto CMD12 Not Executed (CMD12_NOT_EXE)</b> —R/W 0 = No interrupt 1 = Interrupt is generated

### 24.2.32 FORCE\_EVENT\_ERR\_INT\_STAT—Force Event Register for Error Interrupt Status

Register Offset: BAR + 52h  
Default Value: 0000h

Attribute: R/W  
Size: 16 bits

Bit	Description
15:13	Reserved
12	<b>Force Event for Target Response Error (TGT_RSP_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
11:10	Reserved.
9	<b>Force Event for ADMA Error (ADMA_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
8	<b>Force Event for Auto CMD12 Error (CMD12_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
7	<b>Force Event for Current Limit Error (CUR_LIMIT_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
6	<b>Force Event for Data End Bit Error (DATA_END_BIT_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
5	<b>Event for Data CRC Error (DATA_CRC_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
4	<b>Event for Data Timeout Error (DATA_TIMEOUT_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
3	<b>Force Event for Command Index Error (CMD_IND_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
2	<b>Force Event for Command End Bit Error (CMD_END_BIT_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
1	<b>Force Event for Command CRC Error (CMD_CRC_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated
0	<b>Force Event for Command Timeout Error (CMD_TIMEOUT_ERR)</b> —R/W 0 = No interrupt 1 = Interrupt is generated

### 24.2.33 ADMA\_ERR\_STAT—ADMA Error Status Register

Register Offset: BAR + 54h  
Default Value: 00h

Attribute: RO  
Size: 8 bits

Bit	Description
7:3	Reserved
2	<b>ADMA Length Mismatch Error (ADMA_LEN_MIS_ERR)</b> —RO. (1) While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. (2) Total data length can not be divided by the block length. 0 = No error 1 = Error
1:0	<b>ADMA Error State (ADMA_ERR_STATE)</b> —RO. This field indicates the state of ADMA when error is occurred during ADMA data transfer. This field never indicates "10" because ADMA never stops in this state. D01 – D00: ADMA Error State when error is occurred Contents of SYS_SDR register 00 = ST_STOP (Stop DMA) Points next of the error descriptor 01 = ST_FDS (Fetch Descriptor) Points the error descriptor 10 = Never set this state (Not used) 11 = ST_TFR (Transfer Data) Points the next of the error descriptor

### 24.2.34 ADMA\_SYS\_ADDR—System Address Register

Register Offset: BAR + 58h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:0	<b>ADMA System Address (ADMA_SYS_ADDR)</b> —R/W. This register holds the byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32 bits of this register. At the start of ADMA, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The Host Driver shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b. 32-bit Address ADMA Register Value 32-bit System Address xxxxxxxx 00000000h 00000000h xxxxxxxx 00000004h 00000004h ..... xxxxxxxx FFFFFFFFCh FFFFFFFFCh

### 24.2.35 PRESET\_VAL0—Preset Values Registers

Register Offset: BAR + 60h  
Default Value: 0002h

Attribute: RO  
Size: 16 bits

Bit	Description
15:14	<b>Driver Strength Select Value</b> —RO. Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling. 11b = Driver Type D is Selected 10b = Driver Type C is Selected 01b = Driver Type A is Selected 00b = Driver Type B is Selected
13:11	Reserved
10	<b>Clock Generator Select Value</b> —RO. This bit is effective when Host Controller supports programmable clock generator. 0 = Host Controller Version 2.00 Compatible Clock Generator 1 = Programmable Clock Generator
9:0	<b>SDCLK Frequency Select Value</b> —RO. 10-bit preset value to set SDCLK Frequency Select in the Clock Control register is described by a host system.

### 24.2.36 BOOT\_TO\_CTRL—Boot Timeout Control Register

Register Offset: BAR + 70h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:0	<b>Boot Data Timeout Counter Value (TIME_CNT_VAL)</b> —R/W. This value determines the interval by which DAT line Timeouts are detected during boot operation for e-MMC* 4.4 card. The value is in number of sd clock.

### 24.2.37 SHARED BUS—Shared Bus Control Register

Register Offset: BAR + 0E0h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:24	Reserved
23	Reserved
22:20	<b>Interrupt Pin Select</b> —R/W. Interrupt pin inputs are enabled by this field. Enable of unsupported interrupt pin is meaningless. 000b Interrupt is detected by Interrupt Cycle xx1b = INT_A is Enabled x1xb = INT_B is Enabled 1xxb = INT_C is Enabled
19	Reserved
18:16	<b>Clock Pin Select</b> —R/W. One of clock pin outputs is selected by this field. Select of unsupported clock pin is meaningless. Refer to Figure 2-38 for the timing of clock outputs. 000b = Clock Pins are Disabled 001b = CLK[1] is Selected 010b = CLK[2] is Selected ..... 111b = CLK[7] is Selected
15	Reserved



Bit	Description
14:8	<p><b>Bus Width Preset</b>—RO. Shared bus supports mixing of 4-bit and 8-bit bus width devices. Each bit of this field specifies the bus width for each embedded device. The number of devices supported is specified by Number of Clock Pins and a maximum of 7 devices are supported. This field is effective when multiple devices are connected to a shared bus (Slot Type is set to 10b in the Capabilities register).</p> <p>In the other case, Extended Data Transfer Width in the Host Control 1 register is used to select 8-bit bus width. As use of 1-bit mode is not intended for shared bus, Data Transfer Width in the Host Control 1 register should be set to 1.</p> <p>D08 - Bus width preset for Device 1  D09 - Bus width preset for Device 2  D10 - Bus width preset for Device 3  D11 - Bus width preset for Device 4  D12 - Bus width preset for Device 5  D13 - Bus width preset for Device 6  D14 - Bus width preset for Device 7</p> <p>The function of each bit is defined as follows:  0 = 4-bit bus width mode  1 = 8-bit bus width mode</p>
7:6	Reserved
5:4	<p><b>Number of Interrupt Input Pins</b>—RO. This field indicates support of interrupt input pins for shared bus system. Three asynchronous interrupt pins are defined: INT_A#, INT_B#, and INT_C#. Which interrupt pin is used is determined by the system. Each one is driven by open drain and then wired OR connection is possible.</p> <p>00b = Interrupt Input Pin is Not Supported  01b = INTA is Supported  10b = INTA and INTB are Supported  11b = INTA, INTB, and INTC are Supported</p>
3	Reserved
2:0	<p><b>Number of Clock Pins</b>—RO. This field indicates support of clock pins to select one of devices for shared bus system. Up to 7 clock pins can be supported. Shared bus is supported by specific system. Then Standard Host Driver does not support control of these clock pins.</p> <p>000b = Shared bus is not supported  001b = 1 SDCLK pin is supported  010b = 2 SDCLK pins are supported  .....  111b = 7 SDCLK pins are supported</p>

### 24.2.38 SPI\_INT\_SUP—SPI Interrupt Support Register

Register Offset: BAR + 0F0h  
Default Value: 00h

Attribute: R/W  
Size: 8 bits

Bit	Description
7:0	<b>SPI Interrupt Support</b> —R/W. This bit is set to indicate the assertion of interrupts in the SPI mode at any time, irrespective of the status of the card select (CS) line. If this bit is zero, then SDIO card can only assert the interrupt line in the SPI mode when the CS line is asserted.

### 24.2.39 SLOT\_INT\_STAT—Slot Interrupt Status Register

Register Offset: BAR + 0FCh  
Default Value: 0000h

Attribute: RO  
Size: 16 bits

Bit	Description
15:8	Reserved
7:0	<b>Interrupt Signal For Each Slot (INT_SIG_SLOT)</b> —RO. These status bit indicate the logical OR of Interrupt signal and wakeup signal for each slot. A maximum of 8 slots can be defined. If one interrupt signal is associated with multiple slots. The host driver can know which interrupt is generated by reading these status bits. By a power on reset or by Software Reset For All, the Interrupt signal shall be de asserted and this status shall read 00h

### 24.2.40 GEN—GENERAL

Register Offset: BAR + 1008h  
Default Value: 00000000h

Attribute: R/W  
Size: 32 bits

Bit	Description
31:3	Reserved
2	<b>LTR Mode</b> —R/W 0 = Auto Mode 1 = Software Mode
1:0	Reserved

#### 24.2.41 SW\_LTR\_VAL—Software LTR Value Register

Register Offset: BAR + 1010h      Attribute: R/W, RO  
 Default Value: 00000800h      Size: 32 bits

Bit	Description
31	<b>Non Snoop Requirement</b> —RO. If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (that is, it can wait for service indefinitely). If the 10-bit latency value is zero, it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	Reserved.
28:26	<b>Non Snoop Latency Scale</b> —RO. Support for codes 010 (1 µs) or 011 (32 µs) for Snoop Latency Scale (1 µs – 32 ms total span) only. Writes to this field which don't match those values will be dropped completely. Next read will return previous value.
25:16	<b>Non Snoop Value</b> —RO 10-bit latency value.
15	<b>Snoop Requirement</b> —R/W. If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	Reserved
12:10	<b>Snoop Latency Scale</b> —R/W. Support for codes 010 (1 µs) or 011 (32 µs) for Snoop Latency Scale (1 µs – 32 ms total span) only. Writes to this field which do not match those values will be dropped completely. Next read will return previous value.
9:0	<b>Snoop Value</b> —R/W 10-bit latency value.

#### 24.2.42 AUTO\_LTR\_VAL—Auto LTR Value Register

Register Offset: BAR + 1014h      Attribute: R/W, RO  
 Default Value: 00000800h      Size: 32 bits

Bit	Description
31	<b>Non Snoop Requirement</b> —RO. If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
30:29	Reserved
28:26	<b>Non Snoop Latency Scale</b> —RO. Support for codes 010 (1 µs) or 011 (32 µs) for Snoop Latency Scale (1 µs – 32 ms total span) only. Writes to this field which do not match those values will be dropped completely. Next read will return previous value.
25:16	<b>Non Snoop Value</b> —RO 10-bit latency value.
15	<b>Snoop Requirement</b> —R/W. If the Requirement (bit 15) is clear, that indicates that the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely). If the 10-bit latency value is zero it indicates that the device cannot tolerate any delay and needs the best possible service/response time.
14:13	Reserved
12:10	<b>Snoop Latency Scale</b> —R/W. Support for codes 010 (1 µs) or 011 (32 µs) for Snoop Latency Scale (1 µs – 32 ms total span) only. Writes to this field which do not match those values will be dropped completely. Next read will return previous value.
9:0	<b>Snoop Value</b> —R/W 10-bit latency value.

#### 24.2.43 RX\_DELAY\_SDR\_MODE—Receive Delay for Default Mode and SDR25 Register

Register Offset: BAR +102Ch  
Default Value: 00000204h

Attribute: WO, RO  
Size: 32 bits

Bit	Description
31:13	Reserved
12:8	<p><b>RX SDR Mode Multiplex Select (SDL_RX_SDR_MUXSEL)</b>—R/W. This field selects number of delay elements to use to generate the delay for the RX path in Default Speed Mode and SDR25 Mode.</p> <p>00h = 1 inch to 3.5 inches board trace length  01h = 3.5 inches to 5.25 inches board trace length  02h = 5.25 inches to 7 inches board trace length  03h = 7 inches to 8.75 inches board trace length  04h = 8.75 inches to 10.5 inches board trace length  05h = 10.5 inches to 12.5 inches board trace length</p> <p><b>Note:</b> The trace lengths are based on a range of 160–185 ps/inch propagation delays. Boards with propagation delays outside this range should adjust their settings accordingly.</p>
9:0	Reserved

#### 24.2.44 RX\_DELAY\_DDR50\_MODE—Receive Delay for DDR50 Register

Register Offset: BAR +1034h  
Default Value: 0000030Eh

Attribute: WO, RO  
Size: 32 bits

Bit	Description
31:13	Reserved
12:8	<p><b>RX DDR50 Mode Multiplex Select (SDL_RX_DDR50_MUXSEL)</b>—R/W. This field selects number of delay elements to use to generate the delay for the RX path in DDR50 Mode.</p> <p>02h = 1 inch to 2.5 inches board trace length  03h = 2.5 inches to 4 inches board trace length  04h = 4 inches to 6 inches board trace length  05h = 6 inches to 7.5 inches board trace length  06h = 7.5 inches to 9.5 inches board trace length</p> <p><b>Note:</b> The trace lengths are based on a range of 160 ps/inch to 185 ps/inch propagation delays. Boards with propagation delays outside this range should adjust their settings accordingly.</p>

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# 25 Intel® Serial I/O UART Controller Registers (D21:F5/F6)

## 25.1 PCI Configuration Registers (UART—D21:F5/F6)

Table 25-1. UART Controller PCI Register Address Map (UART—D21:F5/F6)

Offset	Mnemonic	Register Name	Default	Attribute
00h-01h	VID	Vendor Identification	0000	RO
02h-03h	DID	Device Identification	See register description	RO
04h-05h	PCICMD	PCI Command	0000h	R/W, RO
06h-07h	PCISTS	PCI Status	0010h	RO, R/WC
08h-0Bh	RID	Revision Identification	See register description	RO
0Ch-0Fh	CLLH	Cache Line Latency Header	00800000h	R/W, RO
10h-13h	BAR0	Memory Base Address 0	00000000h	RO, R/W
14h-17h	BAR1	Memory Base Address 1	00000000h	RO, R/W
2Ch-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
34h-35h	CAPPTR	Capabilities Pointer	00h	RO
2Eh-2Fh	SID	Subsystem Identification	0000h	R/WO
3Ch	INT_LN	Interrupt Line	00h	R/W
3Dh	INT_PN	Interrupt Pin	01h	RO
80h-83h	PWR_CAP	Power Capability	00030001h	RO
84h-87h	PME_CTRL_STA	PME Control and Status	00000008h	RO, R/W, R/WC

**Note:** Registers that are not shown should be treated as Reserved.

### 25.1.1 VID—Vendor Identification Register (UART—D21:F5/F6)

Address: 00h-01h Attribute: RO  
 Default Value: 8086h Size: 16 bits

Bit	Description
15:0	<b>Vendor ID</b> —RO.

### 25.1.2 DID—Device Identification Register (UART—D21:F5/F6)

Address: 02h–03h      Attribute: RO  
 Default Value: 9CE3h      Size: 16 bits

Bit	Description
15:0	<b>Device ID</b> —RO. This is a 16-bit value assigned to the controller. See <a href="#">Section 1.4</a> for the value of the DID Register.

### 25.1.3 PCICMD—PCI Command Register (UART—D21:F5/F6)

Address: 04h–05h      Attributes: RO, R/W  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:11	Reserved
10	<b>Interrupt Disable</b> —R/W 0 = Enable 1 = Disable
9	Reserved
8	<b>SERR# Enable (SERR_EN)</b> —R/W 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7:3	Reserved
2	<b>Bus Master Enable (BME)</b> —R/W
1	<b>Memory Space Enable (MSE)</b> —R/W 0 = Disables memory mapped Configuration space. 1 = Enables memory mapped Configuration space.
0	Reserved

#### 25.1.4 PCISTS—PCI Status Register (UART—D21:F5/F6)

Address: 06h-07h      Attributes: RO, R/WC  
 Default Value: 0010h      Size: 16 bits

**Note:** For the writable bits, software must write a 1 to clear bits that are set. Writing a 0 to the bit has no effect.

Bit	Description
15	Reserved.
14	<b>Signaled System Error (SSE)</b> —R/WC 0 = No system error detected. 1 = System error detected.
13	<b>Received Master Abort (RMA)</b> —R/WC
12	<b>Received Target Abort (RTA)</b> —R/WC
11	<b>Signaled Target Abort (STA)</b> —R/WC
10:5	Reserved
4	<b>Capabilities List (CAP_LIST)</b> —RO. Hardwired to 1 to indicate there are capability list structures in this function
3	<b>Interrupt Status (INTS)</b> —RO. This bit indicates that an interrupt is pending. It is independent from the state of the Interrupt Enable bit in the PCI Command register.
2:0	Reserved

#### 25.1.5 RID—Revision Identification and Class Code Register (UART—D21:F5/F6)

Offset Address: 08h-0Bh      Attribute: RO  
 Default Value: See bit description      Size: 32 bits

Bit	Description
31:8	<b>Class Code</b> —RO. Hardwired to 070002h
7:0	<b>Revision ID</b> —RO. See <a href="#">Section 1.4</a> for the value of the RID Register.

#### 25.1.6 CLLH—Cache Line Latency Header Register (UART—D21:F5/F6)

Offset Address: 0Ch-0Fh      Attribute: R/W, RO  
 Default Value: 00800000h      Size: 32 bits

Bit	Description
31:24	Reserved
23	<b>Multi-Function Device</b> —RO
22:16	<b>Header Type</b> —RO
15:8	<b>Latency Timer</b> —RO
7:0	<b>Cache Line Size</b> —R/W

### 25.1.7 BAR0—Memory Base Address 0 Register (UART—D21:F5/F6)

Address Offset: 10–13h  
Default Value: 00000000h

Attributes: R/W, RO  
Size: 32 bits

Bit	Description
31:12	<b>Base Address 0</b> —R/W. Provides system memory base address for the UART logic.
11:4	<b>Size Indicator</b> —RO
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that BAR0 is not prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO.
0	<b>Memory Space Indicator</b> —RO. This read-only bit always is 0, indicating that the UART logic is Memory mapped.

### 25.1.8 BAR1—Memory Base Address 1 Register (UART—D21:F5/F6)

Address Offset: 14h–17h  
Default Value: 00000000h

Attributes: RO, R/W  
Size: 32 bits

Bit	Description
31:12	<b>Base Address 1</b> —R/W. Provides system memory base address for the UART logic.
11:4	<b>Size Indicator</b> —RO
3	<b>Prefetchable (PREF)</b> —RO. Hardwired to 0. Indicates that BAR1 is not prefetchable.
2:1	<b>Address Range (ADDRNG)</b> —RO.
0	<b>Memory Space Indicator 1</b> —RO. This read-only bit always is 0, indicating that the SPI logic is Memory mapped.

### 25.1.9 SVID—Subsystem Vendor Identification Register (UART—D21:F5/F6)

Address Offset: 2Ch–2Dh  
Default Value: 0000h

Attribute: R/WO  
Size: 16 bits

Bit	Description
15:0	<b>Subsystem Vendor ID (SVID)</b> —R/WO. The SVID register, in combination with the Subsystem ID (SID) register, enables the operating system (OS) to distinguish subsystems from each other. <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 25.1.10 SID—Subsystem Identification Register (UART—D21:F5/F6)

Address Offset: 2Eh–2Fh      Attribute: R/WO  
 Default Value: 0000h      Size: 16 bits

Bit	Description
15:0	<b>Subsystem ID (SID)</b> —R/WO. The SID register, in combination with the SVID register, enables the operating system (OS) to distinguish subsystems from each other.  <b>Note:</b> Software can write to this register only once per core well reset. Writes should be done as a single 16-bit cycle.

### 25.1.11 CAPPTR—Capabilities Pointer Register (UART—D21:F5/F6)

Address Offset: 34h–35h      Attribute: RO  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Power Capabilities (CAPPTR_POWER)</b> —RO

### 25.1.12 INT\_LN—Interrupt Line Register (UART—D21:F5/F6)

Address Offset: 3Ch      Attributes: R/W  
 Default Value: 00h      Size: 8 bits

Bit	Description
7:0	<b>Interrupt Line (INT_LN)</b> —R/W. This data is not used by the PCH. It is to communicate to software the interrupt line that the interrupt pin is connected to.

### 25.1.13 INT\_PN—Interrupt Pin Register (UART—D21:F5/F6)

Address Offset: 3Dh      Attributes: RO  
 Default Value: 01h      Size: 8 bits

Bit	Description
7:4	Reserved
3:0	<b>Interrupt PIN (INT_PN)</b> —RO

### 25.1.14 PWR\_CAP—Power Capability Register (UART—D21:F5/F6)

Address Offset: 80h-83h  
Default Value: 00030001h

Attributes: RO  
Size: 32 bits

Bit	Description
31:27	<b>PME Support</b> —RO
26:16	Reserved
15:8	<b>Next Capability (NXT_CAP)</b> —RO
7:0	<b>Power Capabilities (PWR_CAP)</b> —RO. Hardwired to 01h.

### 25.1.15 PME\_CTRL\_STA—PME Control and Status Register (UART—D21:F5/F6)

Address Offset: 84h-87h  
Default Value: 00000008h

Attributes: RO, R/W, R/WC  
Size: 32 bits

Bit	Description
31:16	Reserved
15	<b>PME Status (PME_STA)</b> —RW/C
14:9	Reserved
8	<b>PME Enable (PME_EN)</b> —R/W
7:4	Reserved
3	<b>No Soft Reset</b> —RO. Hardwired to 1.
2	Reserved
1:0	<b>Power State (PWR_STATE)</b> —R/W.

## 25.2 UART Memory Mapped I/O Registers

The DMA MMIO registers can be accessed through BAR0 in PCI mode or through BAR1 when in ACPI mode (for example, when PCI Configuration space is hidden). BAR0 and BAR1 are located in PCI configuration space.

**Note:** Only 32-bit operation is supported.

**Table 25-2. UART I/O and Memory Mapped I/O Register Address Map**

BAR + Offset	Mnemonic	Register Name	Default	Attributes
00h	RBR_THR_DLL	Receive Buffer/Transmit Holding/Divisor Latch Low	00000000h	R/W, RO, WO
04h	IER_DLH	Interrupt Enable/Divisor Latch High	00000000h	R/W, RO
08h	IIR_FCR	Interrupt Identification/FIFO Control	00000001h	R/W, RO, WO
0Ch	LCR	Line Control	00000001h	R/W, RO
10h	MCR	Modem Control	00000000	R/W, RO
14h	LSR	Line Status	00000060h	RO
18h	MSR	Modem Status	00000000h	RO
1Ch	SCR	Scratchpad	00000000h	R/W, RO
30h-6Ch	SRBR_STHR[15:0]	Shadow Receive/Transmit Holding 0 to 15	00000000h	RO, R/W
70h	FAR	FIFO Access	00000000h	R/W, RO
74h	TFR	Transmit FIFO Read	00000000h	RO
78h	RFW	Receive FIFO Write	00000000h	WO, RO
7Ch	USR	UART Status	0000006h	RO
80h	TFL	Transmit FIFO Level	00000000h	RO
84h	RFL	Receive FIFO Level	00000000h	RO
88h	SRR	Software Reset	00000000h	WO, RO
8Ch	SRTS	Shadow Request	00000000h	R/W, RO
90h	SBCR	Shadow Break Control	00000000h	R/W, RO
94h	SDMAM	Shadow DMA Mode	00000000h	R/W, RO
98h	SFE	Shadow FIFO Enable	00000000h	R/W, RO
9Ch	SRT	Shadow Receiver Trigger	00000000h	R/W, RO
A0h	STET	Shadow Transmitter Empty Trigger	00000000h	R/W, RO
A4h	HTX	Halt Transmit	00000000h	R/W, RO
A8h	DMASA	DMA Software Acknowledge	00000000h	WO, RO
800h	CLK_PARM	Clock Parameter	00000000h	R/W
804h	RESET	Reset	00000000h	R/W, RO
808h	GEN	General	00000000h	R/W, RO
810h	SW_LTR_VAL	Software LTR Value	00000800h	R/W, RO
814h	Auto_LTR_VAL	Auto LTR Value	00000800h	R/W, RO
818h	TX_BYTE_COUNT	TX Byte Count	00000000h	RO
820h	TX_INTR_MASKT	TX Interrupt Mask	00000000h	R/W, RO

## 25.2.1 RBR\_THR\_DLL—Receive Buffer/Transmit Holding/Divisor Latch Low Register (UART—D23:F5/6)

Register Offset: BAR + 00h  
Default Value: 00000000h

Attribute: RO/WO/RW  
Size: 32 bits

This register is utilized for different purposes. RBR/THR modes are only available when LCR register [7] (DLAB bit) = 0. DLL mode is available when LCR register [7] (DLAB bit) = 1

Bit	Description
31:8	Reserved
7:0	<p><b>RBR</b>—RO. Data byte received on the serial input port (sin) in UART mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set.  If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an over-run error.  If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an over-run error occurs.</p> <p><b>THR</b>—WO.  Data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If FIFOs are disabled (FCR[0] = 0) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If FIFOs are enabled (FCR[0] = 1) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p> <p><b>DLL</b>—R/W.  Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set.</p> <p>The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock frequency)/(16 * divisor).</p> <p><b>Note:</b> With the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.</p>



## 25.2.2 IER\_DLH—Interrupt Enable/Divisor Latch High Register (UART—D23:F5/6)

Register Offset: BAR + 04h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

This register is utilized for different purposes. IER modes are only available when LCR register [7] (DLAB bit) = 0. DLH mode is available when LCR register [7] (DLAB bit) = 1

### As DLH

Bit	Description
31:8	Reserved
7:0	<p><b>DLH</b>—R/W. Upper 8-bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may be accessed only when the DLAB bit (LCR[7]) is set. The output baud rate is equal to the serial clock frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock frequency)/(16 * divisor).</p> <p><b>Note:</b> With the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data</p>

### As IER:

Bit	Description
31:8	Reserved
7	<p><b>IER: PTIME (PTIME)</b>—R/W. THRE Interrupt Mode Enable. This is used to enable/disable the generation of THRE Interrupt.            0 = disabled            1 = enabled</p>
6:4	Reserved
3	<p><b>IER: EDSSI (EDSSI)</b>—R/W. Enable Modem Status Interrupt. This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt.            0 = disabled            1 = enabled</p>
2	<p><b>IER: ELSI (ELSI)</b>—R/W. Enable Receiver Line Status Interrupt. This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt.            0 = disabled            1 = enabled</p>
1	<p><b>IER: ETBEI (ETBEI)</b>—R/W. Enable Transmit Holding Register Empty Interrupt. This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt.            0 = disabled            1 = enabled</p>
0	<p><b>IER: ERBFI (ERBFI)</b>—R/W. Enable Received Data Available Interrupt. This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts.            0 = disabled            1 = enabled</p>

### 25.2.3 IIR\_FCR—Interrupt Identification/FIFO Control Register (UART—D23:F5/6)

Register Offset: BAR + 08h  
Default Value: 00000001h

Attribute: RO/WO  
Size: 32 bits

Bit	Description
31:8	Reserved
7:6	<p><b>IIR: FIFOE (FIFOE)</b>—RO. FIFOs Enabled. This is used to indicate whether the FIFOs are enabled or disabled.  00 = disabled  11 = enabled</p> <p><b>FCR: RT (RT)</b>—WO. RCVR Trigger. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. The following trigger levels are supported:  00 = 1 character in the FIFO  01 = FIFO 1/4 full  10 = FIFO 1/2 full  11 = FIFO 2 less than full</p>
5:4	<p><b>IIR: Reserved</b>—WO</p> <p><b>FCR: TET</b>—WO. TX Empty Trigger. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. The following trigger levels are supported:  00 = FIFO empty  01 = 2 characters in the FIFO  10 = FIFO 1/4 full  11 = FIFO 1/2 full</p>
3:0	<p><b>IIR: IID (IID)</b>—RO. Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types:  0000 = modem status  0001 = no interrupt pending  0010 = THR empty  0100 = received data available  0110 = receiver line status  0111 = busy detect  1100 = character timeout</p> <p><b>Note:</b> An interrupt of type 0111 (busy detect) is never indicated because the controller is compatible with UART_16550 mode. Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.</p> <p><b>FCR: IID (IID)</b>—R/W.</p> <p>Bit 3: Reserved. Standard DMA signals are generated.</p> <p>Bit 2: SFIFOR. XMIT FIFO Reset. This resets the control portion of the transmit FIFO and treats the FIFO as empty.</p> <p><b>Note:</b> This bit is 'self-clearing'. It is not necessary to clear this bit.</p> <p>Bit 1: SFIFOR. RCVR FIFO Reset. This resets the control portion of the receive FIFO and treats the FIFO as empty.</p> <p><b>Note:</b> This bit is 'self-clearing'. It is not necessary to clear this bit.</p> <p>Bit 0: FIFOE. FIFO Enable. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset</p>

## 25.2.4 LCR—Line Control Register (UART—D23:F5/6)

Register Offset: BAR + 0Ch      Attribute: R/W, RO  
 Default Value: 00000001h      Size: 32 bits

Bit	Description
31:8	Reserved
7	<b>Divisor Latch Access Bit (DLAB)</b> —R/W. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers
6	<b>Break Control Bit (BREAK)</b> —R/W. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. When in Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low
5	Reserved
4	<b>Even Parity Select (EPS)</b> —R/W. This is used to select between even and odd parity, when parity is enabled (PEN set to one). 0 = An odd number of logic 1s is transmitted or checked 1 = An even number of logic 1s is transmitted or checked
3	<b>Parity Enable (PEN)</b> —R/W. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively 0 = Disabled 1 = Enabled
2	<b>Number of Stop Bits (STOP)</b> —R/W. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits is transmitted. Otherwise, two stop bits are transmitted.  <b>Note:</b> Regardless of the number of stop bits selected the receiver checks only the first stop bit. 0 = 1 stop bit 1 = 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit
1:0	<b>Data Length Select (DLS)</b> —R/W. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected are as follows: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

## 25.2.5 MCR—Modem Control Register (UART—D23:F5/6)

Register Offset: BAR + 10h      Attribute: RO, R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:6	Reserved
5	<b>Auto Flow Control Enable (AFCE)</b> —R/W. When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set. The bit is used to help for flow control using external I/O pins with the pairing device. 0 = Auto Flow Control Mode disabled 1 = Auto Flow Control Mode enabled

Bit	Description
4	<b>Loop Back (LOOPBACK)</b> —R/W. This is used to put the UART into a diagnostic mode for test purposes. Data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional. Also, in loop back mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	<b>OUT2 (OUT2)</b> —R/W. This is used to directly control the user-designated Output2 (out2_n) output. The value written to this location is inverted and driven out on out2_n, that is: 0 = out2_n de-asserted (logic 1) 1 = out2_n asserted (logic 0). <b>Note:</b> In Loopback mode (MCR[4] set to one), the out2_n output is held inactive high while the value of this location is internally looped back to an input.
2	<b>OUT1 (OUT1)</b> —R/W. This is used to directly control the user-designated Output1 (out1_n) output. The value written to this location is inverted and driven out on out1_n, that is: 0 = out1_n de-asserted (logic 1) 1 = out1_n asserted (logic 0). <b>Note:</b> In Loopback mode (MCR[4] set to one), the out1_n output is held inactive high while the value of this location is internally looped back to an input.
1	<b>Request to Send (RTS)</b> —R/W. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low. <b>Note:</b> In Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.
0	<b>Data Terminal Ready (DTR)</b> —R/W. This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n, that is: 0 = dtr_n de-asserted (logic 1) 1 = dtr_n asserted (logic 0). The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications. <b>Note:</b> In Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.

## 25.2.6 LSR—Line Status Register (UART—D23:F5/6)

Register Offset: BAR + 14h  
Default Value: 00000060h

Attribute: RO  
Size: 32 bits

Bit	Description
31:8	Reserved
7	<b>Rx FIFO Error (RFE)</b> —RO. This bit is only relevant when FIFOs are enabled (FCR[0] set to one). This is used to indicate if there is at least one parity error, framing error, or break indication in the FIFO. 0 = No error in Rx FIFO 1 = Error in Rx FIFO This bit is cleared when the LSR is read and the character with the error is at the top of the receiver FIFO and there are no subsequent errors in the FIFO.



Bit	Description
6	<b>Tx Empty (TEM)</b> —RO. If FIFOs enabled(FCR[0] set to one), this bit is set whenever the Transmitter Shift Register and the FIFO are both empty. If FIFOs are disabled, this bit is set whenever the Transmitter Holding Register and the Transmitter Shift Register are both empty.
5	<b>Tx Holding Register Empty (THRE)</b> —RO. If THRE mode is disabled (IER[7] set to zero) and regardless of FIFO's being implemented/enabled or not, this bit indicates that the THR or TX FIFO is empty. This bit is set whenever data is transferred from the THR or TX FIFO to the transmitter shift register and no new data has been written to the THR or TX FIFO. This also causes a THRE Interrupt to occur, if the THRE Interrupt is enabled. If both THRE Interrupt and FIFO modes are active (IER[7] set to one and FCR[0] set to one respectively), the functionality is switched to indicate the transmitter FIFO is full, and no longer controls THRE interrupts, which are then controlled by the FCR[5:4] threshold setting
4	<b>Break Interrupt (BI)</b> —RO. This is used to indicate the detection of a break sequence on the serial input data. It is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of start time + data bits + parity + stop bits. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART. In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read
3	<b>Framing Error (FE)</b> —RO. This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data. In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to re-synchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit(LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit(LSR[4]) 0 = No error 1 = Framing error. Reading the LSR clears the FE bit.
2	<b>Parity Error (PE)</b> —RO. This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]). 0 = No error 1 = Parity error Reading the LSR clears the PE bit.
1	<b>Overrun Error Bit (OE)</b> —RO. This is used to indicate the occurrence of an overrun error. This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost. 0 = No overrun error 1 = Overrun error. Reading the LSR clears the OE bit
0	<b>Data Ready (DR)</b> —RO. This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO 0 = No data Ready 1 = Data Ready This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode



## 25.2.7 MSR—Modem Status Register (UART—D23:F5/6)

Register Offset: BAR + 18h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Whenever bits 0, 1, 2 or 3 are set to logic one, to indicate a change on the modem control inputs, a modem status interrupt is generated if enabled through the IER, regardless of when the change occurred. Since the delta bits—(bits 0, 1, 3) can get set after a reset if their respective modem signals are active (see individual bits for details), a read of the MSR after reset can be performed to prevent unwanted interrupts.

Bit	Description
31:8	Reserved
7	<b>Data Carrier Detect (DCD)</b> —RO. This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0 = dcd_n input is de-asserted (logic 1) 1 = dcd_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DCD is the same as MCR[3] (Out2).
6	<b>Ring Indicator (RI)</b> —RO. This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0 = ri_n input is de-asserted (logic 1) 1 = ri_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), RI is the same as MCR[2] (Out1)
5	<b>Data Set Ready (DSR)</b> —RO. This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with the UART. 0 = dsr_n input is de-asserted (logic 1) 1 = dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as MCR[0] (DTR).
4	<b>Clear to Send (CTS)</b> —RO. This is used to indicate the current state of the modem control line cts_n. This bit is the complement of cts_n. When the Clear to Send input (cts_n) is asserted it is an indication that the modem or data set is ready to exchange data with the UART. 0 = cts_n input is de-asserted (logic 1) 1 = cts_n input is asserted (logic 0) In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).
3	<b>Delta Data Carrier Detect (DDCD)</b> —RO. This is used to indicate that the modem control line dcd_n has changed since the last time the MSR was read. 0 = no change on dcd_n since last read of MSR 1 = change on dcd_n since last read of MSR Reading the MSR clears the DDCD bit. In Loopback Mode (MCR[4] = 1), DDCD reflects changes on MCR[3] (Out2). <b>Note:</b> If the DDCD bit is not set and the dcd_n signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the dcd_n signal remains asserted.
2	<b>Trailing Edge Of Ring Indicator (TERI)</b> —RO. This is used to indicate that a change on the input ri_n (from an active-low to an inactive-high state) has occurred since the last time the MSR was read. 0 = no change on ri_n since last read of MSR 1 = change on ri_n since last read of MSR Reading the MSR clears the TERI bit. In Loopback Mode (MCR[4] = 1), TERI reflects when MCR[2] (Out1) has changed state from a high to a low.



Bit	Description
1	<p><b>Delta Data Set Ready (DDSR)</b>—RO. This is used to indicate that the modem control line <code>dsr_n</code> has changed since the last time the MSR was read.</p> <p>0 = no change on <code>dsr_n</code> since last read of MSR 1 = change on <code>dsr_n</code> since last read of MSR</p> <p>Reading the MSR clears the DDSR bit. In Loopback Mode (MCR[4] = 1), DDSR reflects changes on MCR[0] (DTR).</p> <p><b>Note:</b> If the DDSR bit is not set and the <code>dsr_n</code> signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the <code>dsr_n</code> signal remains asserted.</p>
0	<p><b>Delta Clear to Send (DCTS)</b>—RO. This is used to indicate that the modem control line <code>cts_n</code> has changed since the last time the MSR was read.</p> <p>0 = no change on <code>cts_n</code> since last read of MSR 1 = change on <code>cts_n</code> since last read of MSR</p> <p>Reading the MSR clears the DCTS bit. In Loopback Mode (MCR[4] = 1), DCTS reflects changes on MCR[1] (RTS).</p> <p><b>Note:</b> If the DCTS bit is not set and the <code>cts_n</code> signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the <code>cts_n</code> signal remains asserted.</p>

## 25.2.8 SCR—Scratchpad Register (UART—D23:F5/6)

Register Offset: BAR + 1Ch  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<b>Scratchpad (SCR)</b> —R/W. This field is for software use. There is no hardware impact.

## 25.2.9 SRBR\_STHR[15:0]—Shadow Receive Buffer/Shadow Transmit Holding [15:0] Register (UART—D23:F5/6)

Register Offset: BAR + 30h (Register 0)  
BAR + 34h (Register 1)  
BAR + 38h (Register 2)  
.....  
BAR + 68h (Register 14)  
BAR + 6Ch (Register 15)  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:8	Reserved

Bit	Description
7:0	<p><b>Shadow Receive Buffer (SRBR)</b>—RO.</p> <p>This is a shadow register for the RBR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains the data byte received on the serial input port (sin) in UART. The data in this register is valid only if the Data Ready (DR) bit in the Line status Register (LSR) is set.</p> <p>If FIFOs are disabled (FCR[0] set to zero), the data in the RBR must be read before the next data arrives, otherwise it is overwritten, resulting in an overrun error.</p> <p>If FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO are preserved, but any incoming data is lost. An overrun error also occurs.</p> <p><b>Shadow Transmit Holding (STHR)</b>—WO</p> <p>This is a shadow register for the THR and has been allocated sixteen 32-bit locations so as to accommodate burst accesses from the master. This register contains data to be transmitted on the serial output port (sout) in UART mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set.</p> <p>If FIFOs are disabled (FCR[0] set to zero) and THRE is set, writing a single character to the THR clears the THRE. Any additional writes to the THR before the THRE is set again causes the THR data to be overwritten.</p> <p>If FIFOs are enabled (FCR[0] set to one) and THRE is set, x number of characters of data may be written to the THR before the FIFO is full. The number x (default=16) is determined by the value of FIFO Depth that you set during configuration. Any attempt to write data when the FIFO is full results in the write data being lost.</p>

### 25.2.10 FAR—FIFO Access Register (UART—D23:F5/6)

Register Offset: BAR + 70h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<p><b>FIFO Access (FAR)</b>—R/W. This register is used to enable a FIFO access mode for testing, so that the receive FIFO can be written by the master and the transmit FIFO can be read by the master when FIFOs are implemented and enabled. When FIFOs are not implemented or not enabled it allows the RBR to be written by the master and the THR to be read by the master.</p> <p>0 = FIFO access mode disabled  1 = FIFO access mode enabled</p> <p><b>Note:</b> When the FIFO access mode is enabled/ disabled, the control portion of the receive FIFO and transmit FIFO is reset and the FIFOs are treated as empty</p>

### 25.2.11 TFR—Transmit FIFO Read Register (UART—D23:F5/6)

Register Offset: BAR + 74h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:8	Reserved
7:0	<p><b>Transmit FIFO Read (TFR)</b>—RO. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one).</p> <p>When FIFOs are implemented and enabled, reading this register gives the data at the top of the transmit FIFO. Each consecutive read pops the transmit FIFO and gives the next data value that is currently at the top of the FIFO.</p> <p>When FIFOs are not implemented or not enabled, reading this register gives the data in the THR.</p>

## 25.2.12 RFW—Receive FIFO Write Register (UART—D23:F5/6)

Register Offset: BAR + 78h      Attribute: WO, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:10	Reserved
9	<b>Receive FIFO Framing Error (RFFE)</b> —WO. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write framing error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write framing error detection information to the RBR.
8	<b>Receive FIFO Parity Error (RFPE)</b> —WO. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, this bit is used to write parity error detection information to the receive FIFO. When FIFOs are not implemented or not enabled, this bit is used to write parity error detection information to the RBR.
7:0	<b>Receive FIFO Write Data (RFWD)</b> —WO. These bits are only valid when FIFO access mode is enabled (FAR[0] is set to one). When FIFOs are enabled, the data that is written to the RFWD is pushed into the receive FIFO. Each consecutive write pushes the new data to the next write location in the receive FIFO. When FIFOs are not implemented or not enabled, the data that is written to the RFWD is pushed into the RBR.

## 25.2.13 USR—UART Status Register (UART—D23:F5/6)

Register Offset: BAR + 7Ch      Attribute: RO  
 Default Value: 00000006h      Size: 32 bits

Bit	Description
31:5	Reserved
4	<b>Receive FIFO Full (RFF)</b> —RO 0 = Rx FIFO is not full 1 = Rx FIFO is full This bit is cleared when the Rx FIFO is no longer full
3	<b>Receive FIFO Not Empty (RFNE)</b> —RO 0 = Rx FIFO is empty 1 = Rx FIFO is not empty This bit is cleared when the Rx FIFO is empty.
2	<b>Transmit FIFO Empty (TFE)</b> —RO 0 = Tx FIFO is not empty 1 = Tx FIFO is empty This bit is cleared when the Tx FIFO is no longer empty.
1	<b>Transmit FIFO Not Full (TFNF)</b> —RO 0 = Tx FIFO is full 1 = Tx FIFO is not full This bit is cleared when the Tx FIFO is full.
0	Reserved

## 25.2.14 TFL—Transmit FIFO Level Register (UART—D23:F5/6)

Register Offset: BAR + 80h      Attribute: RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:5	Reserved
4:0	<b>Transmit FIFO Level</b> —RO. Indicates the number of data entries in the Tx FIFO



### 25.2.15 RFL—Receive FIFO Level Register (UART—D23:F5/6)

Register Offset: BAR + 84h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:5	Reserved
4:0	<b>Receive FIFO Level</b> —RO. Indicates the number of data entries in the Rx FIFO

### 25.2.16 SRR—Software Reset Register (UART—D23:F5/6)

Register Offset: BAR + 88h  
Default Value: 00000000h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31:3	Reserved
2	<b>Tx FIFO Reset (XFR)</b> —R/W. This is a shadow register for the transmit FIFO Reset bit (FCR[2]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the transmit FIFO. This resets the control portion of the transmit FIFO and treats the FIFO as empty. <b>Note:</b> This bit is 'self-clearing'. It is not necessary to clear this bit.
1	<b>Rx FIFO Reset (RFR)</b> —R/W. This is a shadow register for the receive FIFO Reset bit (FCR[1]). This can be used to remove the burden on software having to store previously written FCR values (which are pretty static) just to reset the receive FIFO. This resets the control portion of the receive FIFO and treats the FIFO as empty. <b>Note:</b> This bit is 'self-clearing'. It is not necessary to clear this bit.
0	<b>UART Reset (UR)</b> —R/W. This asynchronously resets the UART and synchronously remove the reset assertion.

### 25.2.17 SRTS—Shadow Request Register (UART—D23:F5/6)

Register Offset: BAR + 8Ch  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Shadow Request To Send (SRTS)</b> —R/W. This is a shadow register for the RTS bit (MCR[1]). This can be used to remove the burden of having to perform a read-modify-write on the MCR. This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] = 0), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control active (MCR[5] = 1) and FIFOs enable (FCR[0] = 1), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). <b>Note:</b> In Loopback mode (MCR[4] = 1), the rts_n output is held inactive-high while the value of this location is internally looped back to an input.

## 25.2.18 SBCR—Shadow Break Control Register (UART—D23:F5/6)

Register Offset: BAR + 90h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Shadow Break Control (SBCB)</b> —R/W. This is a shadow register for the Break bit (LCR[6]), this can be used to remove the burden of having to performing a read modify write on the LCR. This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. When in Loopback Mode, the break condition is internally looped back to the receiver.

## 25.2.19 SDMAM—Shadow DMA Mode Register (UART—D23:F5/6)

Register Offset: BAR + 94h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Shadow DMA Mode (SDMAM)</b> —R/W. This is a shadow register for the DMA mode bit (FCR[3]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the DMA Mode bit gets updated. 0 = Mode 0 1 = Mode 1

## 25.2.20 SFE—Shadow FIFO Enable Register (UART—D23:F5/6)

Register Offset: BAR + 98h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Shadow FIFO Enable (SFE)</b> —R/W. This is a shadow register for the FIFO enable bit (FCR[0]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the FIFO enable bit gets updated. This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. If this bit is set to zero (disabled) after being enabled then both the XMIT and RCVR controller portion of FIFOs are reset.

### 25.2.21 SRT—Shadow Receiver Trigger Register (UART—D23:F5/6)

Register Offset: BAR + 9Ch  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:2	Reserved
1:0	<b>Shadow Receiver Trigger (SRT)</b> —R/W. This is a shadow register for the RCVR trigger bits(FCR[7:6]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the RCVR trigger bit gets updated. This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. It also determines when the dma_rx_req_n signal is asserted when DMA Mode (FCR[3]) = 1. The following trigger levels are supported: 00 = 1 character in the FIFO 01 = FIFO ¼ full 10 = FIFO ½ full 11 = FIFO 2 less than full

### 25.2.22 STET—Shadow Transmitter Empty Trigger Register (UART—D23:F5/6)

Register Offset: BAR + A0h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:2	Reserved
1:0	<b>Shadow TX Empty Trigger (STET)</b> —R/W. This is a shadow register for the TX empty trigger bits(FCR[5:4]). This can be used to remove the burden of having to store the previously written value to the FCR in memory and having to mask this value so that only the TX empty trigger bit gets updated. This is used to select the empty threshold level at which the Interrupts are generated when the mode is active. The following trigger levels are supported: 00 = FIFO empty 01 = 2 characters in the FIFO 10 = FIFO ¼ full 11 = FIFO ½ full

### 25.2.23 HTX—Halt Transmit Register (UART—D23:F5/6)

Register Offset: BAR + A4h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:1	Reserved
0	<b>Halt TX (HTX)</b> —R/W. This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled. 0 = Halt TX disabled 1 = Halt TX enabled <b>Note:</b> If FIFOs are not enabled, the setting of the halt TX register has no effect on operation.

### 25.2.24 DMASA—DMA Software Acknowledge Register (UART—D23:F5/6)

Register Offset: BAR + A8h      Attribute: WO, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:2	Reserved
0	<b>DMA Software Acknowledge (DMASA)</b> —R/W. This register is used to perform a DMA software acknowledge if a transfer needs to be terminated due to an error condition. For example, if the DMA disables the channel, then the UART should clear its request. This causes the TX request, TX single, RX request and RX single signals to de-assert. <b>Note:</b> This bit is 'self-clearing'. It is not necessary to clear this bit.

### 25.2.25 CLK\_PARM—Clock Parameter Register (UART—D23:F5/6)

Register Offset: BAR + 800h      Attribute: R/W  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31	<b>Clock Update</b> —R/W 0 = No clock update 1 = clock gets updated
30:16	<b>N_VAL</b> —R/W. This is the denominator value for the M over N divider logic that creates the SPI_CLK_OUT for the SSP. (M/N value used to generate input clk to SSP)
15:1	<b>M_VAL</b> —R/W. The numerator value for the M over N divider logic that creates the SPI_CLK_OUT for the SSP.
0	<b>Clock Enable</b> —R/W 0 = Clock disabled 1 = Clock enabled

### 25.2.26 RESET—Reset Register (UART—D23:F5/6)

Register Offset: BAR + 804h      Attribute: R/W, RO  
 Default Value: 00000000h      Size: 32 bits

Bit	Description
31:2	Reserved
1:0	<b>UART Host Controller Reset</b> —R/W. This bit is used to reset the UART Host Controller by software control. All UART Configuration State and Operational State will be forced to the Default state. There is no timing requirement (software can assert and de-assert in back to back transactions) Driver should re-initialize registers related to Driver context following an UART host controller reset. 00 = UART in Reset—(Reset Asserted) 01 = Reserved 10 = Reserved 11 = UART out of Reset—(Reset de-asserted)

## 25.2.27 GEN—General Register (UART—D23:F5/6)

Register Offset: BAR + 808h  
Default Value: 00000000h

Attribute: R/W, RO  
Size: 32 bits

Bit	Description
31:1	Reserved
2	<p><b>LTR Mode</b>—R/W.  0 = Auto mode  1 = Software mode</p> <p>In the auto mode, the BIOS will write to the "host controllers Auto LTR register (offset 0x814) with the active state LTR value and software LTR register (offset 0x810) with the idle state LTR value. When the host controller goes active, the reported LTR value forwarded to the coalescing logic (see below) will be the value in the Auto LTR register. When the host controller goes inactive (Idle), the reported LTR value will be taken from the Software LTR register (offset 0x810).</p> <p>The following must be true for at least one character time for the assertion of the Idle state to occur:</p> <ul style="list-style-type: none"> <li>• RX FIFO is empty (in FIFO mode)</li> <li>• TX FIFO is empty (in FIFO mode)</li> <li>• sin and sout are inactive indicating no activity</li> <li>• No change on the CTS modem control input signal</li> </ul> <p>In software mode the software will write to the host controllers Software LTR register (offset 0x810). The value will then be forwarded to the hardware coalescing logic (see below). It is the software's responsibility to update the LTR with the appropriate value.</p> <p><b>Note:</b> If the software does not update the Software LTR register no LTR value will be forwarded to the coalescing logic (see below), effectively disabling LTR generation for this module.</p>
1:0	Reserved



## 25.2.28 SW\_LTR\_VAL—Software LTR Value Register (UART—D23:F5/6)

Register Offset: BAR + 810h Attribute: R/W, RO  
Default Value: 00000800h Size: 32 bits

Bit	Description
31	<b>Non Snoop Requirement</b> —RO. If bit 15 is clear, that indicates the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely). If the 10 bit latency value is 0, it indicates that the device cannot tolerate any delay and needs the best possible service/response time
30:29	Reserved
28:26	<b>Non Snoop Latency Scale</b> —RO. Support for codes 010 (1 µs) or 011 (32 µs) for snoop latency scale (1 µs – 32 ms total span) only. Writes to this CSR which don't match those value will be dropped completely; next read will return previous value.
25:16	<b>Non Snoop Value</b> —RO. 10-bit latency value.
15	<b>Snoop Requirement</b> —R/W. If this bit is clear, that indicates the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely). If the 10-bit latency value is 0, it indicates that the device cannot tolerate any delay and needs the best possible service/response time
14:13	Reserved
12:10	<b>Snoop Latency Scale</b> —R/W. Support for codes 010 (1 µs) or 011 (32 µs) for snoop latency scale (1 µs – 32 ms total span) only. Writes to this CSR which don't match those value will be dropped completely; next read will return previous value.
9:0	<b>Snoop Value</b> —R/W. 10 latency value.

## 25.2.29 AUTO\_LTR\_VAL—Auto LTR Value Register (UART—D23:F5/6)

Register Offset: BAR + 814h Attribute: R/W, RO  
Default Value: 00000800h Size: 32 bits

Bit	Description
31	<b>Non Snoop Requirement</b> —RO. If bit 15 is clear, that indicates the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely). If the 10-bit latency value is 0, it indicates that the device cannot tolerate any delay and needs the best possible service/response time
30:29	Reserved
28:26	<b>Non Snoop Latency Scale</b> —RO. Support for codes 010 (1 µs) or 011 (32 µs) for snoop latency scale (1 µs – 32 ms total span) only. Writes to this CSR which don't match those value will be dropped completely; next read will return previous value.
25:16	<b>Non Snoop Value</b> —RO. 10-bit latency value.
15	<b>Snoop Requirement</b> —R/W. If this bit is clear, that indicates the device has no LTR requirement for this type of traffic (for example, it can wait for service indefinitely). If the 10-bit latency value is 0, it indicates that the device cannot tolerate any delay and needs the best possible service/response time
14:13	Reserved
12:10	<b>Snoop Latency Scale</b> —R/W. Support for codes 010 (1 µs) or 011 (32 µs) for snoop latency scale (1 µs – 32 ms total span) only. Writes to this CSR which don't match those value will be dropped completely; next read will return previous value.
9:0	<b>Snoop Value</b> —R/W. 10 latency value.

### 25.2.30 TX\_BYTE\_COUNT—TX Byte Count Register (UART—D23:F5/6)

Register Offset: BAR + 818h  
Default Value: 00000000h

Attribute: RO  
Size: 32 bits

Bit	Description
31:16	Reserved
15:0	<b>Tx Byte Count</b> —RO. 16-bit up-counter which counts the number of Tx Bytes transmitted onto the UART serial bus (pop of the UART TX FIFO). The Counter will be automatically cleared by hardware when the register is read.

### 25.2.31 TX\_INTR\_MASKT—TX Interrupt Mask Register (UART—D23:F5/6)

Register Offset: BAR + 820h  
Default Value: 00000000h

Attribute: RO, R/W  
Size: 32 bits

Bit	Description
31:2	Reserved
1	<b>Overflow Interrupt Mask</b> —R/W. When set, this bit masks the byte counter overflow interrupt.
0	<b>Overflow Interrupt</b> —RO. When set, this bit indicates byte counter overflow

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