ECE 425/520 - VLSI Design & Test Automation - Fall 2015
Lab 5 - Logic Synthesis at the RTL
Due Date: 10-19-2015

1 Objective

The objective of this lab is to **introduce two synthesis tools Cadence Encounter RTL compiler and Synopsys Design Compiler and perform some simple optimization using these tools**.

2 Exercises

1. Use the **EncounterRTLCompiler** tutorial.
   (a) Use the file **FullAdder.vhd** and finish upto the end of section 2 in the tutorial.
   (b) Use the file **c17.vhd** and finish upto the end of section 2 in the tutorial first, then optimize the area using the commands in Section 3.1 only. Similarly, use the file **c6288.v** and finish upto the end of section 2 in the tutorial first, then optimize the area using the commands in Section 3. The objective of this exercise is to obtain the minimum area for the given design with low overhead on power.
2. Use the **DesignCompiler** tutorial.
   (a) Use the file **FullAdder.vhd** and finish upto the end of section 2 in the tutorial.
   (b) Use the file **c17.v** and finish upto the end of section 2 in the tutorial first, then optimized the area using the commands in Section 3. **The given design constraints are input delay(Max,Min) = (6,0.2) and output delay (Max,Min) = (5,0.1) and wire model is the same as specified in the tutorial**. The objective of this exercise is to obtain the minimum possible area with small period value on the clock for the given design without violating the timing constraints.

Note: Exercises 1b and 2b focus on the optimization, points are awarded on relative grading basis.

3 Submission

1. For Exercises 1a and 2a, final mapped schematic and synthesized verilog code.
2. For Exercises 1b and 2b, final mapped schematic, synthesized verilog code (except c6288.v) and reports on area, power, timing, and (violations or constraints) before optimization and after final optimization. For 1b, form a table which shows the intermediate results on area, power, and respective operation done during optimization. For 2b, form a table which shows the intermediate results on area, power, time constraint status, and respective clock value during optimization.