États	Opérations entre registres
S_Init	PC 0x1000
S_Pre_Fetch	mem_addr ← mem[PC]
S_Fetch	IR ← mem_datain
S_Decode	PC ← PC + 4
S_LUI	RD ← $IR_{31..12}$ || 0^12 mem_addr ← mem[PC]
S_AUIPC	RD ← ($IR_{31..12}$ || 0^12) + PC mem_addr ← mem[PC]
S_JAL	rd ← PC + 4 cst = ($IR_{12\ 31}$ || $IR_{19..12}$ || IR_{20} || $IR_{30..25}$ || $IR_{24..21}$ || 0) PC ← PC + cst
S_JALR	rd ← PC + 4 PC ← (rs1 + ($IR_{20\ 31}$ || $IR_{31..20}$))$_{31..1}$ || 0
S_BEQ	cst = ($IR_{20\ 31}$ || IR_{7} || $IR_{30..25}$ || $IR_{11..8}$ || 0) if rs1 = rs2 ⇒ PC ← PC + cst else PC ← PC + 4
S_BNE	cst = ($IR_{20\ 31}$ || IR_{7} || $IR_{30..25}$ || $IR_{11..8}$ || 0) if rs1 ≠ rs2 ⇒ PC ← PC + cst else PC ← PC + 4
S_BLT	cst = ($IR_{20\ 31}$ || IR_{7} || $IR_{30..25}$ || $IR_{11..8}$ || 0) if rs1< rs2 ⇒ PC ← PC + cst else PC ← PC + 4
S_BGE	cst = ($IR_{20\ 31}$ || IR_{7} || $IR_{30..25}$ || $IR_{11..8}$ || 0) if rs1>= rs2 ⇒ PC ← PC + cst else PC ← PC + 4
S_BLTU	cst = ($IR_{20\ 31}$ || IR_{7} || $IR_{30..25}$ || $IR_{11..8}$ || 0) if rs1 $_{usg}$< rs2 ⇒ PC ← PC + cst else PC ← PC + 4
S_BGEU	cst = ($IR_{20\ 31}$ || IR_{7} || $IR_{30..25}$ || $IR_{11..8}$ || 0) if rs1 $_{usg}$>= rs2 ⇒ PC ← PC + cst else PC ← PC + 4
S_LB	mem_addr ← mem[($IR_{20\ 31}$ || $IR_{31..20}$) + rs1]$_{24\ 7}$ || mem[$IR_{20\ 31}$ || $IR_{31..20}$ + rs1]$_{7..0}$
S_LH	mem_addr ← mem[($IR_{20\ 31}$ || $IR_{31..20}$) + rs1]$_{16\ 15}$ || mem[($IR_{20\ 31}$ || $IR_{31..20}$) + rs1]$_{15..0}$
S_LW	mem_addr ← mem[($IR_{20\ 31}$ || $IR_{31..20}$) + rs1]
S_LBU	mem_addr ← 0^24 || mem[($IR_{20\ 31}$ || $IR_{31..20}$) + rs1]$_{7..0}$

S_LHU	mem_addr ← 0^16 || mem[(IR20 31 || IR31..20) + rs1]15..0
S_SB	cst = (IR20 31 || IR31..25 || IR11..7) mem_addr ← mem[cst+ rs1]
S_SH	cst = (IR20 31 || IR31..25 || IR11..7) mem_addr ← mem[cst+ rs1]
S_SW	cst = (IR20 31 || IR31..25 || IR11..7) mem_addr ← mem[cst+ rs1]
S_ADDI	rd ← rs1 + (IR20 31 || IR31..20) mem_addr ← mem[PC]
S_SLTI	rs1 < (IR20 31 || IR31..20) ⇒ rd ← 0^31 || 1 rs1 >= (IR20 31 || IR31..20) ⇒ rd ← 0^32 mem_addr ← mem[PC]
S_SLTIU	(0 || rs1) < (0 || (IR20 31 || IR31..20)) ⇒ rd ← 0^31 || 1 (0 || rs1) >= (0 || (IR20 31 || IR31..20)) ⇒ rd ← 0^32 mem_addr ← mem[PC]
S_XORI	rd ← (IR20 31 || IR31..20) xor rs1 mem_addr ← mem[PC]
S_ORI	rd ← (IR20 31 || IR31..20) or rs1 mem_addr ← mem[PC]
S_ANDI	rd ← (IR20 31 || IR31..20) and rs1 mem_addr ← mem[PC]
S_SLLI	rd ← rs231-shamt..0 || 0^shamt mem_addr ← mem[PC]
S_SRLI	rd ← 0^shamt || rs131..shamt mem_addr ← mem[PC]
S_SRAI	rd ← rs1shamt 31 || rs131..shamt mem_addr ← mem[PC]
S_ADD	rd ← rs1 + rs2 mem_addr ← mem[PC]
S_SUB	rd ← rs1 - rs2 mem_addr ← mem[PC]
S_SLL	rd ← rs131-rs24..0..0 || 0^rs24..0 mem_addr ← mem[PC]
S_SLT	rs1 < rs2 ⇒ rd ← 0^31 || 1 rs1 >= rs2 ⇒ rd ← 0^32 mem_addr ← mem[PC]
S_SLTU	(0 || rs1) < (0 || rs2) ⇒ rd ← 0^31 || 1 (0|| rs1) >= (0 || rs2) ⇒ rd ← 0^32 mem_addr ← mem[PC]
S_XOR	rd ← rs1 xor rs2 mem_addr ← mem[PC]

S_SRL	rd ← 0^$rs2_{4..0}$ || $rs1_{31..rs2_{4..0}}$ mem_addr ← mem[PC]
S_SRA	rd ← $rs1_{rs2_{4..0}\ 31}$ || $rs1_{31..rs2_{4..0}..0}$ mem_addr ← mem[PC]
S_OR	rd ← rs1 or rs2 mem_addr ← mem[PC]
S_AND	rd ← rs1 and rs2 mem_addr ← mem[PC]
LoadFromMemory	rd ← mem[mem_addr]
SaveInTheMemory	mem[mem_addr] ← rs2
ReadNextPCInstruction	mem_addr ← mem[PC]
WriteNewInstructionInPC	mem_addr ← mem[PC]