Final

Digital Circuit and Systems

Department of Electronics Engineering

National Chiao Tung University

15:30 ~ 18:30

Data Preparation

Extract test data from TA's directory:

% tar zxvf ~DCSta01/DCS_FINAL.tar

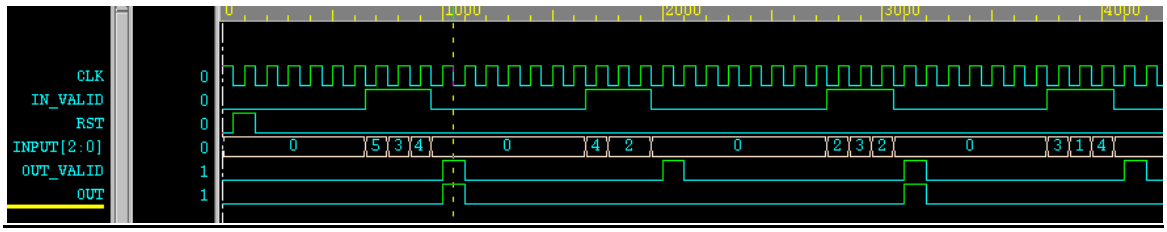
Problem Description

In the final exam, we give you series of number which present the length of side for triangle. The **IN_VALID** hold high for 3 cycles sequentially and you can get the three sides for triangle. And you should verify these three numbers can construct a triangle or not. After IN_VALID = 0, your output should be coming at most 5 cycles with **OUT_VALID** high.

If	**SideA + SideB > SideC**	**OUT = 1**
Else		**OUT = 0**

Hint:

Care about the overflow problem, maybe you can use **4 bits** register to contain the input.



Given Input

Input: **1-bit CLK, RST, IN_VALID**

3-bits INPUT (INPUT!= 0)

Output: **1-bits OUT, OUT_VALID**

Synchronous active high reset is used, and only once

Grading rule

You have two chances to demo. First time pass you can get 100, second time you get 80.

Execution of your program

Your program will only be executed with the following command. If your program fails to execute the following command, you will receive no credit for this lab.

%ncverilog –f Run.f