## Lab 4 – Test Pattern

Digital Circuit and Systems

Department of Electronics Engineering

National Chiao Tung University

Due Date: June 15<sup>th</sup>, June 16<sup>st</sup>

## **Data Preparation**

Extract test data from TA's directory:

% tar zxvf ~DCSta01/DCS\_LAB4.tar

## **Problem Description**

INPUT: 4 bits INPUT1, INPUT2

**OUTPUT: 6 bits OUT** 

The correct circuit is

OUT = INPUT1[3:0] + INPUT2[3:0]

But the circuit we give you is

OUT = INPUT1[2:0] + INPUT2[3:0]

Try to write a test pattern to prove the circuit is incorrect. Using \$display

## **Execution of your program**

Your program will only be executed with the following command. If your program fails to execute the following command, you will receive no credit for this lab.

%ncverilog -f Run.f