Lab2 - Sequential Logic

Digital Circuit and Systems
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Data Preparation

Extract test data from TA's directory:

% tar zxvf ~DCSta01/DCS_LAB2.tar

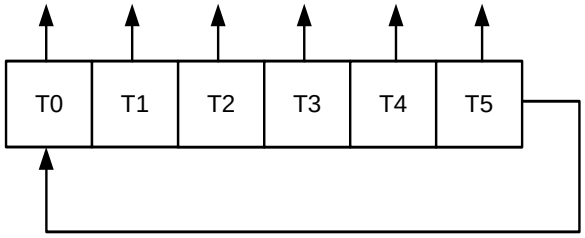
Problem Description

Ring Counter

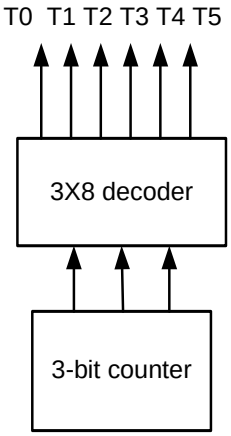
Timing signals that control the sequence of operations in a digital system can be generated by a shifter or by a counter with a decoder. A ring counter is a circular shift register with only one flip-flop being set at any particular time; all others are cleared. The single bit is shifted from one flip-flop to the next to produce the sequence of time signals.

Generate six repeated timing signals T0 through T5 similar to the ones show below. Design the circuit using

1. Flip-flop only



2. A counter and a decoder



Counter

When RST = 1, counter = 3'b 000.

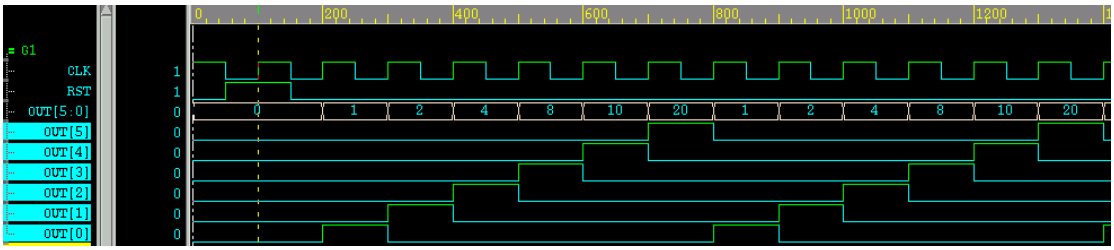
000-> 001-> 010-> 011->100->101->000 …

Given Input

Input: 1-bit **CLK**, **RST**

Output: 6-bits **OUT**.

Synchronous active high reset is used, and only once



Execution of your program

Your program will only be executed with the following command. If your program fails to execute the following command, you will receive no credit for this lab.

%ncverilog –f Run.f