# Lab3 - FSMs with Verilog

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**Data Preparation**

Extract test data from TA's directory:

**% tar zxvf ~DCSta01/DCS_LAB3.tar**

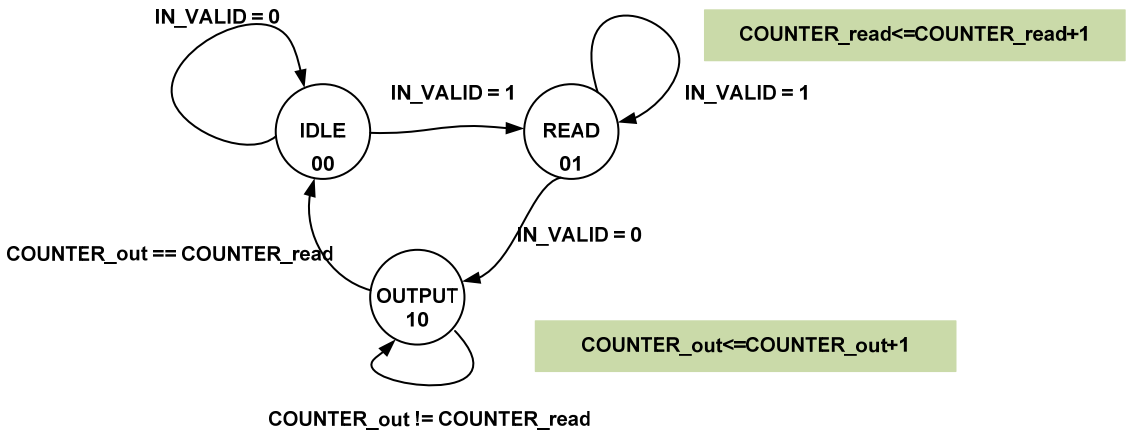
**Problem Description**

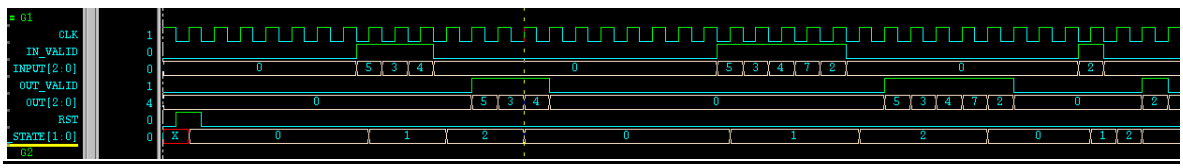
## Finite State Machine

Divide a sequential circuit operation into finite number of states.

A state machine controller can output results depending on the input signal, control signal and states.

As different input or control signal changes, the state machine will take a proper state transition.



```
always @ (posedge CLK)
    if(RST)
        CURRENT_STATE<=2'b00;
    else
        CURRENT_STATE<=NEXT_STATE;

always @*
    case(CURRENT_STATE)
      2'b00:
          if(IN_VALID==1'b1)
              NEXT_STATE<=2'b01;
          else
              NEXT_STATE<=CURRENT_STATE;
      2'b01:
          if(IN_VALID==1'b0)
              NEXT_STATE<=2'b10;
          else
              NEXT_STATE<=CURRENT_STATE;
      2'b10:
          if(COUNTER_out==COUNTER_read)
              NEXT_STATE<=2'b00;
          else
              NEXT_STATE<=CURRENT_STATE;
     endcase
```

**Given Input**

**Input: 1-bit CLK, RST, IN_VALID**
**3-bits INPUT**

**Output: 3-bits OUT.**
**1-bit OUT_VALID**

**Synchronous** active high reset is used, and only once

輸入為 3bit 的 INPUT, 當 IN_VALID = 1 時, 要去讀取 INPUT 的值, IN_VALID 可能維持 1~5 個 cycle(等同於可能輸入 1~5 個值). 此次 LAB 題目就為利用 FSM 去讀取動態的輸入值, 存取後在最後輸出. 輸出時 OUT_VALID 要 = 1, OUT 就為輸出值.

hint: 使用 register 來存值, 使用 counter 來算輸入值的個數.

**Execution of your program**

Your program will only be executed with the following command. If your program fails to execute the following command, you will receive no credit for this lab.

**%ncverilog –f Run.f**