H-bridge Design & Evaluation

TNE089 - Electromagnetic Compatibility and Printed Circuit Board Design

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Abstract

A H-bridge with a connecting driver is designed and evaluated from an EMC perspective. Tests are conducted to decide where the circuit have its maximum efficiency and how it differs with different duty cycles. The designed circuit had its maximum efficiency when driven with a 7 kHz PWM signal.

The objective of the H-bridge is to power a thrust fan of a hovercraft.

Contents

1 Introduction

A H-bridge specified to drive a 12 V 3 A motor will be designed. The circuit will then be evaluated with regards to efficiency and signal quality. The aim of this project is that the designed H-bridge shall have good EMC characteristics and that it can be used as part of another project in the course TNE085, where each instance of the circuit will be used to control a DC-motor on a hovercraft.

2 Theoretical background

A H-bridge is used to control speed and direction of a DC-motor. A simple schematic picture is shown in Figure 1 to show the basic principle of an H-bridge.

By turning the switches on in pairs (S1 & S4, S2 & S3) the current will flow through the motor in different directions. In extention, the direction of the motor is altered by opening the other pair of switches.

The speed is determined by the voltage over the motor. A common way to control the speed is by switching the switches fast to adjust the mean voltage over the motor.

In the physical impelementation, the switches are transistors which are controlled by a PWM signal. The duty cycle of the signal determines the time for which the transistor is on and the result is a mean voltage that is proportional to the value of the duty cycle. The H-bridge will be controlled by a microprocessor that controls PWM duty-cycle and also decides the direction in which the motor will run.

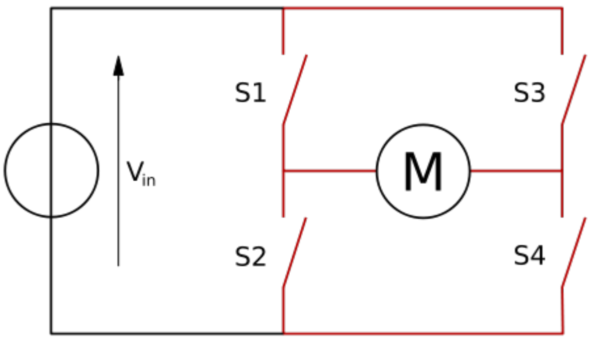

Figure 1: H-bridge principle.

3 Method

The switches used in the design is in reality MOSFETs. They must be able to handle at least 12 V 3 A, which is specified in the designs requirements. A low "on-resistance" is also desired for better efficiency.

To switch a MOSFET the gate voltage has to have a higher potential then the source voltage, the source voltage for the upper transistors in this design is 12 V, which is higher than what the microcontroller can supply, hence a MOSFET driver circuit is needed. The MOSFET driver IC HIP4081 from Intersil was chosen for this design, due to its price and functionality. This IC uses a built in charge-pump and an external boot-strap circuit to supply a high gate voltage to the upper transistors. The bootstrap technique supplies the high instantaneous current needed for turning on the power devices, while the charge pump provides enough current to "maintain" bias voltage on the upper driver sections and MOSFETs.

Shoot-through can occur when switches S1 and S2 or S3 and S4 is on at the same time, which will short-circuit the transistors. The HIP4081 has functionality to avoid shoot-through by adding a short delay to the rising edge of the PWM signal, the delay time is externally adjusted by choosing resistor values, see the datasheet for the HIP4081.

Flyback-diodes are placed in anti-parallel with the transistors to "catch" voltage spikes which could otherwise damage the transistors. These voltage spikes occur when current over the motor is changed rapidly (since a motor is an inductive load V =L*di/dt). Schottky diodes are used for this application because of its low forward breakdown voltage and fast reverse voltage recovery time. The diodes choosen are rated for for 5 A 40 V, so that if another motor was to be run an upgrade of the components would not be needed.

Two inputs will be needed from the microcontroller to set speed and direction. Five NAND-gates are used in this application to implement the logic for switching the transistors. A logic table showing how the logical circuity operates is shown in Table 1. As can be seen in the table both the lower transistors will be open then the upper one is closed, this is to implement regenerative current circulation which will further protect the transistors from voltage spikes.

A simple enable-circuit was also implemented to make sure that "shoot-through" does not occur when power is applied. When the circuit is powered on it sends a logic one signal to the MOSFET drivers disable pin. This willl make the MOSFET driver disable both the upper MOSFETS making it impossible for "shoot-through" to occur. The disable pin will then have to

Table 1: Logic table.

Dir	**PWM**	**S1**	**S2**	**S3**	**S4**
0	0	0	1	0	1
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	1	1	0

be set to a logic zero for the circuit to start operating.

A schematic for the design was created using Altium Designer 6 and is shown in Figure 2.

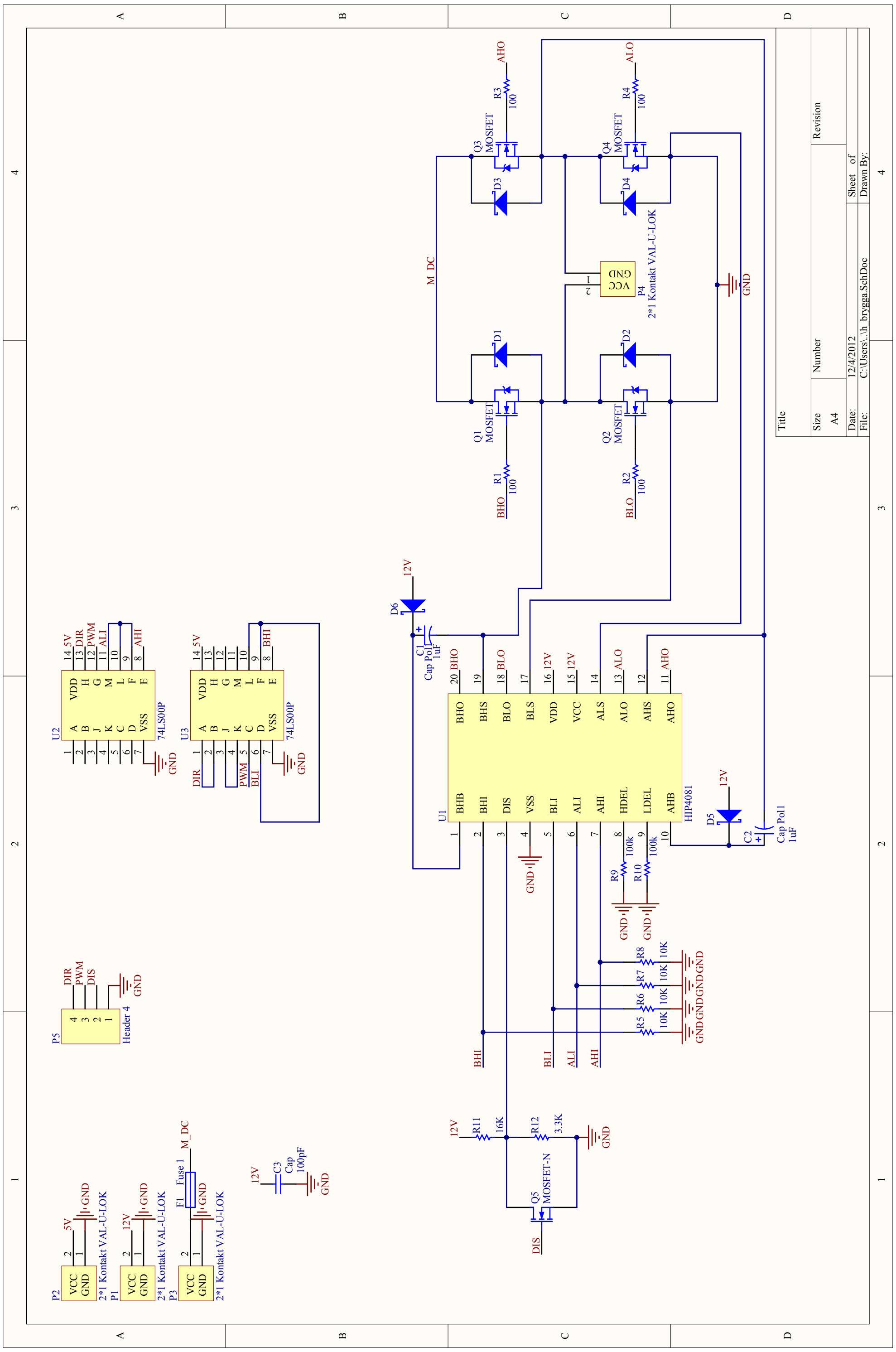

Figure 2: Schematic.

The HIP4081 pinout configuration encourages a tight layout by placing the gate drive output terminals along the right side of the chip while the input signals is on the left. This provides for short gate and source return leads connecting the IC with the power MOSFETs. The series inductance in the gate driver loop is minimized by running the gate leads to the MOSFETs almost on top of the source return leads of the MOSFET. The PC board separates the traces and provides a small amount of capacitance as well as reducing the loop inductance by reducing the encircled area of the gate drive loop. The PCB-layout was also created using Altium Designer 6, the result is shown in Figure 3.

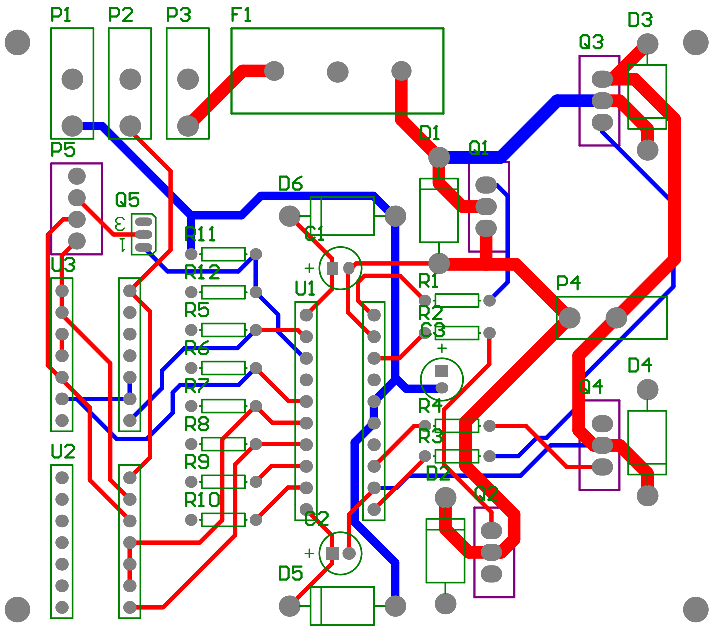

Figure 3: PCB-layout.

A prototype PCB was created in the campus PCB laboratory to verify the design, the design proved to be good with some minor changes to hole sizes and pin spacing. Once the verification was done, a PCB was ordered from a british company, which manufactures user specified PCBs in China.

4 Tests

The tests on the H-bridge circuit was performed twice with different loads. The first load was a simple 50 Ω resistor and the second load was a DC-motor. During all tests the signal was observed on an oscilloscope in order to check the its quality.

To examine the power consumption and efficiency of the circuit, the power consumed by the circuit was measured at different PWM frequencies using a duty cycle of 50 %.

To further test the efficiency of the circuit a second test was performed were the PWM frequency was held constant at 10 kHz while the duty cycle varied. The frequency of 10 kHz was chosen since it had proved to provide a high efficiency during the first test. A similar test with the motor as load and 20 kHz was also conducted.

Given the results of the two former PWM tests, the frequency with the peak efficiency is compared with 10 kHz and the 20 kHz measurements to see how high frequency PWMs works at different duty cycles.

5 Results

The power consumption at different PWM frequencies with a motor as load with 50 % duty cycle is presented in Table 2.

Table 2: Efficiency at PWM frequencies, 50 % duty cycle with a motor as load.

Frequency [kHz]	Effect PSU [W]	Effect Motor [W]	Efficiency
2	2,41	1,10	45,63%
3	2,03	1,10	54,48%
4	1,87	1,10	59,02%
5	1,79	1,10	61,59%
6	1,79	1,10	61,59%
7	1,79	1,10	61,67%
8	1,87	1,14	60,98%
9	1,87	1,14	60,98%
10	1,95	1,18	60,65%
20	2,33	1,13	48,77%
30	2,62	0,98	37,19%
40	3,07	0,97	31,57%
50	3,52	0,96	27,34%
60	3,96	0,95	24,11%
70	4,39	0,95	21,73%
80	4,84	0,95	19,61%
90	5,27	0,94	17,91%

The power consumption at different duty cycles with a PWM frequency at 20 kHz with a motor as load is presented in Table 3.

Table 3: Efficiency at 20 kHz with a motor as a load.

Duty cycle	Effect PSU [W]	Effect Motor [W]	Efficiency
20%	1,71	0,63	36,86%
30%	2,56	1,43	56,06%
40%	3,94	2,68	67,96%
50%	5,86	4,38	74,83%
60%	8,60	6,78	78,84%
70%	11,84	9,55	80,68%
80%	15,79	13,03	82,53%
100%	24,58	21,81	88,72%

The power consumption at different duty cycles with a PWM frequency at 10 kHz with a motor as load is presented in Table 4.

Table 4: Efficiency at 10 kHz with a motor as load.

Duty cycle	Effect PSU [W]	Effect Motor [W]	Efficiency
20%	1,01	0,35	34,93%
30%	1,32	0,56	42,45%
40%	1,55	0,75	48,49%
50%	1,86	0,98	52,77%
60%	2,09	1,23	58,71%
70%	2,25	1,49	66,15%
80%	2,48	1,76	71,19%
100%	2,48	2,45	98,71%

The power consumption at different duty cycles with a PWM frequency at 7 kHz with a motor as load is presented in Table 5.

Table 5: Efficiency at 7 kHz with a motor as load.

Duty cycle	Effect PSU [W]	Effect Motor [W]	Efficiency
20%	0,94	0,42	44,52%
30%	1,25	0,66	52,52%
40%	1,64	0,90	54,95%
50%	1,87	1,21	64,87%
60%	2,18	1,51	69,14%
70%	2,49	1,87	75,07%
80%	2,65	2,14	80,84%
100%	2,88	2,85	98,84%

The power consumption at different PWM frequencies with a 50 Ω resistor as a load with 50 % duty cycle is presented in Table 6.

Table 6: Efficiency at different PWM frequencies with a resistor as load.

Frequency [kHz]	Effect PSU [W]	Effect Motor [W]	Efficiency
2	0,78	0,35	44,54%
3	0,78	0,39	49,55%
4	0,86	0,39	45,05%
5	0,94	0,39	41,19%
6	0,94	0,35	37,12%
7	1,01	0,35	34,26%
8	1,01	0,35	34,30%
9	1,09	0,35	31,77%
10	1,09	0,35	31,77%
20	1,63	0,34	21,18%
30	2,16	0,34	15,84%
40	2,61	0,34	13,03%
50	3,13	0,34	10,77%
60	3,50	0,33	9,56%
70	4,09	0,33	8,17%
80	4,46	0,33	7,47%
90	5,11	0,33	6,45%

The power consumption at different duty cycles with a PWM frequency at 10 kHz with a 50 Ω resistor as a load is presented in Table 7.

Table 7: Efficiency at 10 kHz with a resistor as load.

Duty cycle	Effect PSU [W]	Effect Motor [W]	Efficiency
20%	1,32	0,15	11,14%
30%	1,71	0,36	20,90%
40%	2,17	0,63	28,94%
50%	2,63	0,97	36,95%
60%	3,01	1,44	47,66%
70%	3,47	1,99	57,32%
80%	3,86	2,58	66,81%
100%	4,25	4,08	96,02%

The relationship between efficiency and PWM frequency given in Table 2 and 6 is non linear and can be seen in Figure 4

As stated in Section 4, a duty cycle test for the frequency with the peak the peak efficiency was conducted. The result is depicted in 5.

The mounted circuit is depicted in Figure 6.

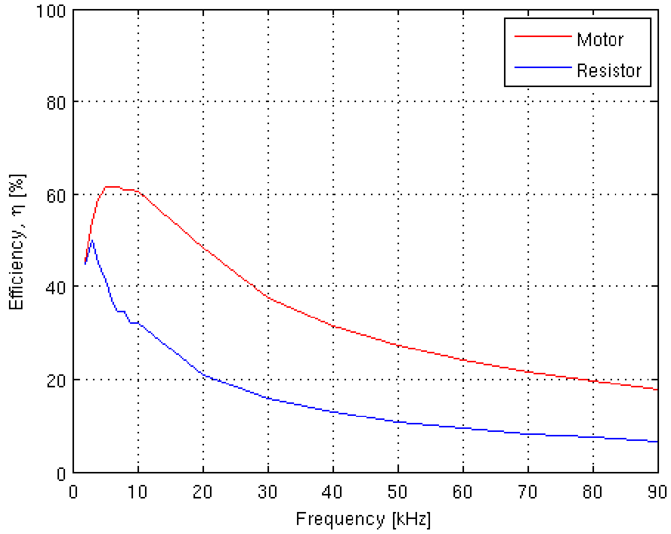

Figure 4: Efficiency for different frequencies when and different loads at a duty cycle of 50 %.

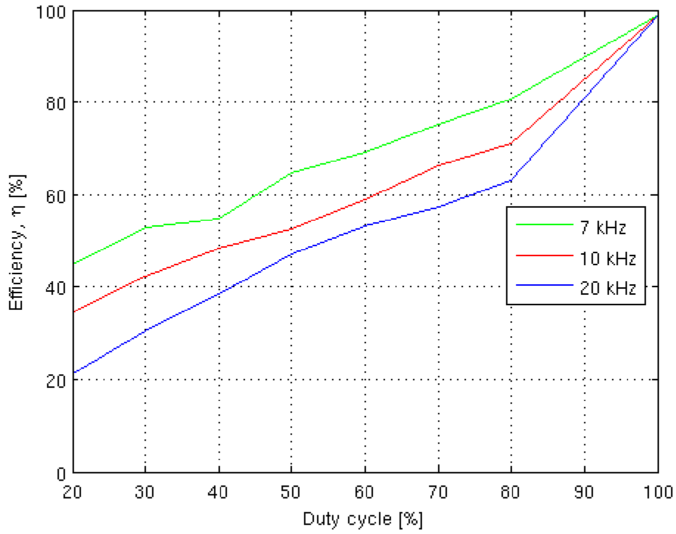

Figure 5: Efficiency for different duty cycles at different frequencies when the load is a motor.

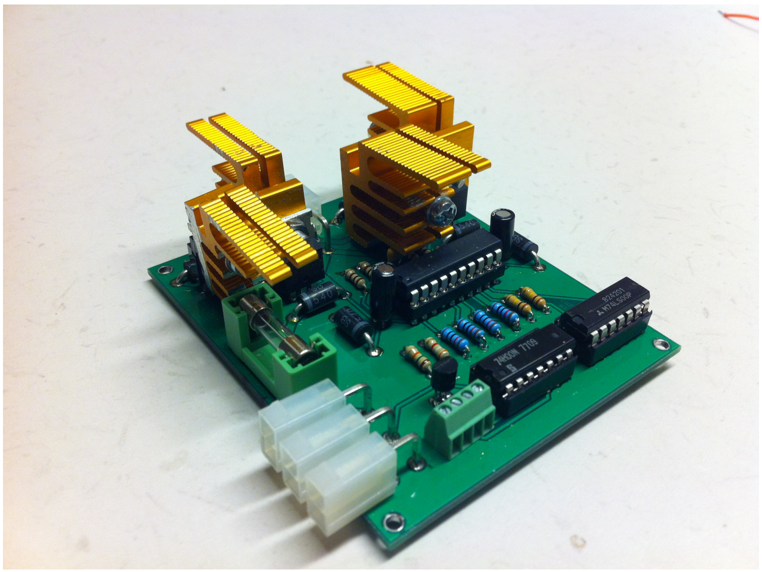

Figure 6: The mounted H-bridge.

6 Discussion

A trade-off between efficiency and signal quality has to be made to decide what the best PWM-frequency for this application is. 7 kHz was chosen as PWM-frequency due to its low power consumption and still maintaining a good signal quality.

7 Conclusion

A H-bridge will have some EMC emissions since there are signals with different frequencies present. There are however some steps that can be performed to reduce these emissions such as reducing the loop areas for these signals.

A higher PWM-frequency with a DC-motor as load results in a lower efficiency. The quality of the signal seems to remain the same.

8 Appendix

8.1 Reference list

www.intersil.com - Datasheet for HIP4081

8.2 Abbreviations

EMC	-	Electromagnetic compatibility
IC	-	Integrated circuit
MOSFET	-	Metal–oxide–semiconductor field-effect transistor
PCB	-	Printed Circuit Board
PWM	-	Pulse Width Modulation

8.3 Bill of materials

Table 8: Bill of materials

Component	**Information**	**Qty**	**Schematic notation**
MOSFET driver	HIP4081AIPZ	1	U1
Schottky diode	SB340	6	D1-D5
Power MOSFET	IRF3205PBF	4	Q1-Q4
Small signal transistor	2N3906	1	Q5
Resistor	100 kΩ	2	R9, R10
Resistor	10 kΩ	4	R5-R8
Resistor	100 Ω	4	R1-R4
Resistor	16 kΩ	1	R11
Resistor	3.3 kΩ	1	R12
Quad 2-input NAND	7400	2	U2, U3
Electrolytic capacitor	1 uF	2	C1, C2
Ceramic capacitor	1 uF	1	C3
Male Connector 90°	2 p	4	P1-P4
PCB Terminal Block 4p	4 p	1	P5
Fuse holder	6.7 A	1	F1

8.4 Contribution

Daniel - Project manager, testing, report.
Viktor - Design, schematic, PCB-layout, report, soldering, testing.
Rickard - Manufacturing of the PCB, report, testing.