1. Description

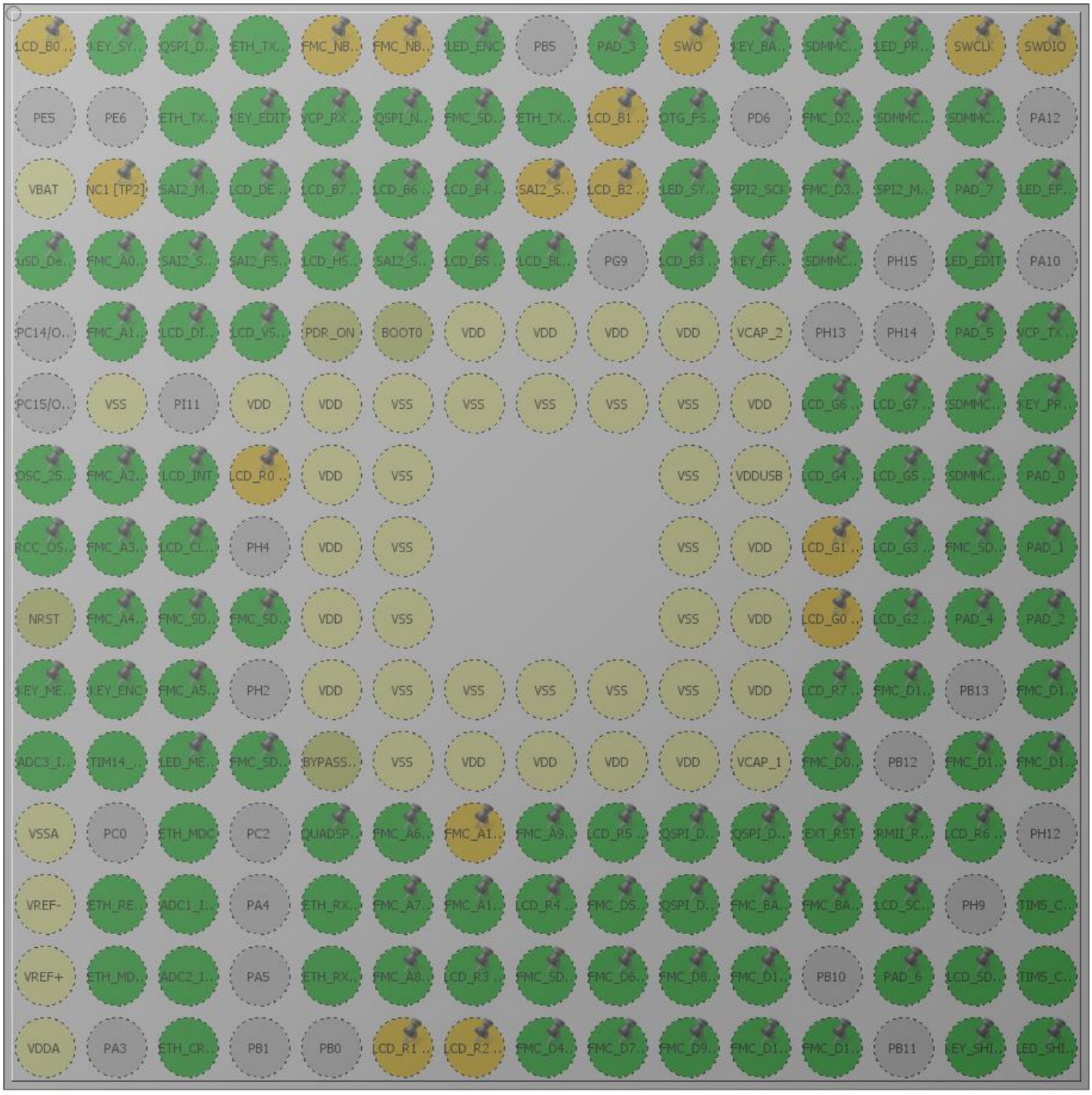
1.1. Project

Project Name	F7
Board Name	STM32F746G-DISCO
Generated with:	STM32CubeMX 4.22.0
Date	11/23/2022

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F746NGHx
MCU Package	TFBGA216
MCU Pin number	216

2. Pinout Configuration



STM32F746NGHx
TFBGA216 (Top view)

3. Pins Configuration

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	PE4 *	I/O	LTDC_B0	LCD_B0 [RK043FN48H-CT672B_B0]
A2	PE3 **	I/O	GPIO_Input	KEY_SYNC_OUT
A3	PE2	I/O	QUADSPI_BK1_IO2	QSPI_D2 [N25Q128A13EF840E_DQ2]
A4	PG14	I/O	ETH_TXD1	
A5	PE1 *	I/O	FMC_NBL1	FMC_NBL1 [MT48LC4M32B2B5-6A_DQM1]
A6	PE0 *	I/O	FMC_NBL0	FMC_NBL0 [MT48LC4M32B2B5-6A_DQM0]
A7	PB8 **	I/O	GPIO_Output	LED_ENC
A9	PB4 **	I/O	GPIO_Input	PAD_3
A10	PB3 *	I/O	SYS_JTDO-SWO	SWO
A11	PD7 **	I/O	GPIO_Input	KEY_BACK
A12	PC12	I/O	SDMMC1_CK	SDMMC_CK
A13	PA15 **	I/O	GPIO_Output	LED_PRESET
A14	PA14 *	I/O	SYS_JTCK-SWCLK	SWCLK
A15	PA13 *	I/O	SYS_JTMS-SWDIO	SWDIO
B3	PG13	I/O	ETH_TXD0	
B4	PB9 **	I/O	GPIO_Input	KEY_EDIT
B5	PB7	I/O	USART1_RX	VCP_RX [STM32F103CBT6_PA2]
B6	PB6	I/O	QUADSPI_BK1_NCS	QSPI_NCS [N25Q128A13EF840E_S]
B7	PG15	I/O	FMC_SDNCAS	FMC_SDNCAS [MT48LC4M32B2B5-6A_CAS]
B8	PG11	I/O	ETH_TX_EN	
B9	PJ13 *	I/O	LTDC_B1	LCD_B1 [RK043FN48H-CT672B_B1]
B10	PJ12 **	I/O	GPIO_Input	OTG_FS_VBUS
B12	PD0	I/O	FMC_D2	FMC_D2 [MT48LC4M32B2B5-6A_DQ2]
B13	PC11	I/O	SDMMC1_D3	SDMMC_D3

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
B14	PC10	I/O	SDMMC1_D2	SDMMC_D2
C1	VBAT	Power		
C2	PI8 *	I/O	RTC_TS	NC1 [TP2]
C3	PI4	I/O	SAI2_MCLK_A	SAI2_MCLKA [WM8994ECS/R_MCLK1]
C4	PK7	I/O	LTDC_DE	LCD_DE [RK043FN48H-CT672B_DE]
C5	PK6	I/O	LTDC_B7	LCD_B7 [RK043FN48H-CT672B_B7]
C6	PK5	I/O	LTDC_B6	LCD_B6 [RK043FN48H-CT672B_B6]
C7	PG12	I/O	LTDC_B4	LCD_B4 [RK043FN48H-CT672B_B4]
C8	PG10 *	I/O	SAI2_SD_B	SAI2_SDB [WM8994ECS/R_ADCDAT1]
C9	PJ14 *	I/O	LTDC_B2	LCD_B2 [RK043FN48H-CT672B_B2]
C10	PD5 **	I/O	GPIO_Output	LED_SYNC_OUT
C11	PD3	I/O	SPI2_SCK	
C12	PD1	I/O	FMC_D3	FMC_D3 [MT48LC4M32B2B5-6A_DQ3]
C13	PI3	I/O	SPI2_MOSI	
C14	PI2 **	I/O	GPIO_Input	PAD_7
C15	PA11 **	I/O	GPIO_Output	LED_EFFECT
D1	PC13 **	I/O	GPIO_Input	uSD_Detect
D2	PF0	I/O	FMC_A0	FMC_A0 [MT48LC4M32B2B5-6A_A0]
D3	PI5	I/O	SAI2_SCK_A	SAI2_SCKA [WM8994ECS/R_BCLK1]
D4	PI7	I/O	SAI2_FS_A	SAI2_FSA [WM8994ECS/R_LRCLK1]
D5	PI10	I/O	LTDC_HSYNC	LCD_HSYNC [RK043FN48H-CT672B_HSYNC]
D6	PI6	I/O	SAI2_SD_A	SAI2_SDA [WM8994ECS/R_DACDAT1]
D7	PK4	I/O	LTDC_B5	LCD_B5 [RK043FN48H-CT672B_B5]
D8	PK3 **	I/O	GPIO_Output	LCD_BL_CTRL [STLD40DPUR_EN]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
D10	PJ15	I/O	LTDC_B3	LCD_B3 [RK043FN48H-CT672B_B3]
D11	PD4 **	I/O	GPIO_Input	KEY_EFFECT
D12	PD2	I/O	SDMMC1_CMD	SDMMC_D0
D14	PI1 **	I/O	GPIO_Output	LED_EDIT
E2	PF1	I/O	FMC_A1	FMC_A1 [MT48LC4M32B2B5-6A_A1]
E3	PI12 **	I/O	GPIO_Output	LCD_DISP [RK043FN48H-CT672B_DISP]
E4	PI9	I/O	LTDC_VSYNC	LCD_VSYNC [RK043FN48H-CT672B_VSYNC]
E5	PDR_ON	Reset		
E6	BOOT0	Boot		
E7	VDD	Power		
E8	VDD	Power		
E9	VDD	Power		
E10	VDD	Power		
E11	VCAP_2	Power		
E14	PI0 **	I/O	GPIO_Input	PAD_5
E15	PA9	I/O	USART1_TX	VCP_TX [STM32F103CBT6_PA3]
F2	VSS	Power		
F4	VDD	Power		
F5	VDD	Power		
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F11	VDD	Power		
F12	PK1	I/O	LTDC_G6	LCD_G6 [RK043FN48H-CT672B_G6]
F13	PK2	I/O	LTDC_G7	LCD_G7 [RK043FN48H-CT672B_G7]
F14	PC9	I/O	SDMMC1_D1	
F15	PA8 **	I/O	GPIO_Input	KEY_PRESET
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	OSC_25M [NZ2520SB-25.00M_OUT]
G2	PF2	I/O	FMC_A2	FMC_A2 [MT48LC4M32B2B5-6A_A2]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
G3	PI13	I/O	GPIO_EXTI13	LCD_INT
G4	PI15 *	I/O	LTDC_R0	LCD_R0 [RK043FN48H-CT672B_R0]
G5	VDD	Power		
G6	VSS	Power		
G10	VSS	Power		
G11	VDDUSB	Power		
G12	PJ11	I/O	LTDC_G4	LCD_G4 [RK043FN48H-CT672B_G4]
G13	PK0	I/O	LTDC_G5	LCD_G5 [RK043FN48H-CT672B_G5]
G14	PC8	I/O	SDMMC1_D0	
G15	PC7 **	I/O	GPIO_Input	PAD_0
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H2	PF3	I/O	FMC_A3	FMC_A3 [MT48LC4M32B2B5-6A_A3]
H3	PI14	I/O	LTDC_CLK	LCD_CLK [RK043FN48H-CT672B_CLK]
H5	VDD	Power		
H6	VSS	Power		
H10	VSS	Power		
H11	VDD	Power		
H12	PJ8 *	I/O	LTDC_G1	LCD_G1 [RK043FN48H-CT672B_G1]
H13	PJ10	I/O	LTDC_G3	LCD_G3 [RK043FN48H-CT672B_G3]
H14	PG8	I/O	FMC_SDCLK	FMC_SDCLK [MT48LC4M32B2B5-6A_CLK]
H15	PC6 **	I/O	GPIO_Input	PAD_1
J1	NRST	Reset		
J2	PF4	I/O	FMC_A4	FMC_A4 [MT48LC4M32B2B5-6A_A4]
J3	PH5	I/O	FMC_SDNWE	FMC_SDNME [MT48LC4M32B2B5-6A_WE]
J4	PH3	I/O	FMC_SDNE0	FMC_SDNE0 [MT48LC4M32B2B5-6A_CS]
J5	VDD	Power		
J6	VSS	Power		
J10	VSS	Power		

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J11	VDD	Power		
J12	PJ7 *	I/O	LTDC_G0	LCD_G0 [RK043FN48H-CT672B_G0]
J13	PJ9	I/O	LTDC_G2	LCD_G2 [RK043FN48H-CT672B_G2]
J14	PG7 **	I/O	GPIO_Input	PAD_4
J15	PG6 **	I/O	GPIO_Input	PAD_2
K1	PF7 **	I/O	GPIO_Input	KEY_MENU
K2	PF6 **	I/O	GPIO_Input	KEY_ENC
K3	PF5	I/O	FMC_A5	FMC_A5 [MT48LC4M32B2B5-6A_A5]
K5	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K11	VDD	Power		
K12	PJ6	I/O	LTDC_R7	LCD_R7 [RK043FN48H-CT672B_R7]
K13	PD15	I/O	FMC_D1	FMC_D1 [MT48LC4M32B2B5-6A_DQ1]
K15	PD10	I/O	FMC_D15	FMC_D15 [MT48LC4M32B2B5-6A_DQ15]
L1	PF10	I/O	ADC3_IN8	
L2	PF9	I/O	TIM14_CH1	
L3	PF8 **	I/O	GPIO_Output	LED_MENU
L4	PC3	I/O	FMC_SDCKE0	FMC_SDCKE0 [MT48LC4M32B2B5-6A_CKE]
L5	BYPASS_REG	Reset		
L6	VSS	Power		
L7	VDD	Power		
L8	VDD	Power		
L9	VDD	Power		
L10	VDD	Power		
L11	VCAP_1	Power		
L12	PD14	I/O	FMC_D0	FMC_D0 [MT48LC4M32B2B5-6A_DQ0]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L14	PD9	I/O	FMC_D14	FMC_D14 [MT48LC4M32B2B5-6A_DQ14]
L15	PD8	I/O	FMC_D13	FMC_D13 [MT48LC4M32B2B5-6A_DQ13]
M1	VSSA	Power		
M3	PC1	I/O	ETH_MDC	
M5	PB2	I/O	QUADSPI_CLK	
M6	PF12	I/O	FMC_A6	FMC_A6 [MT48LC4M32B2B5-6A_A6]
M7	PG1 *	I/O	FMC_A11	FMC_A11 [MT48LC4M32B2B5-6A_A11]
M8	PF15	I/O	FMC_A9	FMC_A9 [MT48LC4M32B2B5-6A_A9]
M9	PJ4	I/O	LTDC_R5	LCD_R5 [RK043FN48H-CT672B_R5]
M10	PD12	I/O	QUADSPI_BK1_IO1	QSPI_D1 [N25Q128A13EF840E_DQ1]
M11	PD13	I/O	QUADSPI_BK1_IO3	QSPI_D3 [N25Q128A13EF840E_DQ3]
M12	PG3 **	I/O	GPIO_Output	EXT_RST
M13	PG2 **	I/O	GPIO_Input	RMII_RXER
M14	PJ5	I/O	LTDC_R6	LCD_R6 [RK043FN48H-CT672B_R6]
N1	VREF-	Power		
N2	PA1	I/O	ETH_REF_CLK	
N3	PA0/WKUP	I/O	ADC1_IN0	
N5	PC4	I/O	ETH_RXD0	
N6	PF13	I/O	FMC_A7	FMC_A7 [MT48LC4M32B2B5-6A_A7]
N7	PG0	I/O	FMC_A10	FMC_A10 [MT48LC4M32B2B5-6A_A10]
N8	PJ3	I/O	LTDC_R4	LCD_R4 [RK043FN48H-CT672B_R4]
N9	PE8	I/O	FMC_D5	FMC_D5 [MT48LC4M32B2B5-6A_DQ5]

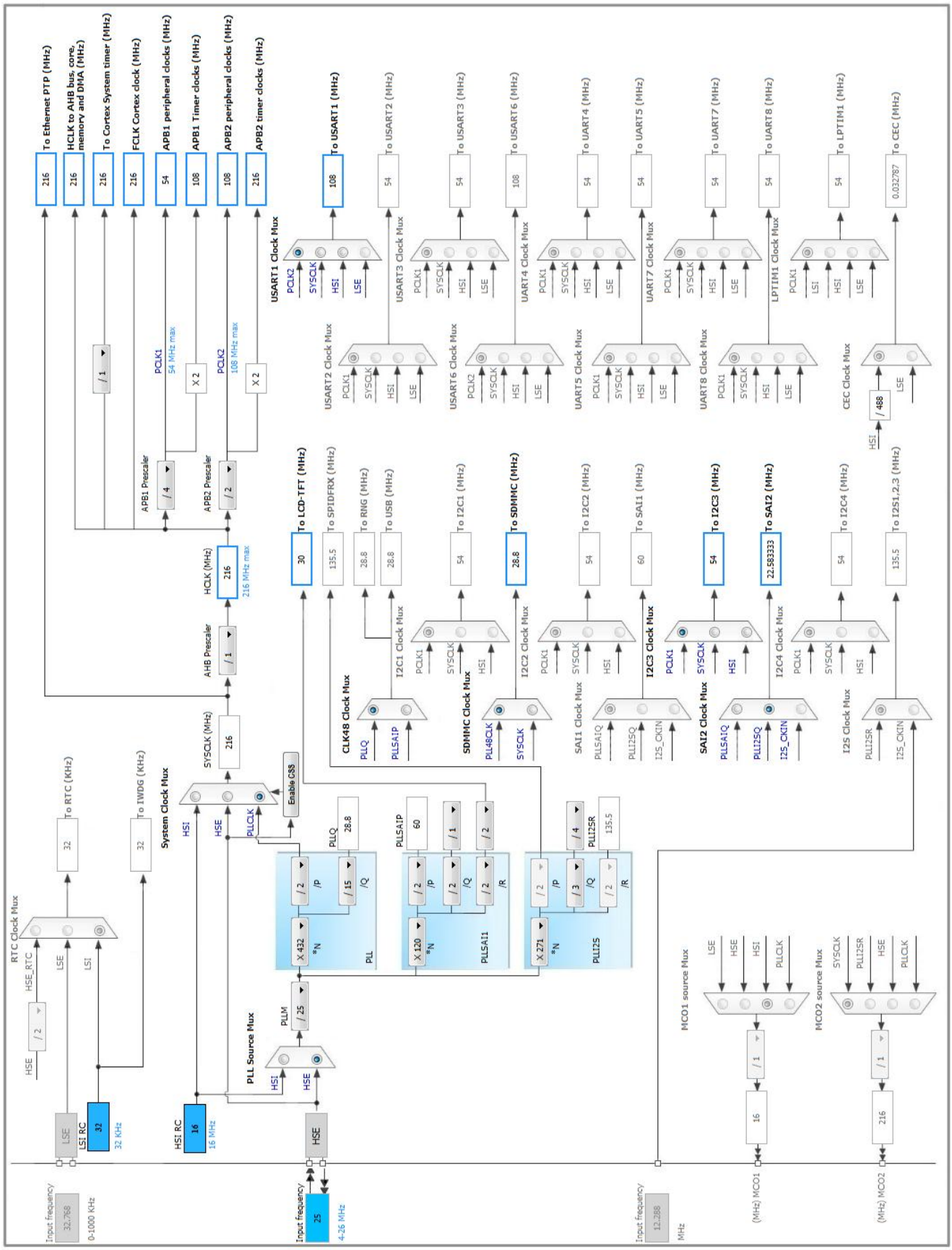
Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N10	PD11	I/O	QUADSPI_BK1_IO0	QSPI_D0 [N25Q128A13EF840E_DQ0]
N11	PG5	I/O	FMC_BA1	FMC_BA1 [MT48LC4M32B2B5-6A_BA1]
N12	PG4	I/O	FMC_BA0	FMC_BA0 [MT48LC4M32B2B5-6A_BA0]
N13	PH7	I/O	I2C3_SCL	LCD_SCL [RK043FN48H-CT672B_SCL]
N15	PH11	I/O	TIM5_CH2	
P1	VREF+	Power		
P2	PA2	I/O	ETH_MDIO	
P3	PA6	I/O	ADC2_IN6	
P5	PC5	I/O	ETH_RXD1	
P6	PF14	I/O	FMC_A8	FMC_A8 [MT48LC4M32B2B5-6A_A8]
P7	PJ2	I/O	LTDC_R3	LCD_R3 [RK043FN48H-CT672B_R3]
P8	PF11	I/O	FMC_SDNRAS	FMC_SDNRAS [MT48LC4M32B2B5-6A_RAS]
P9	PE9	I/O	FMC_D6	FMC_D6 [MT48LC4M32B2B5-6A_DQ6]
P10	PE11	I/O	FMC_D8	FMC_D8 [MT48LC4M32B2B5-6A_DQ8]
P11	PE14	I/O	FMC_D11	FMC_D11 [MT48LC4M32B2B5-6A_DQ11]
P13	PH6 **	I/O	GPIO_Input	PAD_6
P14	PH8	I/O	I2C3_SDA	LCD_SDA [RK043FN48H-CT672B_SDA]
P15	PH10	I/O	TIM5_CH1	
R1	VDDA	Power		
R3	PA7	I/O	ETH_CRS_DV	
R6	PJ0 *	I/O	LTDC_R1	LCD_R1 [RK043FN48H-CT672B_R1]
R7	PJ1 *	I/O	LTDC_R2	LCD_R2 [RK043FN48H-CT672B_R2]

Pin Number TFBGA216	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R8	PE7	I/O	FMC_D4	FMC_D4 [MT48LC4M32B2B5-6A_DQ4]
R9	PE10	I/O	FMC_D7	FMC_D7 [MT48LC4M32B2B5-6A_DQ7]
R10	PE12	I/O	FMC_D9	FMC_D9 [MT48LC4M32B2B5-6A_DQ9]
R11	PE15	I/O	FMC_D12	FMC_D12 [MT48LC4M32B2B5-6A_DQ12]
R12	PE13	I/O	FMC_D10	FMC_D10 [MT48LC4M32B2B5-6A_DQ10]
R14	PB14 **	I/O	GPIO_Input	KEY_SHIFT
R15	PB15 **	I/O	GPIO_Output	LED_SHIFT

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN6

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 6
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. ADC3

mode: IN8

5.3.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 8
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.4. DMA2D

mode: Activated

5.4.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	ARGB8888
Output Offset	0

Foreground layer Configuration:

DMA2D Input Color Mode	ARGB8888
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)

5.5. ETH

Mode: RMII

5.5.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address

	EE:81:EA:AA:DD:F1 *
PHY Address	**0 ***

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

5.5.2. Advanced Parameters:

External PHY Configuration:

PHY	LAN8742A_PHY_ADDRESS
PHY Address Value	0
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x10 ***
PHY Speed mask	**0x0002 ***
PHY Duplex mask	**0x0004 ***
PHY Interrupt Source Flag register Offset	**0x000B ***

PHY Link down inturrupt	**0x000B ***

5.6. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 11 bits

Data: 16 bits

5.6.1. SDRAM 1:

SDRAM control:	
Bank	SDRAM bank 1
Number of column address bits	8 bits
Number of row address bits	11 bits
CAS latency	**2 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	Disabled
SDRAM common burst read	**Enabled ***
SDRAM common read pipe delay	0 HCLK clock cycle
SDRAM timing in memory clock cycles:	
Load mode register to active delay	**2 ***
Exit self-refresh delay	**6 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**6 ***
Write recovery time	**2 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

5.7. I2C3

I2C: I2C

5.7.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.8. LTDC

Display Type: RGB565 (16 bits)

5.8.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**41 ***
Horizontal Back Porch	**13 ***
Active Width	**480 ***
Horizontal Front Porch	**32 ***
HSync Width	40
Accumulated Horizontal Back Porch Width	53
Accumulated Active Width	533
Total Width	565

Synchronization for Height:

Vertical Synchronization Height	**10 ***
Vertical Back Porch	2
Active Height	**272 ***
Vertical Front Porch	2
VSync Height	9
Accumulated Vertical Back Porch Height	11
Accumulated Active Height	283

Total Height	285

Signal Polarity:

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

5.8.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**480 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**272 ***
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	**480 ***
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	**272 ***

Pixel Parameters:

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Default Alpha value	0
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	**255 ***
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	Alpha constant

Layer 1 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Adress	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

Number of Layers:

Number of Layers	2 layers

5.9. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

5.9.1. Parameter Settings:

General Parameters:

Clock Prescaler	**1 ***
Fifo Threshold	**4 ***
Sample Shifting	**Sample Shifting Half Cycle ***
Flash Size	**23 ***
Chip Select High Time	**2 Cycles ***
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

5.10. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.10.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3

Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.11. SAI2

Mode: Master with Master Clock Out

5.11.1. Parameter Settings:

SAI A:

Basic Parameters	
Protocol	Free
Audio Mode	Master Transmit
Frame Length	**64 bits ***
Data Size	**16 Bits ***
Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Frame Parameters	
First Bit	MSB First
Frame Synchro Active Level Length	**32 ***
Frame Synchro Definition	**Channel Identification ***
Frame Synchro Polarity	Active Low
Frame Synchro Offset	**Before First Bit ***
Slot Parameters	
First Bit Offset	0
Number of Slots (only Even Values)	2
Slot Active Final Value	**0x00000003 ***
Slot Active	**User Setting ***
Slot 0 Active	**true ***
Slot 1 Active	**true ***

Clock Parameters	
Master Clock Divider	Enabled
Audio Frequency	**44.1 KHz ***
Real Audio Frequency	**44.108 KHz ***
Error between Selected	**-8.1 % ***
Clock Strobing	**Rising Edge ***
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	**Enabled ***
Synchronization External	Disabled

5.12. SDMMC1

Mode: SD 4 bits Wide bus

5.12.1. Parameter Settings:

SDMMC parameters:

SDMMCCLK clock divide factor	**12 ***

5.13. SPI2

Mode: Transmit Only Master

5.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**3.375 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled

NSSP Mode	**Disabled ***
NSS Signal Type	Software

5.14. SYS

Timebase Source: SysTick

5.15. TIM2

Clock Source : Internal Clock

5.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**21599 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**4 ***
Internal Clock Division (CKD)	**Division by 2 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	**Update Event ***

5.16. TIM5

Combined Channels: Encoder Mode

5.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**4 ***

5.17. TIM14

mode: Activated

Channel1: PWM Generation CH1

5.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**24 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**255 ***
Internal Clock Division (CKD)	**Division by 4 ***
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**200 ***
Fast Mode	Disable
CH Polarity	High

5.18. USART1

Mode: Asynchronous

5.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**8 Bits (including Parity) ***
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.19. FATFS

mode: SD Card

5.19.1. Set Defines:

Version:

FATFS version	R0.11

Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Multilingual Latin 1 (OEM)
USE_LFN (Use Long Filename)	**Enabled with static working buffer on the BSS ***

MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	**4096 ***
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
WORD_ACCESS (Platform dependent access option)	Byte access
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

5.19.2. IPs instances:

SDIO/SDMMC:

SDMMC instance	SDMMC1

5.20. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

5.20.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.0.0

IPv4 - DHCP Option:

LWIP_DHCP (DHCP Module)	**Disabled ***

IP Address Settings:

IP_ADDRESS (IP Address)	**169.254.040.241 ***
NETMASK_ADDRESS (Netmask Address)	**255.255.000.000 ***
GATEWAY_ADDRESS (Gateway Address)	**169.254.001.001 ***

RTOS Settings:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Disabled

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	**5 ***
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

5.20.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Not Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144

TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Disabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Disabled

5.20.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

5.20.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

5.20.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

5.20.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

5.20.7. SNTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

5.20.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

5.20.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

5.20.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

5.20.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Disabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

5.20.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0/WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA6	ADC2_IN6	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PF10	ADC3_IN8	Analog mode	No pull-up and no pull-down	n/a	
ETH	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PG11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
FMC	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNCAS [MT48LC4M32B2B5-6A_CAS]
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D2 [MT48LC4M32B2B5-6A_DQ2]
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D3 [MT48LC4M32B2B5-6A_DQ3]
	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A0 [MT48LC4M32B2B5-6A_A0]
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						[MT48LC4M32B2B5-6A_A1]
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A2 [MT48LC4M32B2B5-6A_A2]
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A3 [MT48LC4M32B2B5-6A_A3]
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDCLK [MT48LC4M32B2B5-6A_CLK]
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A4 [MT48LC4M32B2B5-6A_A4]
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNME [MT48LC4M32B2B5-6A_WE]
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNE0 [MT48LC4M32B2B5-6A_CS]
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A5 [MT48LC4M32B2B5-6A_A5]
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D1 [MT48LC4M32B2B5-6A_DQ1]
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D15 [MT48LC4M32B2B5-6A_DQ15]
	PC3	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDCKE0 [MT48LC4M32B2B5-6A_CKE]
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D0 [MT48LC4M32B2B5-6A_DQ0]
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D14 [MT48LC4M32B2B5-6A_DQ14]
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D13 [MT48LC4M32B2B5-6A_DQ13]
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A6 [MT48LC4M32B2B5-6A_A6]
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A9 [MT48LC4M32B2B5-6A_A9]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A7 [MT48LC4M32B2B5-6A_A7]
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A10 [MT48LC4M32B2B5-6A_A10]
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D5 [MT48LC4M32B2B5-6A_DQ5]
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_BA1 [MT48LC4M32B2B5-6A_BA1]
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_BA0 [MT48LC4M32B2B5-6A_BA0]
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A8 [MT48LC4M32B2B5-6A_A8]
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_SDNRAS [MT48LC4M32B2B5-6A_RAS]
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D6 [MT48LC4M32B2B5-6A_DQ6]
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D8 [MT48LC4M32B2B5-6A_DQ8]
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D11 [MT48LC4M32B2B5-6A_DQ11]
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D4 [MT48LC4M32B2B5-6A_DQ4]
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D7 [MT48LC4M32B2B5-6A_DQ7]
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D9 [MT48LC4M32B2B5-6A_DQ9]
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D12 [MT48LC4M32B2B5-6A_DQ12]
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_D10 [MT48LC4M32B2B5-6A_DQ10]
I2C3	PH7	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High**	LCD_SCL [RK043FN48H-CT672B_SCL]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PH8	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	LCD_SDA [RK043FN48H-CT672B_SDA]
LTDC	PK7	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_DE [RK043FN48H-CT672B_DE]
	PK6	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B7 [RK043FN48H-CT672B_B7]
	PK5	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B6 [RK043FN48H-CT672B_B6]
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B4 [RK043FN48H-CT672B_B4]
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_HSYNC [RK043FN48H-CT672B_HSYNC]
	PK4	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B5 [RK043FN48H-CT672B_B5]
	PJ15	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B3 [RK043FN48H-CT672B_B3]
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_VSYNC [RK043FN48H-CT672B_VSYNC]
	PK1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G6 [RK043FN48H-CT672B_G6]
	PK2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G7 [RK043FN48H-CT672B_G7]
	PJ11	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G4 [RK043FN48H-CT672B_G4]
	PK0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G5 [RK043FN48H-CT672B_G5]
	PI14	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_CLK [RK043FN48H-CT672B_CLK]
	PJ10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G3 [RK043FN48H-CT672B_G3]
	PJ9	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G2 [RK043FN48H-CT672B_G2]
	PJ6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R7 [RK043FN48H-CT672B_R7]
	PJ4	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R5 [RK043FN48H-CT672B_R5]
	PJ5	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R6 [RK043FN48H-CT672B_R6]
	PJ3	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R4 [RK043FN48H-CT672B_R4]
	PJ2	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R3 [RK043FN48H-

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						CT672B_R3]
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	QSPI_D2 [N25Q128A13EF840E_DQ2]
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	QSPI_NCS [N25Q128A13EF840E_S]
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PD12	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	QSPI_D1 [N25Q128A13EF840E_DQ1]
	PD13	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	QSPI_D3 [N25Q128A13EF840E_DQ3]
	PD11	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	QSPI_D0 [N25Q128A13EF840E_DQ0]
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	OSC_25M [NZ2520SB-25.00M_OUT]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SAI2	PI4	SAI2_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_MCLKA [WM8994ECS/R_MCLK1]
	PI5	SAI2_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SCKA [WM8994ECS/R_BCLK1]
	PI7	SAI2_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_FSA [WM8994ECS/R_LRCLK1]
	PI6	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SDA [WM8994ECS/R_DACDAT1]
SDMMC1	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDMMC_CK
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDMMC_D3
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDMMC_D2
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	SDMMC_D0
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI2	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High***	
TIM5	PH11	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM14	PF9	TIM14_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART1	PB7	USART1_RX	Alternate Function Push Pull	*	Low	VCP_RX [STM32F103CBT6_PA2]
	PA9	USART1_TX	Alternate Function Push Pull	*	Low	VCP_TX [STM32F103CBT6_PA3]
Single Mapped Signals	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B0 [RK043FN48H-CT672B_B0]
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_NBL1 [MT48LC4M32B2B5-6A_DQM1]
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_NBL0 [MT48LC4M32B2B5-6A_DQM0]
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	SWO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PJ13	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B1 [RK043FN48H-CT672B_B1]
	PI8	RTC_TS	n/a	n/a	n/a	NC1 [TP2]
	PG10	SAI2_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low	SAI2_SDB [WM8994ECS/R_ADCDAT1]
	PJ14	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_B2 [RK043FN48H-CT672B_B2]
	PI15	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R0 [RK043FN48H-CT672B_R0]
	PJ8	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G1 [RK043FN48H-CT672B_G1]
	PJ7	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_G0 [RK043FN48H-CT672B_G0]
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	FMC_A11 [MT48LC4M32B2B5-6A_A11]
	PJ0	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R1 [RK043FN48H-CT672B_R1]
	PJ1	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	LCD_R2 [RK043FN48H-CT672B_R2]
GPIO	PE3	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY_SYNC_OUT
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	LED_ENC
	PB4	GPIO_Input	Input mode	**Pull-down ***	**n/a**	PAD_3
	PD7	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY_BACK
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	LED_PRESET

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB9	GPIO_Input	Input mode	**Pull-up ***	**n/a**	KEY_EDIT
	PJ12	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	OTG_FS_VBUS
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	LED_SYNC_OUT
	PI2	GPIO_Input	Input mode	**Pull-down ***	**n/a**	PAD_7
	PA11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	LED_EFFECT
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	uSD_Detect
	PK3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_BL_CTRL [STLD40DPUR_EN]
	PD4	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY_EFFECT
	PI1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	LED_EDIT
	PI12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_DISP [RK043FN48H-CT672B_DISP]
	PI0	GPIO_Input	Input mode	**Pull-down ***	n/a	PAD_5
	PA8	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY_PRESET
	PI13	GPIO_EXTI13	**External Event Mode with Rising edge trigger detection ***	No pull-up and no pull-down	n/a	LCD_INT
	PC7	GPIO_Input	Input mode	**Pull-down ***	n/a	PAD_0
	PC6	GPIO_Input	Input mode	**Pull-down ***	n/a	PAD_1
	PG7	GPIO_Input	Input mode	**Pull-down ***	n/a	PAD_4
	PG6	GPIO_Input	Input mode	**Pull-down ***	n/a	PAD_2
	PF7	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY_MENU
	PF6	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY_ENC
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	LED_MENU
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EXT_RST
	PG2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	RMII_RXER
	PH6	GPIO_Input	Input mode	**Pull-down ***	n/a	PAD_6
	PB14	GPIO_Input	Input mode	**Pull-up ***	n/a	KEY_SHIFT
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	LED_SHIFT

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI2_TX	DMA1_Stream4	Memory To Peripheral	Low

SPI2_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream4 global interrupt	true	0	0
TIM2 global interrupt	true	2	0
USART1 global interrupt	true	7	0
TIM5 global interrupt	true	3	0
SAI2 global interrupt	true	1	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
SPI2 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
FMC global interrupt	unused		
SDMMC1 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		
QUADSPI global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F746NGHx
Datasheet	027590_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	F7
Project Folder	C:\Keil_v5\Projects\Sampler
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F7 V1.7.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No