

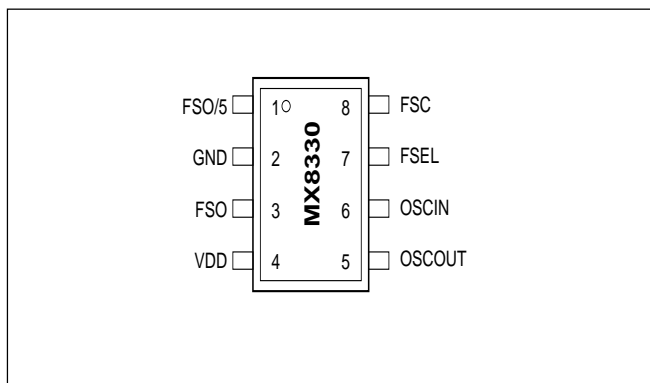
RAMBUS CLOCK GENERATOR**FEATURES**


- Clock generator for Rambus™ Channel
- Provide output frequency select pin
- Provide a Rambus interface level output frequency which is 14 or 17 times of input frequency
- Provide a TTL interface level output frequency which is input frequency divided by 4
- Provide a TTL interface level output frequency which is 14/5 or 17/5 times of input frequency
- 3.3 V power supply
- Package
8-pin SOP (150mil)

GENERAL DESCRIPTION

The product is a clock synthesizer chip for Rambus Channel. It uses advanced Phase lock loop technology to generate three desired clock. The reference clock is supplied by external crystal. The crystal frequency is 4 x 3.579545 MHz in NTSC case, and is 4 x 4.43361875 MHz in PAL case. The output clock (FSO) is 243.40906 MHz and 248.28265 MHz respectively. The FSO clock interface level has to be Rambus interface compatible. Beside FSO clock, a FSO divided by five clock output is also provided. The FSO/5 clock output is TTL compatible.

The product is 3.3 V operation, and the package type is 8-pin SOP.

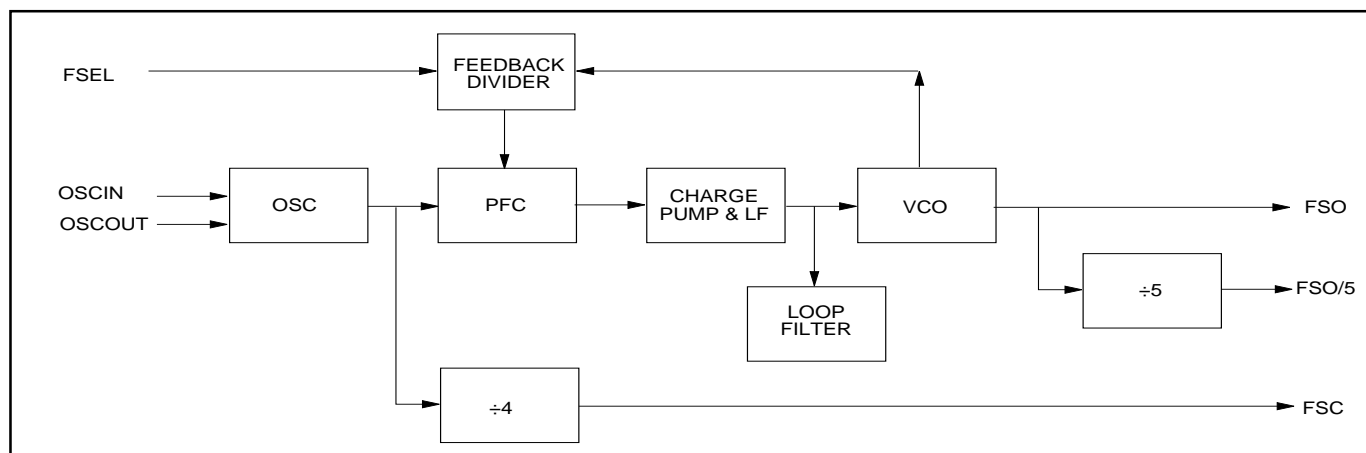
PIN CONFIGURATIONS**8-PIN SOP**

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PIN DESCRIPTION

SYMBOL	PIN TYPE	PIN NUMBER	DESCRIPTION
FSO/5	O	1	Clock output. FSO divided by 5.
GND		2	Ground
FSO	O	3	Rambus clock output. Rambus interface level.
VDD		4	Power supply
OSCOUT	O	5	Crystal pin
OSCIN	I	6	Crystal pin
FSEL	I	7	Frequency select pin(High:FSO=17*4*FSC, Low:FSO=14*4*FSC). Toggling of FSEL will reset the counter in the FEEDBACK DIVIDER.
FSC	O	8	Clock output. Crystal frequency divided by 4.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The Rambus clock generator is an integrated circuit of phase locked loop frequency synthesizer. It provides three clock output frequencies. The first output frequency (FSC) is the crystal frequency divided by 4 clock. The second output frequency (FSO) is 14 or 17 times of crystal frequency. The FSO output frequency can be selected by FSEL Pin. When FSEL pin is high, FSO is 17 times of crystal frequency. When FSEL is low, FSO is 14 times of crystal frequency. FSO is Rambus interface level output. The third output frequency is FSO divided by 5 clock output.

As shown in the block diagram, a Phase locked loop consists of feedback divider, phase frequency comparator(PFC), Charge pump, voltage controlled oscillator(VCO), and loop filter. All components for PLL are integrated inside the chip.

Note: Application notice for Rev.E of the MX8330. Because the VCO and the counter in the FEEDBACK

DIVIDER can not operate in accordance with each other in the initial stage. If the power on voltage is less than 3.3V the counter in the FEEDBACK DIVIDER must be reseted. The counter in the FEEDBACK DIVIDER can be reset by toggling the FSEL after VDD exceed 3.0V. It takes 5ms for FSO to be stable after FSEL's toggling.

FREQUENCY TABLE(in MHz) (in NTSC case)

CRYSTAL	FSEL	FSC	FSO
4*3.579545	1	3.579545	17*4*3.579545
4*3.579545	0	3.579545	14*4*3.579545

(in PAL case)

CRYSTAL	FSEL	FSC	FSO
4*4.43361875	1	4.43361875	17*4*4.43361875
4*4.43361875	0	4.43361875	14*4*4.43361875

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Storage Temperature	-85°C to 150°C
Applied Input Voltage	-0.5V to VDD + 0.5V
Applied Output Voltage	-0.5V to VDD + 0.5V
Supply Voltage	-0.5V to 5V
Operating Temperature	0 to 70°C
Power Dissipation	0.5Watts

NOTICE:

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:

Specifications contained within the following tables are subject to change.

DC CHARACTERISTICS TA = 0°C to 80°C, VDD = 3.15V to 3.6V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VIL	Input Low Voltage			0.8	V	
VIH	Input High Voltage	2.4			V	
IIL	Input Low Current			-5	uA	
IIH	Input High Current			5	uA	
IVDD	VDD Current	20	30	40	mA	
VOL	Output Low Voltage			0.4	V	IOL=8mA, FSO/5 output
VOH	Output High Voltage	2.4			V	IOH=-4mA, FSO/5 output
CI	Input Capacitance			10	pF	
RL	Line Impedance	20	50	75	Ohm	Rambus Level, see note 1
VLT	Line Termination Voltage	2.2		2.7	V	Rambus Level, see note 1
IOH	Output High Current	-10		10	uA	FSO output
IOL	Output Low Current	40	50	75	mA	VOL=0.4V, FSO output
Ro	Output Resistance	5.3	8	10	Ohm	FSO output
Ro (PMOS)	Output Resistance	175	350	525	Ohm	IOH=-600uA, FSC output
Ro (NMOS)	Output Resistance	85	175	260	Ohm	IOL=600uA, FSC output

AC CHARACTERISTICS TA = 0°C to 80°C, VDD = 3.15V to 3.6V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Dt ₁	Duty Cycle	45		55	%	FSO, FSC
Dt ₂	Duty Cycle	55	59	62	%	FSO/5 for Rev.E
J	Jitter, short term			150	ps	
Tr/Tf	Rise/Fall Time	0.3		0.7	ns	Rambus level, FSO output
Tr/Tf	Rise/Fall Time	2	3.5	5	ns	FSO/5 output, 30 pF load
Tup	Power up Time		1	5	ms	1. After power is stable 2. Frequency from 0 to 250 MHz

Note1: Defined by customer's system implementation

ORDERING INFORMATION

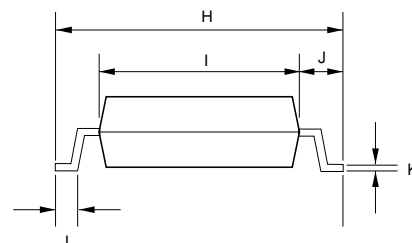
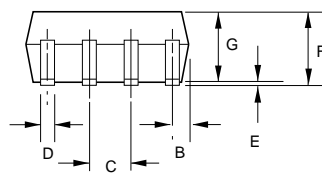
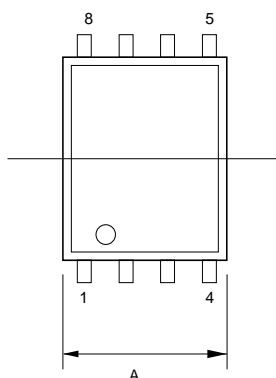
PART NO.	PACKAGE
MX8330MC	8-PIN SOP

PACKAGE INFORMATION

8-PIN PLASTIC SOP (150 mil)

ITEM	MILLIMETER	INCHES
A	4.95 MAX.	.195 MAX.
B	.53 [REF]	.021 [REF]
C	1.27 [TP]	.050 [TP]
D	.41 [TYP.]	.016 [TYP.]
E	.10 MIN.	.004 MIN.
F	1.73 MAX.	.068 MAX.
G	1.45 ± .13	.057 ± .005
H	5.99 ± .3	.236 ± .012
I	3.91 ± .13	.154 ± .005
J	1.02	.040
K	.20 [TYP.]	.008 [TYP.]
L	.76	.030

NOTE: Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.



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