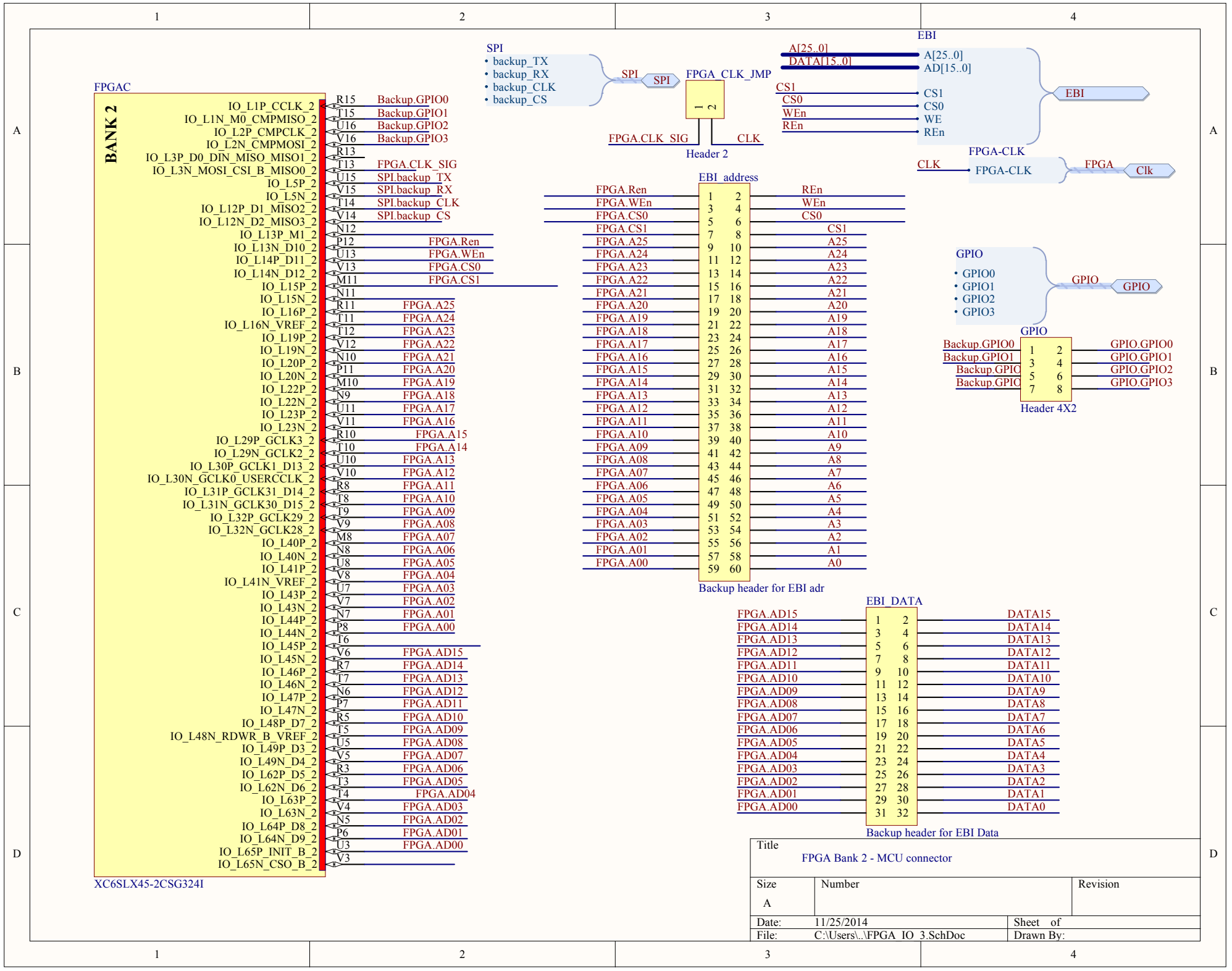
FPGAC
BANK 2
IO_L1P_CCLK_2 R15 Backup.GPIO0
IO_L1N_M0_CMPMISO_2 T15 Backup.GPIO1
IO_L2P_CMPCLK_2 U16 Backup.GPIO2
IO_L2N_CMPMOSI_2 V16 Backup.GPIO3
IO_L3P_D0_DIN_MISO_MISO1_2 R13
IO_L3N_MOSI_CSI_B_MISO0_2 T13 FPGA.CLK_SIG
IO_L5P_2 U15 SPI.backup_TX
IO_L5N_2 V15 SPI.backup_RX
IO_L12P_D1_MISO2_2 T14 SPI.backup_CLK
IO_L12N_D2_MISO3_2 V14 SPI.backup_CS
IO_L13P_M1_2 N12
IO_L13N_D10_2 P12 FPGA.Ren
IO_L14P_D11_2 U13 FPGA.WEn
IO_L14N_D12_2 V13 FPGA.CS0
IO_L15P_2 M11 FPGA.CS1
IO_L15N_2 N11
IO_L16P_2 R11 FPGA.A25
IO_L16N_VREF_2 T11 FPGA.A24
IO_L19P_2 T12 FPGA.A23
IO_L19N_2 V12 FPGA.A22
IO_L20P_2 N10 FPGA.A21
IO_L20N_2 P11 FPGA.A20
IO_L22P_2 M10 FPGA.A19
IO_L22N_2 N9 FPGA.A18
IO_L23P_2 U11 FPGA.A17
IO_L23N_2 V11 FPGA.A16
IO_L29P_GCLK3_2 R10 FPGA.A15
IO_L29N_GCLK2_2 T10 FPGA.A14
IO_L30P_GCLK1_D13_2 U10 FPGA.A13
IO_L30N_GCLK0_USERCCLK_2 V10 FPGA.A12
IO_L31P_GCLK31_D14_2 R8 FPGA.A11
IO_L31N_GCLK30_D15_2 T8 FPGA.A10
IO_L32P_GCLK29_2 T9 FPGA.A09
IO_L32N_GCLK28_2 V9 FPGA.A08
IO_L40P_2 M8 FPGA.A07
IO_L40N_2 N8 FPGA.A06
IO_L41P_2 U8 FPGA.A05
IO_L41N_VREF_2 V8 FPGA.A04
IO_L43P_2 U7 FPGA.A03
IO_L43N_2 V7 FPGA.A02
IO_L44P_2 N7 FPGA.A01
IO_L44N_2 P8 FPGA.A00
IO_L45P_2 T6
IO_L45N_2 V6 FPGA.AD15
IO_L46P_2 R7 FPGA.AD14
IO_L46N_2 T7 FPGA.AD13
IO_L47P_2 N6 FPGA.AD12
IO_L47N_2 P7 FPGA.AD11
IO_L48P_D7_2 R5 FPGA.AD10
IO_L48N_RDWR_B_VREF_2 T5 FPGA.AD09
IO_L49P_D3_2 U5 FPGA.AD08
IO_L49N_D4_2 V5 FPGA.AD07
IO_L62P_D5_2 R3 FPGA.AD06
IO_L62N_D6_2 T3 FPGA.AD05
IO_L63P_2 T4 FPGA.AD04
IO_L63N_2 V4 FPGA.AD03
IO_L64P_D8_2 N5 FPGA.AD02
IO_L64N_D9_2 P6 FPGA.AD01
IO_L65P_INIT_B_2 U3 FPGA.AD00
IO_L65N_CSO_B_2 V3
XC6SLX45-2CSG324I
SPI
• backup_TX
• backup_RX
• backup_CLK
• backup_CS
SPI
SPI
FPGA_CLK_JMP
1 2
FPGA.CLK_SIG
CLK
Header 2
EBI
A[25..0]
DATA[15..0]
A[25..0]
AD[15..0]
CS1
CS0
WEn
REn
CS1
CS0
WE
REn
EBI
FPGA-CLK
CLK
FPGA-CLK
FPGA
Clk
EBI_address
FPGA.Ren 1 2 REn
FPGA.WEn 3 4 WEn
FPGA.CS0 5 6 CS0
FPGA.CS1 7 8 CS1
FPGA.A25 9 10 A25
FPGA.A24 11 12 A24
FPGA.A23 13 14 A23
FPGA.A22 15 16 A22
FPGA.A21 17 18 A21
FPGA.A20 19 20 A20
FPGA.A19 21 22 A19
FPGA.A18 23 24 A18
FPGA.A17 25 26 A17
FPGA.A16 27 28 A16
FPGA.A15 29 30 A15
FPGA.A14 31 32 A14
FPGA.A13 33 34 A13
FPGA.A12 35 36 A12
FPGA.A11 37 38 A11
FPGA.A10 39 40 A10
FPGA.A09 41 42 A9
FPGA.A08 43 44 A8
FPGA.A07 45 46 A7
FPGA.A06 47 48 A6
FPGA.A05 49 50 A5
FPGA.A04 51 52 A4
FPGA.A03 53 54 A3
FPGA.A02 55 56 A2
FPGA.A01 57 58 A1
FPGA.A00 59 60 A0
Backup header for EBI adr
GPIO
• GPIO0
• GPIO1
• GPIO2
• GPIO3
GPIO
GPIO
GPIO
Backup.GPIO0 1 2 GPIO.GPIO0
Backup.GPIO1 3 4 GPIO.GPIO1
Backup.GPIO 5 6 GPIO.GPIO2
Backup.GPIO 7 8 GPIO.GPIO3
Header 4X2
EBI_DATA
FPGA.AD15 1 2 DATA15
FPGA.AD14 3 4 DATA14
FPGA.AD13 5 6 DATA13
FPGA.AD12 7 8 DATA12
FPGA.AD11 9 10 DATA11
FPGA.AD10 11 12 DATA10
FPGA.AD09 13 14 DATA9
FPGA.AD08 15 16 DATA8
FPGA.AD07 17 18 DATA7
FPGA.AD06 19 20 DATA6
FPGA.AD05 21 22 DATA5
FPGA.AD04 23 24 DATA4
FPGA.AD03 25 26 DATA3
FPGA.AD02 27 28 DATA2
FPGA.AD01 29 30 DATA1
FPGA.AD00 31 32 DATA0
Backup header for EBI Data
Title
FPGA Bank 2 - MCU connector
Size
A
Number
Revision
Date: 11/25/2014
Sheet of
File: C:\Users\..\FPGA_IO_3.SchDoc
Drawn By: