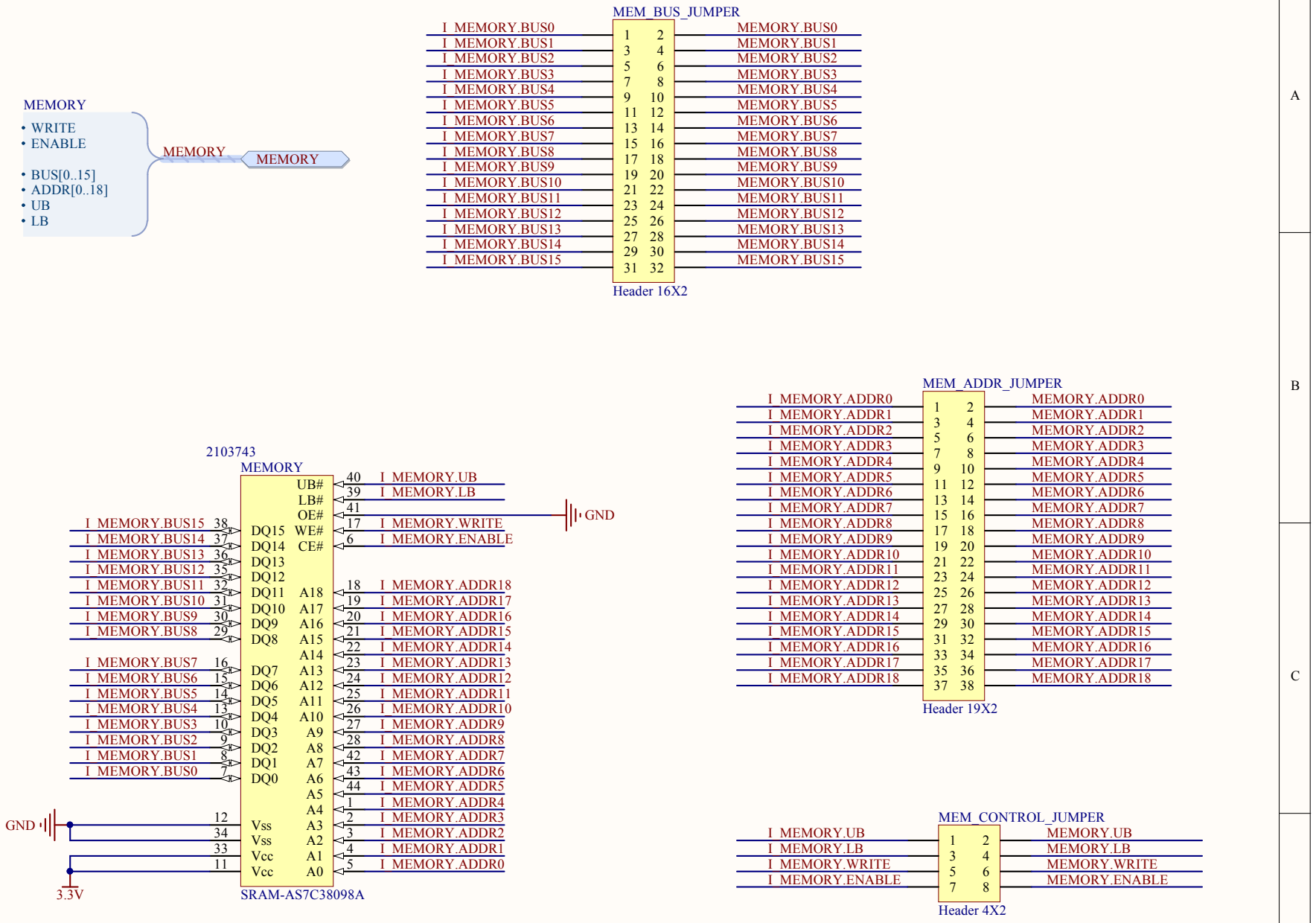
MEMORY
• WRITE
• ENABLE
• BUS[0..15]
• ADDR[0..18]
• UB
• LB
MEMORY
MEMORY
MEM_BUS_JUMPER
I_MEMORY.BUS0 1 2 MEMORY.BUS0
I_MEMORY.BUS1 3 4 MEMORY.BUS1
I_MEMORY.BUS2 5 6 MEMORY.BUS2
I_MEMORY.BUS3 7 8 MEMORY.BUS3
I_MEMORY.BUS4 9 10 MEMORY.BUS4
I_MEMORY.BUS5 11 12 MEMORY.BUS5
I_MEMORY.BUS6 13 14 MEMORY.BUS6
I_MEMORY.BUS7 15 16 MEMORY.BUS7
I_MEMORY.BUS8 17 18 MEMORY.BUS8
I_MEMORY.BUS9 19 20 MEMORY.BUS9
I_MEMORY.BUS10 21 22 MEMORY.BUS10
I_MEMORY.BUS11 23 24 MEMORY.BUS11
I_MEMORY.BUS12 25 26 MEMORY.BUS12
I_MEMORY.BUS13 27 28 MEMORY.BUS13
I_MEMORY.BUS14 29 30 MEMORY.BUS14
I_MEMORY.BUS15 31 32 MEMORY.BUS15
Header 16X2
2103743
MEMORY
UB# 40 I_MEMORY.UB
LB# 39 I_MEMORY.LB
OE# 41 GND
I_MEMORY.BUS15 38 DQ15 WE# 17 I_MEMORY.WRITE
I_MEMORY.BUS14 37 DQ14 CE# 6 I_MEMORY.ENABLE
I_MEMORY.BUS13 36 DQ13
I_MEMORY.BUS12 35 DQ12
I_MEMORY.BUS11 32 DQ11 A18 18 I_MEMORY.ADDR18
I_MEMORY.BUS10 31 DQ10 A17 19 I_MEMORY.ADDR17
I_MEMORY.BUS9 30 DQ9 A16 20 I_MEMORY.ADDR16
I_MEMORY.BUS8 29 DQ8 A15 21 I_MEMORY.ADDR15
A14 22 I_MEMORY.ADDR14
I_MEMORY.BUS7 16 DQ7 A13 23 I_MEMORY.ADDR13
I_MEMORY.BUS6 15 DQ6 A12 24 I_MEMORY.ADDR12
I_MEMORY.BUS5 14 DQ5 A11 25 I_MEMORY.ADDR11
I_MEMORY.BUS4 13 DQ4 A10 26 I_MEMORY.ADDR10
I_MEMORY.BUS3 10 DQ3 A9 27 I_MEMORY.ADDR9
I_MEMORY.BUS2 9 DQ2 A8 28 I_MEMORY.ADDR8
I_MEMORY.BUS1 8 DQ1 A7 42 I_MEMORY.ADDR7
I_MEMORY.BUS0 7 DQ0 A6 43 I_MEMORY.ADDR6
A5 44 I_MEMORY.ADDR5
A4 1 I_MEMORY.ADDR4
GND 12 Vss A3 2 I_MEMORY.ADDR3
34 Vss A2 3 I_MEMORY.ADDR2
33 Vcc A1 4 I_MEMORY.ADDR1
3.3V 11 Vcc A0 5 I_MEMORY.ADDR0
SRAM-AS7C38098A
MEM_ADDR_JUMPER
I_MEMORY.ADDR0 1 2 MEMORY.ADDR0
I_MEMORY.ADDR1 3 4 MEMORY.ADDR1
I_MEMORY.ADDR2 5 6 MEMORY.ADDR2
I_MEMORY.ADDR3 7 8 MEMORY.ADDR3
I_MEMORY.ADDR4 9 10 MEMORY.ADDR4
I_MEMORY.ADDR5 11 12 MEMORY.ADDR5
I_MEMORY.ADDR6 13 14 MEMORY.ADDR6
I_MEMORY.ADDR7 15 16 MEMORY.ADDR7
I_MEMORY.ADDR8 17 18 MEMORY.ADDR8
I_MEMORY.ADDR9 19 20 MEMORY.ADDR9
I_MEMORY.ADDR10 21 22 MEMORY.ADDR10
I_MEMORY.ADDR11 23 24 MEMORY.ADDR11
I_MEMORY.ADDR12 25 26 MEMORY.ADDR12
I_MEMORY.ADDR13 27 28 MEMORY.ADDR13
I_MEMORY.ADDR14 29 30 MEMORY.ADDR14
I_MEMORY.ADDR15 31 32 MEMORY.ADDR15
I_MEMORY.ADDR16 33 34 MEMORY.ADDR16
I_MEMORY.ADDR17 35 36 MEMORY.ADDR17
I_MEMORY.ADDR18 37 38 MEMORY.ADDR18
Header 19X2
MEM_CONTROL_JUMPER
I_MEMORY.UB 1 2 MEMORY.UB
I_MEMORY.LB 3 4 MEMORY.LB
I_MEMORY.WRITE 5 6 MEMORY.WRITE
I_MEMORY.ENABLE 7 8 MEMORY.ENABLE
Header 4X2
Title
Memory
Size
A
Number
Revision
version 1
Date: 11/25/2014
Sheet of
File: C:\Users\..\SRAM.SchDoc
Drawn By: