CMOSTEK

CMT2300A

Ultra-low Power Sub-1GHz RF Transceiver

Features

- Frequency range: 127 ~1020 MHz
- Modem: OOK, (G)FSK and (G)MSK
- Data rate: 0.5 ~ 300 kbps
- Sensitivity: - 121 dBm 2.0 kbps, F_{RF} = 433.92 MHz
  -111 dBm 50 kbps, F_{RF} = 433.92 MHz
- Voltage range: 1.8 ~3.6 V
- Transmit current: 23 mA @ 13 dBm, 433.92 MHz, FSK
  72 mA @ 20 dBm, 433.92 MHz, FSK
- Rx current: 8.5 mA @ 433.92 MHz, FSK (High power mode)
  7.2 mA @ 433.92 MHz, FSK (Low power mode)
- Super-low Power receive mode
- Sleep current: 300 nA, Duty Cycle = OFF
  800 nA, Duty Cycle = ON
- Receiver features:
  - Fast and stable automatic frequency control (AFC)
  - 3 types of clock data recovery system (CDR)
  - Fast and accurate signal detection (PJD)
- 4-wire SPI interface
- Direct and packet mode supported
- Configurable packet handler and 64-Byte FIFO.
- NRZ, Manchester codec, Whitening codec, Forward Error Correction (FEC)

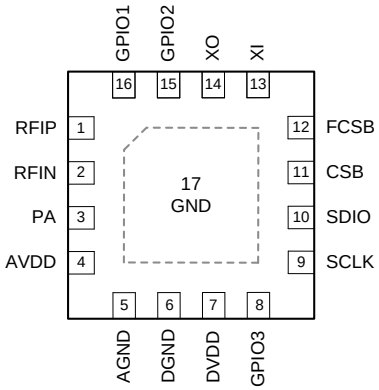
Application

- Automatic meter reading
- Home security and building automation
- ISM band data communication
- Industrial monitoring and control
- Remote control and security system
- Remote key entry
- Wireless sensor node
- Tag reader

Ordering Information

Model	Frequency	Package	MOQ
CMT2300A-EQR	433.92 MHz	QFN16	3,000 pcs
Please see Table 23 for more ordering details.			

QFN16 (3x3) Packaging



CMT2300 Top View

Description

CMT2300A is an ultra-low power, high performance, OOK (G) FSK RF transceiver suitable for a variety of 140 to 1020 MHz wireless applications. It is part of the CMOSTEK NextGenRF™ RF product line. The product line contains the complete transmitters, receivers and transceivers. The high integration of CMT2300A simplifies the peripheral materials required in the system design. Up to +20 dBmTx Power and -121 dBm sensitivity optimize the performance of the application. It supports a variety of packet formats and codec methods to meet the needs of various different applications. In addition, CMT2300A also supports 64-byte Tx/Rx FIFO, GPIO and interrupt configuration, Duty-Cycle operation mode, channel sensing, high-precision RSSI, low-voltage detection, power-on reset, low frequency clock output, manual fast frequency hopping, squelch and etc. The features make the application design more flexible and differentiated. CMT2300A operates from 1.8 V to 3.6 V. Only 8.5 mA current is consumed when the sensitivity is -121 dBm, SuperLow Power mode can further reduce the chip power consumption. Only 23mA Tx current is consumed when the output power is 13 dBm.

Table of Contents

1. Electrical Characteristics

V_{DD}= 3.3 V, T_{OP}= 25 °C, F_{RF} = 433.92 MHz, the sensitivity is measured by receiving a PN9 coded data and matching the impedance to 50Ω under the 0.1%BER standard. Unless otherwise stated, all results are tested on the CMT2300A-EM evaluation board.

1.1 Recommended Operation Condition

Table 1. Recommended Operation Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		-40		85	℃
Power voltage slope			1			mV/us

1.2 Absolute Maximum Rating

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} +0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating[2]		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Notes:

[1]. Exceeding the Absolute Maximum Ratings may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT2300A is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.

Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Power Consumption

Table 3. Power Consumption Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep current	I_{SLEEP}	Sleep mode, sleep timer is off		300		nA
		Sleep mode, sleep timer is on		800		nA
Standby current	$I_{Standby}$	Crystal oscillator is on		1.45		mA
RFS current	I_{RFS}	433 MHz		5.7		mA
		868 MHz		5.8		mA
		915 MHz		5.8		mA
TFS current	I_{TFS}	433 MHz		5.6		mA
		868 MHz		5.9		mA
		915 MHz		5.9		mA
RXcurrent (high power mode)	I_{Rx-HP}	FSK, 433 MHz, 10 kbps,10 kHz F_{DEV}		8.5		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		8.6		mA
		FSK, 915 MHz, 10 kbps,10 kHz F_{DEV}		8.9		mA
RX current (low power mode)	I_{Rx-LP}	FSK, 433 MHz, 10 kbps, 10 kHz F_{DEV}		7.2		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		7.3		mA
		FSK, 915 MHz, 10 kbps, 10 kHz F_{DEV}		7.6		mA
TX current	I_{Tx}	FSK, 433 MHz, +20 dBm (Direct Tie)		72		mA
		FSK, 433 MHz, +20 dBm (RF switch)		77		mA
		FSK, 433 MHz, +13 dBm (Direct Tie)		23		mA
		FSK, 433 MHz, +10 dBm (Direct Tie)		18		mA
		FSK, 433 MHz, -10 dBm(Direct Tie)		8		mA
		FSK, 868 MHz, +20 dBm(Direct Tie)		87		mA
		FSK, 868 MHz, +20 dBm(RF switch)		80		mA
		FSK, 868 MHz, +13 dBm (Direct Tie)		27		mA
		FSK, 868 MHz, +10 dBm (Direct Tie)		19		mA
		FSK, 868 MHz, -10 dBm (Direct Tie)		8		mA
		FSK, 915 MHz, +20 dBm (Direct Tie)		70		mA
		FSK, 915 MHz, +20 dBm (RF switch)		75		mA
		FSK, 915 MHz, +13 dBm (Direct Tie)		28		mA
		FSK, 915 MHz, +10 dBm (Direct Tie)		19		mA
		FSK, 915 MHz, -10 dBm (Direct Tie)		8		mA

1.4 Receiver

Table 4. Receiver specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR	OOK	0.5		40	kbps
		FSK and GFSK	0.5		300	kbps
Deviation	F_{DEV}	FSK and GFSK	2		200	kHz
Sensitivity @ 433 MHz	$S_{433\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-121		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-116		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power setting）		-115		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-113		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power		-112		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-111		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-108		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-105		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--103		dBm
Sensitivity @ 868 MHz	$S_{868\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-119		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power setting）		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power setting）		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-108		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Sensitivity @ 915 MHz	$S_{915\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-117		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power mode）		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power mode）		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Saturation Input Signal Level	P_{LVL}				20	dBm
Input Impedance	HF（High frequency band）	180R // 2.8pF				
	LF（Low frequency band）	135R // 1.9pF				
Image Rejection Ratio	IMR	F_{RF}=433 MHz		35		dBc
		F_{RF}=868 MHz		33		dBc
		F_{RF}=915 MHz		33		dBc

RX Channel Bandwidth	BW	RX channel bandwidth	50		500	kHz
Co-channel Rejection Ratio	CCR	DR = 10 kbps, F_{DEV} = 10 kHz; Interference with the same modulation		-7		dBc
Adjacent Channel Rejection Ratio	ACR-I	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100kHz, 200 kHzChannel spacing, interference with the same modulation		30		dBc

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
AlternateChannel Rejection Ratio	ACR-II	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100kHz, 400 kHz Channel spacing, interference with the same modulation		45		dBc
Blocking Rejection Ratio	BI	DR = 10 kbps, F_{DEV} = 10 kHz; ±1 MHz Deviation, continuous wave interference		70		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz; ± 2 MHz Deviation, continuous wave interference		72		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz; ±10 MHz Deviation, continuous wave interference		75		dBc
Input 3rd Order Intercept Point	IIP3	DR = 10 kbps, F_{DEV} = 10 kHz; 1 MHz and 2 MHz Deviation dual tone test, maximum system gain setting.		-25		dBm
RSSIRange	RSSI		-120		20	dBm
More Sensitivity (Typical Configuration)		433.92 MHz, DR = 1.2kbps, F_{DEV} = 5 kHz		-122.9		dBm
		433.92 MHz, DR = 1.2kbps, F_{DEV} = 10 kHz		-121.8		dBm
		433.92 MHz, DR = 1.2kbps, F_{DEV} = 20 kHz		-119.5		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 5 kHz		-120.6		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 10 kHz		-120.3		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 20 kHz		-119.7		dBm
		433.92 MHz, DR = 9.6 kbps, F_{DEV} = 9.6 kHz		-116.0		dBm
		433.92 MHz, DR = 9.6 kbps, FDEV = 19.2 kHz		-116.1		dBm
		433.92 MHz, DR = 20 kbps, FDEV = 10 kHz		-114.2		dBm
		433.92 MHz, DR = 20 kbps, FDEV = 20 kHz		-113.0		dBm
		433.92 MHz, DR = 50 kbps, FDEV = 25 kHz		-110.6		dBm
		433.92 MHz, DR = 50 kbps, FDEV = 50 kHz		-109.0		dBm
		433.92 MHz, DR = 100 kbps, FDEV = 50 kHz		-107.8		dBm
		433.92 MHz, DR = 200 kbps, FDEV = 50 kHz		-103.5		dBm
		433.92 MHz, DR = 200 kbps, FDEV = 100 kHz		-104.3		dBm
		433.92 MHz, DR = 300 kbps, FDEV = 50 kHz		-98.0		dBm
		433.92 MHz, DR = 300 kbps, FDEV = 150 kHz		-101.6		dBm

1.5 Transmitter

Table 5. Transmitter Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output power	P_{OUT}	Need specific peripheral materials for different frequency bands	-20		+20	dBm
Output power step	P_{STEP}			1		dB
GFSK Gaussian filter coefficient	BT		0.3	0.5	1.0	-
Output power variation	$P_{OUT-TOP}$	Temperature from -40 to +85 □C		1		dB
Stray radiation		P_{OUT} = +13 dBm,433MHz, F_{RF}<1 GHz			-42	dBm
		1 GHz to 12.75 GHz, with harmonic			-36	dBm
Harmonic output for F_{RF}= 433 MHz[1]	$H2_{433}$	2nd harmonic +20 dBm P_{OUT}		-46		dBm
	$H3_{433}$	3nd harmonic +20 dBm P_{OUT}		-50		dBm
Harmonic output for F_{RF}= 868 MHz[1]	$H2_{868}$	2nd harmonic +20 dBm P_{OUT}		-43		dBm
	$H3_{868}$	3nd harmonic +20 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 915 MHz[1]	$H2_{868}$	2nd harmonic +20 dBm P_{OUT}		-48		dBm
	$H3_{868}$	3nd harmonic +20 dBm P_{OUT}		-53		dBm
Harmonic output for F_{RF}= 433 MHz[1]	$H2_{433}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{433}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 868 MHz[1]	$H2_{868}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{868}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm
Harmonic output for F_{RF}= 915 MHz[1]	$H2_{868}$	2nd harmonic +13 dBm P_{OUT}		-52		dBm
	$H3_{868}$	3nd harmonic +13 dBm P_{OUT}		-52		dBm

Notes:

[1]. The harmonic parameter values mainly depend on the quality of the hardware matching network. The above data is measured based on the CMT2300A-EM module.

1.6 Settling Time

Table 6. Settling Time

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settle time	T_{SLP-RX}	From Sleep to RX		1000		us
	T_{SLP-TX}	From Sleep to TX		1000		us
	T_{STB-RX}	From Standby to RX		350		us
	T_{STB-TX}	From Standby to TX		350		us
	T_{RFS-RX}	From RFS to RX		20		us
	T_{TFS-RX}	From TFS to TX		20		us
	T_{TX-RX}	From TX to RX （Ramp Down time needs $2T_{symbol}$ ）		$2T_{symbol}$ +350		us
	T_{RX-TX}	From RX to TX		350		us

Notes:

[1]. T_{SLP-RX} and T_{SLP-TX} depend on the crystal oscillator startup time, which is related to crystal characteristics.

1.7 Frequency Synthesizer

Table 7. Frequency Synthesizer Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Need different matching networks	760		1020	MHz
			380		510	MHz
			190		340	MHz
			127		170	MHz
Frequency resolution	F_{RES}			25		Hz
Frequency tuning time	t_{TUNE}			150		us
Phase noise@ 433 MHz	PN_{433}	10 kHz frequency deviation		-94		dBc/Hz
		100 kHz frequency deviation		-99		dBc/Hz
		500 kHz frequency deviation		-118		dBc/Hz
		1MHz frequency deviation		-127		dBc/Hz
		10 MHz frequency deviation		-134		dBc/Hz
Phase noise@ 868 MHz	PN_{868}	10 kHz frequency deviation		-92		dBc/Hz
		100 kHz frequency deviation		95		dBc/Hz
		500 kHz frequency deviation		-114		dBc/Hz
		1MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz
Phase noise@ 915 MHz	PN_{915}	10 kHz frequency deviation		-89		dBc/Hz
		100 kHz frequency deviation		-92		dBc/Hz
		500 kHz frequency deviation		-111		dBc/Hz
		1MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz

1.8 Crystal Oscillator

Table 8. Crystal Oscillator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
Equivalent resistance	Rm			60		Ω
Start-up time[3]	t_{XTAL}			400		us

Notes:

[1]. CMT2300A can use the external reference clock to drive the XIN pin through the coupling capacitor. The peak value of the external clock signal is between 0.3V and 0.7V.

[2]. The value includes (1) initial error; (2) crystal load; (3) aging; and (4) change with temperature. The acceptable crystal frequency tolerance is limited by the receiver bandwidth and the RF frequency offset between the transmitter and the receiver.

[3]. The parameter is largely related to the crystal.

1.9 Low Frequency Oscillator

Table 9. Low Frequency Oscillator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Calibration frequency [1]	F_{LPOSC}			32		kHz
Frequency accuracy		After calibration		±1		%
Temperature coefficient [2]				-0.02		%/°C
Supply voltage coefficient [3]				+0.5		%/V
Initial calibration time	$t_{LPOSC-CAL}$			4		ms

Notes:

[1]. The low frequency oscillator is automatically calibrated to the crystal oscillator frequency at the PUP stage and periodically calibrated at this stage.

[2]. After calibration, the frequency changes with temperature.

[3]. After calibration, the frequency changes with the change of the supply voltage.

1.10 Low Battery Detection

Table 10. Low Battery Detection Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection accuracy	LBD_{RES}			50		mV

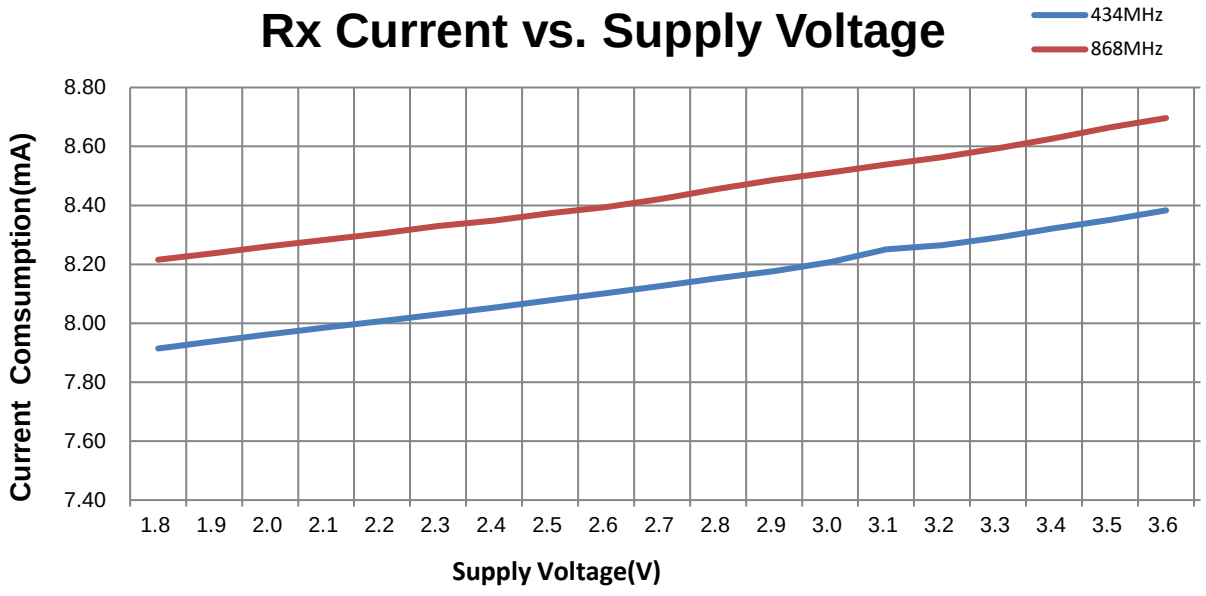
1.11 Digital Interface

Table 11. Digital interface specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital input high level	V_{IH}		Vdd-0.4			V_{DD}
Digital input low level	V_{IL}				0.2	V_{DD}
Digital output high level	V_{OH}	@I_{OH}= -0.5mA	Vdd-0.4			V
Digital output low level	V_{OL}	@I_{OL}= 0.5mA			0.4	V
SCLK Frequency	F_{SCL}				5	MHz
SCLK high time	T_{CH}		80			ns
SCLK low time	T_{CL}		80			ns
SCLKrise time	T_{CR}				50	ns
SCLKfall time	T_{CF}				50	ns

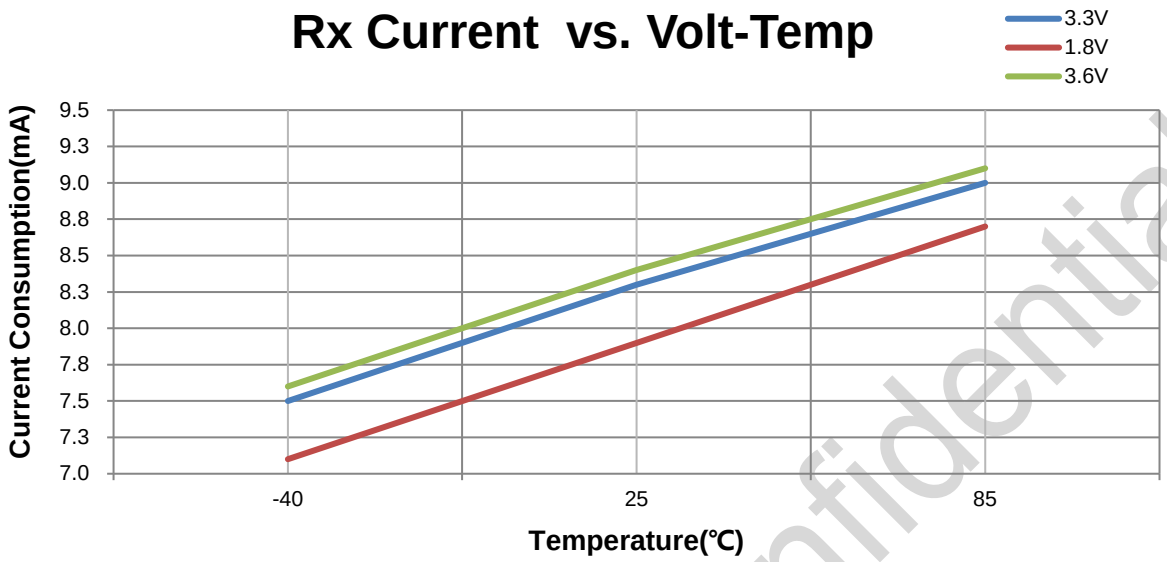
1.12 Figures of Critical Parameters

1.12.1 Rx Current VS. Supply Voltage

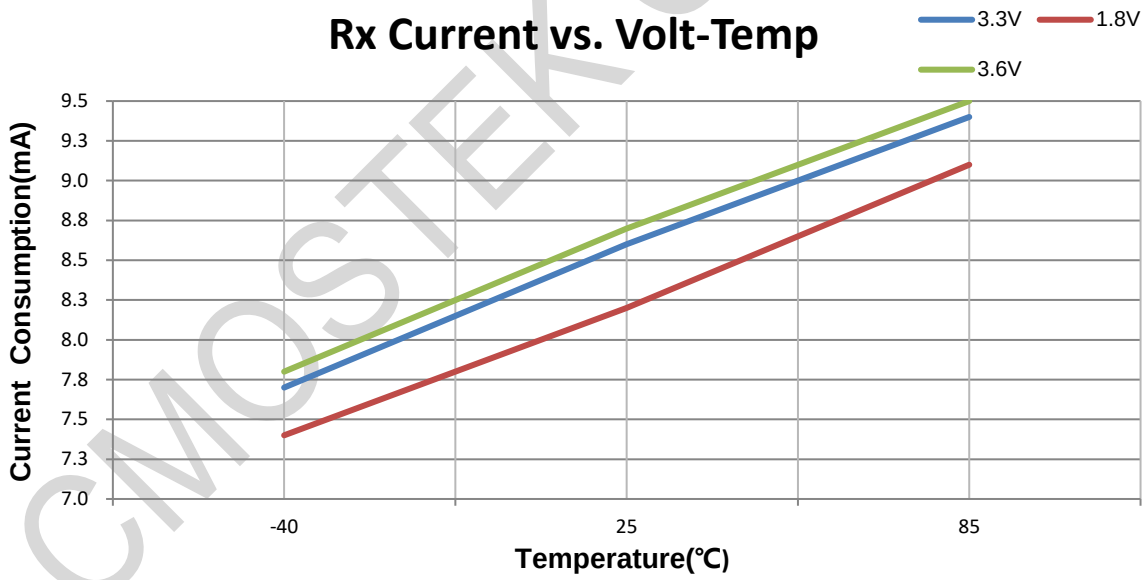


Testing Condition: Freq = 434MHz / 868MHz, Fdev = 10KHz, BR = 10Kbps

1.12.2 Rx Current VS. Voltage Temperature

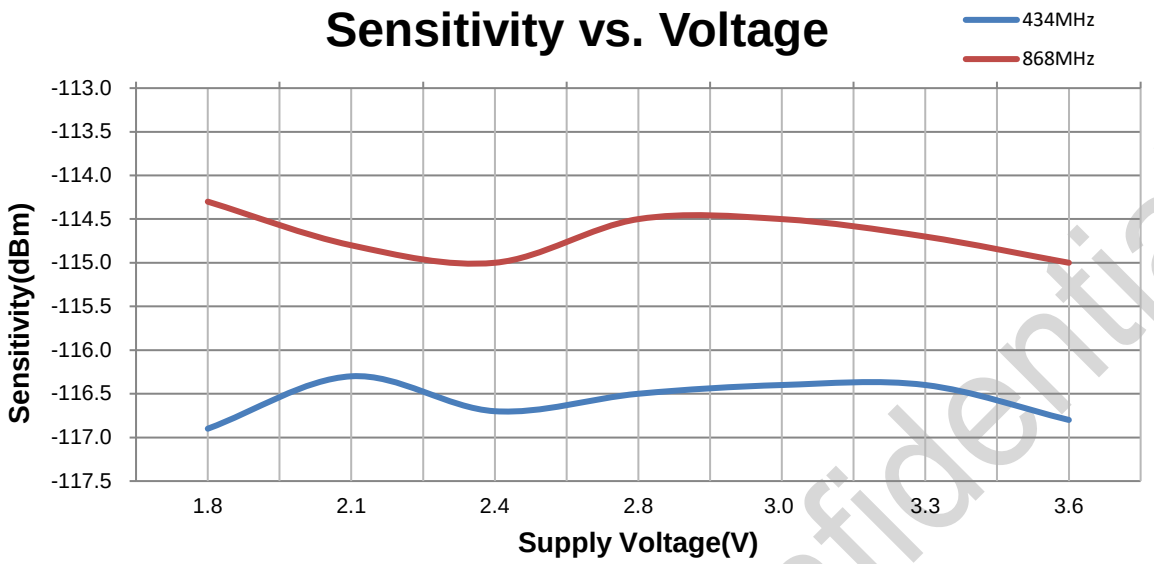


Test Condition: Freq = 434MHz,Fdev = 10KHz, BR = 10Kbps



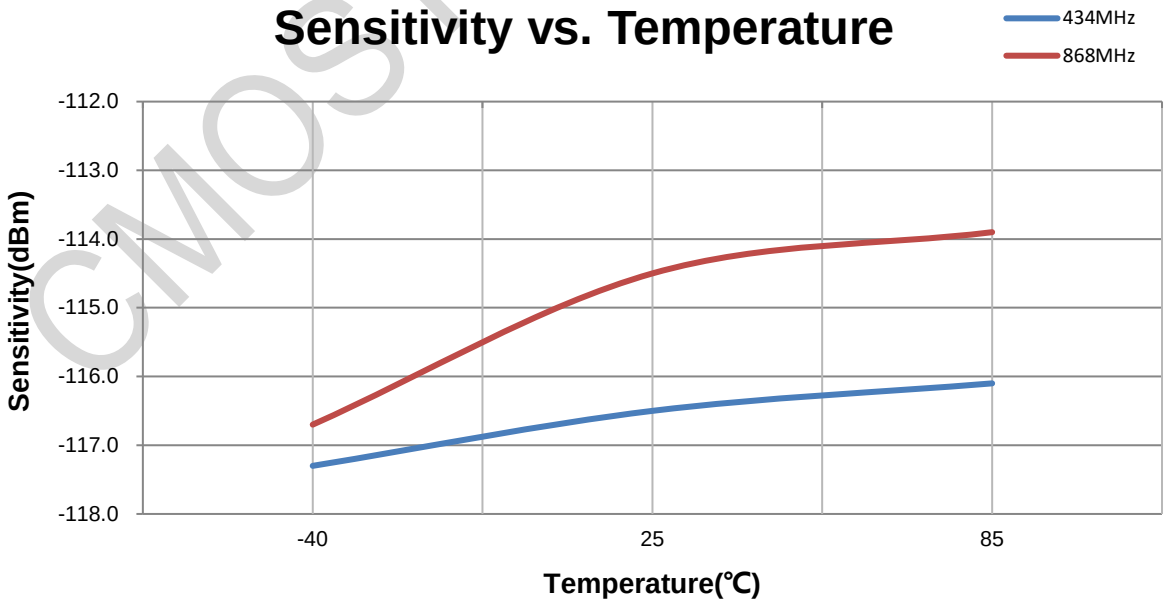
Test Condition: Freq = 868MHz, Fdev = 10KHz, BR = 10Kbps

1.12.3 Sensitivity VS. Voltage



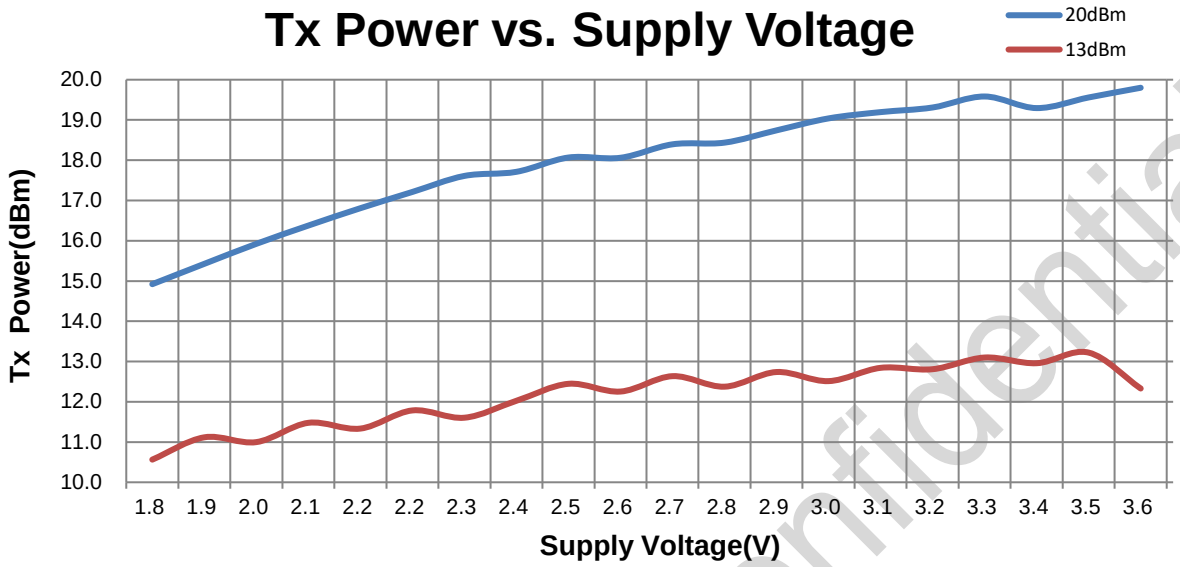
Test Condition: FSK modulation, DEV = 10KHz, BR = 10Kbps

1.12.4 Sensitivity VS. Temperature

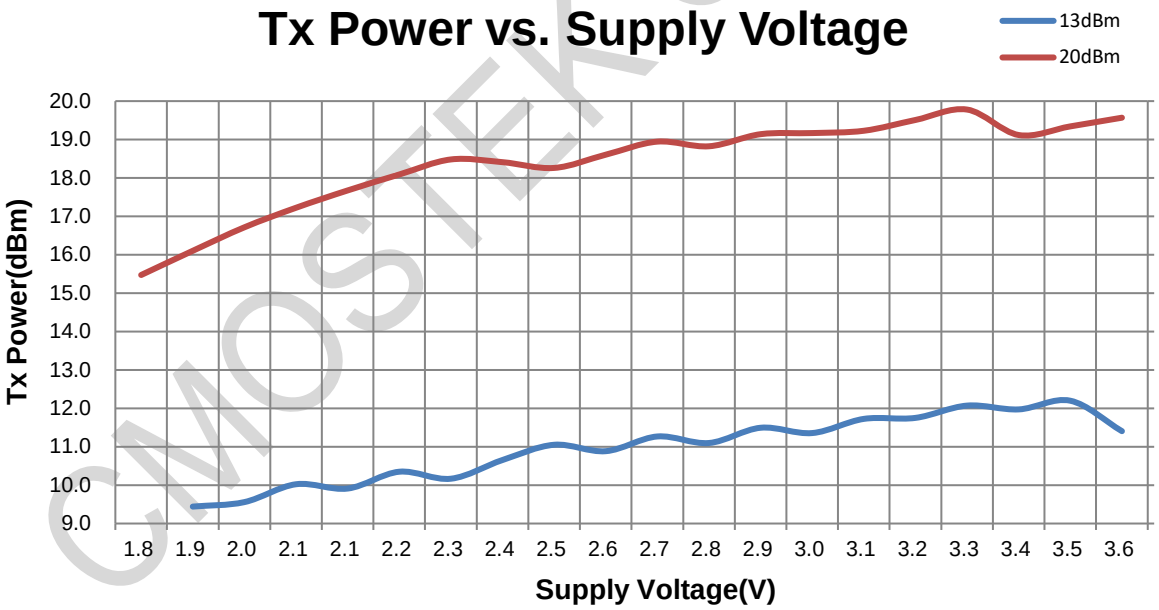


Test Condition: FSK, DEV = 10KHz, BR = 10Kbps

1.12.5 Tx Power VS. Supply Voltage

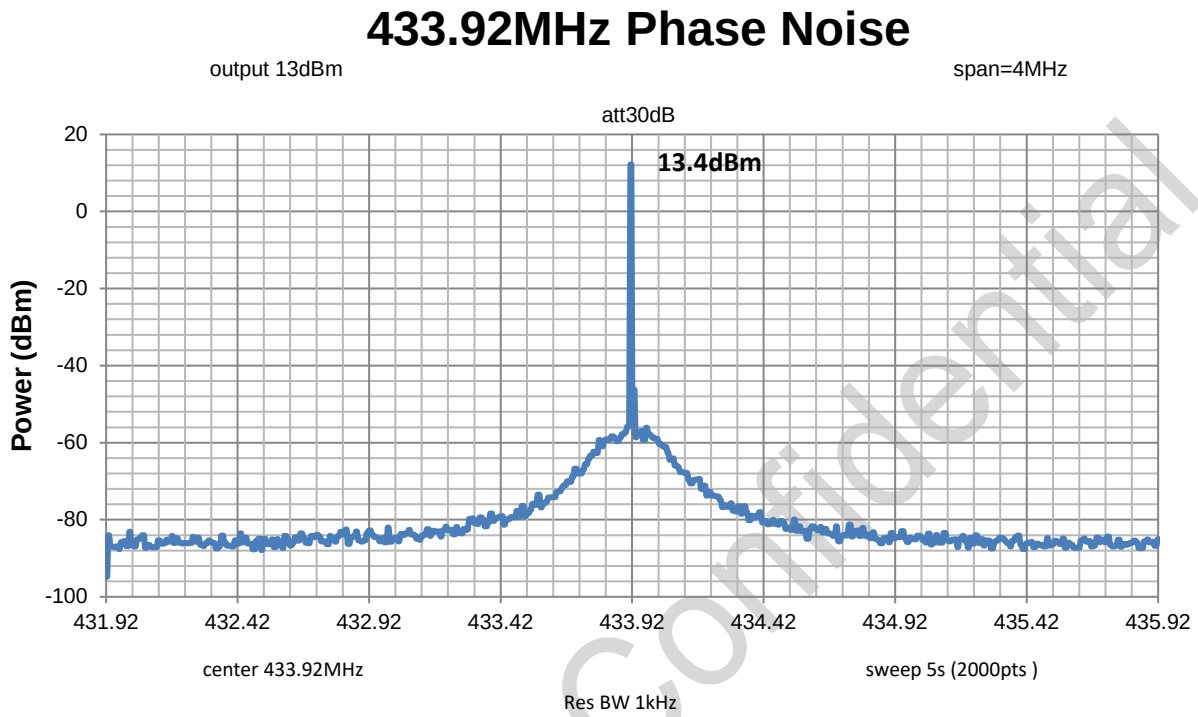


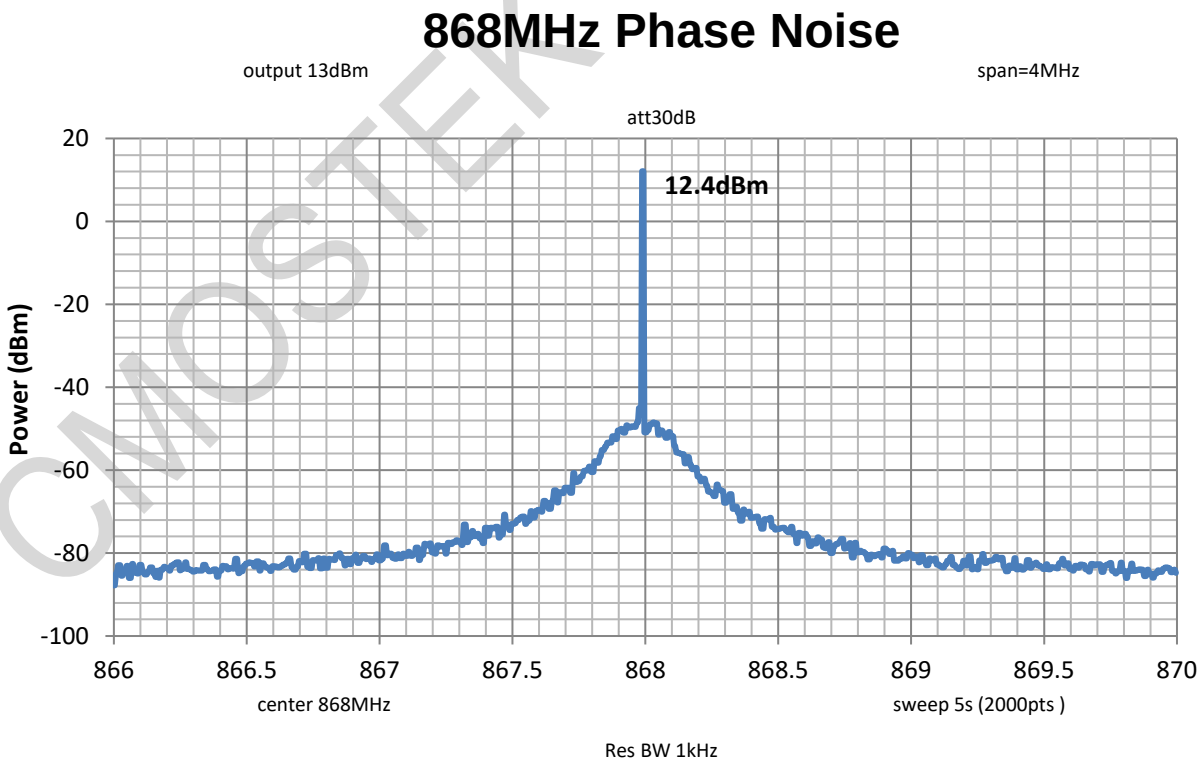
Test Condition: Freq = 434 MHz, 20 dBm / 13dBm matching network



Test Condition: Freq = 868 MHz, 20 dBm / 13dBm matching network

1.12.6 Tx Phase Noise





2. Pin Descriptions

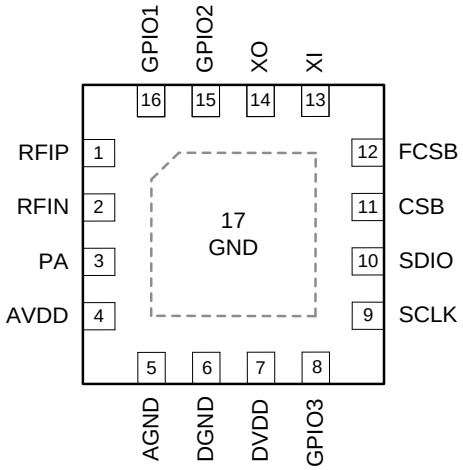
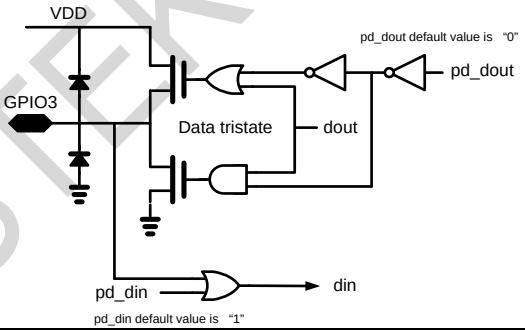
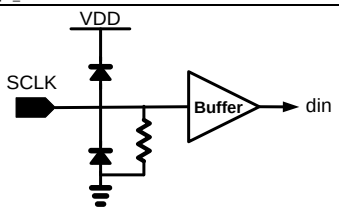
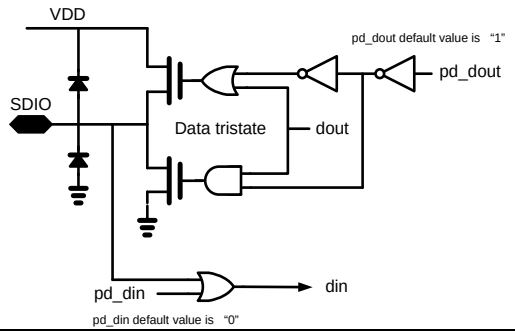
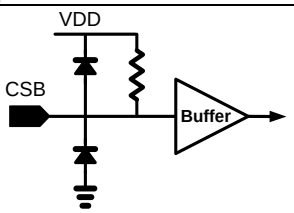
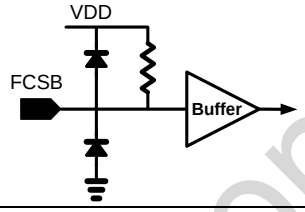
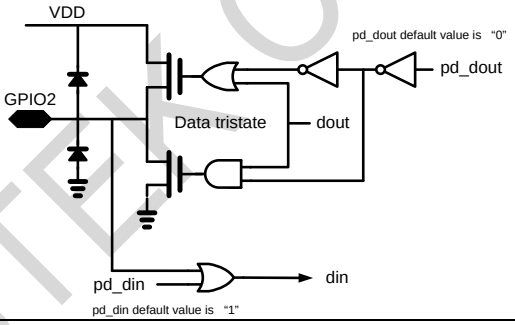
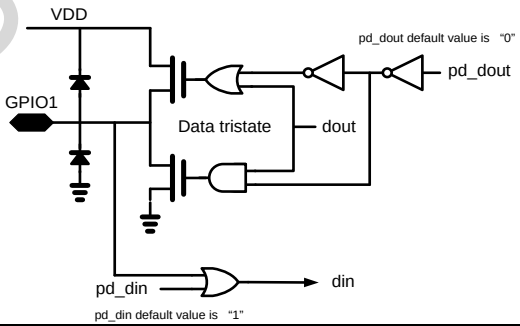


Figure 1. CMT2300A pin descriptions

Table 12. CMT2300A Pin Descriptions

Pin #	Name	I/O	Internal IO Schematic	Descriptions
1	RFIP	I		RF signal input P
2	RFIN	I		RF signal input N
3	PA	O		PA output
4	AVDD	IO		Analog VDD
5	AGND	IO		Analog GND
6	DGND	IO		Digital GND
7	DVDD	IO		Digital VDD
8[1]	GPIO3	IO		Configured as CLKO, DOUT/DIN, INT2 and DCLK (TX/RX)
9	SCLK	I		SPI clock

Pin #	Name	I/O	Internal IO Schematic	Descriptions
10	SDIO	IO		SPI data input and output
11	CSB	I		SPI chip selection bar for register access, active low
12	FCSB	I		SPI chip selection bar for FIFO access, active low
13	XI	I		Crystal circuit input
14	XO	O		Crystal circuit output
15[1]	GPIO2	IO		Configured as INT1, INT2, DOUT/DIN, DCLK (TX/RX) and RF_SWT
16[1]	GPIO1	IO		Configured as DOUT/DIN, INT1, INT2, DCLK (TX/RX) and RF_SWT
17	GND	I		Analog GND. It must be grounded.

Pin #	Name	I/O	Internal IO Schematic	Descriptions

Notes:

[1]. INT1 and INT2 are interrupts. DOUT is demodulated output. DIN is a modulation input. DCLK is a modulation or demodulation data rate synchronization clock, automatic switching in TX/RX mode.

[2]. The SCLK pin connects an internal pull-down resistor of 4.7 kΩ inside the chip. Thus in low-power applications, the MCU cannot output high level (pull up), otherwise it will generate leakage current and will cause low-power implementation failure.

[3]. The SDIO pin connects an internal pull-up resistor of 15 kΩ inside the chip. Thus in low-power applications, the MCU cannot output low level (pull down), otherwise it will generate leakage current and will cause low-power implementation failure.

[4]. The GPIO pins connect an internal pull-up resistor of 15 kΩ inside the chip. Thus in low-power applications, the MCU cannot output low level (pull down), otherwise it will generate leakage current and will cause low-power implementation failure.

3. Typical Application Schematic

3.1 Direct Tie Schematic Diagram

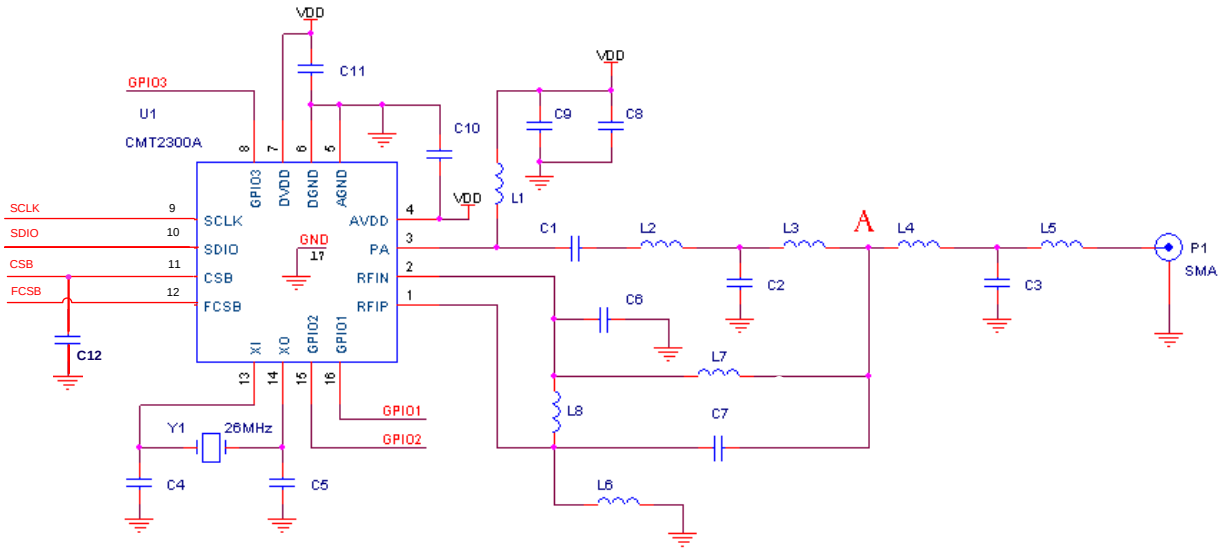


Figure 2. Direct Tie Application Schematic Diagram

Table 13. 13 dBm direct tie application BOM

No.	Descriptions	Values			Unit	Supplier
		433 MHz +13 dBm	868 MHz +13dBm	915 MHz +13dBm		
C1	±5%, 0603 NP0, 50 V	15	22	22	pF	
C2	±5%, 0603 NP0, 50 V	5.6	6.2	6.2	pF	
C3	±5%, 0603 NP0, 50 V	7.5	3.6	3.3	pF	
C4	±5%, 0603 NP0, 50 V	24	24	24	pF	
C5	±5%, 0603 NP0, 50 V	24	24	24	pF	
C6	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C7	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C8	±5%, 0603 NP0, 50 V	4.7			uF	
C9	±5%, 0603 NP0, 50 V	470			pF	
C10	±5%, 0603 NP0, 50 V	0.1			uF	
C11	±5%, 0603 NP0, 50 V	0.1			uF	
C12	±5%, 0603 NP0, 50 V	47			pF	
L1	±5%, 0603 Multilayer chip inductor	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Multilayer chip inductor	56	10	8.2	nH	Sunlord SDCL
L3	±5%, 0603 Multilayer chip inductor	39	8.2	6.8	nH	Sunlord SDCL
L4	±5%, 0603 Multilayer chip inductor	18	10	8.2	nH	Sunlord SDCL
L5	±5%, 0603 Multilayer chip inductor	18	10	8.2	nH	Sunlord SDCL
L6	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
L7	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
L8	±5%, 0603 Multilayer chip inductor	68	12	12	nH	Sunlord SDCL

Y1	±10 ppm, SMD32*25 mm		26		MHz	EPSON
U1	CMT2300A, Ultra Low Power Sub-1GHz RF Transceiver				-	CMOSTEK

Table 14. 20 dBm Direct Tie Application BOM

No.	Descriptions	Values			Unit	Supplier
		433 MHz +20 dBm	868 MHz +20 dBm	915 MHz +20 dBm		
C1	±5%, 0603 NP0, 50 V	15	18	18	pF	
C2	±5%, 0603 NP0, 50 V	3.0	3.6	3.6	pF	
C3	±5%, 0603 NP0, 50 V	6.2	3.3	3.3	pF	
C4	±5%, 0603 NP0, 50 V	24	24	24	pF	
C5	±5%, 0603 NP0, 50 V	24	24	24	pF	
C6	±5%, 0603 NP0, 50 V	4.7	2	1.8	pF	
C7	±5%, 0603 NP0, 50 V	4.7	2	1.8	pF	
C8	±5%, 0603 NP0, 50 V	4.7			uF	
C9	±5%, 0603 NP0, 50 V	470			pF	
C10	±5%, 0603 NP0, 50 V	0.1			uF	
C11	±5%, 0603 NP0, 50 V	0.1			uF	
C12	±5%, 0603 NP0, 50 V	47			pF	
L1	±5%, 0603 Multilayer chip inductor	180	100	100	nH	Sunlord SDCL
L2	±5%, 0603 Multilayer chip inductor,	22	12	12	nH	Sunlord SDCL
L3	±5%, 0603 Multilayer chip inductor	cap 15pF	15	15	nH	Sunlord SDCL
L4	±5%, 0603 Multilayer chip inductor	33	6.2	6.2	nH	Sunlord SDCL
L5	±5%, 0603 Multilayer chip inductor	33	6.2	6.2	nH	Sunlord SDCL
L6	±5%, 0603 Multilayer chip inductor	27	15	15	nH	Sunlord SDCL
L7	±5%, 0603 Multilayer chip inductor	27	15	15	nH	Sunlord SDCL
L8	±5%, 0603 Multilayer chip inductor	68	12	12	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26			MHz	EPSON
U1	CMT2300A, Ultra Low Power Sub-1GHz RF Transceiver				-	CMOSTEK

3.2 RF Switch Type Schematic

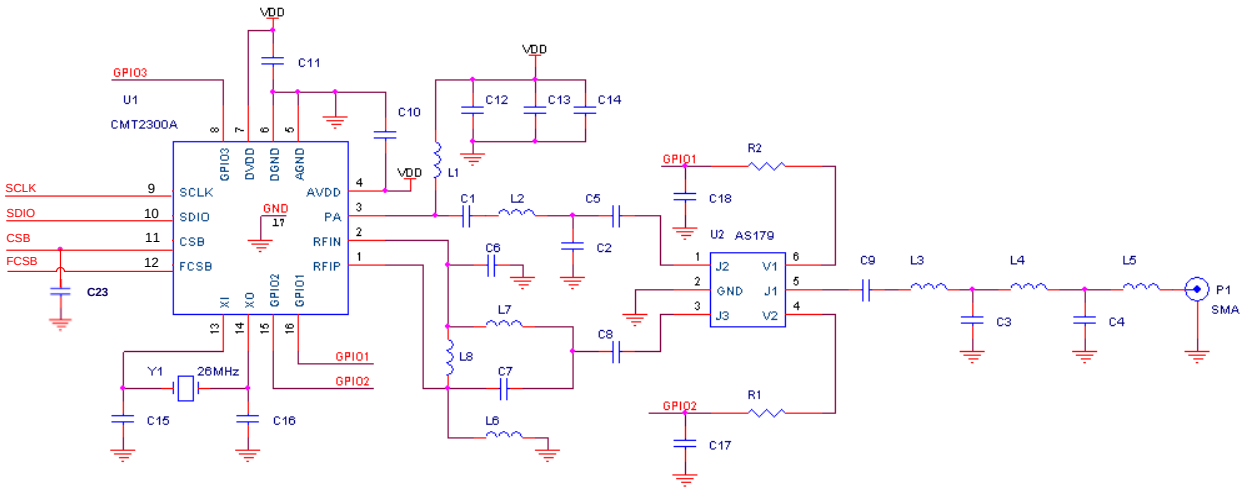


Figure 3. Application Schematic Diagram for RF Switch Type

Table 15. Typical Application BOM for RF Switch Type

No.	Descriptions	Values		Unit	Supplier
		434 MHz +20 dBm	868 /915 MHz +20 dBm		
C1	±5%, 0402 NP0, 50 V	15	15	pF	
C2	±5%, 0402 NP0, 50 V	10	3.9	pF	
C3	±5%, 0402 NP0, 50 V	8.2	2.7	pF	
C4	±5%, 0402 NP0, 50 V	8.2	2.7	pF	
C5	±5%, 0402 NP0, 50 V	18nH	220	pF	
C6	±5%, 0402 NP0, 50 V	4.7	2	pF	
C7	±5%, 0402 NP0, 50 V	4.7	2	pF	
C8	±5%, 0402 NP0, 50 V	220	220	uF	
C9	±5%, 0402 NP0, 50 V	220	220	pF	
C10	±5%, 0402 NP0, 50 V	0.1		uF	
C11	±5%, 0402 NP0, 50 V	0.1		uF	
C12	±5%, 0402 NP0, 50 V	470		pF	
C13	±5%, 0402 NP0, 50 V	2200		pF	
C14	±5%, 0402 NP0, 50 V	4.7		uF	
C15	±5%, 0402 NP0, 50 V	24	24	pF	
C16	±5%, 0402 NP0, 50 V	24	24	pF	
C17	±5%, 0402 NP0, 50 V	10	10	pF	
C18	±5%, 0402 NP0, 50 V	10	10	pF	
C23	±5%, 0402 NP0, 50 V	47		pF	
L1	±5%, 0603 Multilayer chip inductor	180	100	nH	Sunlord SDCL
L2	±5%, 0402 Multilayer chip inductor	27	6.8	nH	Sunlord SDCL
L3	±5%, 0402 Multilayer chip inductor	18	12	nH	Sunlord SDCL
L4	±5%, 0402 Multilayer chip inductor	33	22	nH	Sunlord SDCL
L5	±5%, 0402 Multilayer chip inductor	15	10	nH	Sunlord SDCL
L6	±5%, 0402 Multilayer chip inductor	27	12	nH	Sunlord SDCL
L7	±5%, 0402 Multilayer chip inductor	27	12	nH	Sunlord SDCL
L8	±5%, 0402 Multilayer chip inductor	68	18	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26		MHz	EPSON
U1	CMT2300A, Ultra Low Power Sub-1GHz RF Transceiver	-		-	CMOSTEK
U2	AS179, PHEMT GaAs IC SPDT Switch	-		-	SKYWORKS
R1	±5%, 0402	2.2	kΩ		
R2	±5%, 0402	2.2	kΩ		

4. Function Descriptions

CMT2300A is an ultra-low power, high performance transceiver chip. It supports OOK, (G) FSK and (G) MSK. It is suitable for applications in the range from 140 to 1020 MHz. The product belongs to CMOSTEK NextGenRF™ series. The series includes transmitters, receivers and transceivers and other complete product lines. CMT2300A block diagram is as shown in the following figure.

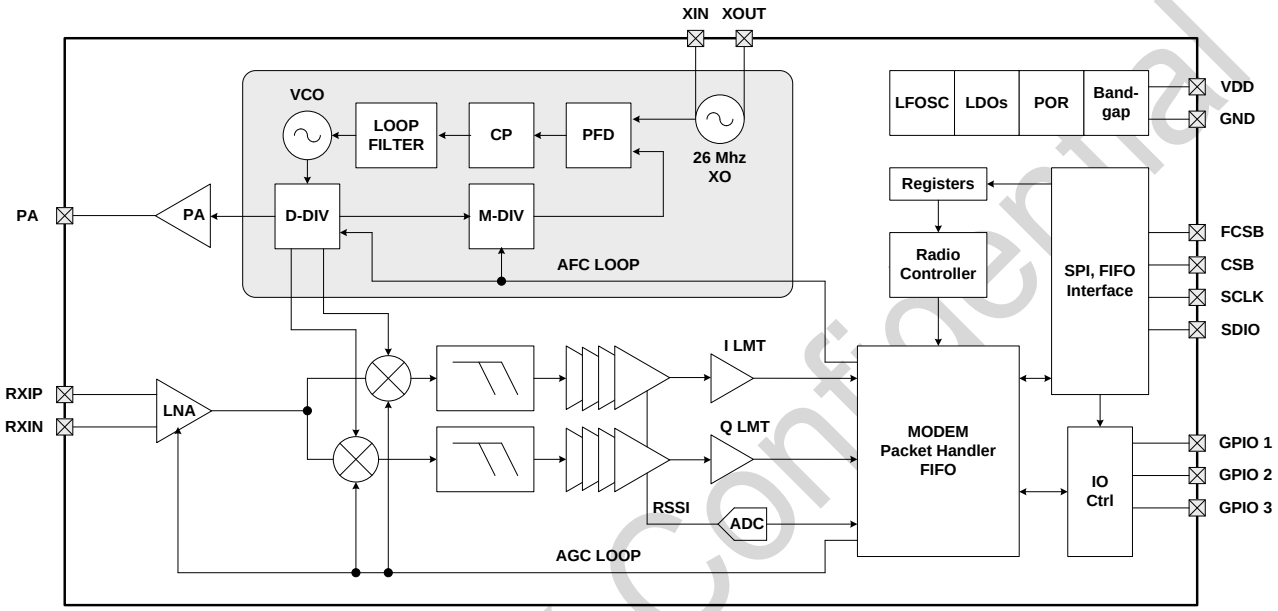


Figure 4. Functional Block Diagram

In the receiver part, the chip uses LNA+MIXER+IFFILTER+LIMITTER+PLL low-IF architecture to achieve the Sub-GHz wireless reception function. The chip uses PLL+PA architecture to achieve the Sub-GHz wireless transmitting function.

In the receiver system, the analog circuit mixes the RF signal to IF and converts the signal from analog to digital through the Limiter module, then outputs I/Q two single bit signals to the digital circuit for (G) FSK demodulation. At the same time, SARADC will convert the real-time RSSI signal to 8-bit digital signal, and sent them to the digital part for OOK demodulation and other processing. The digital circuit is responsible for mixing the intermediate frequency to zero frequency (Baseband) and performing a series of filtering and decision processing, while AFC and AGC control the analog circuit dynamically, finally the 1-bit original signal is demodulated. After demodulation, the signal will be sent to the decoder to decode and fill in the FIFO, or output to the PAD directly.

In the transmitter system, the digital circuitry will encode the data and then send them to the modulator (or send them to the modulator directly without encoding). The modulator will directly control the PLL and PA, modulate the data by (G) FSK or OOK and transmit them.

The chip provides the SPI communication port. The external MCU can configure the various functions by accessing to the register, control the main state machine, and access to the FIFO.

4.1 Transmitter

The transmitter is based on direct frequency synthesis technology. The carrier is generated by a low noise fractional-N frequency synthesizer. The modulated data is transmitted by an efficient single-ended power amplifier (PA). The output power can be read and written via registers, step by step from -20dBm to +20dBm with 1dB.

When the PA is switched fast, the varying input impedance will disturb the output frequency of the VCO instantaneously. The effect is called VCO pulling. It will generate the spurious and spurs on the spectrum around the desired carrier. The PA spurs can be reduced to a minimum instantaneously by the PA output power ramping. CMT2300A has a built-in PA ramping mechanism. When the PA Ramp is turned on, the PA output power can ramp the desired amplitude in a pre-configured rate, so as to reduce the spurs. In FSK mode, the signal can be filtered by a Gaussian Filter before transmitted, e.g. GFSK, which can reduce the spectral width and interference with neighboring channels.

According to different application requirements, the user can design a PA matching network to optimize the transmitting efficiency. The typical application schematic and the required BOM is shown in Chapter 3 "Typical application schematic". For more schematic details and layout guidelines, please refer to“AN141 CMT2300A Schematic and PCB Layout Design Guideline”.

The transmitter can operate in direct mode and package mode. In the direct mode, the data to be transmitted can be sent to the chip by the DIN pin and transmitted directly. In the package mode, the data can be pre-loaded into the TX FIFO in STBY state, and transmitted together with other package elements.

4.2 Receiver

CMT2300A has a built-in ultra-low power, high performance low-IF OOK, FSK receiver. The RF signal induced by the antenna is amplified by a low noise amplifier, and is converted to an intermediate frequency by an orthogonal mixer. The signal is filtered by the image rejection filter, and is amplified by the limiting amplifier and then sent to the digital domain for digital demodulation.
During power on reset (POR) each analog block is calibrated to the internal reference voltage. This allows the chip to remain its best performance at different temperatures and voltages. Baseband filtering and demodulation is done by the digital demodulator. The AGC loop adjust the system gain by the broadband power detector and attenuation network nearby LNA, so as to obtain the best system linearity, selectivity, sensitivity and other performance.

Leveraging CMOSTEK's low power design technology, the receiver consumes only a very low power when it is turned on. The periodic operation mode and wake up function can further reduce the average power consumption of the system in the application with strict requirements of power consumption.

Similar to the transmitter, the CMT2300A receiver can operate in direct mode and packet mode. In the direct mode, the demodulator output data can be directly output through the DOUT pin of the chip. DOUT can be assigned to GPIO1/2/3. In the packet mode, the demodulator data output is sent to the data packet handler, get decoded and is filled in the FIFO. MCU can read the FIFO by the SPI interface.

4.3 Additional Functions

4.3.1 Power-On Reset (POR)

The Power-On Reset circuit detect the change of the VDD power supply, and generate the reset signal for the entire CMT2300A system. After the POR, the MCU must go through the initialization process and re-configure the CMT2300A. There are two circumstances those will lead to the generation of POR.

The first case is a very short and sudden decrease of VDD. The POR triggering condition is, VDD dramatically decreases by 0.9V +/- 20% (e.g. 0.72V – 1.08V) within less than 2 us. To be noticed, it detects a decreasing amplitude of the VDD, not the absolute value of VDD as shown in the below figure.

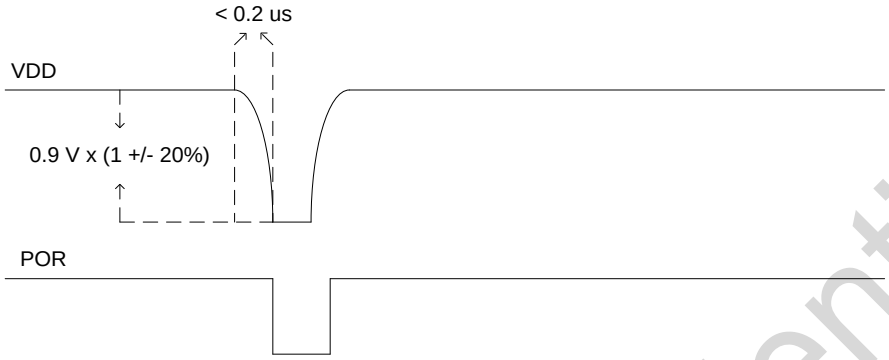


Figure 5. Sudden Decrease of VDD lead to Generation of POR

The second case is, a slow decrease of the VDD. The POR triggering condition is, VDD decreases to 1.45V +/- 20% (e.g. 1.16V – 1.74V) within a time more than or equal to 2 us. To be noticed, it detects an absolute value of VDD, not a decreasing amplitude.

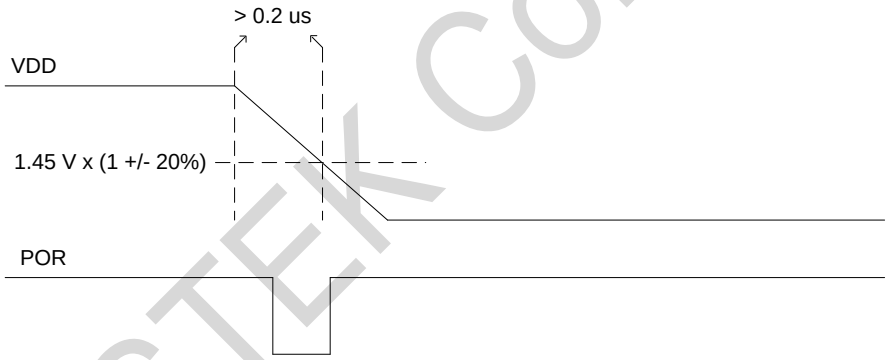


Figure 6. Slow Decrease of VDD lead to Generation of POR

4.3.2 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop as well as a system clock for the digital circuits. The value of load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CL, in order to make the crystal accurately oscillate at 26 MHz.

$$C_L = \frac{1}{1/C15 + 1/C16} + C_{par} + 2.5pF$$

C15 and C16 are the load capacitances at both ends of the crystal. Cpar is the parasitic capacitance on the PCB. Each crystal pin has 5pF internal parasitic capacitance, together is equivalent to 2.5pF. The equivalent series resistance of the crystal must be within the specifications so that the crystal can have a reliable vibration. Also, an external signal source can be connected to the XI pin to replace the conventional crystal. The recommended peak value of this clock signal is from 300mV to 700mV. The clock is coupled to XI pin via a blocking capacitor.

4.3.3 Sleep Timer

The CMT2300A integrates a sleep timer driven by 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer wakes the chip from sleep periodically. When the chip operates in a duty cycle mode, the sleep time can be configured from 0.03125 ms to 41922560 ms. Due to the low power oscillator frequency will change with the temperature and voltage drift, it will be automatically calibrated during power on and will be periodically calibrated since then. These calibrations will keep the frequency tolerance of the oscillator within + 1%.

4.3.4 Low Battery Detection

The chip sets up low voltage detection.When the chip is tuned to a certain frequency, the test is performed once.Frequency tuning occurs when the chip jumps from the SLEEP/STBY state to the RFS/TFS/TX/RX state. The result can be read by the LBD_VALUE register.

4.3.5 Received Signal Strength Indicator(RSSI)

RSSI is used to evaluate the signal strength inside the channel. The cascaded I/Q logarithmic amplifier amplifies the signal before it is sent to the demodulator. The logarithmic amplifier of I channels and Q channel contains the received signal indicator, in which the DC voltage is generated is proportional to the input signal strength. The output of RSSI is the sum of the values of the two channels' signals. The output has 80dB dynamic range above the sensitivity. After the RSSI output is sampled by the ADC and filtered by a SAR FILTER and a RSSI AVG FILTER. The order of the average filter can be set by RSSI_AVG_MODE<2:0>. The code value is translated into dBm value after filtering. Users can read the register RSSI_CODE<7:0> to obtain the RSSI code value, or RSSI_DBM<7:0> to obtain the dBm value. By setting the register RSSI_DET_SEL<1:0> Users can determine whether the RSSI is output to the MCU in real time, or latched at the instance when the preamble, sync, or the whole packet is received.

Also, CMT2300A allows the user to setup a threshold by RSSI_TRIG_TH<7:0> to compare with the real-time RSSI value. If the RSSI is larger than the threshold it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, of the receive time extending condition in the super- low power (SLP) mode

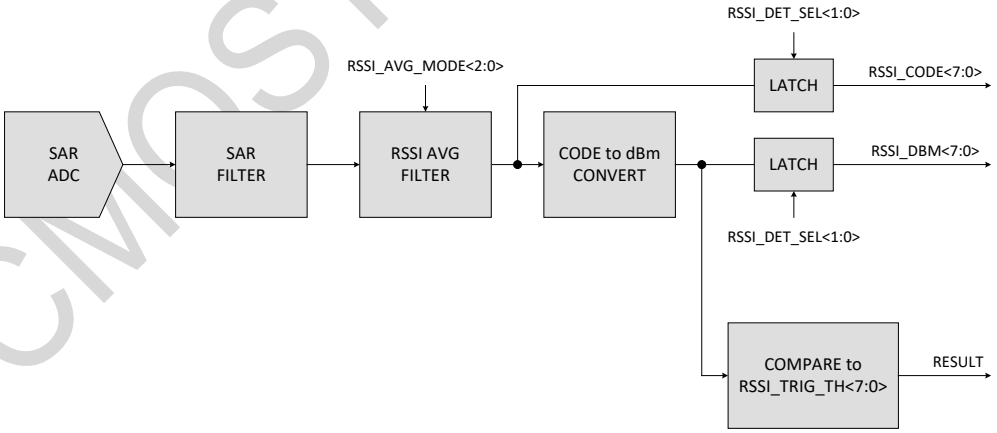


Figure 7. RSSI detection and comparison circuit

CMT2300A has done a certain degree of calibration before delivery. In order to obtain more accurate RSSI measurement results, the user needs to recalibrate the RSSI circuit in their dedicated applications. For further information, please refer to the "AN144-CMT2300AW RSSI Usage Guideline".

4.3.6 Phase Jump Detector（PJD）

PJD is Phase Jump Detector. When the chip is in FSK demodulation, it can automatically observe the phase jump characteristics of the received signal to determine whether it is a wanted signal or an unwanted noise.

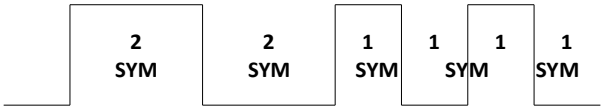


Figure 8. Received signal jump diagram

The PJD mechanism defines that the input signal switching from 0 to 1 or from 1 to 0 is a phase jump. Users can configure the PJD_WIN_SEL<1:0> to determine the number of detected jumps for the PJD to identify a wanted signal .As shown in the above figure, in total 8 symbols are received. But the phase jump only appeared 6 times. Therefore, the number of jumpsis not equal to the number of symbols. Only when a preamble is received they are equal .In general, the more jumps are used to identify the signal, the more reliable they result is; the less jumps are used, the faster the result is obtained. If the RX time is set to a relatively short period, it is necessary to reduce the number of jumps to meet the timing requirements. Normally, 4 jumps allow pretty reliable result, e.g. the chip will not mistakenly treat an incoming noise as a wanted signal, and vice versa will not treat a wanted signal as noise.

Detecting the phase jump of a signal, is identical to detect whether the signal has the expected data rate. In fact, at the same time, the PJD will also detect the FSK deviation and see if it is legal, as well as to see if the SNR is over 7 dB. With these three parameters the PJD is able to make a very reliable judgment. If the signal is wanted it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, or the receive time extending condition in the super low power (SLP) mode. In direct data mode, by setting the DOUT_MUTE register bit to 1, the PJD can mute the FSK demodulated data output while there is not wanted signal received.

The PJD technique is similar to the traditional carrier sense technique, but more reliable. While users combine the RSSI detection and PJD technique, they can precisely identify the status of the current channel.

4.3.7 Automatic Frequency Control (AFC)

The AFC mechanism allows the receiver to minimize the frequency error between the TX and RX in a very short time once a wanted signal comes in. This helps the receiver to maintain its highest sensitivity performance. CMT2300A has the most advanced AFC technology. Compare with the other competitors, within the same bandwidth, CMT2300A can identify larger frequency error, and remove the error in a much shorter time (8-10 symbols).

Normally the frequency error between the TX and RX is caused by the crystal oscillators used in both sides. CMT2300A allows the user to fill in the value of crystal tolerance (in PPM) on RFPDK. Based on the crystal tolerance, the RFPDK will calculate the AFC range while minimizing the receiver bandwidth (to maintain the best performance). Due to the excellent performance of the AFC, it provides a good solution to the crystal aging problem which would lead to more frequency error as time goes by.
Therefore, compare to other similar transceiver chips, CMT2300A can solve more severe crystal aging problem and effectively extend the life time of the product.

4.3.8 Clock Data Recovery (CDR)

The basic task of a CDR system is to recover the clock signal that is synchronized with the symbol rate, while receiving the data. Not only for decoding inside the chip, but also for outputting the synchronized clock to GPIO for users to sample the data. So CDR's task is simple and important. If the recovered clock frequency is in error with the actual symbol rate, it will cause data acquisition errors at the time of reception.

CMT2300A has designed three types of CDR systems, as follows:

1. **COUNTING system**–The system is designed for the symbol rates to be more accurate. If the symbol rate is 100% aligned, the unlimited length of 0 can be received continuously without error.

2. **TRACING system** –The system is designed to correct the symbol rate error. It has the tracking function. It can automatically detect the symbol rate transmitted by TX, and adjust quickly the local symbol rate of RX at the same time, so as to minimize the error between them. The system can withstand up to 15.6% or symbol rate error. Other similar products in the industry cannot reach this level.

3. **MANCHESTER system** –This system evolves from the COUNTING system. The basic feature is the same. The only difference is that the system is specially designed for Manchester codec. Special processing can be done when the TX symbol rate has unexpected changes.

4.3.9 Fast Frequency Hopping

The mechanism of fast frequency hopping is, based on the frequency configured on the RFPDFK, for instance 433.92 MHz, during applications the MCU can simply change 1 or 2 registers to quickly switch to another frequency channel. This simplify the way of change the RX or TX frequency in multiple channels application.

$$\mathbf{FREQ} = \mathbf{Base\ Freq} + \mathbf{2.5\ kHz} \times \mathbf{FH\_OFFSET} < \mathbf{7:0} > \times \mathbf{FH\_CHANNEL} < \mathbf{7:0} >$$

In general, the user can configure FH_OFFSET<7:0>during the chip initialization process. And then in the application, the user can switch the channel by changing FH_CHANNEL<7:0>.

When users need to use the fast frequency hopping in the RX mode, in some particular frequency points, one parameter of the AFC circuit must be re-configured. Please refer to “AN197-CMT2300A-CMT2119B-CMT2219B fast frequency hopping” and “CMT2300A-CMT2219B frequency hopping calculation tool” for more details.

5. Chip Operation

5.1 SPI Interface

The chip communicates with the outside through the 4-wire SPI interface. The CSB is the active-low chip select signal for accessing to the registers. The FCSB is the active-low select signal for accessing to the FIFO. They cannot be set to low at the same time. The SCLK is the serial clock. Its highest speed is 5MHz.The chip itself and the external MCU send the data at the falling edge of SCLK and capture the data at the rising edge of SCLK. The SDA is a bidirectional pin for input and output data. The address and data are transferred starting from the MSB.

When accessing to the register, CSB is pulled low. A R/W bit is sent first, followed by a 7-bit register address. After the external MCU pulls down the CSB, it must wait for at least half a SCL cycle, and then send the R/W bit. After the MCU sends out the last falling edge of SCLK, it must wait for at least half a SCLK cycle, and then pull the CSB high.

To be noticed, when reading a register, MCU and CMT2300A will have to switch the direction of their IO (SDIO) between the address bit 0 and the data bit 7. It is required that the MCU switches the IO to input mode before send out the falling edge of the SCLK; CMT2300A should switch the IO to output mode after it has seen the falling edge of the SCLK. This avoids data contention of the SDIO (both of the MCU and CMT2300A set the SDIO to output mode at the same time), which would cause unexpected electrical problem.

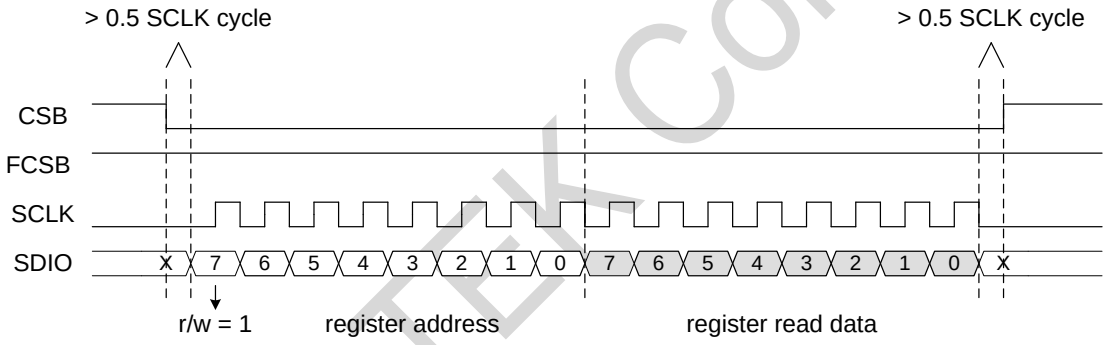


Figure 9. SPI read register timing

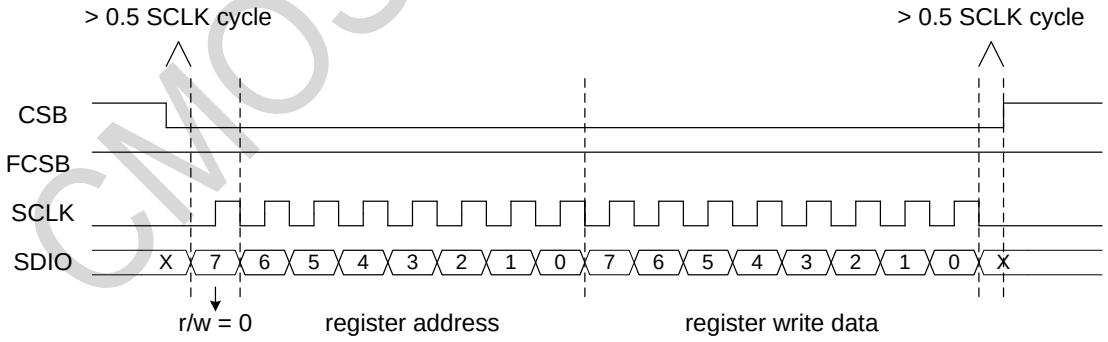


Figure 10. SPI write register timing

5.2 FIFO

CMT2300A provides two separated 32-byte FIFO by default. They are used for RX and TX, respectively. Users can also set FIFO_MARGE_EN to 1 to merge the two separated FIFO into one 64-byte FIFO. It can be used both under TX and RX. By configuring the FIFO_RX_TX_SEL to indicate whether it is currently used as TX FIFO or RX FIFO. When the two FIFO are not merged, users can fill in the TX FIFO while the RX FIFO is used to receive data in the RX mode.

The FIFO can be accessed via the SPI interface. The user can clear the FIFO by setting FIFO_CLR_TXor FIFO_CLR_RX to 1. Also, the user can re-send the old data in the TX FIFO by setting FIFO_RESTORE to 1, without the need of re-filling the data.

5.2.1 FIFO Read Operation

When the MCU accesses to the FIFO, the user must first configure a few registers to setup the FIFO read/write mode, as well as some other working mode. The details are introduced in “AN143-CMT2219B FIFO and Data Packet Usage Guideline”. Here is the read-write timing diagram. Note that there is a slight difference in the control of the FCSB for accessing to the FIFO and the control of the CSB for accessing to the register. When the MCU starts to access to the FIFO, FCSB must be pulled down 1-clock cycle at first, and then send the rising edge of SCL. After the last falling edge of SCL is sent, the MCU must wait at least 2 us to pull up the FCSB. Between the adjacent read/write operations, the FCSB must be pulled high for 4us at least. When writing the FIFO, the first bit data must be ready 0.5 clock cycles before sending the first rising edge of SCL.

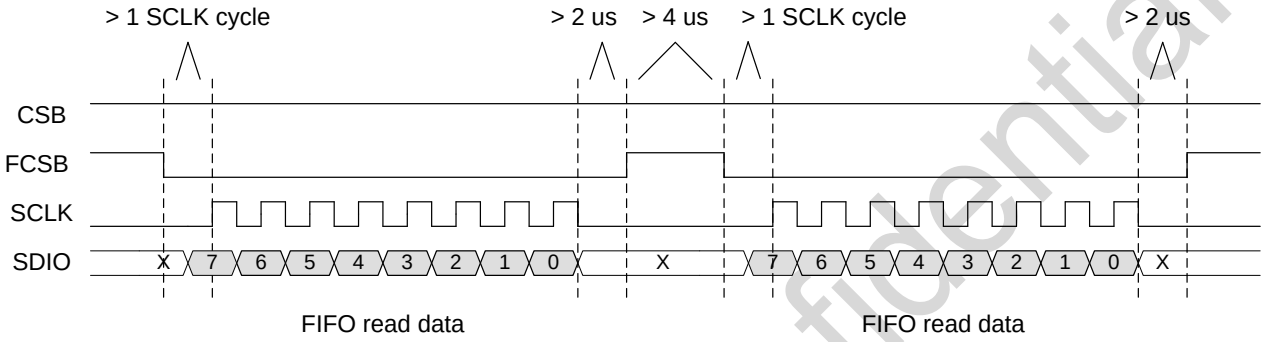


Figure 11. SPI read FIFO timing

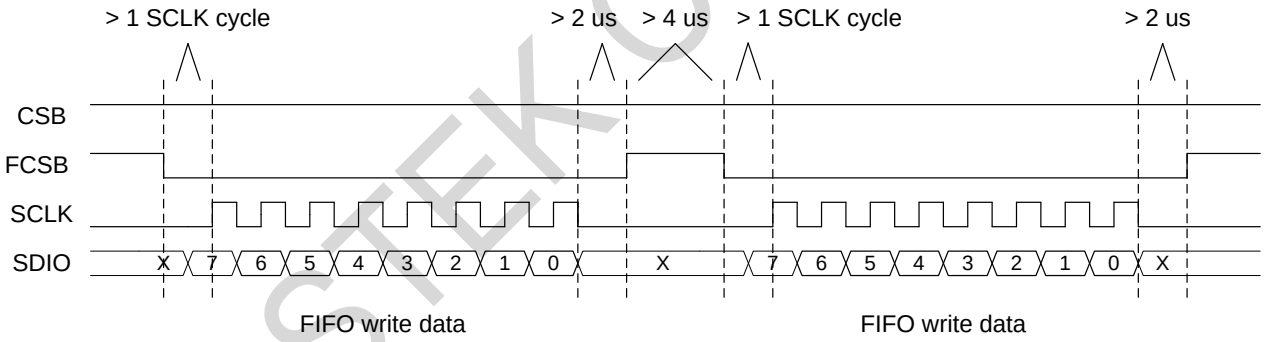


Figure 12. SPI write FIFO timing

5.2.2 FIFO Associated Interrupt

CMT2300A provides rich interrupt sources associated with the FIFO. The interrupt timing for Tx and Rx FIFO is shown below:

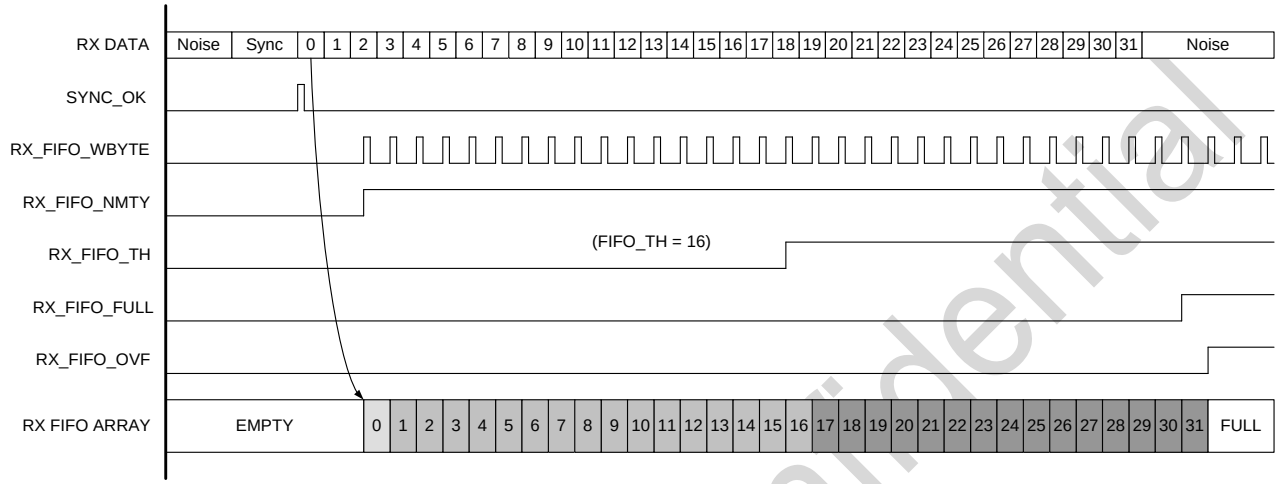


Figure 13. CMT2300ARX FIFO interrupt timing diagram

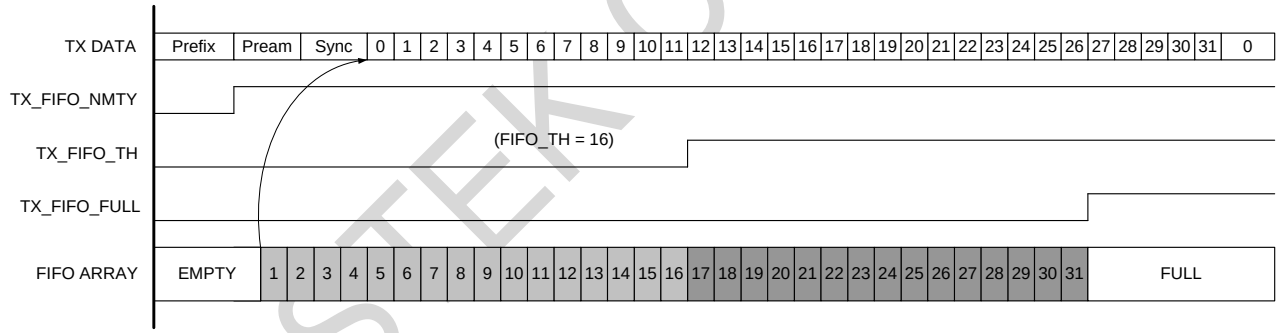


Figure 14. CMT2300A TX FIFO interrupt timing diagram

5.3 Operation State, Timing and Power Consumption

5.3.1 Startup Timing

After the chip VDD is powered up, the chip usually needs to wait about 1ms, then POR will release. After the release of the POR, the crystal will start, the start time is N ms, depending on the characteristics of the crystal itself. After starting, the user need to wait for the crystal settled, then the system starts working. The default setting is 2.48 ms. This time can be modified by writing XTAL_STB_TIME <2:0> afterword (it has to be longer than the crystal inherent settling time). The chip stays in IDLE state until the crystal is settled. After the crystal is settled, the chip perform calibration of each module and stay in SLEEP state after then to wait for initialization configuration by user. The chip will back to IDLE state and redo startup steps upon reset at anytime.

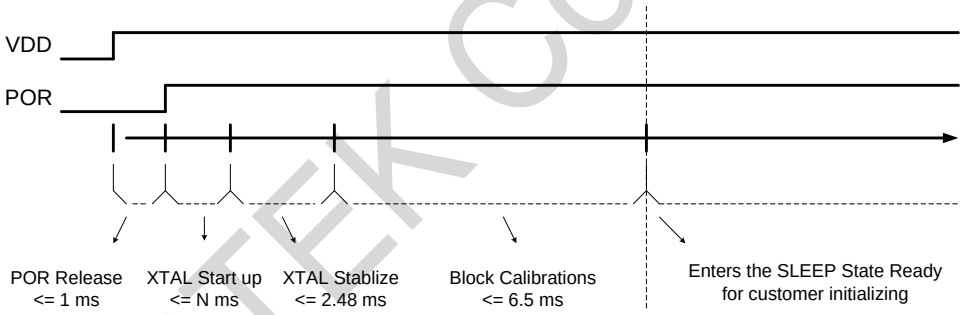


Figure 15. Power-on Timing

The chip enters SLEEP state after calibration. From then on, the MCU can control the chip to switch to different operation states through setting the register CHIP_MODE_SWT<7:0>.

5.3.2 Operation State

CMT2300A has 7 operation states: IDLE, SLEEP, STBY, RFS, RX, TFS and TX, as shown below.

Table 16. CMT2300A state and corresponding active module

State	Binary code	Switch command	Active Modules	Optional Moduels
IDLE	0000	soft_rst	SPI, POR	None
SLEEP	0001	go_sleep	SPI, POR, FIFO	LFOSC, Sleep Timer
STBY	0010	go_stby	SPI, POR, XTAL, FIFO	CLKO
RFS	0011	go_rfs	SPI, POR, XTAL, PLL, FIFO	CLKO
TFS	0100	go_tfs	SPI, POR, XTAL, PLL, FIFO	CLKO
RX	0101	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+IF, FIFO	CLKO, RX Timer
TX	0110	go_tx	SPI, POR, XTAL, PLL, PA, FIFO	CLKO

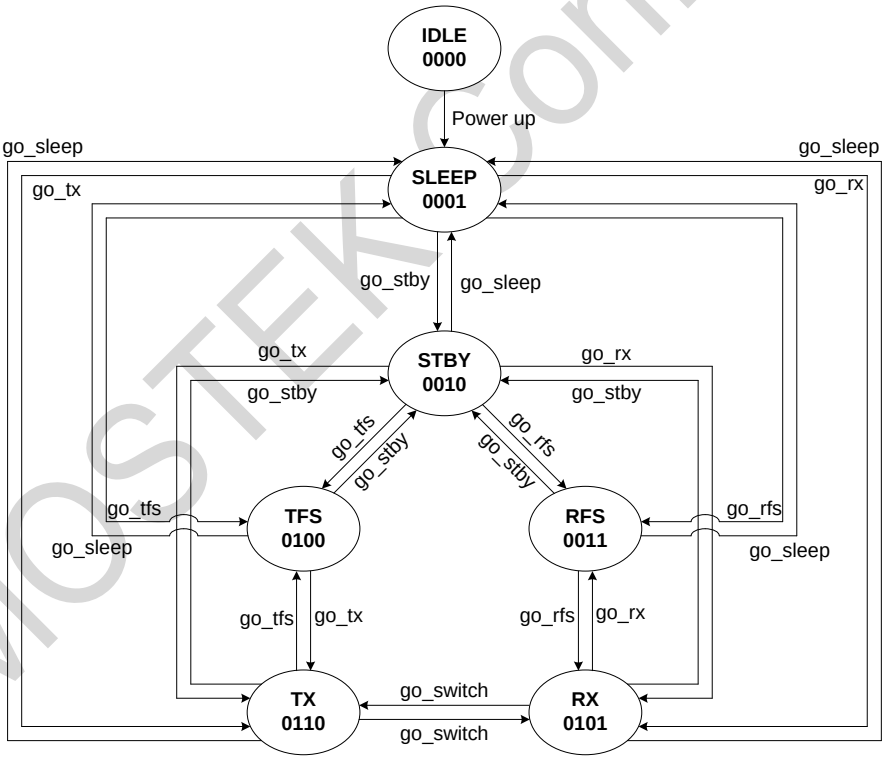


Figure 16. State Switch Diagram

■ **SLEEP State**

The chip power consumption is the lowest in SLEEP state, and almost all the modules are turned off. SPI is open, the registers of the configuration bank and control bank 1 will be saved, and the contents filled in the FIFO before will remain unchanged.

However, the user cannot operate the FIFO and cannot change the contents of the register. If the user opens the wake-up function, the LFOSC and the sleep counter will turn on and start working. The time required to switch from IDLE to SLEEP is the power up time. Switch from other state to SLEEP will be completed immediately.

- **STBY State**

In STBY state, the crystal is turned on, the LDO of the digital circuit will also be turned on, the current will be slightly increased, and the FIFO can be operated. The user can choose whether to output CLKO (system clock) to PIN. Because the crystal and LDO is turned on, compared to the SLEEP, the time switching from the STBY to transmitting or receiving will be relatively short. Switching from SLEEP to STBY will be completed after the crystal is turned on and settled. Switching from other state to STBY will be completed immediately.

- **RFS State**

RFS is a transition state before switching to RX. Except that the receiver RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the RX frequency, RFS cannot switch to TX. Switching from STBY to RFS probably requires PLL calibration and stability time of 350us. Switching from SLEEP to RFS needs to add the crystal start-up and stability time. Switching from other state to RFS will be completed immediately.

- **TFS State**

TFS is a transition state before switching to TX. Except that the transmitter RF module is off, the other modules are turned on, and the current will be larger than STBY. Because PLL has been locked in the TX frequency, TFS cannot switch to RX. Switching from STBY to TFS probably requires PLL calibration and stability time of 350us. Switching from SLEEP to TFS needs to add the crystal start-up and settled time. Switching from other state to TFS will be completed immediately.

- **RX State**

All modules on the receiver will be opened in RX state. Switching from RFS to RX requires only 20us. Switching from STBY to RX needs to add the PLL calibration and settled time of 350us. Switching from SLEEP to RX needs to add the crystal start-up and settled time. TX can be quickly switched to RX by sending go_switch command. Whether the TX and RX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350us to switch successfully.

- **TX State**

All modules on the transmitter will be opened in TX state. Switching from TFS to TX requires only 20us. Switching from STBY to TX needs to add the PLL calibration and settled time of 350us. Switching from SLEEP to TX needs to add the crystal start-up and settled time. RX can be quickly switched to TX by sending go_switch command. Whether the RX and TX setting frequency is the same, the user need to wait for the PLL re-calibration and settled time of 350us to switch successfully.

5.4 GPIO and Interrupt

CMT2300A has 3 GPIO ports. Each GPIO can be configured as a different input or output. CMT2300A has 2 interrupt ports. They can be configured to different GPIO outputs.

Table 17. CMT2300A GPIO

Pin No.	Name	I/O	Function
16	GPIO1	IO	Configured as: DOUT/DIN, INT1, INT2, DCLK (TX/RX), RF_SWT
15	GPIO2	IO	Configured as: INT1, INT2, DOUT/DIN, DCLK (TX/RX), RF_SWT
8	GPIO3	IO	Configured as: CLKO, DOUT/DIN, INT2, DCLK (TX/RX)

Interrupt mapping table is as below. INT1 and INT2 mapping is the same. Take INT1 as an example.

Table 18. CMT2300A interrupt mapping table

Name	INT1_SEL	Descriptions	Clearing methods
RX_ACTIVE	00000	Indicates the chip is entering RX and is already in RX. It is 1 in PLL Tuning and RX state, and it is 0 in the other states.	Auto
TX_ACTIVE	00001	Indicates the chip is entering TX and is already in TX. It is 1 in PLL tuning and TX state, and it is 0 in the other states.	Auto
RSSI_VLD	00010	Indicates whether the RSSI is active.	Auto
PREAM_OK	00011	Indicates that the Preamble is received successfully.	by MCU
SYNC_OK	00100	Indicates that the Sync Word is received successfully.	by MCU
NODE_OK	00101	Indicates that the Node ID is received successfully.	by MCU
CRC_OK	00110	Indicates that the CRC for the current packet is correct.	by MCU
PKT_OK	00111	Indicates that a packet has been received.	by MCU
SL_TMO	01000	Indicates that the SLEEP counter timed out.	by MCU
RX_TMO	01001	Indicates that the RX counter timed out.	by MCU
TX_DONE	01010	Indicates that the TX operation is completed.	by MCU
RX_FIFO_NMTY	01011	Indicates that the RX FIFO is not empty.	Auto
RX_FIFO_TH	01100	Indicates the number of unread bytes of the RX FIFO is over FIFO TH	Auto
RX_FIFO_FULL	01101	Indicates RX FIFO is full.	Auto
RX_FIFO_WBYTE	01110	Indicates each time a byte is written to the RX FIFO. Itis a pulse.	Auto
RX_FIFO_OVF	01111	indicates RX FIFO is overflow	Auto
TX_FIFO_NMTY	10000	Indicates that TX FIFO is not empty	Auto
TX_FIFO_TH	10001	Indicates the number of unread bytes of the TX FIFO is over FIFO TH.	Auto
TX_FIFO_FULL	10010	Indicates TX FIFO is full.	Auto
STATE_IS_STBY	10011	Indicates that the current state is STBY.	Auto
STATE_IS_FS	10100	Indicates that the current state is RFS or TFS.	Auto
STATE_IS_RX	10101	Indicates that the current state is RX.	Auto
STATE_IS_TX	10110	Indicates that the current state is TX.	Auto
LBD	10111	Indicates that low battery is detected (VDD is lower than TH)	Auto
TRX_ACTIVE	11000	Indicates the chip is entering TX or RX and is already in TX or RX. It is 1 in PLL tuning, TX or RX state, and it is 0 in the other states.	Auto
PKT_DONE	11001	Indicates that the current packet has been received, covering 4 possible different situations. 1. The packet is received completely and correctly. 2. Manchester decoding has error. Decoder is automatically reset. 3. NODE ID receiving has error. Decoder is automatically reset. 4. Signal collision occurred. Decoder is not reset, waiting for MCU to response.	by MCU

By default, Interrupt is active high (logic 1 is valid). Users can set the INT_POLAR register bit to 1 to make all interrupts active low (logic 0 is valid).Taking INT1 as an example, the control and sources selection of all the available interrupts is shown below. The control and mapping of INT1 and INT2 are the same.

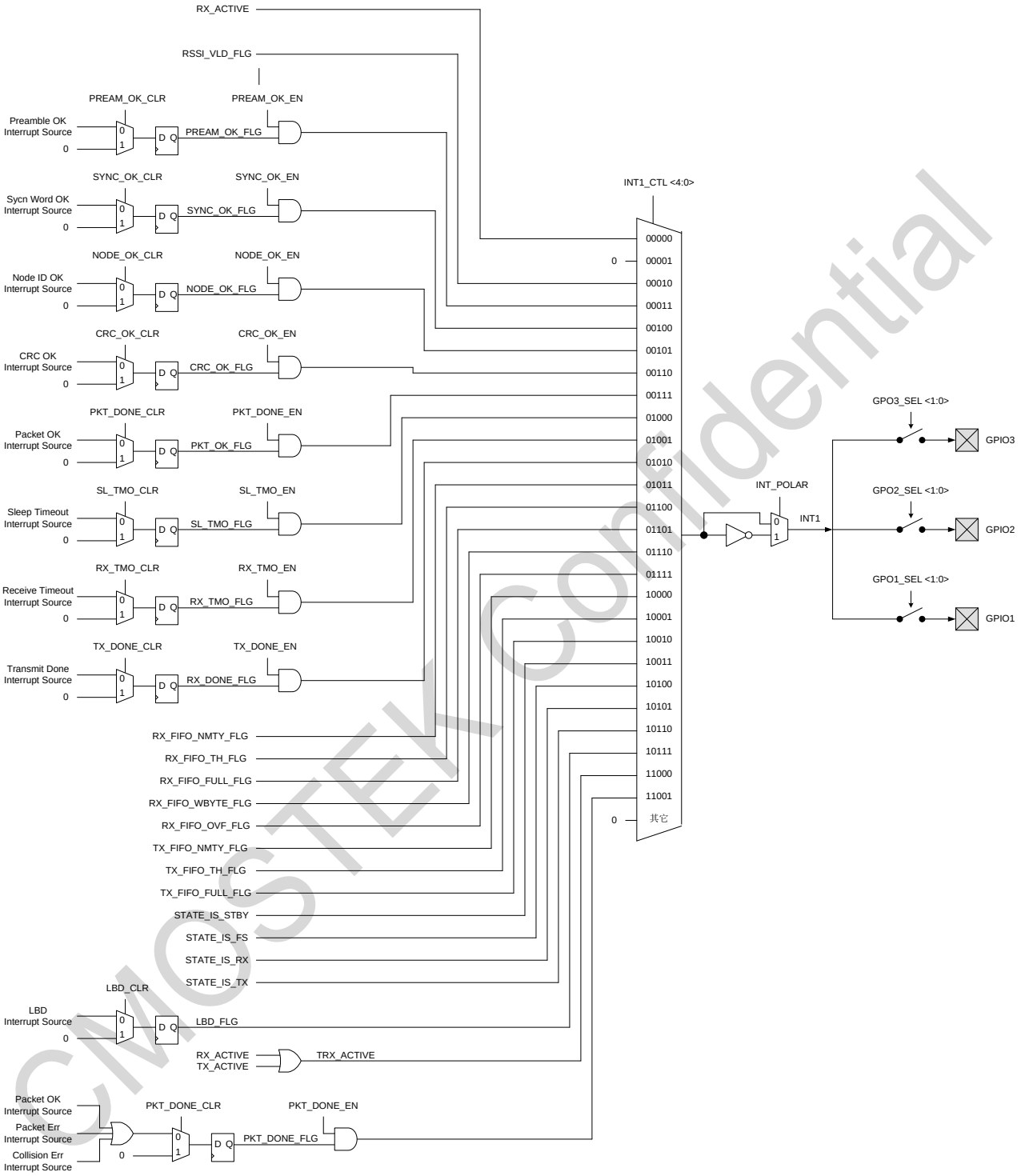


Figure 17. CMT2300A INT1 interrupt mapping diagram

6. Packet Handler

CMT2300A supports direct mode and packet mode:

- Direct Mode – In Rx mode, only supports preamble and sync detection, FIFO does not work, demodulated data sent out from GPIO. In Tx mode, only supports transmitting the data input from GPIO.
- Packet Mode – Supports all packet formats, demodulated data is stored in FIFO, accessed by SPI.

6.1 Direct Mode

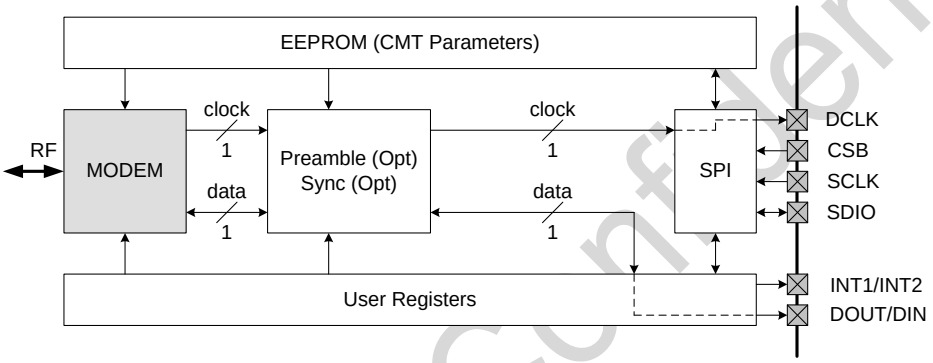


Figure 5. Direct mode data path

Rx processing

In direct mode, the data from the demodulator is sent directly to the external MCU via the DOUT pin. DOUT can be set to GPIO1, 2 or 3. The typicalRX direct mode control sequence for the MCU is:

1. Configures GPIOsusing theCUS_IO_SEL register.
2. Configures DATA_MODE = 0.
3. Send the go_rx command.
4. Capture the data from DOUT continuously.
5. Send the go_sleep/go_stby/go_rfs command to stop receiving and save the power.

Tx processing

In the direct mode, the data to be transmitted is sent directly to the chip from the external MCU by via DIN pin. The data rate is determined by the MCU but must be less than +/- 30% of the data rate configured on the RFPDK. The typical TX direct mode control sequence for the MCU is:

1. Set register TX_DIN_EN to 1 to enable DIN on GPIO.
2. Set TX_DIN_SEL to 0 to configure GPIO1 as DIN, or 1 to configure GPIO2 as DIN.
3. Send the go_tx command,send in the data to the DIN pinwith the desired data rate, the data is transmitted immediately.

4. Send the go_sleep/go_stby/go_rfs command to stop transmission and save the power.

6.2 Packet Mode

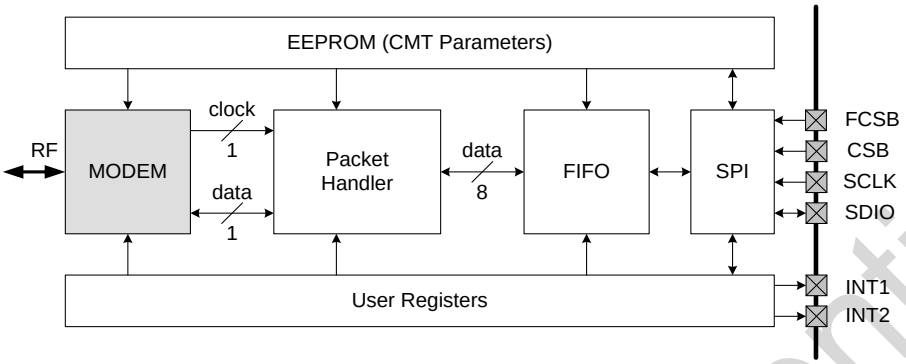


Figure 6. Packet mode data path

The packet handler supports the classic and more flexible packet format in both TX and RX mode. It includes variable packet format (Length in front of the Node ID), variable packet format (Length in the back of the Node ID) and fixed packet format. Each element in the packet supports flexible configurations, as shown below.

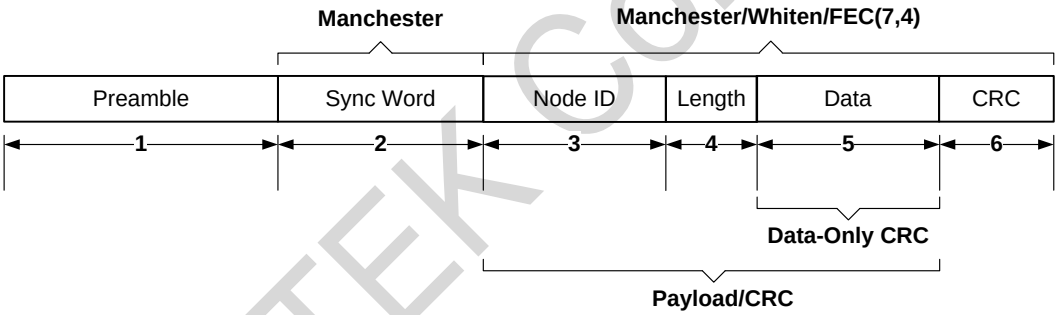


Figure 20. Variable length packet (Length in front of Node ID)

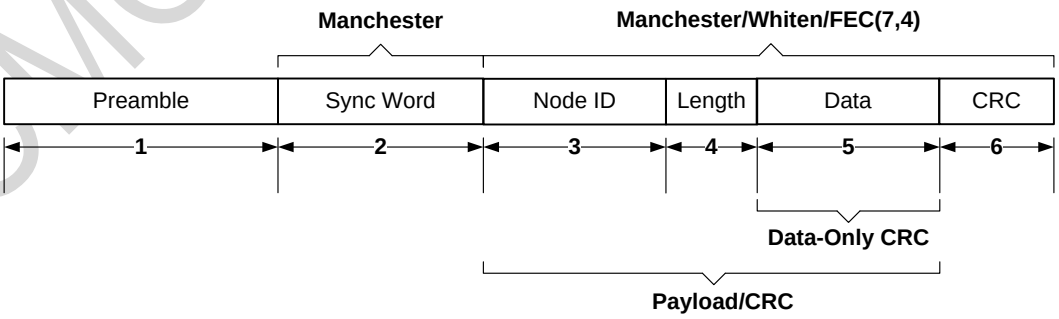


Figure 21. Variable length packet (Length behind Node ID)

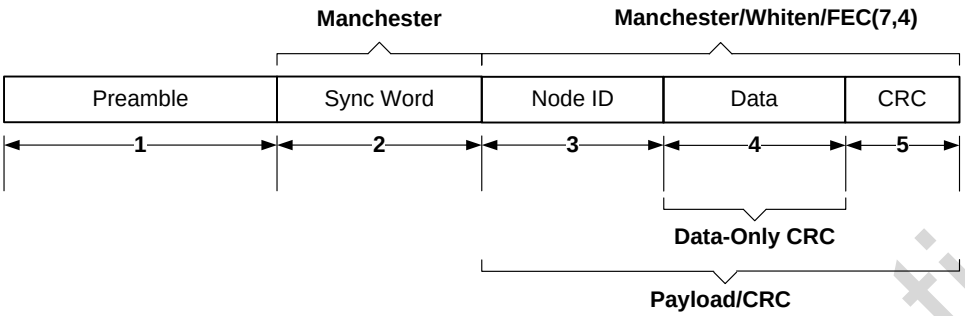


Figure 22. Fixed length packet

Rx processing

In the packet mode, the output data from the demodulator will be transferred to the packet handler for decoding, and then filled in the FIFO. The packet handler provides a variety of decoding mechanisms and options to determine the validity of the data. These can reduce the work load of the MCU. The typical package mode control sequence for the MCU is:

1. Configures GPIO using the CUS_IO_SEL register.
2. Setup the interrupts usingCUS_INT1_CTL, CUS_INT2_CTL and CUS_INT_EN registers.
3. Send the go_rx command.
4. Reads the RX FIFO according to the relevant interrupts.
5. Sends the go_sleep/go_stby/go_rfs command to stop the receiving and save the power.
6. Clears the packet interrupts using CUS_ INT_CLR1 and CUS_INT_CLR2 registers.

Tx processing

In the packet mode, MCU can fill the data in the FIFO in advance in the STBY and TFS state, or fill them in the FIFO while the chip sends the data, or use the combination of the above two methods. The typical Txpacket mode control sequence for the MCU is:

1. Configures GPIO usingthe CUS_IO_SEL register
2. Sends go_stby/go_tfs command when the data is filled in FIFO in advance.
3. Sends go_tx command.
4. Writes the data into FIFO according to the relevant interrupt status.
5. Sends go_sleep/go_stby/go_rfs command to save power.

CMT2300A has rich configurable hardware resources of FIFO, packet and their interrupts, which makes it compatible with most of the similar RF products in the market. For more details please refer to the interface of RFPDK and “AN143-CMT2300A FIFO and Data Packet Usage Guideline”.

7. Low Power Operation

7.1 Duty Cycle Operation Mode

CMT2300A makes the Tx and Rx work in duty cycle operation mode to save the power consumption. Among them, the Rx Duty Cycle can be classified into the following 5 modes.

Fully manual control.

1. Automatic SLEEP wakeup, switch to manual control.
2. Automatic SLEEP wakeup, automatically enter to RX, manually exit RX.
3. Automatic SLEEP wakeup, manually enter RX, automatically exit RX.
4. Fully automatic receive and sleep control.

The Tx Duty Cycle can be divided into the following 3 modes.

1. Manually enter TX, automatically exit TX
2. Automatic SLEEP wakeup, manually enter TX, automatically exit TX
3. Fully automatic transmit and sleep control

7.2 Super-low Power Rx Mode

The CMT2300A provides a series of options helping users achieving super-low power (SLP) Rx upon different application requirements. All these options are available only when RX_TIMER_EN is set as 1, namely Rx counter is active. The core function of SLP Rx is to reduce Rx time to the best during no-signal period meanwhile properly extend Rx time during signal existing time, then to reach stable Rx with minimum power consumption.

In general, traditional short-range wireless transceiver systems apply the solution as shown in the below figure to fulfill low-power transceiver. Based on the solution, the CMT2300A extends 13 solutions with better power consumption performance. Among them, a fundamental solution by setting RX_EXTEND_MODE<3:0> to 0 is shown in the below figure.

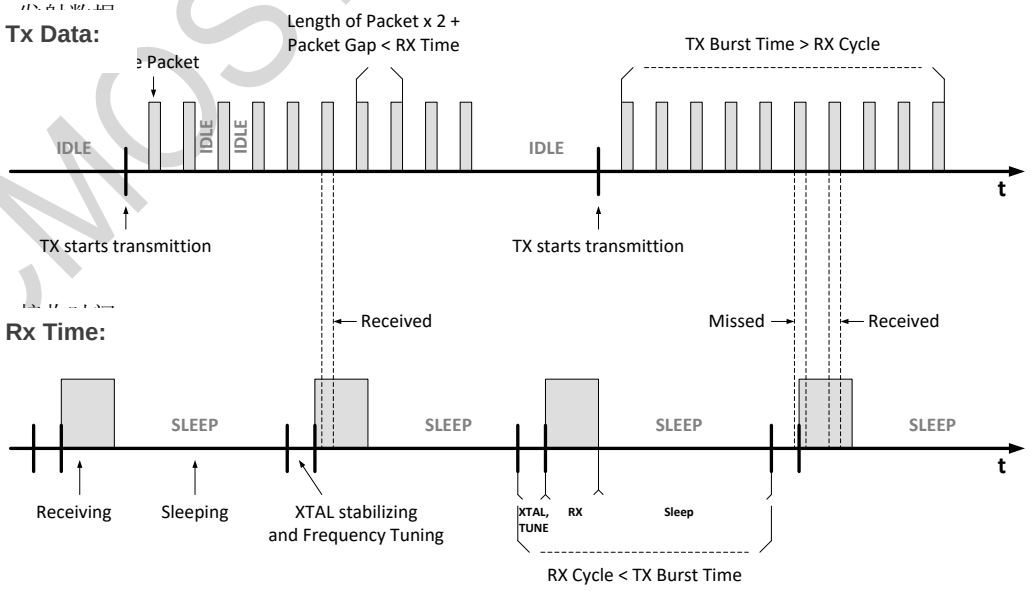


Figure 23. Basic low-power receiver scheme

The traditional low-power transceiver solution and the 13 extended low-power solutions based on it are listed in the below table.

Table 19. Low-power Rx mode

No.	Rx Extended Methods	Rx Extended Condition
0	No Rx extension is supported. Exit Rx state as soon as T1 timed out.	None
1	Once meet the Rx extended condition during T1, leave T1 and pass the control authority to MCU.	RSSI_VLD is valid.
2		PREAM_OK is valid.
3		RSSI_VLD and PREAM_OK are valid simultaneously.
4	Once detect RSSI_VLD = 1 during T1, leave T1 and stays in Rx state, exit Rx state until RSSI_VLD = 0.	RSSI_VLD is valid.
5	Once meet the Rx extended condition during T1, switch to T2. Exit Rx as soon as T2 timed out.	RSSI_VLD is valid
6		PREAM_OK is valid
7		RSSI_VLDandPREAM_OK are valid simultaneously.
8		Any one of PREAM_OK or SYNC_OK is valid.
9		Any one of PREAM_OK or NODE_OK is valid.
10		Any one of PREAM_OK or SYNC_OK or NODE_OK is valid.
11	Once meet the Rx extended condition during T1, switch to T2. Leave T2 and pass the control authority to MCU as soon as SYNC is detected, otherwise exit Rx when T2 timed out.	RSSI_VLD is valid.
12		PREAM_OK is valid.
13		RSSI_VLD and PREAM_OK are valid simultaneously.

The T1 and T2 mentioned in the table refer to the RX T1 and the RX T2 time interval that can be set via the registers or RFPDK. The source of RSSI_VLD can be the comparison result of the RSSI or the detection result of the phase jump detector (PJD). For more details, please refer to “AN146-CMT2300AW Low Power Mode Usage Guideline”.

7.3 Receiver “Power VS Performance” Configuration

CMT2300A provides a set of registers to select the power consumption and sensitivity performance of the RF frontend circuit. The below table shows how they are configured:

Table 20. Low-power receiver mode

Current level	RF Performance	LMT_VTR<1:0>	MIXER_BIAS<1:0>	LNA_MODE<1:0>	LNA_BIAS<1:0>
Low	Low	2	2	1	1
Medium	Medium	2	2	1	2
High	High	1	2	3	2

8. User Register

CMT2300A is configured by writing in the registers. The register details are listed in the below table.

Table 21. CMT2300A Register Table

Addr		Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function
0x00	RW	CUS_CMT1	User does not need to understand the details, just directly export the register contents from the RFPDK								CMT Bank
0x01	RW	CUS_CMT2									
0x02	RW	CUS_CMT3									
0x03	RW	CUS_CMT4									
0x04	RW	CUS_CMT5									
0x05	RW	CUS_CMT6									
0x06	RW	CUS_CMT7									
0x07	RW	CUS_CMT8									
0x08	RW	CUS_CMT9									
0x09	RW	CUS_CMT10									
0x0A	RW	CUS_CMT11									
0x0B	RW	CUS_RSSI									
Addr		**Name**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Function**
0x0C	RW	CUS_SYS1	LMT_VTR[1:0]		MIXER_BIAS[1:0]		LNA_MODE[1:0]		LNA_BIAS[1:0]		System Bank
0x0D	RW	CUS_SYS2	LFOSC_RECAL_EN	LFOSC_CAL1_EN	LFOSC_CAL2_EN	RX_TIMER_EN	SLEEP_TIMER_EN	TX_DC_EN	RX_DC_EN	DC_PAUSE	
0x0E	RW	CUS_SYS3	SLEEP_BYPASS_EN		XTAL_STB_TIME[2:0]		TX_EXIT_STATE[1:0]		RX_EXIT_STATE[1:0]		
0x0F	RW	CUS_SYS4	SLEEP_TIMER_M								
0x10	RW	CUS_SYS5	SLEEP_TIMER_M				SLEEP_TIMER_R[3:0]				
0x11	RW	CUS_SYS6	RX_TIMER_T1_M								
0x12	RW	CUS_SYS7	RX_TIMER_T1_M				RX_TIMER_T1_R[3:0]				
0x13	RW	CUS_SYS8	RX_TIMER_T2_M								
0x14	RW	CUS_SYS9	RX_TIMER_T2_M				RX_TIMER_T2_R[3:0]				
0x15	RW	CUS_SYS10	COL_DET_EN	COL_OFS_SEL	[10:8]	DOUT_MUTE	RX_EXTEND_MODE[3:0]				
0x16	RW	CUS_SYS11	PID_TH_SEL	CCA_INT_SEL[1:0]		RSSI_DET_SEL[1:0]			RSSI_AVG_MODE		
0x17	RW	CUS_SYS12	PID_WIN_SEL[1:0]		CLKOUT_EN				[2:0]		
Addr		**Name**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Function**
0x18	RW	CUS_RF1	User does not need to understand the details, just directly export the register contents from the RFPDK								Frequency Bank
0x19	RW	CUS_RF2									
0x1A	RW	CUS_RF3									
0x1B	RW	CUS_RF4									
0x1C	RW	CUS_RF5									
0x1D	RW	CUS_RF6									
0x1E	RW	CUS_RF7									
0x1F	RW	CUS_RF8									
Addr	**R/W**	**Name**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Function**
0x20	RW	CUS_RF9	User does not need to understand the details, just directly export the register contents from the RFPDK								Data Rate Bank
0x21	RW	CUS_RF10									
0x22	RW	CUS_RF11									
0x23	RW	CUS_RF12									
0x24	RW	CUS_FSK1									
0x25	RW	CUS_FSK2									
0x26	RW	CUS_FSK3									
0x27	RW	CUS_FSK4									
0x28	RW	CUS_FSK5									
0x29	RW	CUS_FSK6									
0x2A	RW	CUS_FSK7									
0x2B	RW	CUS_CDR1									
0x2C	RW	CUS_CDR2									
0x2D	RW	CUS_CDR3									
0x2E	RW	CUS_CDR4									
0x2F	RW	CUS_AGC1									
0x30	RW	CUS_AGC2									
0x31	RW	CUS_AGC3									
0x32	RW	CUS_AGC4									
0x33	RW	CUS_OOK1									
0x34	RW	CUS_OOK2									
0x35	RW	CUS_OOK3									
0x36	RW	CUS_OOK4									
0x37	RW	CUS_OOK5									
Addr	**R/W**	**Name**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Function**
0x38	RW	CUS_PKT1	RX_PREAM_SIZE[4:0]					PREAM_LENG_UNIT	DATA_MODE[1:0]		Baseband Bank
0x39	RW	CUS_PKT2	TX_PREAM_SIZE[7:0]								
0x3A	RW	CUS_PKT3	TX_PREAM_SIZE [15:8]								
0x3B	RW	CUS_PKT4									
0x3C	RW	CUS_PKT5	RESV	SYNC_TOL[2:0]				SYNC_SIZE[2:0]		SYNC_MAN_EN	
0x3D	RW	CUS_PKT6	SYNC_VALUE[7:0]								
0x3E	RW	CUS_PKT7	SYNC_VALUE[15:8]								
0x3F	RW	CUS_PKT8	SYNC_VALUE[23:16]								
0x40	RW	CUS_PKT9	SYNC_VALUE[31:24]								
0x41	RW	CUS_PKT10	SYNC_VALUE[39:32]								
0x42	RW	CUS_PKT11	SYNC_VALUE[47:40]								
0x43	RW	CUS_PKT12									
0x44	RW	CUS_PKT13	SYNC_VALUE[63:56]								
0x45	RW	CUS_PKT14	RESV	PAYLOAD_LENG			AUTO_ACK_EN	NODE_LENG_POS_SEL	PAYLOAD_BIT_ORDER	PKT_TYPE	
0x46	RW	CUS_PKT15	PAYLOAD_LENG[7:0]								
0x47	RW	CUS_PKT16	RESV	RESV	NODE_FREE_EN	NODE_ERR_MASK	NODE_SIZE[1:0]		NODE_DET_MODE		
0x48	RW	CUS_PKT17	NODE_VALUE[7:0]								
0x49	RW	CUS_PKT18	NODE_VALUE[15:8]								
0x4A	RW	CUS_PKT19	NODE_VALUE[23:16]								
0x4B	RW	CUS_PKT20	NODE_VALUE[31:24]								
0x4C	RW	CUS_PKT21	FEC_TYPE	FEC_EN	CRC_BYTE_SWAP	CRC_BIT_INV	CRC_RANGE	CRC_TYPE[1:0]		CRC_EN	
0x4D	RW	CUS_PKT22	CRC_SEED[7:0]								
0x4E	RW	CUS_PKT23	CRC_SEED[15:8]								
0x4F	RW	CUS_PKT24	CRC_BIT_ORDER	WHITEN_SEED[8]	WHITEN_SEED_TYPE	WHITEN_TYPE[1:0]		WHITEN_EN	MANCH_TYPE	MANCH_EN	
0x50	RW	CUS_PKT25	WHITEN_SEED[7:0]								
0x51	RW	CUS_PKT26	RESV	RESV	RESV	RESV	RESV	RESV	TX_PREFIX_TYPE		
0x52	RW	CUS_PKT27	TX_PKT_NUM[7:0]								
0x53	RW	CUS_PKT28	TX_PKT_GAP[7:0]								
0x54	RW	CUS_PKT29	FIFO_AUTO_RES_EN	FIFO_TH[6:0]							
Addr		**Name**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Function**
0x55	RW	CUS_TX1	User does not need to understand the details, just directly export the register contents from the RFPDK								TX Bank
0x56	RW	CUS_TX2									
0x57	RW	CUS_TX3									
0x58	RW	CUS_TX4									
0x59	RW	CUS_TX5									
0x5A	RW	CUS_TX6									
0x5B	RW	CUS_TX7									
0x5C	RW	CUS_TX8									
0x5D	RW	CUS_TX9									
0x5E	RW	CUS_TX10									
0x5F	RW	CUS_LBD									
Addr		**Name**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Function**
0x60		CUS_MODE_CTL	CHIP_MODE_SWT[7:0]								Control Bank 1
0x61	RW	CUS_MODE_STA	RESV	RESV	RSTN_IN_EN	CFG_RETAIN	CHIP_MODE_STA[3:0]				
0x62	RW	CUS_EN_CTL	RESV	RESV	LOCKING_EN	RESV	RESV	RESV	RESV	RESV	
0x63	RW	CUS_FREQ_CHNL	FH_CHANNEL[7:0]								
0x64	RW	CUS_FREQ_OFS	FH_OFFSET[7:0]								
0x65	RW	CUS_IO_SEL	RESV	RESV	GPIO3_SEL[1:0]		GPIO2_SEL[1:0]		GPIO1_SEL[1:0]		
0x66	RW	CUS_INT1_CTL	RF_SWT1_EN	RF_SWT2_EN	INT_POLAR	INT1_SEL[4:0]					
0x67	RW	CUS_INT2_CTL	RESV	LFOSC_OUT_EN	TX_DIN_INV	INT2_SEL[4:0]					
0x68	RW	CUS_INT_EN	SL_TMO_EN	RX_TMO_EN	TX_DONE_EN	PREAM_OK_EN	SYNC_OK_EN	NODE_OK_EN	CRC_OK_EN	PKT_DONE_EN	
0x69	RW	CUS_FIFO_CTL	TX_DIN_EN	TX_DIN_SEL[1:0]		FIFO_AUTO_CLR_DIS	FIFO_TX_RD_EN	FIFO_RX_TX_SEL	FIFO_MERGE_EN	SPI_FIFO_RD_WR_SEL	
0x6A	RW	CUS_INT_CLR1	RESV	RESV	SL_TMO_FLG	RX_TMO_FLG	TX_DONE_FLG	TX_DONE_CLR	SL_TMO_CLR	RX_TMO_CLR	
Addr		**Name**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Function**
0x6B		CUS_INT_CLR2	RESV	RESV	LBD_CLR	PREAM_OK_CLR	SYNC_OK_CLR	NODE_OK_CLR	CRC_OK_CLR	PKT_DONE_CLR	Control Bank 2
0x6C	W	CUS_FIFO_CLR	RESV	RESV	RESV	RESV	RESV	FIFO_RESTORE	FIFO_CLR_RX	FIFO_CLR_TX	
0x6D	W	CUS_INT_FLAG	LBD_FLG	COL_ERR_FLG	PKT_ERR_FLG	PREAM_OK_FLG	SYNC_OK_FLG	NODE_OK_FLG	CRC_OK_FLG	PKT_OK_FLG	
0x6E	R	CUS_FIFO_FLAG	RESV	RX_FIFO_FULL_FLG	RX_FIFO_NMTY_FLG	RX_FIFO_TH_FLG	RX_FIFO_OVF_FLG	TX_FIFO_FULL_FLG	TX_FIFO_NMTY_FLG	TX_FIFO_TH_FLG	
0x6F	R	CUS_RSSI_CODE	RSSI_CODE[7:0]								
0x70	R	CUS_RSSI_DBM	RSSI_DBM[7:0]								
0x71	R	CUS_LBD_RESULT	LBD_RESULT[7:0]								

From the above table, it can be seen that the address range is from 0x00 to 0x71, which can be divided into 3 main banks for better understanding. They are: Configuration bank (including 6 sub-banks), Control Bank1, and Control Bank 2. For the 3 banks the address is continuous. They are all accessed via the SPI bus. They have different functionalities and design purposes, which are shown in the below table:

Table 22. Description of Register Banks

Address	Bank Name		Bank Name in the RFPDKExport File	Functionality
0x00-0x0B	Configuration Bank (RFPDK export the register values）	CMT Bank	CMT Bank	Users do not change them.
0x0C-0x17		System Bank	System Bank	Mainly relates to low power mode.
0x18-0x1F		Frequency Bank	Frequency Bank	To setup the TX and RX frequencies.
0x20-0x37		Data Rate Bank	Data Rate Bank	To setup data rate, deviation, bandwidths and other related parameters.
0x38-0x54		Baseband Bank	Baseband Bank	To setup packet format and some FIFO features.
0x55-0x5F		TX Bank	TX Bank	To setup TX deviation and power.
0x60-0x6A	Control Bank 1（Set by MCU in application, not generated by RFPDK）		--	To setup chip working state, frequency hopping, GPIOs and interrupts control.
0x6B-0x71	Control Bank 1(Set by MCU in application, not generated by RFPDK）		--	To read interrupt flags and RSSI value, control the FIFO.

To simplify the operation, users should firstly setup all the desired parameters on the RFPDK, export the register contents to the HEX file, and use it to initialize the CMT2300A. For the CMT Bank, Frequency Bank, Data Rate Bank, and the TX Bank, users do not need to study the details of the registers. Instead, these register configurations totally rely on the RFPDK. For System Bank and Baseband Bank, users must study the details in order to play with them in different applications. Meanwhile, for Control Bank 1 and 2, users must also understand the meaning of each register.

CMOSTEK provides a series Application Notes (AN) for the users to study how to play with the chip, how to configure the parameters on RFPDK, how to use each register, and other notable application skills. Users can start their learning from reading “AN142 CMT2300AW Quick Start Guide”, which provides step-by-step guidance and leads the users to read other documents.

9. Ordering Information

Table 23. CMT2300A ordering information

Part Number	Descriptions	Packaging	Packing	Condition	MOQ
CMT2300A-EQR[1]	CMT2300A, Ultra Low Power Sub-1GHz RF Transceiver	QFN16 (3x3)	Tape& Reel	1.8 to 3.6V, -40 to 85℃	3,000

Notes:

[1]. "E" represents extended industrial grade. The temperature range is from -40 to +85.
"Q" represents QFN16 packaging.
"R" represents tape &reel packing. MOQ is 3000pcs.

For more information about product, please visit www.hoperf.com.
For purchasing or price requirements, please contact sales@hoperf.com or local sales representative

10. Packaging Information

CMT2300A packaging is QFN16 (3x3). The packaging information is as below.

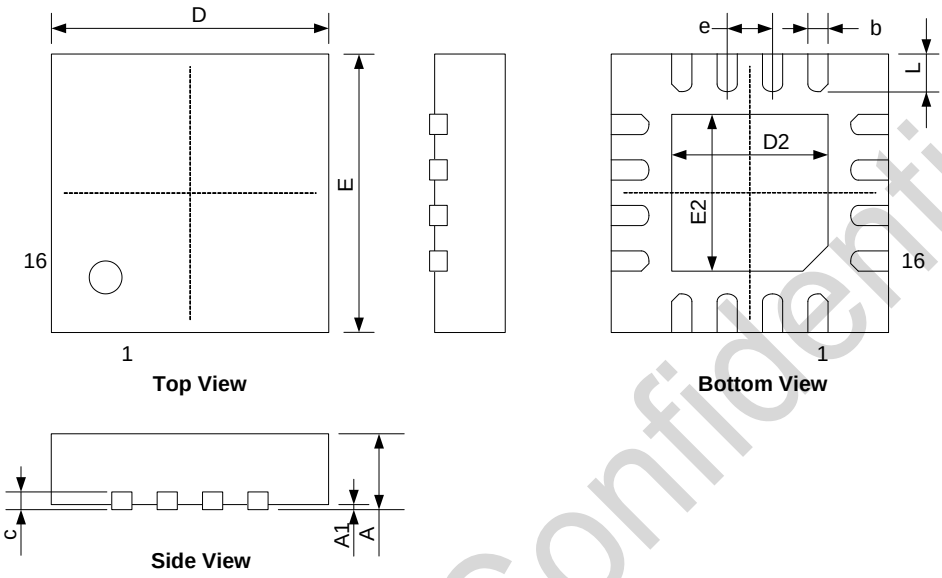


Figure 24. 16-Pin QFN 3x3 packaging

Table 24. 16-Pin QFN 3x3 packaging

Symbol	Size (mm)	
	Min.	Max.
A	0.7	0.8
A1	—	0.05
b	0.18	0.30
c	0.18	0.25
D	2.90	3.10
D2	1.55	1.75
e	0.50 BSC	
E	2.90	3.10
E2	1.55	1.75
L	0.35	0.45

11. Top Marking

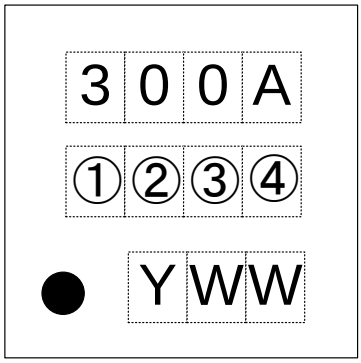


Figure 25. CMT2300A top marking

Table 25. CMT2300A top marking description

Marking method	Laser
Pin 1 mark	Circle diameter = 0.3 mm
Font size	0.5 mm, right aligned.
Line 1 marking	300A represents model CMT2300A
Line 2 marking	①②③④ **represents th**e internal tracking coding
Line 3 marking	Date code is assigned by assembly factory. Y represents the last digit of the year. WW represents working week.

12. Revise History

Table 26. Revise History Records

Version No.	Chapter	Description	Date
Preliminary	All	Preliminary version for internal verification	2015-06-09
Preliminary 0.2	5.14.1 5.14.2	Update 1st paragraph Update Table 34	2015-06-10
0.6	All	Split Chapter 5 and 6 from Chapter 4	2015-08-06
0.7	All	Initial release for production version	2017-03-22
0.8	All	Changed T&R to 3,000 pcs Added AN document list Added new RF parameters and curves	2017-08-10
0.9	All	Added and changed some performance numbers Changed RSSI descriptions Added POR descriptions Added PJD, AFC and CDR descriptions Added receiver “Power VS Performance” descriptions Changed some characters and figures Detected the AN document list	2018-01-03
1.0	All	Changed some descriptions	2018-01-15
1.0a	All	Reformat on English version	2020-03-03
1.1	4.3.7	Remove document reference AN196	2020-09-09
1.2	1.11	Table 11, adjust SCLK related parameter values	2021-07-21
1.3	1.11	Table 11, adjust SCLK, V_{IH} related parameter values	2021-12-24
1.4	2, 3, 5.3.2	Section 2, add notes for some pins when they are used in low-power applications. Section 3, modify typical schematic diagrams of both direct-tie and switch-type and the corresponding component BOMs: remove capacitors for SCLK/SDIO/FCSB pins and keep the capacitor for CSB pin only. Section 5.3.2, figure 16, modify some minor typo error.	2022-01-05
1.5	1.4	Added input impedance value in Table 4	2022-10-27

13. Contacts

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