

A

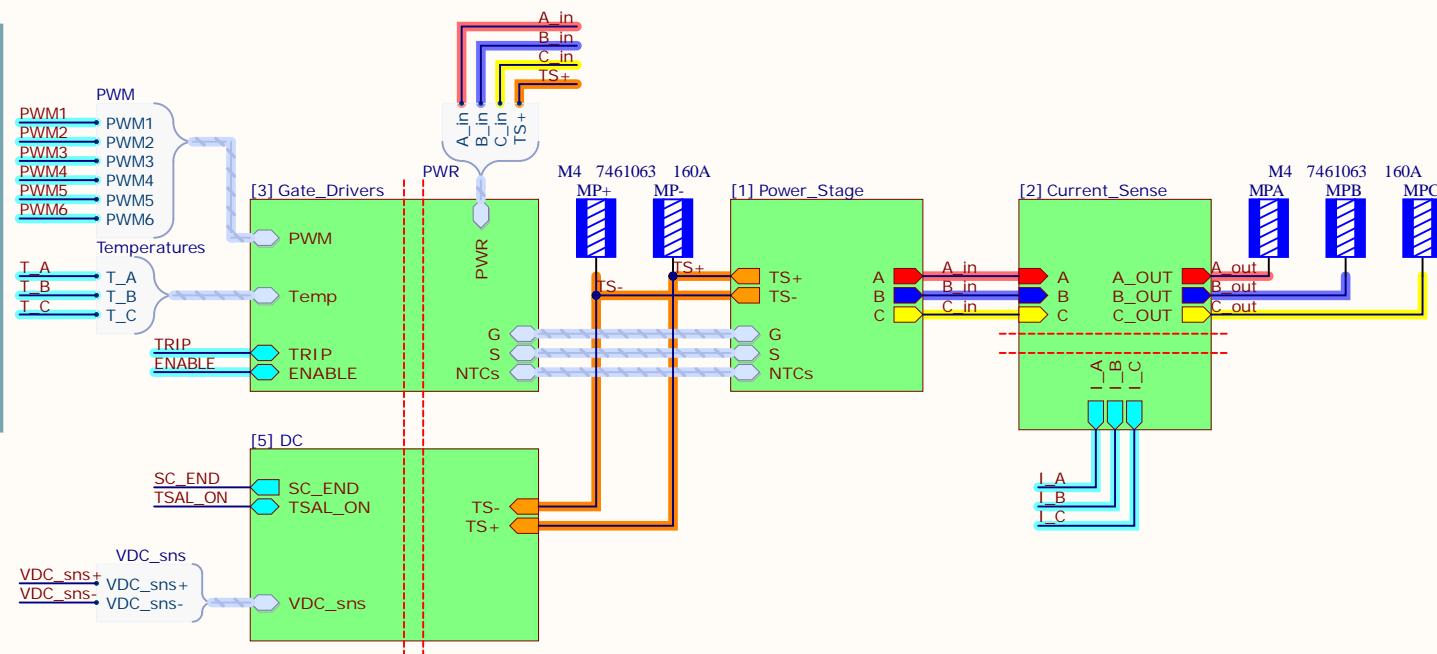
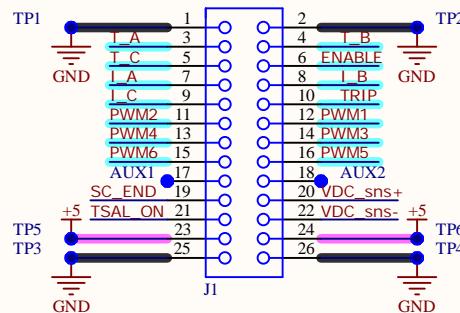
① Dashed red lines indicate isolation barriers between TS and LV.

① Cyan areas indicate GLVS and cyan nets indicate signals from/to GLVS.

① Orange areas indicate TS and orange nets indicate high power TS.

Specifications:  
 $V_{in}$ , max = 600 VDC  
 $V_{out}$ , max = 245 VRMS (SVPWM)  
 $f_{sw}$  = 50 kHz  
 $P_{out}$ , max = 40kW  
 $I_{out}$ , max = 80 ARMS  
Liquid cooled with water at 50°C max

## LV Connector

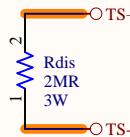


Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Inverter_Power	
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Department:	Powertrain		
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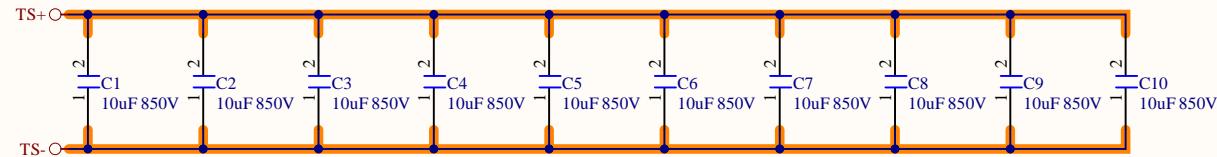
A

A

### Passive discharge



### DC Bus capacitors, 100uF, Murata FHA85Y106KS



#### DC Link design considerations:

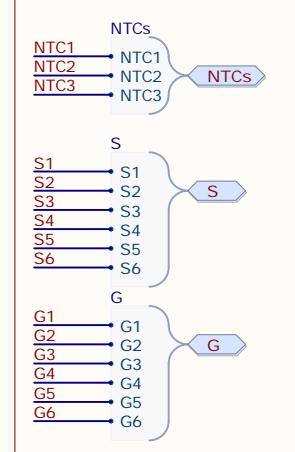
$$V_{C} > 1.1 \cdot V_{max} = 1.1 \cdot 600 \text{ V} = 660 \text{ V} \rightarrow 850 \text{ V}$$

$$I_{C,RMS} \approx 0.65 \cdot I_{phase,RMS} = 0.65 \cdot 80 \text{ A,RMS} = 52 \text{ A,RMS} \rightarrow 10 \times 5 \text{ A,RMS } (\Delta T = 10^\circ\text{C})$$

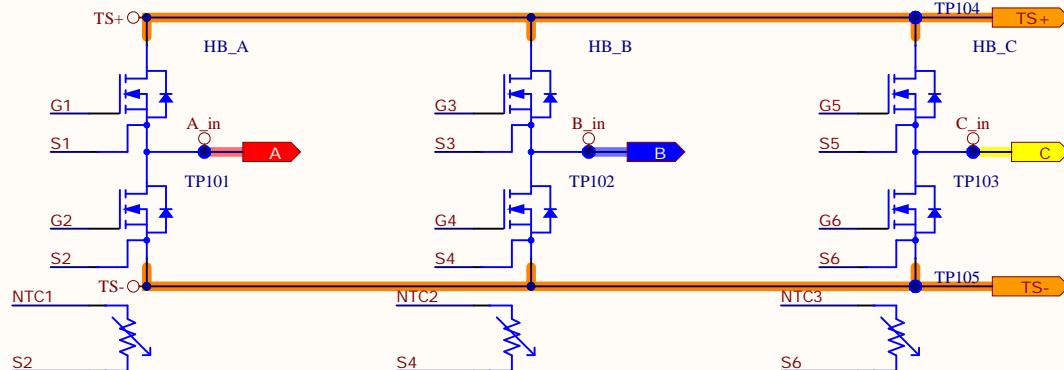
$$C > I_{C,RMS} / (V_{ripple} \cdot f_{sw}) = 52 \text{ A,RMS} / (15 \text{ V} \cdot 50 \text{ kHz}) \approx 79 \mu\text{F} \rightarrow 10 \times 10 \mu\text{F}$$

Lowering the switching frequency will proportionally lower the current rating for the same voltage ripple or proportionally increase the voltage ripple for the same output current. Check:  
<https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter>

### INPUTS/OUTPUTS



### SiC Half-Bridges, Leapers DFS05HF12EYR1



#### Semiconductor details:

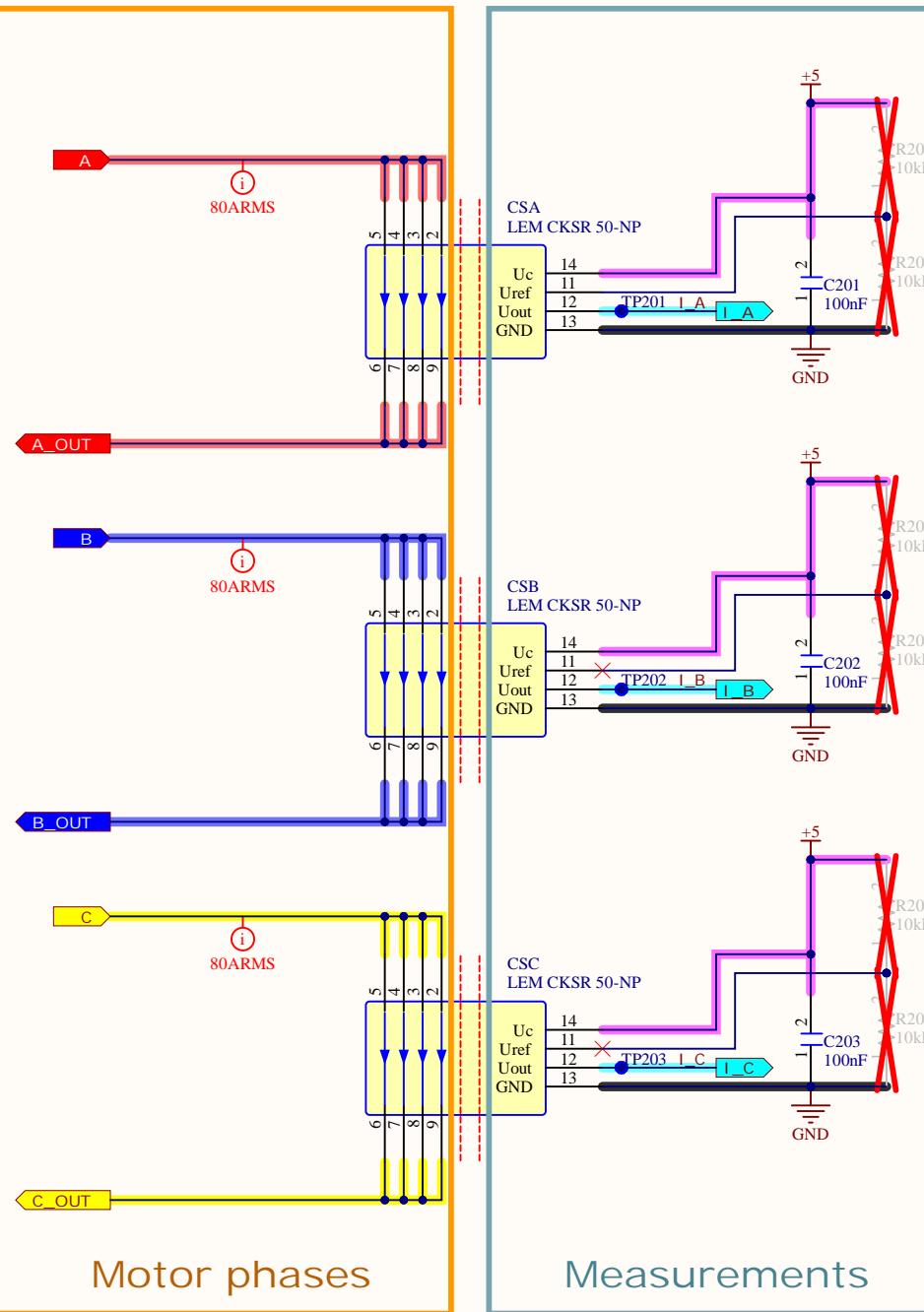
$V_{DSS}(\text{breakdown}) = 1200 \text{ V}$   
 $R_{on} = 5.5 \dots 13 \text{ m}\Omega$   
 $V_f,D = 3.3 \dots 4 \text{ V}$   
 $T_{rr} = 41.5 \dots 45 \text{ ns}$   
 $Q_{rr} = 2.19 \dots 3.94 \mu\text{C}$   
 $R_{th,jc} = 0.12 \dots 0.15 \text{ K/W}$   
 $Q_G(600V, 150A, V_{GS} = +15/0V) = 520 \text{ nC}$   
 $C_{in} = 14.5 \text{ nF}$   
 $R_G(\text{int}) = 1.9 \Omega$   
 $V_{GS(th)} = 2.8 \dots 4.8 \text{ V}$

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A

CSA, CSB, CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R\_phase-connector = 0.18 mΩ)



B

C

D

A

B

C

D

CSA, CSB, CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values. Voltage divider implemented just in case.

I\_A, I\_B, I\_C

$$U_{\text{meas}} = (12.5 \text{mV/A} \cdot I_{\text{meas}} + 2.5 \text{V})$$

For  $\pm 150 \text{Apk}$ :

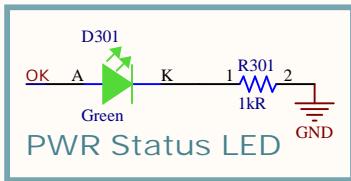
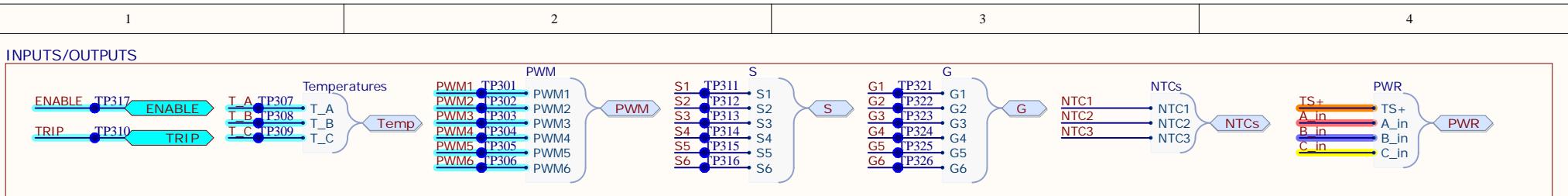
$$V_{\text{meas\_pk+}} = 4.375 \text{V}$$

$$V_{\text{meas\_pk-}} = 0.625 \text{V}$$

C201, C202, C203

The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

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**A**

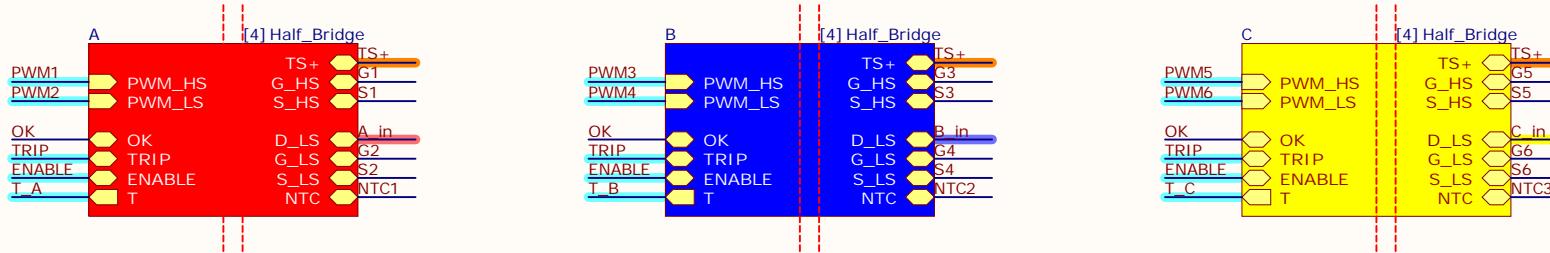
**T\_A, T\_B, T\_C**

Look-up table obtained with MATLAB script.

For different temperatures:

- $V_{meas}(0^{\circ}C) = 0.246V$
- $V_{meas}(25^{\circ}C) = 2V$
- $V_{meas}(50^{\circ}C) = 2.578V$
- $V_{meas}(90^{\circ}C) = 2.864V$

**B**



**D**

Company: e-Tech Racing e-techracing.es		
Project: Inverter Power Variant: Inverter_Power		
Size:	Page Contents: [3]Gate_Drivers.SchDoc	Version: 1.0
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Author: David Redondo dredondovinolo@gmail.com		Sheet 4 of 8
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**U\_HS**, **U\_LS**

1. **TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
  2. IN- is not used and tied to **GND**.
  3. **ENABLE** to be given by MCU in active-high mode. When set to low for more than 1  $\mu$ s, **TRIP** is reset.
  4. Temperature sensing using low-side drivers. Ain outputs a current of 200  $\mu$ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **R405**, **R406** and **C411** from SPICE simulation.
  5. Miller clamp protection is used.
  6. **RGS\_HS**, **RGS\_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
  7. Overcurrent/Shoot-through detection is not implemented.

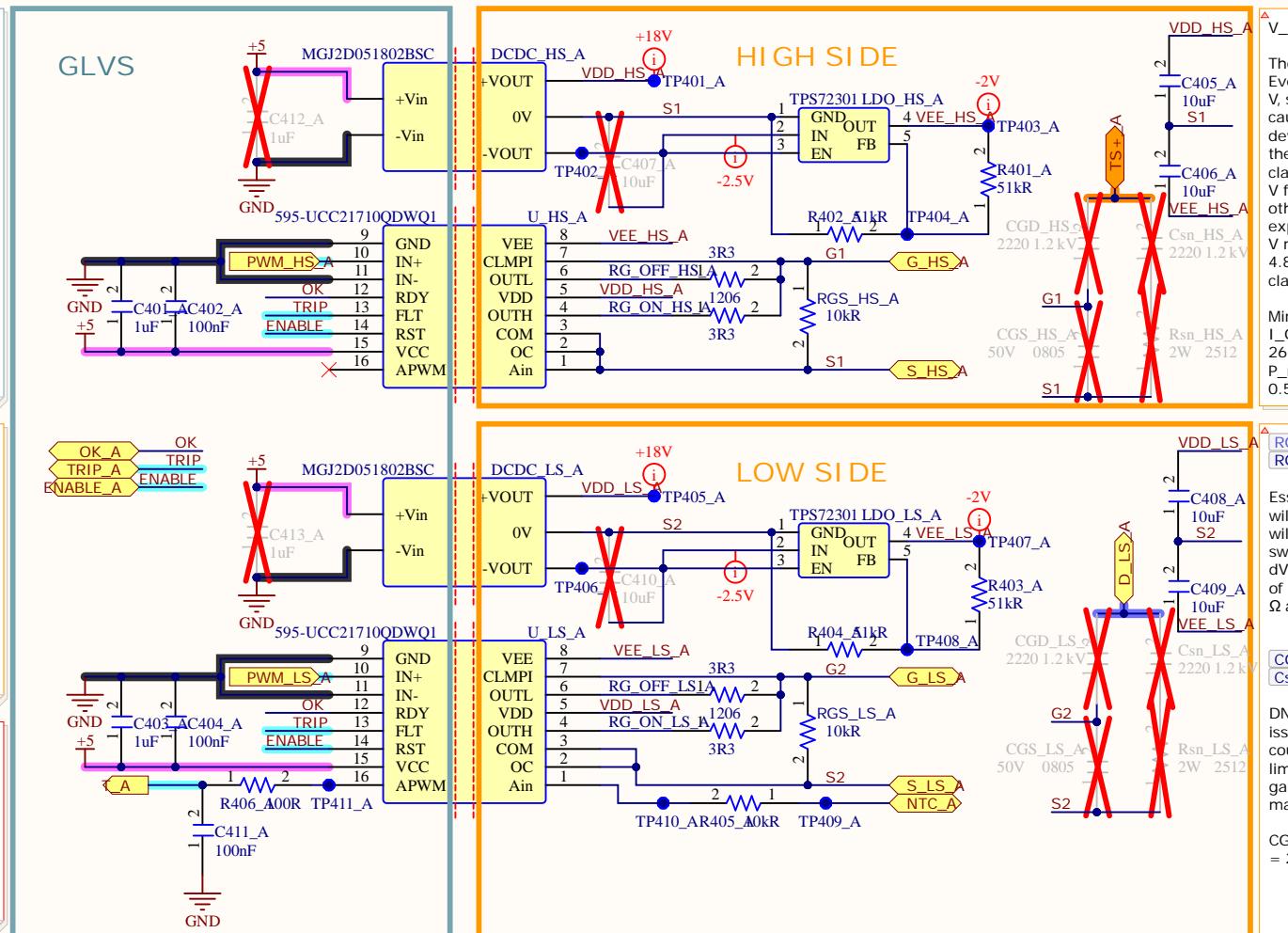
LDO HS LDO LS

- An LDO is implemented to trim `VEE_HS_A` and `VEE_LS_A` during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, `DCDC_HS` and `DCDC_LS` must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing  
 $V_{GS} = +18 \text{ V} / -2 \text{ V}$   
 $VEE = -1.186 \cdot (1 + R1/R2)$   
 $R1 = R2 \approx 100 \text{ k}\Omega$

**DCDC\_HS**, **DCDC\_LS**

U\_HS, U\_LS



A △ V<sub>GS</sub> values:

The values chosen for  $V_{GS}$  are +18 V / -2 V. Even though Leapers recommends using +18 V / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum  $V_{GS(th)}$ . A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:  
 $I_{GD(min)} = f_{sw} \cdot Q_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$   
 $P_{min} = \Delta V_{GS} \cdot I_{GD(min)} = 20 \text{ V} \cdot 26 \text{ mA} = 520 \text{ mW}$

**RG ON HS**

**A** Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the  $dV/dt$  will be higher, which can be responsible of EMI increase. The considered values of 3.3  $\Omega$  are recommended by the datasheet.

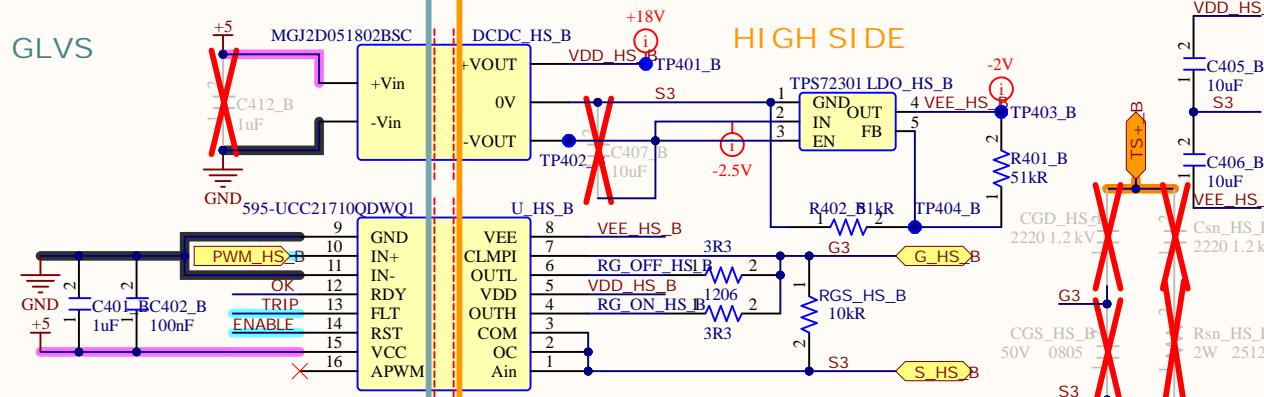
A  
kV CGS\_HS , CGS\_LS , CGD\_HS , CGD\_LS ,  
Csn\_HS , Csn\_LS , Rsn\_HS , Rsn\_LS

DNP, but they could be useful with EMI related issues to decrease  $dV/dt$ . Implementing them could result in further issues with the power limit for [DCDC\\_HS](#) and [DCDC\\_LS](#), as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$\text{CGS}_{\text{max}} = 2 \cdot P_{\text{DCDC}} / (\Delta V_{\text{GS}}^2 \cdot f_{\text{sw}}) \\ = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

**A** ▲ **U\_HS**, **U\_LS**

- TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
- IN- is not used and tied to **GND**.
- ENABLE** is to be given by MCU in active-high mode. When set to low for more than 1  $\mu$ s, **TRIP** is reset.
- Temperature sensing using low-side drivers. Ain outputs a current of 200  $\mu$ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **R405**, **R406** and **C411** from SPICE simulation.
- Miller clamp protection is used.
- RGS\_HS**, **RGS\_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
- Overcurrent/Shoot-through detection is not implemented.

**GLVS****V\_GS values:**

The values chosen for  $V_{GS}$  are +18 / -2 V. Even though Leapers recommends using +18 / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum  $V_{GS(th)}$ . A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:

$$I_{GD(min)} = f_{sw} \cdot Q_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$$

$$P_{min} = \Delta V_{GS} \cdot I_{GD(min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$$

**LDO\_HS**, **LDO\_LS**

An LDO is implemented to trim **VEE\_HS\_A** and **VEE\_LS\_A** during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, **DCDC\_HS** and **DCDC\_LS** must be replaced with another variant and bypassing the LDOs.

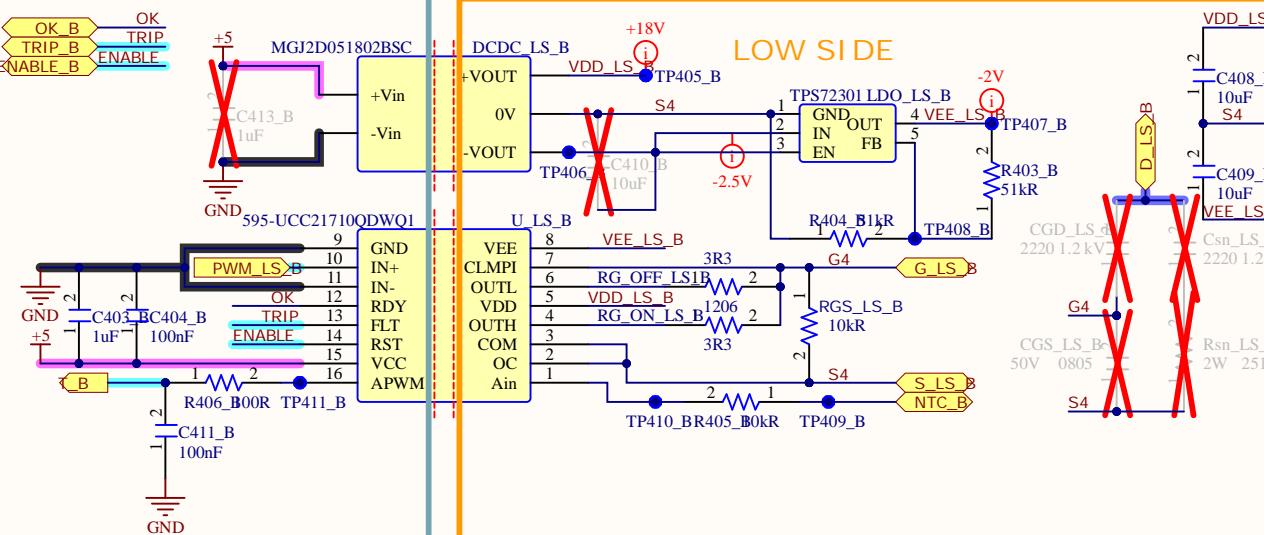
Feedback voltage divider adjusted to -2V, providing  $V_{GS} = +18 \text{ V} / -2 \text{ V}$   
 $VEE = -1.186 \cdot (1 + R1/R2)$   
 $R1 + R2 \approx 100 \text{ k}\Omega$

**DCDC\_HS**, **DCDC\_LS**

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

**U\_HS**, **U\_LS**

VIOTM ( $t = 60 \text{ s}$  (qualification test)): 8000 VPK

**OK\_B**, **TRIP\_B**, **ENABLE****RG\_ON\_HS**, **RG\_OFF\_HS**, **RG\_ON\_LS**, **RG\_OFF\_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the  $dV/dt$  will be higher, which can be responsible of EMI increase. The considered values of 3.3  $\Omega$  are recommended by the datasheet.

**CGS\_HS**, **CGS\_LS**, **CGD\_HS**, **CGD\_LS**, **Csn\_HS**, **Csn\_LS**, **Rsn\_HS**, **Rsn\_LS**

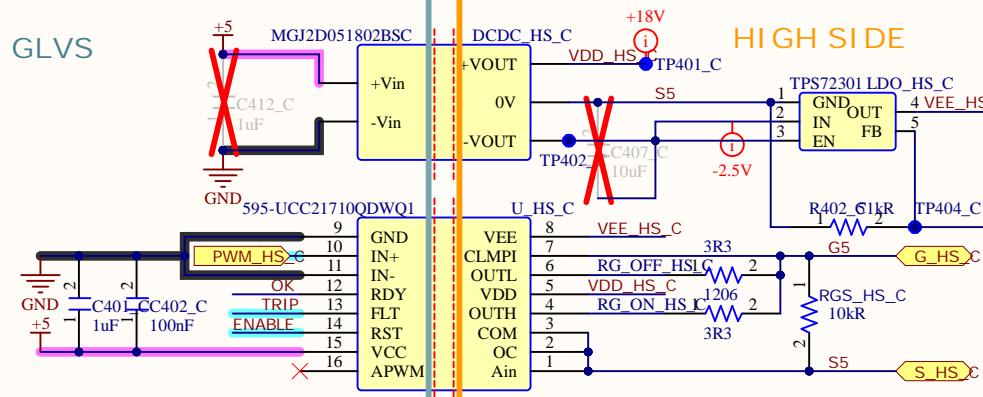
DNP, but they could be useful with EMI related issues to decrease  $dV/dt$ . Implementing them could result in further issues with the power limit for **DCDC\_HS** and **DCDC\_LS**, as the gate charge would increase significantly. The maximum allowed capacitance would be:

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Project:	Inverter Power	Variant: Inverter_Power	
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Author:	David Redondo	dredondovinolo@gmail.com	Sheet 52 of 8
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**A** ▲ **U\_HS, U\_LS**

1. **TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to **GND**.
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**GLVS****B** ▲ **LDO\_HS, LDO\_LS**

An LDO is implemented to trim **VEE\_HS\_A** and **VEE\_LS\_A** during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, **[DCDC\_HS]** and **[DCDC\_LS]** must be replaced with another variant and bypassing the LDOs.

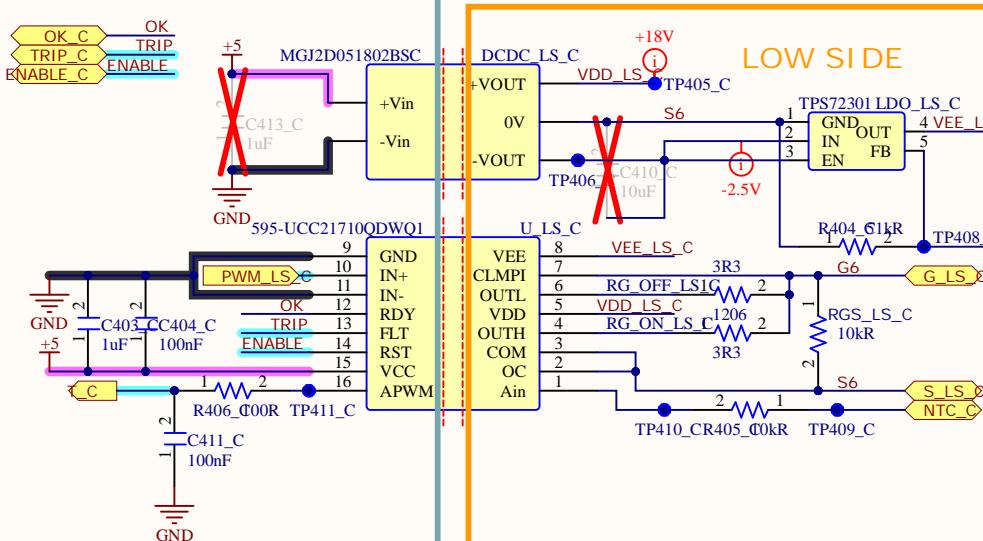
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 $VEE = -1.186 \cdot (1 + R1/R2)$   
 $R1 + R2 \approx 100 \text{ k}\Omega$

**C** ▲ **DCDC\_HS, DCDC\_LS**

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

**D** ▲ **U\_HS, U\_LS**

VIOTM ( $t = 60 \text{ s}$  (qualification test)): 8000 VPK



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Author:	David Redondo	dredondovinolo@gmail.com	Sheet 5.3 of 8
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**A** ▲ **V\_GS values:**

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 $P_{min} = \Delta V_{GS} \cdot I_{GD(min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

**B** ▲ **RG\_ON\_HS, RG\_OFF\_HS, RG\_ON\_LS, RG\_OFF\_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the  $dV/dt$  will be higher, which can be responsible of EMI increase. The considered values of 3.3  $\Omega$  are recommended by the datasheet.

**C** ▲ **CGS\_HS, CGS\_LS, CGD\_HS, CGD\_LS, Csn\_HS, Csn\_LS, Rsn\_HS, Rsn\_LS**

DNP, but they could be useful with EMI related issues to decrease  $dV/dt$ . Implementing them could result in further issues with the power limit for **[DCDC\_HS]** and **[DCDC\_LS]**, as the gate charge would increase significantly. The maximum allowed capacitance would be:

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