ⓘ Dashed red lines indicate isolation barriers between TS and LV.

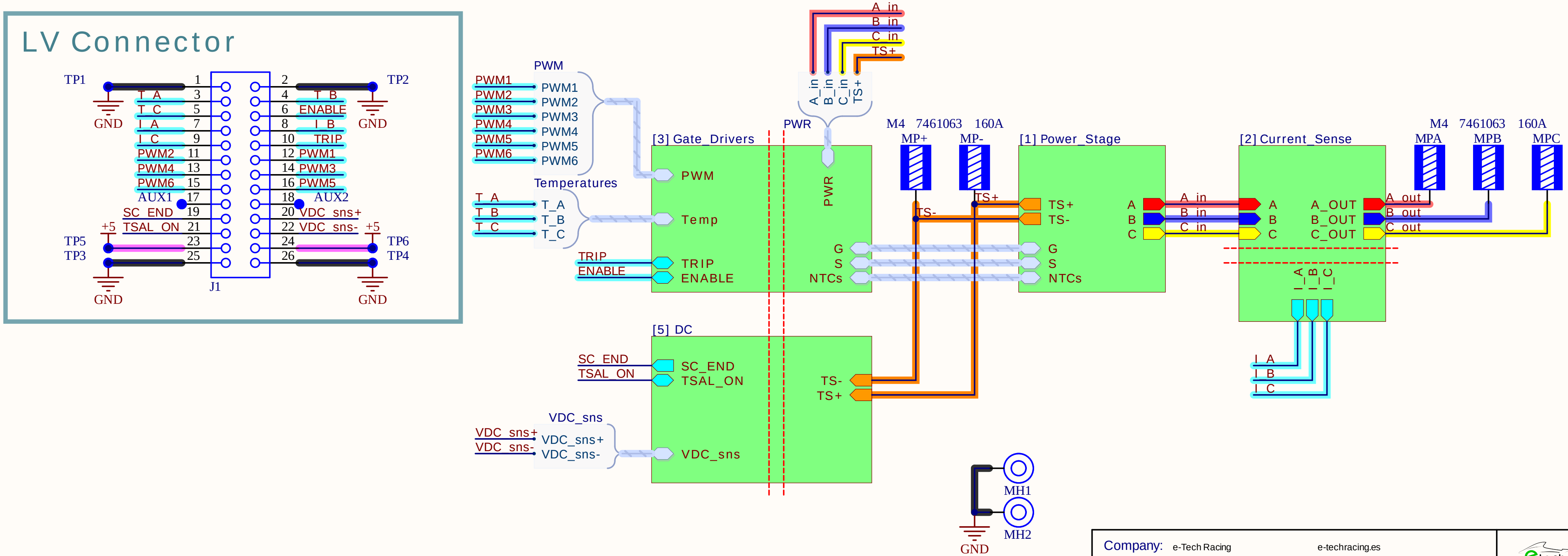
ⓘ Cyan areas indicate GLVS and cyan nets indicate signals from/to GLVS.

ⓘ Orange areas indicate TS and orange nets indicate high power TS.

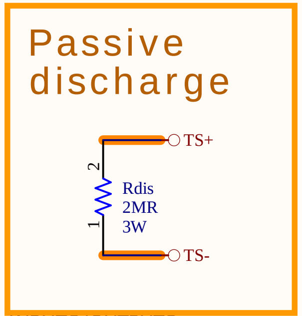
Specifications:

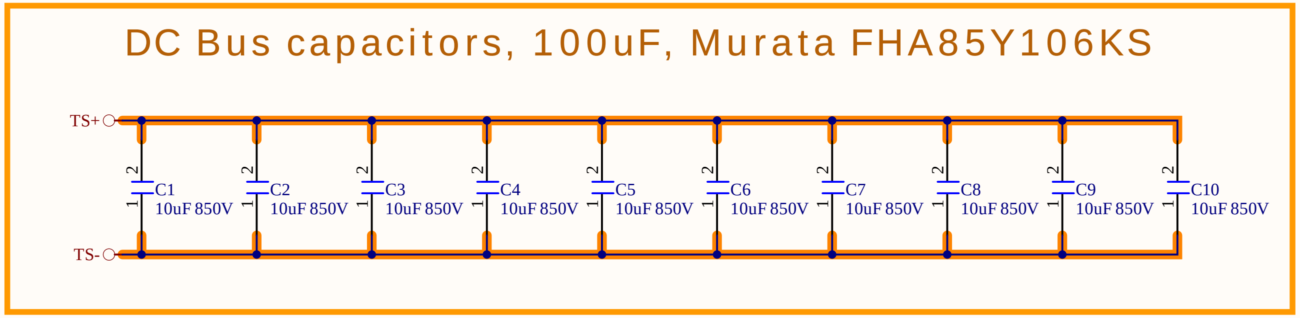
V_in, max = 600 VDC
V_out, max = 245 VRMS (SVPWM)
f_sw = 50 kHz
P_out, max = 40kW
I_out, max = 80 ARMS

Liquid cooled with water at 50ºC max



Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Inverter_Power		
Size: -	Page Contents: Inverter_Power.SchDoc	Version: 1.0	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet 1 of 5	
Checked by: _		Date: 14/02/2024	



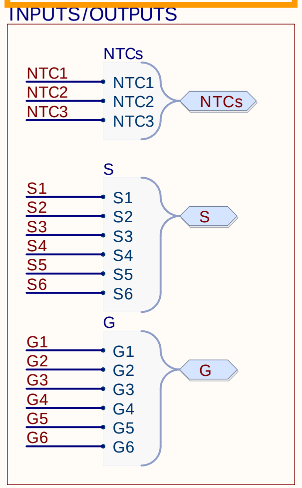


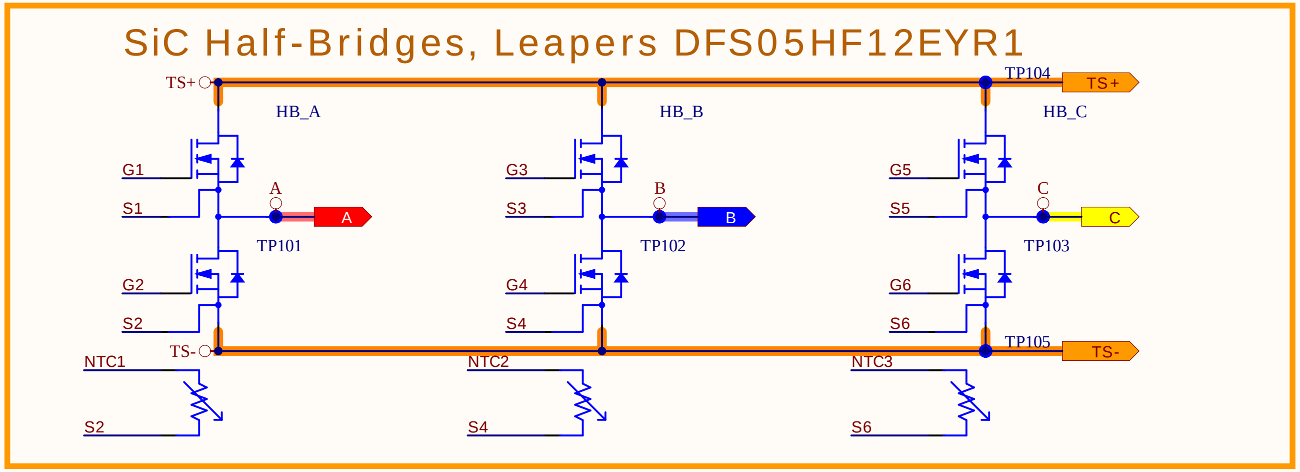
DC Link design considerations:

V_C > 1.1 · Vmax = 1.1 · 600 V = 660 V → 850 V

I_C,RMS ≈ 0.65 · I_phase,RMS = 0.65 · 80 A,RMS = 52 A,RMS → 10 x 5 A,RMS (ΔT = 10 ºC)
C > I_C,RMS / (V_ripple · f_sw) = 52 A,RMS / (15V · 50 kHz) ≈ 79 μF → 10 x 10 μF

Lowering the switching frequency will proportionally lower the current rating for the same voltage ripple or proportionally increase the voltage ripple for the same output current. Check: https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter





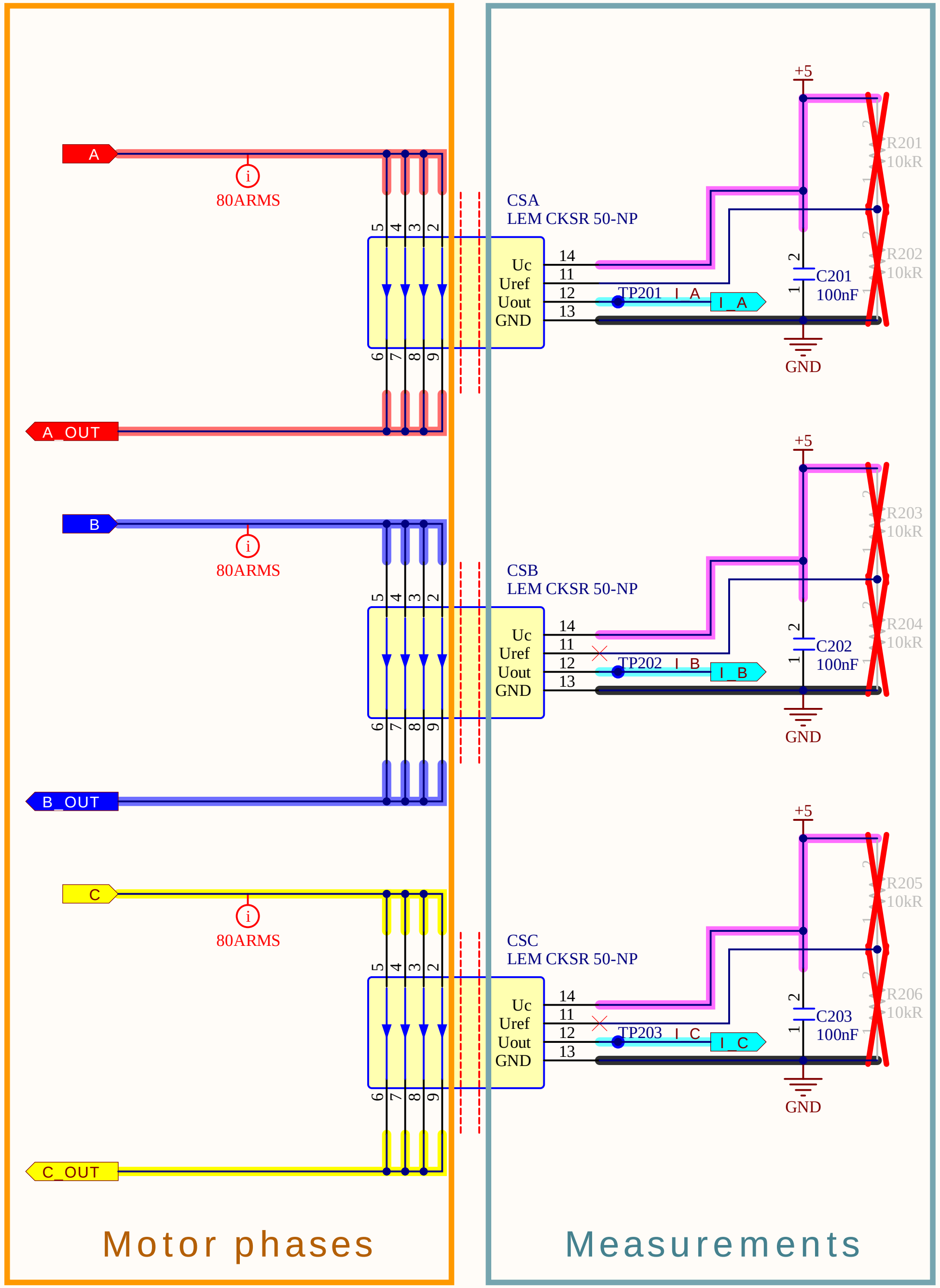
Semiconductor details:

V_DSS(breakdown) = 1200 V
Ron = 5.5 .. 13 mΩ
Vf_D = 3.3 .. 4 V
T_rr = 41.5 .. 45 ns
Q_rr = 2.19 .. 3.94 μC
R_th_jc = 0.12 .. 0.15 K/W
Q_G (600V, 150A, V_GS = +15/0V) = 520 nC
C_in = 14.5 nF
R_G(int) = 1.9 Ω
V_GS(th) = 2.8 .. 4.8 V

Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Inverter_Power		
Size: -	Page Contents: [1] Power_Stage.SchDoc	Version: 1.0	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet 2 of 5	
Checked by: -		Date: 14/02/2024	

CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R_phase-connector = 0.18 mΩ)



CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values. Voltage divider implemented just in case.

I_A , I_B , I_C

U_meas = (12.5mV/A · I_meas + Uref)

For ±150Apk:
V_meas_pk+ = 4.375V
V_meas_pk- = 0.625V

C201 , C202 , C203

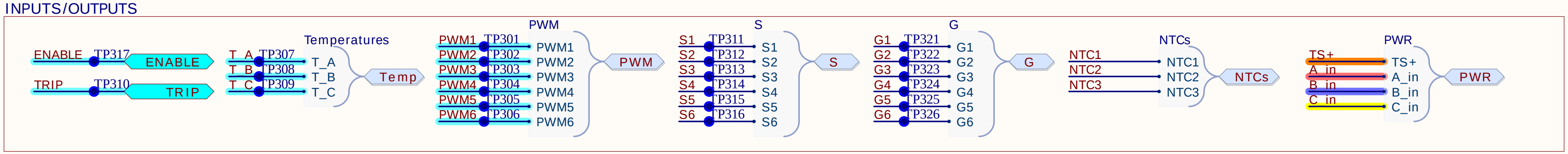
The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

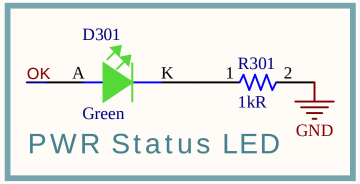
CSA , CSB , CSC

AC insulation test
RMS voltage, 50 Hz,
1 min:

Ud = 4.3 kV >
3*V_max = 1.8 kV

Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Inverter_Power		
Size: -	Page Contents: [2] Current_Sense.SchDoc	Version: 1.0	Department: Powertrain
Author: David Redondo	dredondovinolo@gmail.com	Sheet 3 of 5	
Checked by: _		Date: 14/02/2024	

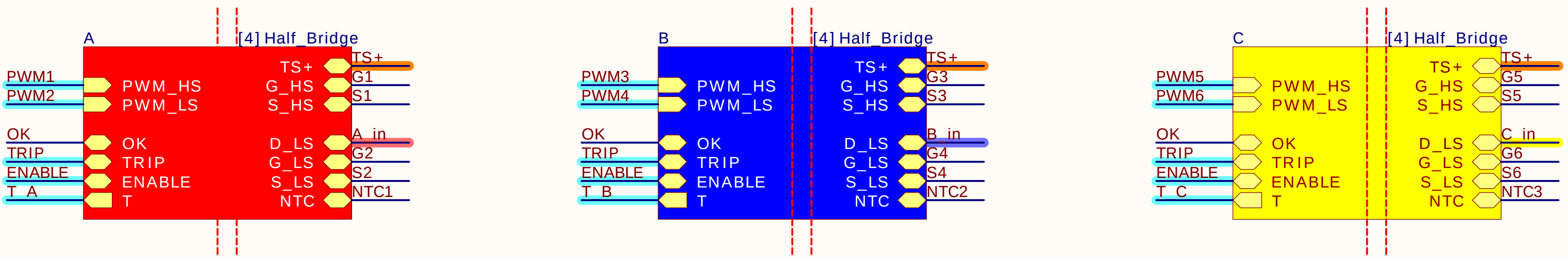


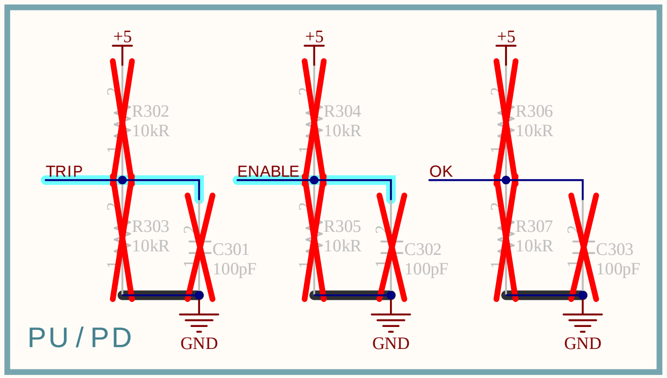


T_A, T_B, T_C

Look-up table obtained with MATLAB script.

For different temperatures:
V_meas(0ºC) = 0.246V
V_meas(25ºC) = 2V
V_meas(50ºC) = 2.578V
V_meas(90ºC) = 2.864V





Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Inverter_Power		
Size: -	Page Contents: [3] Gate_Drivers.SchDoc	Version: 1.0	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet 4 of 5	
Checked by: _		Date: 14/02/2024	

U_HS, U_LS

1. TRIP and OK signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to GND.
3. ENABLE to be given by MCU in active-high mode. When set to low for more than 1 μs, TRIP is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200 μA. PWM to analog using a RC filter, to be fed directly to MCU ADC. R405, R406 and C411 from SPICE simulation.
5. Miller clamp protection is used.
6. RGS_HS, RGS_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
7. Overcurrent/Shoot-through detection is not implemented.

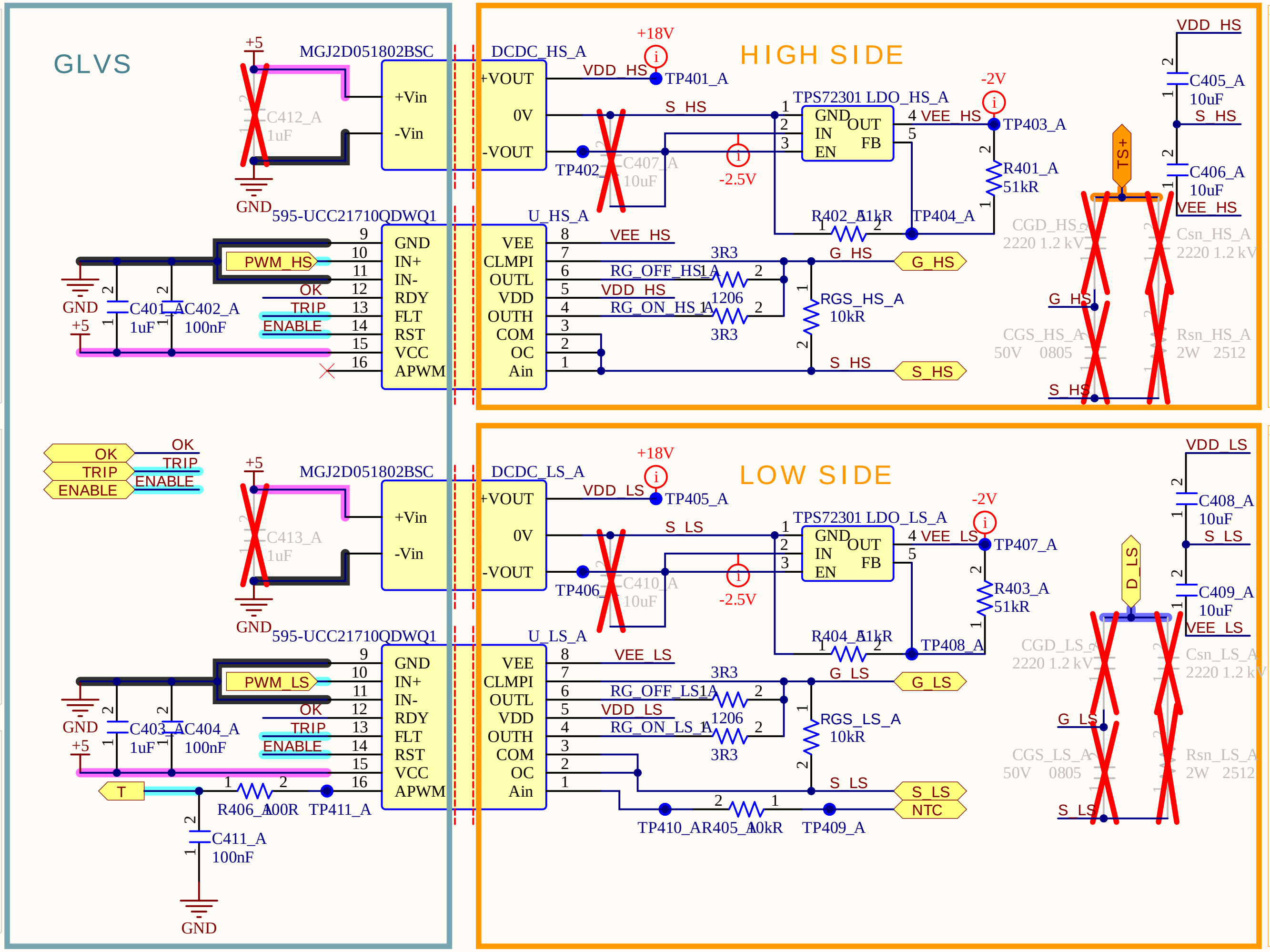
LDO_HS, LDO_LS

An LDO is implemented to trim VEE_HS_A and VEE_LS_A during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, DCDC_HS and DCDC_LS must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing
V_GS = +18 V / -2 V
VEE = - 1.186 · (1 + R1/R2)
R1 + R2 ≈ 100 kΩ

DCDC_HS, DCDC_LS
Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS
VIOTM (t = 60 s (qualification test)): 8000 VPK



V_GS values:

The values chosen for V_GS are +18 / -2 V. Even though Leapers recommends using +18 / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum V_GS(th). A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:
I_GD(min) = f_sw · Q_G = 50 kHz · 520 nC = 26 mA
P_min = ΔV_GS · I_GD(min) = 20 V · 26 mA = 0.52 W → 2 W

RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible for EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS, CGS_LS, CGD_HS, CGD_LS, Csn_HS, Csn_LS, Rsn_HS, Rsn_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could result in further issues with the power limit for DCDC_HS and DCDC_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

CGS_max = 2 · P_DCDC / (ΔV_GS ^2 · f_sw)
= 2 · 2 W / ((20 V)^2) · 50 kHz) = 200 nF

Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Inverter_Power		
Size: -	Page Contents: [4] Half_Bridge.SchDoc	Version: 1.0	Department: Powertrain
Author: David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5	
Checked by: _		Date: 14/02/2024	

U_HS, U_LS

1. TRIP and OK signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to GND.
3. ENABLE to be given by MCU in active-high mode. When set to low for more than 1 μs, TRIP is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200 μA. PWM to analog using a RC filter, to be fed directly to MCU ADC. R405, R406 and C411 from SPICE simulation.
5. Miller clamp protection is used.
6. RGS_HS, RGS_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
7. Overcurrent/Shoot-through detection is not implemented.

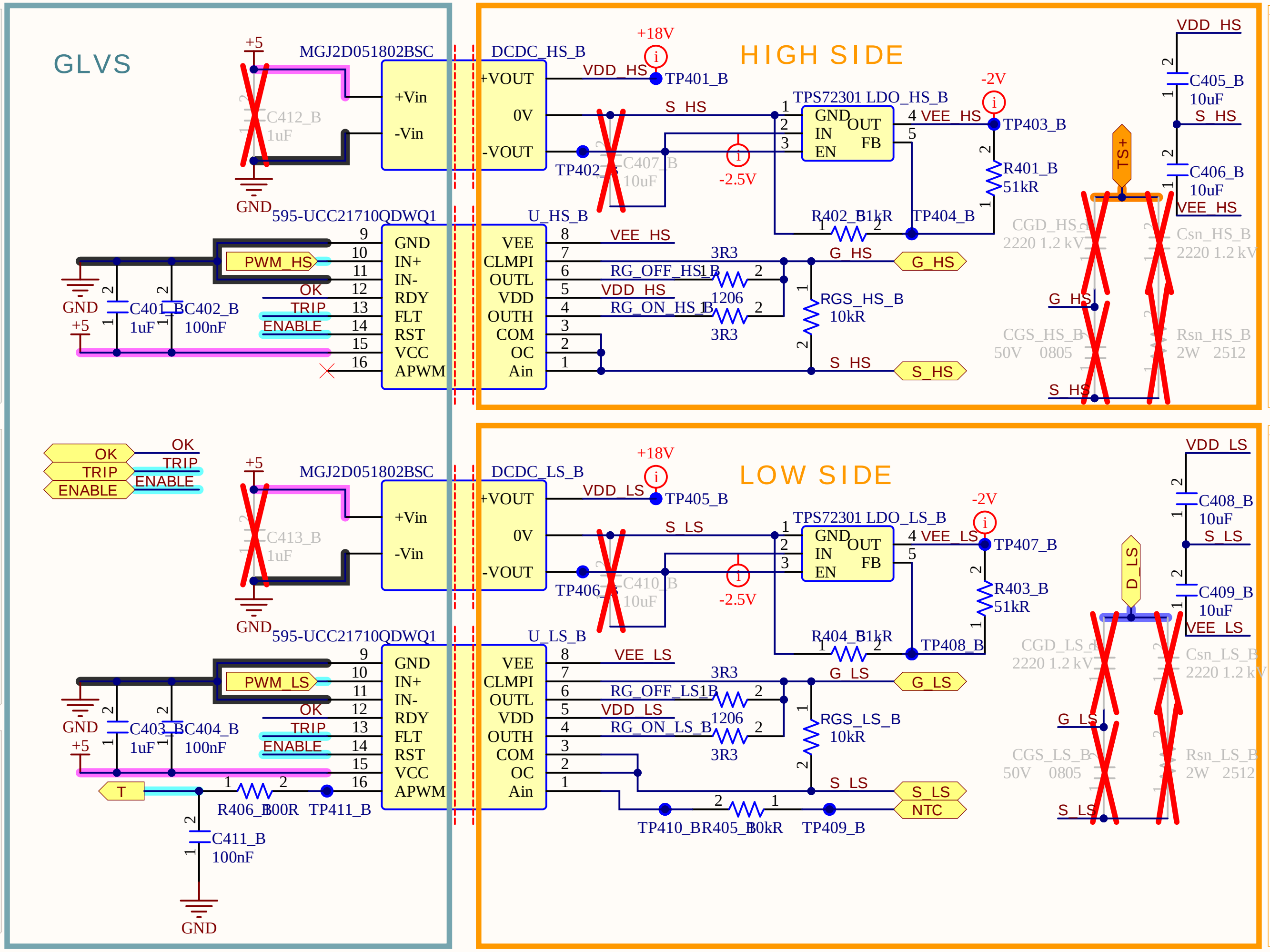
LDO_HS, LDO_LS

An LDO is implemented to trim VEE_HS_A and VEE_LS_A during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, DCDC_HS and DCDC_LS must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing
V_GS = +18 V / -2 V
VEE = - 1.186 · (1 + R1/R2)
R1 + R2 ≈ 100 kΩ

DCDC_HS, DCDC_LS
Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS
VIOTM (t = 60 s (qualification test)): 8000 VPK



V_GS values:

The values chosen for V_GS are +18 / -2 V. Even though Leapers recommends using +18 / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum V_GS(th). A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:
I_GD(min) = f_sw · Q_G = 50 kHz · 520 nC = 26 mA
P_min = ΔV_GS · I_GD(min) = 20 V · 26 mA = 0.52 W → 2 W

RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS, CGS_LS, CGD_HS, CGD_LS, Csn_HS, Csn_LS, Rsn_HS, Rsn_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could result in further issues with the power limit for DCDC_HS and DCDC_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

CGS_max = 2 · P_DCDC / (ΔV_GS ^2 · f_sw) = 2 · 2 W / ((20 V)^2) · 50 kHz) = 200 nF

Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Inverter_Power		
Size: -	Page Contents: [4] Half_Bridge.SchDoc	Version: 1.0	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5	
Checked by: _		Date: 14/02/2024	

U_HS, U_LS

1. TRIP and OK signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to GND.
3. ENABLE to be given by MCU in active-high mode. When set to low for more than 1 μs, TRIP is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200 μA. PWM to analog using a RC filter, to be fed directly to MCU ADC. R405, R406 and C411 from SPICE simulation.
5. Miller clamp protection is used.
6. RGS_HS, RGS_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
7. Overcurrent/Shoot-through detection is not implemented.

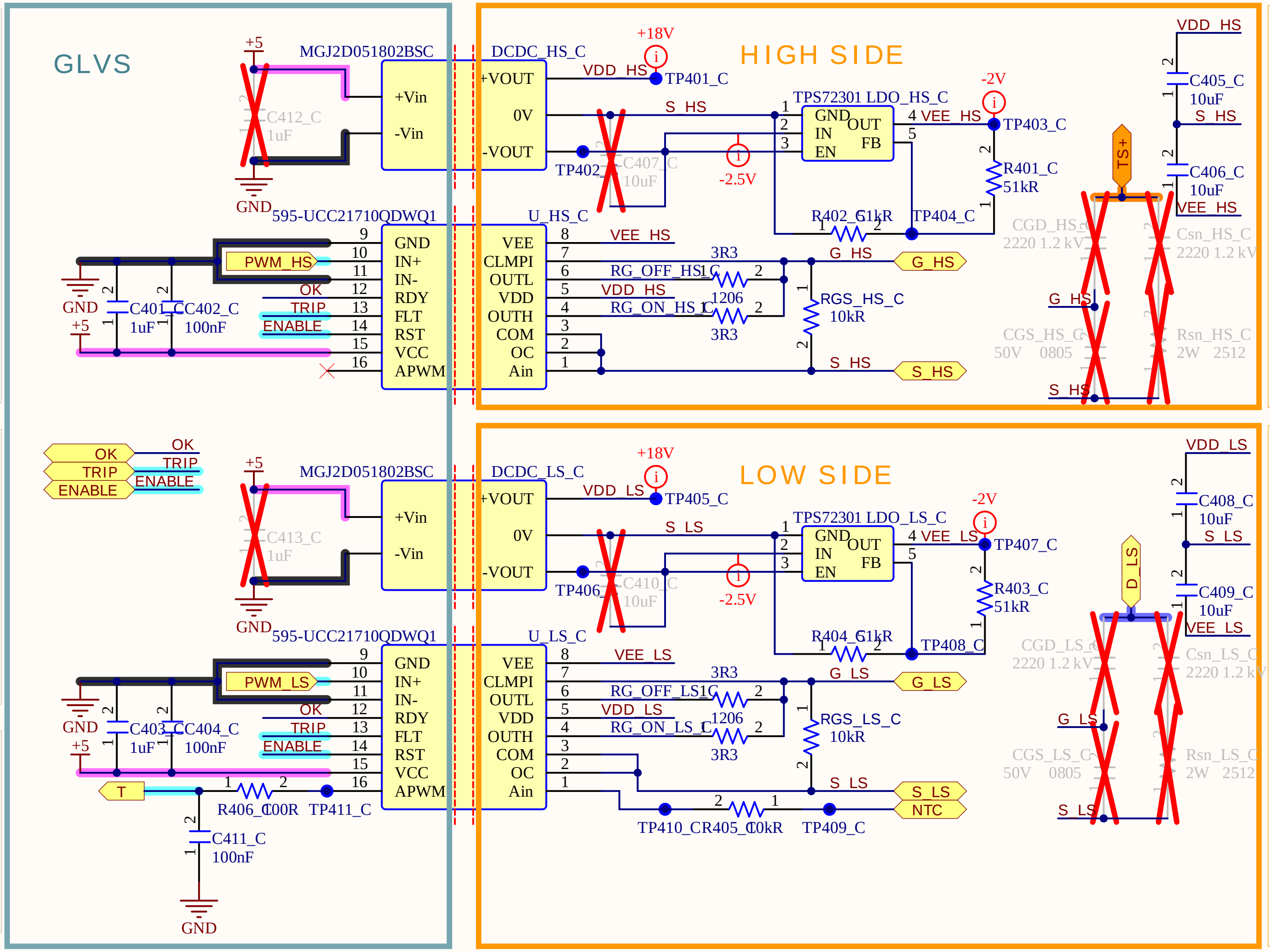
LDO_HS, LDO_LS

An LDO is implemented to trim VEE_HS_A and VEE_LS_A during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, DCDC_HS and DCDC_LS must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing
V_GS = +18 V / -2 V
VEE = - 1.186 · (1 + R1/R2)
R1 + R2 ≈ 100 kΩ

DCDC_HS, DCDC_LS
Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS
VIOTM (t = 60 s (qualification test)): 8000 VPK



V_GS values:

The values chosen for V_GS are +18 / -2 V. Even though Leapers recommends using +18 / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum V_GS(th). A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:
I_GD(min) = f_sw · Q_G = 50 kHz · 520 nC = 26 mA
P_min = ΔV_GS · I_GD(min) = 20 V · 26 mA = 0.52 W → 2 W

RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS, CGS_LS, CGD_HS, CGD_LS, Csn_HS, Csn_LS, Rsn_HS, Rsn_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could result in further issues with the power limit for DCDC_HS and DCDC_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

CGS_max = 2 · P_DCDC / (ΔV_GS ^2 · f_sw) = 2 · 2 W / ((20 V)^2) · 50 kHz) = 200 nF

Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Inverter_Power		
Size: -	Page Contents: [4] Half_Bridge.SchDoc	Version: 1.0	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5	
Checked by: _		Date: 14/02/2024	

Discharge resistors:

t_dis = R_dis · C · ln(V_initial/V_final) = (470 kΩ / 24) · (100 µF) · ln(600 V / 60 V) = 4.509 s

P(R_dis, max) = V_max^2 / R_dis = 600 V^2 / 470 kΩ = 0.766 W < 1 W

I_dis, max = 600 V / (470 kΩ / 24) = 30.64 mA

R501

For U501 , the recommended diode forward current is 10 mA. SC_END can be between 20 V and 30 V.

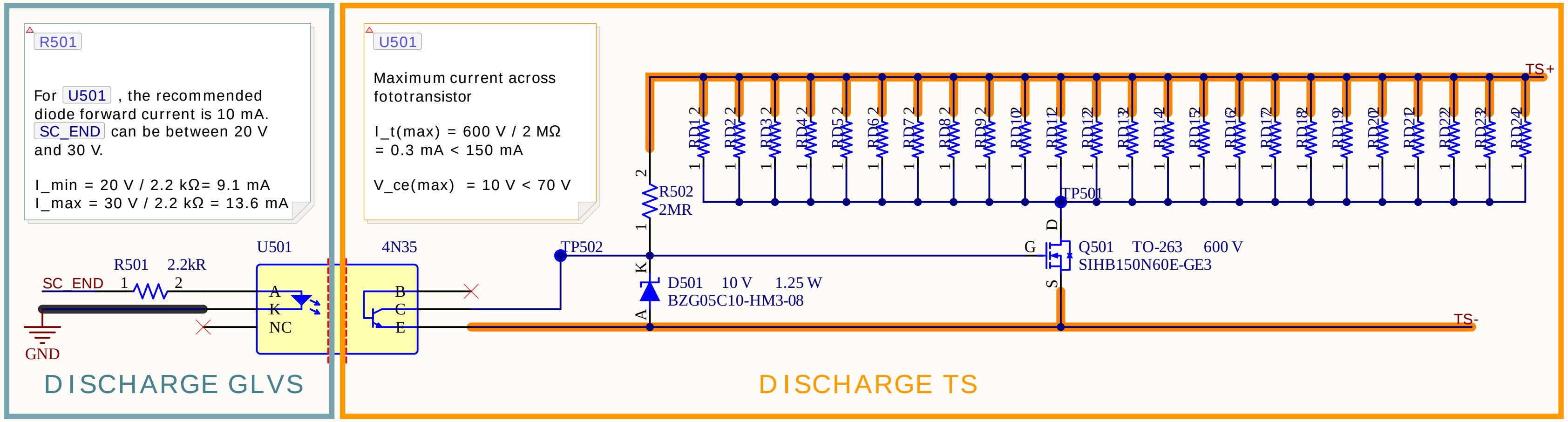
I_min = 20 V / 2.2 kΩ= 9.1 mA
I_max = 30 V / 2.2 kΩ = 13.6 mA

U501

Maximum current across fototransistor

I_t(max) = 600 V / 2 MΩ = 0.3 mA < 150 mA

V_ce(max) = 10 V < 70 V



U503

Single supply configuration as per datasheet.

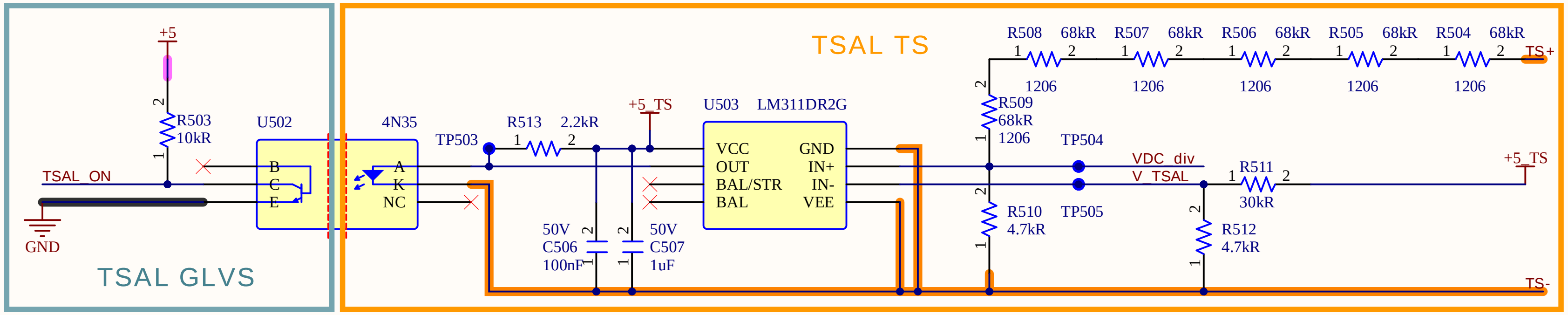
Maximum differential input voltage = 6.833 V - 677 mV = 6.156 V < 30 V

VDC_div = (TS+ - TS-) · 4.7 kΩ / (4.7 kΩ + 6 · 68 kΩ)

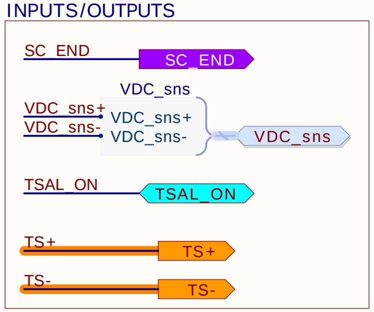
600 V · 4.7 kΩ / (4.7 kΩ + 6 · 68 kΩ) = 6.833 V
60 V · 4.7 kΩ / (4.7 kΩ + 6 · 68 kΩ) = 683 mV

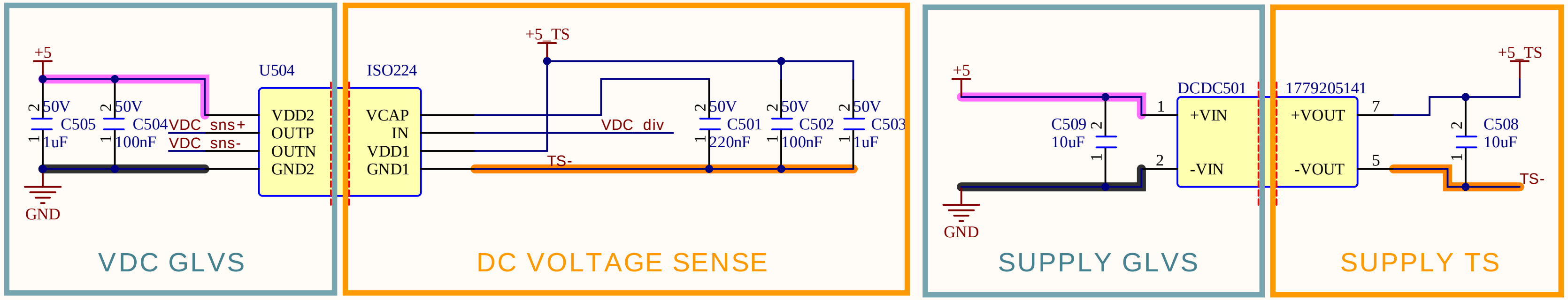
P_R4 = I_R4^2 · R4 = ((600 V / (4.7 kΩ + 6 · 68 kΩ)) / 68 kΩ)^2 · 68 kΩ = 144 mW → 1206 package

V_TSAL = 5 V · 4.7 kΩ / (4.7 kΩ + 30 kΩ) = 677 mV ≡ 59.46 V in TS+ - TS-



INPUTS/OUTPUTS





(TS+ - TS-) > 60V → TSAL_ON = 0V

(TS+ - TS-) < 60V → TSAL_ON = 5V

U504

(VDC_sns+ - VDC_sns-) = 1/3 · VDC_div = 1/3 · ((TS+ - TS-) 4.7 kΩ / (4.7 kΩ + 6 · 68 kΩ)) = 1/3 · 0.011388 · (TS+ - TS-)

(VDC_sns+ - VDC_sns-) = 1/3 · 0.011388 · 600 V = 2.278 V

U501 , U502

Isolation Voltage: AC For 1 Minute, R.H. = 40 ~ 60% Viso = 5000 Vrms

U504

Maximum transient isolation voltage: VTEST = VIOTM, t = 60 s (qualification test) VIOTM = 7071 Vpk

DCDC501

Isolation voltage input to output, tested 100% for 60s(2) VISO = 3000 V

Company: e-Tech Racing	e-techracing.es		
Project: Inverter Power	Variant: Inverter_Power		
Size: -	Page Contents: [5] DC.SchDoc	Version: 1.0	
		Department: Powertrain	
Author: David Redondo	dredondovinolo@gmail.com	Sheet * of *	
Checked by: _		Date: 14/02/2024	

A
B
C
LV
TS
GND GND
+5V +5V
TSAL VDC+
SC VDC-
AUX1 AUX2
PWM6 PWM5
PWM4 PWM3
PWM2 PWM1
I_C TRIP
I_A I_B
T_C ENA
T_A T_B
GND GND
MPA
MPB
MPC
CSA
CSB
CSC
HB_A
HB_B
HB_C
DIN912
M2.5x08
0.4 N·m
DIN912
M4x06
2 N·m
DIN912 M4x16
DIN980 M4
DIN125 M4
Warning
High voltage
Warning
High temperatures
David Redondo

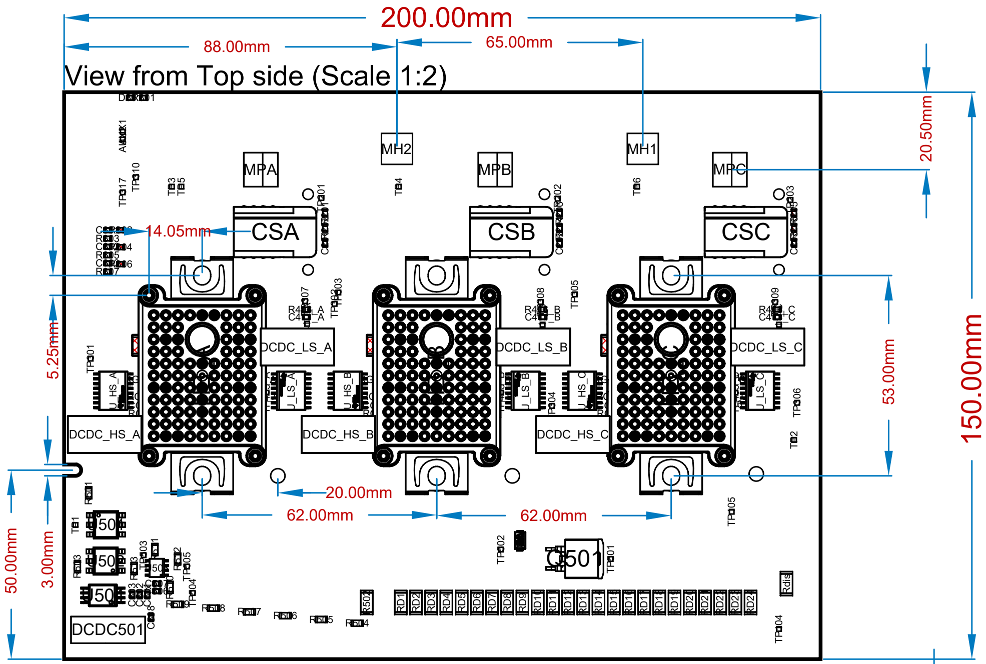
GND GND
+5V +5V
TSAL VDC+
SC VDC-
AUX1 AUX2
PWM6 PWM5
PWM4 PWM3
PWM2 PWM1
I_C TRIP
I_A I_B
T_C ENA
T_A T_B
GND GND
LV
A
B
C
MPA
MPB
MPC
CSA
CSB
CSC
HB_A
HB_B
HB_C
DIN912
M2.5x08
0.4 N·m
DIN912
M4x06
2 N·m
DIN912 M4x16
DIN980 M4
DIN125 M4
Warning
High voltage
TS
Warning
High temperatures
DC501
David Redondo

GND GND
+5V +5V
TSAL VDC+
SC VDC-
AUX1 AUX2
PWM6 PWM5
PWM4 PWM3
PWM2 PWM1
I_C TRIP
I_A I_B
T_C ENA
T_A T_B
GND GND
LV
A
B
C
MPA
MPB
MPC
CSA
CSB
CSC
HB_A
HB_B
HB_C
DIN912
M2.5x08
0.4 N·m
DIN912
M4x06
2 N·m
DIN912 M4x16
DIN980 M4
DIN125 M4
TS
Warning
High voltage
Warning
High temperatures
DC501
David Redondo

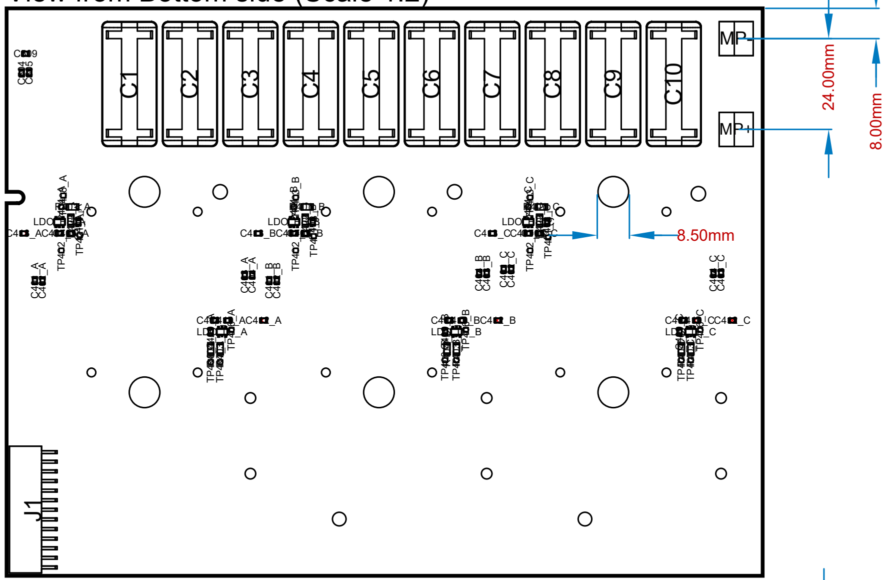
GND GND
+5V +5V
TSAL VDC+
SC VDC-
AUX1 AUX2
PWM6 PWM5
PWM4 PWM3
PWM2 PWM1
I_C TRIP
I_A I_B
T_C ENA
T_A T_B
GND GND
LV
A
B
C
MPA
MPB
MPC
CSA
CSB
CSC
HB_A
HB_B
HB_C
R405_A
R405_B
R405_C
RG_OFF_HS_A
RG_ON_HS_A
RGS_LS_A
RG_ON_LS_A
RG_OFF_LS_A
RG_OFF_HS_B
RG_ON_HS_B
RGS_LS_B
RG_ON_LS_B
RG_OFF_LS_B
RG_OFF_HS_C
RG_ON_HS_C
RGS_LS_C
RG_ON_LS_C
RG_OFF_LS_C
DIN912
M2.5x08
0.4 N·m
DIN912
M4x06
2 N·m
DIN912 M4x16
DIN980 M4
DIN125 M4
Warning
High voltage
TS
Warning
High temperatures
DC501
David Redondo

Inverter Power

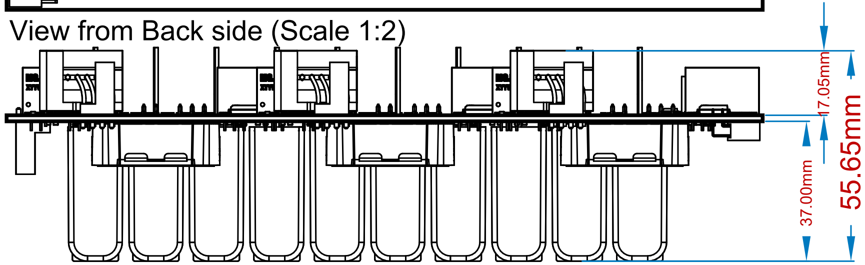
View from Top side (Scale 1:2)



View from Bottom side (Scale 1:2)



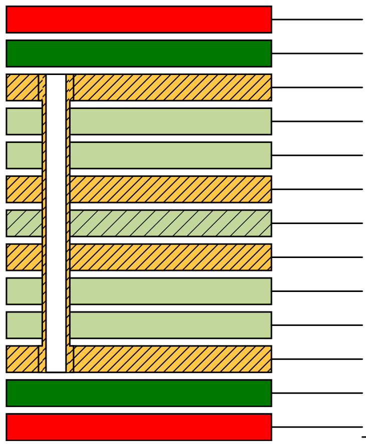
View from Back side (Scale 1:2)



Bill Of Materials

Designator	Name	Quantity
C405_A, C405_B, C405_C, C406_A, C406_B, C406_C, C408_A, C408_B, C408_C, C409_A, C409_B, C409_C, C508, C509	10uF	14
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	10uF 850V	10
DCDC501	1779205141	1
J1	613026243121	1
R503	CRCW120610K0FKEA	1
R511	CRCW120630K0FKEA	1
HB_A, HB_B, HB_C	DFS05HF12EYR1	3
MP-, MP+, MPA, MPB, MPC	M4	5
MH1, MH2	Mounting_Hole_M4	2
RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24	RCV2512470KFKEG	24
R406_A, R406_B, R406_C	CR0805-FX-1000ELF	3
R301	CR0805-JW-102ELF	1
R405_A, R405_B, R405_C, RGS_HS_A, RGS_HS_B, RGS_HS_C, RGS_LS_A, RGS_LS_B, RGS_LS_C	CR0805-JW-103ELF	9
R504, R505, R506, R507, R508, R509	CR1206AFX-6802EAS	6
R501, R513	CR1206-FX-2201ELF	2
R510, R512	CRS1206-FX-4701ELF	2
CSA, CSB, CSC	LEM CKSR 50-NP	3
DCDC_HS_A, DCDC_HS_B, DCDC_HS_C, DCDC_LS_A, DCDC_LS_B, DCDC_LS_C	MGJ6-series	6
U503	LM311DR2G	1
R401_A, R401_B, R401_C, R402_A, R402_B, R402_C, R403_A, R403_B, R403_C, R404_A, R404_B, R404_C	CRCW120610K0FKEA	12
C501	885012208058	1
RG_OFF_HS_A, RG_OFF_HS_B, RG_OFF_HS_C, RG_OFF_LS_A, RG_OFF_LS_B, RG_OFF_LS_C, RG_ON_HS_A, RG_ON_HS_B, RG_ON_HS_C, RG_ON_LS_A, RG_ON_LS_B, RG_ON_LS_C	CRG1206F100R	12
U504	ISO224	1
LDO_HS_A, LDO_HS_B, LDO_HS_C, LDO_LS_A, LDO_LS_B, LDO_LS_C	TPS72301	6
U_HS_A, U_HS_B, U_HS_C, U_LS_A, U_LS_B, U_LS_C	UCC21710	6
Q501	SIHB150N60E-GE3	1
R502, Rdis	R2M-2512FTK	2
U501, U502	4N35	2
D501	BZG05C10	1
D301	150080GS75000	1
C201, C202, C203, C402_A, C402_B, C402_C, C404_A, C404_B, C404_C, C411_A, C411_B, C411_C, C502, C504, C506	885012207098	15
C401_A, C401_B, C401_C, C403_A, C403_B, C403_C, C503, C505, C507	885012207103	9

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
CF-004	**TOP**	**0.07mm**		**Signal**	**GTL**
Prepreg		*0.10mm*	*PP-006*	*Dielectric*	
Prepreg		*0.10mm*	*PP-006*	*Dielectric*	
Copper	**GND**	**0.07mm**		**Signal**	**G1**
		0.90mm	*FR-4*	*Dielectric*	
Copper	**PWR**	**0.07mm**		**Signal**	**G2**
Prepreg		*0.10mm*	*PP-006*	*Dielectric*	
Prepreg		*0.10mm*	*PP-006*	*Dielectric*	
CF-004	**BOT**	**0.07mm**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.60mm