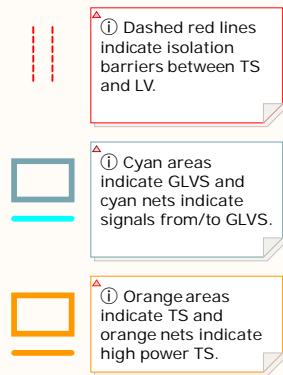


A



**Specifications:**

V<sub>in</sub>, max = 600 VDC  
V<sub>out</sub>, max = 245 VRMS (SVPWM)  
f<sub>sw</sub> = 50 kHz  
P<sub>out</sub>, max = 40kW  
I<sub>out</sub>, max = 80 ARMS

Liquid cooled with water at 50°C max

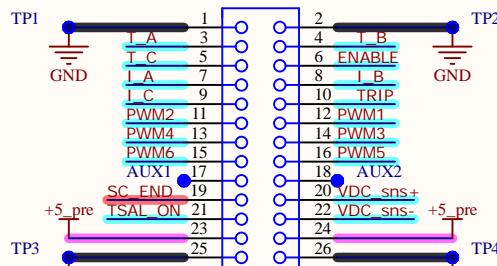
**Changelog:**

Version 1.0:  
- Base version, sent to production 15-02-2024

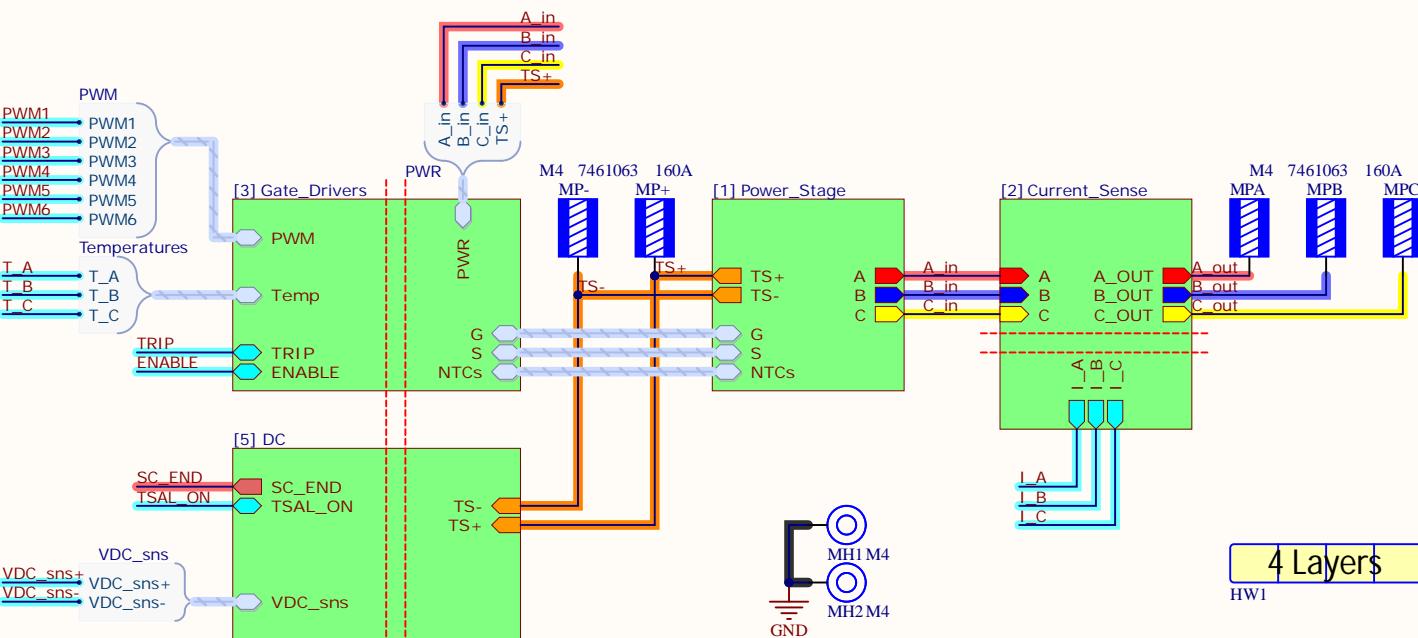
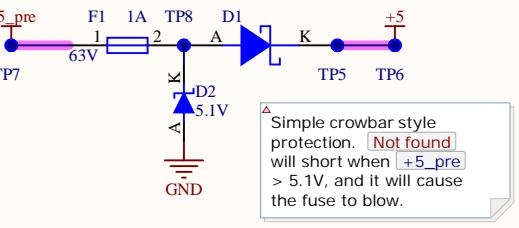
Version 1.1:  
- Added 5V supply protections  
- Swapped pins 4 and 5 in gate drivers' LDOs  
- Swapped MP+ and MP-, and their silkscreen  
- Added testpoints for current sensors' reference  
- Added testpoints for VDC\_sns+ and VDC\_sns-

- Renamed testpoints in [3]  
- Added various silkscreen texts and indications

## LV Connector

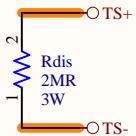


## OCP, OVP, reverse

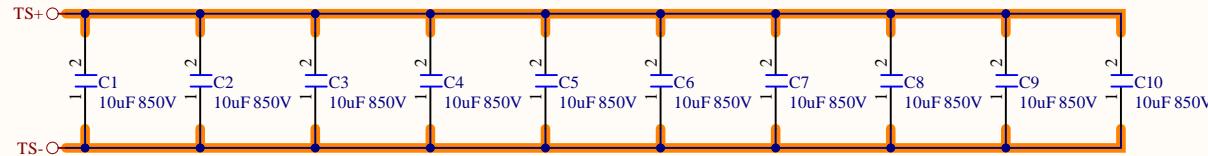


|             |   |                          |              |
|-------------|---|--------------------------|--------------|
| Company:    | e-Tech Racing                           | e-techracing.es          |              |
| Project:    | Inverter Power                          | Variant: Wolfspeed       |              |
| Size:       | Page Contents:<br>Inverter_Power.SchDoc | Version: 1.1             |              |
|             |   | Department: Powertrain   |              |
| Author:     | David Redondo                           | dredondovinolo@gmail.com | Sheet 1 of 5 |
| Checked by: |   | Date: 20/03/2024         |              |

## Passive discharge



## DC Bus capacitors, 100uF, Murata FHA85Y106KS



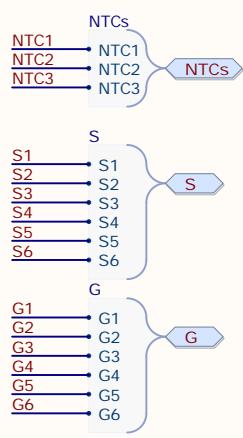
### DC Link design considerations:

$V_C > 1.1 \cdot V_{max} = 1.1 \cdot 600 V = 660 V \rightarrow 850 V$

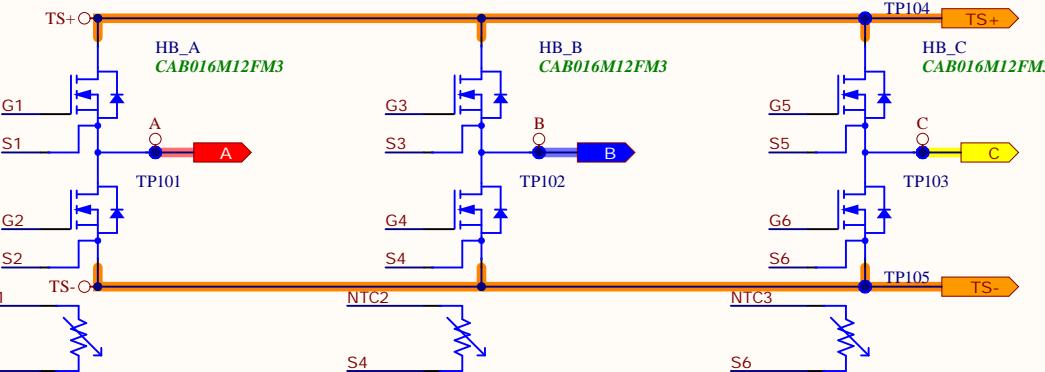
$I_{C,RMS} \approx 0.65 \cdot I_{phase,RMS} = 0.65 \cdot 80 A, RMS = 52 A, RMS \rightarrow 10 \times 5 A, RMS (\Delta T = 10 ^\circ C)$   
 $C > I_{C,RMS} / (V_{ripple} \cdot f_{sw}) = 52 A, RMS / (15V \cdot 50 kHz) \approx 79 \mu F \rightarrow 10 \times 10 \mu F$

Lowering the switching frequency will proportionally lower the current rating for the same voltage ripple or proportionally increase the voltage ripple for the same output current. Check:  
<https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter>

## INPUTS/OUTPUTS



## SiC Half-Bridges



### Semiconductor details:

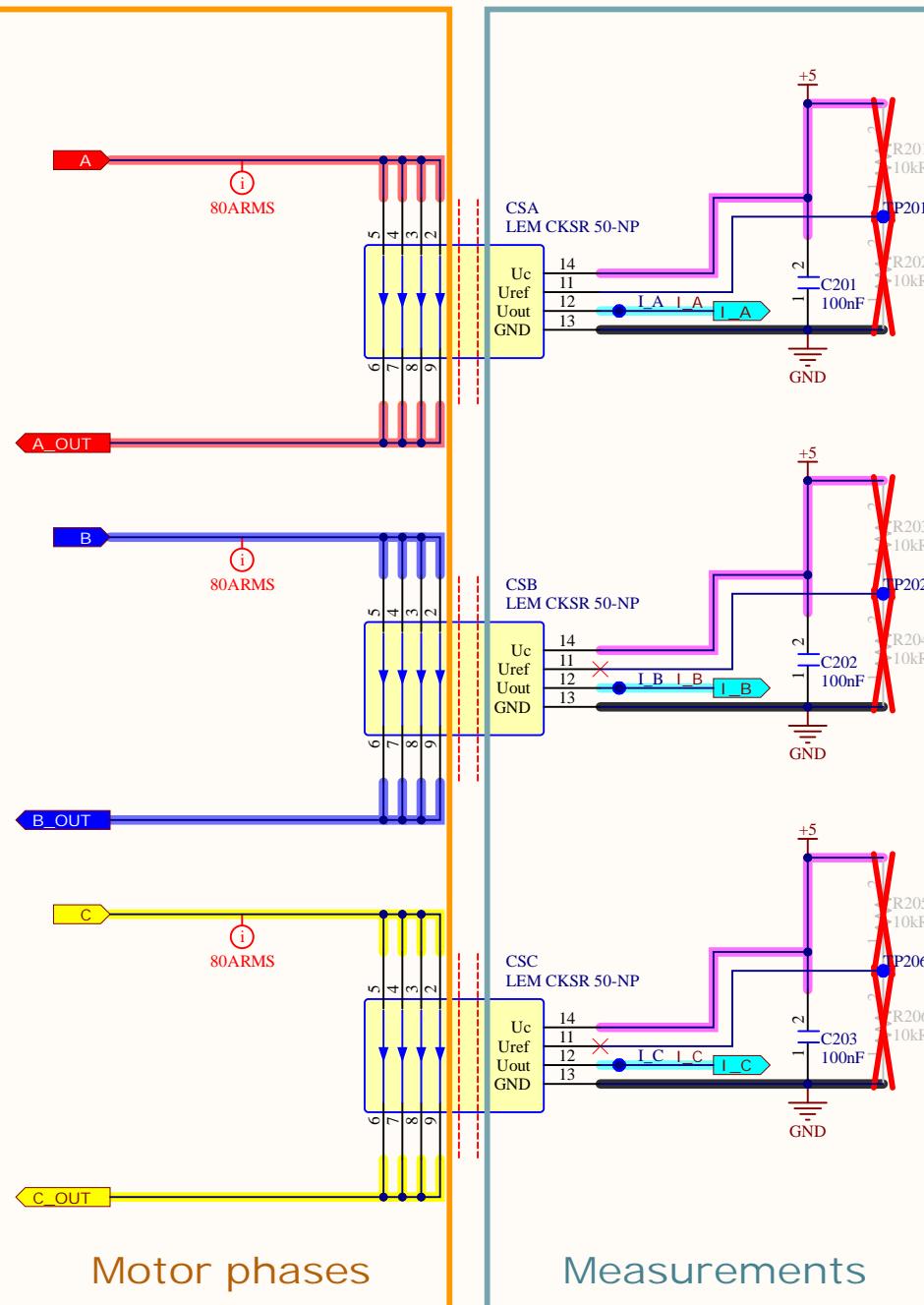
$V_{DSS}(\text{breakdown}) = 1200 V // 1200 V$   
 $R_{on} = 5.5 .. 13 m\Omega // 16.0 .. 28.8 m\Omega$   
 $V_f_{D} = 3.3 .. 4 V // 4.9 .. 5.5 V$   
 $T_{rr} = 41.5 .. 45 ns // 20.0 ns$   
 $Q_{rr} = 2.19 .. 3.94 \mu C // 1.30 \mu C$   
 $R_{th,Jc} = 0.12 .. 0.15 K/W // 0.543 K/W$   
 $Q_G = 520 nC // 236 nC$   
 $C_{in} = 14.5 nF // 6.6 nF$   
 $R_G(\text{int}) = 1.9 \Omega // 2.4 \Omega$   
 $V_{GS(th)} = 2.8 .. 4.8 V // 1.8 .. 3.6 V$

|             |  |                          |              |
|-------------|--|--------------------------|--------------|
| Company:    | e-Tech Racing                            | e-techracing.es          |              |
| Project:    | Inverter Power                           | Variant: Wolfspeed       |              |
| Size:       | Page Contents:<br>[1]Power_Stages.SchDoc | Version: 1.1             |              |
| -           |  | Department: Powertrain   |              |
| Author:     | David Redondo                            | dredondovinolo@gmail.com | Sheet 2 of 5 |
| Checked by: | _  | Date: 20/03/2024         |              |

A

CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R\_phase-connector = 0.18 mΩ)



CSA , CSB , CSC

AC insulation test  
RMS voltage, 50 Hz,  
1 min:

$U_d = 4.3 \text{ kV} >$   
 $3 \cdot V_{\text{max}} = 1.8 \text{ kV}$

CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values.  
Voltage divider implemented just in case.

I\_A , I\_B , I\_C

$$U_{\text{meas}} = (12.5 \text{ mV/A} \cdot I_{\text{meas}} + U_{\text{ref}})$$

For  $\pm 150 \text{ Apk}$ :  
 $V_{\text{meas\_pk+}} = 4.375 \text{ V}$   
 $V_{\text{meas\_pk-}} = 0.625 \text{ V}$

C201 , C202 , C203

The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

|             |   |                          |              |
|-------------|---|--------------------------|--------------|
| Company:    | e-Tech Racing                             | e-techracing.es          |              |
| Project:    | Inverter Power                            | Variant:                 | Wolfspeed    |
| Size:       | Page Contents:<br>[2]Current_Sense.SchDoc | Version:                 | 1.1          |
| -           |   | Department:              | Powertrain   |
| Author:     | David Redondo                             | dredondovinolo@gmail.com | Sheet 3 of 5 |
| Checked by: | _   | Date:                    | 20/03/2024   |

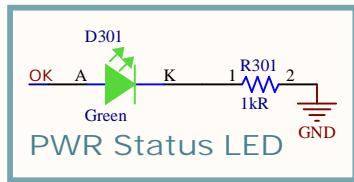
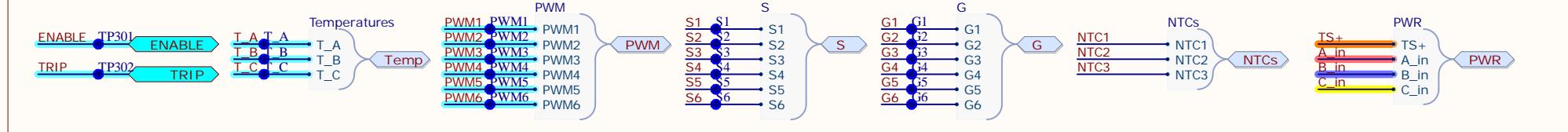
1

2

3

4

## INPUTS/OUTPUTS



**[T\_A], [T\_B], [T\_C]**

Look-up table obtained with MATLAB script which can be found in the simulations folder.

For different temperatures:

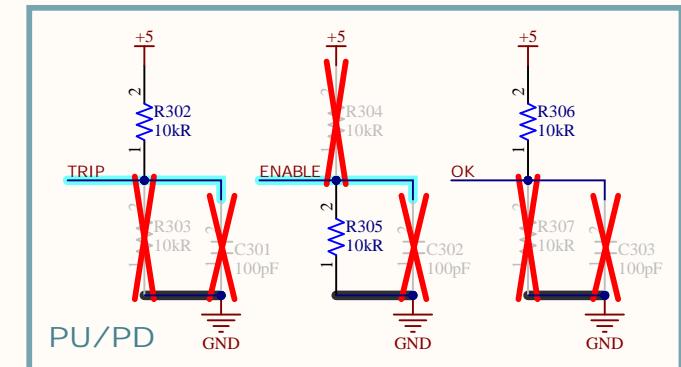
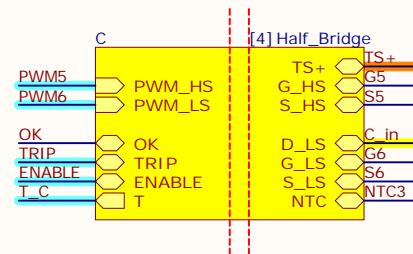
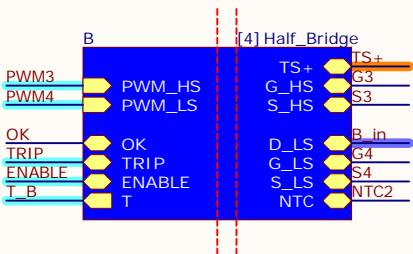
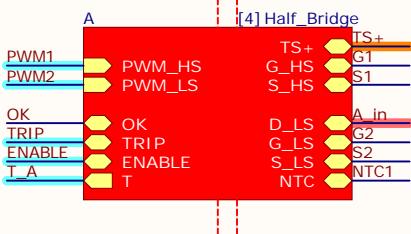
- V<sub>meas</sub>(0°C) = 0.246V
- V<sub>meas</sub>(25°C) = 2V
- V<sub>meas</sub>(50°C) = 2.578V
- V<sub>meas</sub>(90°C) = 2.864V

B

B

C

C



|             |  |                          |                  |
|-------------|--|--------------------------|------------------|
| Company:    | e-Tech Racing                            | e-techracing.es          |                  |
| Project:    | Inverter Power                           | Variant: Wolfspeed       |                  |
| Size:       | Page Contents:<br>[3]Gate_Drivers.SchDoc | Version: 1.1             |                  |
| -           |  | Department: Powertrain   |                  |
| Author:     | David Redondo                            | dredondovinolo@gmail.com | Sheet 4 of 5     |
| Checked by: |  |                          | Date: 20/03/2024 |

1

2

3

4

A

**U\_HS, U\_LS**

- TRIP and OK signals are in open drain configuration, so they can be paralleled.
- IN- is not used and tied to GND.
- ENABLE to be given by MCU in active-high mode. When set to low for more than 1  $\mu$ s, TRIP is reset.
- Temperature sensing using low-side drivers. Ain outputs a current of 200  $\mu$ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. R405, R406 and C411 from SPICE simulation.
- Miller clamp protection is used.
- RGS\_HS, RGS\_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
- Overcurrent detection is not implemented.

**LDO\_HS, LDO\_LS**

An LDO is implemented to trim VEE\_HS\_A and VEE\_LS\_A during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

$$\text{VEE} = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers  $\rightarrow R1 = 36 \text{ k}\Omega$ ,  $R2 = 56 \text{ k}\Omega$

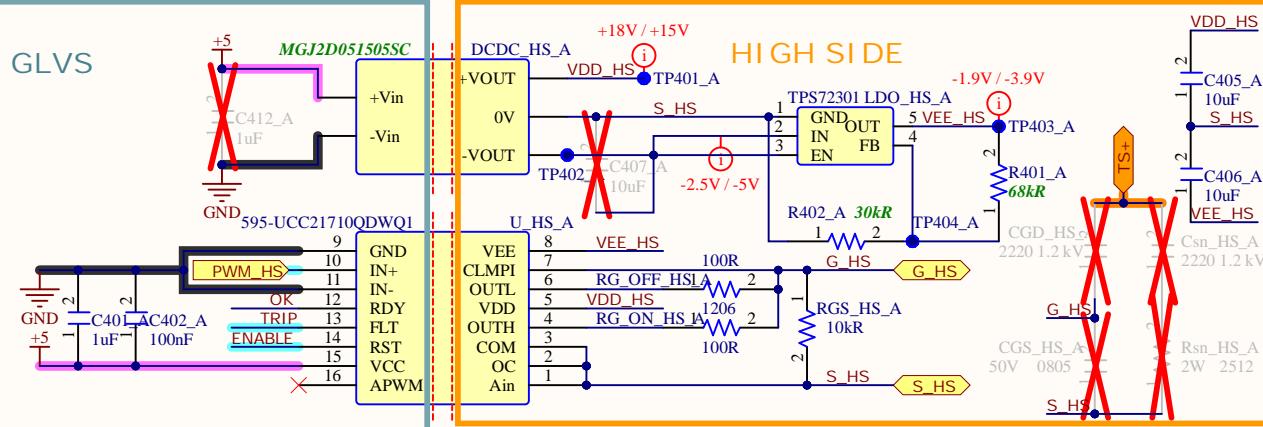
Wolfspeed  $\rightarrow R1 = 68 \text{ k}\Omega$ ,  $R2 = 30 \text{ k}\Omega$

**DCDC\_HS, DCDC\_LS**

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

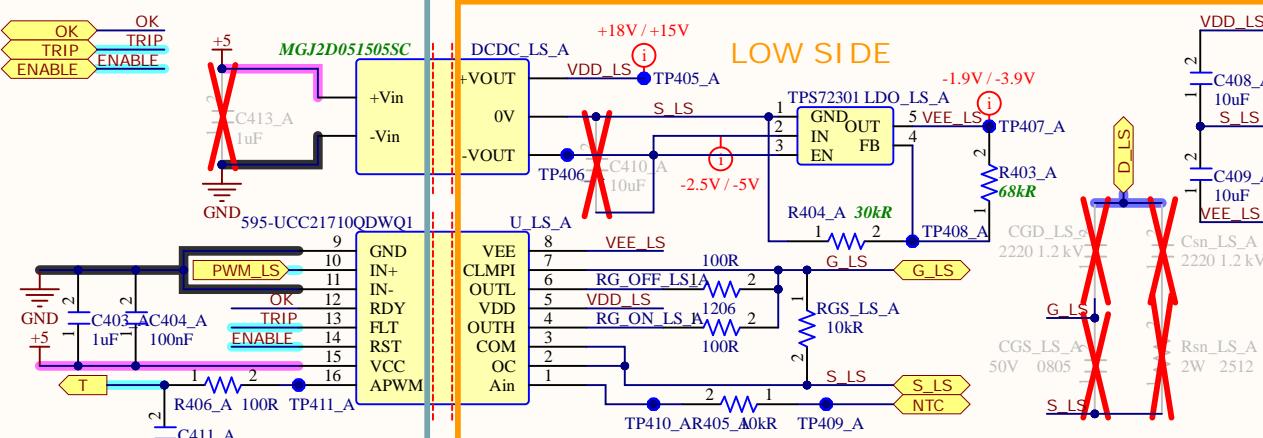
**U\_HS, U\_LS**

VIOTM ( $t = 60$  s (qualification test)): 8000 VPK

**GLVS****HIGH SIDE****V\_GS values:**

The values can be modified by replacing DCDC\_HS and DCDC\_LS with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

Minimum gate driver current and power:  
 $I_{GD(\min)} = f_{sw} \cdot O_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$   
 $P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

**OK, TRIP, ENABLE****LOW SIDE****RG\_ON\_HS, RG\_OFF\_HS, RG\_ON\_LS, RG\_OFF\_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3  $\Omega$  are recommended by the datasheet.

CGS\_HS, CGS\_LS, CGD\_HS, CGD\_LS, Csn\_HS, Csn\_LS, Rsn\_HS, Rsn\_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could help in these issues with the power limit for DCDC\_HS and DCDC\_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

Company: e-Tech Racing e-techracing.es



Project: Inverter Power Variant: Wolfspeed

|       |   |                        |
|-------|---|------------------------|
| Size: | Page Contents:<br>[4]Half_Bridge.SchDoc | Version: 1.1           |
|       |   | Department: Powertrain |

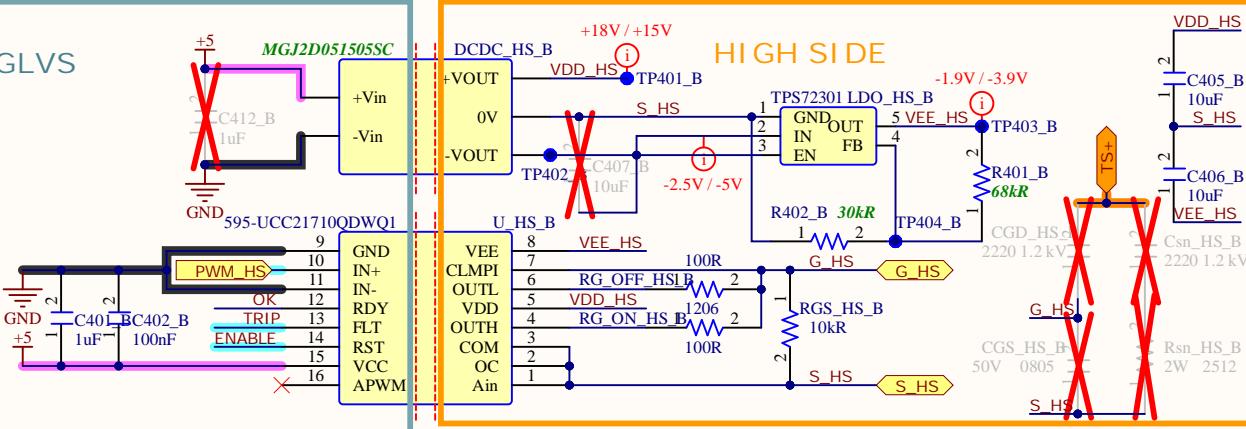
Author: David Redondo dredondovinolo@gmail.com Sheet 5 of 5

Checked by: Date: 20/03/2024

A

**U\_HS, U\_LS**

- TRIP and OK signals are in open drain configuration, so they can be paralleled.
- IN- is not used and tied to GND.
- ENABLE to be given by MCU in active-high mode. When set to low for more than 1  $\mu$ s, TRIP is reset.
- Temperature sensing using low-side drivers. Ain outputs a current of 200  $\mu$ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. [R405], [R406] and [C411] from SPICE simulation.
- Miller clamp protection is used.
- RGS\_HS, RGS\_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
- Overcurrent detection is not implemented.

**GLVS**

B

**LDO\_HS, LDO\_LS**

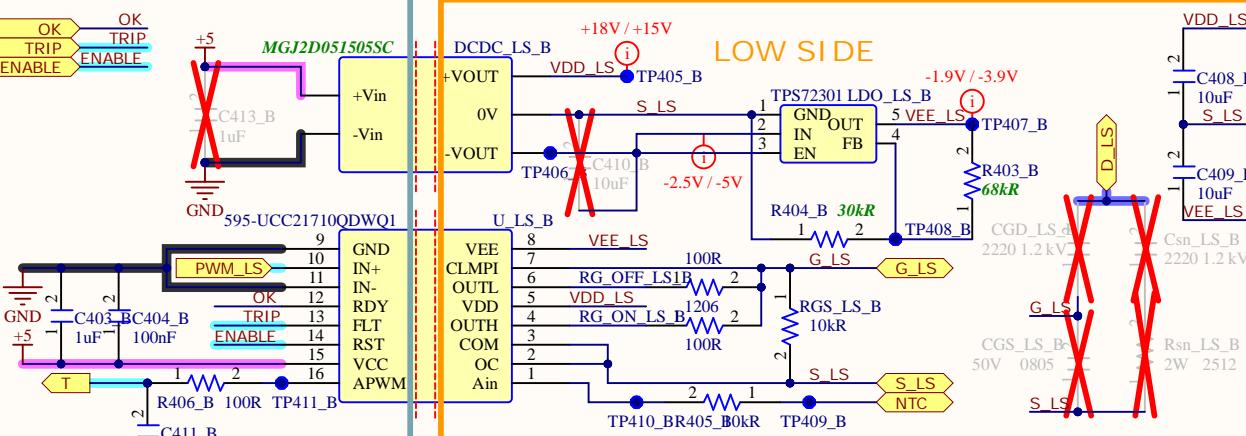
An LDO is implemented to trim VEE\_HS\_A and VEE\_LS\_A during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

$$\text{VEE} = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers  $\rightarrow R1 = 36 \text{ k}\Omega$ ,  $R2 = 56 \text{ k}\Omega$

Wolfspeed  $\rightarrow R1 = 68 \text{ k}\Omega$ ,  $R2 = 30 \text{ k}\Omega$

**OK  
TRIP  
ENABLE**

C

**DCDC\_HS, DCDC\_LS**

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

**U\_HS, U\_LS**

VIOTM ( $t = 60$  s (qualification test)): 8000 VPK

**T****V\_GS values:**

The values can be modified by replacing DCDC\_HS and DCDC\_LS with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

Minimum gate driver current and power:  
 $I_{GD(\min)} = f_{sw} \cdot O_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$   
 $P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

**RG\_ON\_HS, RG\_OFF\_HS,  
RG\_ON\_LS, RG\_OFF\_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3  $\Omega$  are recommended by the datasheet.

CGS\_HS, CGS\_LS, CGD\_HS, CGD\_LS, Csn\_HS, Csn\_LS, Rsn\_HS, Rsn\_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could avoid issues with the power limit for DCDC\_HS and DCDC\_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

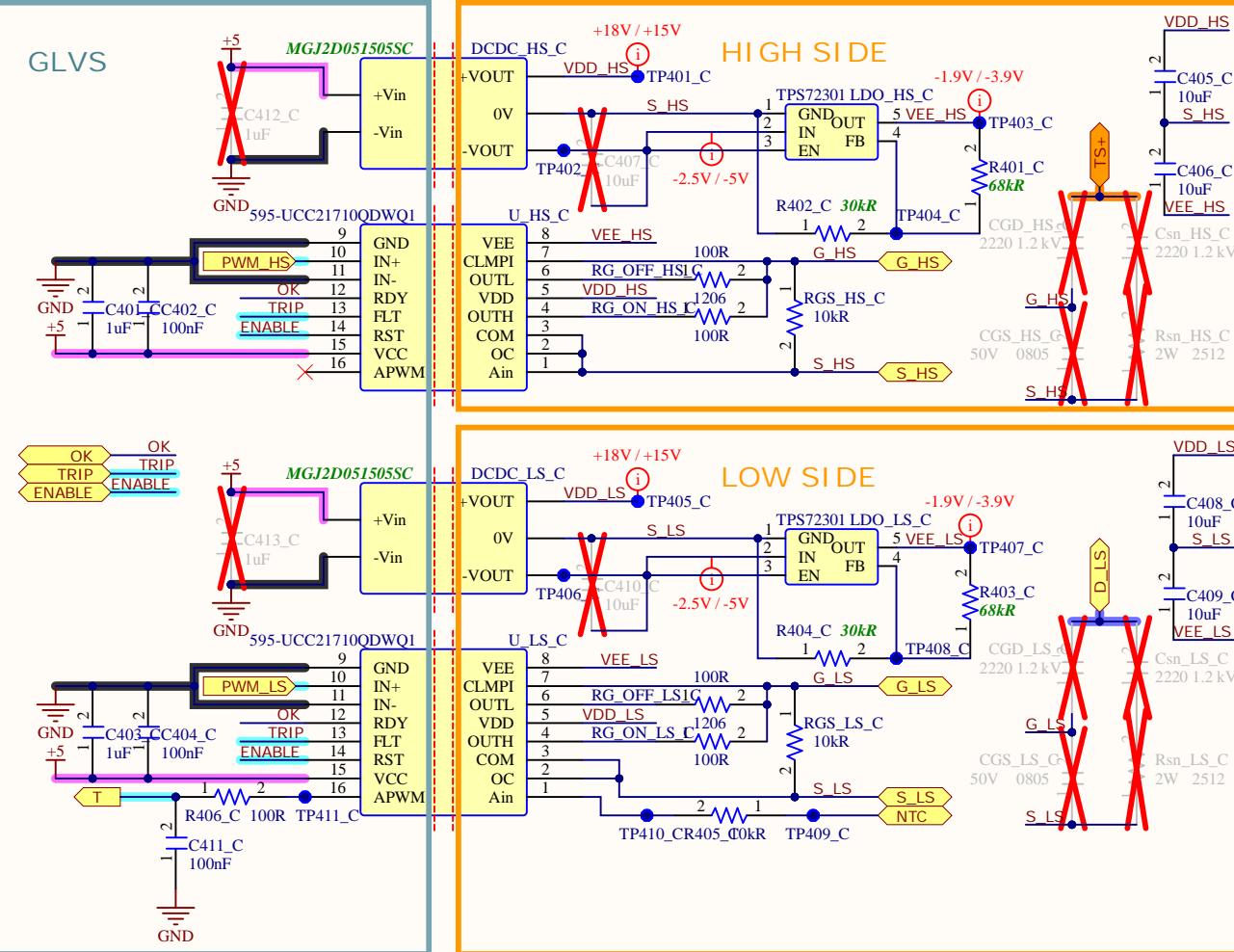
$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

|             |   |                          |                  |
|-------------|---|--------------------------|------------------|
| Company:    | e-Tech Racing                           | e-techracing.es          |                  |
| Project:    | Inverter Power                          | Variant: Wolfspeed       |                  |
| Size:       | Page Contents:<br>[4]Half_Bridge.SchDoc | Version: 1.1             |                  |
| Department: | Powertrain                              |                          |                  |
| Author:     | David Redondo                           | dredondovinolo@gmail.com | Sheet 5 of 5     |
| Checked by: |   |                          | Date: 20/03/2024 |

A

**▲ U\_HS, U\_LS**

1. **TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to **GND**.
3. **ENABLE** to be given by MCU in active-high mode. When set to low for more than 1  $\mu$ s, **TRIP** is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200  $\mu$ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **[R405]**, **[R406]** and **[C411]** from SPICE simulation.
5. Miller clamp protection is used.
6. **RGS\_HS**, **RGS\_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
7. Overcurrent detection is not implemented.

**GLVS****▲ V\_GS values:**

The values can be modified by replacing **DCDC\_HS** and **DCDC\_LS** with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

Minimum gate driver current and power:  
 $I_{GD(min)} = f_{sw} \cdot O_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$   
 $P_{min} = \Delta V_{GS} \cdot I_{GD(min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

B

**▲ LDO\_HS, LDO\_LS**

An LDO is implemented to trim **VEE\_HS\_A** and **VEE\_LS\_A** during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

$$VEE = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers  $\rightarrow R1 = 36 \text{ k}\Omega$ ,  $R2 = 56 \text{ k}\Omega$

Wolfspeed  $\rightarrow R1 = 68 \text{ k}\Omega$ ,  $R2 = 30 \text{ k}\Omega$

**▲ DCDC\_HS, DCDC\_LS**

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

**▲ U\_HS, U\_LS**

VIOTM ( $t = 60 \text{ s}$  (qualification test)): 8000 VPK

**▲ RG\_ON\_HS, RG\_OFF\_HS, RG\_ON\_LS, RG\_OFF\_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the  $dV/dt$  will be higher, which can be responsible of EMI increase. The considered values of 3.3  $\Omega$  are recommended by the datasheet.

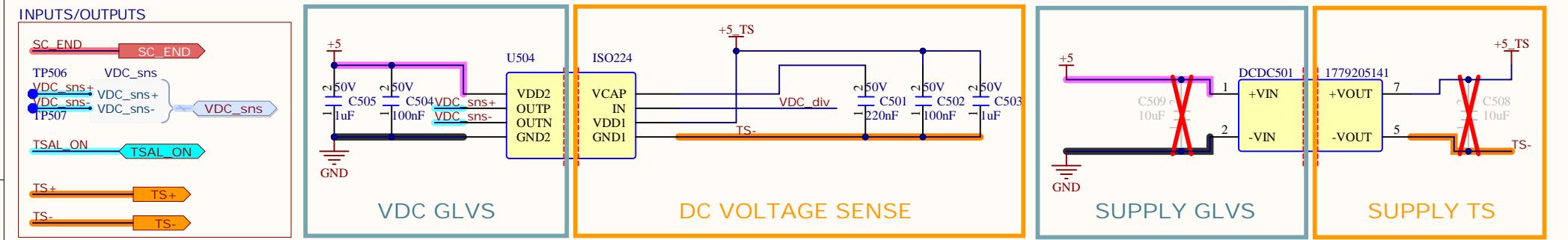
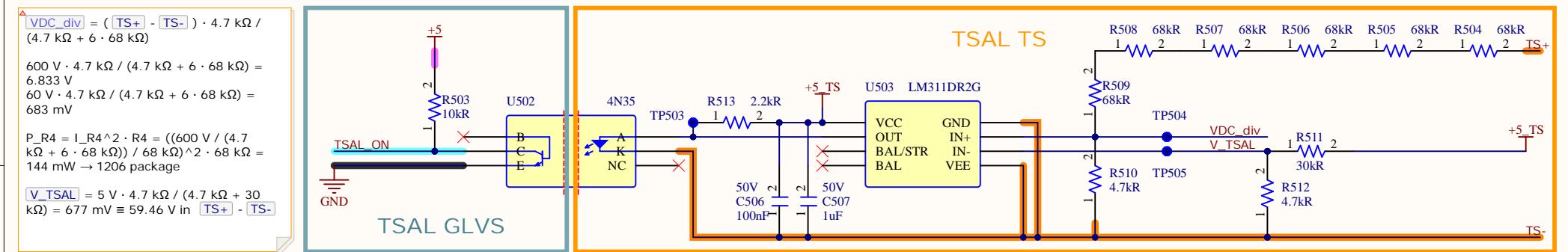
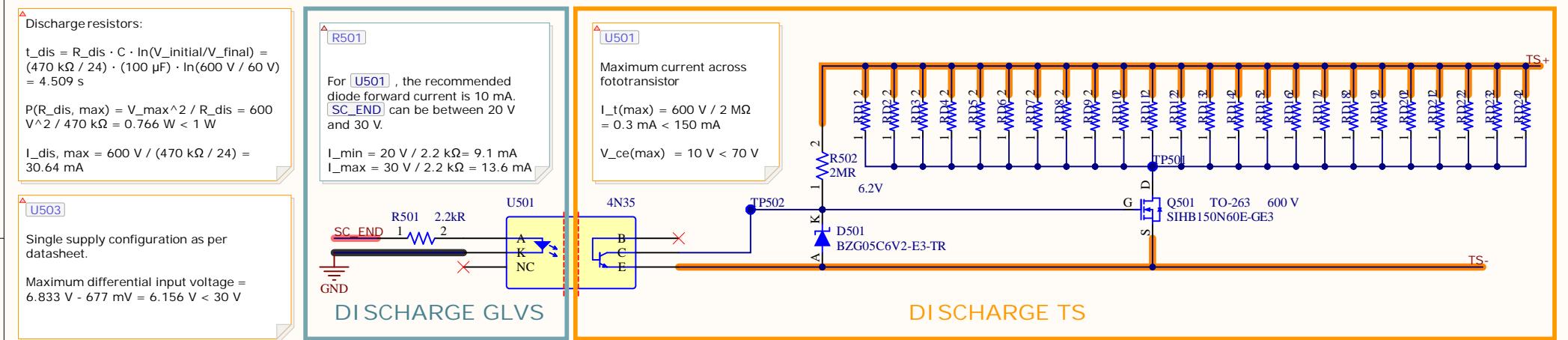
**CGS\_HS**, **CGS\_LS**, **CGD\_HS**, **CGD\_LS**, **Csn\_HS**, **Csn\_LS**, **Rsn\_HS**, **Rsn\_LS**

DNP, but they could be useful with EMI related issues to decrease  $dV/dt$ . Implementing them could avoid issues with the power limit for **DCDC\_HS** and **DCDC\_LS**, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

C

|             |   |                          |                  |
|-------------|---|--------------------------|------------------|
| Company:    | e-Tech Racing                           | e-techracing.es          |                  |
| Project:    | Inverter Power                          | Variant: Wolfspeed       |                  |
| Size:       | Page Contents:<br>[4]Half_Bridge.SchDoc | Version: 1.1             |                  |
|             |   | Department: Powertrain   |                  |
| Author:     | David Redondo                           | dredondovinolo@gmail.com | Sheet 5 of 5     |
| Checked by: |   |                          | Date: 20/03/2024 |



$\Delta$   $(TS+ - TS-) > 60V \rightarrow TSAL\_ON = 0V$   
 $(TS+ - TS-) < 60V \rightarrow TSAL\_ON = 5V$

$$\begin{aligned}
 & (\text{VDC}_{\text{sns+}} - \text{VDC}_{\text{sns-}}) = 1/3 \cdot \\
 & \text{[VDC}_\text{div} = 1/3 \cdot ((\text{TS+} - \text{TS-}) \\
 & 4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega)) = 1/3 \cdot \\
 & 0.011388 \cdot (\text{TS+} - \text{TS-}) \\
 & (\text{VDC}_{\text{sns+}} - \text{VDC}_{\text{sns-}}) = 1/3 \cdot \\
 & 0.011388 \cdot 600 \text{ V} = 2.278 \text{ V}
 \end{aligned}$$

**U501**, **U502**

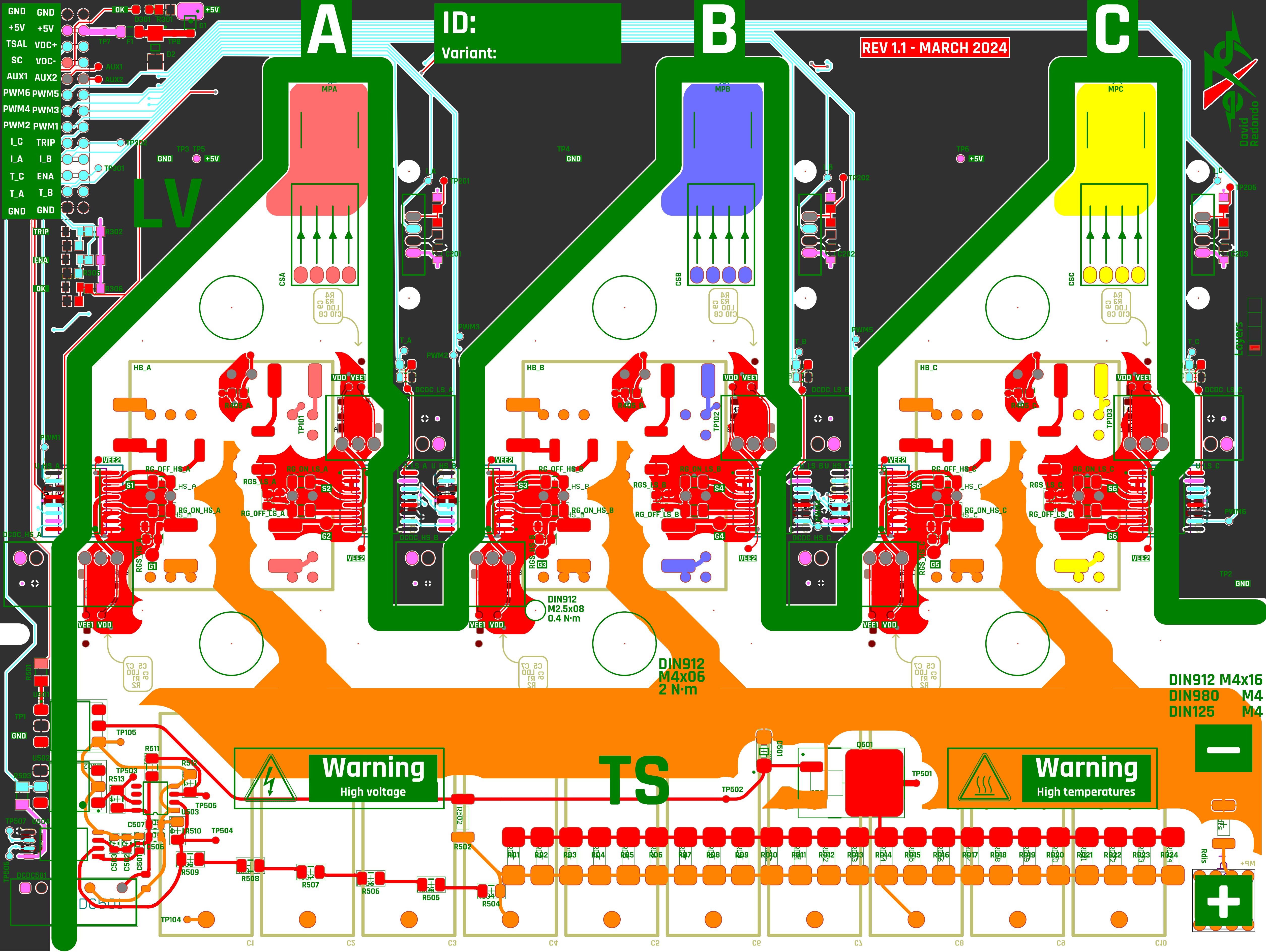
Isolation Voltage: AC For 1 Minute,  
R.H. = 40 ~ 60% Viso = 5000 Vrms

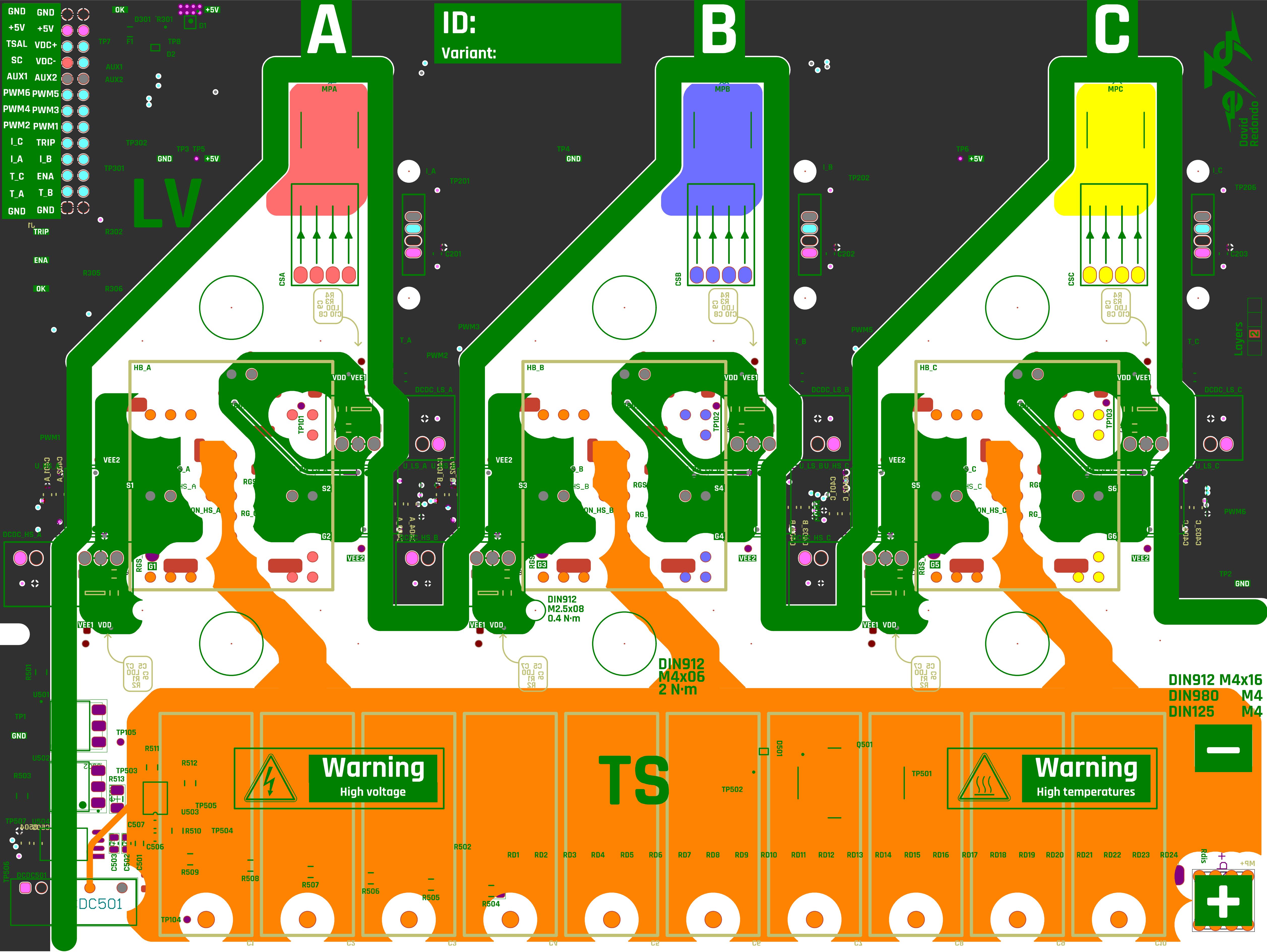
**U504**

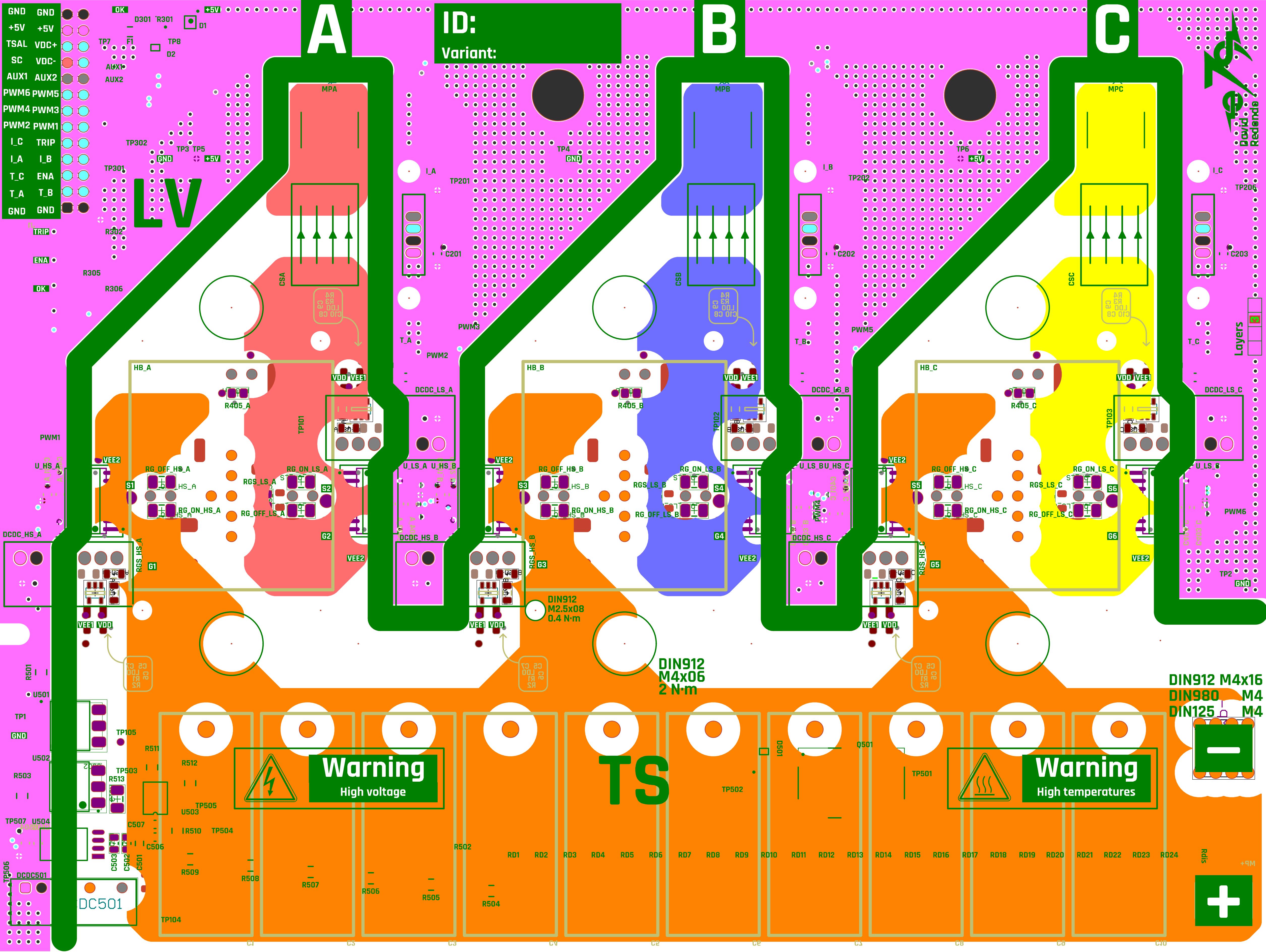
Maximum transient isolation voltage:  
VTEST = VIOTM, t = 60 s (qualification  
test) VIOTM = 7071 Vpk

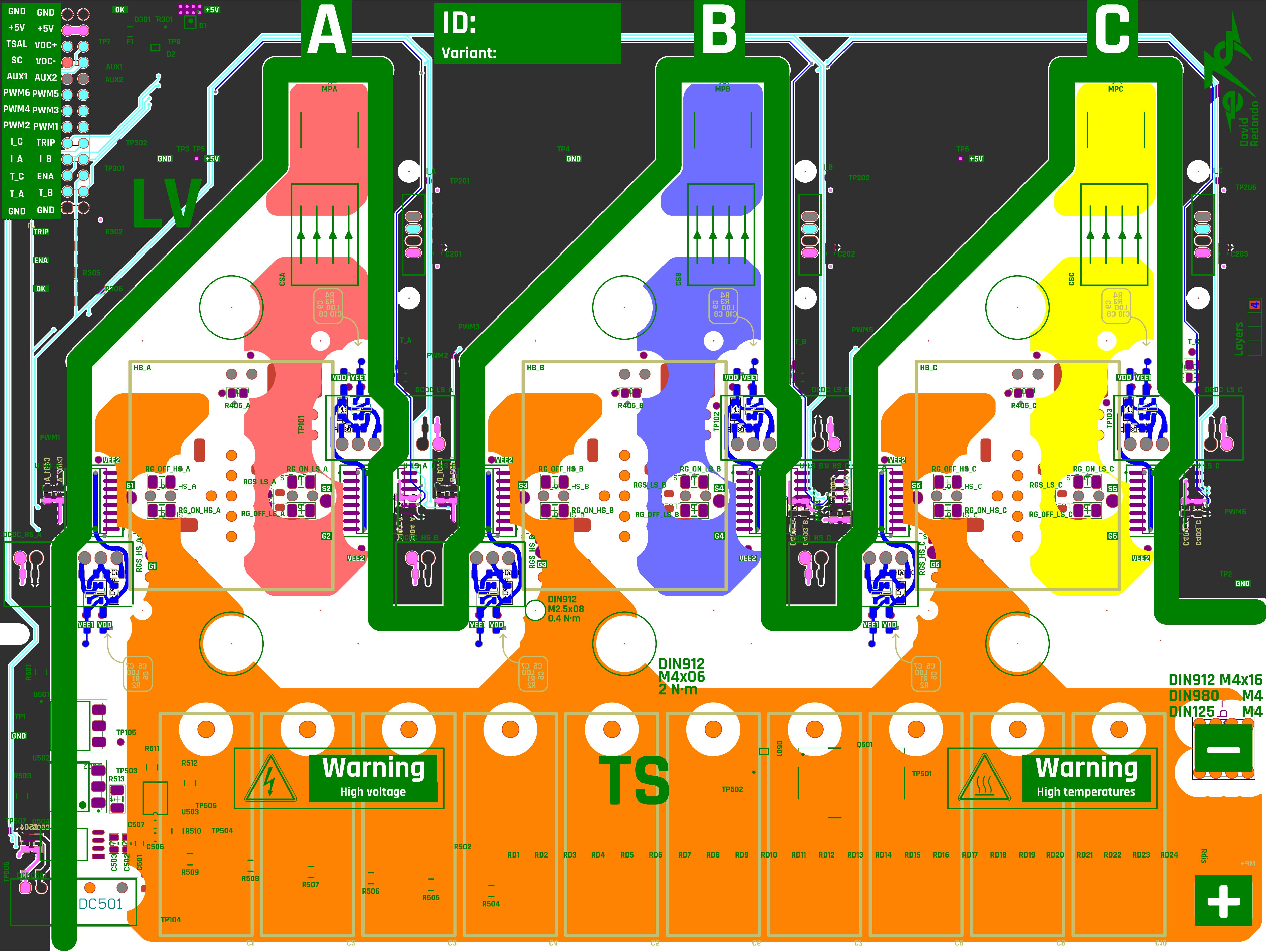
## DCDC501

|                    |  |                           |   |
|--------------------|--|---------------------------|---|
| <b>Company:</b>    | e-Tech Racing                            | e-techracing.es           |  |
| <b>Project:</b>    | Inverter Power                           | <b>Variant:</b> Wolfspeed |   |
| <b>Size:</b>       | <b>Page Contents:</b><br>- [5] DC.SchDoc | <b>Version:</b>           | 1.1   |
|                    |  | <b>Department:</b>        | Powertrain  |
| <b>Author:</b>     | David Redondo                            | dredondovinolo@gmail.com  | Sheet * of *  |
| <b>Checked by:</b> | -  | <b>Date:</b>              | 20/03/2024  |

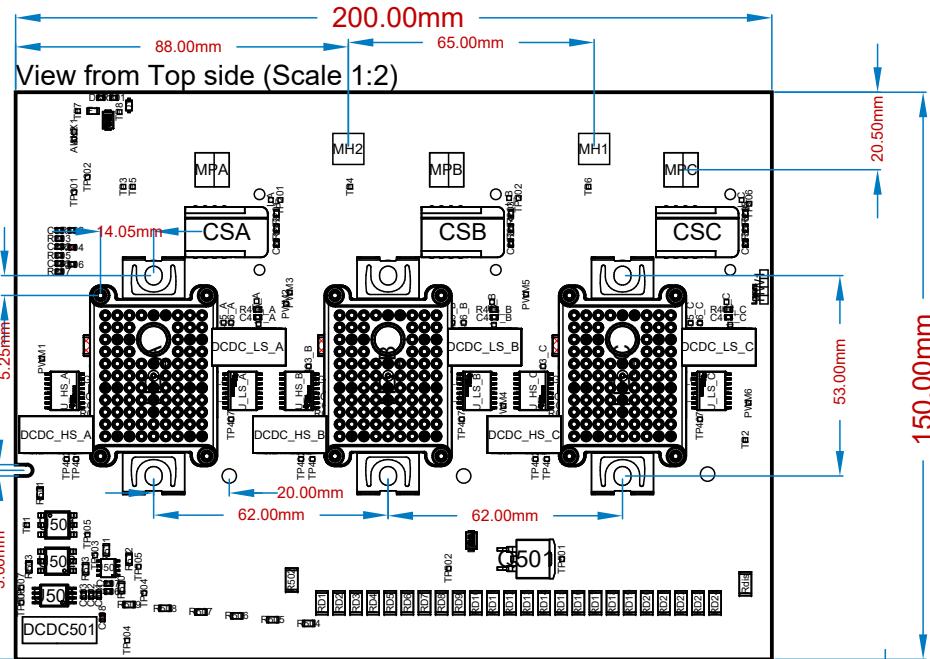




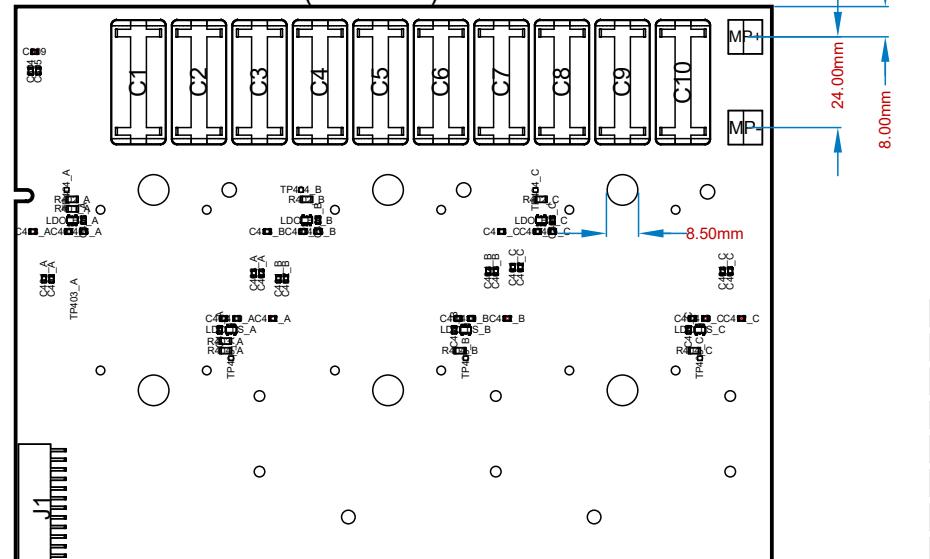




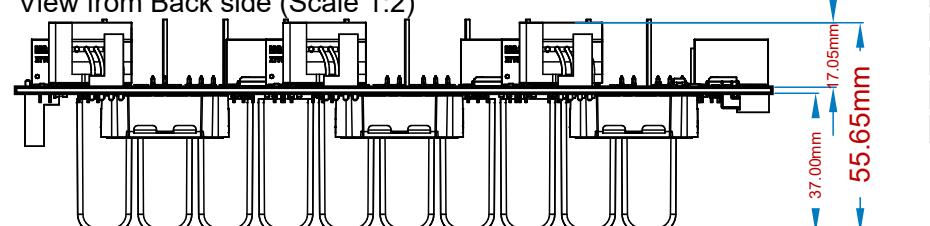
# Inverter Power



View from Top side (Scale 1:2)



View from Bottom side (Scale 1:2)



## Layer Stack Legend

| Material | Layer            | Thickness | Dielectric Material | Type          | Gerber |
|----------|------------------|-----------|---------------------|---------------|--------|
|          | Top Overlay      |           |                     |               | GTO    |
|          | Surface Material | 0.01mm    |                     | Solder Resist | GTS    |
| CF-004   | TOP              | 0.07mm    |                     | Signal        | GTL    |
|          | Prepreg          | 0.10mm    | PP-006              | Dielectric    |        |
|          | Prepreg          | 0.10mm    | PP-006              | Dielectric    |        |
| Copper   | GND              | 0.07mm    |                     | Signal        | G1     |
|          | FR-4             | 0.90mm    |                     | Dielectric    |        |
| Copper   | PWR              | 0.07mm    | PP-006              | Signal        | G2     |
|          | Prepreg          | 0.10mm    | PP-006              | Dielectric    |        |
|          | Prepreg          | 0.10mm    | PP-006              | Dielectric    |        |
| CF-004   | BOT              | 0.07mm    |                     | Signal        | GBL    |
|          | Surface Material | 0.01mm    |                     | Solder Resist | GBS    |
|          | Bottom Overlay   |           |                     | Legend        | GBO    |

Total thickness: 1.60mm

## Bill Of Materials

| Designator   | Name               | Quantity |
|--|--------------------|----------|
| C405_A, C405_B, C405_C, C406_A, C406_B, C406_C, C408_A, C408_B, C408_C, C409_A, C409_B, C409_C   | 10uF               | 12       |
| C1, C2, C3, C4, C5, C6, C7, C8, C9, C10  | 10uF 850V          | 10       |
| F1   | 0437001.WRA        | 1        |
| DCDC501  | 1779205141         | 1        |
| J1   | 613026243121       | 1        |
| D2   | BZG05C5V1-E3-TR    | 1        |
| HB_A, HB_B, HB_C   | CAB016M12FM3       | 3        |
| R402_A, R402_B, R402_C, R404_A, R404_B, R404_C   | CR1206-JV-303ELF   | 6        |
| R401_A, R401_B, R401_C, R403_A, R403_B, R403_C   | CR1206-JV-683ELF   | 6        |
| R503   | CROW120610K0FKEA   | 1        |
| R511   | CROW120630K0FKEA   | 1        |
| HW1  | LOGO CAPAS (4)     | 1        |
| MP-, MP+, MPA, MPB, MPC  | M4                 | 5        |
| DCDC_HS_A, DCDC_HS_B, DCDC_HS_C, DCDC_LS_A, DCDC_LS_B, DCDC_LS_C   | MBR0530            | 1        |
| MH1, MH2   | MGJ6-series        | 6        |
| RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24                | Mounting Hole M4   | 24       |
| R406_A, R406_B, R406_C   | RCV2512470KFKEG    | 24       |
| R301   | CR0805-FX-1000ELF  | 3        |
| R302, R305, R306, R405_A, R405_B, R405_C, RGS_HS_A, RGS_HS_B, RGS_HS_C, RGS_LS_A, RGS_LS_B, RGS_LS_C   | CR0805-JV-102ELF   | 1        |
| R504, R505, R506, R507, R508, R509   | CR0805-JV-103ELF   | 12       |
| R501, R513   | CR1206-FX-6802EAS  | 6        |
| R510, R512   | CR1206-FX-2201ELF  | 2        |
| CSA, CSB, CSC  | CRS1206-FX-4701ELF | 2        |
| U503   | LEM CCSR 50-NP     | 3        |
| C501   | LM311DR2G          | 1        |
| RG_OFF_HS_A, RG_OFF_HS_B, RG_OFF_HS_C, RG_OFF_LS_A, RG_OFF_LS_B, RG_OFF_LS_C, RG_ON_HS_A, RG_ON_HS_B, RG_ON_HS_C, RG_ON_LS_A, RG_ON_LS_B, RG_ON_LS_C | 885012208058       | 1        |
| U504   | CRG1206F100R       | 12       |
| LDO_HS_A, LDO_HS_B, LDO_HS_C, LDO_LS_A, LDO_LS_B, LDO_LS_C   | ISO224             | 1        |
| U_HS_A, U_HS_B, U_HS_C, U_LS_A, U_LS_B, U_LS_C   | TPS72301           | 6        |
| Q501   | UCC21710           | 6        |
| R502, Rds  | SIH150N60E-GE3     | 1        |
| U501, U502   | R2M-2512FTK        | 2        |
| D501   | 4N35               | 2        |
| D301   | BZG05C6V2-E3-TR    | 1        |
| C201, C202, C203, C402_A, C402_B, C402_C, C404_A, C404_B, C404_C, C411_A, C411_B, C411_C, C502, C504, C506   | 150080GS75000      | 1        |
| C401_A, C401_B, C401_C, C403_A, C403_B, C403_C, C503, C505, C507   | 885012207098       | 15       |
|  | 885012207103       | 9        |

Copper thickness in hole 25-50um, watch out for 1.10mm holes  
Chemical tin 1-15um