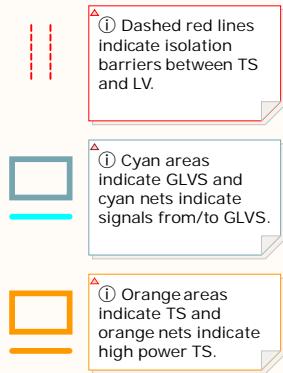


A



Specifications:

V_{in}, max = 600 VDC
V_{out}, max = 245 VRMS (SVPWM)
f_{sw} = 50 kHz
P_{out}, max = 40kW
I_{out}, max = 80 ARMS

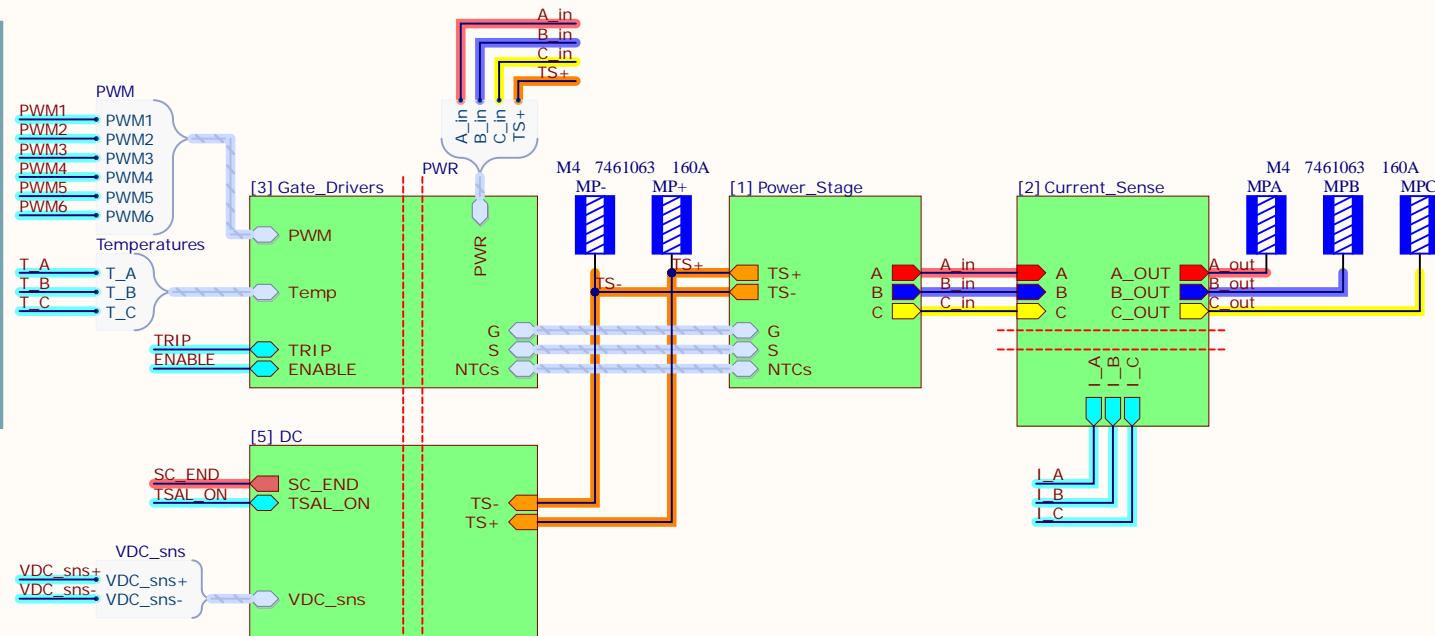
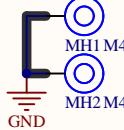
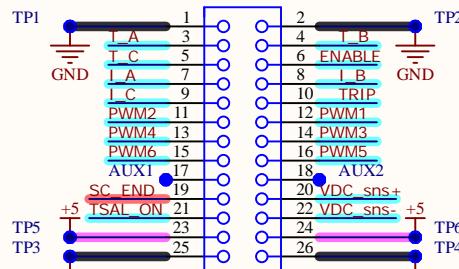
Liquid cooled with water at 50°C max

NOTES
Sent to production on 15-02-2024.
Changes on SCH since production:
- [MP+] and [MP-] swapped.
Changes on PCB since production:

PENDING ERRORS:

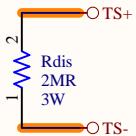
- Silkscreen and positioning of [MP+] and [MP-] in PCB
- [LDO_HS], [LDO_LS] pins 4-5 swap in symbol and footprint.

LV Connector

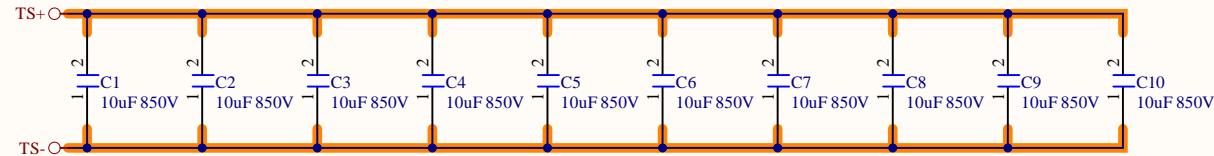


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|-------------|---|--------------------------|--------------|
| Company: | e-Tech Racing | e-techracing.es | |
| Project: | Inverter Power | Variant: Wolfspeed | |
| Size: | Page Contents: Inverter_Power.SchDoc | Version: 1.0 | |
| | | Department: Powertrain | |
| Author: | David Redondo | dredondovinolo@gmail.com | Sheet 1 of 5 |
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Passive discharge



DC Bus capacitors, 100uF, Murata FHA85Y106KS



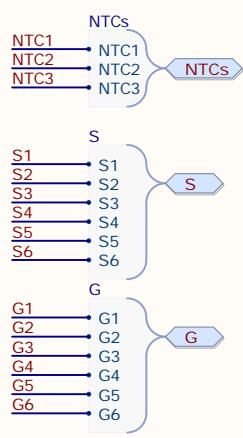
△ DC Link design considerations:

$V_C > 1.1 \cdot V_{max} = 1.1 \cdot 600 V = 660 V \rightarrow 850 V$

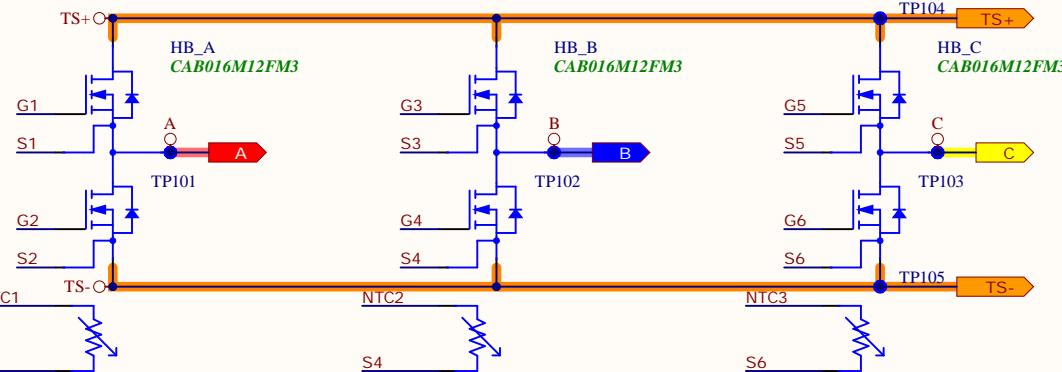
$I_{C,RMS} \approx 0.65 \cdot I_{phase,RMS} = 0.65 \cdot 80 A, RMS = 52 A, RMS \rightarrow 10 \times 5 A, RMS (\Delta T = 10 ^\circ C)$
 $C > I_{C,RMS} / (V_{ripple} \cdot f_{sw}) = 52 A, RMS / (15V \cdot 50 kHz) \approx 79 \mu F \rightarrow 10 \times 10 \mu F$

Lowering the switching frequency will proportionally lower the current rating for the same voltage ripple or proportionally increase the voltage ripple for the same output current. Check:
<https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter>

INPUTS/OUTPUTS



SiC Half-Bridges



△ Semiconductor details:

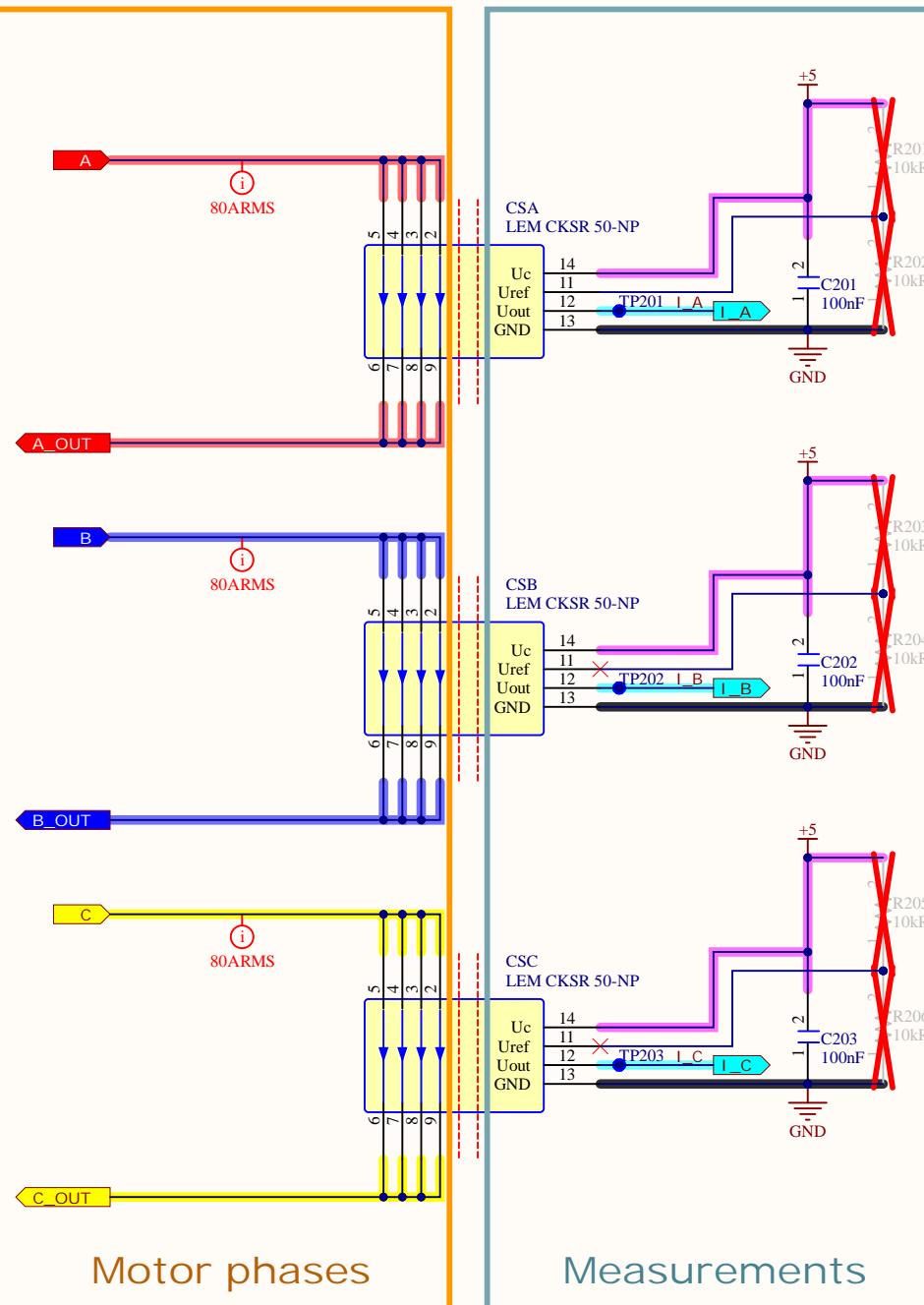
$V_{DSS}(\text{breakdown}) = 1200 V // 1200 V$
 $R_{on} = 5.5 .. 13 m\Omega // 16.0 .. 28.8 m\Omega$
 $V_{f,D} = 3.3 .. 4 V // 4.9 .. 5.5 V$
 $T_{rr} = 41.5 .. 45 ns // 20.0 ns$
 $Q_{rr} = 2.19 .. 3.94 \mu C // 1.30 \mu C$
 $R_{th,Jc} = 0.12 .. 0.15 K/W // 0.543 K/W$
 $Q_G = 520 nC // 236 nC$
 $C_{in} = 14.5 nF // 6.6 nF$
 $R_G(\text{int}) = 1.9 \Omega // 2.4 \Omega$
 $V_{GS(th)} = 2.8 .. 4.8 V // 1.8 .. 3.6 V$

| | | | |
|-------------|--|--------------------------|--------------|
| Company: | e-Tech Racing | e-techracing.es | |
| Project: | Inverter Power | Variant: Wolfspeed | |
| Size: | Page Contents: [1]Power_Stages.SchDoc | Version: 1.0 | |
| - | | Department: Powertrain | |
| Author: | David Redondo | dredondovinolo@gmail.com | Sheet 2 of 5 |
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A

CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R_phase-connector = 0.18 mΩ)



B

CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values. Voltage divider implemented just in case.

I_A , I_B , I_C

$$U_{\text{meas}} = (12.5 \text{mV/A} \cdot I_{\text{meas}} + U_{\text{ref}})$$

For $\pm 150 \text{Apk}$:
 $V_{\text{meas_pk+}} = 4.375 \text{V}$
 $V_{\text{meas_pk-}} = 0.625 \text{V}$

C201 , C202 , C203

The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

C

CSA , CSB , CSC

AC insulation test
RMS voltage, 50 Hz,
1 min:

$$U_d = 4.3 \text{kV} > 3 \cdot V_{\text{max}} = 1.8 \text{kV}$$

D

| | | | |
|-------------|---|--------------------------|--------------|
| Company: | e-Tech Racing | e-techracing.es | |
| Project: | Inverter Power | Variant: | Wolfspeed |
| Size: | Page Contents: [2]Current_Sense.SchDoc | Version: | 1.0 |
| - | | Department: | Powertrain |
| Author: | David Redondo | dredondovinolo@gmail.com | Sheet 3 of 5 |
| Checked by: | _ | Date: | 01/03/2024 |

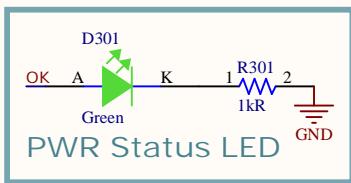
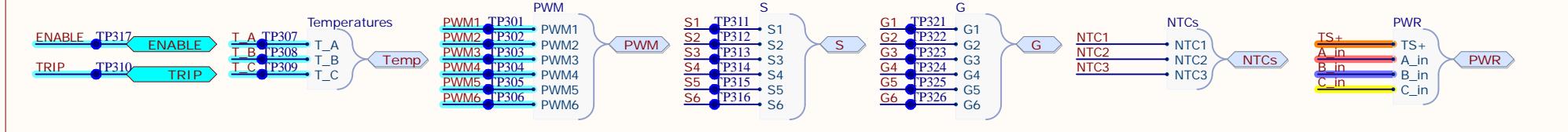
1

2

3

4

INPUTS/OUTPUTS



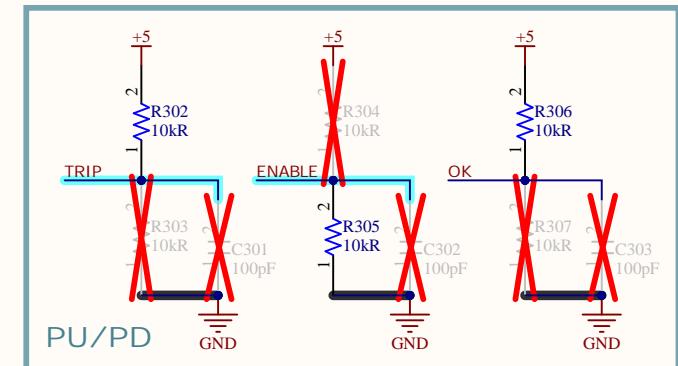
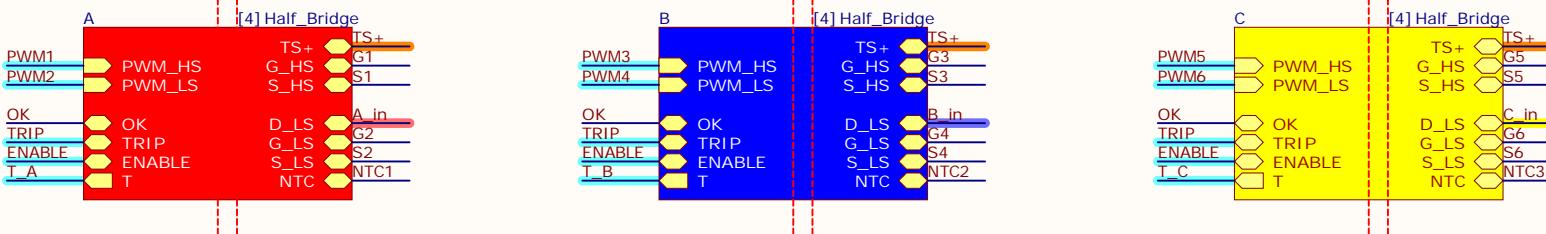
[T_A, T_B, T_C]
Look-up table obtained with MATLAB script which can be found in the simulations folder.
For different temperatures:
 $V_{meas}(0^\circ\text{C}) = 0.246\text{V}$
 $V_{meas}(25^\circ\text{C}) = 2\text{V}$
 $V_{meas}(50^\circ\text{C}) = 2.578\text{V}$
 $V_{meas}(90^\circ\text{C}) = 2.864\text{V}$

B

B

C

C



| | | | |
|-------------|--|--------------------------|------------------|
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| Project: | Inverter Power | Variant: | Wolfspeed |
| Size: | Page Contents: [3]Gate_Drivers.SchDoc | Version: | 1.0 |
| - | | Department: | Powertrain |
| Author: | David Redondo | dredondovinolo@gmail.com | Sheet 4 of 5 |
| Checked by: | | | Date: 01/03/2024 |

1

2

3

4

A

U_HS, U_LS

- TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
- IN- is not used and tied to **GND**.
- ENABLE** to be given by MCU in active-high mode. When set to low for more than 1 μ s, **TRIP** is reset.
- Temperature sensing using low-side drivers. Ain outputs a current of 200 μ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **R405**, **R406** and **C411** from SPICE simulation.
- Miller clamp protection is used.
- RGS_HS**, **RGS_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
- Overcurrent detection is not implemented.

LDO_HS, LDO_LS

An LDO is implemented to trim **VEE_HS_A** and **VEE_LS_A** during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

$$\text{VEE} = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers $\rightarrow R1 = 36 \text{ k}\Omega$, $R2 = 56 \text{ k}\Omega$

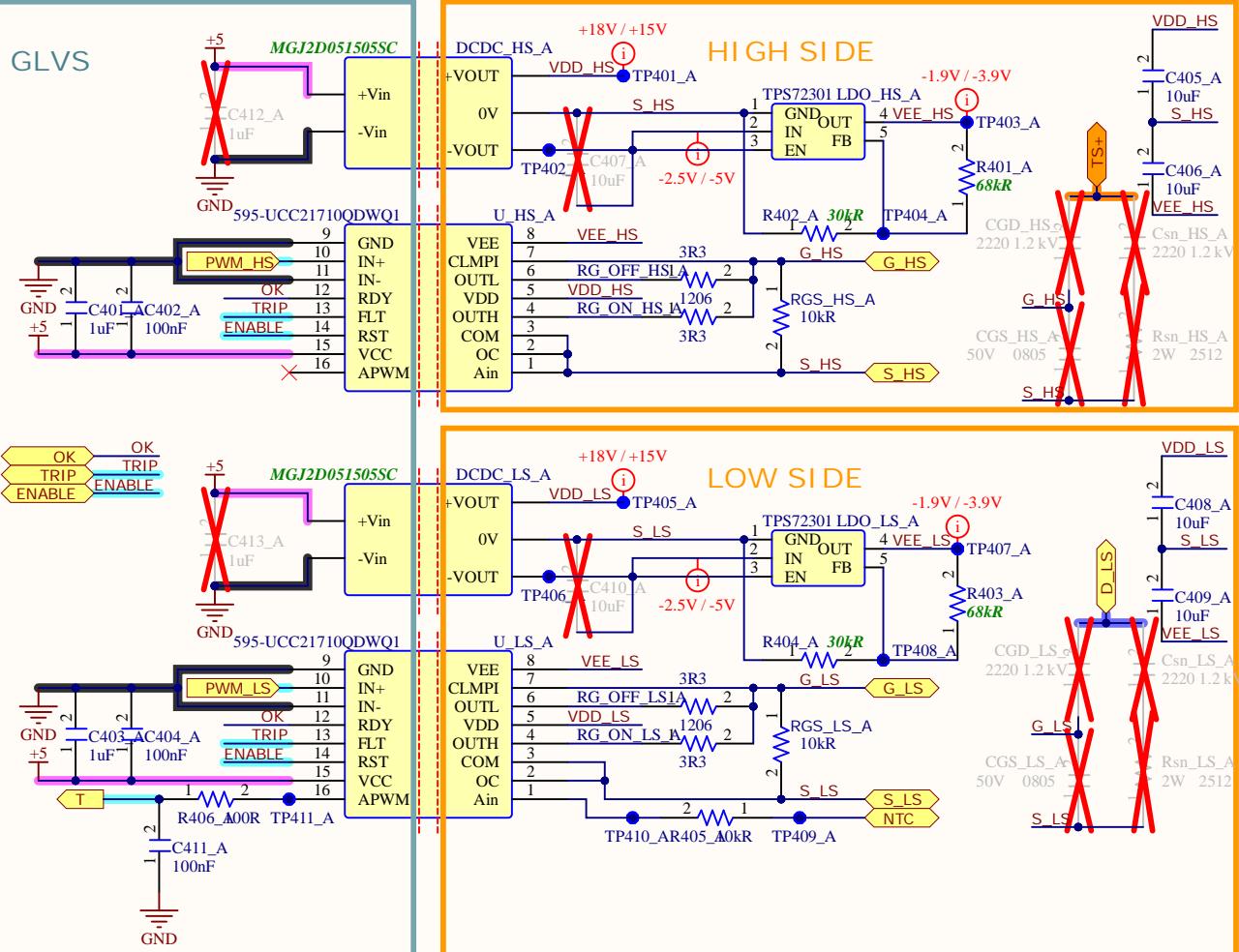
Wolfspeed $\rightarrow R1 = 68 \text{ k}\Omega$, $R2 = 30 \text{ k}\Omega$

DCDC_HS, DCDC_LS

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS

VIOTM ($t = 60$ s (qualification test)): 8000 VPK

GLVS**V_GS values:**

The values can be modified by replacing **DCDC_HS** and **DCDC_LS** with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

Minimum gate driver current and power:
 $I_{GD(\min)} = f_{sw} \cdot O_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$
 $P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS, **CGS_LS**, **CGD_HS**, **CGD_LS**, **Csn_HS**, **Csn_LS**, **Rsn_HS**, **Rsn_LS**

DNP, but they could be useful with EMI related issues to decrease dV/dt . Implementing them could avoid issues with the power limit for **DCDC_HS** and **DCDC_LS**, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

Company: e-Tech Racing e-techracing.es



Project: Inverter Power Variant: Wolfspeed

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|-------------|---|------------------------|
| Size: | Page Contents: [4]Half_Bridge.SchDoc | Version: 1.0 |
| | | Department: Powertrain |
| Author: | dredondovinolo@gmail.com | Sheet 5 of 5 |
| Checked by: | | Date: 01/03/2024 |

A

U_HS, U_LS

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- IN- is not used and tied to GND.
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- Temperature sensing using low-side drivers. Ain outputs a current of 200 μ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. [R405], [R406] and [C411] from SPICE simulation.
- Miller clamp protection is used.
- RGS_HS, RGS_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
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LDO_HS, LDO_LS

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$$\text{VEE} = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers $\rightarrow R1 = 36 \text{ k}\Omega$, $R2 = 56 \text{ k}\Omega$

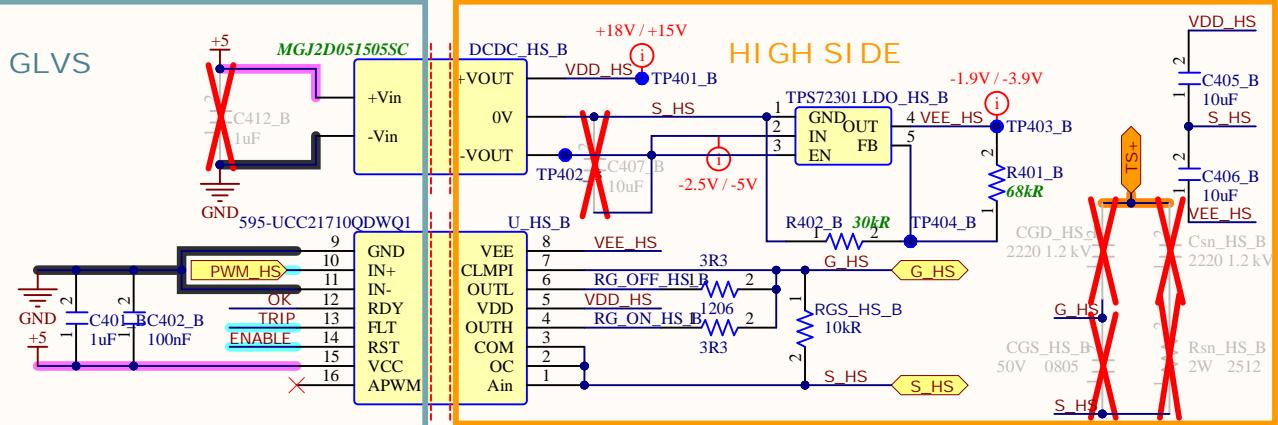
Wolfspeed $\rightarrow R1 = 68 \text{ k}\Omega$, $R2 = 30 \text{ k}\Omega$

DCDC_HS, DCDC_LS

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

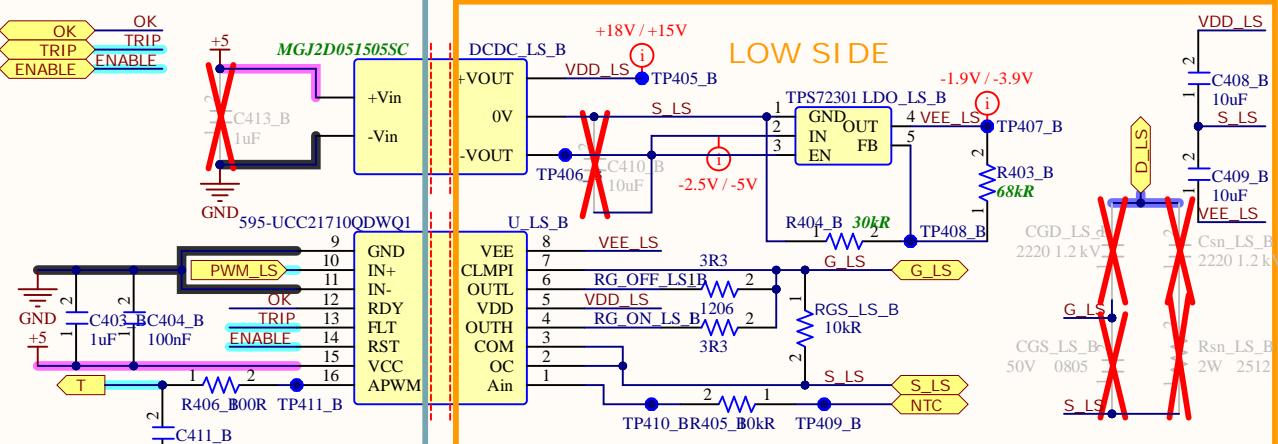
U_HS, U_LS

VIOTM ($t = 60$ s (qualification test)): 8000 VPK

GLVS**V_GS values:**

The values can be modified by replacing DCDC_HS and DCDC_LS with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

Minimum gate driver current and power:
 $I_{GD(\min)} = f_{sw} \cdot O_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$
 $P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

OK, TRIP, ENABLE**RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS, CGS_LS, CGD_HS, CGD_LS, Csn_HS, Csn_LS, Rsn_HS, Rsn_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could result in issues with the power limit for DCDC_HS and DCDC_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

Company: e-Tech Racing e-techracing.es



Project: Inverter Power

Variant: Wolfspeed

Size: - Page Contents: [4]Half_Bridge.SchDoc Version: 1.0

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Checked by: _ Date: 01/03/2024

U_HS, **U_LS**

- TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
 - IN- is not used and tied to **GND**.
 - ENABLE** to be given by MCU in active-high mode. When set to low for more than 1 μ s, **TRIP** is reset.
 - Temperature sensing using low-side drivers. Ain outputs a current of 200 μ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **R405**, **R406** and **C411** from SPICE simulation.
 - Miller clamp protection is used.
 - RGS_HS**, **RGS_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
 - Overscurrent detection is not implemented.

LDO HS LDO LS

An LDO is implemented to trim `VEE_HS_A` and `VEE_LS_A` during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

$$VEE = -1.186 \cdot (1 + R1/R2)$$

$$R_1 + R_2 \approx 100 \text{ k}\Omega$$

Leapers $\rightarrow R_1 = 36 \text{ k}\Omega$, $R_2 = 56 \text{ k}\Omega$

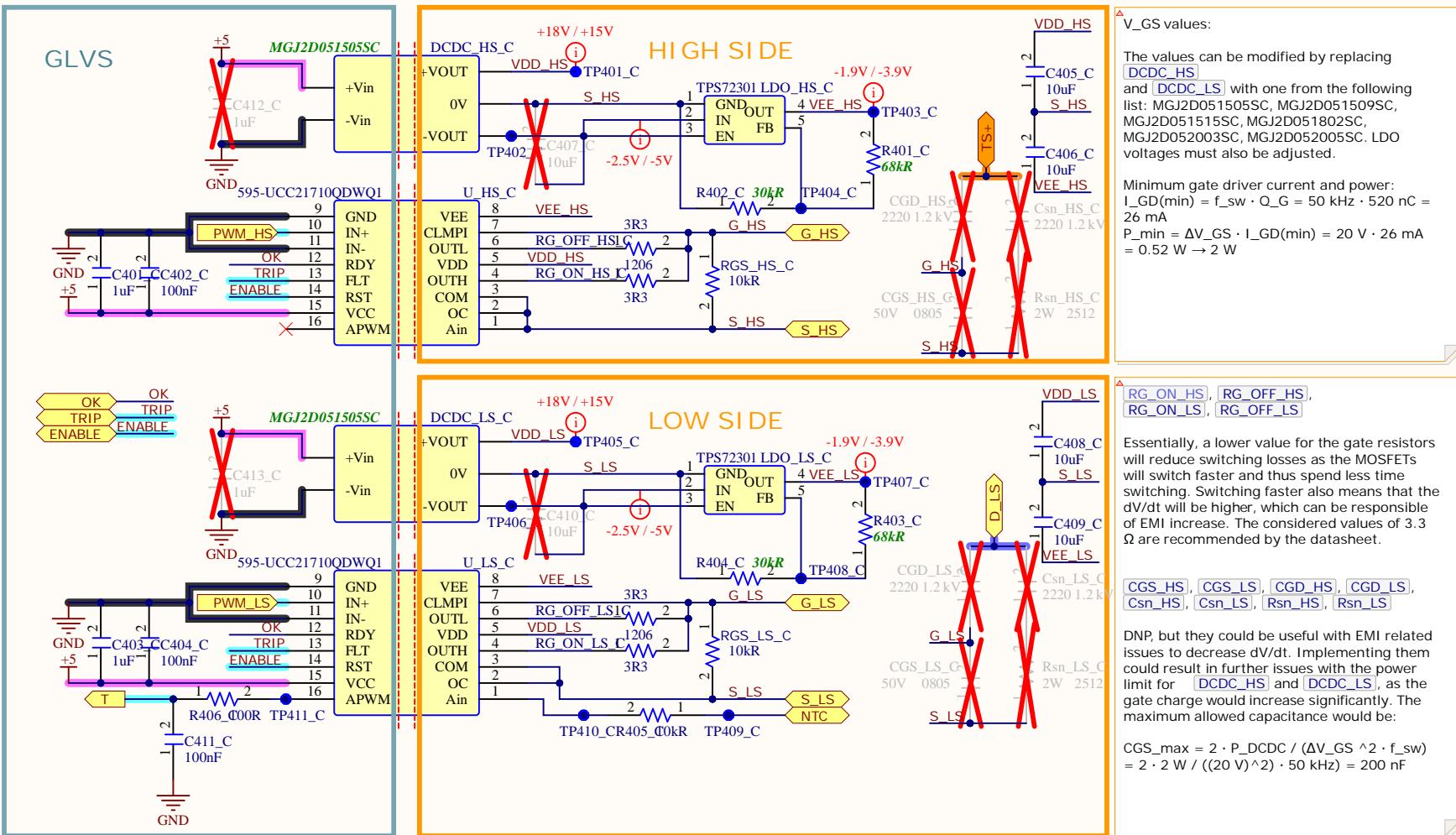
Wolfspeed → R1 = 68 kΩ, R2 = 30 kΩ

△

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS

VIOTM ($t = 60$ s (qualification test))
8000 VPK



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| Project: | InverterPower | Variant: Wolfspeed | |
| Size: - | Page Contents: [4] Half_Bridge.SchDoc | Version: 1.0 | |
| Author: | David Redondo | dredondovinolo@gmail.com | Department: Powertrain |
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A

Discharge resistors:

$$t_{dis} = R_{dis} \cdot C \cdot \ln(V_{initial}/V_{final}) = (470 \text{ k}\Omega / 24) \cdot (100 \mu\text{F}) \cdot \ln(600 \text{ V} / 60 \text{ V}) = 4.509 \text{ s}$$

$$P(R_{dis}, \text{max}) = V_{max}^2 / R_{dis} = 600 \text{ V}^2 / 470 \text{ k}\Omega = 0.766 \text{ W} < 1 \text{ W}$$

$$I_{dis, \text{max}} = 600 \text{ V} / (470 \text{ k}\Omega / 24) = 30.64 \text{ mA}$$

U503

Single supply configuration as per datasheet.

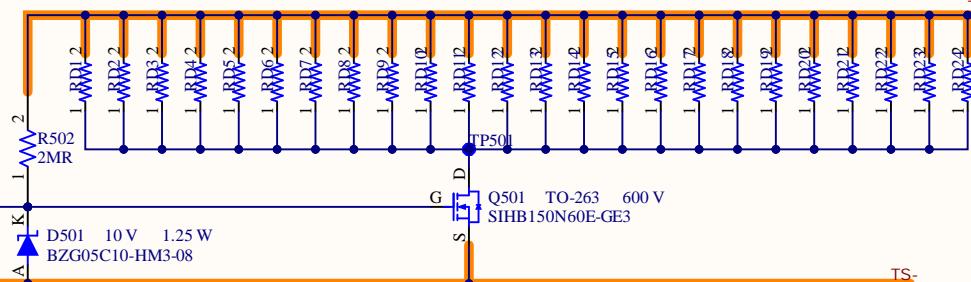
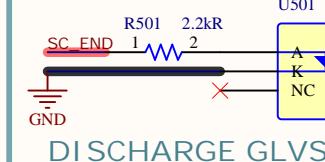
$$\text{Maximum differential input voltage} = 6.833 \text{ V} - 677 \text{ mV} = 6.156 \text{ V} < 30 \text{ V}$$

R501
For U501, the recommended diode forward current is 10 mA. SC-END can be between 20 V and 30 V.

U501
Maximum current across phototransistor
 $I_t(\text{max}) = 600 \text{ V} / 2 \text{ M}\Omega = 0.3 \text{ mA} < 150 \text{ mA}$
 $V_{ce(\text{max})} = 10 \text{ V} < 70 \text{ V}$

$$I_{min} = 20 \text{ V} / 2.2 \text{ k}\Omega = 9.1 \text{ mA}$$

$$I_{max} = 30 \text{ V} / 2.2 \text{ k}\Omega = 13.6 \text{ mA}$$



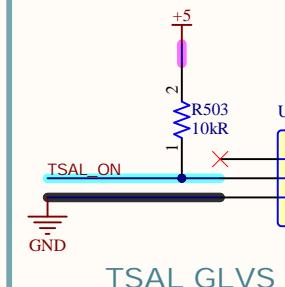
$$VDC_div = (TS+ - TS-) \cdot 4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega)$$

$$600 \text{ V} \cdot 4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega) = 6.833 \text{ V}$$

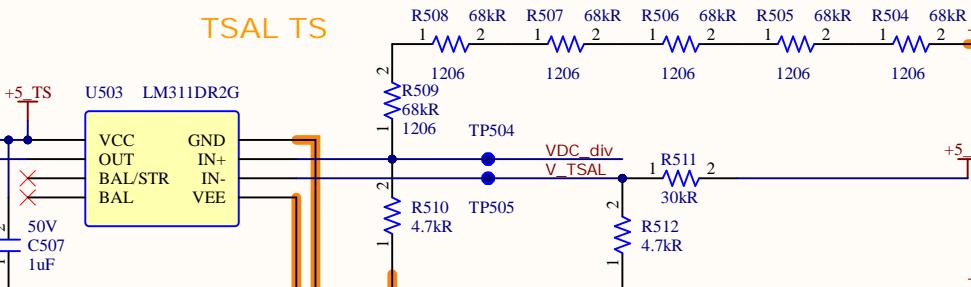
$$60 \text{ V} \cdot 4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega) = 683 \text{ mV}$$

$$P_{R4} = I_{R4}^2 \cdot R_4 = ((600 \text{ V} / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega)) / 68 \text{ k}\Omega)^2 \cdot 68 \text{ k}\Omega = 144 \text{ mW} \rightarrow 1206 \text{ package}$$

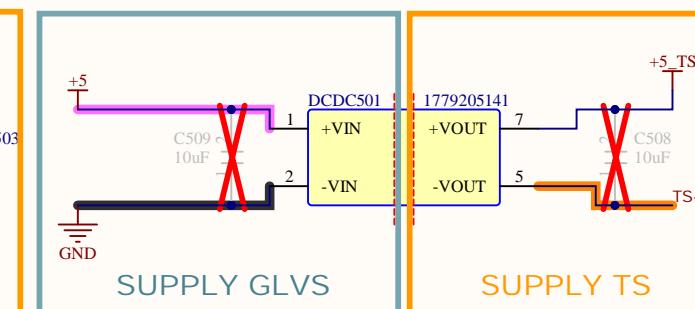
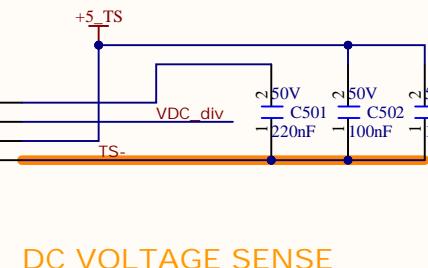
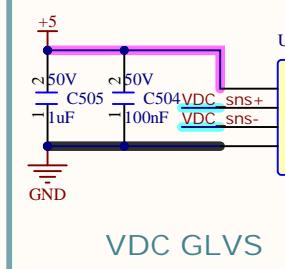
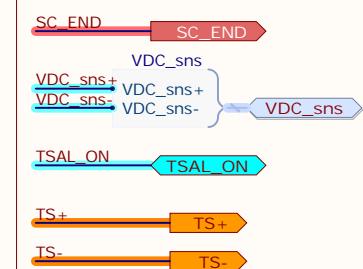
$$V_{TSAL} = 5 \text{ V} \cdot 4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 30 \text{ k}\Omega) = 677 \text{ mV} \equiv 59.46 \text{ V in } TS+ - TS-$$



TSAL TS



INPUTS/OUTPUTS



$$(TS+ - TS-) > 60 \text{ V} \rightarrow TSAL_ON = 0 \text{ V}$$

$$(TS+ - TS-) < 60 \text{ V} \rightarrow TSAL_ON = 5 \text{ V}$$

$$U504 \quad (\text{VDC}_sns+ - \text{VDC}_sns-) = 1/3 \cdot (\text{VDC}_div) = 1/3 \cdot ((TS+ - TS-))$$

$$4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega) = 1/3 \cdot 0.011388 \cdot (TS+ - TS-)$$

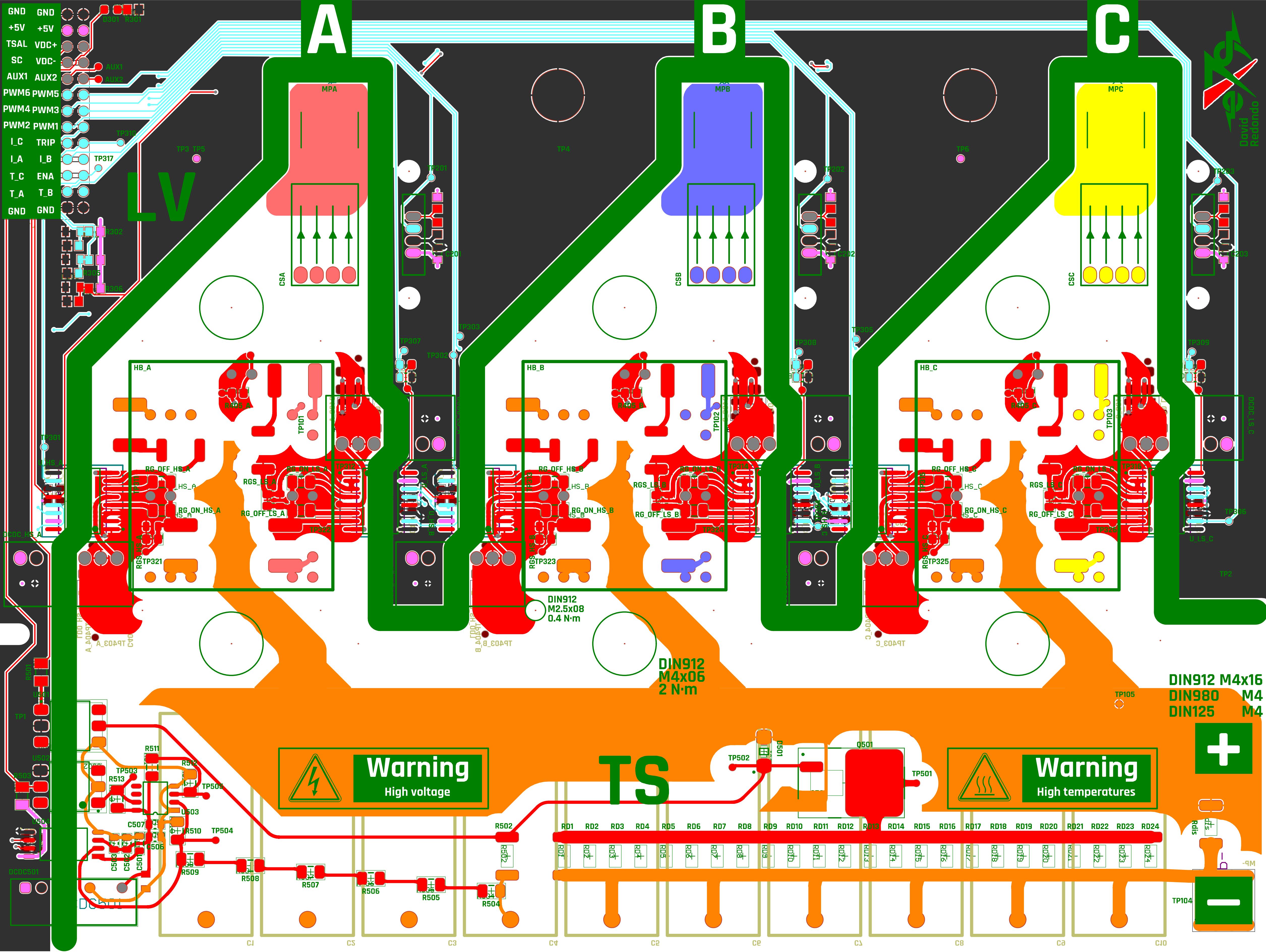
$$(\text{VDC}_sns+ - \text{VDC}_sns-) = 1/3 \cdot 0.011388 \cdot 600 \text{ V} = 2.278 \text{ V}$$

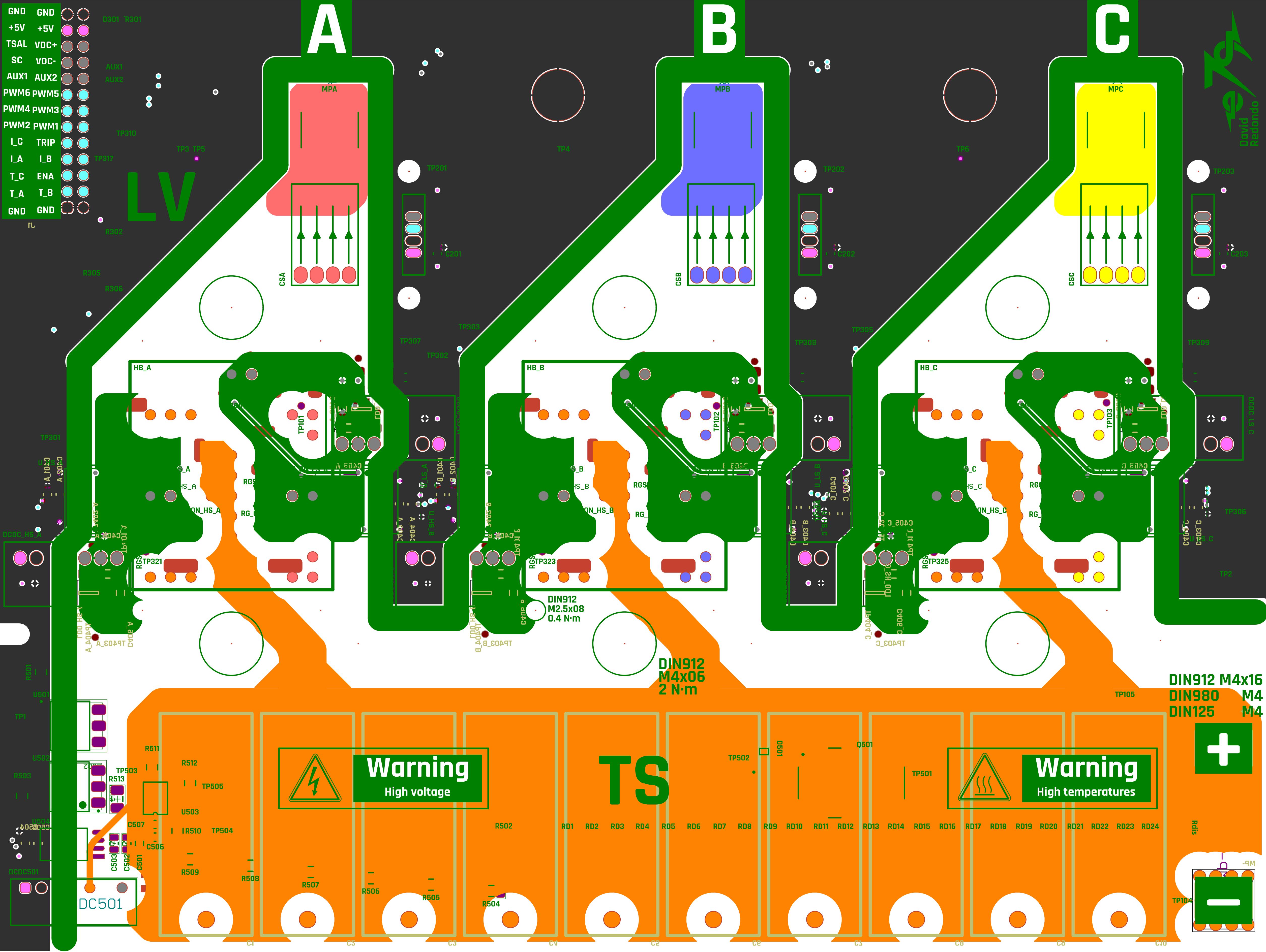
U504
 $(\text{VDC}_sns+ - \text{VDC}_sns-) = 1/3 \cdot ((TS+ - TS-))$
 $4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega) = 1/3 \cdot 0.011388 \cdot (TS+ - TS-)$

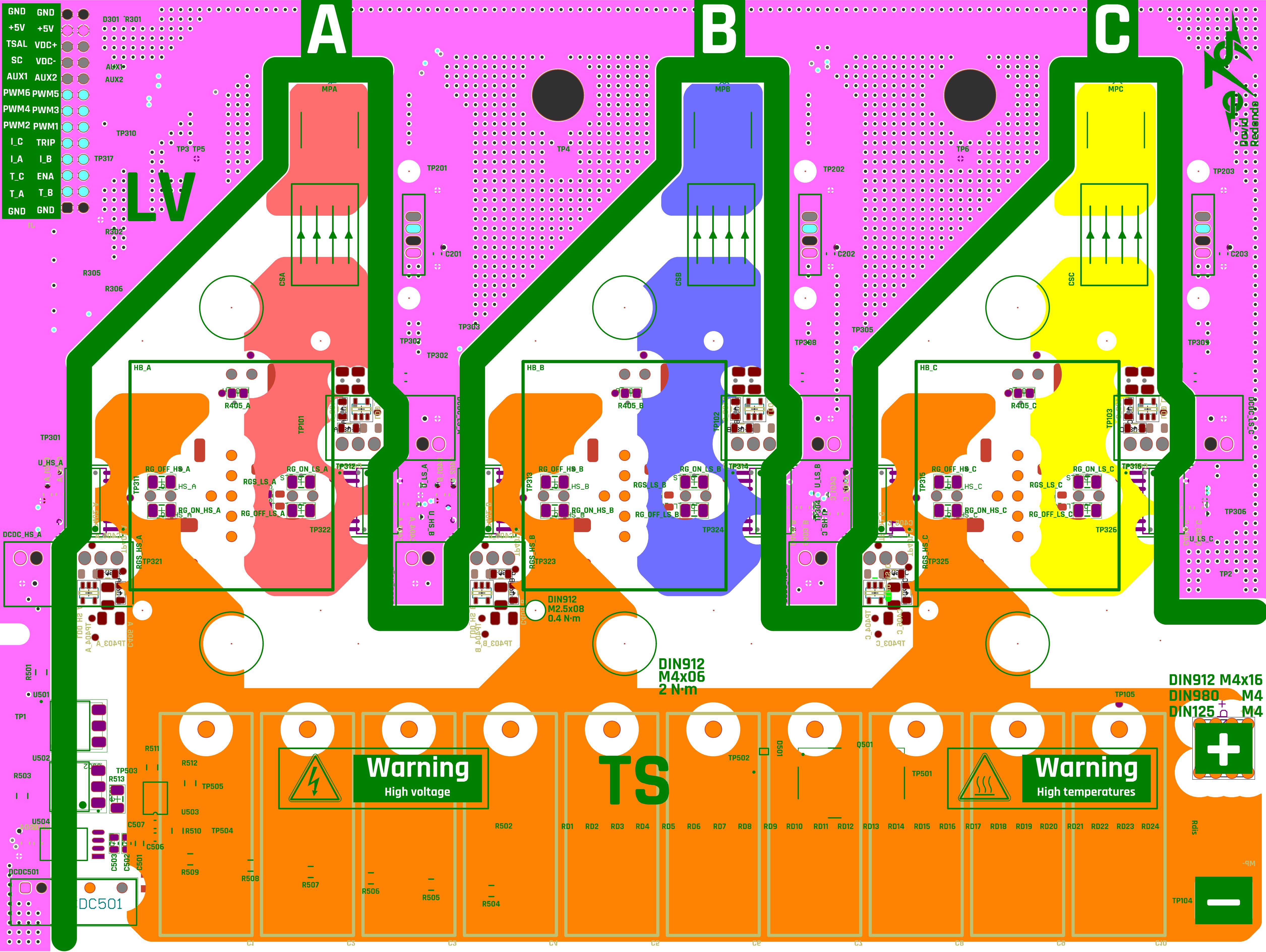
U501, U502
Isolation Voltage: AC For 1 Minute, R.H. = 40 ~ 60% Viso = 5000 Vrms

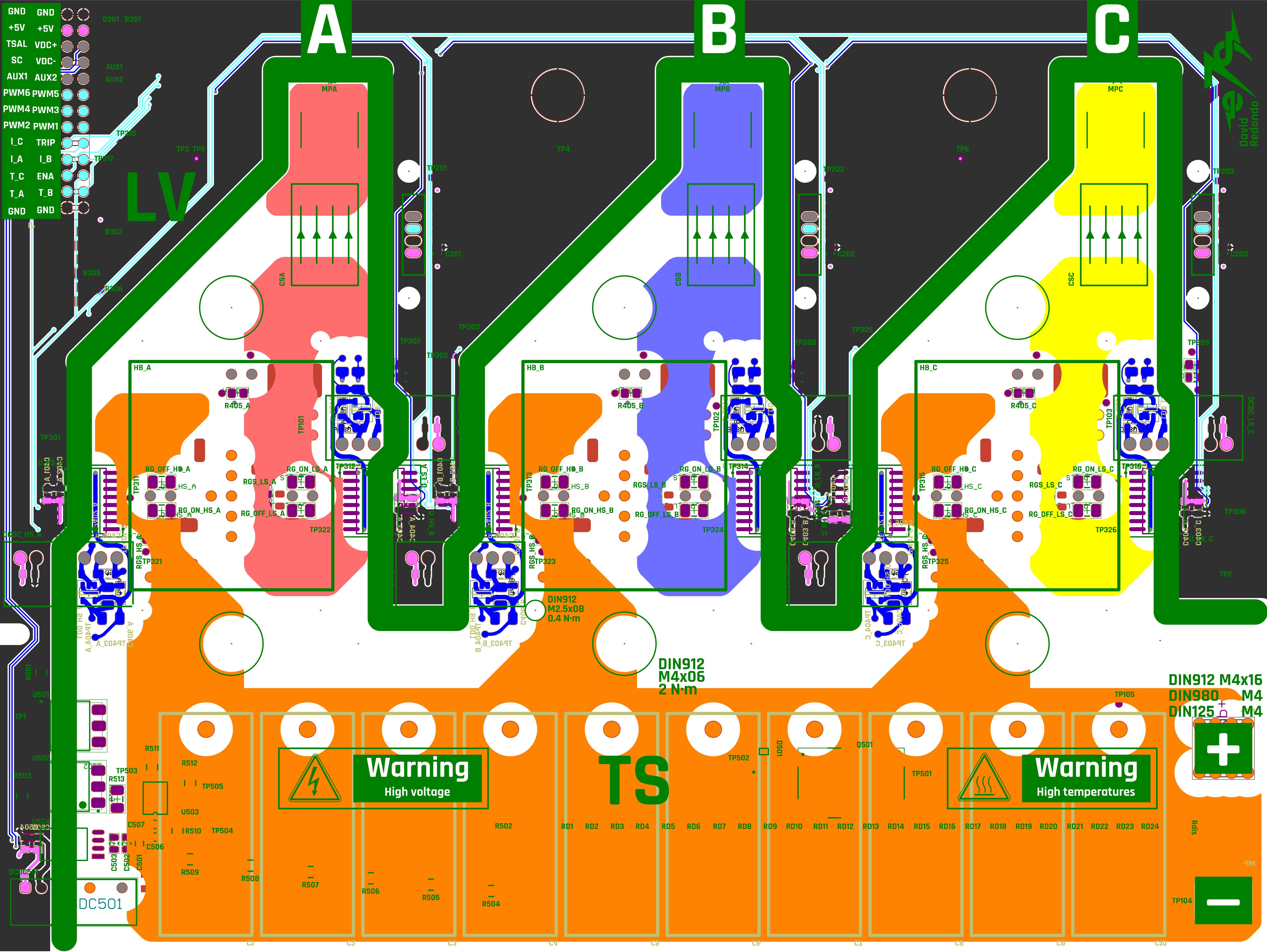
DCDC501
Maximum transient isolation voltage: VTEST = VIOTM, t = 60 s (qualification test) VIOTM = 7071 Vpk

| | | | |
|-------------|--------------------------------|--------------------------|--|
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| Project: | Inverter Power | Variant: Wolfspeed | |
| Size: | Page Contents: [5]DC.SchDoc | Version: 1.0 | |
| Department: | Powertrain | | |
| Author: | David Redondo | dredondovinolo@gmail.com | Sheet <input type="text"/> of <input type="text"/> |
| Checked by: | <input type="text"/> | Date: 01/03/2024 | |

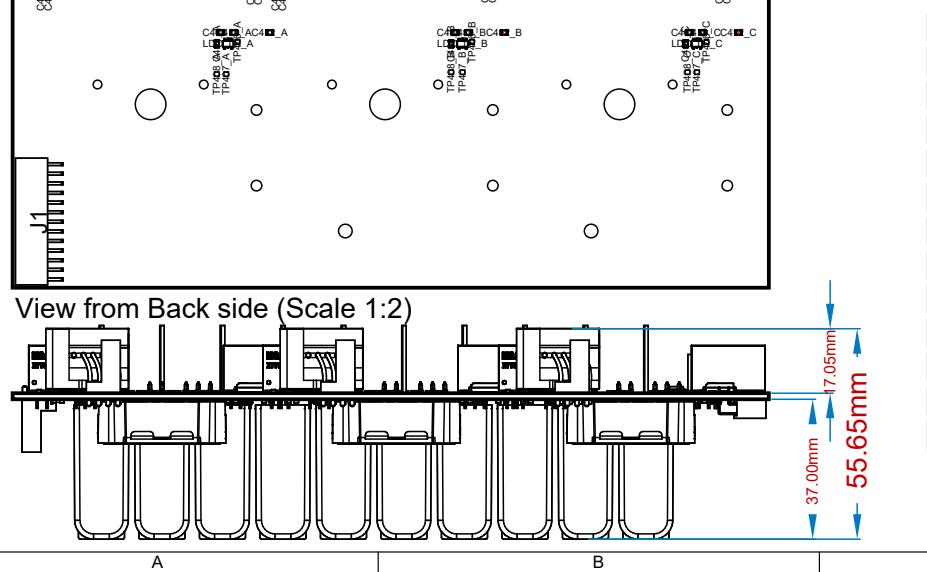
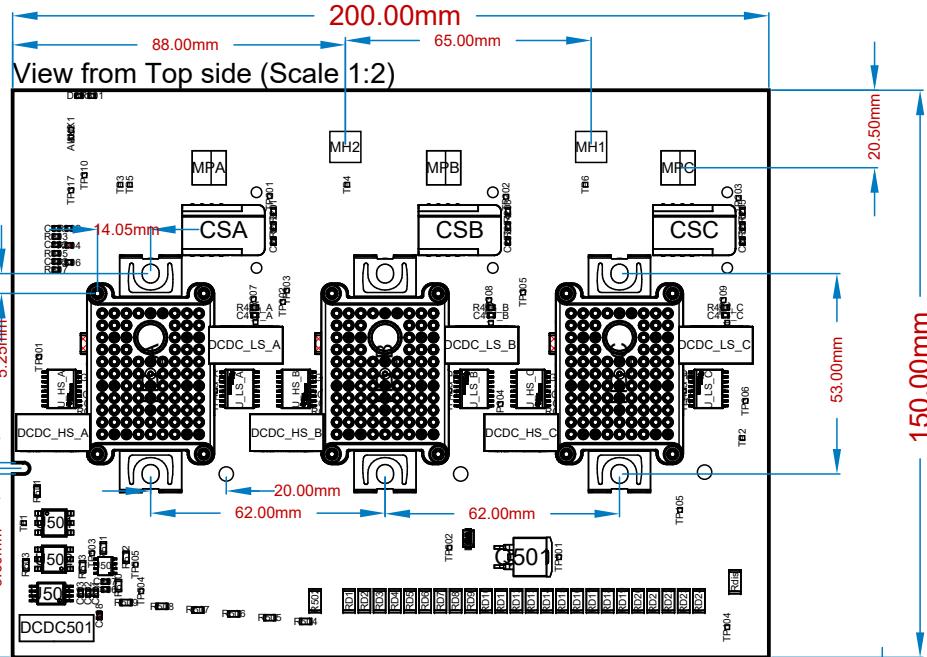








Inverter Power



Bill Of Materials

| Designator | Name | Quantity |
|---|-------------------|----------|
| C405_A, C405_B, C405_C, C406_A, C406_B, C406_C, C408_A, C408_B, C408_C | 10uF | 12 |
| C1, C2, C3, C4, C5, C6, C7, C8, C9, C10 | 10uF 850V | 10 |
| DCDC501 | 1779205141 | 1 |
| J1 | 613026243121 | 1 |
| HB_A, HB_B, HB_C | CAB016M12FM3 | 3 |
| R402_A, R402_B, R402_C, R403_A, R403_B, R403_C | CR0805-JW-303ELF | 6 |
| R503 | CR0805-JW-683ELF | 1 |
| R511 | CRCW120610K0FKEA | 1 |
| MP+, MP+, MPA, MPB, MPC | M4 | 5 |
| DCDC_HS_A, DCDC_HS_B, DCDC_HS_C, DCDC_LS_A, DCDC_LS_B, DCDC_LS_C | MGJ6-series | 6 |
| MH1, MH2 | Mounting Hole M4 | 2 |
| RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24 | RCV2512470KFKEG | 24 |
| R406_A, R406_B, R406_C | CR0805-FX-1000ELF | 3</ |