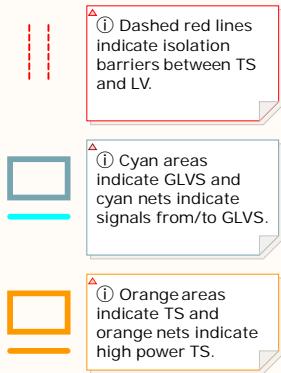


A



**Specifications:**

V<sub>in</sub>, max = 600 VDC  
V<sub>out</sub>, max = 245 VRMS (SVPWM)  
f<sub>sw</sub> = 50 kHz  
P<sub>out</sub>, max = 40kW  
I<sub>out</sub>, max = 80 ARMS

Liquid cooled with water at 50°C max

**NOTES**

Sent to production on 15-02-2024.

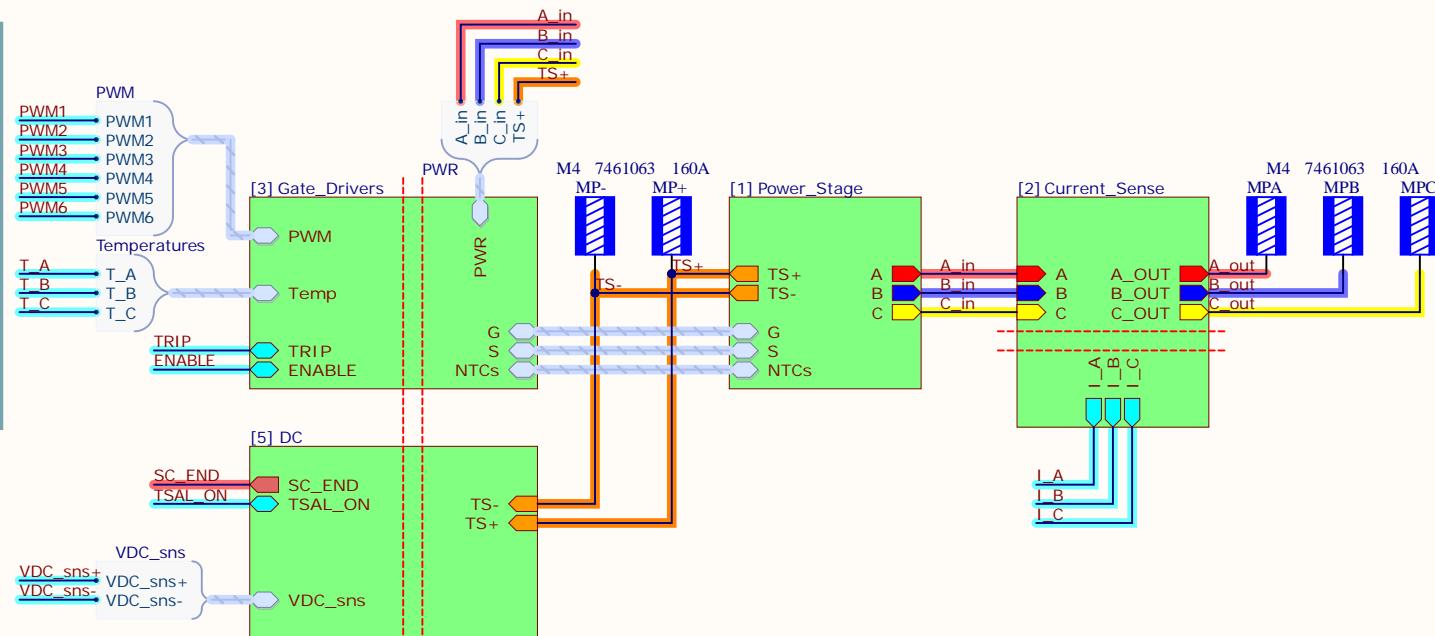
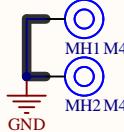
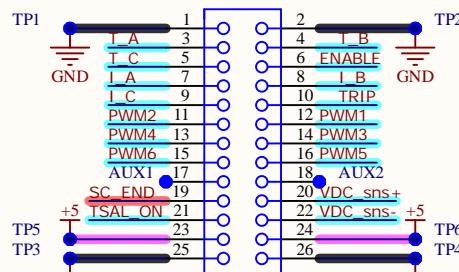
Changes on SCH since production:  
- [MP+] and [MP-] swapped.

Changes on PCB since production:

**PENDING ERRORS:**

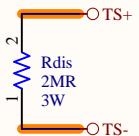
- Silkscreen and positioning of MP+ and MP- in PCB
- LDO\_HS, LDO\_LS pins 4-5 swap in symbol and footprint.

## LV Connector

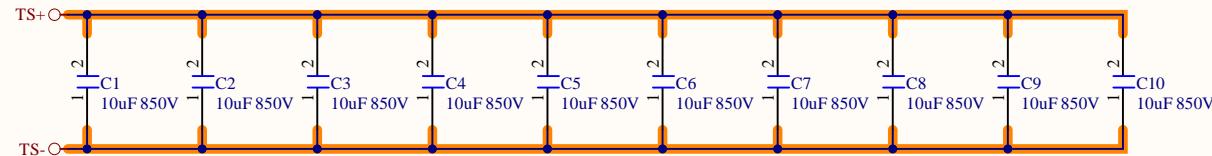


Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Leapers	
Size:	Page Contents: Inverter_Power.SchDoc	Version: 1.0	
		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 1 of 5
Checked by:		Date: 01/03/2024	

## Passive discharge



## DC Bus capacitors, 100uF, Murata FHA85Y106KS



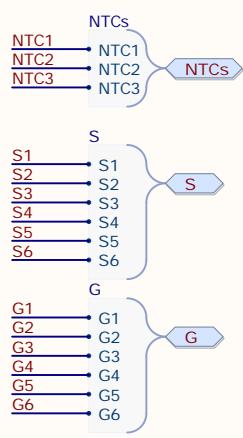
▲ DC Link design considerations:

$V_C > 1.1 \cdot V_{max} = 1.1 \cdot 600 V = 660 V \rightarrow 850 V$

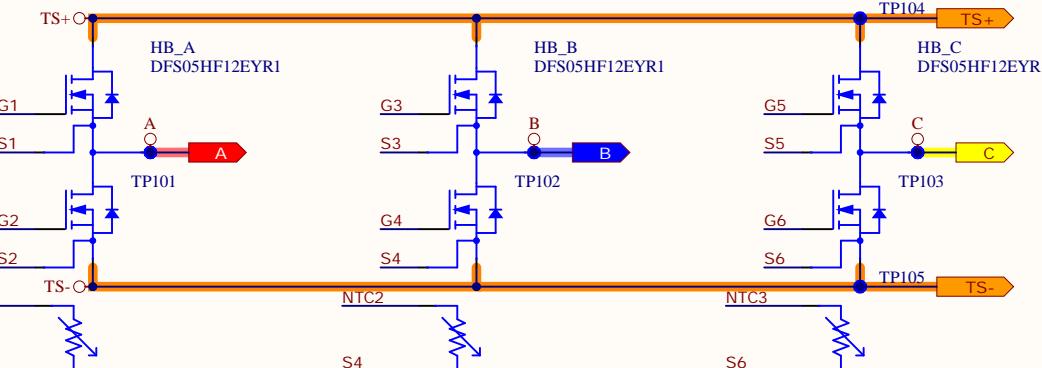
$I_{C,RMS} \approx 0.65 \cdot I_{phase,RMS} = 0.65 \cdot 80 A, RMS = 52 A, RMS \rightarrow 10 \times 5 A, RMS (\Delta T = 10 ^\circ C)$   
 $C > I_{C,RMS} / (V_{ripple} \cdot f_{sw}) = 52 A, RMS / (15V \cdot 50 kHz) \approx 79 \mu F \rightarrow 10 \times 10 \mu F$

Lowering the switching frequency will proportionally lower the current rating for the same voltage ripple or proportionally increase the voltage ripple for the same output current. Check:  
<https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter>

## INPUTS/OUTPUTS



## SiC Half-Bridges



▲ Semiconductor details:

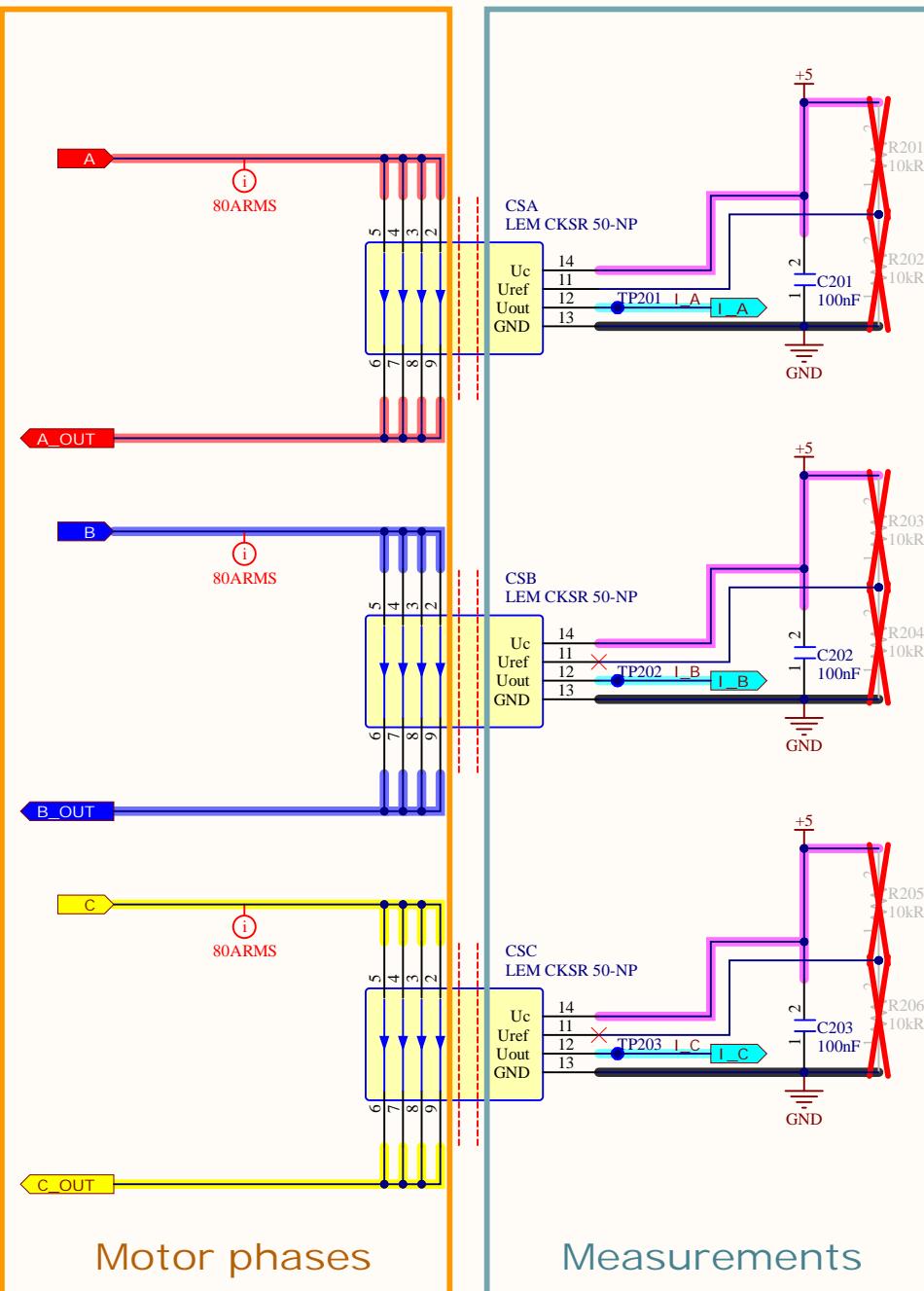
$V_{DSS}(\text{breakdown}) = 1200 V // 1200 V$   
 $R_{on} = 5.5 .. 13 m\Omega // 16.0 .. 28.8 m\Omega$   
 $V_f, D = 3.3 .. 4 V // 4.9 .. 5.5 V$   
 $T_{rr} = 41.5 .. 45 ns // 20.0 ns$   
 $Q_{rr} = 2.19 .. 3.94 \mu C // 1.30 \mu C$   
 $R_{th,Jc} = 0.12 .. 0.15 K/W // 0.543 K/W$   
 $Q_G = 520 nC // 236 nC$   
 $C_{in} = 14.5 nF // 6.6 nF$   
 $R_G(\text{int}) = 1.9 \Omega // 2.4 \Omega$   
 $V_{GS(th)} = 2.8 .. 4.8 V // 1.8 .. 3.6 V$

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Leapers	
Size:	Page Contents: [1]Power_Stage.SchDoc	Version: 1.0	
-		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 2 of 5
Checked by:	_		Date: 01/03/2024

A

CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R\_phase-connector = 0.18 mΩ)



B

CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values. Voltage divider implemented just in case.

I\_A , I\_B , I\_C

$$U_{\text{meas}} = (12.5 \text{mV/A} \cdot I_{\text{meas}} + U_{\text{ref}})$$

For  $\pm 150 \text{Apk}$ :  
 $V_{\text{meas\_pk+}} = 4.375 \text{V}$   
 $V_{\text{meas\_pk-}} = 0.625 \text{V}$

C201 , C202 , C203

The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

C

Company: e-Tech Racing e-techracing.es



Project: Inverter Power Variant: Leapers

Size:	Page Contents: [2]Current_Sense.SchDoc	Version: 1.0
-		Department: Powertrain
Author:	David Redondo dredondovinolo@gmail.com	Sheet 3 of 5
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D

CSA , CSB , CSC

AC insulation test  
RMS voltage, 50 Hz,  
1 min:

$$U_d = 4.3 \text{kV} > 3 \cdot V_{\text{max}} = 1.8 \text{kV}$$

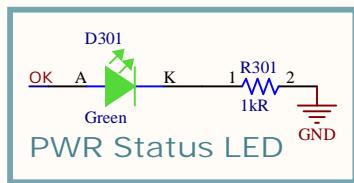
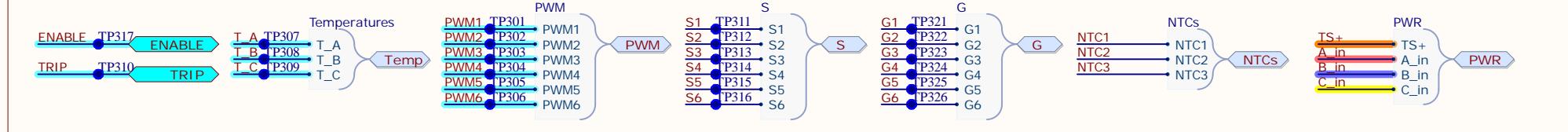
1

2

3

4

## INPUTS/OUTPUTS



**[T\_A, T\_B, T\_C]**  
Look-up table obtained with MATLAB script which can be found in the simulations folder.

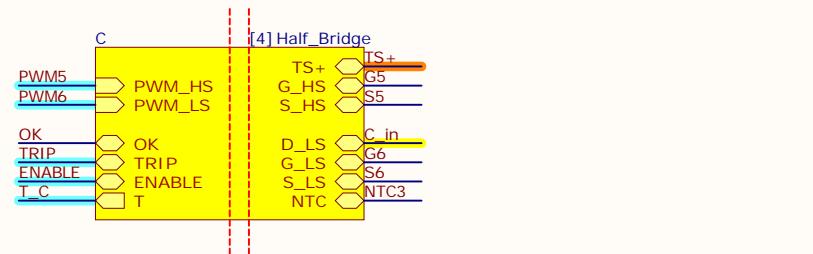
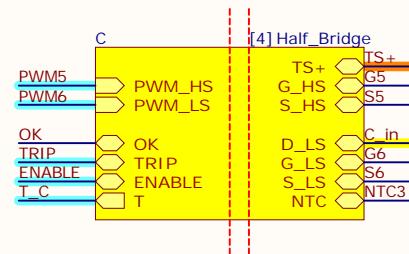
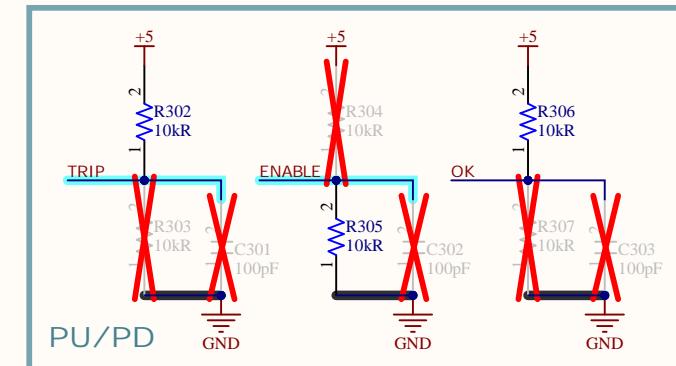
For different temperatures:  
 $V_{\text{meas}}(0^\circ\text{C}) = 0.246\text{V}$   
 $V_{\text{meas}}(25^\circ\text{C}) = 2\text{V}$   
 $V_{\text{meas}}(50^\circ\text{C}) = 2.578\text{V}$   
 $V_{\text{meas}}(90^\circ\text{C}) = 2.864\text{V}$

B

B

C

C



D

D

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Leapers	
Size:	Page Contents: [3]Gate_Drivers.SchDoc	Version: 1.0	
-		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 4 of 5
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1

2

3

4

A

**▲ U\_HS, U\_LS**

1. **TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to **GND**.
3. **ENABLE** to be given by MCU in active-high mode. When set to low for more than 1  $\mu$ s, **TRIP** is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200  $\mu$ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **[R405]**, **[R406]** and **[C411]** from SPICE simulation.
5. Miller clamp protection is used.
6. **RGS\_HS**, **RGS\_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
7. Overcurrent detection is not implemented.

**▲ LDO\_HS, LDO\_LS**

An LDO is implemented to trim **VEE\_HS\_A** and **VEE\_LS\_A** during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

$$\text{VEE} = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers  $\rightarrow R1 = 36 \text{ k}\Omega$ ,  $R2 = 56 \text{ k}\Omega$

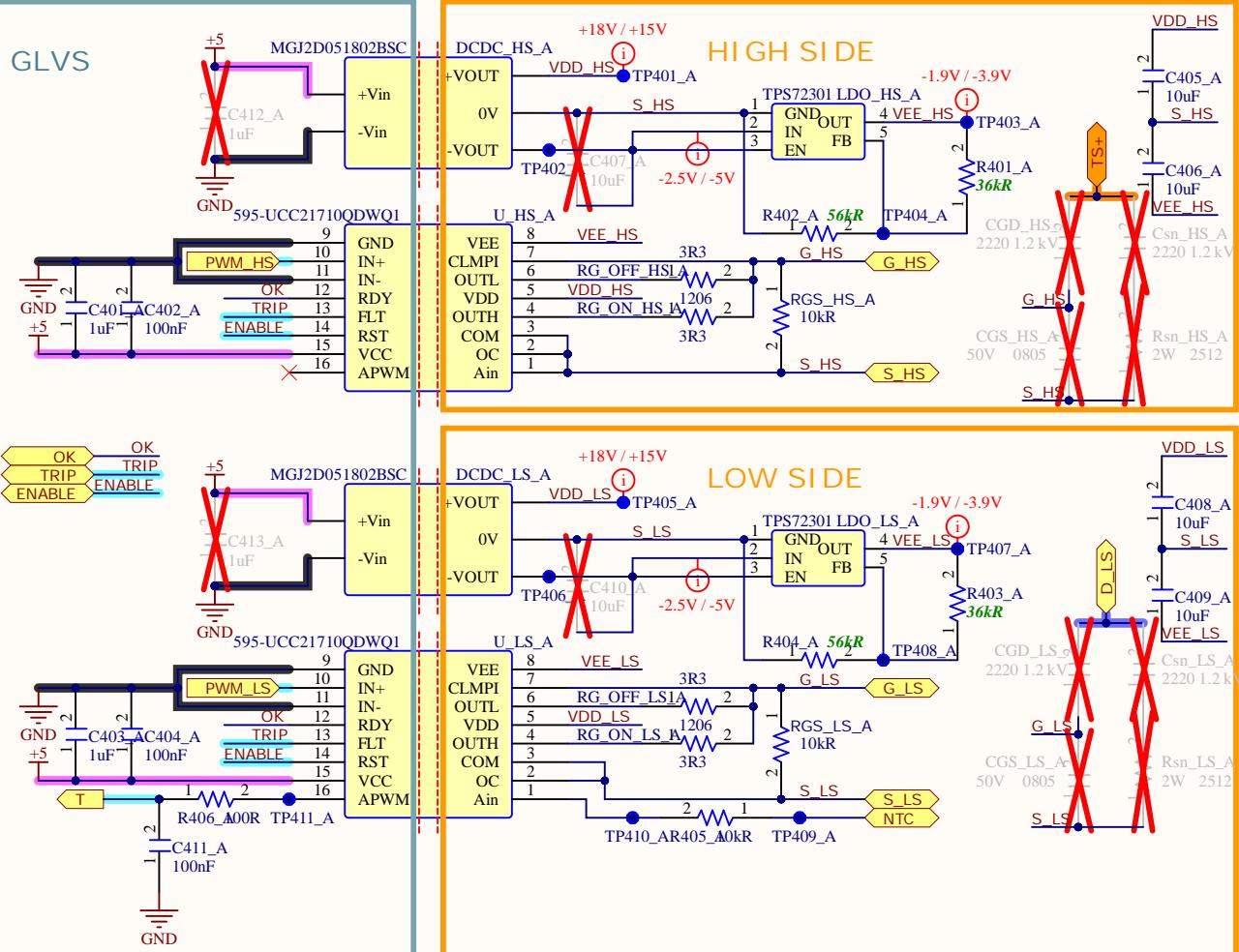
Wolfspeed  $\rightarrow R1 = 68 \text{ k}\Omega$ ,  $R2 = 30 \text{ k}\Omega$

**▲ DCDC\_HS, DCDC\_LS**

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

**▲ U\_HS, U\_LS**

VIOTM ( $t = 60$  s (qualification test)): 8000 VPK

**GLVS****▲ V\_GS values:**

The values can be modified by replacing **DCDC\_HS** and **DCDC\_LS** with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

Minimum gate driver current and power:  
 $I_{GD(\min)} = f_{sw} \cdot O_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$   
 $P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

**▲ RG\_ON\_HS, RG\_OFF\_HS, RG\_ON\_LS, RG\_OFF\_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the  $dV/dt$  will be higher, which can be responsible of EMI increase. The considered values of 3.3  $\Omega$  are recommended by the datasheet.

**CGS\_HS**, **CGS\_LS**, **CGD\_HS**, **CGD\_LS**, **Csn\_HS**, **Csn\_LS**, **Rsn\_HS**, **Rsn\_LS**

DNP, but they could be useful with EMI related issues to decrease  $dV/dt$ . Implementing them could avoid issues with the power limit for **DCDC\_HS** and **DCDC\_LS**, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

Company: e-Tech Racing e-techracing.es



Project: Inverter Power Variant: Leapers

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Checked by:		Date: 01/03/2024

A

**U\_HS, U\_LS**

- TRIP and OK signals are in open drain configuration, so they can be paralleled.
- IN- is not used and tied to GND.
- ENABLE to be given by MCU in active-high mode. When set to low for more than 1  $\mu$ s, TRIP is reset.
- Temperature sensing using low-side drivers. Ain outputs a current of 200  $\mu$ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. [R405], [R406] and [C411] from SPICE simulation.
- Miller clamp protection is used.
- RGS\_HS, RGS\_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
- Overcurrent detection is not implemented.

**LDO\_HS, LDO\_LS**

An LDO is implemented to trim VEE\_HS\_A and VEE\_LS\_A during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

$$\text{VEE} = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers  $\rightarrow R1 = 36 \text{ k}\Omega$ ,  $R2 = 56 \text{ k}\Omega$

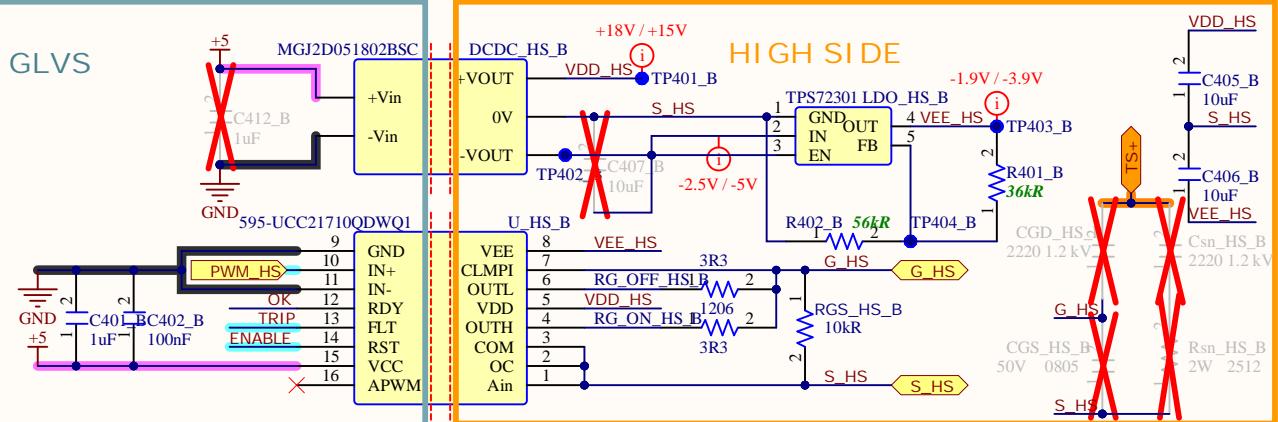
Wolfspeed  $\rightarrow R1 = 68 \text{ k}\Omega$ ,  $R2 = 30 \text{ k}\Omega$

**DCDC\_HS, DCDC\_LS**

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

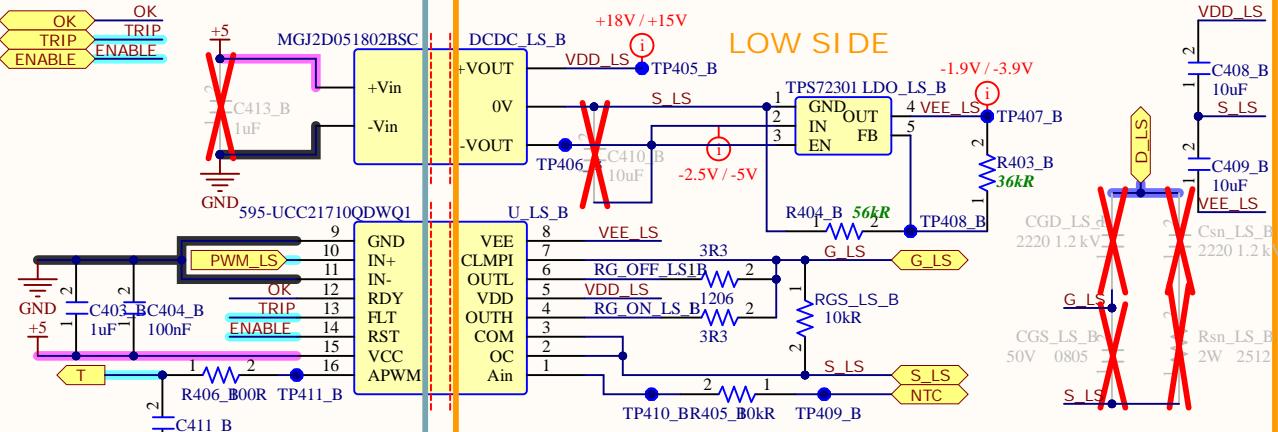
**U\_HS, U\_LS**

VIOTM ( $t = 60$  s (qualification test)): 8000 VPK

**GLVS****V\_GS values:**

The values can be modified by replacing DCDC\_HS and DCDC\_LS with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

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 $P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

**OK, TRIP, ENABLE****RG\_ON\_HS, RG\_OFF\_HS, RG\_ON\_LS, RG\_OFF\_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.0  $\Omega$  are recommended by the datasheet.

CGS\_HS, CGS\_LS, CGD\_HS, CGD\_LS, Csn\_HS, Csn\_LS, Rsn\_HS, Rsn\_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could avoid issues with the power limit for DCDC\_HS and DCDC\_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

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Project: Inverter Power Variant: Leapers

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A

**U\_HS, U\_LS**

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- IN- is not used and tied to GND.
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$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers  $\rightarrow R1 = 36 \text{ k}\Omega$ ,  $R2 = 56 \text{ k}\Omega$

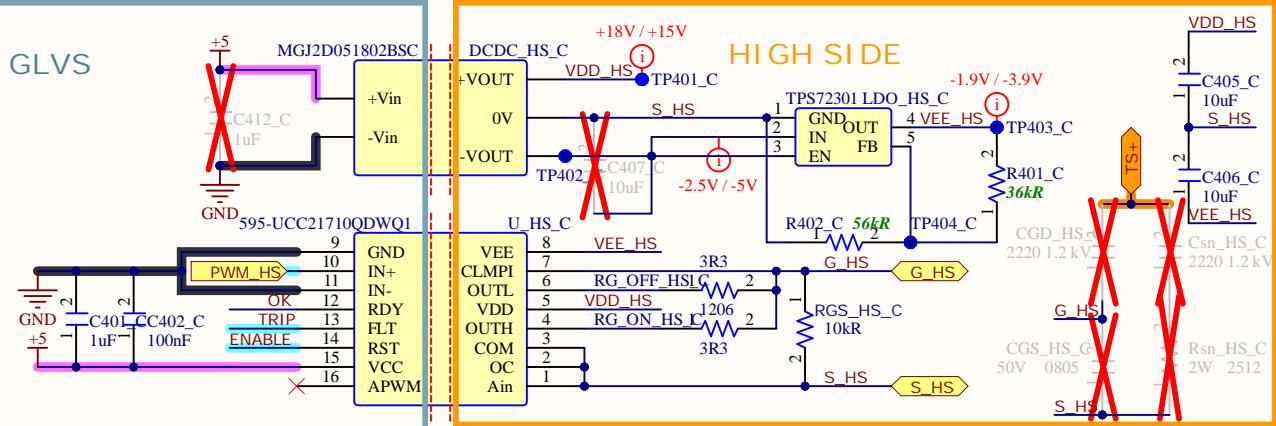
Wolfspeed  $\rightarrow R1 = 68 \text{ k}\Omega$ ,  $R2 = 30 \text{ k}\Omega$

**DCDC\_HS, DCDC\_LS**

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

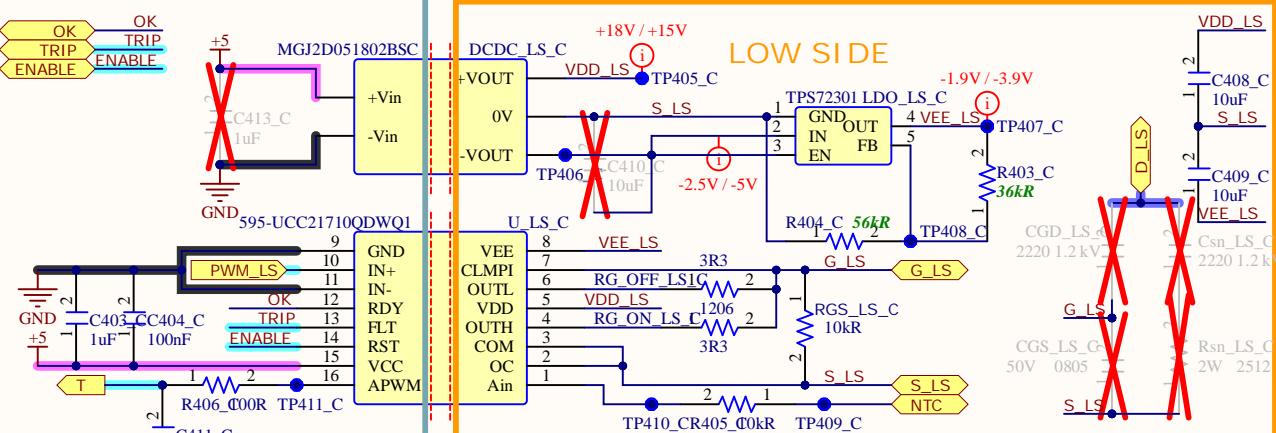
**U\_HS, U\_LS**

VIOTM ( $t = 60$  s (qualification test)): 8000 VPK

**GLVS****V\_GS values:**

The values can be modified by replacing DCDC\_HS and DCDC\_LS with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

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 $P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

**OK, TRIP, ENABLE****RG\_ON\_HS, RG\_OFF\_HS, RG\_ON\_LS, RG\_OFF\_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3  $\Omega$  are recommended by the datasheet.

CGS\_HS, CGS\_LS, CGD\_HS, CGD\_LS, Csn\_HS, Csn\_LS, Rsn\_HS, Rsn\_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could avoid issues with the power limit for DCDC\_HS and DCDC\_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

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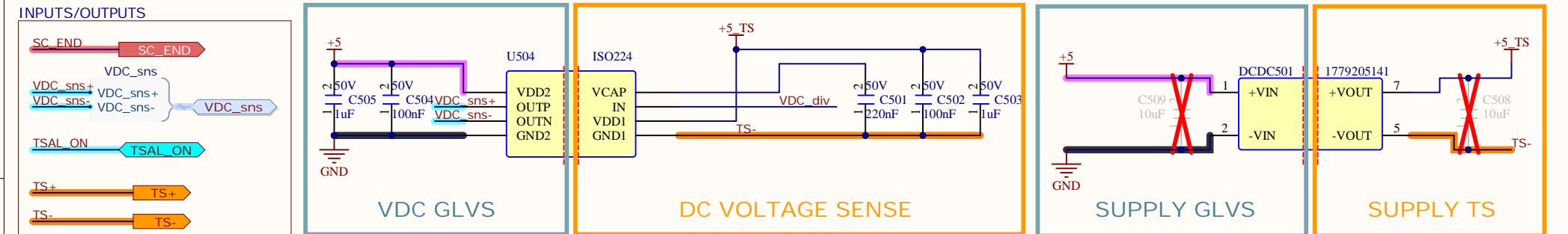
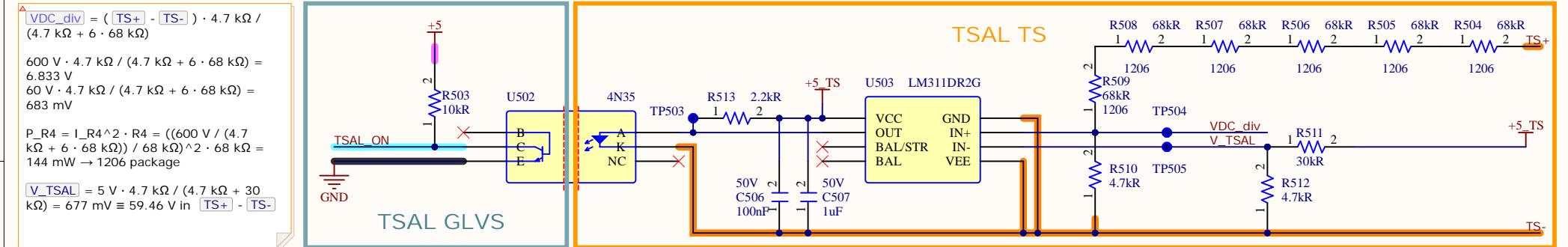
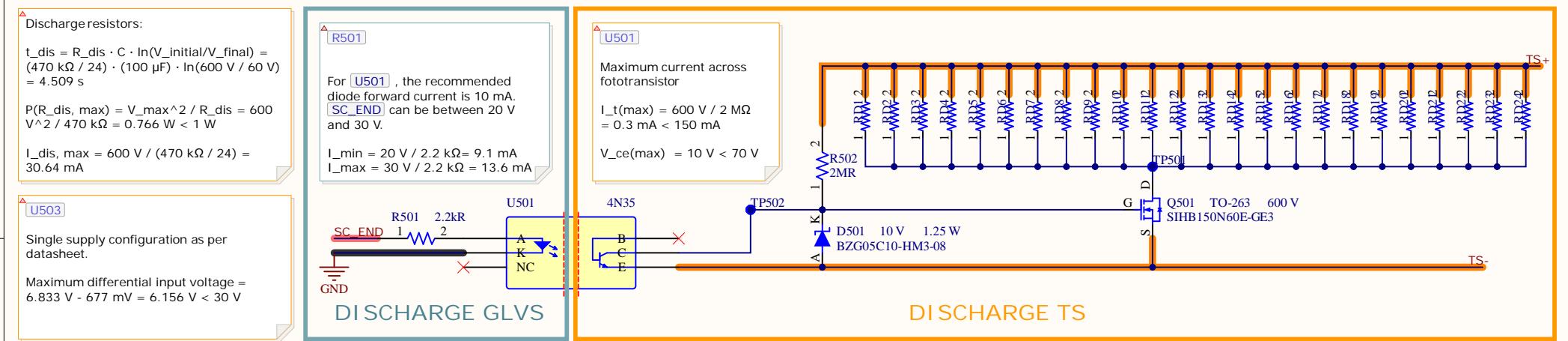


Project: Inverter Power Variant: Leapers

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Author: David Redondo dredondovinolo@gmail.com Sheet 5 of 5

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(TS+ - TS-) > 60V → TSAL\_ON = 0V  
(TS+ - TS-) < 60V → TSAL\_ON = 5V

$$\begin{aligned}
 & (\text{VDC\_sns+} - \text{VDC\_sns-}) = 1/3 \cdot \\
 & \quad [\text{VDC\_div}] = 1/3 \cdot ((\text{TS+} - \text{TS-})) \\
 & 4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega) = 1/3 \cdot \\
 & 0.011388 \cdot (\text{TS+} - \text{TS-}) \\
 \\ 
 & (\text{VDC\_sns+} - \text{VDC\_sns-}) = 1/3 \cdot \\
 & 0.011388 \cdot 600 \text{ V} = 2.278 \text{ V}
 \end{aligned}$$

**U501**, **U502**

Isolation Voltage: AC For 1 Minute,  
R.H. = 40 ~ 60% Viso = 5000 Vrms

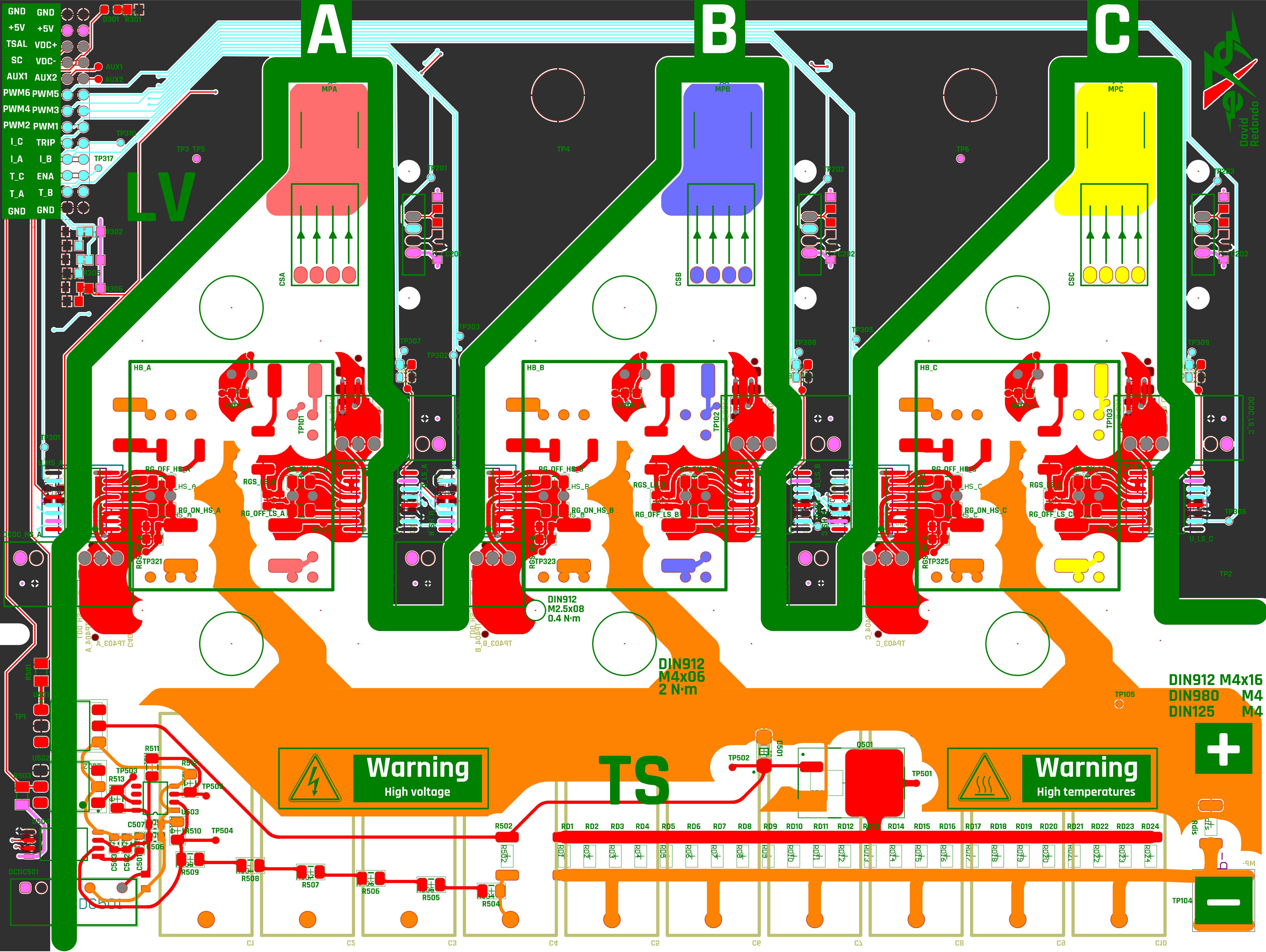
**U504**

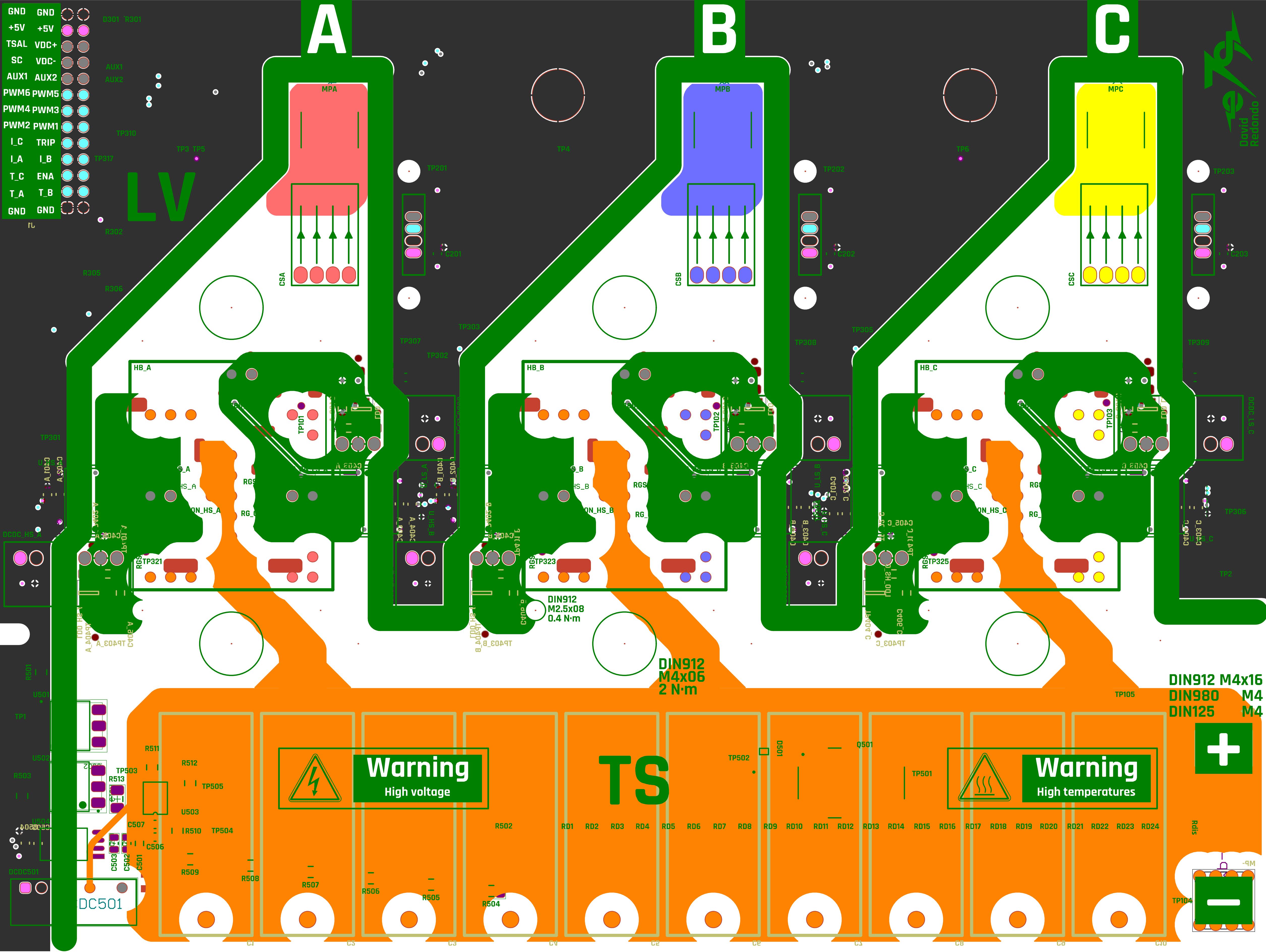
Maximum transient isolation voltage:  
VTEST = VIOTM, t = 60 s (qualification  
test) VIOTM = 7071 Vpk

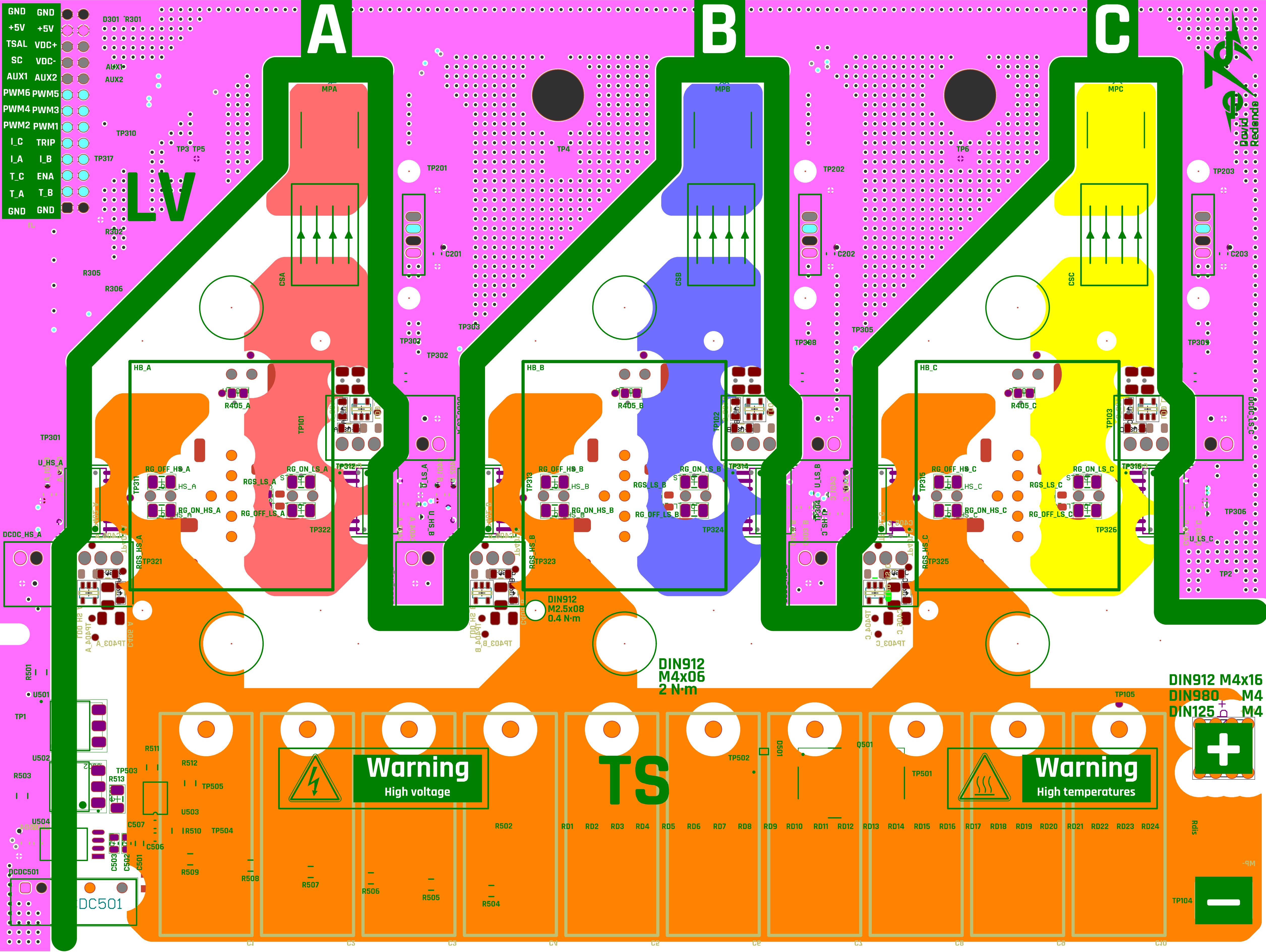
**DCDC501**

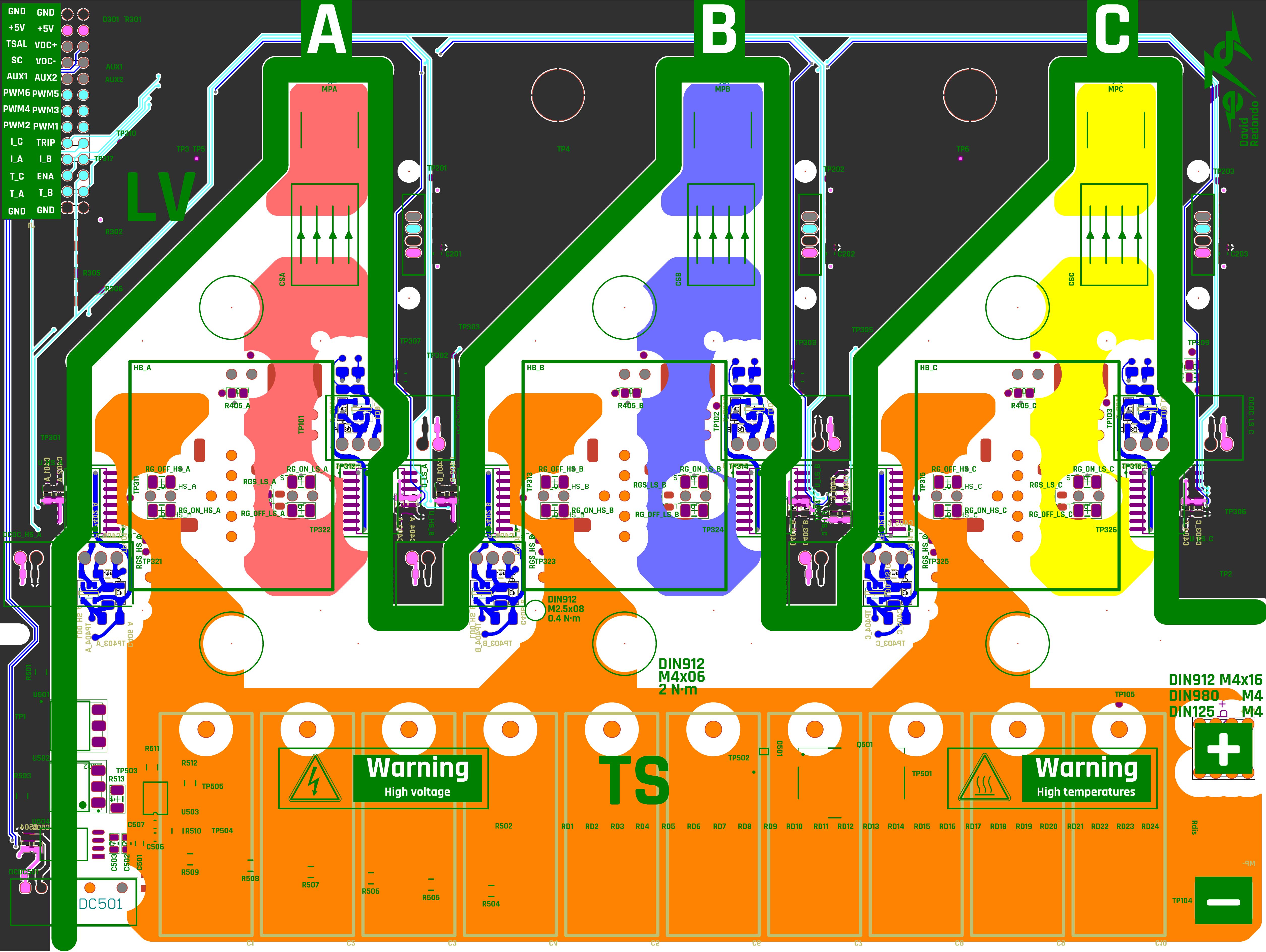
Isolation voltage input to output  
tested 100% for 60s(2)  
VISO = 3000 V

<b>Company:</b>	e-Tech Racing	e-techracing.es	
<b>Project:</b>	Inverter Power	<b>Variant:</b> Leapers	
<b>Size:</b>	<b>Page Contents:</b> - [5] DC.SchDoc	<b>Version:</b>	1.0
		<b>Department:</b>	Powertrain
<b>Author:</b>	David Redondo	dredondovinolo@gmail.com	Sheet * of *
<b>Checked by:</b>	-	Date:	01/03/2024

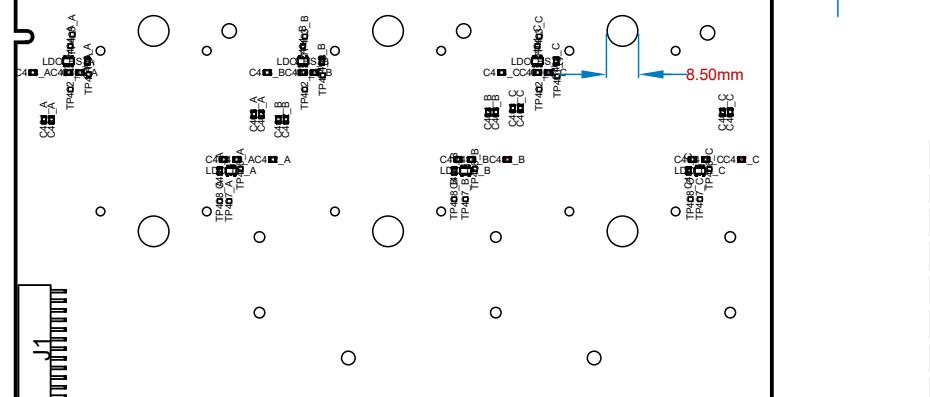
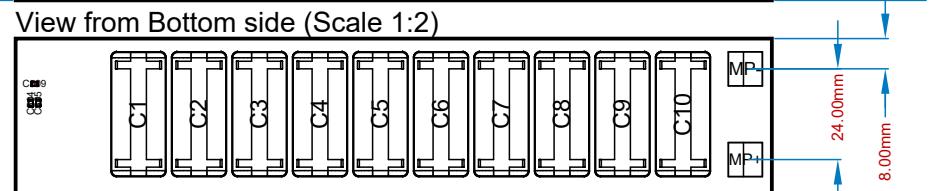
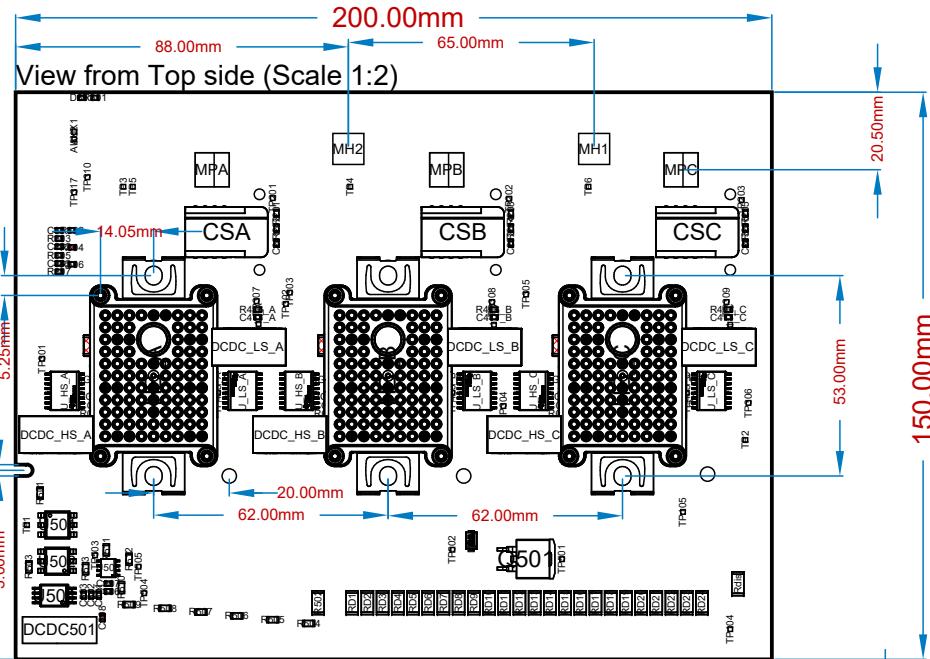








# Inverter Power



## Bill Of Materials

Designator	Name	Quantity
C405_A, C405_B, C405_C, C406_A, C406_B, C406_C, C408_A, C408_B, C408_C	10uF	12
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	10uF 850V	10
DDC501	1779205141	1
J1	613026243121	1
R401_A, R401_B, R401_C, R403_A, R403_B, R403_C	CR0805-JW-563ELF	6
R402_A, R402_B, R402_C, R404_A, R404_B, R404_C	CR0805-JW-563ELF	6
R511	CRCW120610K0FKEA	1
HB_A, HB_B, HB_C	CRCW120630K0FKEA	1
MP_-, MP+, MP_A, MP_B, MPC	DF50HF12EYR1	3
MH1, MH2	M4	5
RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24	Mounting Hole M4	2
RCV2512470KFKEG	RCV2512470KFKEG	24
R406_A, R406_B, R406_C	CR0805-FX-1000ELF	3
R301	CR0805-JW-102ELF	1
R302, R305, R306, R405_A, R405_B, R405_C, RGS_HS_A, RGS_HS_B, RGS_HS_C, RGS_HS_L_A, RGS_HS_L_B, RGS_HS_L_C	CR0805-JW-103ELF	12
R504, R505, R506, R507, R508, R509	CR1206FX-6802EAS	6
R501, R513	CR1206-FX-2201ELF	2
R510, R512	CRS1206-FX-4701ELF	2
CSA, CSB, CSC	LEM CKSR 50-NP	3
DCDC_HS_A, DCDC_HS_B, DCDC_HS_C, DCDC_HS_D, DCDC_LS_A, DCDC_LS_B, DCDC_LS_C	MJGJ6-series	6
U503	LMS311DR2G	1
C501	885012208058	1
RG_OFF_HS_A, RG_OFF_HS_B, RG_OFF_HS_C, RG_OFF_HS_D, RG_OFF_HS_E, RG_OFF_HS_F, RG_OFF_HS_G, RG_OFF_HS_H, RG_ON_HS_A, RG_ON_HS_B, RG_ON_HS_C, RG_ON_HS_D, RG_ON_HS_E, RG_ON_HS_F, RG_ON_HS_G, RG_ON_HS_H	CRG1206F100R	12
U504	ISO224	1
LDO_HS_A, LDO_HS_B, LDO_HS_C, LDO_HS_D, LDO_HS_E, LDO_HS_F, LDO_HS_G, LDO_HS_H	TPS72301	6
U HS_A, U HS_B, U HS_C, U LS_A, U LS_B, U LS_C	UCC21710	6
Q501	SIHB150N60E-GE3	1
R502, Rds	R2M-2512FTK	2
U501, U502	4N35	2
D501	BZG06C10	1
D301	150080GS75000	1
C201, C202, C203, C402_A, C402_B, C402_C, C404_A, C404_B, C404_C, C411_A, C411_B, C411_C, C502, C504, C506	885012207098	15
C401_A, C401_B, C401_C, C403_A, C403_B, C403_C, C503, C505, C507	885012207103	9

Copper thickness in hole 25-50um, watch out for 1.10mm holes  
Chemical tin 1-15um

## Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay				GTO
	Surface Material	0.01mm	Solder Resist		GTS
CF-004	TOP	0.07mm		Signal	GTL
	Prepreg	0.10mm	PP-006		Dielectric
	Prepreg	0.10mm	PP-006		Dielectric
Copper	GND	0.07mm	Signal	G1	
	FR-4	0.90mm			Dielectric
Copper	PWR	0.07mm	Signal	G2	
	Prepreg	0.10mm	PP-006		Dielectric
	Prepreg	0.10mm	PP-006		Dielectric
CF-004	BOT	0.07mm		Signal	GBL
	Surface Material	0.01mm	Solder Resist		GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.60mm