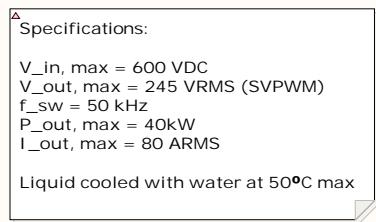
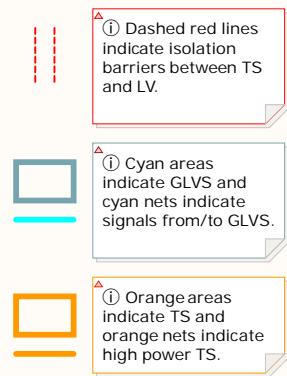
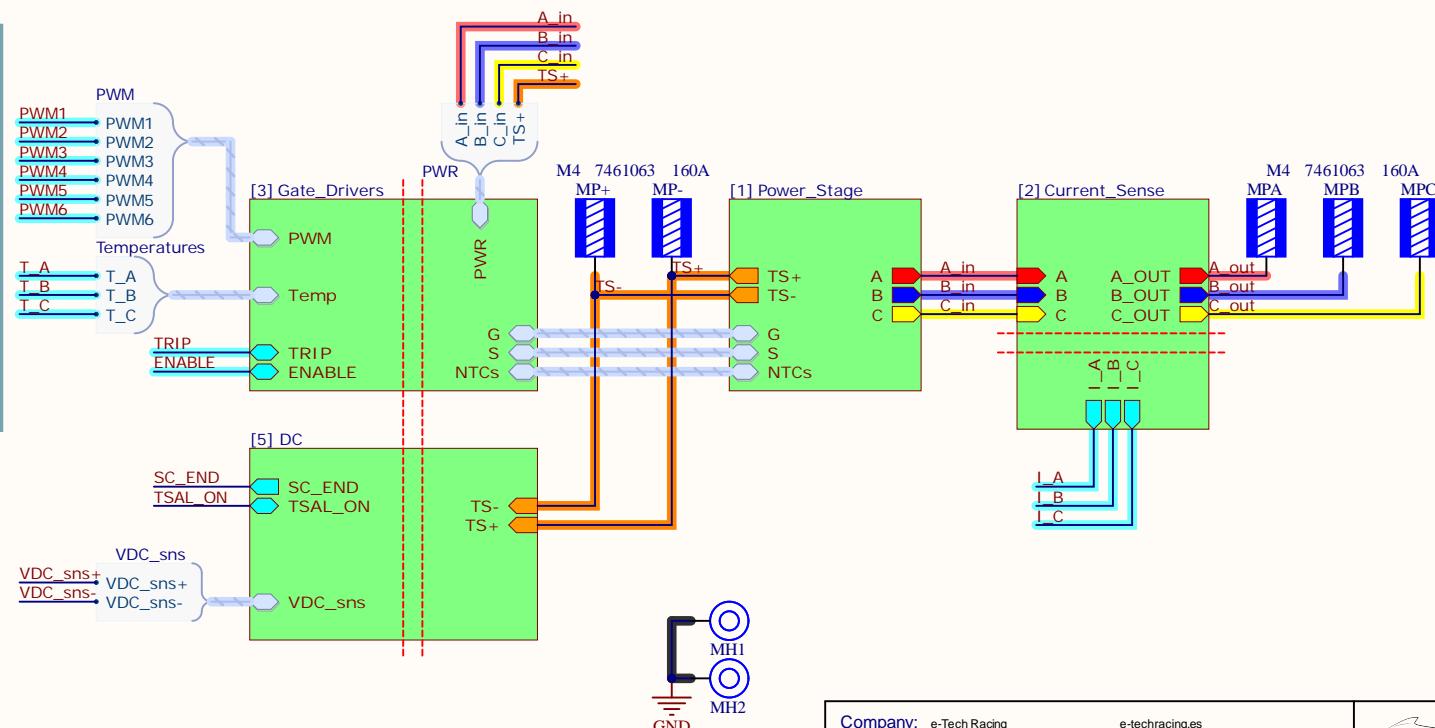
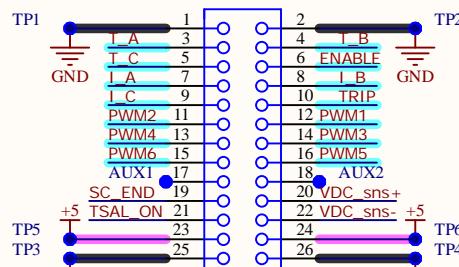


A

A



LV Connector

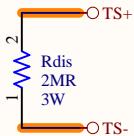


Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Inverter_Power	
Size:	Page Contents: Inverter_Power.SchDoc	Version: 1.0	
-		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 1 of 5
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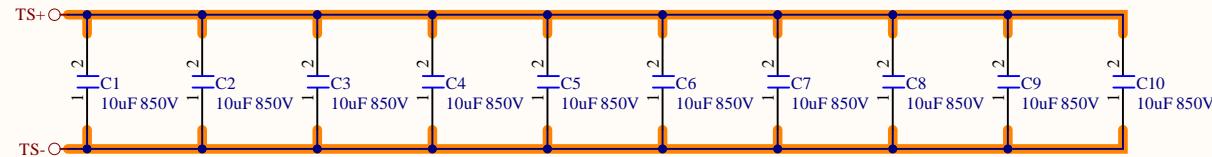
A

A

Passive discharge



DC Bus capacitors, 100uF, Murata FHA85Y106KS



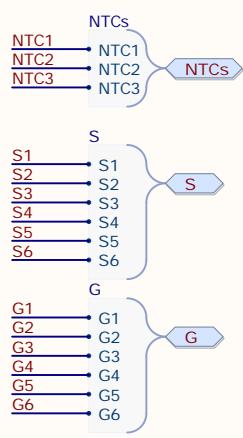
DC Link design considerations:

$V_C > 1.1 \cdot V_{max} = 1.1 \cdot 600 V = 660 V \rightarrow 850 V$

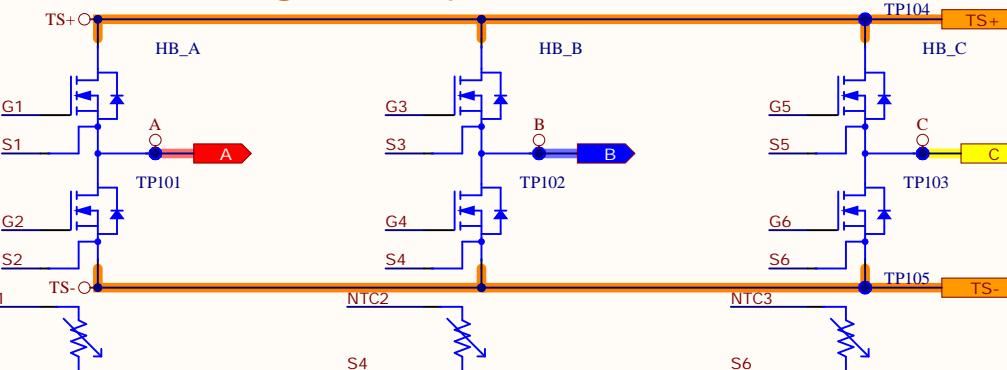
$I_{C,RMS} \approx 0.65 \cdot I_{phase,RMS} = 0.65 \cdot 80 A, RMS = 52 A, RMS \rightarrow 10 \times 5 A, RMS (\Delta T = 10 ^\circ C)$
 $C > I_{C,RMS} / (V_{ripple} \cdot f_{sw}) = 52 A, RMS / (15V \cdot 50 kHz) \approx 79 \mu F \rightarrow 10 \times 10 \mu F$

Lowering the switching frequency will proportionally lower the current rating for the same voltage ripple or proportionally increase the voltage ripple for the same output current. Check:
<https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-your-inverter>

INPUTS/OUTPUTS



SiC Half-Bridges, Leapers DFS05HF12EYR1



Semiconductor details:

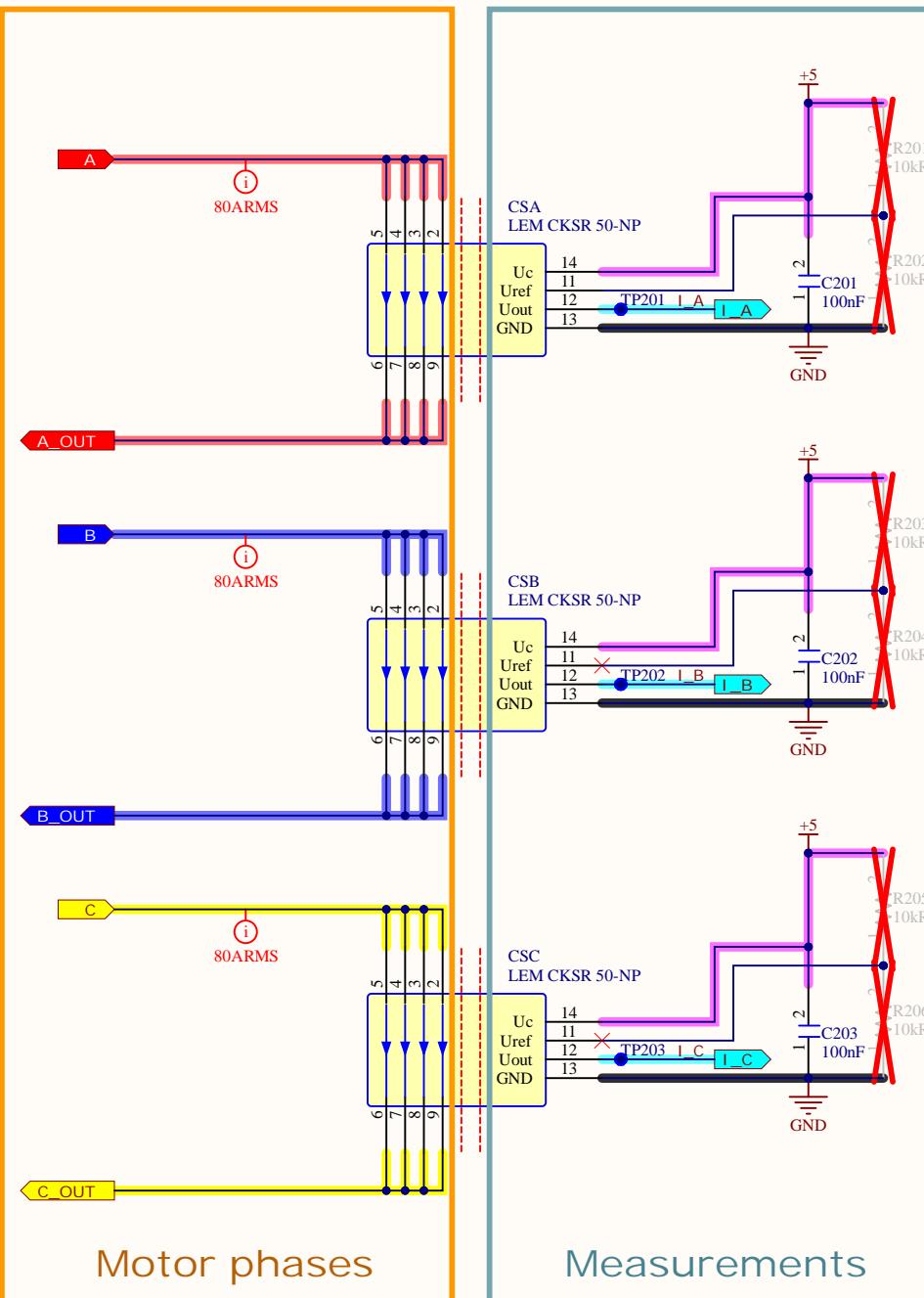
$V_{DSS}(\text{breakdown}) = 1200 V$
 $R_{on} = 5.5 \dots 13 m\Omega$
 $V_f, D = 3.3 \dots 4 V$
 $T_{rr} = 41.5 \dots 45 ns$
 $Q_{rr} = 2.19 \dots 3.94 \mu C$
 $R_{th,jc} = 0.12 \dots 0.15 K/W$
 $Q_G(600V, 150A, V_{GS} = +15/0V) = 520 nC$
 $C_{in} = 14.5 nF$
 $R_G(\text{int}) = 1.9 \Omega$
 $V_{GS(th)} = 2.8 \dots 4.8 V$

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Inverter_Power	
Size:	Page Contents: [1]Power_Stages.SchDoc	Version: 1.0	
-		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 2 of 5
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A

CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R_phase-connector = 0.18 mΩ)



B

C

D

A

B

C

D

CSA , CSB , CSC

AC insulation test
RMS voltage, 50 Hz,
1 min:

$U_d = 4.3 \text{ kV} >$
 $3 \cdot V_{max} = 1.8 \text{ kV}$

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant:	Inverter_Power
Size:	Page Contents: [2]Current_Sense.SchDoc	Version:	1.0
-		Department:	Powertrain
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 3 of 5
Checked by:	_	Date:	13/02/2024

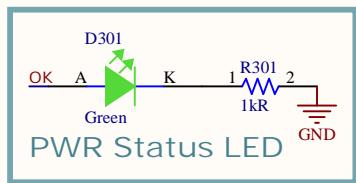
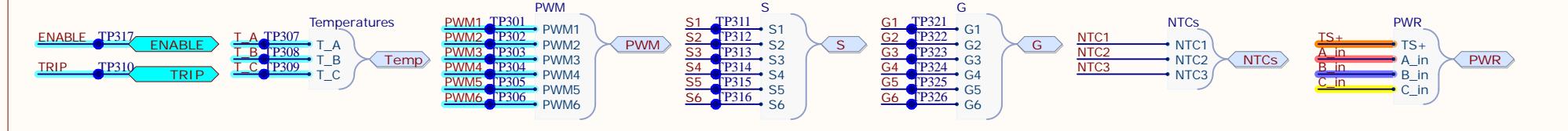
1

2

3

4

INPUTS/OUTPUTS



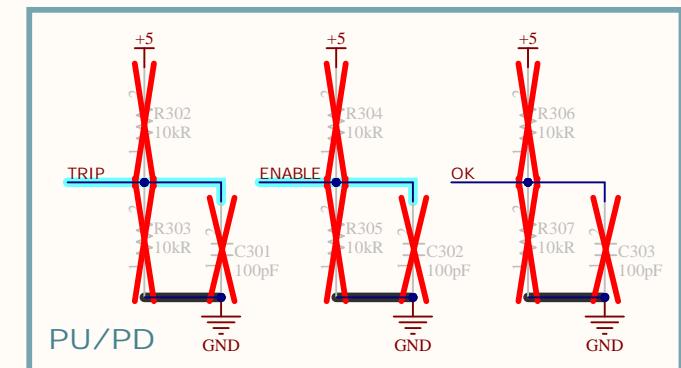
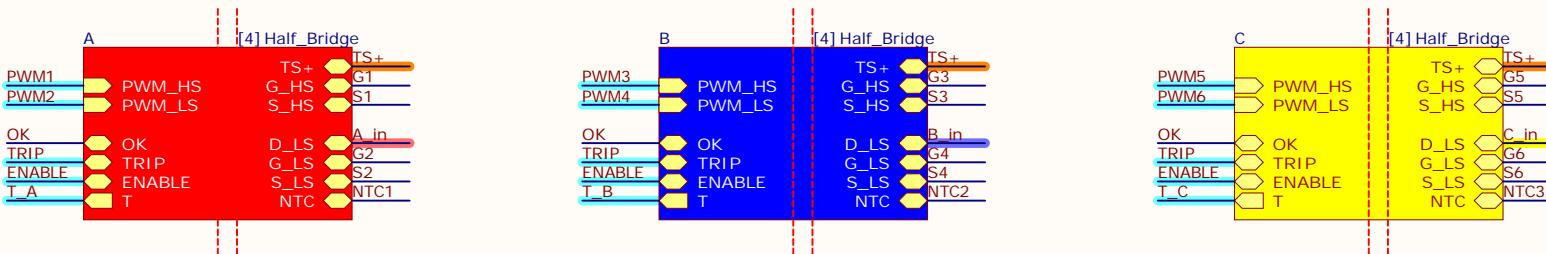
Look-up table obtained with MATLAB script.

For different temperatures:

- $V_{meas}(0^\circ\text{C}) = 0.246\text{V}$
- $V_{meas}(25^\circ\text{C}) = 2\text{V}$
- $V_{meas}(50^\circ\text{C}) = 2.578\text{V}$
- $V_{meas}(90^\circ\text{C}) = 2.864\text{V}$

B

B



Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Inverter_Power	
Size:	Page Contents: [3]Gate_Drivers.SchDoc	Version: 1.0	
-		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 4 of 5
Checked by:			Date: 13/02/2024

1

2

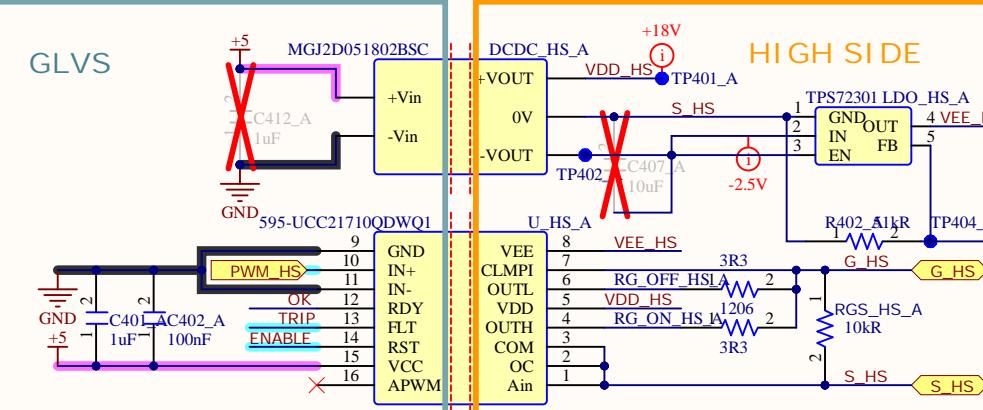
3

4

A

U_HS, U_LS

- TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
- IN- is not used and tied to **GND**.
- ENABLE** to be given by MCU in active-high mode. When set to low for more than 1 μ s, **TRIP** is reset.
- Temperature sensing using low-side drivers. Ain outputs a current of 200 μ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **R405**, **R406** and **C411** from SPICE simulation.
- Miller clamp protection is used.
- RGS_HS**, **RGS_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
- Overcurrent/Shoot-through detection is not implemented.

GLVS

B

LDO_HS, LDO_LS

An LDO is implemented to trim **VEE_HS_A** and **VEE_LS_A** during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, **DCDC_HS** and **DCDC_LS** must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing

$$V_{GS} = +18 \text{ V} / -2 \text{ V}$$

$$VEE = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

C

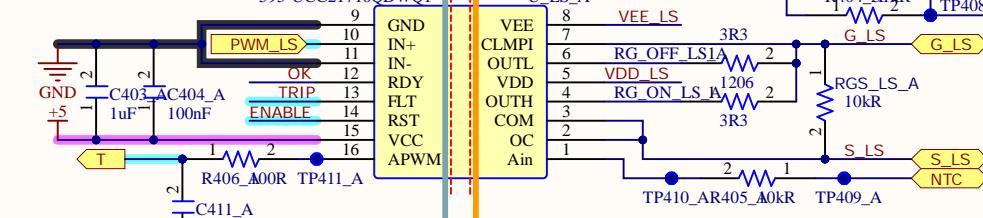
DCDC_HS, DCDC_LS

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS

VIOTM ($t = 60$ s (qualification test)):

$$8000 \text{ VPK}$$

OK**TRIP****ENABLE****V_GS values:**

The values chosen for V_{GS} are +18 / -2 V. Even though Leapers recommends using +18 / 0 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum $V_{GS}(th)$. A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:
 $I_{GD(min)} = f_{sw} \cdot Q_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$

$$P_{min} = \Delta V_{GS} \cdot I_{GD(min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$$

RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.0 Ω are recommended by the datasheet.

CGS_HS, **CGS_LS**, **CGD_HS**, **CGD_LS**, **Csn_HS**, **Csn_LS**, **Rsn_HS**, **Rsn_LS**

DNP, but they could be useful with EMI related issues to decrease dV/dt . Implementing them could result in further issues with the power limit for **DCDC_HS** and **DCDC_LS**, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

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Project:	Inverter Power	Variant: Inverter_Power	
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Author:	David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5
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U_HS, **U_LS**

1. **TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
 2. IN- is not used and tied to **GND**.
 3. **ENABLE** to be given by MCU in active-high mode. When set to low for more than 1 μ s, **TRIP** is reset.
 4. Temperature sensing using low-side drivers. Ain outputs a current of 200 μ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **R405**, **R406** and **C411** from SPICE simulation.
 5. Miller clamp protection is used.
 6. **RGS_HS**, **RGS_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
 7. Overcurrent/Shoot-through detection is not implemented.

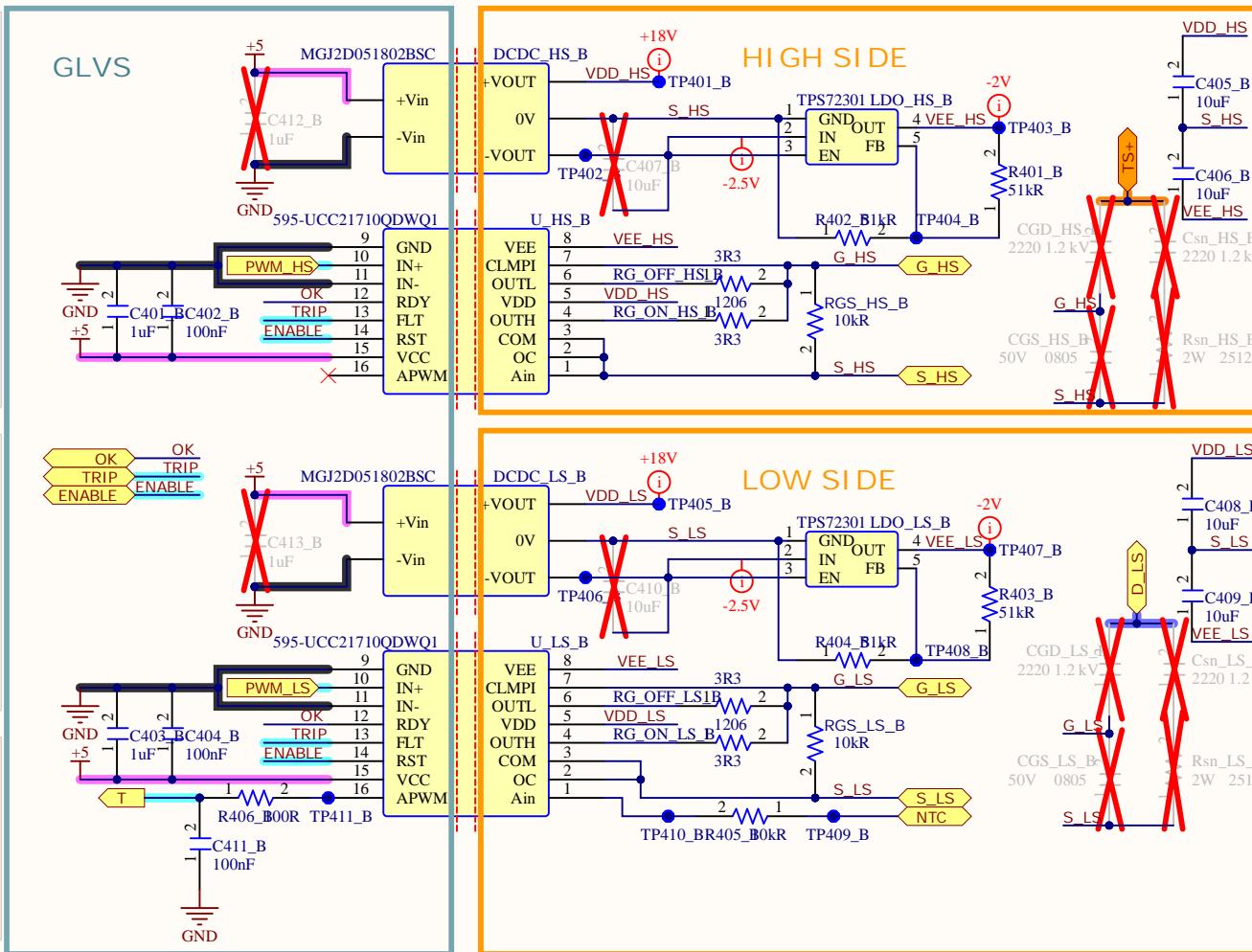
LDO HS LDO LS

An LDO is implemented to trim `VEE_HS_A` and `VEE_LS_A` during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, `[DCDC_HS]` and `[DCDC_LS]` must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing
 $V_{GS} = +18 \text{ V} / -2 \text{ V}$
 $VEE = -1.186 \cdot (1 + R1/R2)$
 $R1 + R2 \approx 100 \text{ k}\Omega$

DCDC_HS, **DCDC_LS**

U_HS, **U_LS**



► V_{GS} values

The values chosen for V_{GS} are +18 V / -2 V. Even though Leapers recommends using +18 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum $V_{GS(th)}$. A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

$$\begin{aligned} & \text{Minimum gate driver current and power:} \\ & I_{GD(\min)} = f_{sw} \cdot Q_G = 50 \text{ kHz} \cdot 520 \text{ nC} = \\ & 26 \text{ mA} \\ & P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 26 \text{ mA} = \\ & 0.52 \text{ W} \rightarrow 2 \text{ W} \end{aligned}$$

RG_ON_HS, **RG_OFF_HS**
RG_ON_LS, **RG_OFF_LS**

- Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

B
kV CGS_HS CGS_LS CGD_HS CGD_LS
Csn_HS Csn_LS Rsp_HS Rsp_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt . Implementing them could result in further issues with the power limit for [DCDC_HS](#) and [DCDC_LS](#), as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) \\ = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Inverter_Power	
Size: -	Page Contents: [4] Half_Bridge.SchDoc	Version: 1.0	
		Department:	Powertrain
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5
Checked by:	-	Date:	13/02/2024

U_HS, **U_LS**

- TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
 - IN- is not used and tied to **GND**.
 - ENABLE** to be given by MCU in active-high mode. When set to low for more than 1 μ s, **TRIP** is reset.
 - Temperature sensing using low-side drivers. Ain outputs a current of 200 μ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **R405**, **R406** and **C411** from SPICE simulation.
 - Miller clamp protection is used.
 - RGS_HS**, **RGS_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
 - Overcurrent/Shoot-through detection is not implemented.

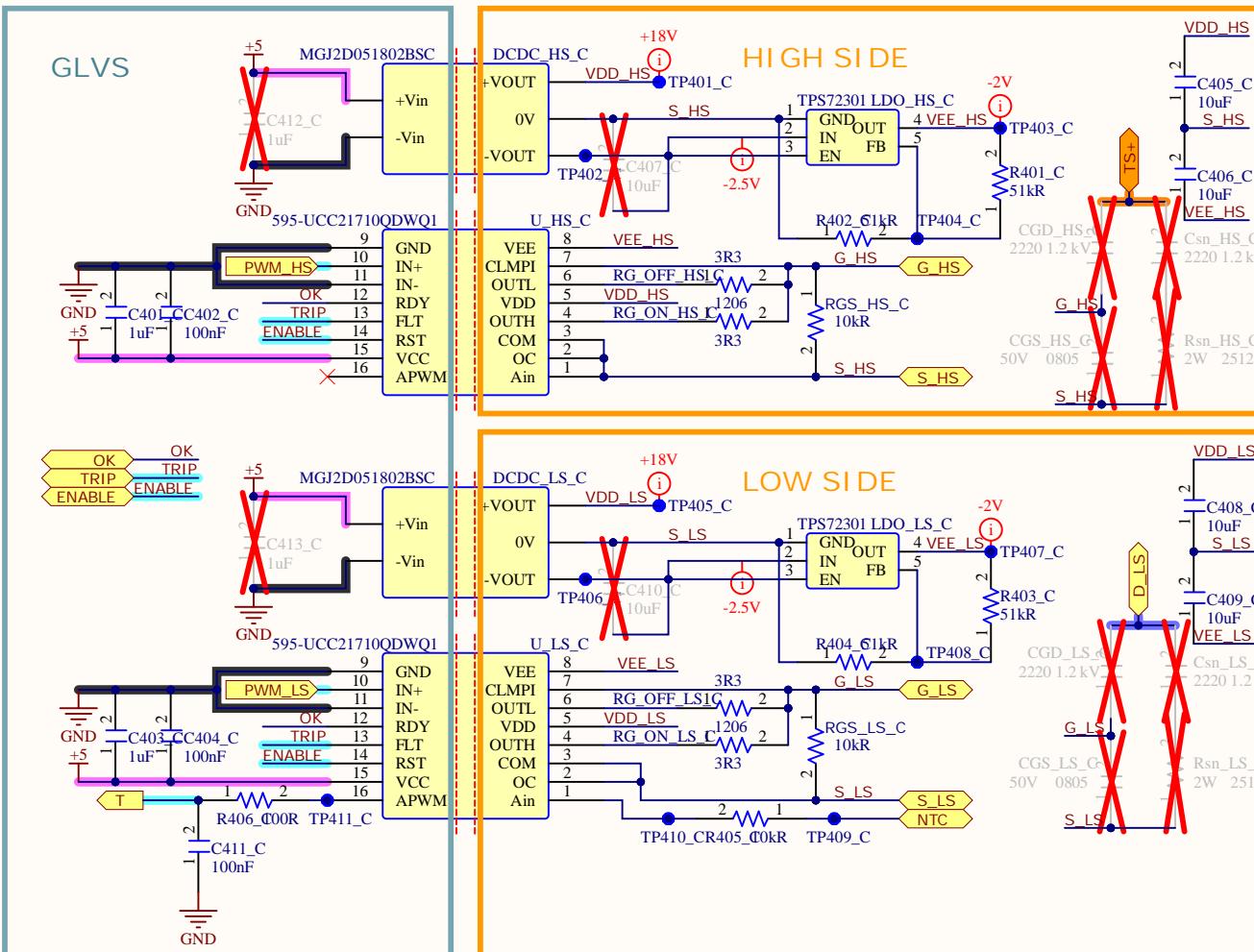
LDO HS LDO LS

An LDO is implemented to trim **VEE_HS_A** and **VEE_LS_A** during testing to fine tune the necessary negative gate voltage. If a higher negative value is needed, **DCDC_HS** and **DCDC_LS** must be replaced with another variant and bypassing the LDOs.

Feedback voltage divider adjusted to -2V, providing
 $V_{GS} = +18 \text{ V} / -2 \text{ V}$
 $VEE = -1.186 \cdot (1 + R1/R2)$
 $R1 + R2 \approx 100 \text{ k}\Omega$

DCDC_HS, **DCDC_LS**

[U_HS](#), [U_LS](#)



► V_{GS} values

The values chosen for V_{GS} are +18 V / -2 V. Even though Leapers recommends using +18 V, shoot-through could be a potential issue causing accidental turn-on of the low side devices because of a voltage spike greater than the minimum $V_{GS(th)}$. A gate driver with Miller clamp is used to mitigate this effect, but using 0 V for turn-off leaves only 2.8 V margin. From other inverter designs and analysis, 3 V can be expected to appear in the low side gates, so a 2 V margin is sufficient. The total margin is then a 4.8 V voltage spike without considering the Miller clamp circuit.

Minimum gate driver current and power:
 $I_{GD(min)} = f_{sw} \cdot Q_G = 50 \text{ kHz} \cdot 520 \text{ nC} = 26 \text{ mA}$
 $P_{min} = \Delta V_{GS} \cdot I_{GD(min)} = 20 \text{ V} \cdot 26 \text{ mA} = 0.52 \text{ W} \rightarrow 2 \text{ W}$

RG_ON_HS, **RG_OFF_HS**
RG_ON_LS, **RG_OFF_LS**

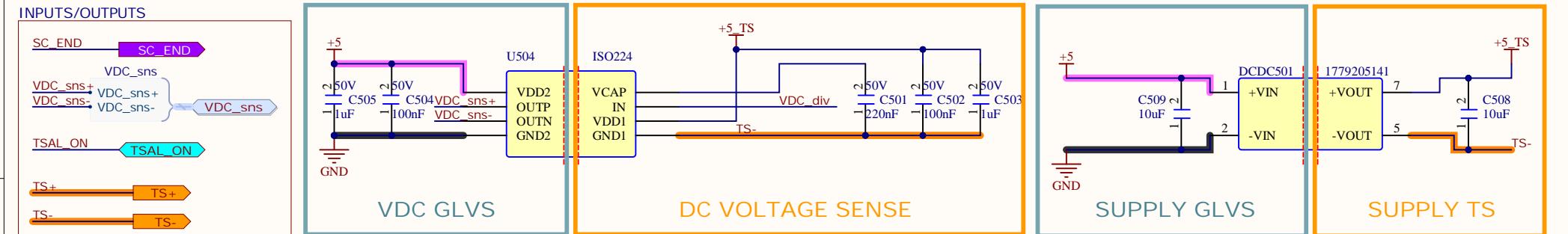
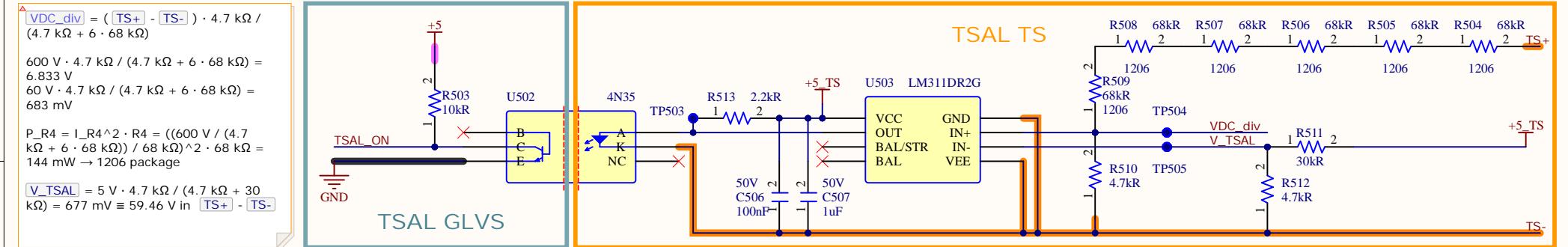
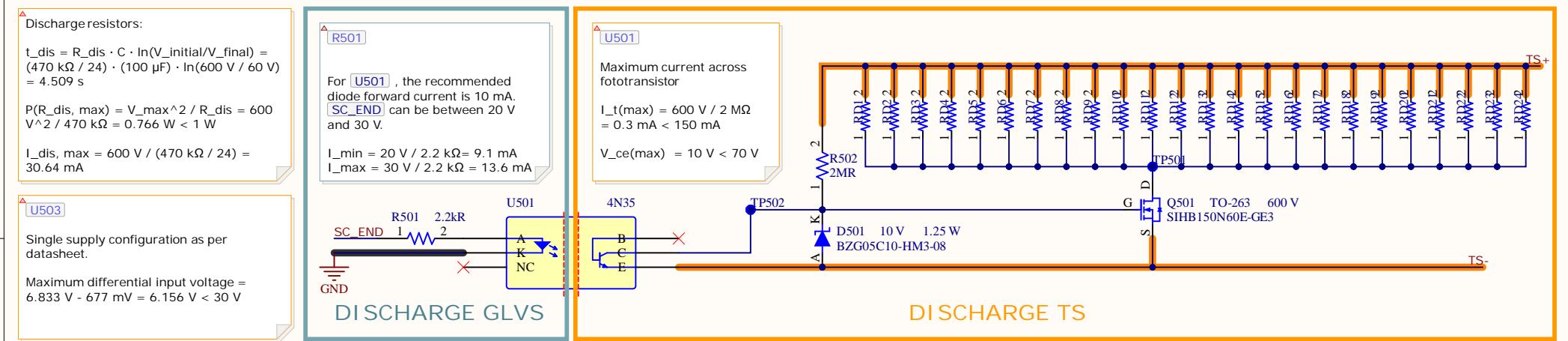
Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS CGS_LS CGD_HS CGD_LS
Csn_HS Csn_LS Rsp_HS Rsp_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt . Implementing them could result in further issues with the power limit for [DCDC_HS](#) and [DCDC_LS](#), as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$\text{CGS}_{\text{max}} = 2 \cdot P_{\text{DCDC}} / (\Delta V_{\text{GS}}^2 \cdot f_{\text{sw}}) \\ = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 50 \text{ kHz}) = 200 \text{ nF}$$

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Inverter_Power	
Size: -	Page Contents: [4] Half_Bridge.SchDoc	Version: 1.0	Department: Powertrain
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Checked by:		Date: 13/02/2024	



$(TS+ - TS-) > 60V \rightarrow TSAL_ON = 0V$
 $(TS+ - TS-) < 60V \rightarrow TSAL_ON = 5V$

$$\begin{aligned}
 & (\text{VDC_sns+} - \text{VDC_sns-}) = 1/3 \cdot \\
 & \quad [\text{VDC_div}] = 1/3 \cdot ((\text{TS+} - \text{TS-})) \\
 & 4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega)) = 1/3 \cdot \\
 & 0.011388 \cdot (\text{TS+} - \text{TS-}) \\
 \\
 & (\text{VDC_sns+} - \text{VDC_sns-}) = 1/3 \cdot \\
 & 0.011388 \cdot 600 \text{ V} = 2.278 \text{ V}
 \end{aligned}$$

U501, **U502**

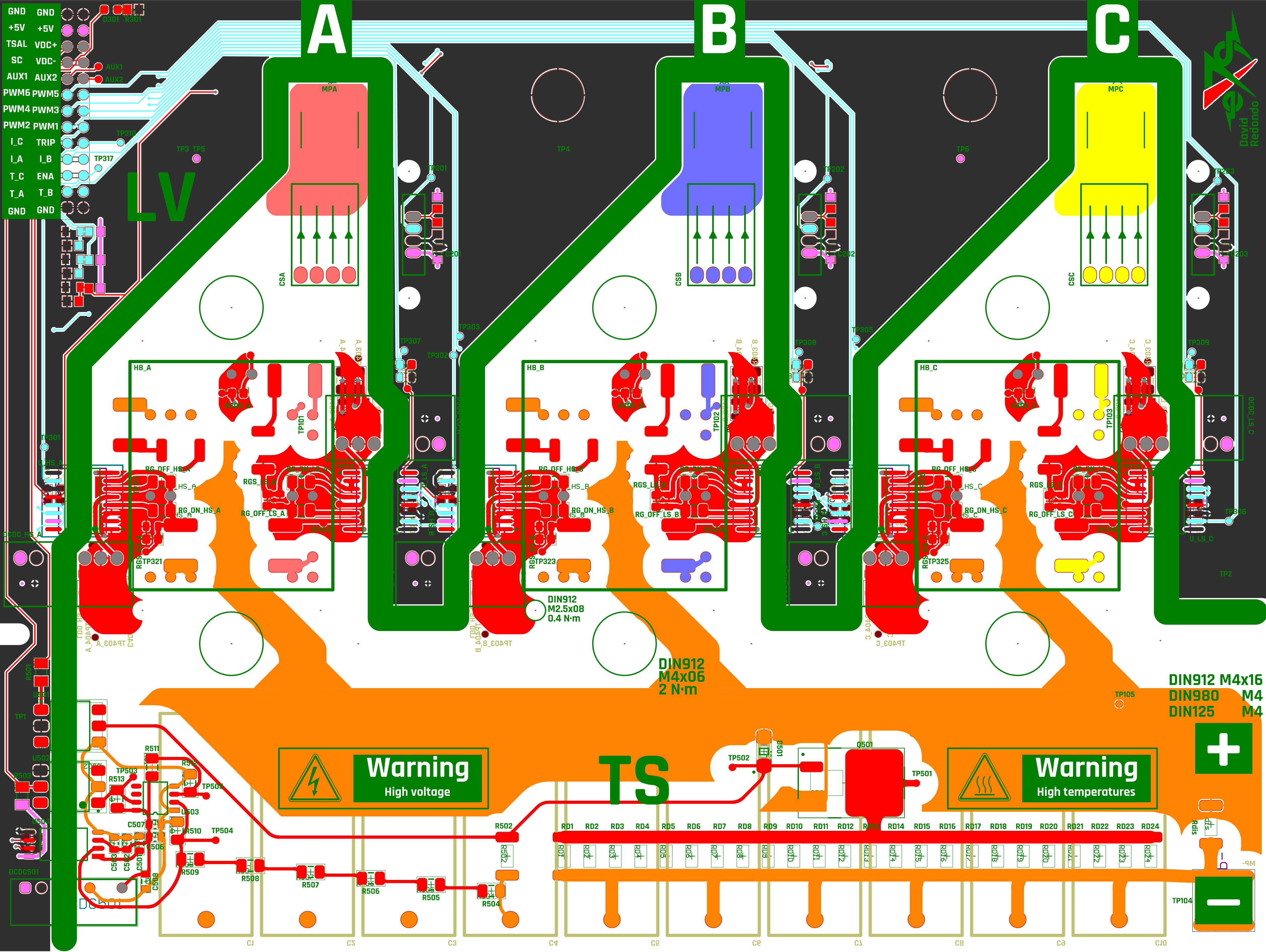
Isolation Voltage: AC For 1 Minute,
R.H. = 40 ~ 60% Viso = 5000 Vrms

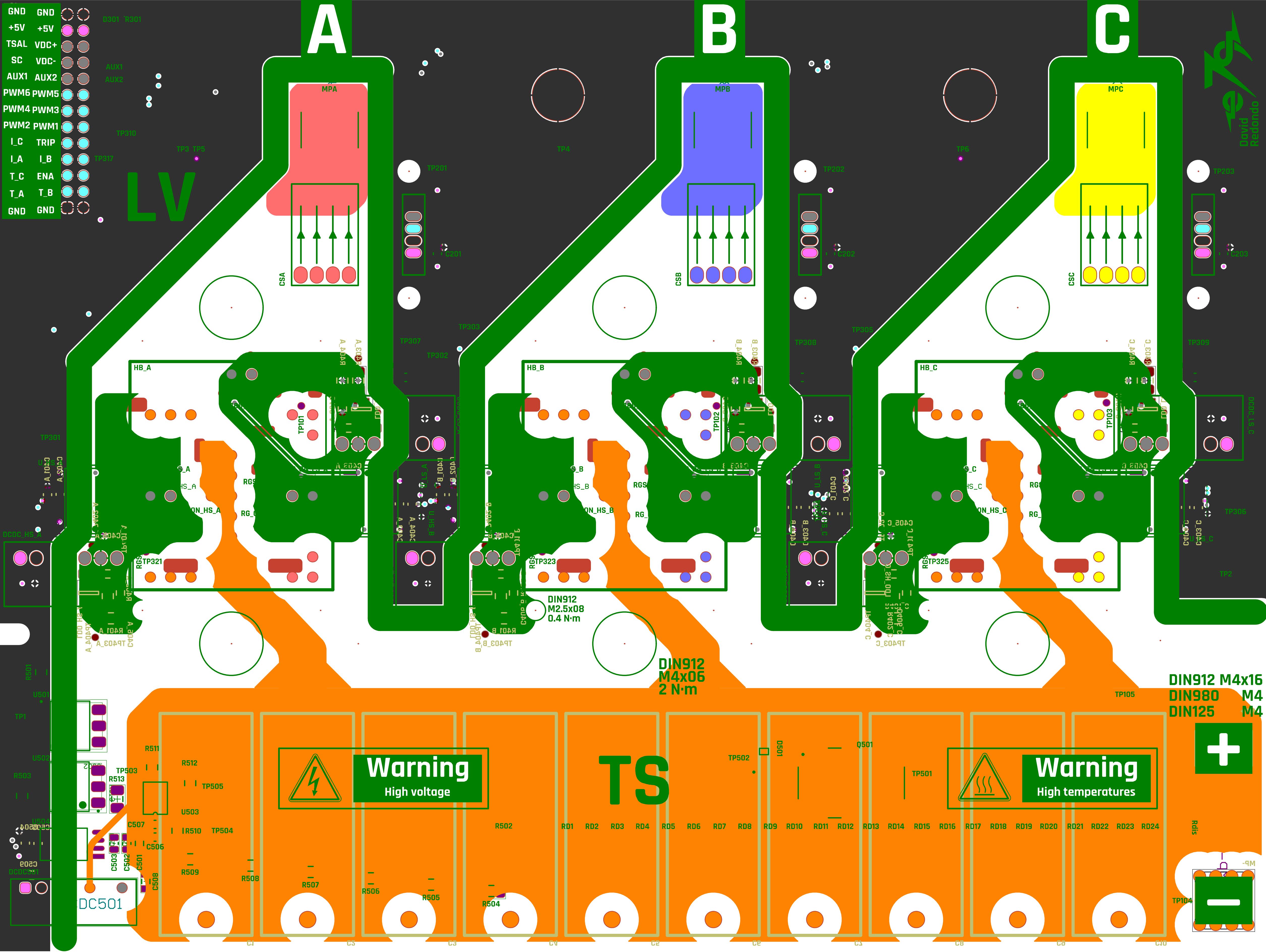
U504

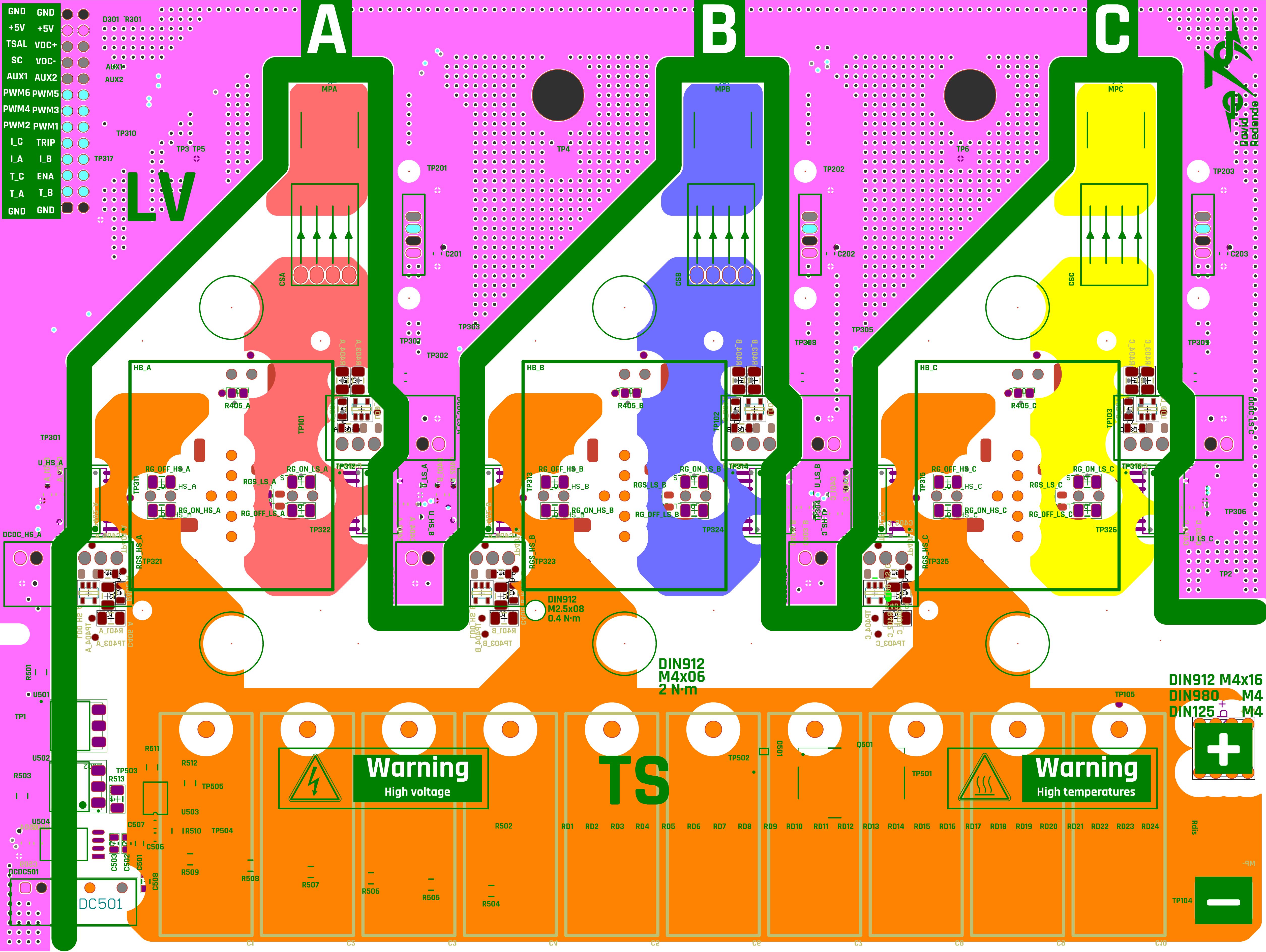
Maximum transient isolation voltage:
VTEST = VIOTM, t = 60 s (qualification
test) VIOTM = 7071 Vpk

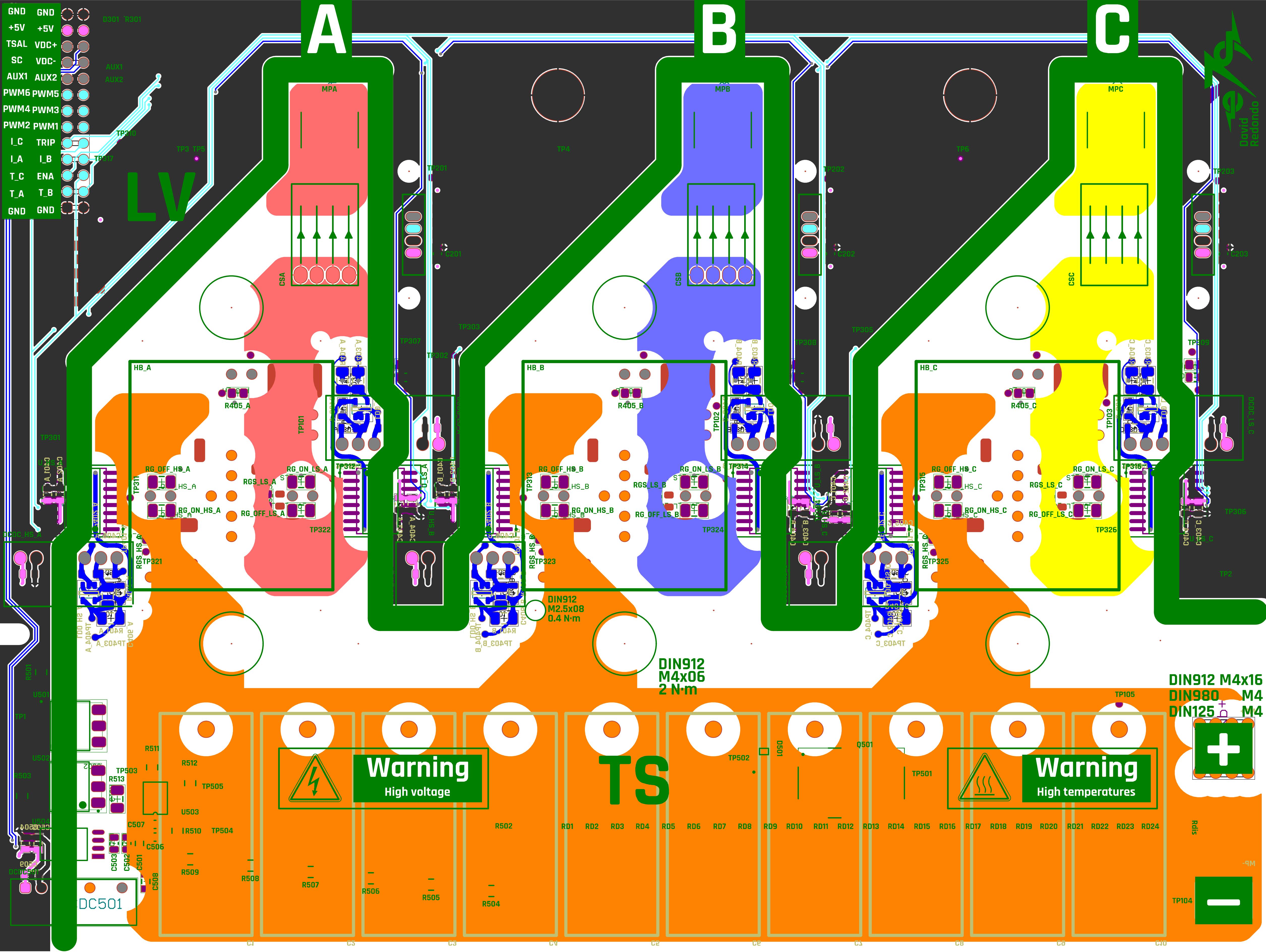
DCDC501

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Inverter_Power	
Size:	Page Contents: - [5] DC.SchDoc	Version:	1.0
		Department:	Powertrain
Author:	David Redondo	dredondovinolo@gmail.com	Sheet * of *
Checked by:	-	Date:	13/02/2024

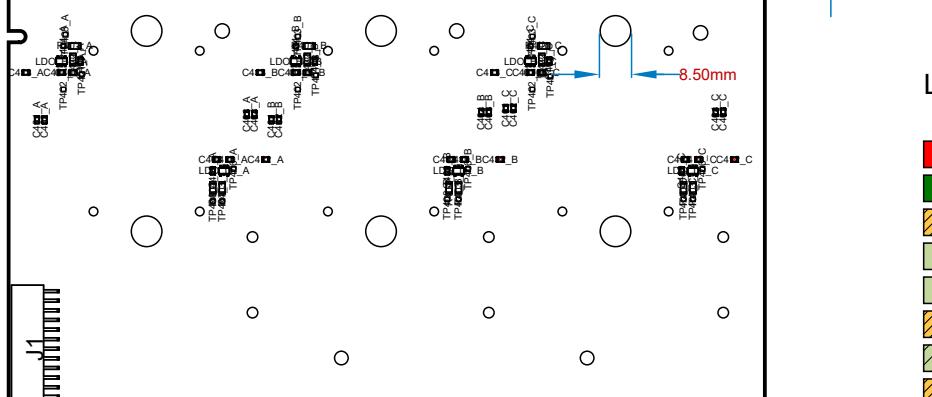
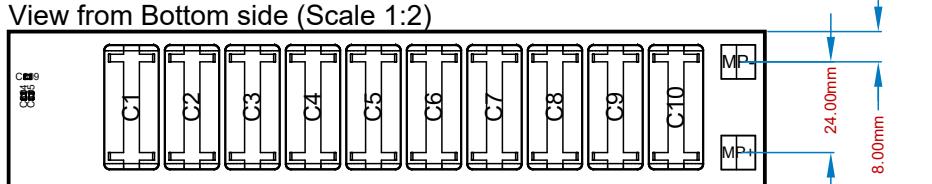
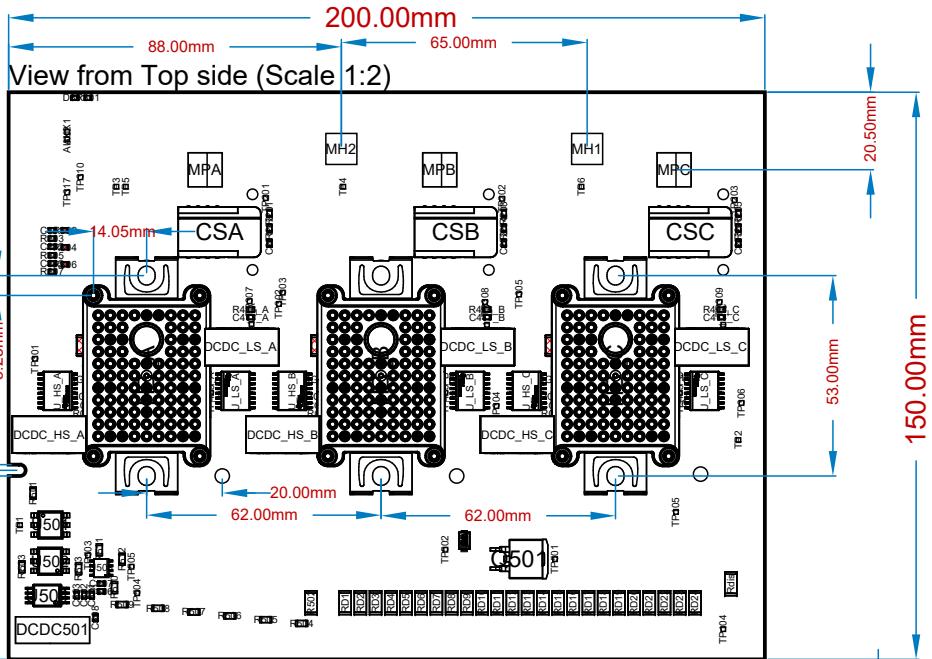








Inverter Power



Bill Of Materials

Designator	Name	Quantity
C405_A, C405_B, C405_C, C406_A, C406_B, C406_C, C408_A, C408_B, C408_C, C409_A, C409_B, C409_C, C508, C509	10uF	14
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	10uF 850V	10
DCDC501	1779205141	1
J1	613026243121	1
R503	CRCW120610K0FKEA	1
R511	CRCW120630K0FKEA	1
HB_A, HB_B, HB_C	DFS05HF12EYR1	3
MP_-, MP+, MPA, MPB, MPC	M4	5
MH1, MH2	Mounting Hole M4	2
RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24	RCV2512470KFKEG	24
R406_A, R406_B, R406_C	CR0805-FX-1000ELF	3
R301	CR0805-JW-102ELF	1
R405_A, R405_B, R405_C, RGS_HS_A, RGS_HS_B, RGS_HS_C, RGS_LS_A, RGS_LS_B, RGS_LS_C	CR0805-JW-103ELF	9
R504, R505, R506, R507, R508, R509	CR1206FX-6802EAS	6
R501, R513	CR1206-FX-4701ELF	2
R510, R512	CRS1206-FX-4701ELF	2
CSA, CSB, CSC	LEM CKSR 50-NP	3
DCDC_HS_A, DCDC_HS_B, DCDC_HS_C, DCDC_HS_D, DCDC_LS_A, DCDC_LS_B, DCDC_LS_C	MJG6-series	6
U503	LM311DR2G	1
R401_A, R401_B, R401_C, R402_A, R402_B, R402_C, R403_A, R403_B, R403_C, R404_A, R404_B, R404_C	CRCW120610K0FKEA	12
C501	885012208058	1
RG_OFF_HS_A, RG_OFF_HS_B, RG_OFF_HS_C, RG_OFF_LS_A, RG_OFF_LS_B, RG_OFF_LS_C, RG_ON_HS_A, RG_ON_HS_B, RG_ON_HS_C, RG_ON_LS_A, RG_ON_LS_B, RG_ON_LS_C	CRG1206F100R	12
U504	ISO224	1
LDO_HS_A, LDO_HS_B, LDO_HS_C, LDO_HS_D, LDO_LS_A, LDO_LS_B, LDO_LS_C	TPS72301	6
U_HS_A, U_HS_B, U_HS_C, U_HS_D, U_LS_A, U_LS_B, U_LS_C	UCC21710	6
Q501	SIHB150N60E-GE3	1
R502, Rds	R2M-2512FTK	2
U501, U502	4N35	2
D501	BZG05C10	1
D301	150080GS75000	1
C201, C202, C203, C402_A, C402_B, C402_C, C404_A, C404_B, C404_C, C411_A, C411_B, C411_C, C502, C504, C506	885012207098	15
C401_A, C401_B, C401_C, C403_A, C403_B, C403_C, C503, C505, C507	885012207103	9

Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay				Legend GTO
	Surface Material	0.01mm	Solder Resist		Solder Mask GTS
CF-004	TOP	0.07mm		Signal GTL	
	Prepreg	0.10mm	PP-006		Dielectric
	Prepreg	0.10mm	PP-006		Dielectric
Copper	GND	0.07mm		Signal G1	
	FR-4	0.90mm			Dielectric
Copper	PWR	0.07mm		Signal G2	
	Prepreg	0.10mm	PP-006		Dielectric
	Prepreg	0.10mm	PP-006		Dielectric
CF-004	BOT	0.07mm		Signal GBL	
	Surface Material	0.01mm	Solder Resist		Solder Mask GBS
	Bottom Overlay				Legend GBO

Total thickness: 1.60mm