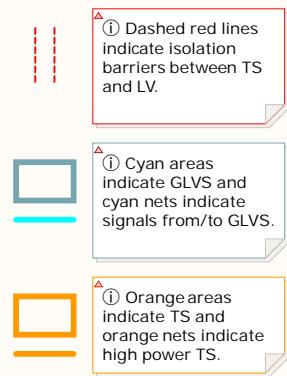


A



Specifications:

$f_{sw} = 40 \text{ kHz}$
 $V_{in, max} = 600 \text{ VDC}$
 $V_{out, max} = 245 \text{ V,RMS,ph-n (SVPWM)}$
 $I_{out, max} = 80 \text{ A,RMS}$
 $I_{out, cont} = 32 \text{ A,RMS}$
 $P_{out, max} = 53 \text{ kW}$
 $P_{out, cont} = 23.5 \text{ kW}$
 Liquid cooled with water at 50°C max

Changelog:

Version 1.0: (sent to production 15-02-2024)
 - Base version

Version 1.1: (sent to production 28-03-2024)
 - Added 5V supply protections
 - Swapped pins 4 and 5 in gate drivers' LDOs
 - Swapped MP+ and MP-, and their silkscreen
 - Added testpoints for current sensors' reference
 - Added testpoints for VDC_{sns+} and VDC_{sns-}
 - Renamed testpoints in [3]
 - Added various silkscreen texts and indications
 - Added layer physical logo

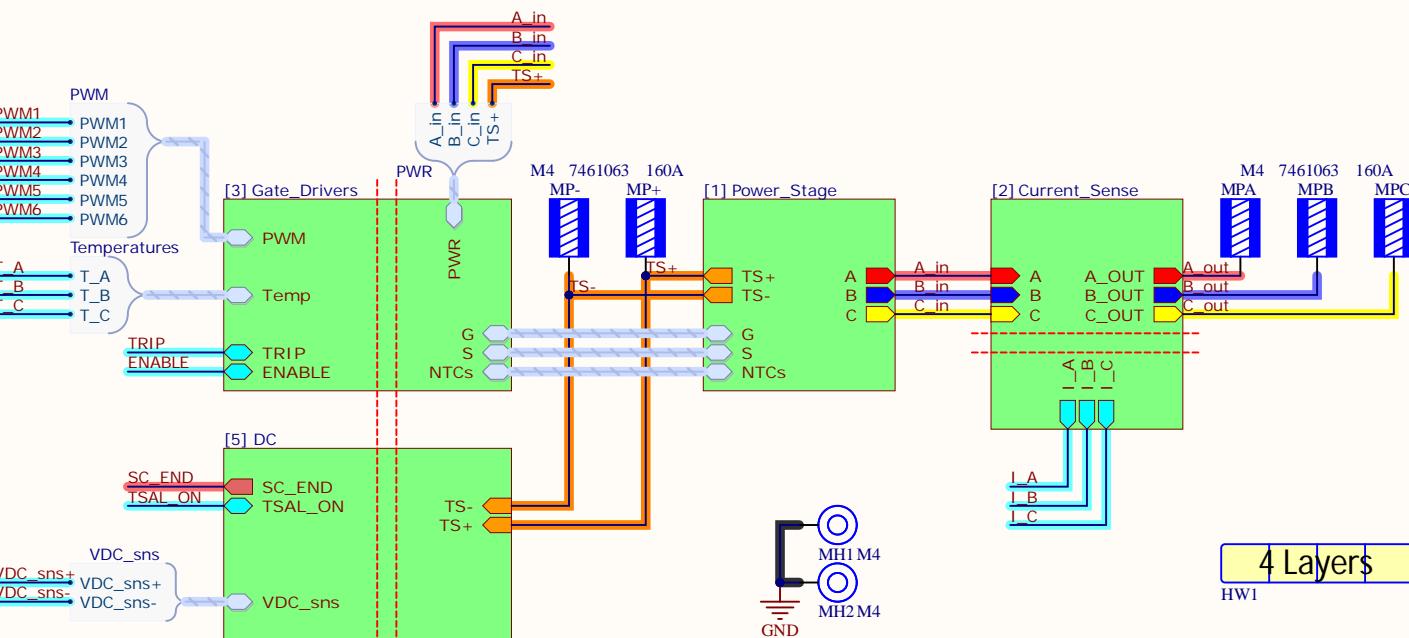
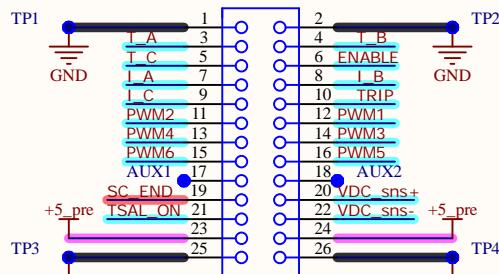
Changes in SCH but not in PCB:

19-04-2024: Added decoupling capacitors to

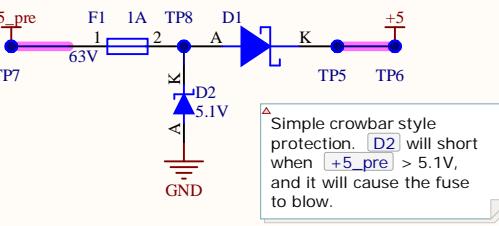
Known issues:

- [D1] is not correctly rated. Replace with appropriate PMOS or beefier Schottky (beware the voltage drop)
- [Rdis] does practically nothing compared to [R504] ... [R510] and could be eliminated.
- [R301] can be of lower value.
- Most DNP caps are actually needed.
- [D501] failed once, but cause remains unknown.
- [R501] should have a bigger value.
- [R511] and [R512] should have a small tolerance, and it should be specified in the schematic.
- 10uF 50V 0805 caps are expensive and should be replaced with 10uF 50V 1206 or 10uF 50V 1210.

LV Connector

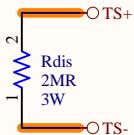


OCP, OVP, reverse

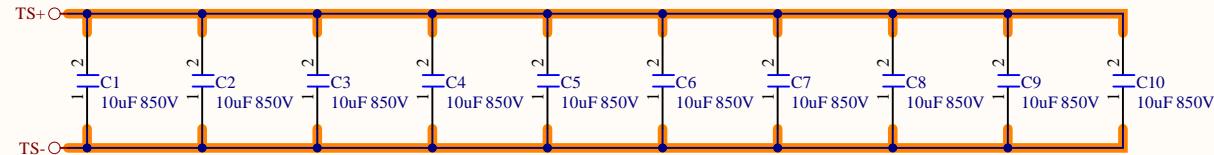


Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Wolfspeed	
Size:	Page Contents: Inverter_Power.SchDoc	Version: 1.1	
		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 1 of 5
Checked by:		Date: 20/05/2024	

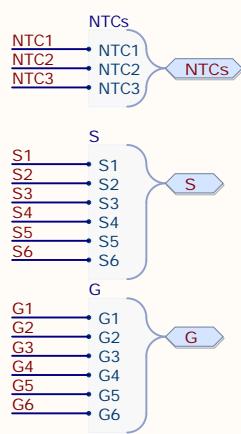
Passive discharge



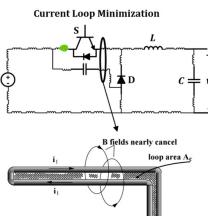
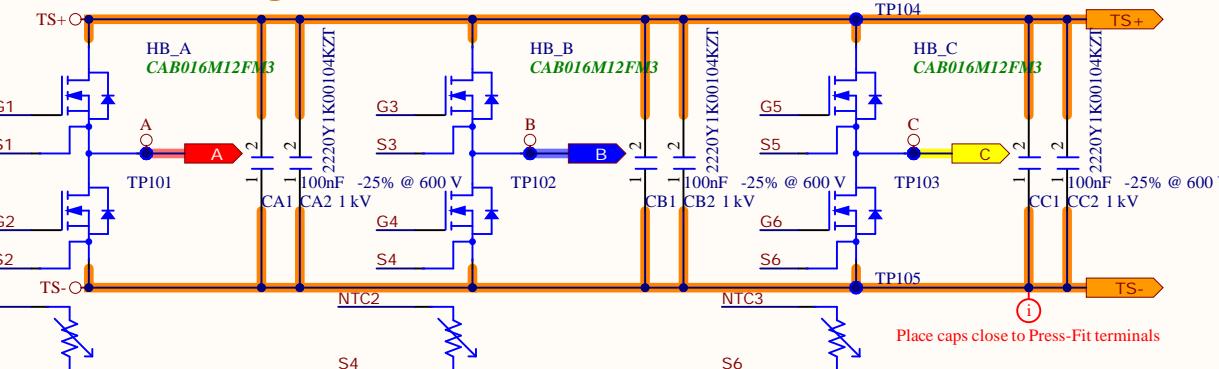
DC Bus capacitors, 100uF, Murata FHA85Y106KS



INPUTS/OUTPUTS



SiC Half-Bridges



Current Loop Minimization
Current loop between top and bottom MOSFETs will cause excessive overshoot due to parasitic inductance and low parasitic capacitance. Increasing capacitance to hundreds of nF mitigates the effect. The capacitors essentially work as a switching decoupling. MLCCs with low DC bias or film, but MLCCs are way more compact. Place as close as possible to semiconductor terminals.

Overshoot analysis can be performed using a linear model proportional to DC bus voltage and output current. Easiest way to do it is using only one half bridge as a synchronous buck and varying input voltage with a fixed duty cycle and a R or RL load.

Linear Model and Data Points

No C leads to 1430 Vp at max. specs.

C brings it down to 720 Vp at max. specs.

DC Link design considerations:

$$V_{\text{C}} > 1.1 \cdot V_{\text{max}} = 1.1 \cdot 600 \text{ V} = 660 \text{ V} \rightarrow 850 \text{ V}$$

$$I_{\text{C,RMS}} \approx 0.65 \cdot I_{\text{phase,RMS}} = 0.65 \cdot 80 \text{ A,RMS} = 52 \text{ A,RMS} \rightarrow 10 \times 5 \text{ A,RMS}$$

$$C > I_{\text{C,RMS}} / (V_{\text{ripple}} \cdot f_{\text{sw}}) = 52 \text{ A,RMS} / (15 \text{ V} \cdot 40 \text{ kHz}) \approx 87 \mu\text{F} \rightarrow 10 \times 10 \mu\text{F}$$

Check:
<https://www.specterengineering.com/blog/2019/9/7/dc-link-capacitor-selection-for-y>

Semiconductor details:

$$V_{\text{DSS}}(\text{breakdown}) = 1200 \text{ V} // 1200 \text{ V}$$

$$R_{\text{on}} = 5.5 .. 13 \text{ m}\Omega // 16.0 .. 28.8 \text{ m}\Omega$$

$$V_{\text{f,D}} = 3.3 .. 4.9 \text{ V} // 4.9 .. 5.5 \text{ V}$$

$$T_{\text{rr}} = 41.5 .. 45 \text{ ns} // 20.0 \text{ ns}$$

$$Q_{\text{rr}} = 2.19 .. 3.94 \mu\text{C} // 1.30 \mu\text{C}$$

$$R_{\text{th,jc}} = 0.12 .. 0.15 \text{ K/W} // 0.543 \text{ K/W}$$

$$Q_{\text{G}} = 520 \text{ nC} // 236 \text{ nC}$$

$$C_{\text{in}} = 14.5 \text{ nF} // 6.6 \text{ nF}$$

$$R_{\text{G(int)}} = 1.9 \Omega // 2.4 \Omega$$

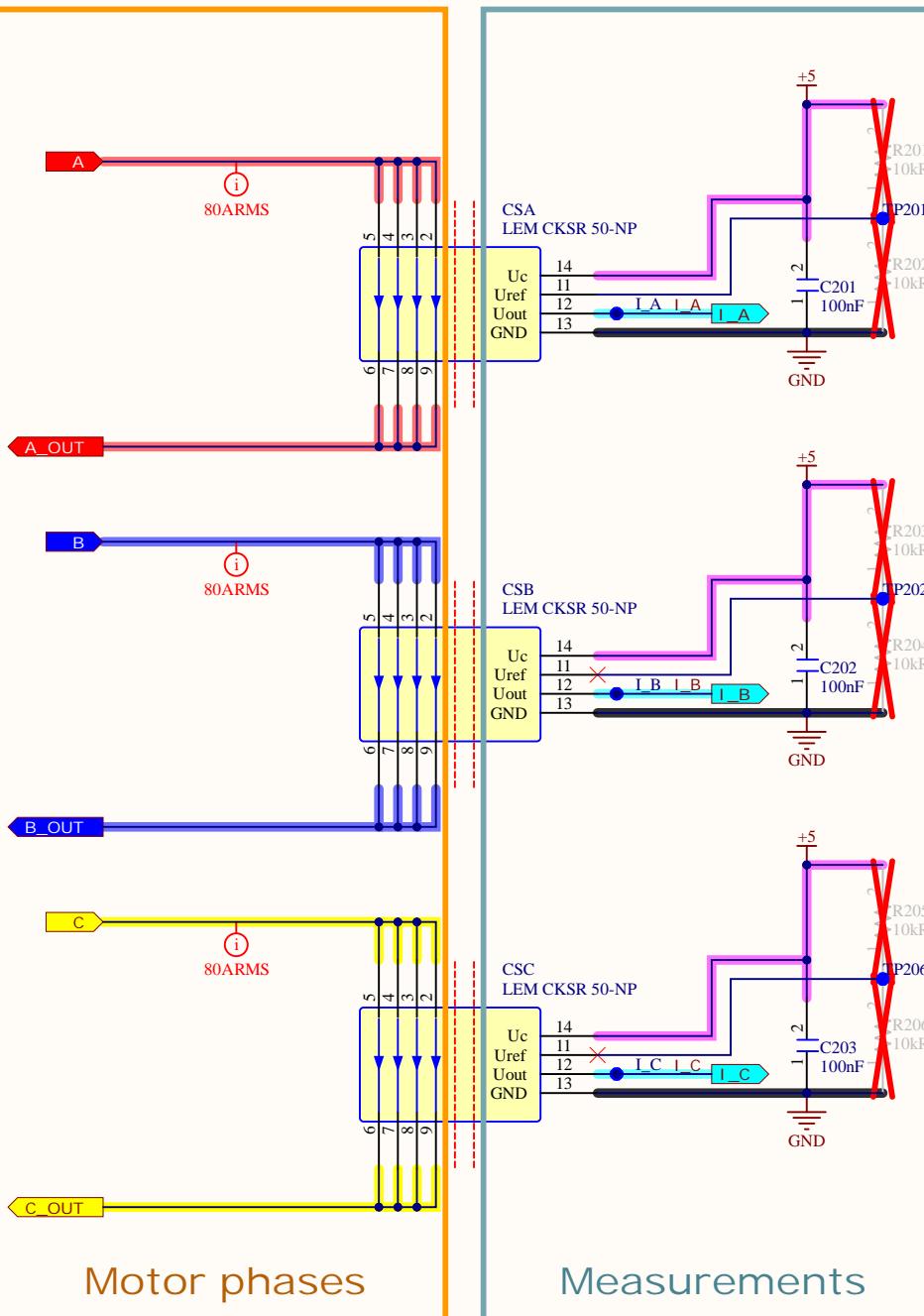
$$V_{\text{GS(th)}} = 2.8 .. 4.8 \text{ V} // 1.8 .. 3.6 \text{ V}$$

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant: Wolfspeed	
Size:	Page Contents:	Version: 1.1	
-	[1]Power_Stages.SchDoc	Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 2 of 5
Checked by:		Date: 20/05/2024	

A

CSA , CSB , CSC

CKSR 50-NP/SP1 configured with Number of primary turns = 1 (R_phase-connector = 0.18 mΩ)



B

CSA , CSB , CSC

CKSR 50-NP/SP1 2.5V internal reference is used in order to have equal measuring range for positive and negative values. Voltage divider implemented just in case.

I_A , I_B , I_C

$$U_{\text{meas}} = (12.5 \text{mV/A} \cdot I_{\text{meas}} + U_{\text{ref}})$$

For ±150Apk:
 $V_{\text{meas_pk+}} = 4.375 \text{V}$
 $V_{\text{meas_pk-}} = 0.625 \text{V}$

C201 , C202 , C203

The fluxgate oscillator draws current pulses of up to 30 mA at a rate of ca. 900 kHz. In the case of a power supply with high impedance, it is advised to provide local decoupling (100 nF or more, located close to the transducer).

C

CSA , CSB , CSC

AC insulation test
RMS voltage, 50 Hz,
1 min:

$$U_d = 4.3 \text{kV} > 3 \cdot V_{\text{max}} = 1.8 \text{kV}$$

D

Company:	e-Tech Racing	e-techracing.es	
Project:	Inverter Power	Variant:	Wolfspeed
Size:	Page Contents:	Version:	1.1
-	[2]Current_Sense.SchDoc	Department:	Powertrain
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 3 of 5
Checked by:	_	Date:	20/05/2024

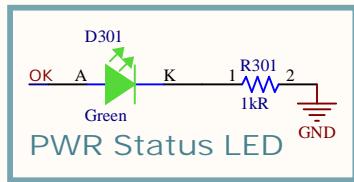
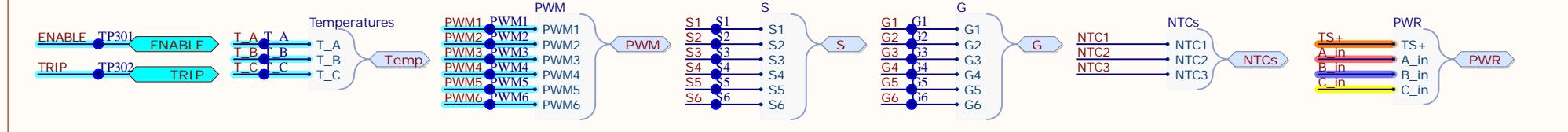
1

2

3

4

INPUTS/OUTPUTS



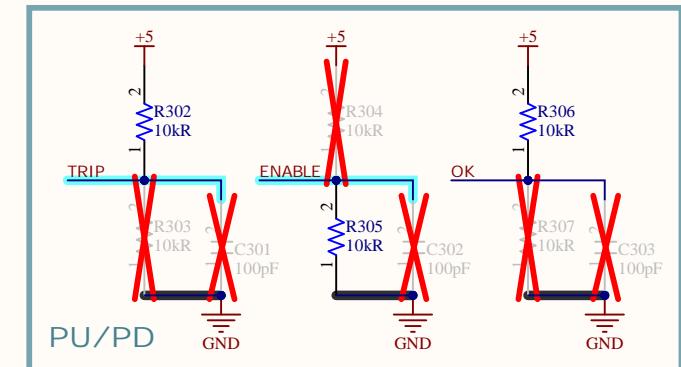
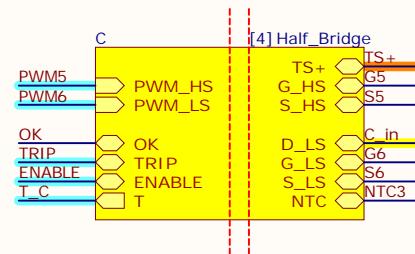
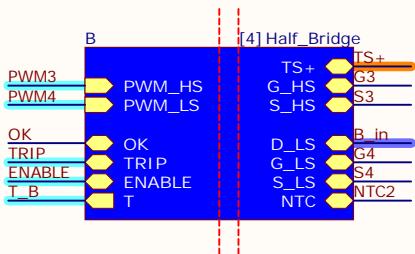
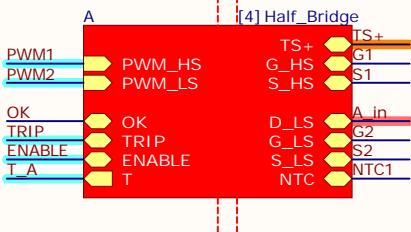
[T_A, T_B, T_C]
Look-up table obtained with MATLAB script which can be found in the simulations folder.
For different temperatures:
 $V_{meas}(0^\circ\text{C}) = 0.246\text{V}$
 $V_{meas}(25^\circ\text{C}) = 2\text{V}$
 $V_{meas}(50^\circ\text{C}) = 2.578\text{V}$
 $V_{meas}(90^\circ\text{C}) = 2.864\text{V}$

B

B

C

C



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Project:	Inverter Power	Variant: Wolfspeed	
Size:	Page Contents: [3]Gate_Drivers.SchDoc	Version: 1.1	
		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 4 of 5
Checked by:			Date: 20/05/2024

1

2

3

4

A

U_HS, U_LS

- TRIP and OK signals are in open drain configuration, so they can be paralleled.
- IN- is not used and tied to GND.
- ENABLE to be given by MCU in active-high mode. When set to low for more than 1 μ s, TRIP is reset.
- Temperature sensing using low-side drivers. Ain outputs a current of 200 μ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. [R405], [R406] and [C411] from SPICE simulation.
- Miller clamp protection is used.
- RGS_HS, RGS_LS: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
- Overcurrent detection is not implemented.

LDO_HS, LDO_LS

An LDO is implemented to trim VEE_HS_A and VEE_LS_A during testing to fine tune the necessary negative gate voltage. Feedback voltage divider adjusted with a Python script which can be found in the simulations folder.

$$\text{VEE} = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers $\rightarrow R1 = 36 \text{ k}\Omega$, $R2 = 56 \text{ k}\Omega$

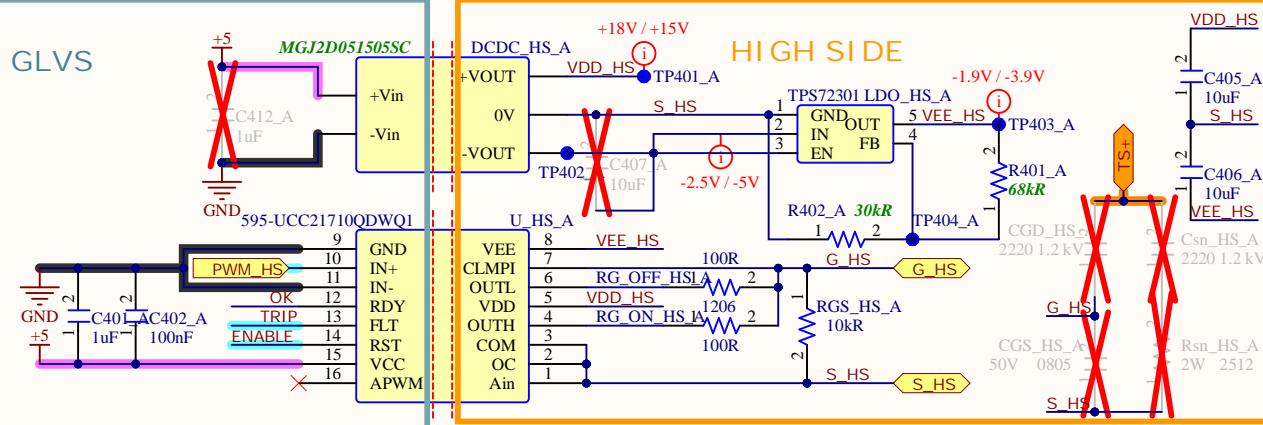
Wolfspeed $\rightarrow R1 = 68 \text{ k}\Omega$, $R2 = 30 \text{ k}\Omega$

DCDC_HS, DCDC_LS

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS

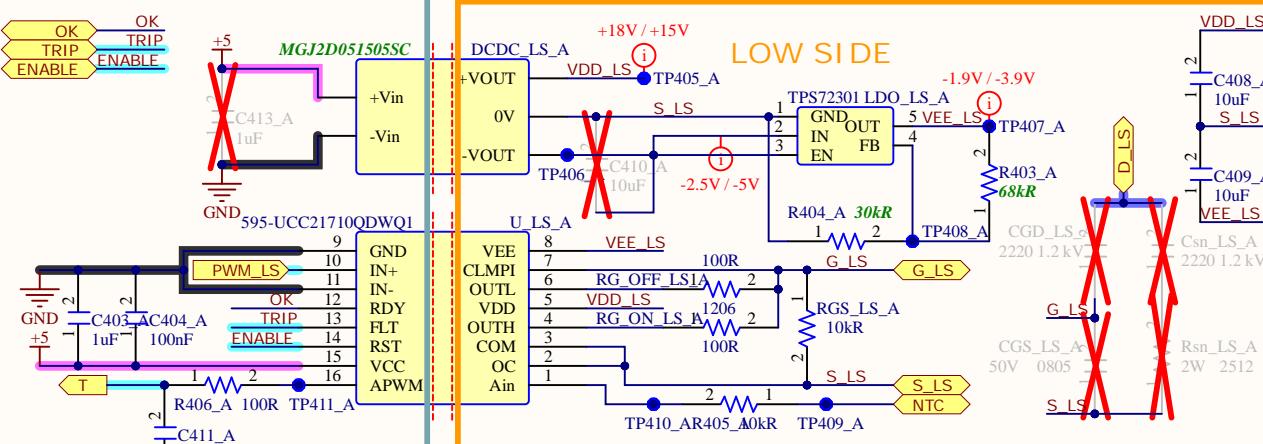
VIOTM ($t = 60$ s (qualification test)): 8000 VPK

GLVS**HIGH SIDE****V_GS values:**

The values can be modified by replacing DCDC_HS and DCDC_LS with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

Minimum gate driver current and power:
 $I_{GD(\min)} = f_{sw} \cdot O_G = 40 \text{ kHz} \cdot 520 \text{ nC} = 20.8 \text{ mA}$

$$P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 20.8 \text{ mA} = 0.416 \text{ W} \rightarrow 2 \text{ W}$$

OK, TRIP, ENABLE**LOW SIDE****RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS**

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS, CGS_LS, CGD_HS, CGD_LS, Csn_HS, Csn_LS, Rsn_HS, Rsn_LS

DNP, but they could be useful with EMI related issues to decrease dV/dt. Implementing them could help in other issues with the power limit for DCDC_HS and DCDC_LS, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 40 \text{ kHz}) = 250 \text{ nF}$$

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Project: Inverter Power

Variant: Wolfspeed

Size: Page Contents:
[4]Half_Bridge.SchDoc

Version: 1.1

Department: Powertrain

Author: David Redondo dredondovinolo@gmail.com

Sheet 5 of 5

Checked by: _

Date: 20/05/2024

A

▲ U_HS, U_LS

1. **TRIP** and **OK** signals are in open drain configuration, so they can be paralleled.
2. IN- is not used and tied to **GND**.
3. **ENABLE** to be given by MCU in active-high mode. When set to low for more than 1 μ s, **TRIP** is reset.
4. Temperature sensing using low-side drivers. Ain outputs a current of 200 μ A. PWM to analog using a RC filter, to be fed directly to MCU ADC. **[R405]**, **[R406]** and **[C411]** from SPICE simulation.
5. Miller clamp protection is used.
6. **RGS_HS**, **RGS_LS**: External gate pull-down is implemented even though the gate drivers implement an active pull-down.
7. Overcurrent detection is not implemented.

▲ LDO_HS, LDO_LS

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$$\text{VEE} = -1.186 \cdot (1 + R1/R2)$$

$$R1 + R2 \approx 100 \text{ k}\Omega$$

Leapers $\rightarrow R1 = 36 \text{ k}\Omega$, $R2 = 56 \text{ k}\Omega$

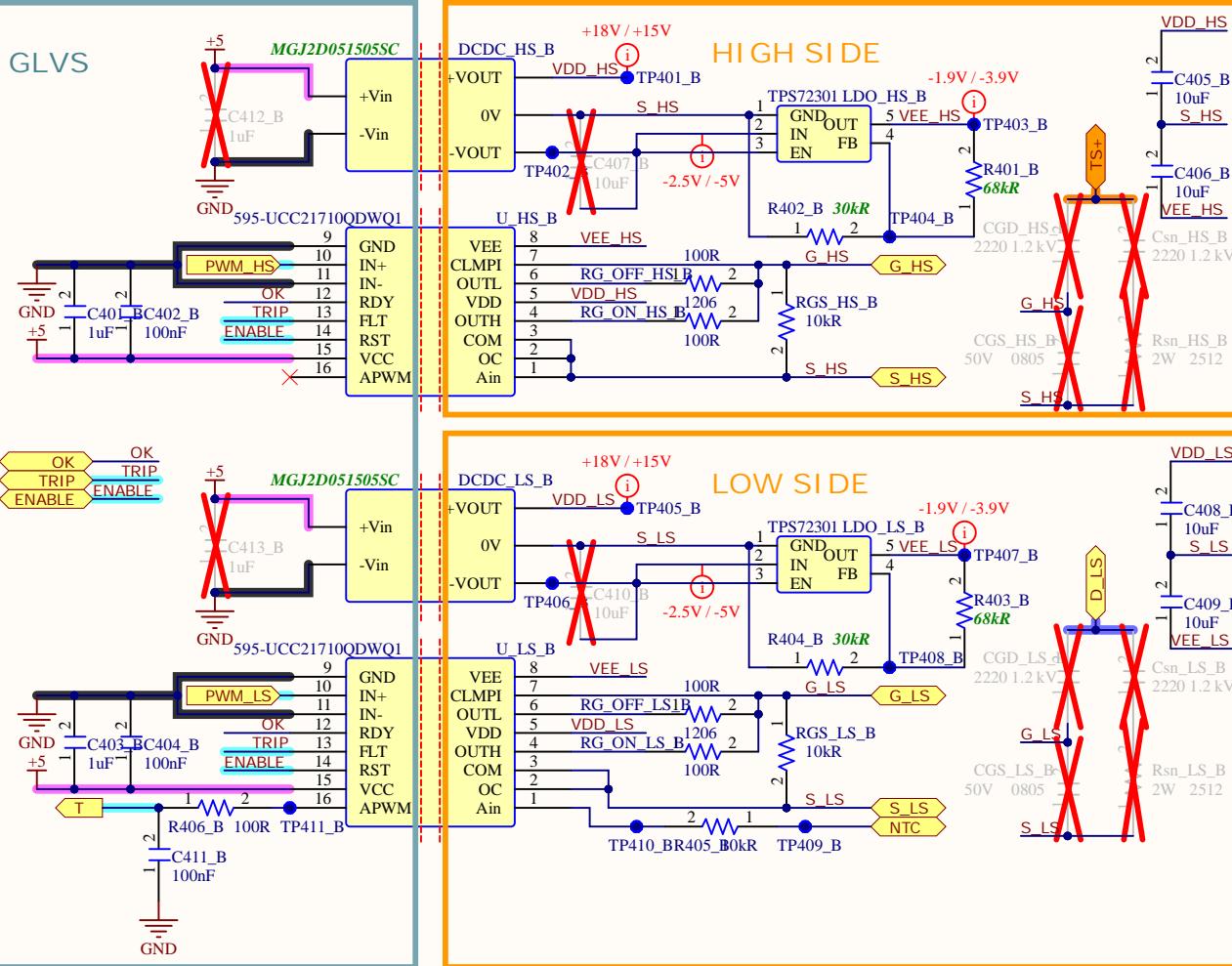
Wolfspeed $\rightarrow R1 = 68 \text{ k}\Omega$, $R2 = 30 \text{ k}\Omega$

▲ DCDC_HS, DCDC_LS

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

▲ U_HS, U_LS

VIOTM ($t = 60$ s (qualification test)): 8000 VPK

GLVS**▲ V_GS values:**

The values can be modified by replacing **DCDC_HS** and **DCDC_LS** with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

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▲ RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

CGS_HS, **CGS_LS**, **CGD_HS**, **CGD_LS**, **Csn_HS**, **Csn_LS**, **Rsn_HS**, **Rsn_LS**

DNP, but they could be useful with EMI related issues to decrease dV/dt . Implementing them could avoid issues with the power limit for **DCDC_HS** and **DCDC_LS**, as the gate charge would increase significantly. The maximum allowed capacitance would be:

$$CGS_{\max} = 2 \cdot P_{DCDC} / (\Delta V_{GS}^2 \cdot f_{sw}) = 2 \cdot 2 \text{ W} / ((20 \text{ V})^2 \cdot 40 \text{ kHz}) = 250 \text{ nF}$$

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Project: Inverter Power Variant: Wolfspeed

Size:	Page Contents: [4]Half_Bridge.SchDoc	Version: 1.1
-		Department: Powertrain

Author: David Redondo dredondovinolo@gmail.com

Sheet 5 of 5

Checked by: _

Date: 20/05/2024

A

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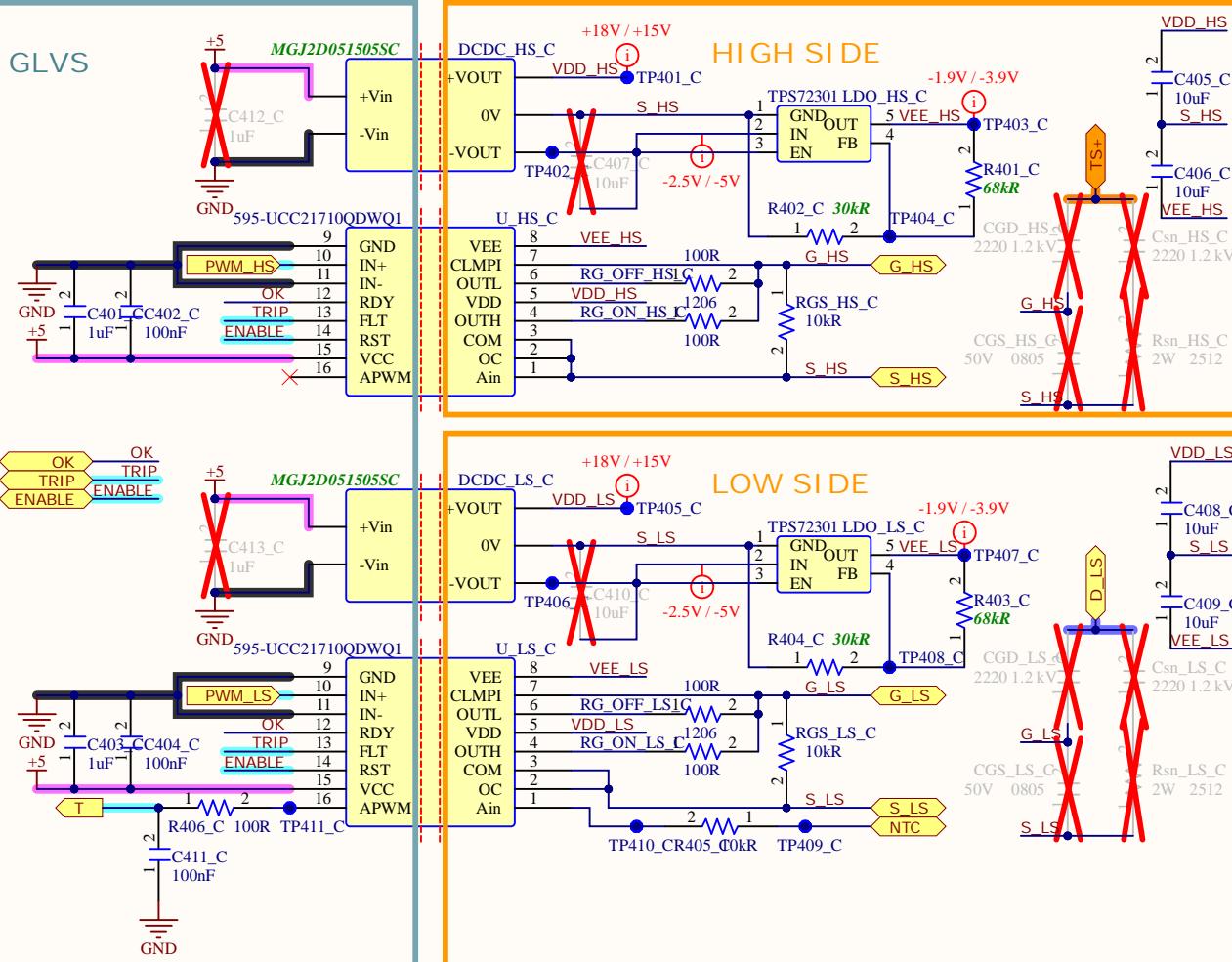
Wolfspeed $\rightarrow R1 = 68 \text{ k}\Omega$, $R2 = 30 \text{ k}\Omega$

DCDC_HS, DCDC_LS

Isolation test voltage (Qualification tested for 1 minute): 5200 VDC

U_HS, U_LS

VIOTM ($t = 60$ s (qualification test)): 8000 VPK

GLVS**V_GS values:**

The values can be modified by replacing **DCDC_HS** and **DCDC_LS** with one from the following list: MGJ2D051505SC, MGJ2D051509SC, MGJ2D051515SC, MGJ2D051802SC, MGJ2D052003SC, MGJ2D052005SC. LDO voltages must also be adjusted.

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 $P_{\min} = \Delta V_{GS} \cdot I_{GD(\min)} = 20 \text{ V} \cdot 20.8 \text{ mA} = 0.416 \text{ W} \rightarrow 2 \text{ W}$

RG_ON_HS, RG_OFF_HS, RG_ON_LS, RG_OFF_LS

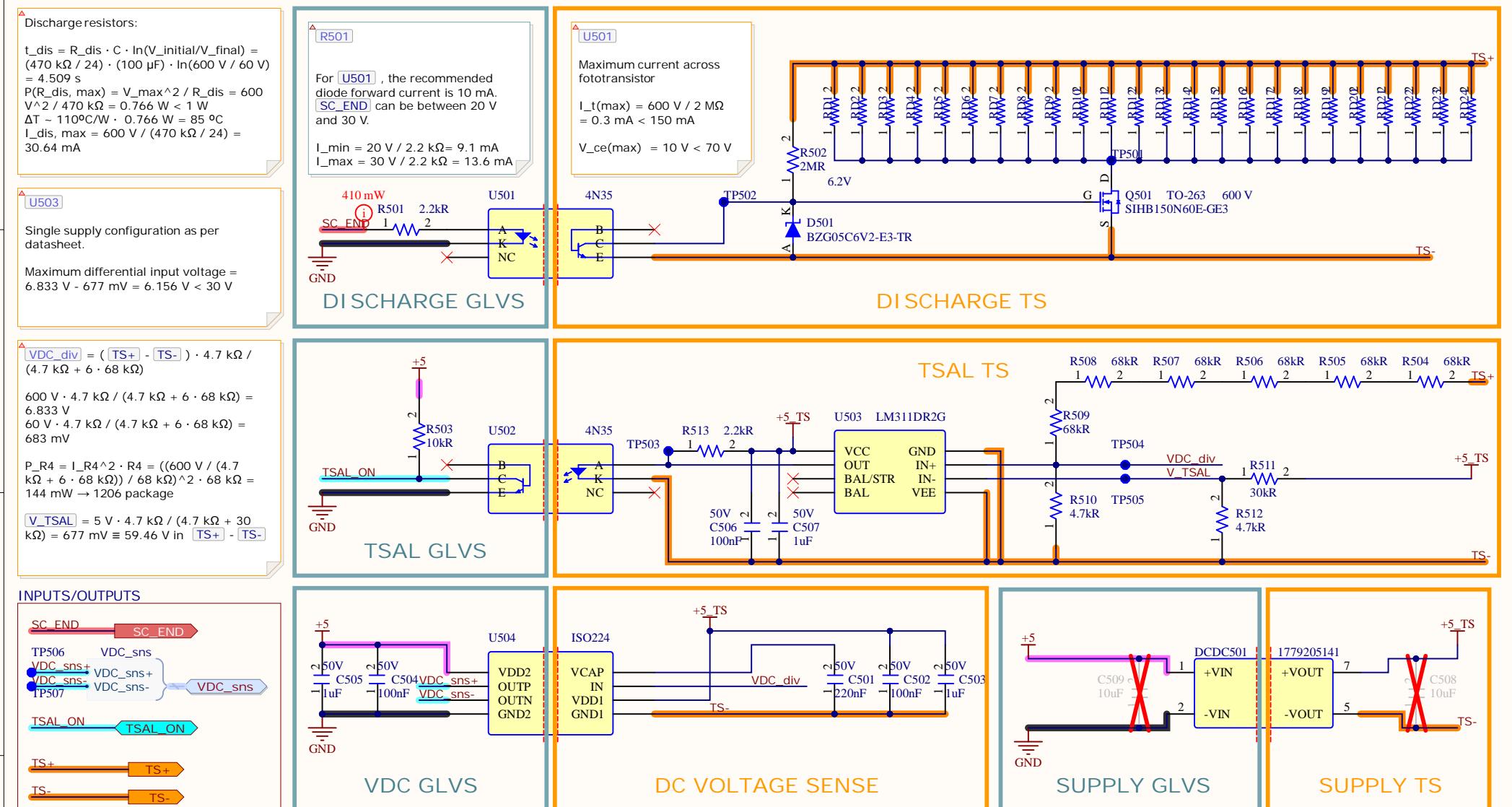
Essentially, a lower value for the gate resistors will reduce switching losses as the MOSFETs will switch faster and thus spend less time switching. Switching faster also means that the dV/dt will be higher, which can be responsible of EMI increase. The considered values of 3.3 Ω are recommended by the datasheet.

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Project:	Inverter Power	Variant: Wolfspeed	
Size:	Page Contents: [4]Half_Bridge.SchDoc	Version: 1.1	
		Department: Powertrain	
Author:	David Redondo	dredondovinolo@gmail.com	Sheet 5 of 5
Checked by:			Date: 20/05/2024



$(TS+ - TS-) > 60V \rightarrow TSAL_ON = 0V$
 $(TS+ - TS-) < 60V \rightarrow TSAL_ON = 5V$

$$\begin{aligned} & \Delta \quad \text{U504} \\ \\ & (\frac{\text{VDC_sns+}}{\text{VDC_div}} - \frac{\text{VDC_sns-}}{\text{VDC_div}}) = 1/3 \cdot \\ & 4.7 \text{ k}\Omega / (4.7 \text{ k}\Omega + 6 \cdot 68 \text{ k}\Omega) = 1/3 \cdot \\ & 0.011388 \cdot (\frac{\text{TS+}}{\text{TS-}} - \frac{\text{TS-}}{\text{TS+}}) \\ \\ & (\frac{\text{VDC_sns+}}{\text{VDC_div}} - \frac{\text{VDC_sns-}}{\text{VDC_div}}) = 1/3 \cdot \\ & 0.011388 \cdot 600 \text{ V} = 2.278 \text{ V} \end{aligned}$$

U501, **U502**

Isolation Voltage: AC For 1 Minute,
R.H. = 40 ~ 60% Viso = 5000 Vrms

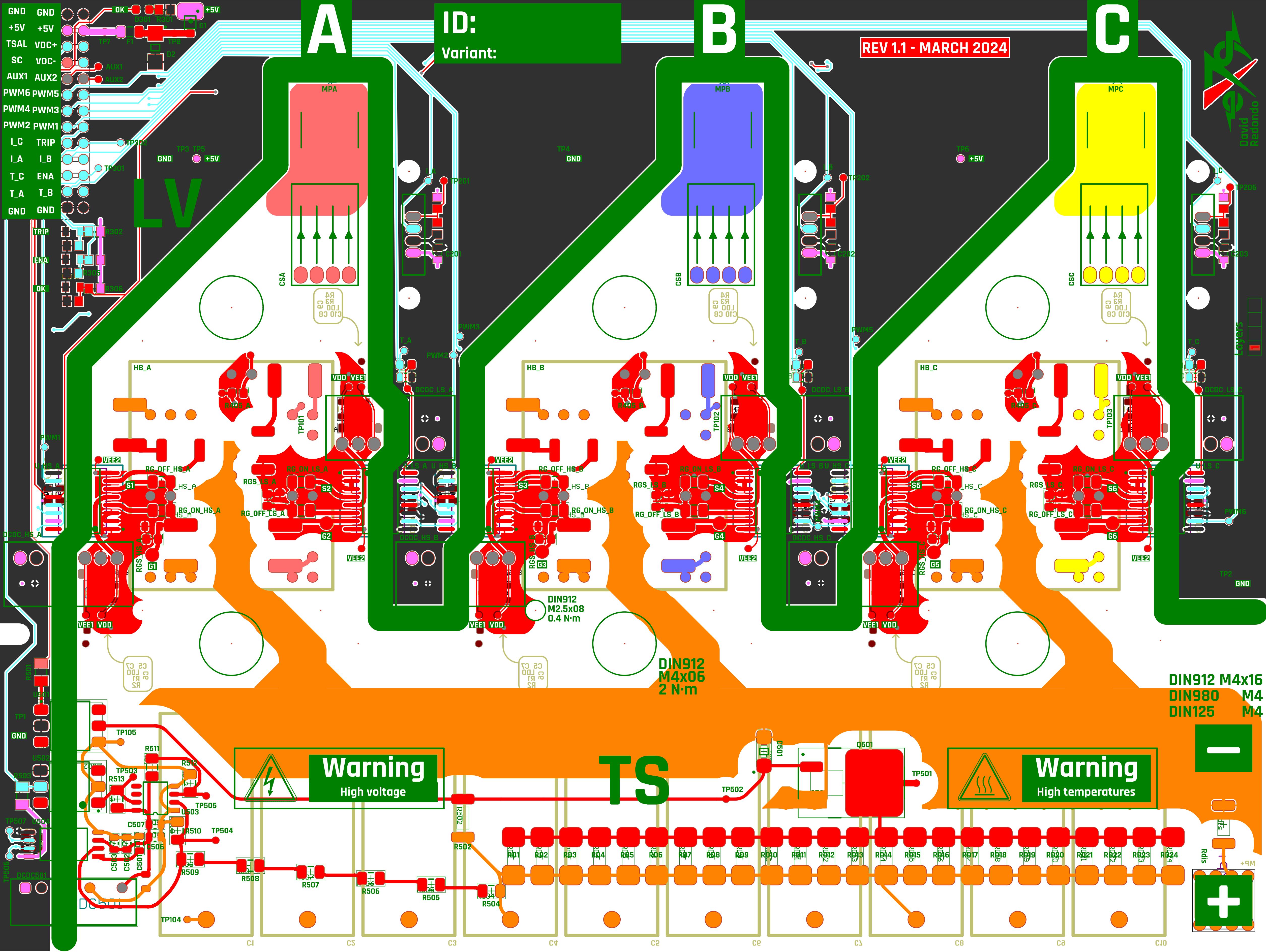
U504

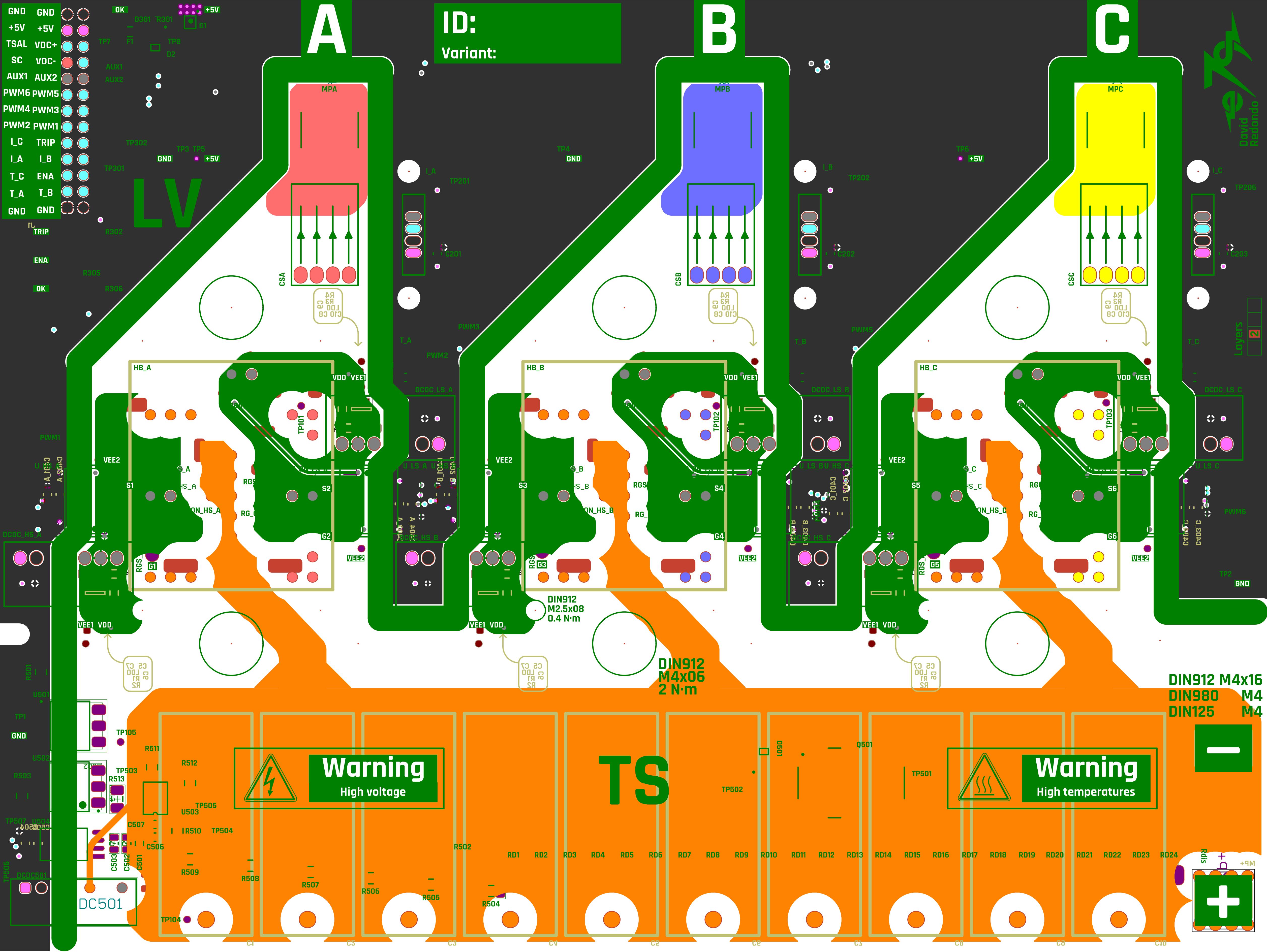
Maximum transient isolation voltage:
VTEST = VIOTM, $t = 60$ s (qualification
test) VIOTM = 7071 Vpk

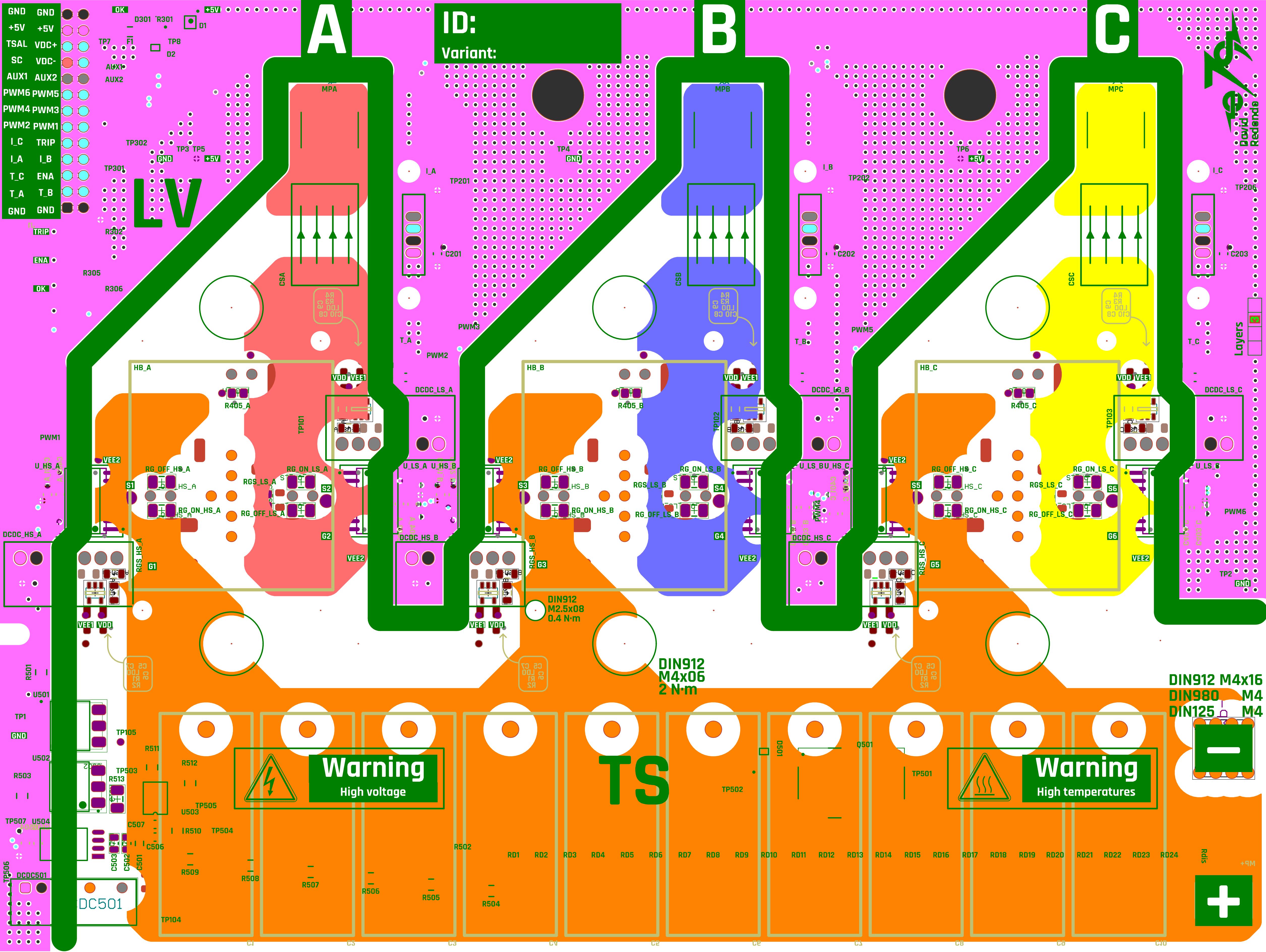
DCDC501

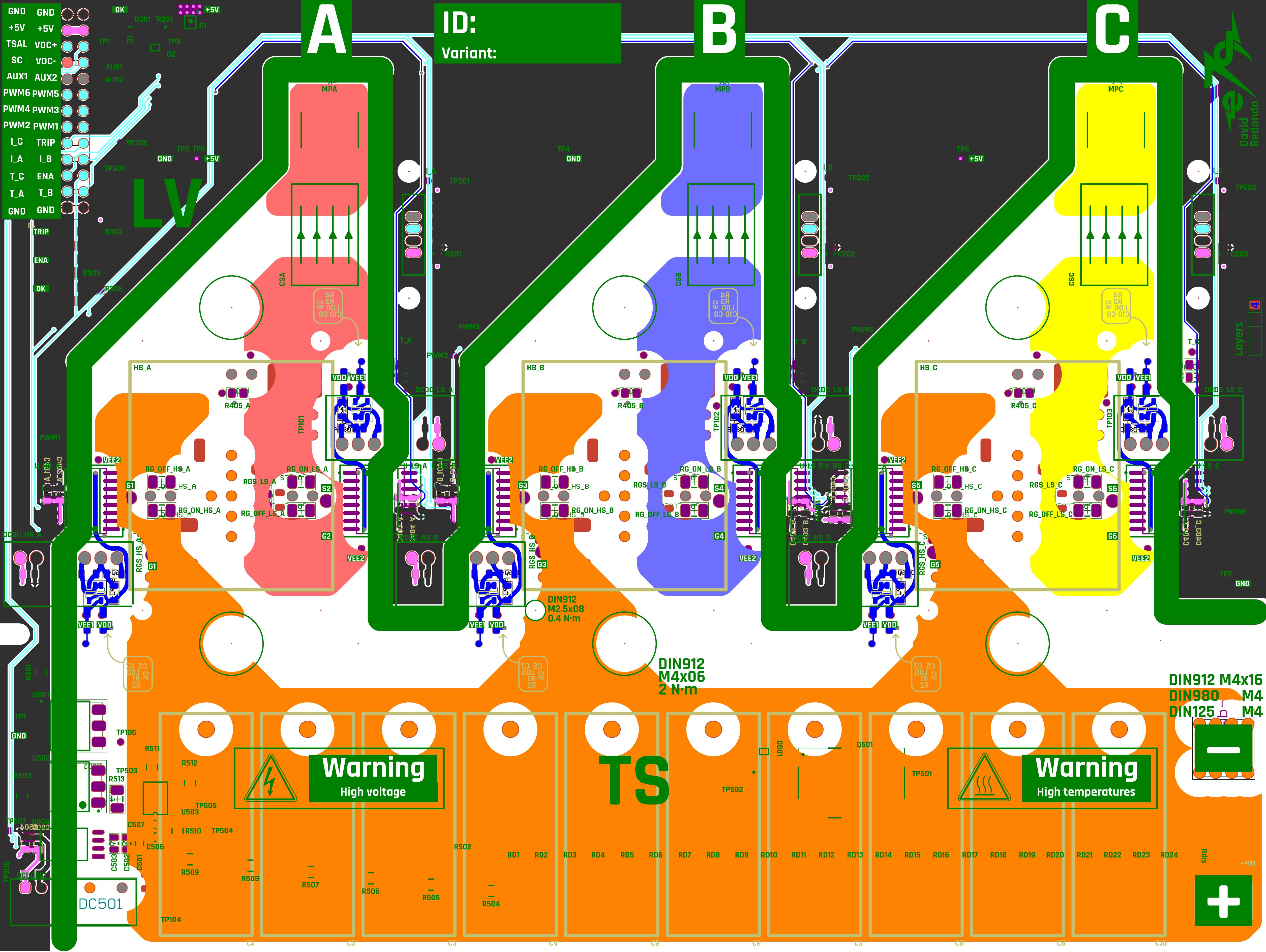
Isolation voltage input to output
tested 100% for 60s(2)
VISO = 3000 V

Company: e-Tech Racing		e-tchracing.es	
Project: Inverter Power		Variant: Wolfspeed	
Size: -	Page Contents: [5]DC.SchDoc		Version: 1.1
			Department: Powertrain
Author: David Redondo		dredondovinolo@gmail.com	Sheet * of *
Checked by: -		Date: 20/05/2024	

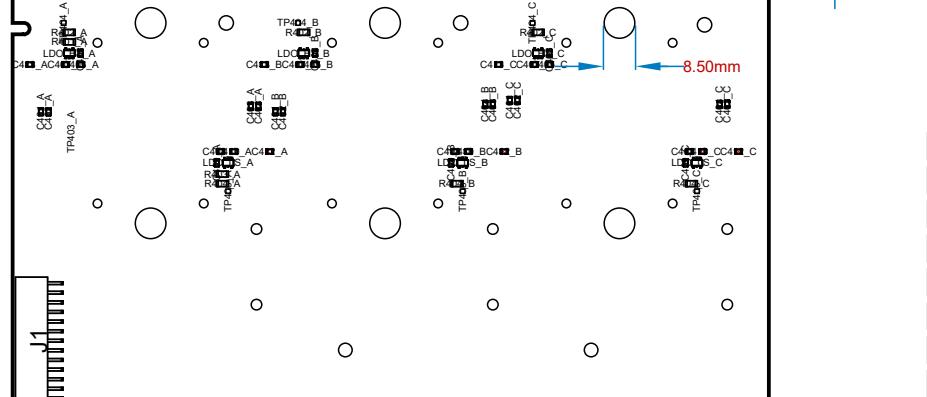
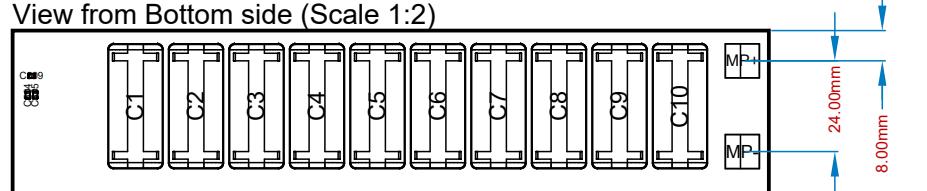
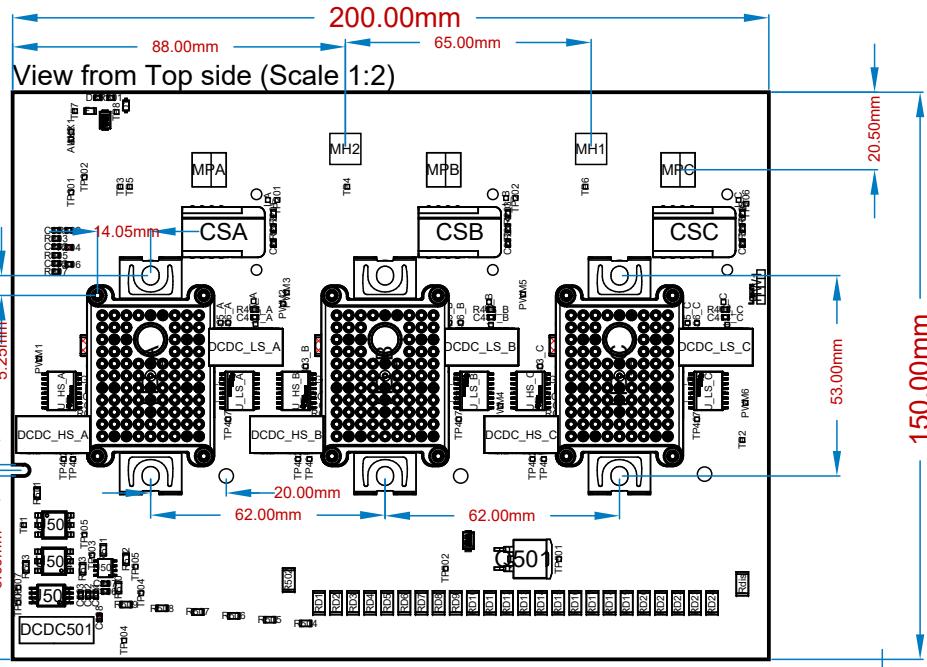








Inverter Power



Bill Of Materials

Designator	Name	Quantity
C405_A, C405_B, C405_C, C406_A, C406_B, C406_C, C408_A, C408_B, C408_C, C409_A, C409_B, C409_C	10uF	12
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	10uF 850V	10
CA1, CA2, CB1, CB2, CC1, CC2	2220Y1K0104KZT	6
F1	0437001WRA	1
D2	1779205141	1
HB_A, HB_B, HB_C	613026243121	1
R402_A, R402_B, R402_C, R404_A, R404_B, R404_C	BZG05C5V1_E3-TR	1
R401_A, R401_B, R401_C, R403_A, R403_B, R403_C	CAB016M12FM3	3
R503	CR1206-JW-303ELF	6
R511	CR1206-JW-683ELF	6
HW1	CRCW120610K0FKEA	1
MP-, MP+, MPA, MPB, MPC	CRCW120630K0FKEA	1
M4	LOGO CAPAS (4)	1
D1	M4R0530	5
DCDC_HS_A, DCDC_HS_B, DCDC_HS_C, DCDC_LS_A, DCDC_LS_B, DCDC_LS_C	MGJ6-series	6
MH1, MH2	Mounting Hole M4	2
RD1, RD2, RD3, RD4, RD5, RD6, RD7, RD8, RD9, RD10, RD11, RD12, RD13, RD14, RD15, RD16, RD17, RD18, RD19, RD20, RD21, RD22, RD23, RD24	RCV2512470KFKEG	24
R406_A, R406_B, R406_C	CR0805-FX-1000ELF	3
R301	CR0805-FX-102ELF	1
R302, R305, R306, R405_A, R405_B, R405_C, RGS_HS_A, RGS_HS_B, RGS_HS_C, RGS_LS_A, RGS_LS_B, RGS_LS_C	CR0805-JW-103ELF	12
R504, R505, R506, R507, R508, R509	CR1206AFX-6802EAS	6
R501, R513	CR1206-FX-2201ELF	2
R510, R512	CRS1206-FX-4701ELF	2
CSA, CSB, CSC	LEM CKSR 50-NP	3
U503	LM311DR2G	1
C501	885012208058	1
RG_OFF_HS_A, RG_OFF_HS_B, RG_OFF_HS_C, RG_OFF_LS_A, RG_OFF_LS_B, RG_OFF_LS_C, RG_ON_HS_A, RG_ON_HS_B, RG_ON_HS_C, RG_ON_LS_A, RG_ON_LS_B, RG_ON_LS_C	CRG1206F100R	12
U504	ISO224	1
LDO_HS_A, LDO_HS_B, LDO_HS_C, LDO_LS_A, LDO_LS_B, LDO_LS_C	TPS72301	6
U_HS_A, U_HS_B, U_HS_C, U_LS_A, U_LS_B, U_LS_C	UCC21710	6
Q501	SIH150N60E-GE3	1
R502, Rds	R2M-2512FTK	2
U501, U502	4N35	2
D501	BZG05C6V2-E3-TR	1
D301	150080GS75000	1
C201, C202, C203, C402_A, C402_B, C402_C, C404_A, C404_B, C404_C, C411_A, C411_B, C411_C, C502, C504, C506	885012207098	15
C401_A, C401_B, C401_C, C403_A, C403_B, C403_C, C503, C507	885012207103	9

Copper thickness in hole 25-50um, watch out for 1.10mm holes
Chemical tin 1-15um

Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
Top Overlay					GTO
Surface Material	Top Solder	0.01mm	Solder Resist		GTS
CF-004	TOP	0.07mm			GTL
Prepreg		0.10mm	PP-006		Dielectric
Prepreg		0.10mm	PP-006		Dielectric
Copper	GND	0.07mm			G1
FR-4		0.90mm			Dielectric
Copper	PWR	0.07mm			G2
Prepreg		0.10mm	PP-006		Dielectric
Prepreg		0.10mm	PP-006		Dielectric
CF-004	BOT	0.07mm			GBL
Surface Material	Bottom Solder	0.01mm	Solder Resist		GBS
Bottom Overlay					GBO

Total thickness: 1.60mm