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POWER PACKAGING THERMAL AND STRESS MODEL FOR QUICK PARAMETRIC ANALYSES

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ABSTRACT

This work presents an easy to use approach to quickly estimate the device temperatures and thermal stresses in a generic high power module. A low order model was developed in MATLAB using a combination of numerical-analytical approach and a 3D nodal resistor network to calculate device temperatures and thermal stresses. The model assumes a heat flux generated at the top of each device which is dissipated through the packaging structure and removed by convection. The temperature distribution is used to calculate thermal stresses throughout the package. This method eliminates computer aided drawings (CAD) in favor of numerical parameters that can be easily and quickly varied over a wide range. The resistor network solves quickly in MATLAB, enabling fast, iterative thermal analyses and design through parametric studies of the chip dimensions, number of chips, chip layout, material types, cooling solutions, etc. The model is adaptable to any number of devices and board layers. The MATLAB model reduced the computational time by 97% compared to an equivalent SOLIDWORKS finite element analysis (FEA) model and that does not include the time required to generate the CAD model and verify mesh convergence and mesh independence. Temperatures from the network model were within 5°C and stresses were within 30% of the values obtained from the FEA model. The ability to quickly assess the thermal and stress effects of a wide variety of power module design parameters during the initial design process, without the complexity of a full FEA analysis, with reasonable results can significantly improve the final module.

INTRODUCTION

Military grade power electronic systems consist of high power devices in physically constrained environments, operated in extreme conditions (temperature, humidity, radiation, pressure, dust, etc.). Additionally, the power modules comprising these power systems are required to have higher power densities and increased reliability. [1-3] The U.S. military is interested in improving power modules for many high-temperature, high-power, and high-voltage applications to enable future Army vehicle platforms. [4-5]

The cross section of a standard power module is shown in Figure 1 indicating locations of the power devices (silicon or silicon carbide), direct bond copper (DBC) substrate, solder, copper heat spreader, thermal interface material (TIM), and the heat sink.

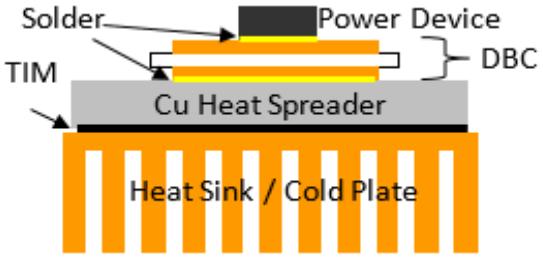


Figure 1: Schematic of a Standard Power Module

The standard package has thermal resistivity between 0.6 - 3.3 cm^2 K/W, measured relative to die area heat flux. [6] Future military modules are anticipated to dissipate 500 W/cm^2 which is significantly higher than the current dissipation of ~ 150 W/cm^2. Combining these higher power densities with an allowable chip temperature rise of 50°C, necessitates power modules with a thermal resistivity of <0.1 cm^2K/W, a very challenging goal. The 50°C is due to a maximum device temperature of 150°C and a fluid temperature between 100°C - 105°C. [4] Increasing power levels plus the need for higher packaging densities leads to higher operating

temperatures which in turn necessitates improved packaging and cooling methods.

The typical method for power module design is sequential, shown in Figure 2a; where, first the electrical schematic is developed, then the packaging is designed, and finally a heat sink is attached to the package. This results in overdesigned, costly, and suboptimal electronic systems. Therefore, a paradigm shift is desired which involves designing for the electrical, mechanical and thermal systems concurrently during the initial design phase, shown in Figure 2b.

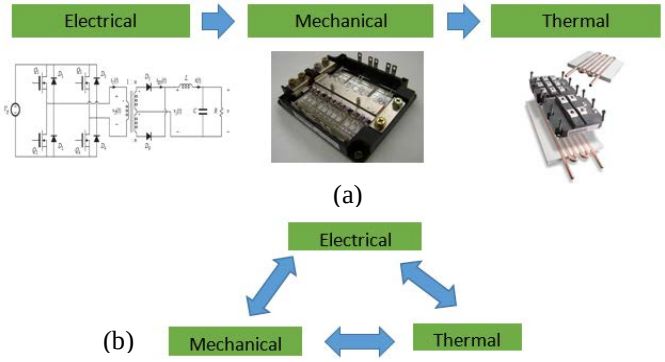


Figure 2: (a) Standard versus (b) Co-Design Approach

This Co-design approach, where individual components are "co-optimized" across multiple domains: electrical, thermal, and mechanical, allows effective evaluation of the trade-offs between the mechanical, electrical and thermal domains during the initial design phase. Doing so enables better understanding and control of the beneficial and detrimental interactions between these sub-components. Co-design allows for a multi-domain parametric analysis to enable packaging solutions that would not present themselves through the traditional design cycle. This can allow significant improvement in SWaP-C, reliability and cost.

The work in this paper presents a combination thermal and mechanical model which eliminates both computer aided design (CAD) and meshing. This is enabled by a low fidelity approach that can be used to quickly analyze a large parametric space, understand tradeoffs, and guide initial design decisions. This tool is shown to be useful for determining device spacing, module layout and the impact of various substrate decisions and cooling options.

NOMENCLATURE

C – Conductance
E – Young's modulus
Q – Heat dissipation
R – Thermal resistance
T – Temperature
c – Uniform component of strain
t_b – Bending axis location
z – Vertical location in the substrate/film stack
α - Coefficient of thermal expansion
ε - Strain
ν - Poisson's ratio
σ - Stress

THEORY

Thermal Resistance Network

The resistor network was run in MATLAB and the primary output is maximum chip temperature. This method significantly reduces extraneous output favoring only the necessary outputs such as the maximum temperatures of each device. A simplified overview of the thermal resistor network used in this analysis is shown in Figures 3 and 4 which show the resistor network in the X-Y and X-Z plane, respectively. The combination of the two networks would encompass the complete thermal resistor network. The purple nodes represent interior nodes where the thermal network equations are solved.

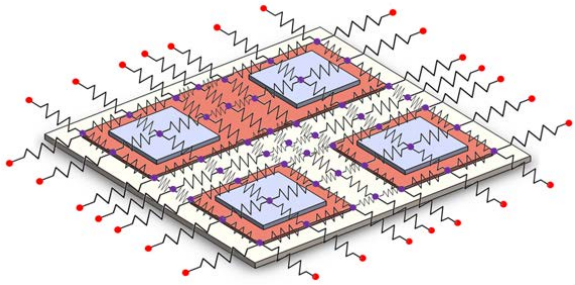


Figure 3: X – Y Plane Resistance Network Example

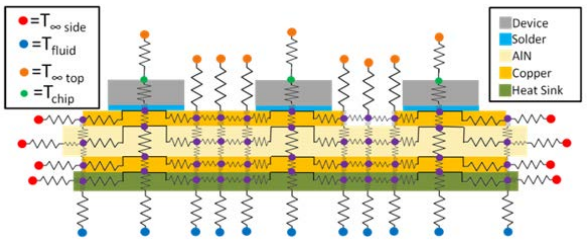


Figure 4: X – Z Plane Resistance Network Example

The green nodes depicted in Figure 4 are chip top nodes and the locations where the heat is applied. Chips should be operated below their upper temperature limit to ensure reliable operation. Therefore, this method can be used to determine the packaging approaches that maintain allowable chip temperatures. There are three types of external nodes, each with a known ambient temperature and depicted with a different color: red for the sides, orange for the top, and blue for the bottom. In addition, the convective resistances in each of these three directions can be varied to represent different cooling methods. For example, forced microchannel water cooling could be assumed at the bottom (h=100,000), pool boiling assumed on the top (h=5,000), and natural convection off the sides (h=5). The tool is very flexible with the ability to model a wide variety of layer, material and boundary configurations.

The temperatures at each of the nodes from Figure 3 and Figure 4 are calculated by performing an energy balance of the six resistances around the node, similar to Kirchhoff's First Law in electronics circuit theory. An expanded view of the resistances around a temperature node is shown in Figure 5.

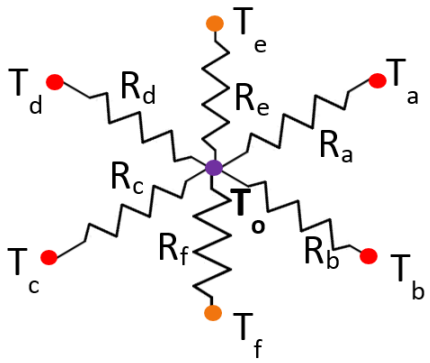


Figure 5: Single Node Resistance Network

Since all the nodes are interior nodes, they each have a resistor in each direction to another node. The equation obtained by summing the resistances around T_o from Figure 5 is:

$$\frac{(T_a - T_o)}{R_a} + \frac{(T_b - T_o)}{R_b} + \frac{(T_c - T_o)}{R_c} + \frac{(T_d - T_o)}{R_d} + \frac{(T_e - T_o)}{R_e} + \frac{(T_f - T_o)}{R_f} = 0 \qquad (1)$$

For the system described above, equations are written for each of the nodes and adjusted to form a matrix equation that is readily solved in MATLAB. The system of equations is illustrated in Figure 6. The constants in the matrix are obtained by calculating the resistances between the chips. The Q-vector represents the power boundary conditions and will consist of mostly zeros except at the locations of the chip surfaces. The T-vector is the output and represents the temperatures at each node. The primary temperatures of interest are located only at the nodes at the center of the chip surface which approximate the maximum chip temperature.

$$\begin{bmatrix} C_{111\_111} & C_{111\_211} \cdots C_{111\_112} & C_{111\_212} \cdots C_{111\_456} & C_{111\_556} \\ C_{211\_111} & C_{211\_211} \cdots C_{211\_112} & C_{211\_212} \cdots C_{211\_456} & C_{211\_556} \\ \cdots & \cdots \cdots \cdots & \cdots \cdots \cdots & \cdots \\ C_{112\_111} & C_{112\_211} \cdots C_{112\_112} & C_{112\_212} \cdots C_{112\_456} & C_{112\_556} \\ C_{212\_111} & C_{212\_211} \cdots C_{212\_112} & C_{212\_212} \cdots C_{212\_456} & C_{212\_556} \\ \cdots & \cdots \cdots \cdots & \cdots \cdots \cdots & \cdots \\ C_{356\_111} & C_{356\_211} \cdots C_{356\_112} & C_{356\_212} \cdots C_{356\_456} & C_{356\_556} \\ C_{456\_111} & C_{456\_211} \cdots C_{456\_112} & C_{456\_212} \cdots C_{456\_456} & C_{456\_556} \\ C_{556\_111} & C_{556\_211} \cdots C_{556\_112} & C_{556\_212} \cdots C_{556\_456} & C_{555\_656} \end{bmatrix} \begin{bmatrix} T111 \\ T211 \\ \cdots \\ T112 \\ T212 \\ \cdots \\ T356 \\ T456 \\ T556 \end{bmatrix} = \begin{bmatrix} Q111 \\ Q211 \\ \cdots \\ Q112 \\ Q212 \\ \cdots \\ Q356 \\ Q456 \\ Q556 \end{bmatrix}$$

Figure 6: Matrix Equation for Temperatures

Thermal Stress Model

Stresses in thin films on thick substrates were first addressed by Stoney [7], with Timoshenko [8] extending the work to include various end conditions. Both Stoney and Timoshenko limited their work to bilayer strips. Townsend et al. [9] and Suhir [10] applied the thin film approach to the problem of thermal stresses resulting from the mismatch between the CTE's of the substrate and thin film. These works extended the results to multiple thin films on a single substrate and to the case of biaxial stresses in plates. Hsueh [11] built upon the previous efforts, providing a closed form solution for the stress in the substrate and multiple thin layers that could have differing thicknesses and material properties. The thermal stress analysis outlined by Hsueh is the approach taken in this paper.

The analysis treats the system as a substrate layer on which the other film layers are stacked. The equations for the stress in the substrate and the individual film layers are:

$$\sigma_s = E_s\left(\varepsilon - \alpha_s \Delta T\right) \quad \text{stress in the substrate,}$$

$$\sigma_i = E_i\left(\varepsilon - \alpha_i \Delta T\right) \quad \text{stress in the individual film layers.} \qquad (2)$$

In both equations the value for E is the biaxial modulus given by $E/(1-\nu)$. This accounts for two dimensional planar stress, as opposed to a single dimension uniaxial stress. At each layer in the assembly, substrate and film(s), the stress distribution is assumed to be planar. The value of ε is given by $\varepsilon = c + \frac{z - t_b}{r}$, where the first term on the right represents the contribution to stress from the uniform strain component and the second term is the contribution from the bending strain. In this paper the exact formulation proposed by Hsueh is used. This formulation results in a closed form exact solution for the case of substrate and films being joined together with zero stress at some elevated processing temperature. Then the entire assembly is cooled to some uniform temperature. The work in this paper treats the heat sink or heat spreading layer as the substrate and the other layers, all the way up to the active device, as the films. In this formulation the effects of the difference in CTE's for the films and substrate are accounted for in the calculation of the uniform strain component, *c*, and the radius of curvature, *r*, of the assembly. In this paper the ΔT's are not assumed to be the same throughout the assembly, but are based on the temperature distribution throughout the assembly. This accounts for differences within a layer, as well as, across the layers. It should be noted that the stress formulation included in this paper is based only on the temperature difference between the zero stress processing temperature and the operating temperature at a particular location. It does not account for the edge effects that result from the interface of differing geometries, materials or both. Including these effects would significantly increase the complexity of the model and the time required to generate a solution.

RESULTS

Network Model Validation

The primary benefit of the technique presented in this paper is the ability to complete parametric studies in short periods of time. However, before presenting examples of some parametric studies, validation of the network model is shown. The validation was performed in two steps. First, the grid density was evaluated to establish a suitable grid size. The second step in the validation process was comparison to a finite element analysis using SolidWorks. Both steps of the validation process and the parametric studies were carried out using the geometry shown in Figure 7. This geometry contains multiple layers of varying thicknesses and materials. It can represent a single assembly or

be the building block for a larger assembly. For the validation analyses the power dissipation in the devices is 125 W/cm^2, sides and top are treated as insulated surfaces and the bottom surface has cooling at a rate of 20,000 W/m^{2}K, with an ambient temperature of 20^{o}C. Material properties were the same for both the network model and the FEA model. In both cases the material properties were constant. This particular geometry is representative of a typical power module.

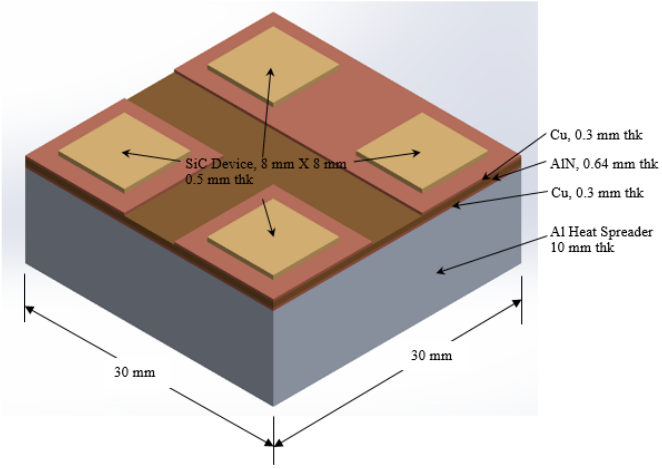


Figure 7: Model Geometry

The grid validation consisted of three grids with increasing numbers of nodes modeling the devices. These grids are shown in Figure 8. The coarse and medium grids modeled the devices as two layers, a lower layer 0.4 mm thick and an upper layer 0.1 mm thick, while the fine grid used 5 equal thickness layers. In all three models the upper layer is where the power dissipation is included. These devices typically have the power dissipation at the top surface and using multiple layers in the model better represents this scenario. For the coarse and medium grids the aluminum heat spreader is divided into two 5 mm layers, for the fine grid five 2 mm layers were used. Table 1 provides a summary of the grids used in this part of the validation process. Maximum temperature and stress results for the three grids are listed in the table. The comparison is made for the top layer of the device. For all three grids the maximum temperature occurs at the same location, the center of the devices.

Table 1: Validation Grid Comparison

Grid	Grid Size	Nodes	T_{max} (C)	σ_{max} (MPa)	Time (s)
Coarse	7 X 7 X 7	343	80.4	489.1	0.25
Medium	12 X 12 X 7	1008	78.7	502.7	0.34
Fine	16 X 16 X 13	3328	77.6	506.9	0.95

The maximum temperature for the coarse grid is 2.8^{o}C higher than the fine grid and the medium grid is 1.1^{o}C higher. In the case of the stress results the coarse grid provides only a single value for each device at its center, whereas the medium and fine grids provide greater detail. The additional detail shows that the maximum stress is located toward the corners of the devices that are closest to the center of the assembly.

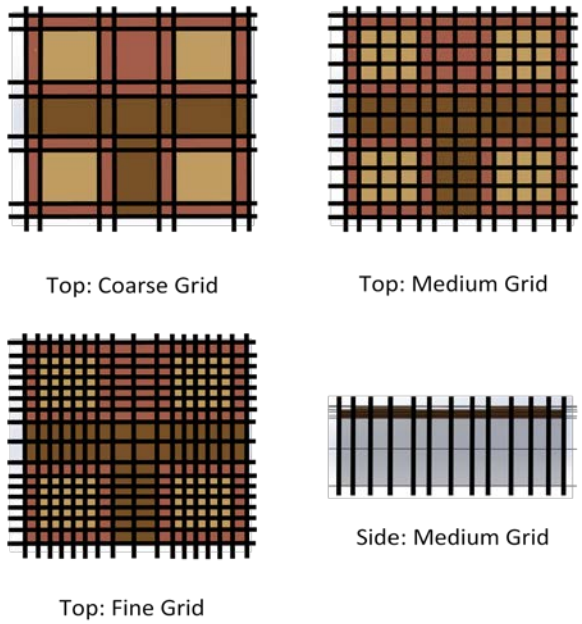


Figure 8: Model Validation Grids

The maximum value for the coarse grid is 17.8 MPa lower than the fine grid, and for the medium grid the difference is 4.2 MPa. Based on these results the medium grid will provide sufficient accuracy, capturing variations across the devices, while minimizing the overall model size.

The next step in the validation process was a comparison to a SolidWorks finite element analysis of the temperatures and stresses for the same model geometry and boundary conditions. Figure 9 shows the finite element mesh used in the validation study.

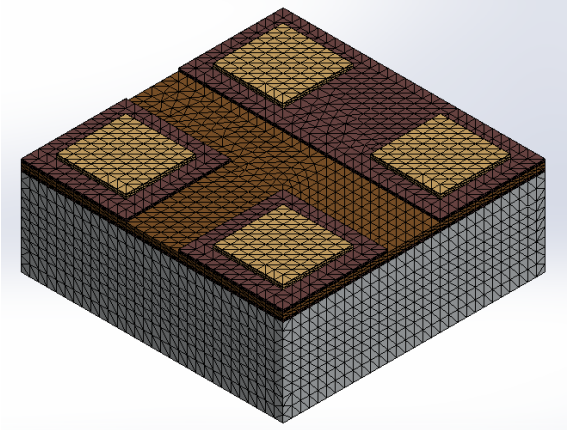


Figure 9: FEA Mesh

The mesh contains 145,771 nodes, which required 14 seconds to generate. The temperature and stress solutions required 26 seconds and 96 seconds, respectively. Similar analyses with a coarse and medium mesh were also completed as additional points of reference for solution time using the finite element

method. These meshes had 17,994 and 53,142 nodes, respectively. They required total times of 21 and 49 seconds for meshing and both solutions, respectively. The fine mesh is used for validation purposes, as the planes for comparing the temperatures and stresses for the network and finite element models were the same. Figure 10 and Figure 11 show the comparison between the network solution and the finite element model for the temperatures on the top layer of the device and the AlN layer, respectively. Due to symmetry between the left and rights sides of the model, only half of the model is shown. Both solutions show the maximum device temperature occurring at the center of the device at the top layer of the device. The FEA model shows 76.9ºC compared to 78.7ºC for the network solution. Both solutions show the temperatures being the lowest at the corners of the device, with the FEA model doing a better job of capturing the spreading effects due to the finer mesh. However, for the purposes of a parametric study the maximum device temperature is the critical value and the network model is within 2ºC. Again, for the AlN layer there is good agreement between the FEA result and the network result. The maximum temperatures are within 2ºC and the network solution accurately captures the temperature distribution throughout this layer. Figure 12 and Figure 13 show the comparison of the network solution to the FEA solution for the Von Mises Stress at these same two layers.

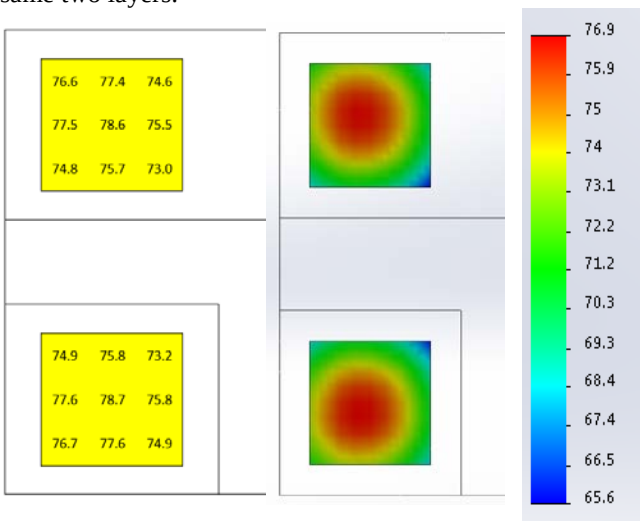


Figure 10: Device Temperature Comparison (ºC)

Comparing the stresses at the device level, the network solution over predicts the device stress by roughly 16%, but does catch the biasing of the stress toward the device corners closest to the center of the assembly. At the AlN layer the FEA solution shows a maximum stress in the center where the temperatures are cooler, with a peak value (ignoring the corner effects) of 850 MPa. The stress in the AlN layer at the device locations is biased towards the center of the assembly and has an average value of roughly 570 MPa. Looking at the results for the network solution the trends in the stress distribution are captured, with higher values at the center of the AlN and the biasing of the stress in the AlN layer under the devices towards the center. The stress at the center of the AlN is 688 MPa and the average at the device location is roughly 513 MPa. The differences between the two solutions are roughly 19% for the center value and 10% for the area under the devices.

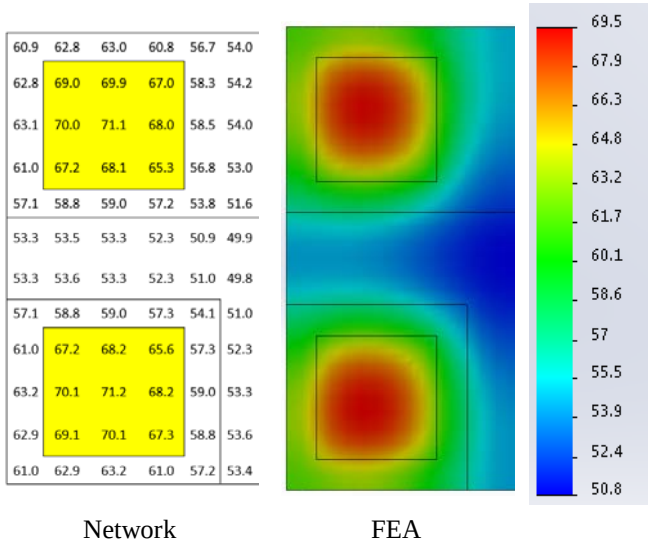


Figure 11: AlN Temperature Comparison (ºC)

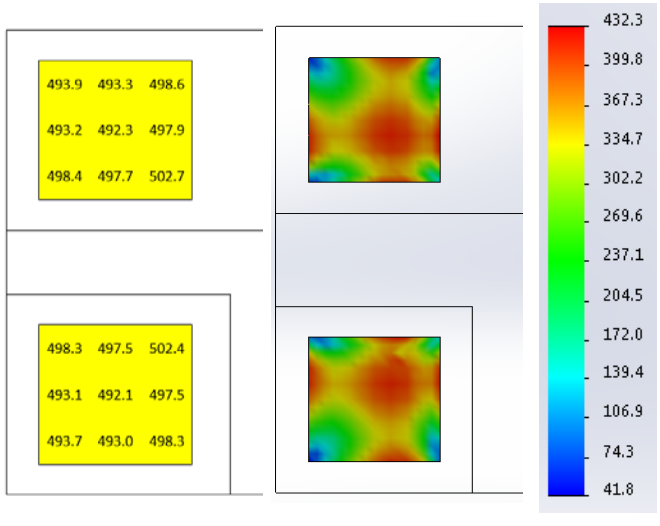
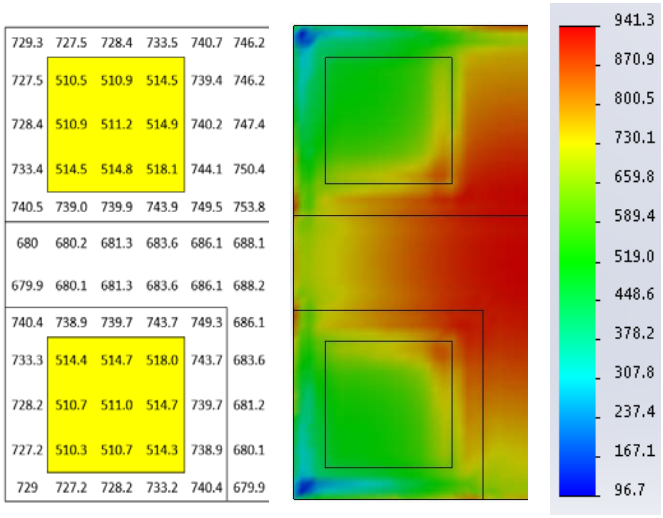


Figure 12: Device Stress Comparison (MPa)

Table 2 provides an overall comparison of the FEA and network solutions at the device level for the three meshes used in each case. Overall the comparison between the FEA and network solutions is very good. For both the temperatures and the stresses the trends in the distributions are captured. The maximum temperatures agree to within 2ºC and overall agreement is within 5ºC. The stress values do not show as good an agreement as the temperatures, but are still within 20% of the FEA solution. Again, the purpose of the network solution is the analysis of a wide range of parameters in a short period of time that correctly predicts the effects of the changes in the various

parameters. The results of the validation process indicate that the network solution will correctly represent the results of a more detailed FEA.



Network FEA

Figure 13: AlN Stress Comparison (MPa)

Table 2: Validation Solution Comparison, Device Level

Mesh	Nodes	T_{max} (C)	σ_{max} (MPa)	Time (sec)
FEA Solution				
Coarse	17994	71.4	461.7	21
Medium	53142	74.5	437.2	49
Fine	145771	76.9	432.2	128
Network Solution				
Coarse	343	80.4	489.1	0.25
Medium	1008	78.7	502.7	0.34
Fine	3328	77.6	506.9	0.95

Parametric Studies

The real benefit of the network solution is in the ability to perform parametric studies in short periods of time. Four such studies are included here to illustrate the types of analysis possible. They are the effect of backside cooling, the effect of AlN thickness, the effect of chip spacing, and the inclusion of a top side encapsulent with various thicknesses and conductivities. As a comparison SolidWorks FEA solutions were also completed for the four studies. These were done to provide a comparison of the temperature and stress results, as well as, a comparison of time.

The backside cooling study varied the bottom side cooling rate from 5,000 W/m^{2}C up to 100,000 W/m^{2}C. Five values were used 5000, 10000, 20000, 40000, 100000 W/m^{2}C. Figure 14, Figure 15 and Figure 16 show the results for the maximum device temperature, the maximum Von Mises stress and the error in the stress for the top surface of the device. The total time required for the network solution was 1.0 seconds versus 92 seconds for the FEA solution. Figure 14 shows that the maximum temperatures for the two techniques never differ by more than 2^{o}C.

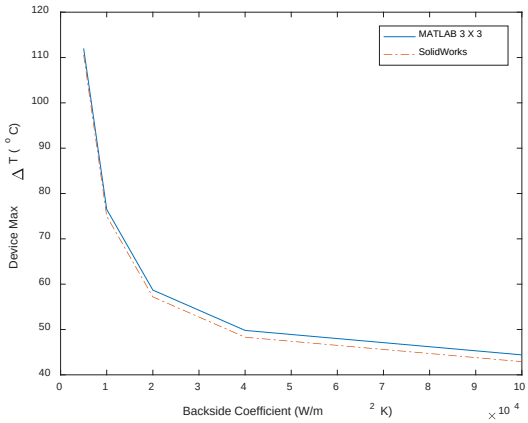


Figure 14: Temperature Comparison

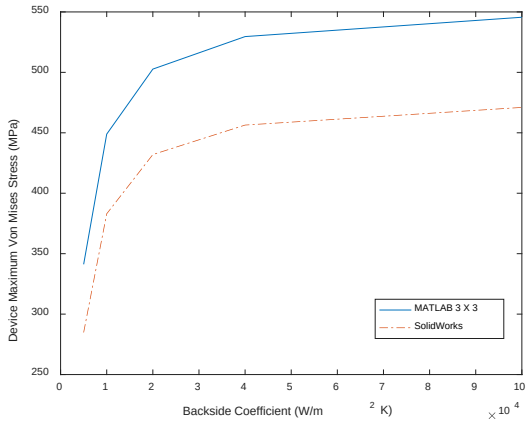


Figure 15: Von Mises Stress Comparison

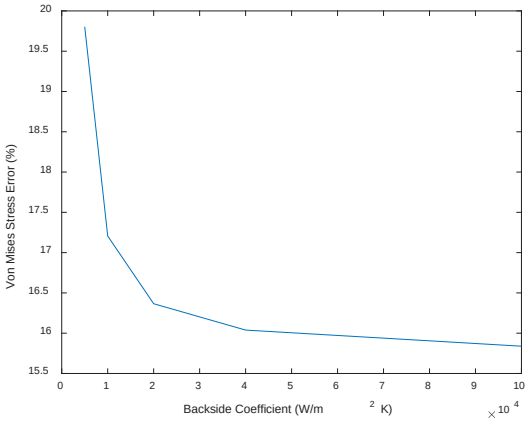


Figure 16: Von Mises Stress Error

For the Von Mises stress Figure 15 shows that the network solution consistently over predicts the stress but that the trend is properly captured. Figure 16 shows the percent difference between the two solutions, with a maximum value of 20% at

5000 W/m^{2}C. This particular study did not require re-meshing for the FEA solution.

The second study looked at the effect of varying the thickness of the AlN layer. The values used were 0.32, 0.64, 0.96, 1.28, 1.6 and 1.92 mm. For this parametric study re-meshing was required for the FEA solution. The network solution time was 1.0 second versus 98 seconds for the FEA solution. The need to re-mesh accounted for 18 seconds of the total time required. Figure 17 and Figure 18 show the temperature and stress results for this study. Figure 17 shows a difference of less than 2ºC between the network and FEA solutions for all thicknesses. It also shows an essentially linear trend with thickness, which is to be expected as the thermal resistance through the AlN varies linearly with thickness. Figure 18 shows that the Von Mises stress is also nearly linear with temperature. This is not surprising given that the CTE mismatch stress is based on the temperature difference, which was shown to be linear in Figure 17. Here again the agreement between the network and FEA solutions is good. The error in the Von Mises stress is 22% at 0.32 mm and drops to 3% at 1.92 mm.

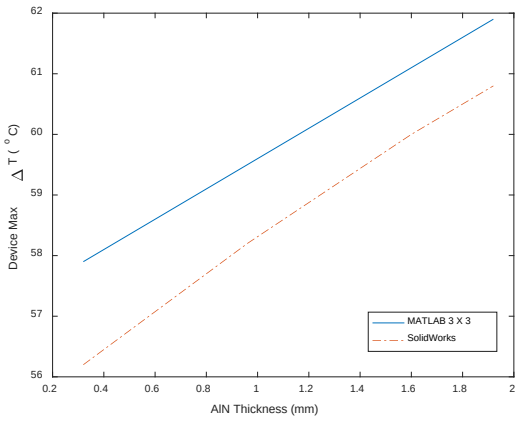


Figure 17: Temperature Comparison

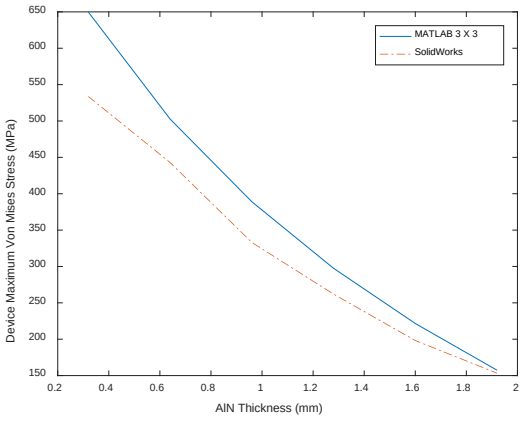


Figure 18: Von Mises Stress Comparison

The next study looked at the effects of chip spacing on temperature, stress and assembly size. The space between the two individual Cu pieces and between large Cu piece and the two individual pieces was set to 1 mm, 2 mm, 4 mm, 6 mm, 8 mm, 10 mm, 12 mm and 20 mm. The total time to complete this run using the network analysis was 1.2 seconds versus 151 seconds for the FEA. Figure 19 shows the effect of spacing on the maximum device temperature and Von Mises stress. Once the spacing reaches 12 mm the benefits of increased assembly size start to fall off, indicating that sizes greater than this do not provide any significant additional benefit. Agreement between the network and FEA results were similar to the other results, temperatures within 3ºC and maximum stresses within 20%.

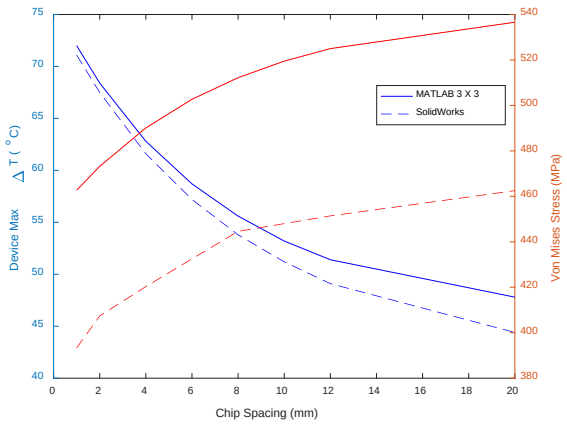


Figure 19: Chip Spacing Study Results

The final study considered the effects of an encapsulent layer on the temperature and stress. Both the encapsulent thickness and conductivity were varied for this study. The thickness of the encapsulent on top of the chips was 1 mm, 2 mm, 5 mm, 7 mm, and 10 mm. The conductivities were 0.1 W/m K, 1.0 W/m K, 5 W/m K, 10 W/m K, and 20 W/m K. Figure 20 shows the results for the device maximum temperature. At low values of conductivity, less than 1.0 W/m K, the thickness has no significant effect on the device temperature. At values greater than this the thickness can have a significant effect on the device temperature, raising it by up to 15ºC. Figure 21shows the results for the Von Mises stress. In this case the stress is more strongly influenced by the thickness than by the conductivity. Both the temperature and stress effects are a result of the amount of heat being transferred through the encapsulent to the ambient. As the conductivity increases or the thickness decreases the secondary heat transfer through the encapsulent increases. This lowers the overall temperature of the system, but raises the stress. The stress increase is due to the lower temperatures relative to the zero stress processing temperature. The network and FEA temperature results agreed to within 2ºC and the stress results to within 30%. The time required to complete this analysis was 4.7 seconds for the network solution versus 527 seconds for the FEA.

Table 3 summarizes the total computation times (all iterations) for these parametric studies. As expected run time scales with the number of iterations and the network solution is consistently two orders of magnitude faster than the FEA. The

network solution speed advantage will most likely increase with more complex models.

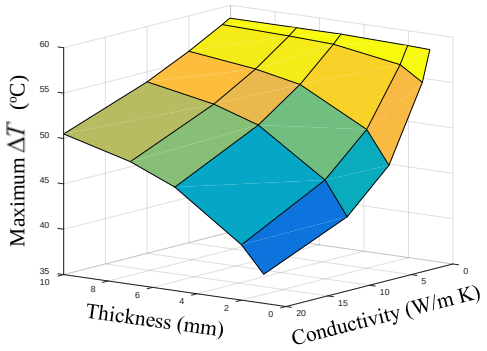


Figure 20: Encapsulent Study Temperature results

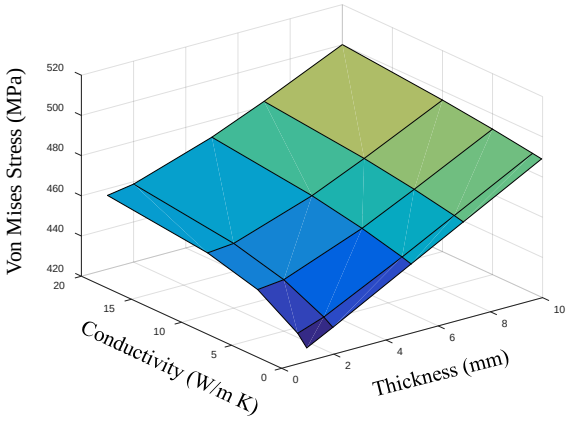


Figure 21: Encapsulent Study Stress Results

Table 3: Parametric Study Times

Study	Total Iterations	Time (sec)	
		Network	FEA
Backside Cooling	5	1.0	92
AlN Thickness	6	1.0	98
Chip Spacing	8	1.2	151
Encapsulent	25	4.7	527

CONCLUSIONS

The network analysis demonstrated in this paper provides a low fidelity, high speed design tool for completing parametric studies in electronic packaging applications. It also incorporates a Co-design approach combining both the thermal and stress analysis in a single tool. Compared to standard FEA tools, the network analysis runs up to two orders of magnitude faster, 1sec vice 100 sec. The solution provides maximum device temperatures that are within 5ºC and maximum Von Mises stresses that are within 30% of the FEA. In addition, the parametric analyses showed the correct trends in both the device temperatures and Von Mises stresses. The real value of this approach is being able to effectively evaluate trade-offs between the mechanical and thermal domains during the design phase. The multi-domain parametric analysis enables packaging solutions that might not be realized through the traditional design cycle.

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