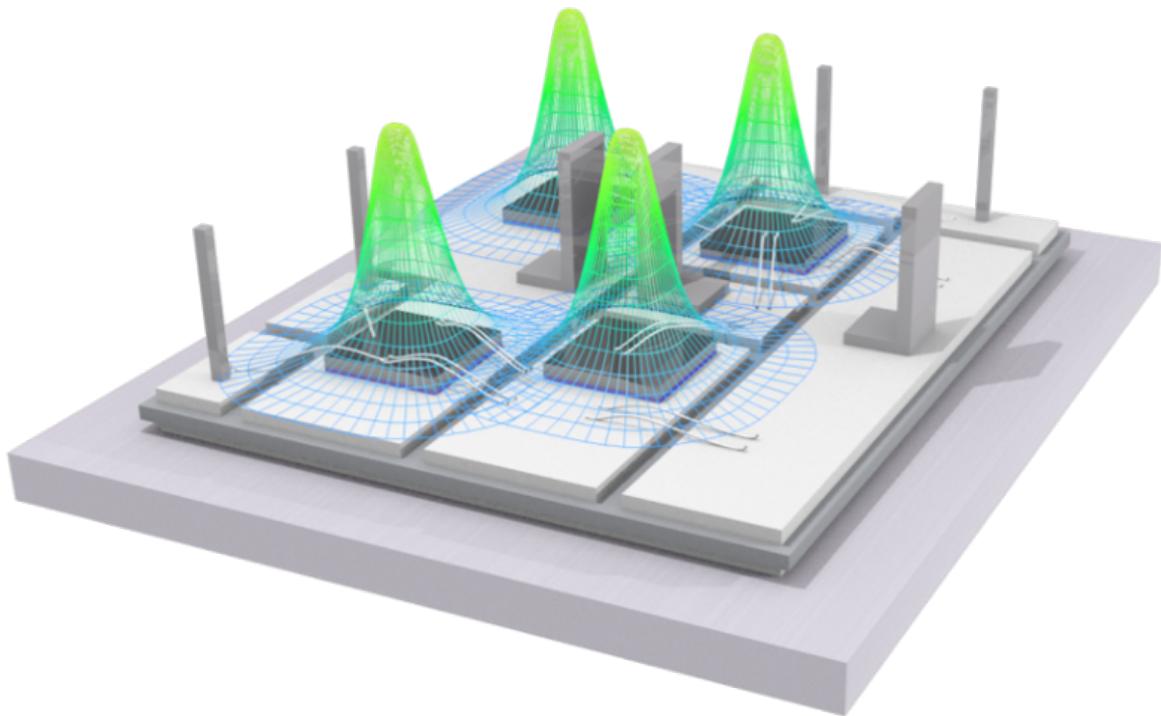




Mixed-Signal Computer-Aided Design Laboratory

## PowerSynth User Manual

June 22, 2018



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# 1 Introduction

## 1.1 Executive Summary

PowerSynth currently performs multi-objective optimization to produce Pareto-front solutions to the proper placement of power semiconductor device die and the routing of metal traces on ceramic substrates. The tool accounts for temperature distributions and electrical parasitics as a function of the layout geometries that it considers. This tool has been hardware validated. Continued research on this project will further elaborate the capabilities by extending the work to greater fidelity in both the thermal and electrical domains.

Some of the major features of this tool include:

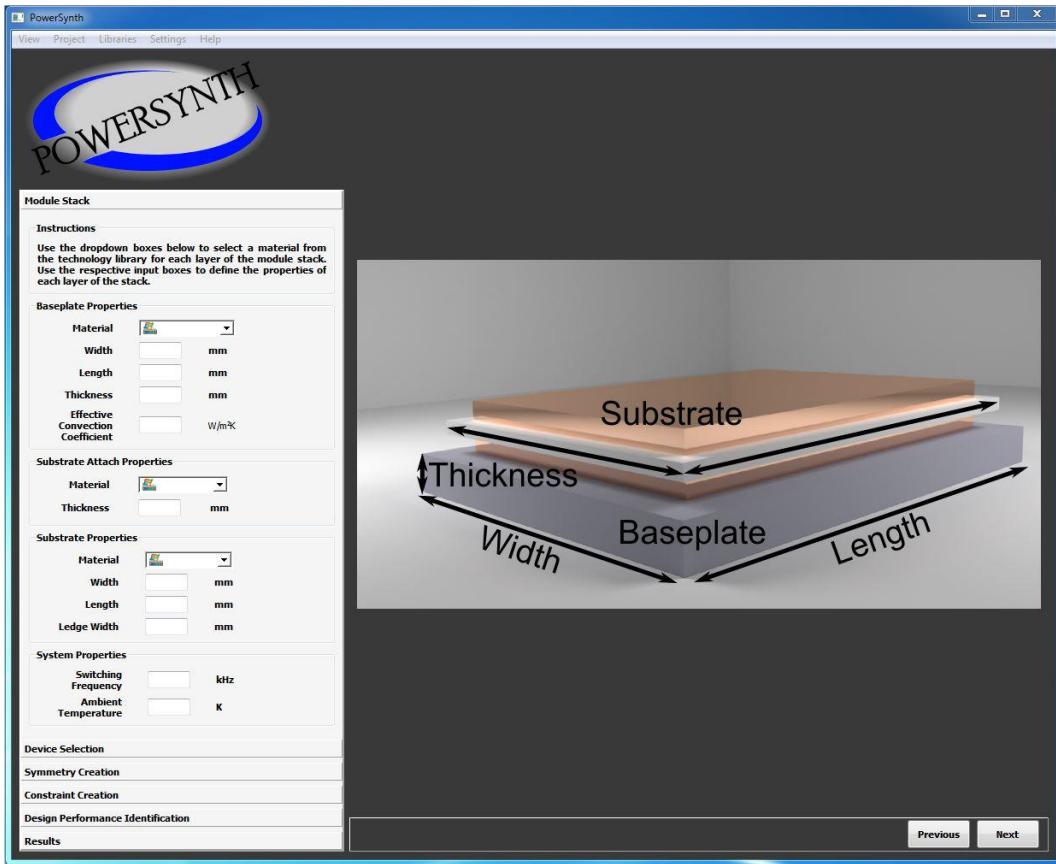
- Fast, accurate models for calculating electrical parasitics and thermal performance
- Multi-objective optimization for layout synthesis
- Able to synthesize and evaluate hundreds of layouts per minute
- User can select multiple performance metrics for optimization
- Built-in technology library including devices, substrates, attachment materials, bondwires, and more.
- Manufacturer Design Kit for incorporating packaging house design rules and tolerances
- Export designs to Ansys Q3D, FastHenry, or SolidWorks
- Post-layout optimization for trace corner filleting
- Easy to use GUI

## 1.2 Organization

After a brief introduction to PowerSynth, this document walks the user through various features of PowerSynth by creating a new project in a step-by-step presentation. Following the walkthrough, some additional information on the Technology Library, Process Design Rules, and Layout Editor are presented.

## 1.3 PowerSynth Overview

PowerSynth is an EDA tool with a friendly, graphical user interface for Multi-Chip Power Module (MCPM) layout synthesis. The tool is capable of importing a symbolic layout, which is an abstract layout representation of an MCPM, to automatically synthesize and generate multiple, real physical-layout solutions. This interface allows users to define technology libraries for power module materials, set up design constraints, and establish performance metrics for optimization. Additionally, export of optimal solutions is supported both graphically, on a 3D Solution Browser, and to modeling and analysis tools such as SolidWorks, Ansys Q3D, FastHenry, and Keysight EMPro.



The layout optimization of PowerSynth is based on fast thermal and electrical parasitic models developed specifically for this tool. The thermal model uses spatial superposition of temperature distributions to determine the temperature of devices in a module. The temperature and heat flux distribution of each device is characterized from a single run of an automated FEM simulation. In this simulation, a single die is placed in the center of the module atop an un-patterned substrate. The top surface of this device is treated as the source of power dissipation and a heat transfer coefficient is applied to the backside of the module heat spreader.

A compact thermal model (CTM) is then constructed from the results of this simulation. Thermal resistance values for the CTM are found by placing the characterized temperature distribution for each device in superposition with neighboring ones. Heat flux distributions obtained in the characterization step are used to account for the interaction among devices given their positions on the current trace layout. Once the CTM is constructed, linear algebra techniques similar to those found in circuit analysis are used to predict the temperatures of each device. The model can predict changes in temperature over variations in trace layout and device positioning with a maximum error of less than 10%.

The electrical parasitics in a module are approximated by closed-form solutions to micro-strip transmission line models. Since all power modules share the same basic geometry, the micro-strip model provides a reasonably accurate representation of a power module's trace parasitics. This is many times faster to execute when compared with finite element analysis. The electrical parasitic extraction works by breaking down a given layout into a lumped element network or graph with resistance and inductance values for each element or edge, approximated by micro-strip solutions. Capacitance from trace to baseplate (effective ground-plane) is evaluated at each lumped element node. These values can be used either directly in optimization or written into a netlist for simulation

purposes.

PowerSynth operates on an imported symbolic layout. This is a simple drawing of the topology of an initial module layout and is easy for a designer to create. A symbolic layout is comprised of three basic elements: lines, points, and rectangles. The line elements represent traces or bond wires. The point elements represent particular devices or leads, and the rectangle elements represent traces which span multiple traces vertically or horizontally in topological space. A designer chooses a set of performance metrics, in this case electrical or thermal, based on the symbolic layout. A multi-objective optimization problem is formulated based on the symbolic layout by allowing each layout line-element a variable width, which constitutes a set of design variables. The Non-dominated Sorting Genetic Algorithm II (NSGA-II) is used to perform the optimization procedure.

After the optimization routine is run, a particular layout can be selected from a set of trade-off solutions for the MCPM design, allowing the designer easy access to the entire, viable design space. This system also allows a designer to quickly test many different layout solutions while maintaining layout quality. The fast electrical and thermal models both predict temperature and parasitic values accurately with respect to FEM tools.

## 2 Using PowerSynth

### 2.1 Installing PowerSynth

1. Run the PowerSynth install wizard
2. Run PowerSynth.exe

**Note:** It is STRONGLY RECOMMENDED that you install PowerSynth in the C drive (the default installation directory) and NOT in Program Files. Installing PowerSynth in Program Files can result in various issues relating to administrator permissions.

### 2.2 Creating a New Project in PowerSynth

#### 2.2.1 User Interface

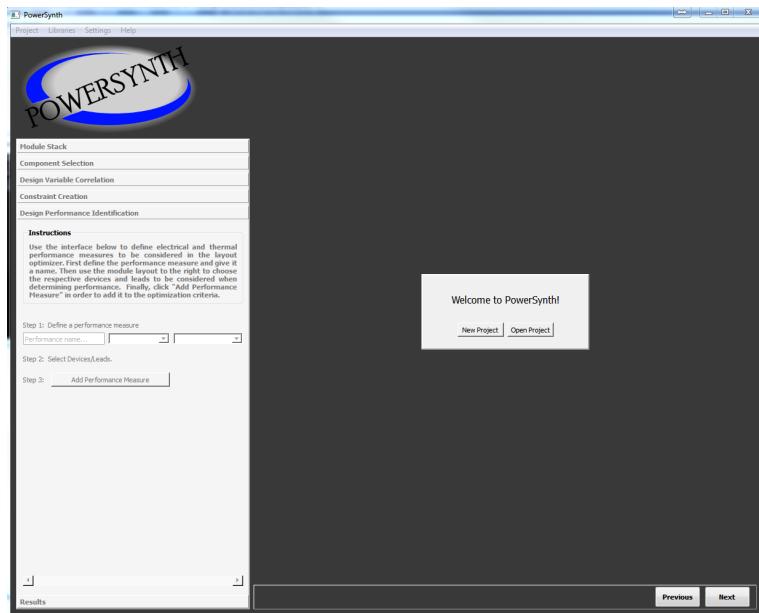
The welcome screen is shown on the right. The navigation pane on the left is used to develop a project once a new project is created or an existing project is opened. Before we click “New Project”, we need to define the layout template that will be imported.

#### 2.2.2 Symbolic Layout File

A symbolic layout is a simple stick diagram used to represent a simple power module’s abstract layout. In the previous version, PowerSynth relies on InkScape to create a SVG file. This SVG file represents a stick diagram which is then imported into PowerSynth for a new project. In this version, SVG feature has been removed due to some unstable functionalities. Instead, the user can provide a script (text file) to define the stick diagram. Each point on this stick diagram represents either a device or a lead, while each line represents a trace. Bondwires information will need to be provided later in the setup (see Assigning Virtual Wires Connections). This script must be created before creating a new project in PowerSynth. Open a text file and define the layout template using lines and points with the syntax as shown below. Lines denote traces, while points denote devices and leads. Below is a sample layout script. It is of the format:

##### Name Type (x1,y1) (x2,y2)

Note: The element name (first column) must be four characters long. For a point, (x1, y1) is the coordinate of the point. For a line, (x1, y1) is one of the end points. (x2, y2) is the other endpoint. Save this file in either .psc or .txt format.

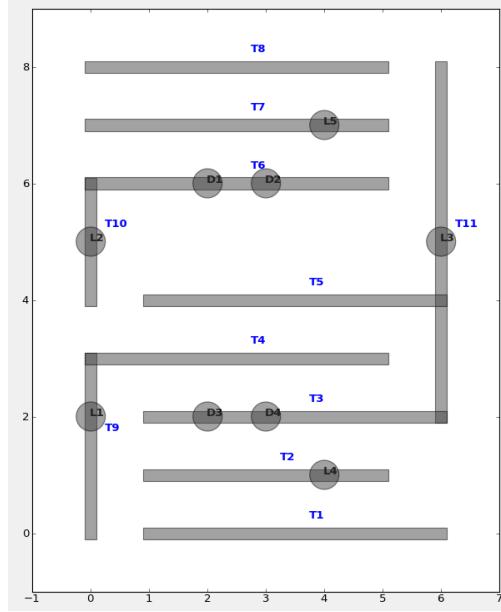


The example script for the symbolic layout is shown below:

```

T1 l (1,0) (6,0)
T2 l (1,1) (5,1)
T3 l (1,2) (6,2)
T4 l (0,3) (5,3)
T5 l (1,4) (6,4)
T6 l (0,6) (5,6)
T7 l (0,7) (5,7)
T8 l (0,8) (5,8)
T9 l (0,0) (0,3)
T10 l (0,4) (0,6)
T11 l (6,2) (6,8)
D3 p (2,2)
D4 p (3,2)
D1 p (2,6)
D2 p (3,6)
L1 p (0,2)
L2 p (0,5)
L3 p (6,5)
L4 p (4,1)
L5 p (4,7)

```



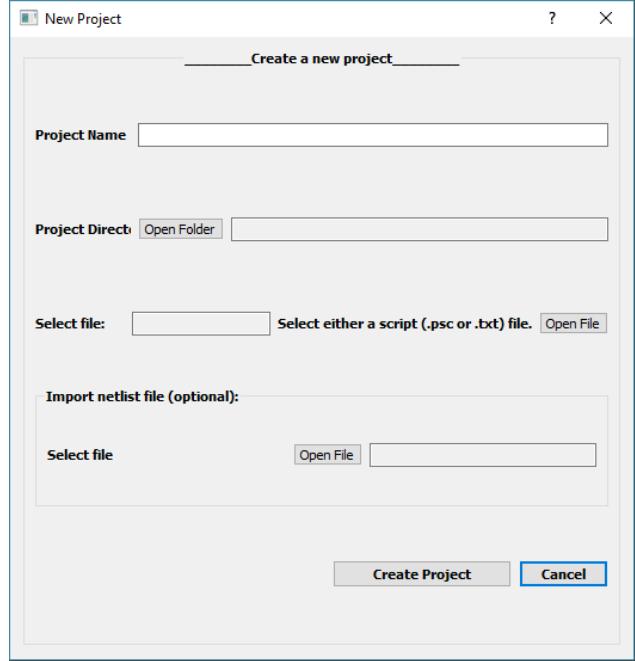
Note that these coordinate values are not real coordinates and thus have no dimensional units. These coordinates are used to find the relative position of each line and point to each other. Once this file is imported to the software, an automatic normalization algorithm will run to count the number of rows and columns. These coordinates are then normalized between zero and the maximum number of rows/columns. The corresponding symbolic layout for the abovementioned script is represented on the left. Once the project is loaded, the layout can still be modified using the Layout editor under **Project -> Open Layout Editor**

### 2.2.3 Create a New Project

Selecting the “New Project” button on the welcome window brings up the dialog for a new project as shown on the right. First, give the project a name. Then, select the folder where it will be saved. Import the symbolic layout file as shown above using “select file”. Select the directory where you saved the text file. Finally, click “Create Project”.

*Optional:* The user can also specify a netlist file that have same circuit topology with the symbolic layout. This can be later used to map the net names with the symbolic layout object. A sample netlist format for a 4 switches half bridge is shown below:

```
*Sample Netlist file:  
M1 DC_plus G_High Out Out NMOS  
M2 DC_plus G_High Out Out NMOS  
M3 Out G_Low DC_neg DC_neg NMOS  
M4 Out G_Low DC_neg DC_neg NMOS  
.model NMOS NMOS  
.model PMOS PMOS  
.end
```



## 2.3 Defining the Module and Components

### 2.3.1 Module Stack

The module stack tab on the left allows the user to input module stack information for the design. This includes dimension and material information of the substrate, substrate attach and baseplate. Operating conditions such as ambient temperature, effective convection coefficient of baseplate and switching frequency are also required for thermal and electrical evaluations. The user can update the tech files (.p) using \* Libraries->Tech lib.

**Module Stack**

Use the dropdown boxes below to select a material from the technology library for each layer of the module stack. Import a layer stack CSV file or use the respective input boxes to define the properties of each layer of the stack.

**Baseplate Properties**

Material	<input type="button" value="MarkTech Mo70Cu Moly - Copy.p"/>
Width	60.0 mm
Length	60.0 mm
Thickness	6.0 mm
Effective Convection Coefficient	100 W/m <sup>2</sup> K

**Substrate Attach Properties**

Material	<input type="button" value="Pb-Sn Solder Alloy.p"/>
Thickness	0.08 mm

**Substrate Properties**

Material	<input type="button" value="Al-AlN-Al 16-25-16 mils.p"/>
Width	40.0 mm
Length	50.0 mm
Ledge Width	2.0 mm

**System Properties**

Switching Frequency	100 kHz
Ambient Temperature	300 K

Another way to import this module stack is through a csv layer stack file. The description for this file is explained in the next section.

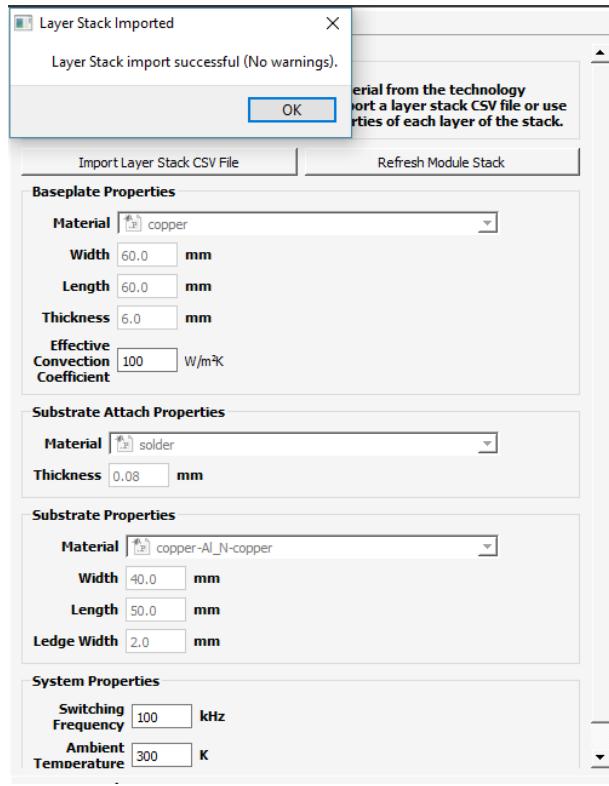
### 2.3.2 Layer Stack File

Abbrev	LayerID	Name	Layer Position	Width	Length	Thickness	Material
B:	1	B1	1	45	45	6	copper
SA:	2	SA1	2	40	40	0.08	solder
M:	3	M1	3	38	38	0.41	copper
D:	4	D1	4	40	40	0.64	Al <sub>N</sub>
I:	5	I1	5	28	28	0.41	copper
C:	5	C1	6	2.5	4	0.2	SiC

The Table above shows the module stack structure. The user can specified this in an excel (.csv) and load it using the **Import Layer Stack File** button in the UI.

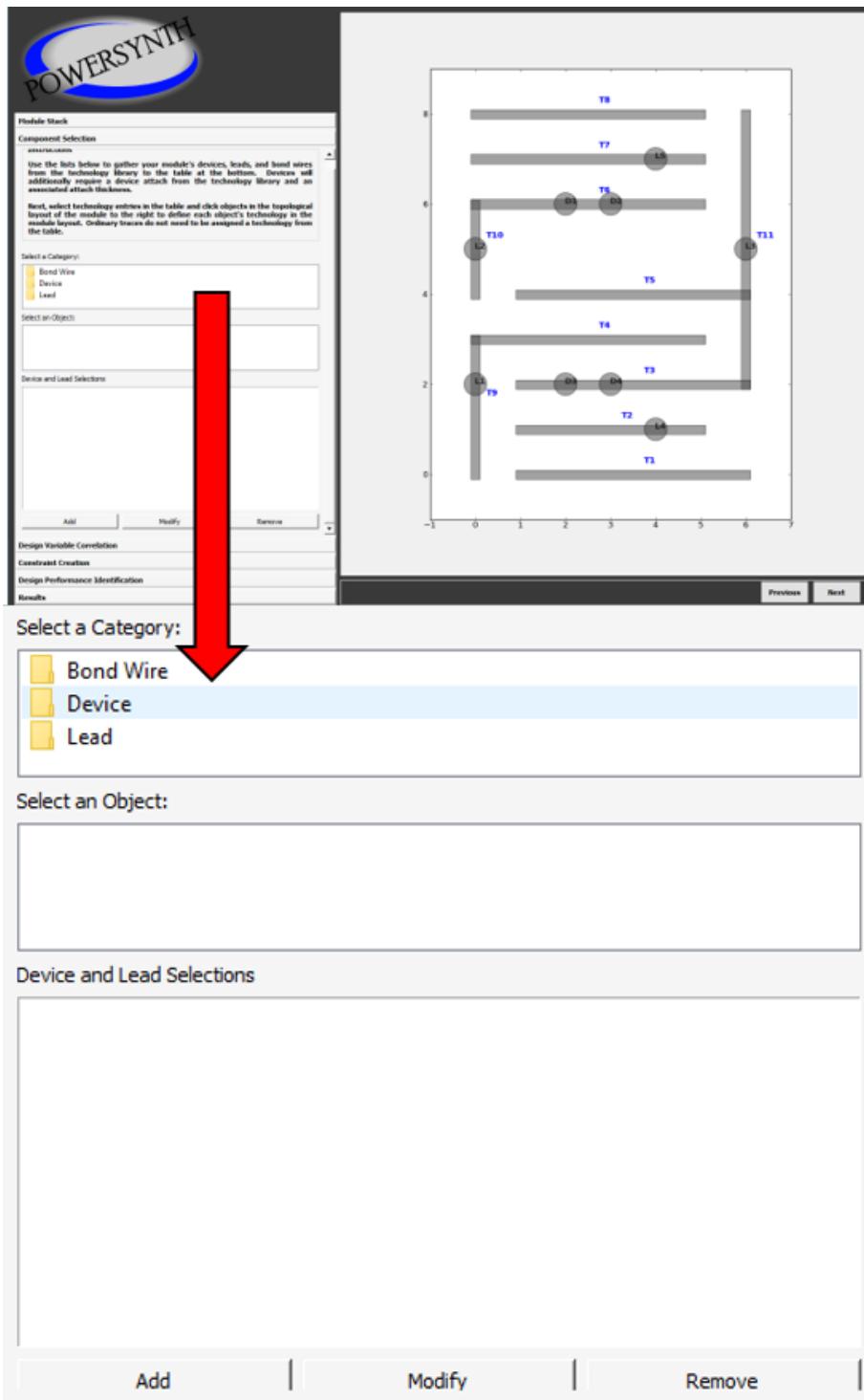
Some Abbreviation: B: Baseplate, SA: Substrate Attach, M: Metal, D: Dielectric, I: Interconnect (Metal), C: Component (this is optional for this version).

Below shows the UI after successfully importing the layer stack. To go back to the normal mode, press the **Refresh Module Stack** button.



### 2.3.3 Component Selection

The symbolic layout is shown on the right side of the interface. This allows users to insert component technology files. These files contain information about the bondwires, leads, and devices the user wishes to include. Notice that the names from the layout script for each traces and Devices are shown on the right-hand side. (Symbolic Layout)

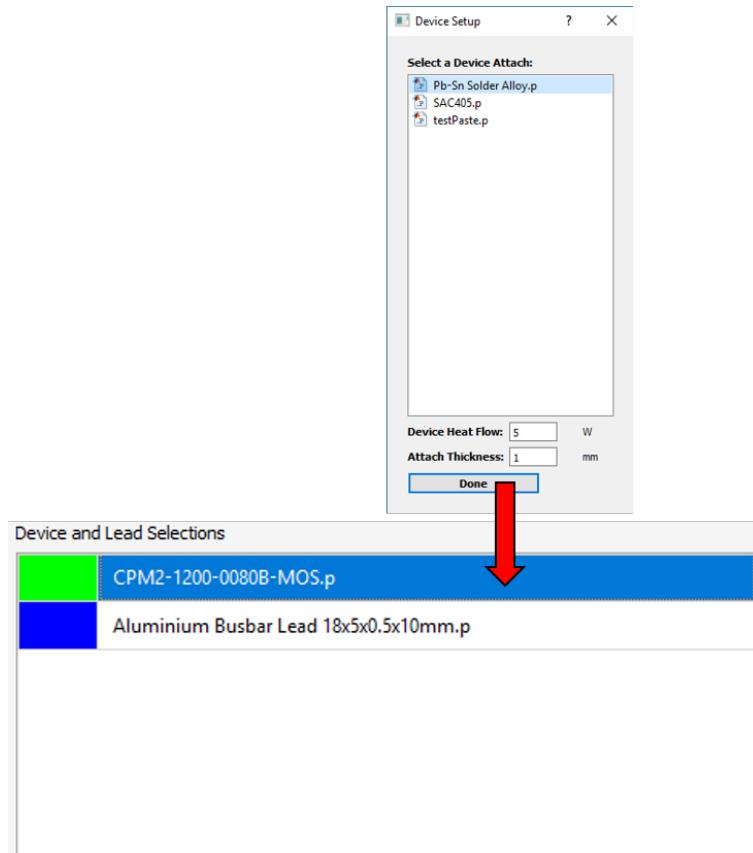
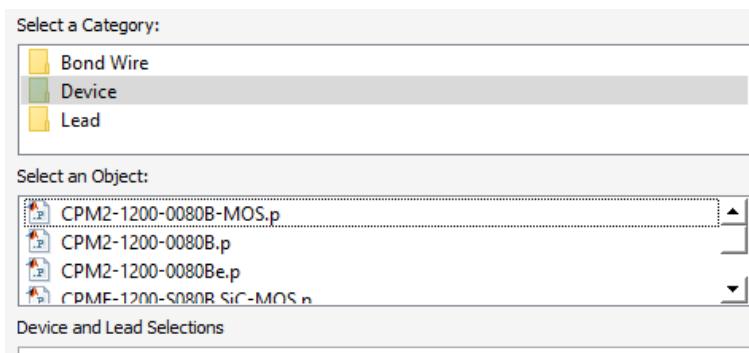


The user can assign devices and leads to the circles on the symbolic layout. The unassigned lines will represent copper or aluminum traces (depending on substrate selection). Wires bond will be treated as virtual connections. However, it is recommended to finish the devices and leads selection first before assigning virtual wire bonds to ensure correct connection.

### 2.3.4 Device and Lead Selection

Click on “Device” or “Lead” from the Category list, a list of objects under object selection will be listed out. This can be specified using the Tech-Lib (See Technology Editor section)

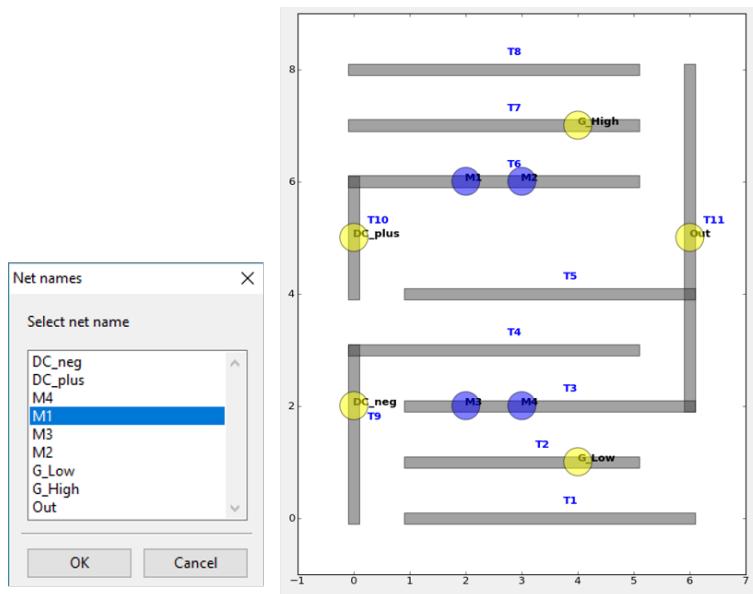
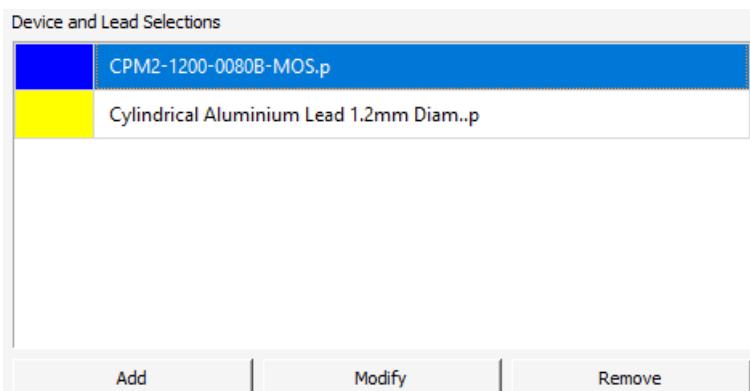
Once an object is selected, press the “Add” button. In case of device, this will pull up a dialog on the right to define the solder type (tech lib), solder thickness and average power of the device. This information will be used for thermal optimization. Click Done to apply this for the device. This will update the device and lead selection table. The user can do the same for the lead selection to fill the Device and Lead Selection table on the right.



### 2.3.5 Assigning Devices and Leads

First, select a device or lead object from the table.

Assigning these selections on the Symbolic Layout by clicking on the circles. To deselect, click on the selected circle one more time. The circles will be colored based on the random generated color on the Device-Lead Table. In case the user imported a netlist (Create new project section), a small dialog will be triggered to select the corresponded net name.

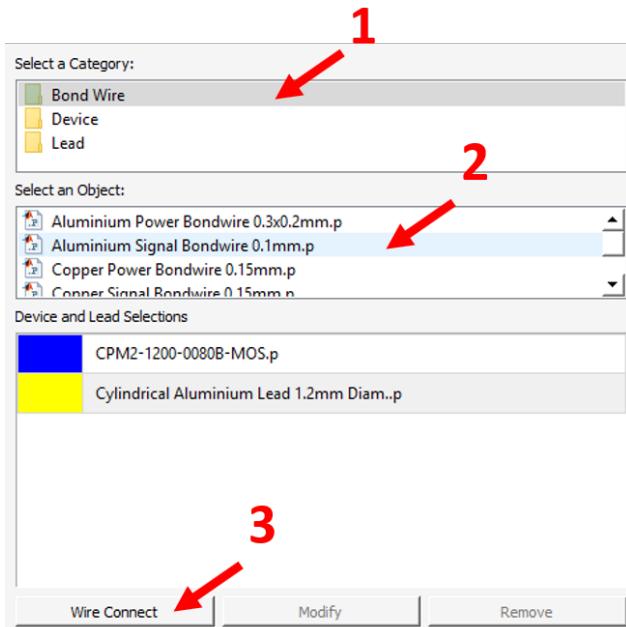


### 2.3.6 Assigning Virtual Wire Connections

Once all of the devices and leads are setup like above, the next step is to setup the virtual wires connections. To do this, first click on “Bond Wire” from the categories selection list. Then, select a bondwire object. The “Add” button will change its text to “Wire Connect” as seen on the right:

A bond wire Setup dialog will open as seen on the right. The symbolic layout is now in wire selection mode. The user will need to select 2 traces or a trace and a device (device to device bondwire is not supported yet) for wire connections. For a MOSFET, it is required to have signal and power wires for signal and source sides. To select 2 objects, simply click on the symbolic layout again. The selected object will be hatched as shown below.

The **Add** button on the dialog will be enabled if 2 objects are selected (click again if you want to deselect an object). Click this to add the wire connection to the table. Doing so, we can have a complete table (on the left). Close the dialog, the table can be saved and edited any time.



The screenshot shows the 'Bondwire Connections' table with 8 entries. The table includes columns for Bondwire Type, Start, Stop, and Model. A schematic diagram at the bottom shows a horizontal bus with points T7, G (High), M1, T6, M2, and T10. The 'Wire Destination Selection' section shows a list of connections:

Bondwire Type	Start	Stop	Model
1 SIGNAL	M1	T7	Aluminium Signal Bondwire 0.1mm.p
2 SIGNAL	M2	T7	Aluminium Signal Bondwire 0.1mm.p
3 SIGNAL	M3	T2	Aluminium Signal Bondwire 0.1mm.p
4 SIGNAL	M4	T2	Aluminium Signal Bondwire 0.1mm.p
5 POWER	M1	T5	Aluminium Power Bondwire 0.3x0.2mm.p
6 POWER	M2	T5	Aluminium Power Bondwire 0.3x0.2mm.p
7 POWER	M3	T4	Aluminium Power Bondwire 0.3x0.2mm.p
8 POWER	M4	T4	Aluminium Power Bondwire 0.3x0.2mm.p

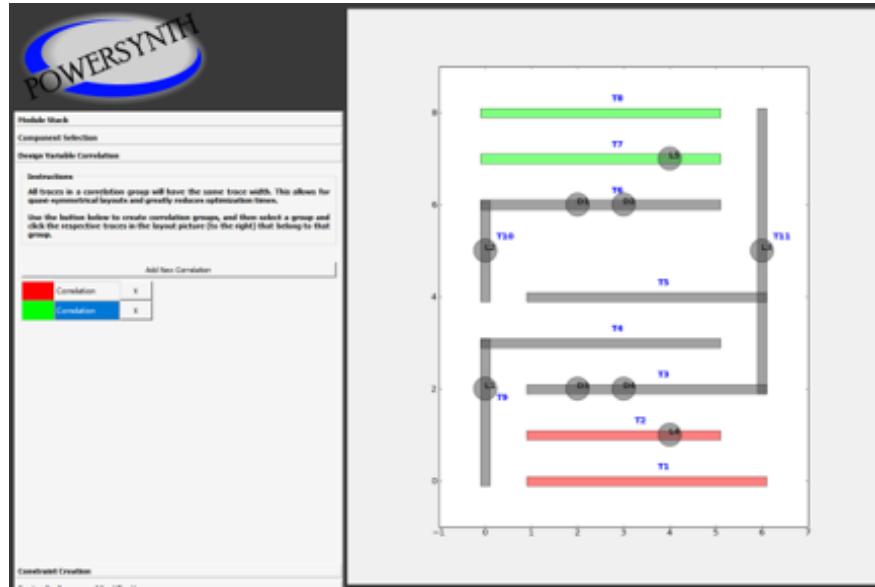
Buttons at the bottom are 'Add' and 'Remove'.

**Full Virtual Connection Table**

## 2.4 Defining Correlations and Constraints

### 2.4.1 Design Variable Correlation

If symmetrical traces or device positions are desired in the design, correlation between devices or traces can be assigned. This will ensure that selected traces will have the same width (length) or that selected devices will have same position. Click “Add New Correlation” and a new row will appear in the table. Click on a row then click on traces or devices to specify a correlation.



### 2.4.2 Constraint Creation

Here, the user can click on each line (trace) to specify a min and max or fixed width for a trace. If there are symmetry constraints, these will be applied to all symmetric traces.

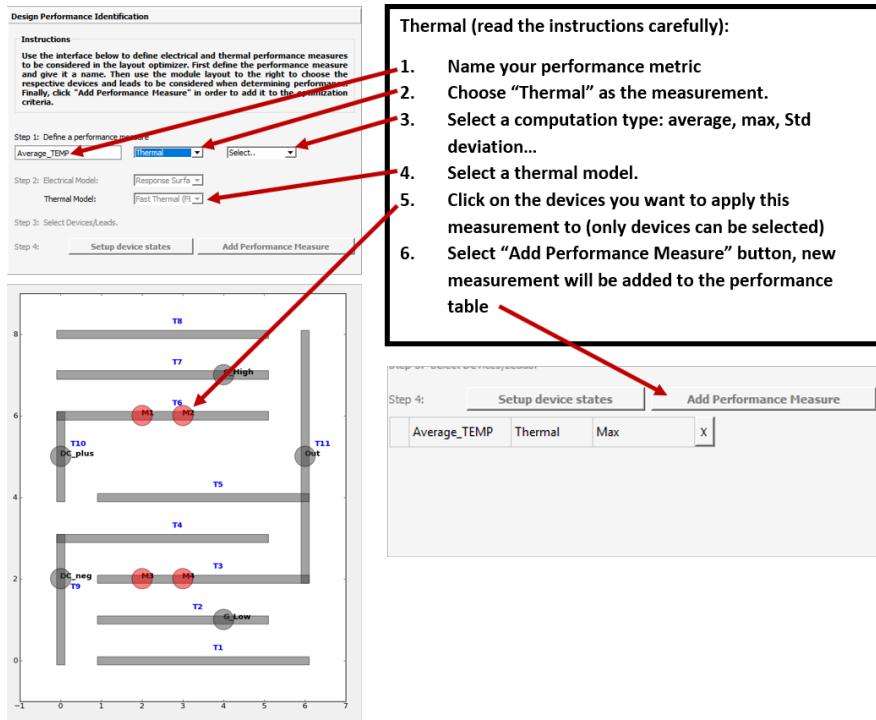


## 2.5 Design Performance Identification

In this step, the user can choose the performance metrics that are to be optimized. The next two sections below show the process for assigning performance metrics. Once the performance metrics are selected, the user can go to the next tab to run the design optimization. Currently, PowerSynth supports thermal and electrical measurement of a power module.

### 2.5.1 Thermal Measurement

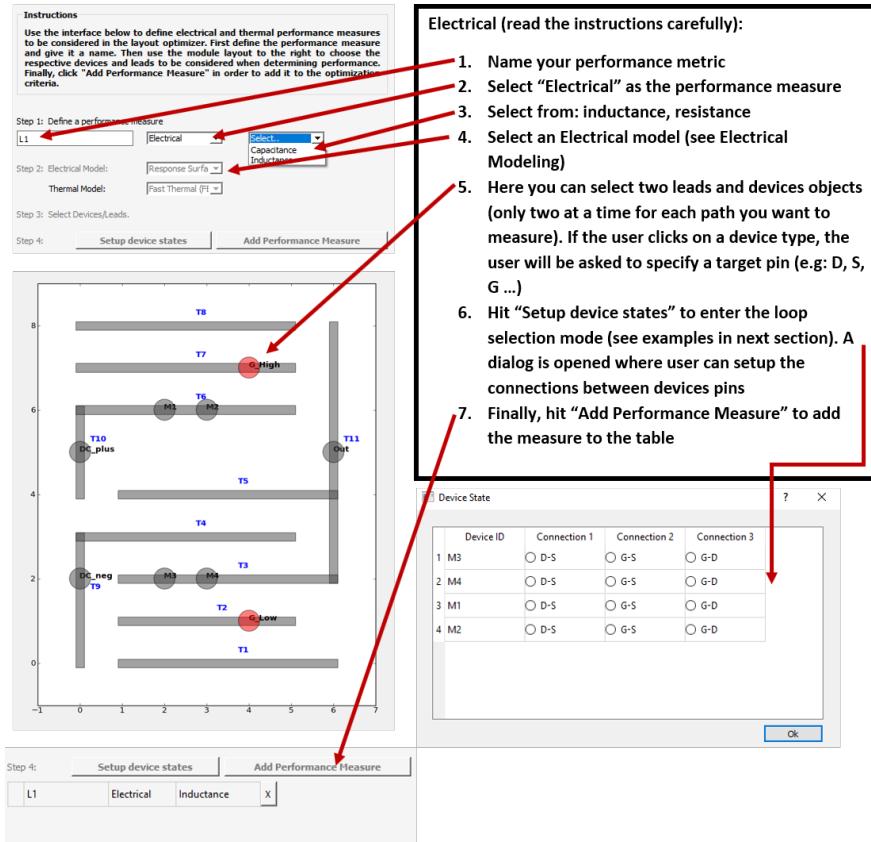
On the navigation tool, a user can define a performance measure. There are 2 available thermal models in PowerSynth: Rectangle Flux (analytical) and Fast Thermal (Characterized by FEM simulation). In case of thermal measurement, follow the steps below:



## 2.5.2 Electrical Measurement

Parasitic capacitance, resistance, and inductance can each be specified as design performance metrics to be optimized. The next few sections will detail the steps necessary to define them and build response surface models for quick evaluation.

## 2.5.3 Inductance and Resistance Measurement



#### 2.5.4 Device Connection Setup (Example)

Although on the symbolic layout devices are represent as nodes (circles), in a real power module layout, these devices have real dimension and several connection pads. By default, there are no connections between these pads (usually a capacitance if this is a MOSFET). To give the user the flexibility to select different loops, the setup device connection feature is used to select virtual connections between any two pins of a given devices. For example, from the same electrical measurement above, we can setup 2 different loops.

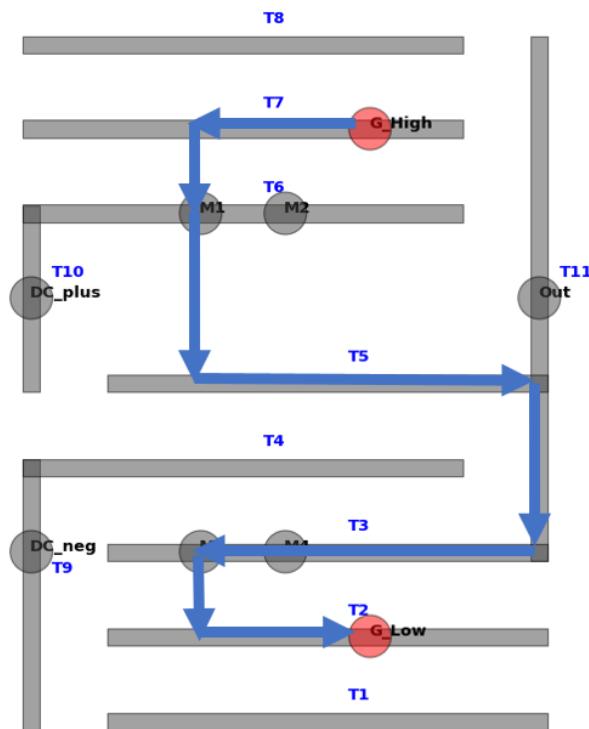
##### Loop 1:

Setup the device connections as follows:

Device ID	Connection 1	Connection 2	Connection 3
1 M3	<input checked="" type="radio"/> D-S	<input type="radio"/> G-S	<input checked="" type="radio"/> G-D
2 M4	<input type="radio"/> D-S	<input type="radio"/> G-S	<input type="radio"/> G-D
3 M1	<input checked="" type="radio"/> D-S	<input type="radio"/> G-S	<input checked="" type="radio"/> G-D
4 M2	<input type="radio"/> D-S	<input type="radio"/> G-S	<input type="radio"/> G-D

Ok

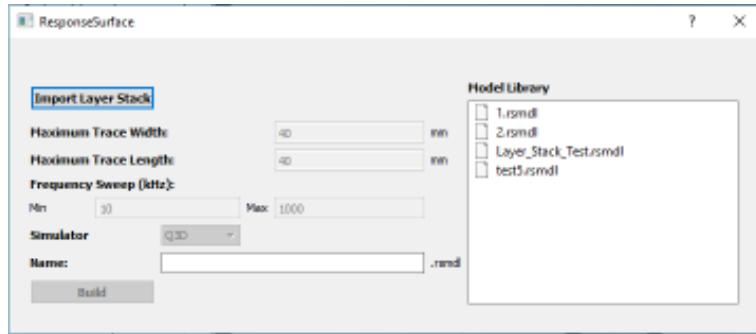
We now have the following loop:



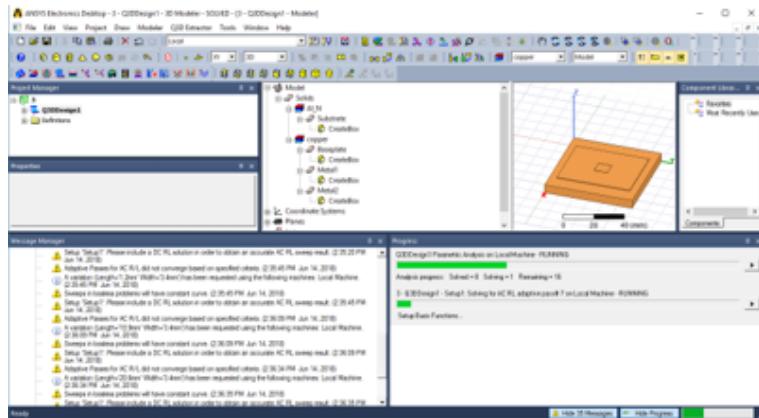
Name this loop as L1 and add this to the table.

## 2.5.5 Electrical Modeling

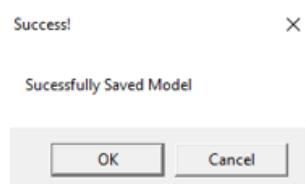
Under the electrical model selection on the UI, the analytical microstrip option can provide quick estimation of the inductance and resistance results. However, there are several drawbacks for this model such as not-frequency dependent, and usually less accurate for big traces. To overcome this problem, a response surface option is also provided. This model can be characterized using FastHenry or Q3D. To open the model creator, the user can go to: **Model -> Response Surface Setup**. A dialog as seen below is opened:



1. **Import Layer Stack:** this is explained in the Module Stack section below, this defines the baseplate and substrate dimensions. Different baseplate structures can affect the inductance calculation.
2. **Defining Maximum Trace Width and Length:** minimum trace width and length are based on minimum trace width in the Design Rule Check from PowerSynth (See Process Design Rules Editor). Define the maximum length and width here to characterize the model
3. **Defining Frequency sweep:** Specify the minimum and maximum frequency in KHz. The maximum frequency will define the minimum mesh in the characterization.
4. **Simulator:** 2 simulators are available now. These include ANSYS Q3D and FastHenry, the default ANSYS directory is: C:\Program Files\AnsysEM\AnsysEM18.2 (Versions up to 18.2 are supported). Another option is FastHenry (recommended), this is an open source parasitic extraction tool from MIT. The exe file for FastHenry is included in the package.
5. **Model name:** Model name can be specified by user. This will be later added to the model library on the right.
6. **Build:** Once everything is setup, hit “build” button. Depending on the Simulator choice, and maximum frequency, the model will be built within 15~30 minutes.

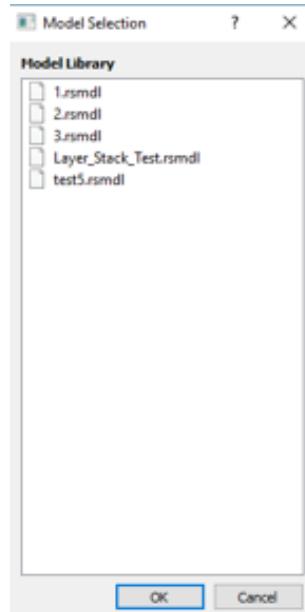


The simulation is automatically run in Q3D to characterize the model. If FastHenry simulation is selected this will be run in the back-end (Command Prompt) of the tool.

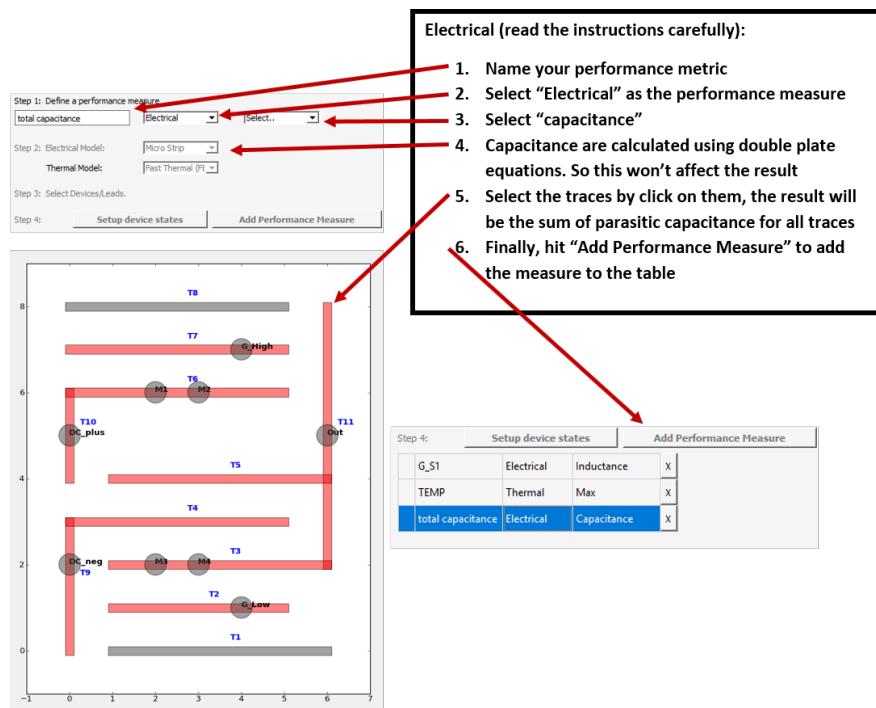


A dialog shows up when the simulations are done. Click Ok to go back to PowerSynth UI.

If the model is selected in the design performance selection, a dialog will be opened. The user can select the models from the list:



## 2.5.6 Capacitance



## 2.6 New Layout Engine (Experimental)

In this version, constraint-aware layout engine has been integrated with PowerSynth. To use this layout engine, the user must follow the steps up to 2.3.6. Then user needs to click on the button (marked with an arrow in Fig. 1) named “**Test New Layout Engine**” to explore the new layout engine.

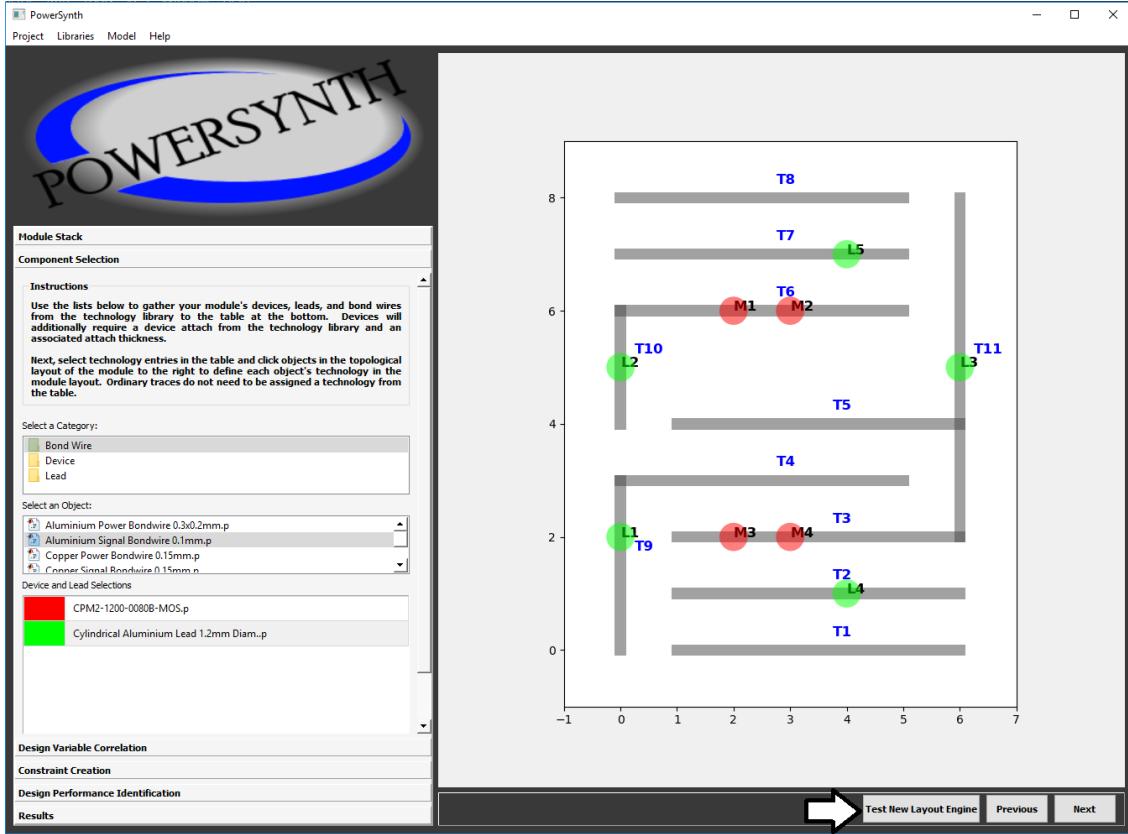


Figure 1: Start Window

### 2.6.1 New Layout Engine Dialog

Upon clicking on the button a new window will appear(shown in Fig. 6). The new window has four parts.

- **Generated Layout:** In this part, layout solution will be appeared.
- **Input (Initial) Layout:** Here, the initial layout that is converted from symbolic layout will appear. This is just rectangular representation of the symbolic lines and points objects.
- **Layout Selection:** This is the solution browser. Here, all solutions will be appeared as dots. Upon click on each dot corresponding layout will be shown in top left part.
- **Control Features:** In this part all information are shown and necessary input information are taken. Here, floorplan size of each layout, controlling features of new layout engine, different operating mode selection option are displayed.

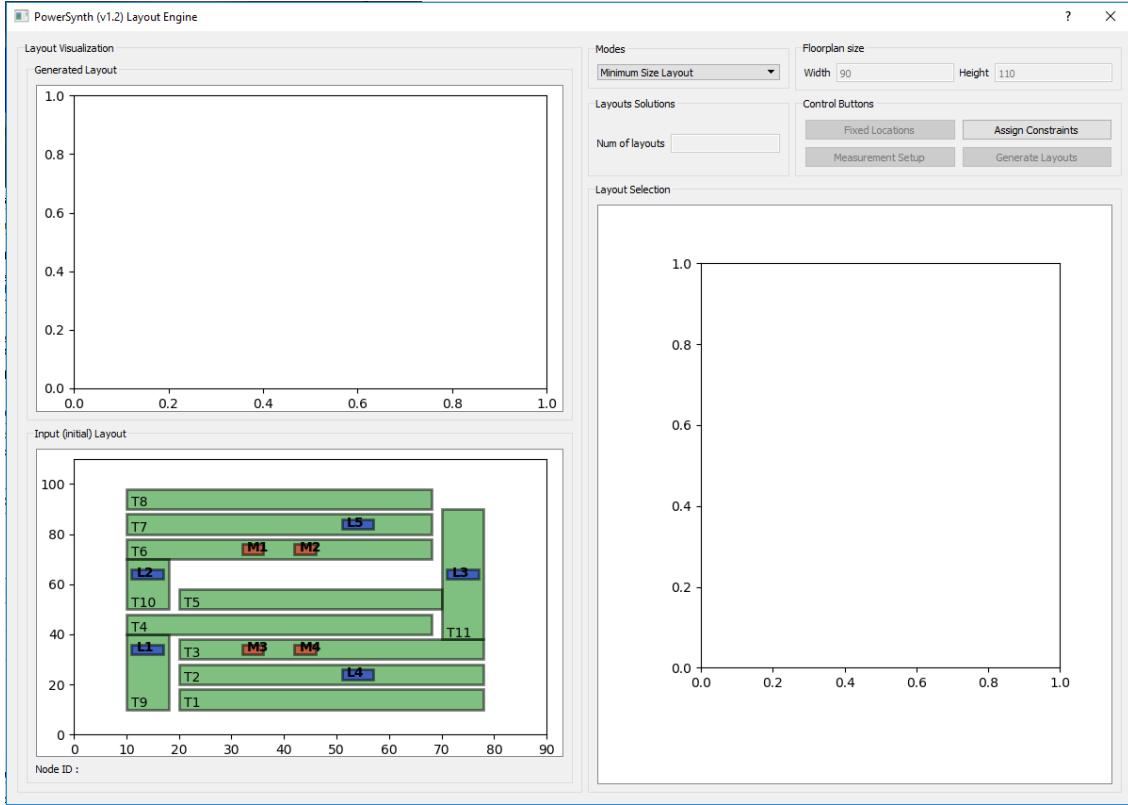


Figure 2: New Layout Engine Window

### 2.6.2 Assign Constraints

At the starting of the new layout engine the constraints must be assigned. To assign constraints, the “**Assign Constraints**” button should be clicked and ‘Constraints setup’ window will appear (shown in Fig. 3). There are three parts in the constraint setup: 1) Dimension Constraints, 2) Spacing Constraints, and 3) Enclosure Constraints. All constraints are automatically updated according to PowerSynth technology library. But the values can be manipulated by the user.

- **Dimension Constraints:** Here, minimum width along x-axis (Min Width), minimum width along y-axis and minimum enclosure are specified for each type of component. Currently, only trace, mos, diodes, and leads are considered.
- **Spacing Constraints:** In this table, minimum spacing values between every pair of components are declared.
- **Enclosure Constraints:** When a component is placed on top of another component, there may be some minimum enclosure value. So, this table has all possible minimum enclosure values.

When the constraints are set, “**Apply to layout**” button should be clicked to apply the constraint values. Besides the built-in constraint table user can also upload the table in the same format as a csv file by clicking on “**Load DRC**” and then “**Save DRC**” will save that data frame. Assign constraints is the first and the most important part for the layout engine. Without performing this step, layout solution generation is impossible.

Constraints setup

?

X

**Dimensions Constraints**

1	2	3	4	5	6
1 Min Dimensions	EMPTY	Trace	MOS	Lead	Diode
2 Min Width	2.0	1.2	3.36	1.2	0
3 Min Height	2.0	1.2	3.36	1.2	0
4 Min Extension	2.0	1.2	3.36	1.2	0

**Spacing Constraints**

1	2	3	4	5	6
1 Min Spacing	EMPTY	Trace	MOS	Lead	Diode
2 EMPTY	2	0	0	0	0
3 Trace	0	1.2	0	0	0
4 MOS	0	0	0.2	0	0
5 Lead	0	0	0.2	0.2	0
6 Diode	0	0	0	0.2	0.2

**Enclosure Constraints**

1	2	3	4	5	6
1 Min Enclosure	EMPTY	Trace	MOS	Lead	Diode
2 EMPTY	0	2.0	0	0	0
3 Trace	0	0	0.1	0.1	0.1
4 MOS	0	0	0	0	0
5 Lead	0	0	0	0	0
6 Diode	0	0	0	0	0

Apply to layout      Load DRC      Save DRC

Figure 3: Constraint Table

### 2.6.3 Measurement Setup

To generate layout solution, the performance metrics should be chosen. In this version, two types of measurements are included: electrical (loop inductance, capacitance, and resistance) and thermal (maximum, average, and std. deviation). The measurement setup is similar to the steps described in 2.5. The only difference is at a time only two performance metrics can be chosen at this stage. 3D- solution plot viewer is not available in this version

### 2.6.4 Modes

After setting up performance metrics, operating mode of layout engine should be selected. To select the mode of operation, the drop down list under “**Modes**” can be used. There are four options in the list and each option has different significance for the user. The list is shown in Fig. 4

- **Minimum Size Layout:** This layout is generated using all minimum constraint values. So, this layout reflects maximum possible power density for a layout. As this is the minimum sized

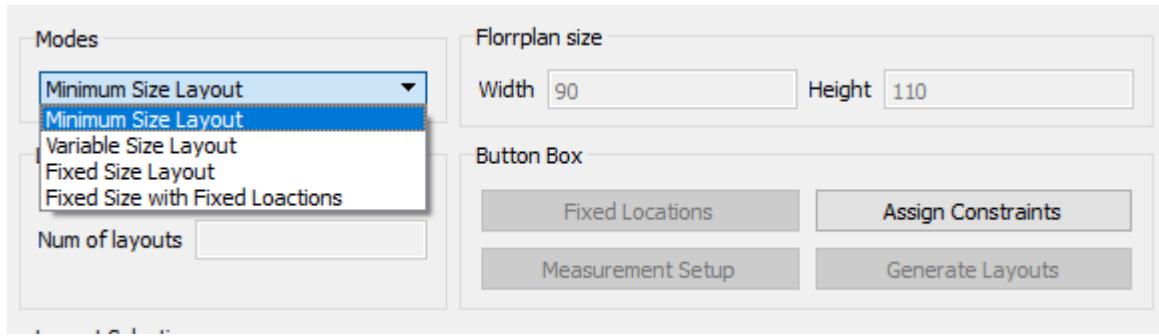


Figure 4: Modes

solution, it is electrically optimized but thermal performance is so poor.

- **Variable Size Layout:** If this mode is selected, all constraint values are randomized and new layout solution is generated. In this mode “**Num of Layouts**” field should also be given as input. This is the desired solution frequency. User can generate N number of valid layout solutions, where N is an integer given by user.
- **Fixed Size Layout:** To have fixed floorplan sized layout solutions, user should enter “**Width**” and “**Height**” along with “**Num of Layouts**”. Width and height correspond to floorplan size of each layout. All components are randomized within given area to generate N number of solutions.
- **Fixed Size with Fixed Locations:** This mode is useful for packaging purpose. If any component is to be always fixed at certain location throughout all solutions, this mode should be used. In this mode, “**Width**”, “**Height**”, and “**Num of Layouts**” must be given. Besides, one additional requirement is the “**Fixed Locations**”.

At a time one mode of operation should be selected to generate solution. How to perform different mode operations is shown in the later part using an example.

## 2.6.5 Generate Layouts

After completing each step stated above the “**Generate Layouts**” button should be clicked to generate solutions. Upon clicking this button, in the solution browser, solutions will appear as dots. By clicking on each dot the layout can be visualized in the **Layout Visualization** section of the window.

## 2.6.6 Test Case

The same case described in 2.2 is used for testing the new layout engine. The whole flow is shown sequentially.

To use new layout engine the input script must be in the same format described in 2.2. The name of the component must start with first letter of the component name (i.e., Trace-> T, MOSFET-> M, Lead-> L, and Diode-> D). In this version these four components are allowed to place in the floorplan.

Before clicking on the “**Test New Layout Engine**” button user must complete each steps up to “**component selection**”. At this stage the GUI will show the state shown in Fig. 5

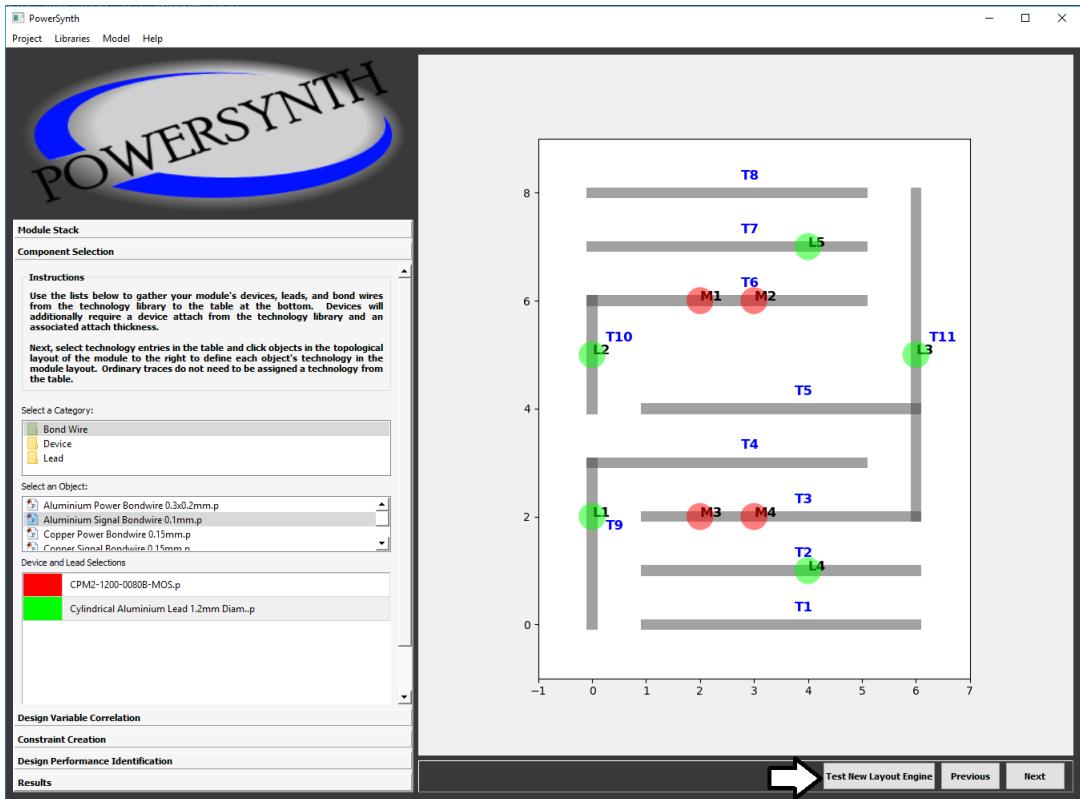


Figure 5: Where to start

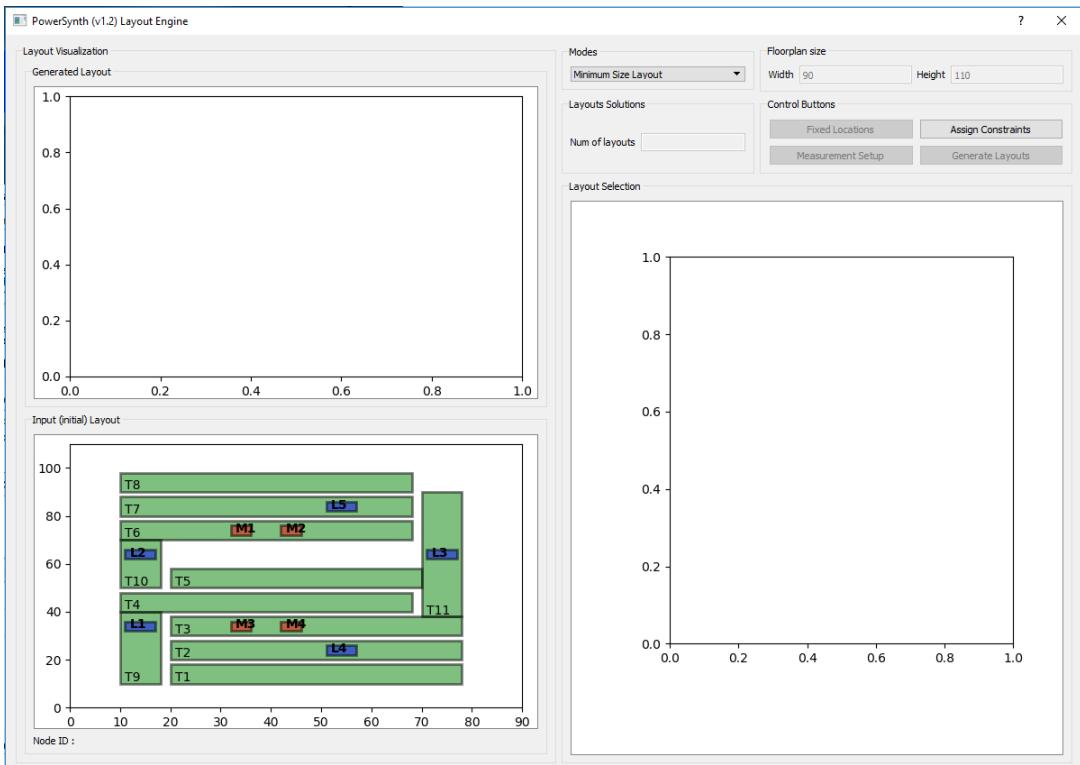


Figure 6: New Layout Engine Dialog

Constraints setup

Dimensions Constraints

	1	2	3	4	5	6
1	Min Dimensions	EMPTY	Trace	MOS	Lead	Diode
2	Min Width	2.0	1.2	3.36	1.2	0
3	Min Height	2.0	1.2	3.36	1.2	0
4	Min Extension	2.0	1.2	3.36	1.2	0

Spacing Constraints

	1	2	3	4	5	6
1	Min Spacing	EMPTY	Trace	MOS	Lead	Diode
2	EMPTY	2	0	0	0	0
3	Trace	0	1.2	0	0	0
4	MOS	0	0	0.2	0	0
5	Lead	0	0	0.2	0.2	0
6	Diode	0	0	0	0.2	0.2

Enclosure Constraints

	1	2	3	4	5	6
1	Min Enclosure	EMPTY	Trace	MOS	Lead	Diode
2	EMPTY	0	2.0	0	0	0
3	Trace	0	0	0.1	0.1	0.1
4	MOS	0	0	0	0	0
5	Lead	0	0	0	0	0
6	Diode	0	0	0	0	0

Apply to layout      Load DRC      Save DRC

Figure 7: Constraint Table

Now “Test New Layout Engine” button should be clicked and the window shown in Fig. 6 will appear.

The layout shown in the **Input (Initial) Layout** part is the rectangular version of the symbolic layout and input for the new layout engine. Now click on the “Assign Constraints” button to get the window shown in Fig. 7.

Let’s use the constraints set up by PowerSynth technology library. Just click on “Apply to Layout” button. Now the performance metrics should be chosen. Click on the “Measurement Setup” button and the window shown in Fig. 8 will appear.

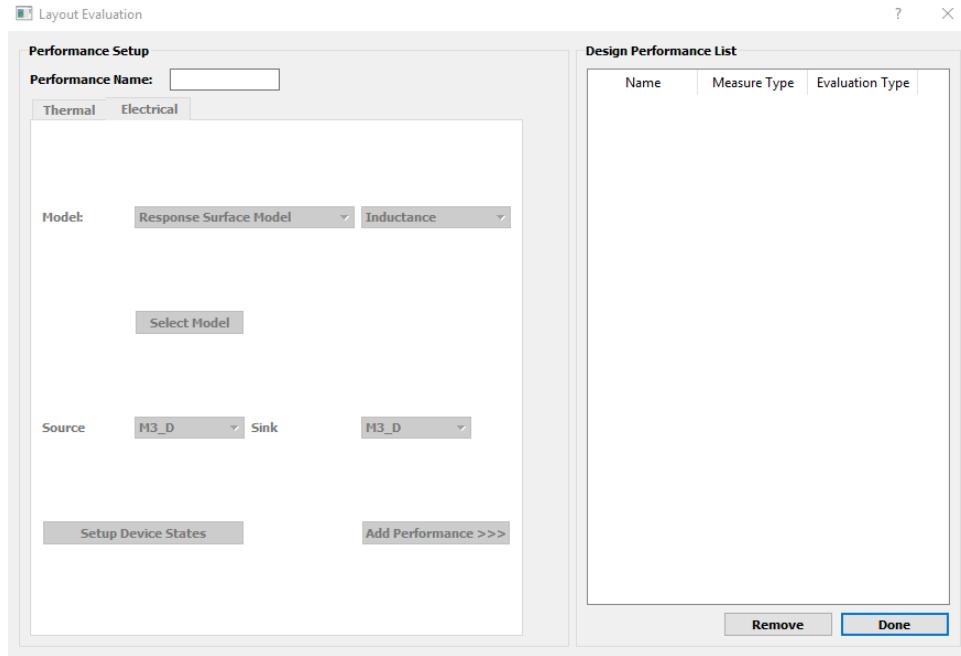


Figure 8: Performance Metrics Window

To start, the “**Performance Name**” field should be given. Let’s choose thermal performance and give name “**T1**” to evaluate the maximum temperature. To do so, after filling the name field click on the ”**Thermal**” tab. Choose **Analytical Rectangular Flux Model** to save characterization time and **Maximum** to evaluate the maximum temperature. The window will look like shown in Fig. 9

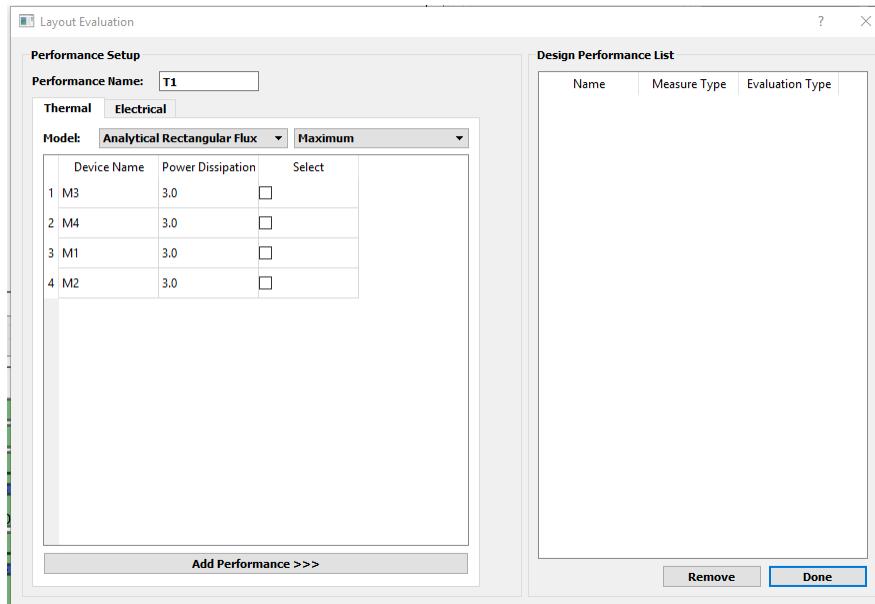


Figure 9: Thermal Metrics

To evaluate, click on the check boxes under **Select** column and then click on the “**Add Per-**

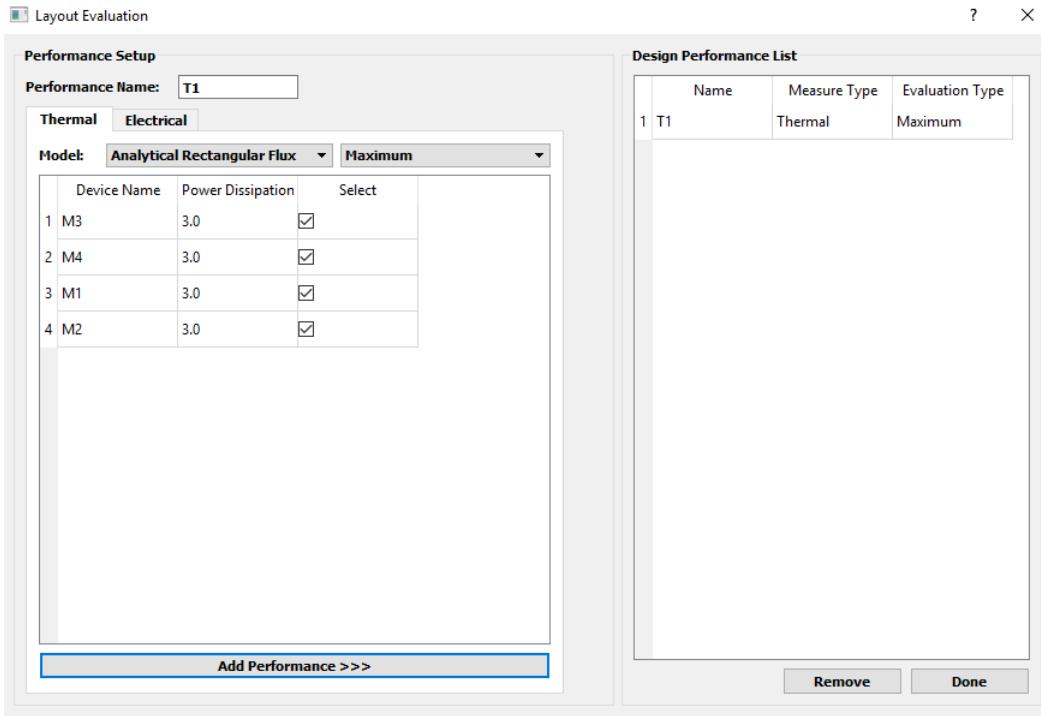


Figure 10: Updated Design Performance List

formance” button. By doing so, the “**Design Performance List**” table will be updated and the window will look like the figure shown in Fig. 10

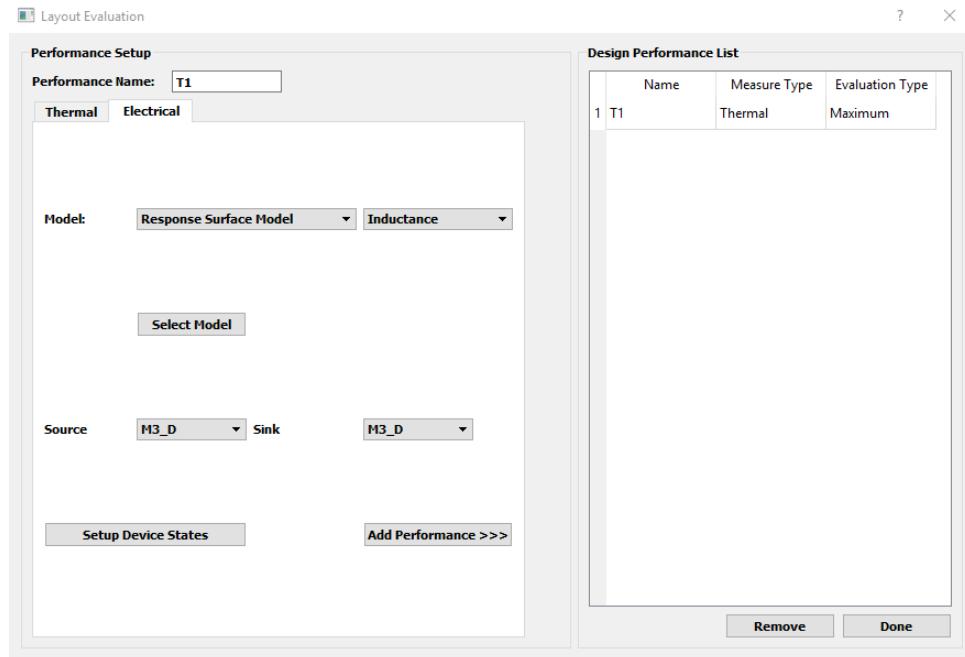


Figure 11: Interface for Electrical Performance Metrics

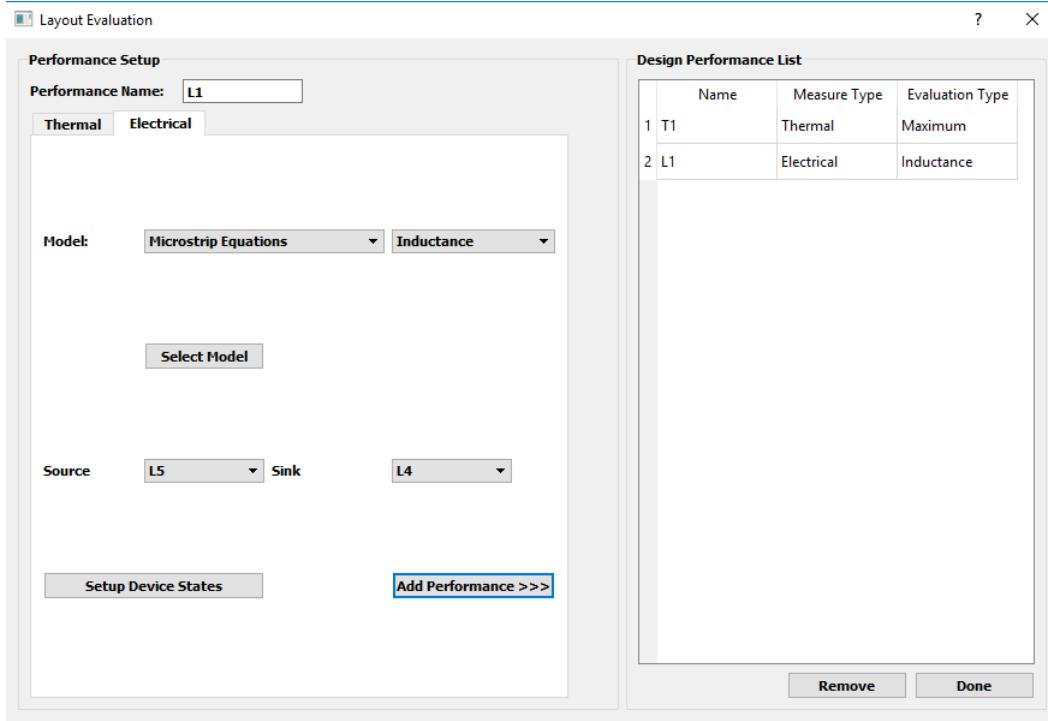


Figure 12: Final Performance Metrics Window Status

Now, electrical performance can be added by clicking on “**Electrical**” tab. The window will appear like the figure shown in Fig. 11.

Now update the “**Performance Name**” field and give all necessary information to evaluate electrical performance using drop down lists and finally update “**Design Performance List**” table by clicking on “**Add Performance**” button. Device states setup is same as described in 2.5.4. The connection depends on the path chosen by the user using **Source** and **Sink** drop down lists. In this version at a time two metrics can be compared. So, after updating **Design Performance Metrics** the window will look same as in Fig. 12

The “**Design Performance List**” table can be manipulated by using “**Remove**” button. However, only two metrics can be chosen in this version to have a trade off. After choosing performance metrics click “**Done**” button to save the setup.

Selecting modes is the next step. At first, to generate minimum-sized layout from the “**Modes**” dropdown list select “**Minimum Size Layout**”. Then click on the “**Generate Layouts**” button. By doing so, in the “**Layout Selection**” part, a dot will appear having inductance and temperature value in x and y axis respectively. In the “**Layout Visualization**” part corresponding solution layout will appear. The window will be same as shown in Fig. 13

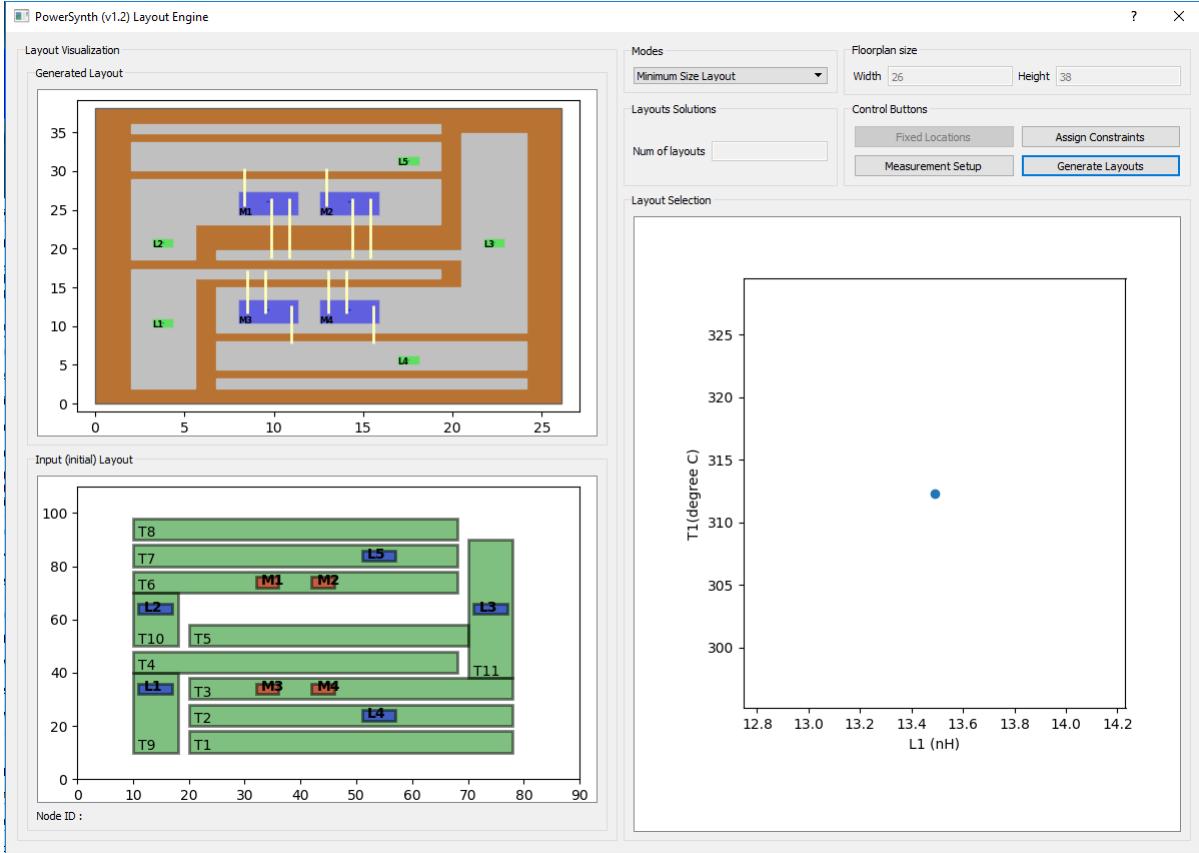


Figure 13: Minimum Size Layout

Now, to generate variable size layout solutions, choose “**Variable Size Layout**” from the “**Modes**” drop down list. This will enable the “**Num of Layouts** field”. Upon choosing variable floorplan size layouts one pop-up window will notify about thermal model. To continue press “**OK**” to that window. Put an integer value greater than 0 in the “**Num of Layouts** field”. To generate 20 layouts the control part will be same as shown in Fig. 14

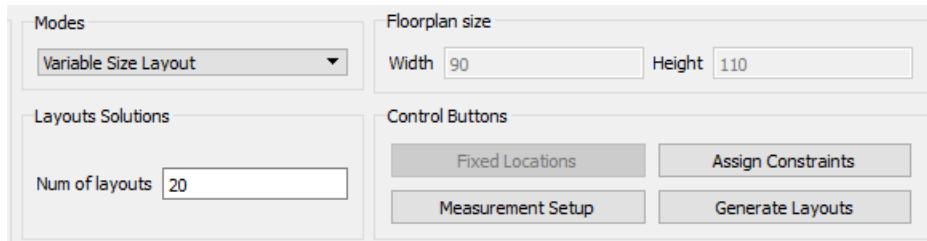


Figure 14: Variable Floorplan Size Setup

After clicking on “**Generate Layouts**” button, 20 dots will appear in the “**Layout Selection**” part and each dot’s inductance and temperature value can be found from the axes. Clicking on each dot, different solution will be shown on the “**Layout Visualization**” part. The solution set is shown in Fig. 15

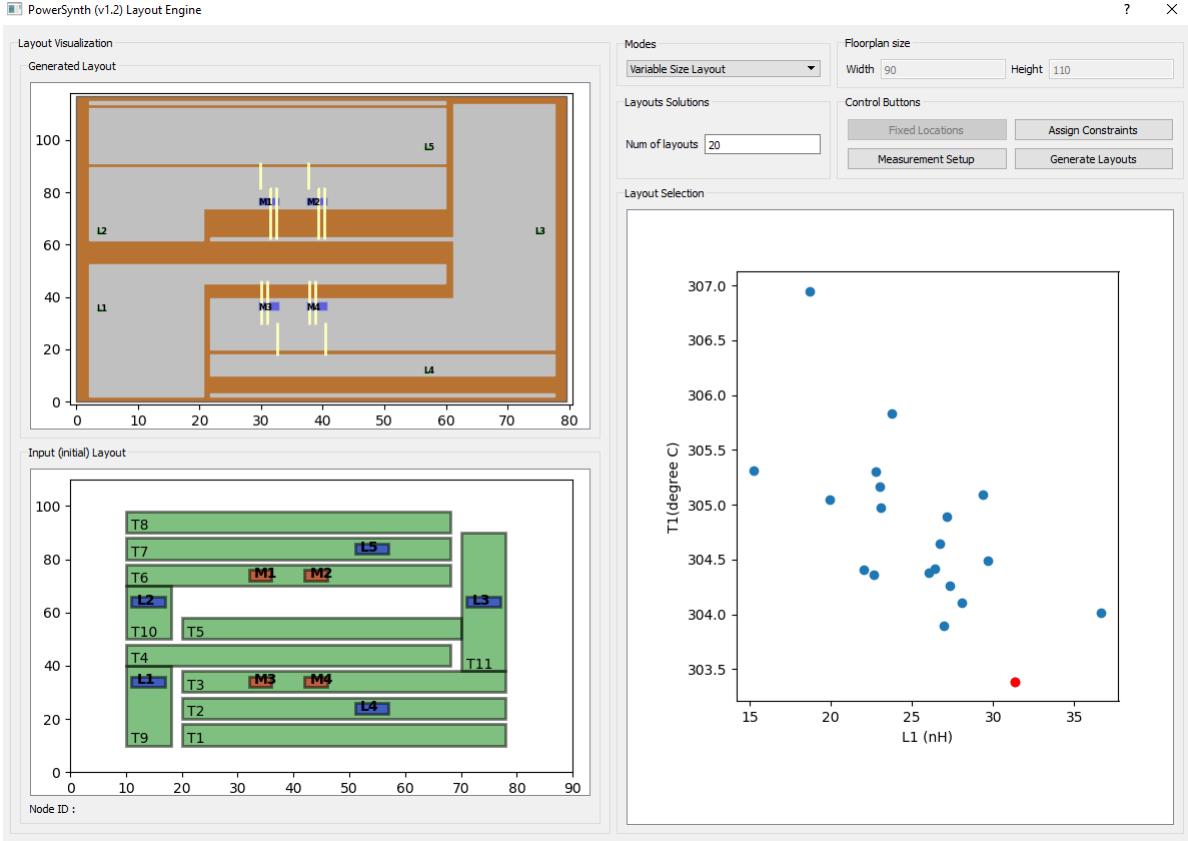


Figure 15: Variable Floorplan Size Solution

Now, to have fixed floorplan size layout solutions, choose “**Fixed Size Layout**” from “**Modes**”. This will enable Floorplan size fields. Put Width and Height value greater or equal the values found in minimum size layout solution.

In this example, we found Minimum Size Layout with Width=26 and Height=38. So, let's put 60 and 70 in the **Width** and **Height** field respectively. To generate 20 layout solutions the control part will look like the figure shown in Fig. 16

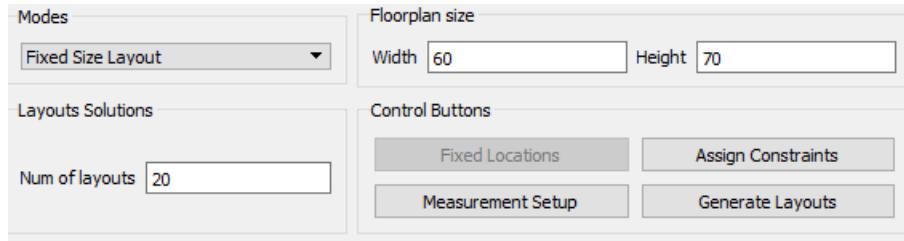


Figure 16: Fixed Floorplan Size Setup

Now by clicking on “**Generate Layouts**” button the window will look like the Fig. 17, when a solution is selected from “**Layout Selection**” part.

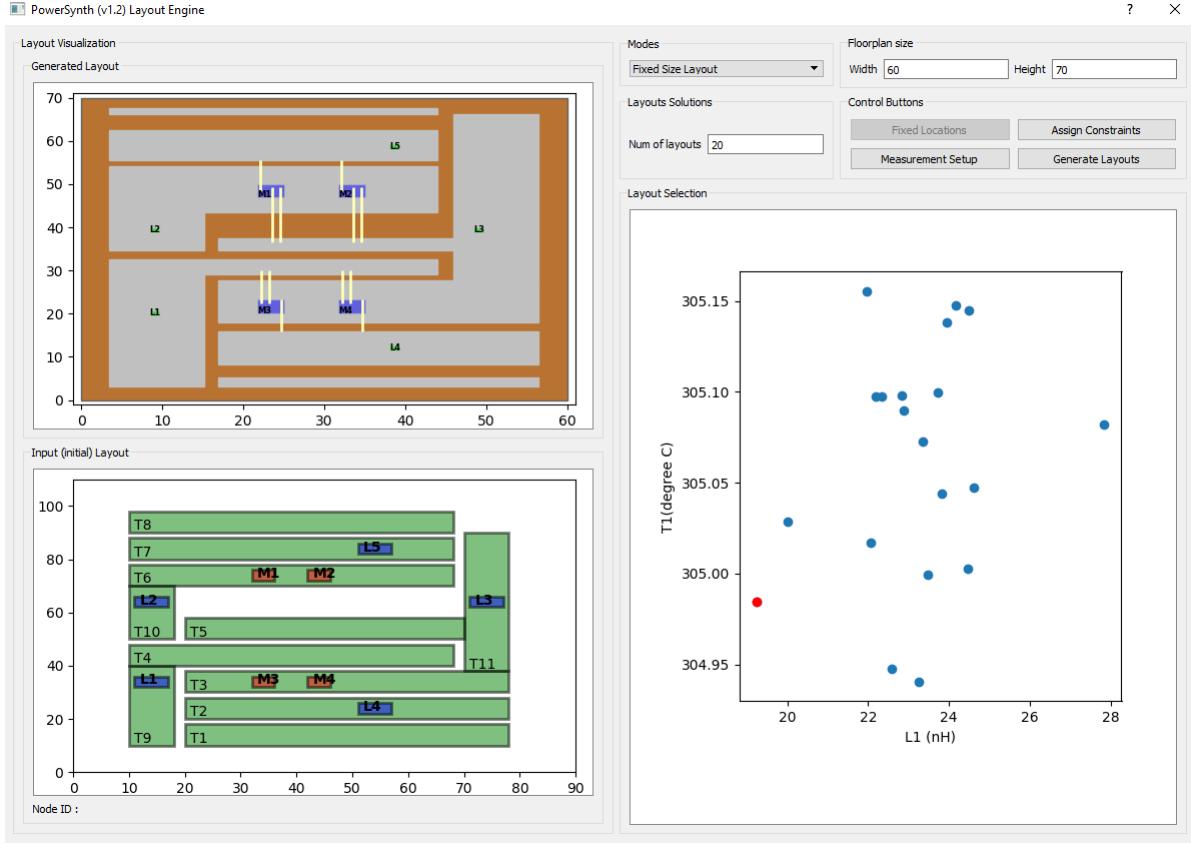


Figure 17: Fixed Floorplan Size Solutions

If the inductance and temperature values are compared with variable floorplan size results, it can be concluded that the later one has less variation than the first one as the later one has a fixed floorplan size.

Finally, to generate fixed floorplan with fixed component location layouts “**Fixed Size with Fixed Location**” is chosen from “**Modes**”. This will require all information same as the previous mode except now “**Fixed Locations**” button will be enabled. There will be two changes: one in **Control part** (shown in Fig. 18) and the other in **Input (Initial) Layout** (shown in Fig. 19).

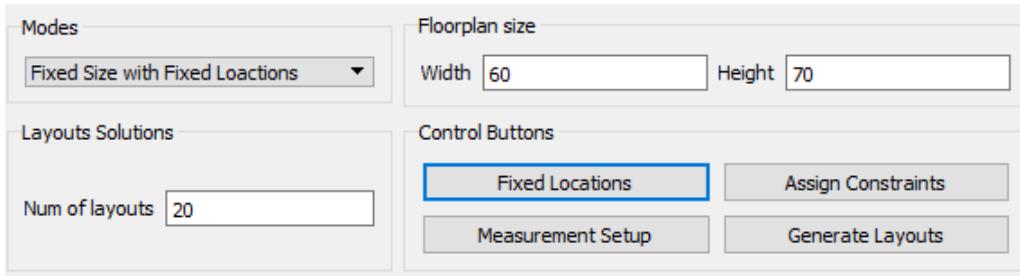


Figure 18: Fixed Floorplan with Fixed Component Location Setup

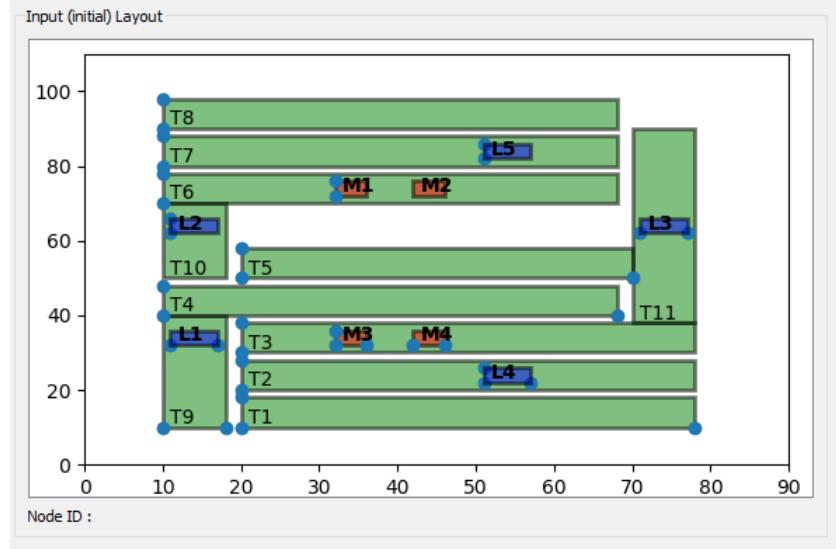


Figure 19: Initial Layout

In the control part, **Fixed Locations** button is now enabled and the locations of the nodes at which they are to be fixed must be given using this button. The **Input Layout** window has some clickable dots which are useful to map with Fixed Locations input using **Node ID** shown at the bottom. Upon clicking on different dots in the **Input Layout** window, corresponding **Node ID** is shown there. Using this Node ID fixed location table should be updated.

Upon clicking **Fixed Locations**" button, the window shown in Fig. 20 will appear.

Node ID	X Location	Y Location

Figure 20: Initial Layout

Here, **Node ID** drop down list is used to map **Node ID** from the parent window and **X** and **Y** fields are to give new location of that node. Either X or Y or both can be given to have a fixed location. In this implementation when a X coordinate is fixed at some location, the whole column is fixed at that location. Similarly, fixing a y co-ordinate will fix all nodes in the same row at that fixed location. By choosing a Node ID from the drop down list corresponding minimum location

will appear on “**Node min Locations**” label. User need to give X and or Y value greater than that minimum value. **But also user needs to be considerate about maximum value.** The value should be given in reasonable manner so that after setting that node’s location rest of the nodes have their minimum space in the rest of the area. If this rule is violated unexpected results can be found in the solution set.

In this example, let’s set up bottom left corner of the layout (Node at bottom left corner of T9) at position X=3 and Y=3, right edge of the L3 lead at X=55, and top edge of T8 at Y= 68. Also, let’s put 60 and 70 in the **Width** and **Height** field respectively and generate 20 solutions.

To set up first node location, the user needs to click on the node in the **Initial Layout** window and corresponding Node ID is shown at the bottom. (Follow Fig. 21)

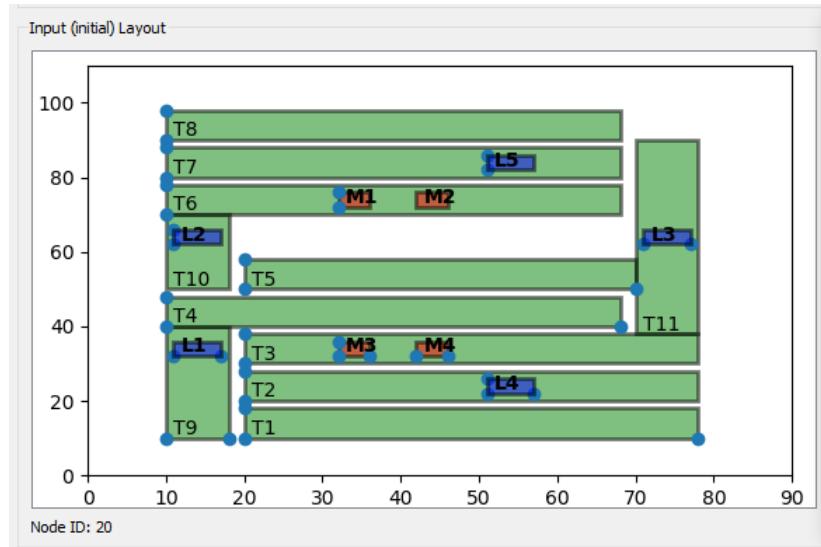


Figure 21: Finding Node ID

So, that node’s id is 20. Now from Fixed Location window find Node Id 20 from drop down list and set up X and Y coordinate in the respective fields by clicking **Add** button.(See Fig. 22 and Fig. 23)

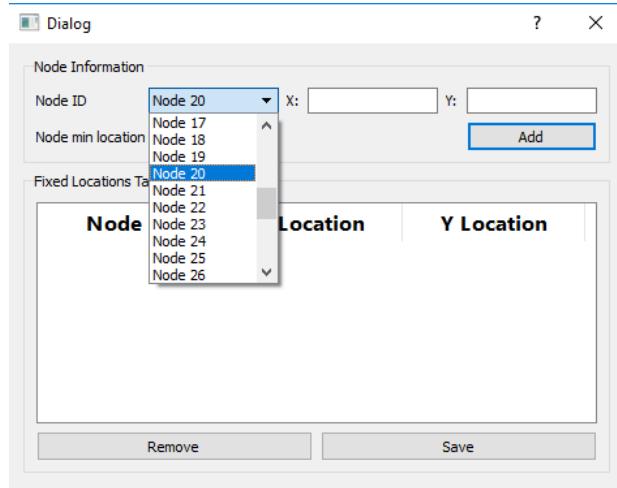


Figure 22: Inserting Node ID

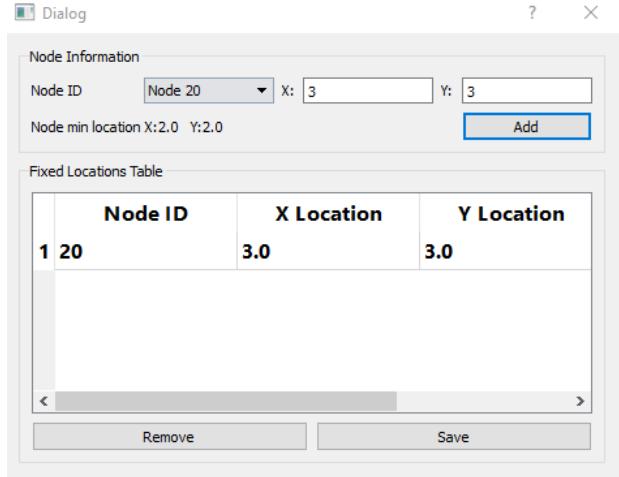


Figure 23: Inserting Fixed Locations

Similarly, click on each node from the layout window and map that using Node ID and put X,Y values and hit ADD button. By doing so for all 3 cases, the final table will look like Fig. 24

Node ID	X Location	Y Location
1 20	3.0	3.0
2 34	55.0	None
3 19	None	58.0

Figure 24: Completing Fixed Location Table

User can modify choice by using “Remove” button. Now, click on the “Save” button to save all fixed locations. Layout solutions can be found from solution browser by clicking "Generate Solutions" button. This may take some time depending on which nodes are chosen to be at fixed locations. Needs to wait until the solution browser is updated.

The solutions can be browsed in the same way as previous. The final window is shown in Fig. 25

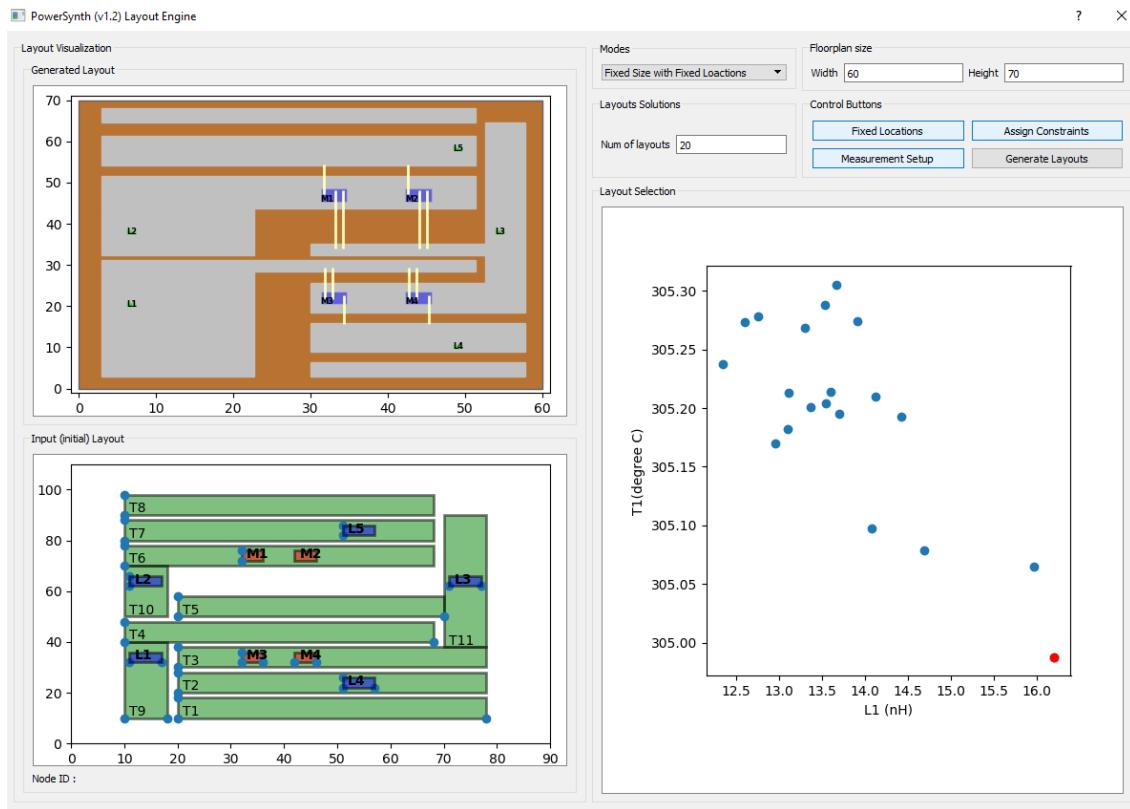
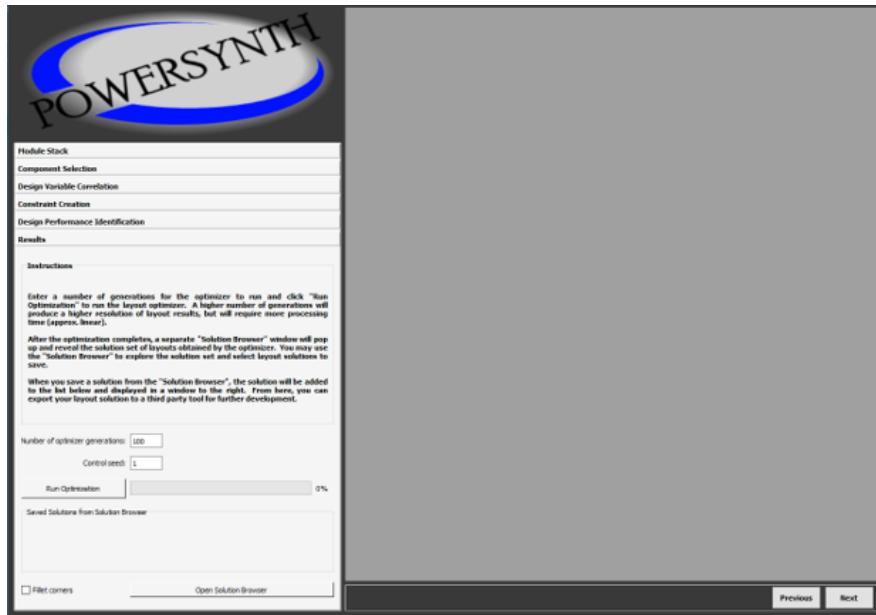


Figure 25: Fixed Location Solutions

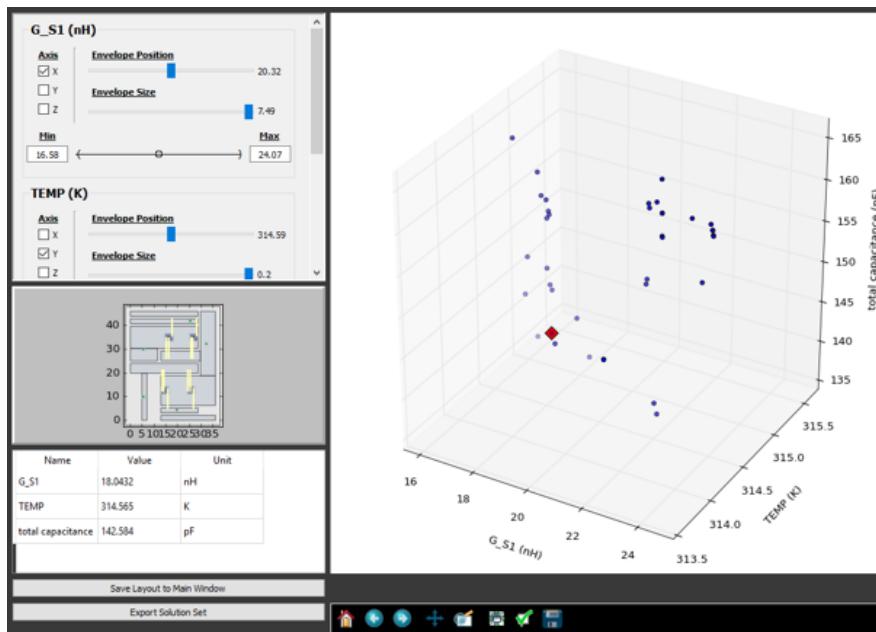
## 2.7 Optimization and Results

In this step, the user will need to specify number of generations. Since PowerSynth is based on a heuristic genetic algorithm, a higher number of generations will give you more solution choices. For this simple example 100 should be sufficient.

Click **Run Optimization**. The software will ask the user to save the project. Navigate to your specified project directory or any other directory to save this information. Note that the information from last run will be erased if it is not saved elsewhere. However, if the setup, number of generations, and the control seed (used for optimizer random generator) are kept the same, the final result will be the same. The runtime depends on number of generations specified. Upon completion, the solution window is opened as shown below.



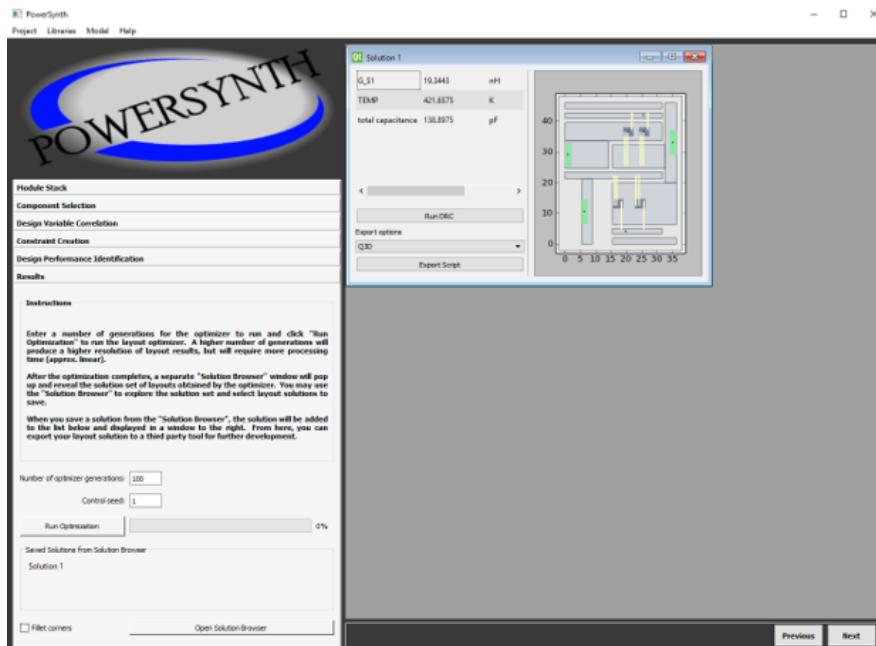
Check the console for progress updates. Once the optimizer routine is over, a new window should appear. Check your task bar if the window does not pop up. This is what the window may look like (depending on your unique solutions).



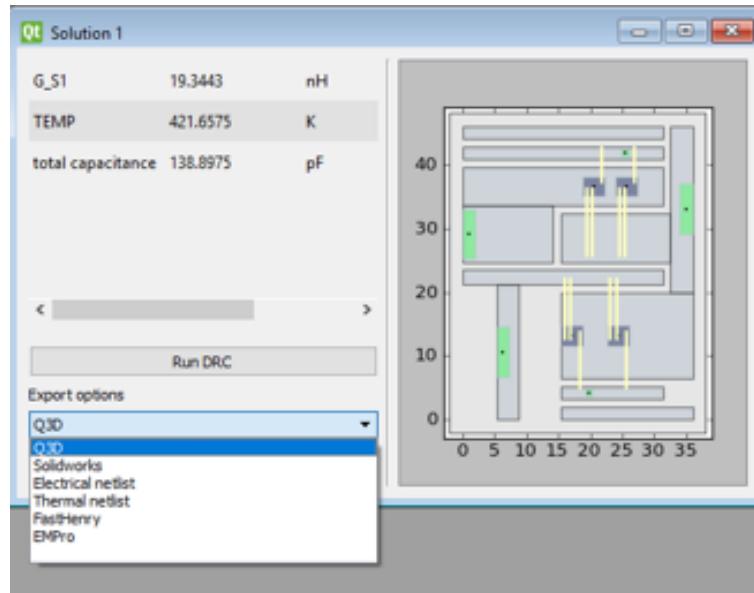
Left click and hold with your mouse inside the graph to rotate the graph. Choose the axes you wish to show using the pane on the left side (the scroll bar on the right will allow you to see more if they are not all visible). Each dot on the graph is a unique solution. Click on a solution and it will be colored red while displaying its preview on the left. Click on a different solution to see how the layout changes. The corresponding values for the objective functions are given below the layout preview.

To save the entire solution set, use the Export Solution Set button and save in .csv format. You can use Excel to open the file.

To save a solution for export into other tools or to see the E/T netlists, click on “Save Layout to Main Window.” You can enter a name for this solution. In this case it is “Solution 1.”



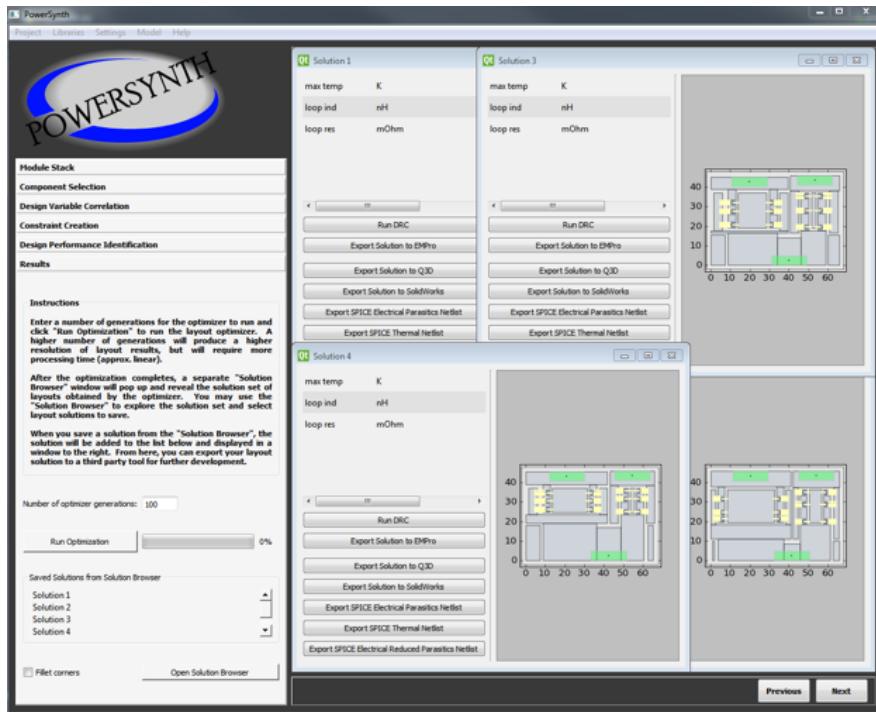
Under “Saved Solutions from Solution Browser” you can see Solution 1. The solution interface allows the user to export the solution to Q3D or SolidWorks. Other options allow the user to obtain the thermal and electrical netlists. The “Run DRC” button allow user to validate the design vs the Process Design Rule. To validate against different Process Design Rules see the section detailing the Process Design Rules Editor.



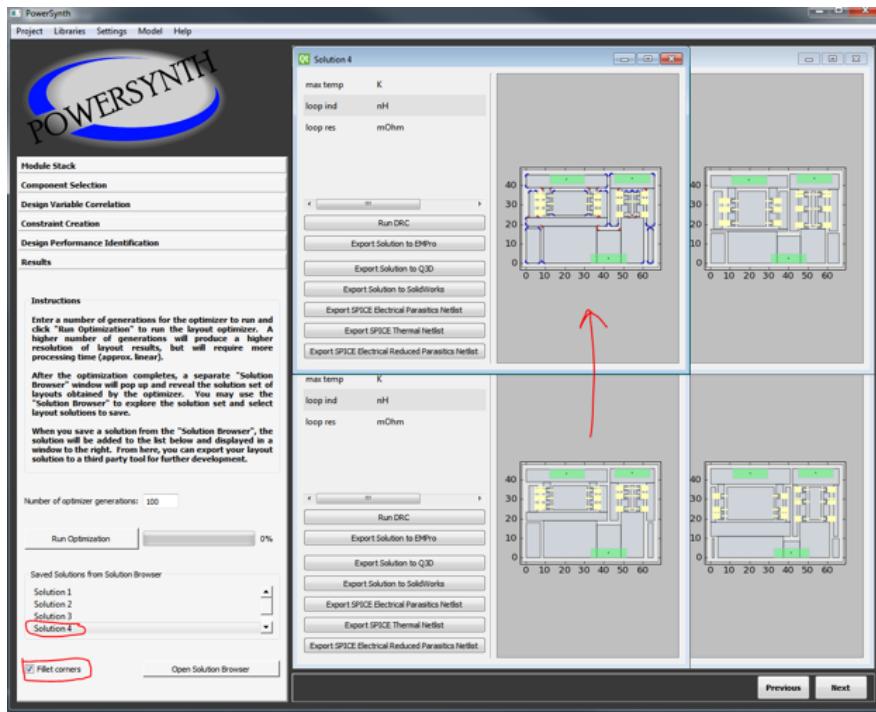
## 2.8 Post-Layout Optimization

PowerSynth allows the user to optionally apply corner correction to prevent electric field focusing and enhance thermo-mechanical reliability.

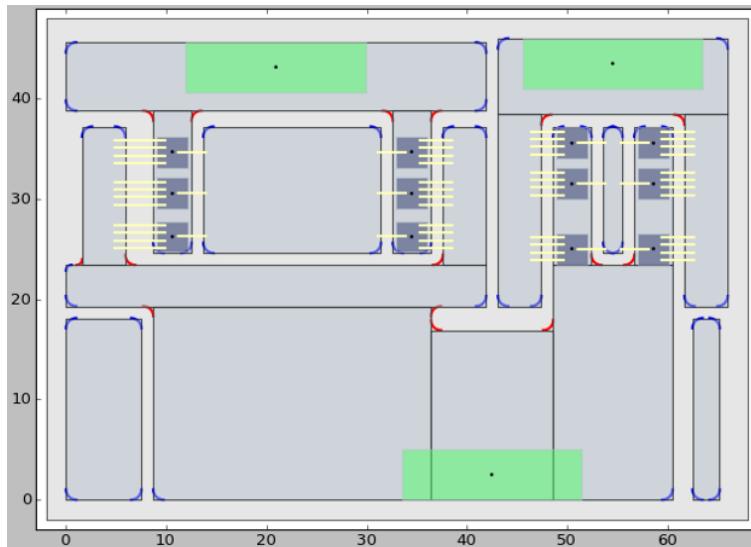
To apply fillets, in the Results tab, one may either check the ‘Fillet corners’ box, open the solution browser, and then select and save a solution, or alternatively, check the ‘Fillet corners’ box, and double click an existing solution under the ‘Saved Solutions from Solution Browser’ section to apply the fillets to an existing solution. For example, before applying fillets to solution 4:



And after applying fillets to solution 4, a new sub-window with the filleted solution appears:



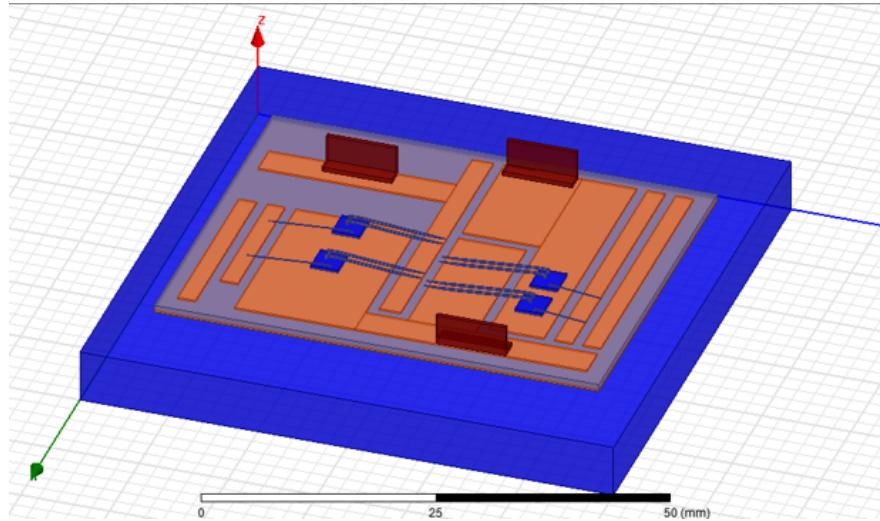
The arrow pointing up shows the same solution without fillets at the tail and with fillets at the head.



## 2.9 Exporting Saved Solutions

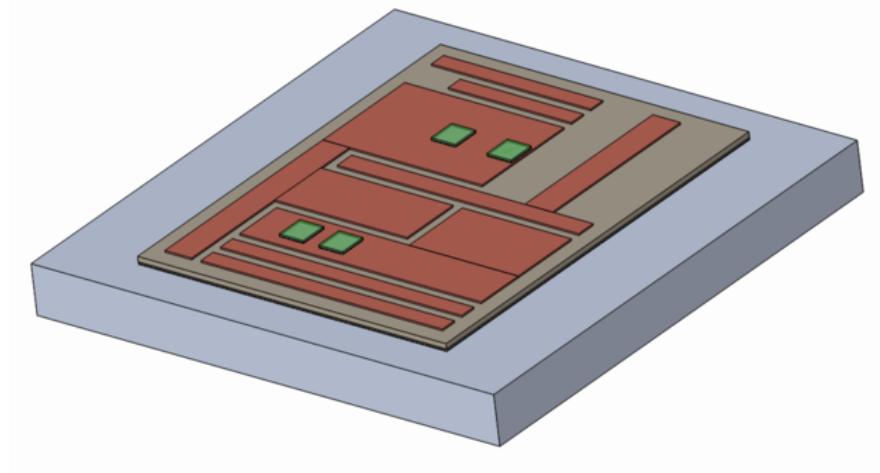
### 2.9.1 Export to ANSYS Q3D

Select Q3D from the export options list. Choose a directory, and create a file name. This will generate a .vbs file. In ANSYS Q3D open a new Q3D project. Go to **Tool-> Run Script** and load the exported .vbs file , the result is shown as below.



### 2.9.2 Export to SolidWorks

Choosing this option will open a dialog asking the user for their SolidWorks version. After typing the version (e.g. 2016) for the SolidWorks. Hit ok and choose an output directory. A \*.swp file is exported. However, this is not a binary file and can be somewhat troublesome to run this script. In SolidWorks, under Tools-> Macro select “New” (do not choose edit or run since the \*.swp from PowerSynth is just a text file, not binary). Copy and paste the text from the exported SolidWorks file and paste into the macro code editor. Finally press “RUN” (green triangular button).



### 2.9.3 Export SPICE Netlist

This will export a text file for thermal and electrical netlists. An example electrical netlist is shown below. This sub circuit netlist is in a SPICE format which is compatible with many circuit simulators. The user can use this along with any device file to do the analysis.

```
.subckt X1 M3_D M4_D M1_D M2_D G_Low M2_S DC_neg \
    DC_plus 00ut M2_G G_High M3_S M3_G M4_S M4_G M1_S M1_G
R0 M3_D 0018 0.000128325620465
L0 0018 M4_D 6.90843508845e-10
C0 M4_D 0 8.36813864105e-12
R1 M3_D 0019 6.20960837181e-05
L1 0019 0020 2.68348440987e-10
C1 0020 0 4.26631730709e-12
R2 0021 0022 2.1073578894e-05
L2 0022 0023 4.59520341299e-11
R3 0021 0024 1e-06
L3 0024 0025 1e-12
R4 0021 0026 0.000395244569043
L4 0026 0027 1.09343343808e-09
C4 0027 0 1.08826978588e-12
R5 0025 0028 0.0291101534176
L5 0028 M3_G 4.33e-09
R6 0029 0030 0.000206772456704
...
...
```

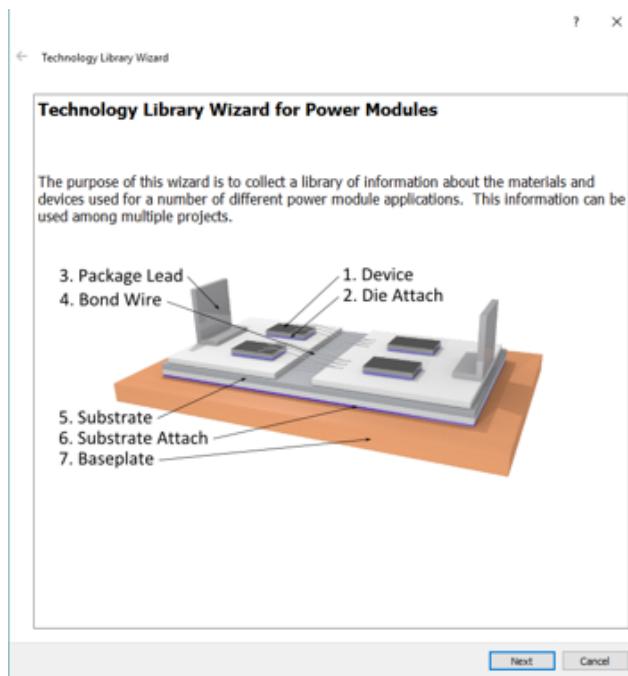
## 2.9.4 Export to Keysight EMPro

Please see the appendix for more detail.

# 3 Libraries and Editors

## 3.1 Technology Library Editor

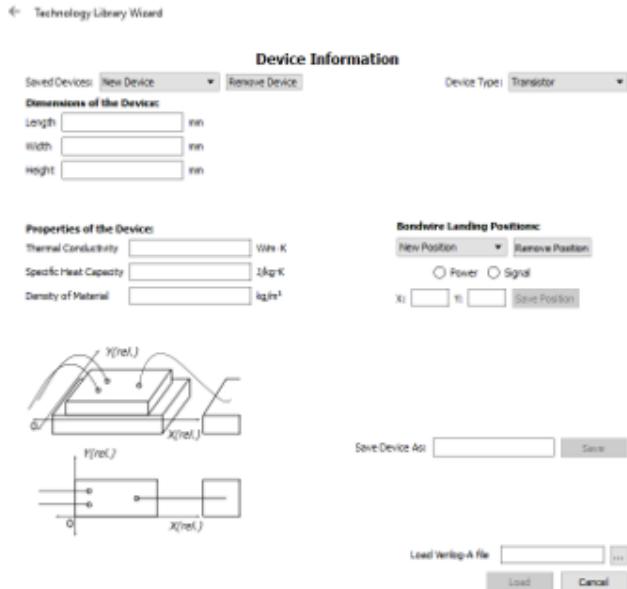
Under **Libraries**, select **Tech. Lib. Editor**. This allows the user to modify different technology files. The first page of the tech lib editor is shown on the right. Click the “Next” button to go through the pages of this wizard for creating or editing components.



### 3.1.1 Device Information

This page allows the user to input device information. This includes the dimension and material properties as well as the landing position for bondwires. The user can also input the Verilog A file for transistor/diode, while this information is not used in the optimization process, it will be included once the user exports the electrical netlist for a selected layout.

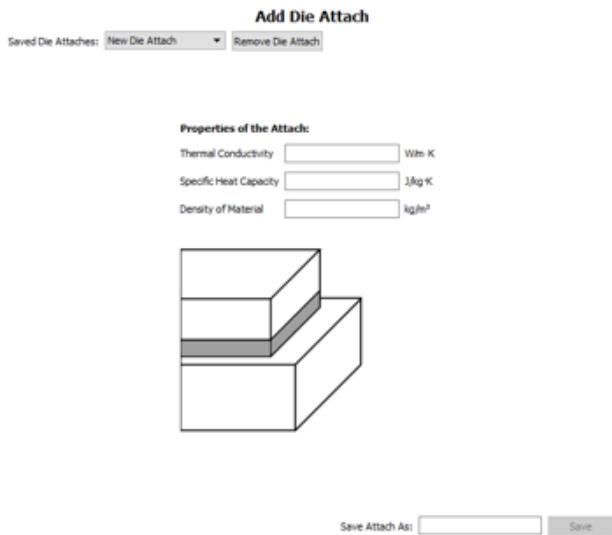
Click the “Save” button to save the new device to the library.



### 3.1.2 Add Die Attach

This page allows the user to assign the material properties for the die attach.

Click the “Save” button to save the new die attach file to the library.



### 3.1.3 Add Lead

This page allows the user to assign the material properties and dimensions for different lead types. In PowerSynth, this currently falls into two categories: “Round” and “Bus Bar leads.”

Click the “Save” button to save the new lead file to the library.

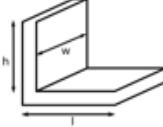
**Add Lead**

Saved Leads:

Type of lead:  Power  Signal  
Shape of lead:  Round  Bus Bar



Diameter:  mm  
Height:  mm



Length:  mm  
Width:  mm  
Height:  mm  
Thickness:  mm

Electrical Resistivity ( $\rho$ ):   $\Omega \cdot m$   
Save Lead as:

### 3.1.4 Add BondWire

This page allows the user to input dimensions and material properties for different bondwire types. The bondwire model is based on JDEC standards.

Click the “Save” button to save the new bondwire file to the library.

**Add Bondwire**

Saved Bondwires:

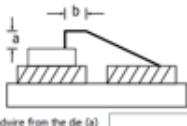
Type of bondwire:  Power  Signal  
Shape of bondwire:  Round  Ribbon



Diameter:  mm



Width:  mm  
Height:  mm



Height of bondwire from the die (a):  mm  
Fraction of bondwire total length (b):  mm

Electrical Resistivity ( $\rho$ ):   $\Omega \cdot m$   
Save Bondwire as:

### 3.1.5 Add Substrate

This page allows the user to input dimensions and material properties for the metal and isolation layers of DBC or DBA substrates.

Click the “Save” button to save the new file to the library.

**Add Substrate**

Saved Substrates:

**Dimensions of the Substrate:**

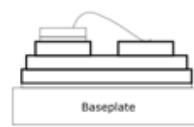
Dielectric Thickness  mm  
Metal Thickness  mm

**Metal Layer Properties:**

Thermal Conductivity  W/m K  
Specific Heat Capacity  J/kg K  
Electrical Resistivity  Ω·m  
Density of Material  kg/m<sup>3</sup>

**Isolation Layer Properties:**

Thermal Conductivity  W/m K  
Specific Heat Capacity  J/kg K  
Density of Material  kg/m<sup>3</sup>  
Relative Permittivity ( $\epsilon_r$ )   
Relative Permeability ( $\mu_r$ )



Save Substrate as:

### 3.1.6 Add Substrate Attach

This allows the user to assign the material properties for the substrate attach.

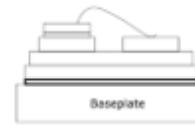
Click the “Save” button to save the new substrate attach file to the library.

**Add Substrate Attach**

Saved Substrate Attaches:

**Properties of the Attach:**

Thermal Conductivity  W/m K  
Specific Heat Capacity  J/kg K  
Density of Material  kg/m<sup>3</sup>



Save Substrate Attach as:

### 3.1.7 Add Baseplate

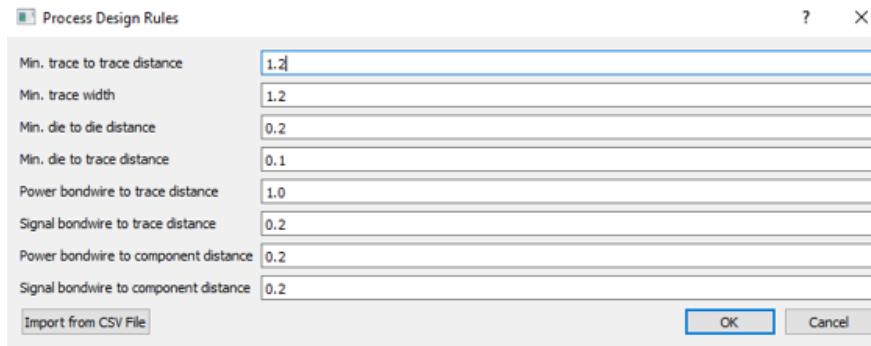
This allows the user to assign the material properties and dimensions for the baseplate.

Click the “Save” button to save the new baseplate file to the library.



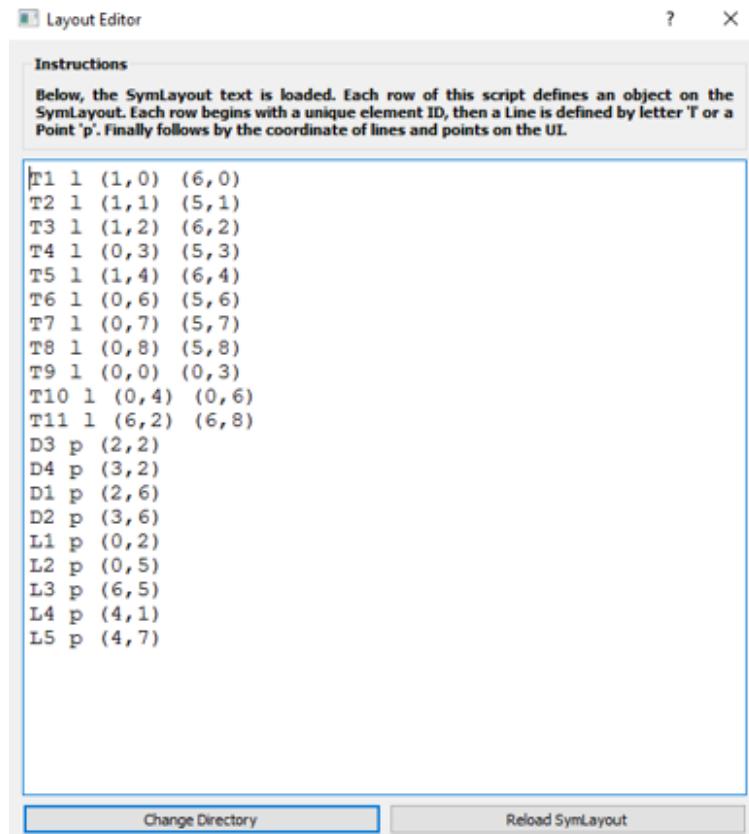
### 3.2 Process Design Rules Editor

The process design rules editor can be opened from **Project -> Design Rule Editors**. The interface below allows the user to input some design rule constraints for the layout. In the optimization process, candidate layouts that violate these rules are deemed as infeasible and will be eliminated from the solution space.



### 3.3 Layout Editor

The layout editor below allows the user to modify the symbolic layout. This can be found under **Project-> Open Layout Editor**. After the script is modified, click “Reload SymLayout” to load the new layout to the workspace.



The screenshot shows a Windows-style application window titled "Layout Editor". At the top right are standard window controls: a question mark icon, a close button, and a maximize/minimize button. Below the title bar is a toolbar with several icons. The main area contains a text editor with the following content:

```
T1 l (1,0) (6,0)
T2 l (1,1) (5,1)
T3 l (1,2) (6,2)
T4 l (0,3) (5,3)
T5 l (1,4) (6,4)
T6 l (0,6) (5,6)
T7 l (0,7) (5,7)
T8 l (0,8) (5,8)
T9 l (0,0) (0,3)
T10 l (0,4) (0,6)
T11 l (6,2) (6,8)
D3 p (2,2)
D4 p (3,2)
D1 p (2,6)
D2 p (3,6)
L1 p (0,2)
L2 p (0,5)
L3 p (6,5)
L4 p (4,1)
L5 p (4,7)
```

Below the text editor is a horizontal toolbar with two buttons: "Change Directory" and "Reload SymLayout".

## 4 PowerSynth-Related Publications

This section contains a list of all the current publications related to PowerSynth as of the date of this document.

1. P. Tucker, "SPICE netlist generation for electrical parasitic modeling of multi-chip power module designs," 2013.
2. B. W. Shook, A. Nizam, Z. Gong, A. M. Francis and H. A. Mantooth, "Multi-objective layout optimization for multi-chip power modules considering electrical parasitics and thermal performance," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, 2013.
3. B. W. Shook, Z. Gong, Y. Feng, A. M. Francis and H. A. Mantooth, "Multi-chip power module fast thermal modeling for layout optimization," *Computer-Aided Design and Applications*, vol. 9, pp. 837-846, 2012.
4. B. W. Shook, "The Design and Implementation of a Multi-Chip Power Module Layout Synthesis Tool," 2014.
5. J. Main, "A Manufacturer Design Kit for Multi-Chip Power Module Layout Synthesis," 2017.
6. Q. Le, T. Evans, S. Mukherjee, Y. Peng, T. Vrotsos and H. A. Mantooth, "Response surface modeling for parasitic extraction for multi-objective optimization of multi-chip power modules (MCPMs)," in *Wide Bandgap Power Devices and Applications (WiPDA), 2017 IEEE 5th Workshop on*, 2017.
7. Q. Le, S. Mukherjee, T. Vrotsos and H. A. Mantooth, "Fast transient thermal and power dissipation modeling for multi-chip power modules: A preliminary assessment of different electro-thermal evaluation methods," in *Control and Modeling for Power Electronics (COMPEL), 2016 IEEE 17th Workshop on*, 2016.
8. Z. Gong, "Thermal and electrical parasitic modeling for multi-chip power module layout synthesis," 2012.
9. T. Evans, Q. Le, S. Mukherjee, I. Al-Razi, T. Vrotsos, Y. Peng and H. A. Mantooth, "PowerSynth: A Module Layout Generation Tool," Manuscript submitted to *IEEE Transactions on Power Electronics* April 2018.
10. S. Mukherjee et al, "Toward Partial Discharge Reduction by Corner Correction in Power Module Layouts," in *Control and Modeling for Power Electronics (COMPEL)*, 2018.

## 5 Appendix 1: EMPro Export

### 5.1 Introduction

The EMPro Export feature in PowerSynth allows a user to export designs generated by PowerSynth for further analysis in Keysight's EMPro and ADS. This document presents an overview of the capabilities available after export as well as the process in doing so. Furthermore, while this document provides a walkthrough of some of the key points for usage, it is assumed that the user is familiar with Keysight EMPro and ADS.

#### 5.1.1 Functionality

This feature of PowerSynth takes a layout design from PowerSynth and generates a script to be run in EMPro. This script automatically defines the simulation type and frequency range, draws all of the design components and assigns materials, and sets up all of the requisite ports for simulation.

Exporting a design generated by PowerSynth to EMPro grants the user several capabilities for further analysis of a given design. These include, but are not limited to:

- S-Parameter modeling of a design
- Near and far field visualization
- Export to ADS for:
  - Incorporation of Verilog-A device models
  - Transient switching analysis
  - Conducted EMI analysis
  - Near field visualization of transient results

#### 5.1.2 Caveats and Limitations in Current Release

Currently PowerSynth assumes a module buildup consisting of:

- Heat spreader
- Substrate attach
- DBC-type substrate (Cu-ceramic-Cu)
- Die attach
- Device
- Wire bonds

This stackup is fixed in the current release and so the resulting model in EMPro reflects this. However, future versions of the tool will allow greater flexibility.

During the export, the thin attachment layers are neglected to allow for easier meshing. Additionally, devices are not physically modeled. Instead, pads corresponding to those of the devices are inserted and wire bonds are connected to them. This is done so that only the parasitics of the module are extracted. Later, in circuit simulators such as ADS, the user can insert a device model of their choosing into the corresponding ports inside the extracted layout parasitics model.

Table 2: Component Material Assignments

<b>Component</b>	<b>Material</b>
Heat Spreader	Aluminum
Traces	Copper
Ceramic	Alumina
Device Pads	PEC
Wire Bonds	Aluminum

Furthermore, materials are automatically assigned to components as shown below, but may be easily changed within EMPro.

As noted above, many of these issues related to the current limitations and assumptions in PowerSynth are currently being revised. As of this writing, a new layout engine is being developed to overcome them and provide even greater flexibility in design. The reader's patience is greatly appreciated as development of PowerSynth continues.

Finally, this feature and document were made using the 2017 versions of EMPro and ADS. Future version compatibility will be ensured. However, compatibility with previous versions has not been tested nor can it be guaranteed.

## 5.2 Exporting from PowerSynth

Once a design has been selected from PowerSynth, exporting the EMPro script is a straight forward task. This section will cover the steps necessary for exporting only and assumes that PowerSynth has been setup, run, and the user has been presented with design solutions. Please refer to the main PowerSynth manual for information on how to perform these steps.

### 5.2.1 Selecting a Design

After PowerSynth completes the optimization routine, the user is presented with a solution as shown in Figure 26. From here, select a design and click on the button "Save Layout to Main Window" then return to the main PowerSynth window.

### 5.2.2 Saving the EMPro Script

In the main window, find the sub-window containing the design that is to be exported. From there, click on the button titled "Export Solution to EMPro" as shown in Figure 27. You will then be presented with a dialog box asking you to specify a name and location for the python script which can be used in EMPro like in Figure 28. The next section will cover how to import the file into EMPro.

## 5.3 Importing to EMPro

Upon saving EMPro script, the file can be opened with EMPro to setup the model and simulation. The following steps provide more detail on these tasks.

### 5.3.1 Creating a New Project

First, open EMPro. Then select "New Project" from the file menu. Here, choose "Generic FEM, design in mm" as shown in Figure 29. Set the frequency ranges to be simulated and press "OK."

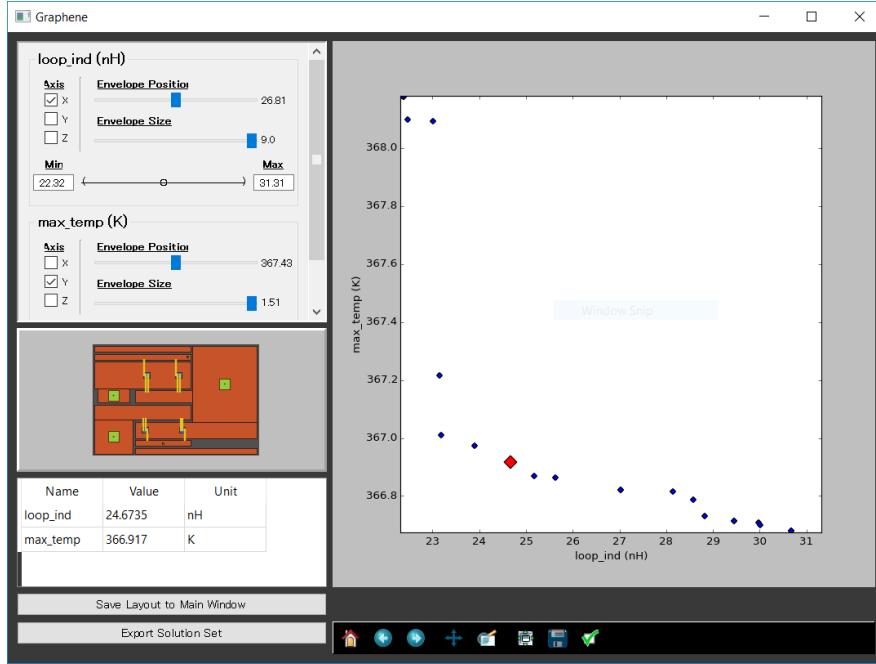


Figure 26: Selecting a design from the solution browser window and saving to the main PowerSynth one.

### 5.3.2 Running the Script

Next, open the scripting pane in EMPro. From here choose to create a new script from the file menu as in Figure 30. Open the script in an external text editor and copy the entire code, then paste it into the new script window in EMPro that was just created. Finally, press the execute script button (Figure 31) and wait until it completes.

Once the script has finished running, you will see the components fully modeled and populated in the main window like in Figure 32. Now the project is ready for simulation.

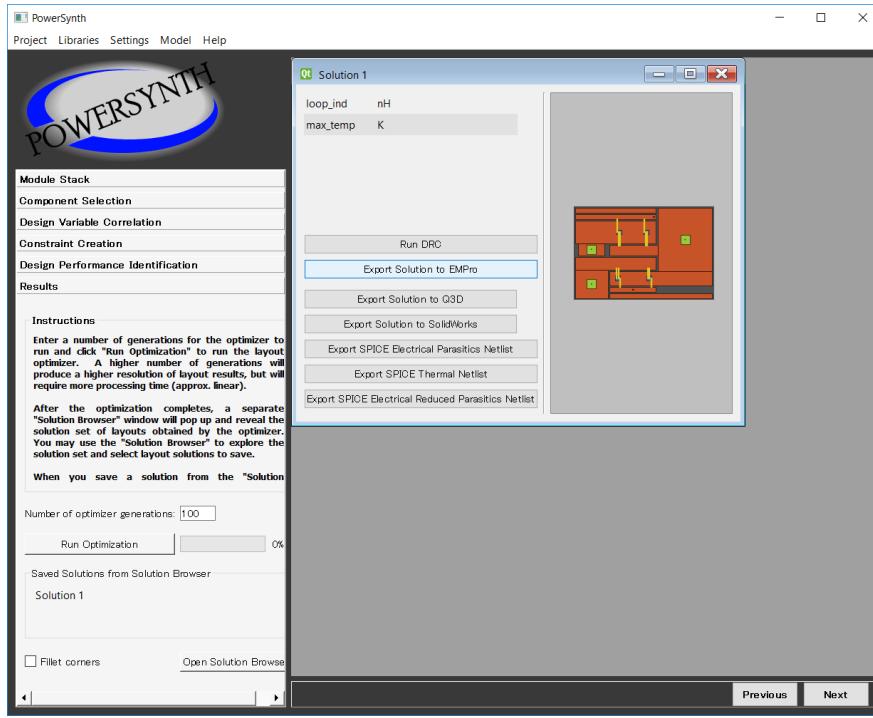


Figure 27: Exporting the design to an EMPro Python script.

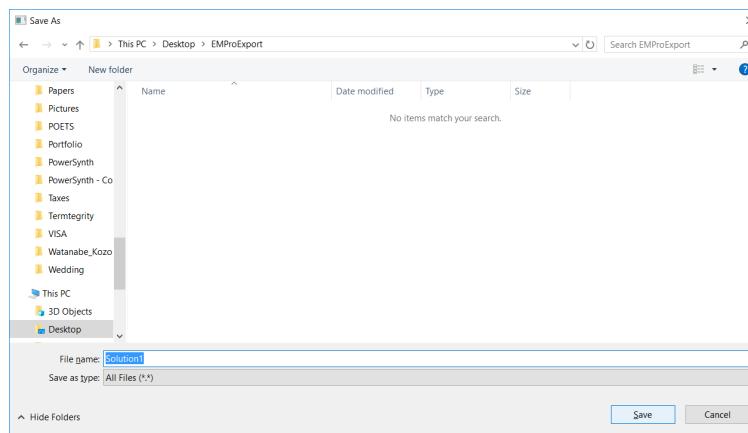


Figure 28: Specifying the file name for export to EMPro.

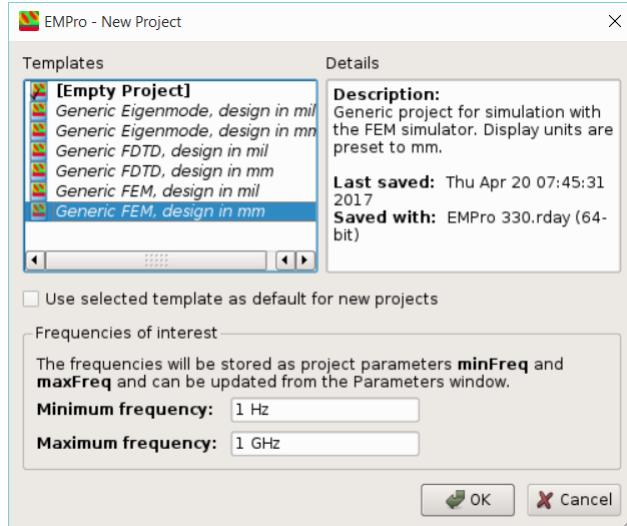


Figure 29: Creating a new EMPro Project.

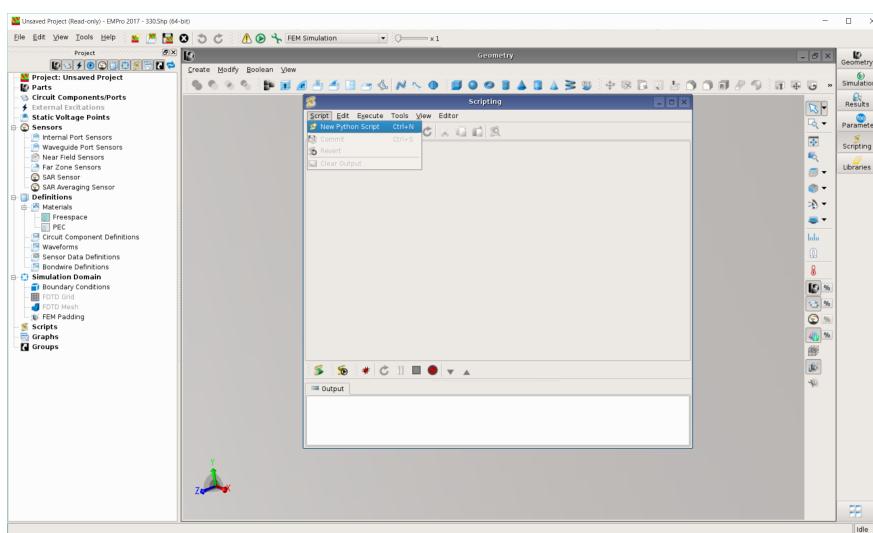


Figure 30: Creating a new script.

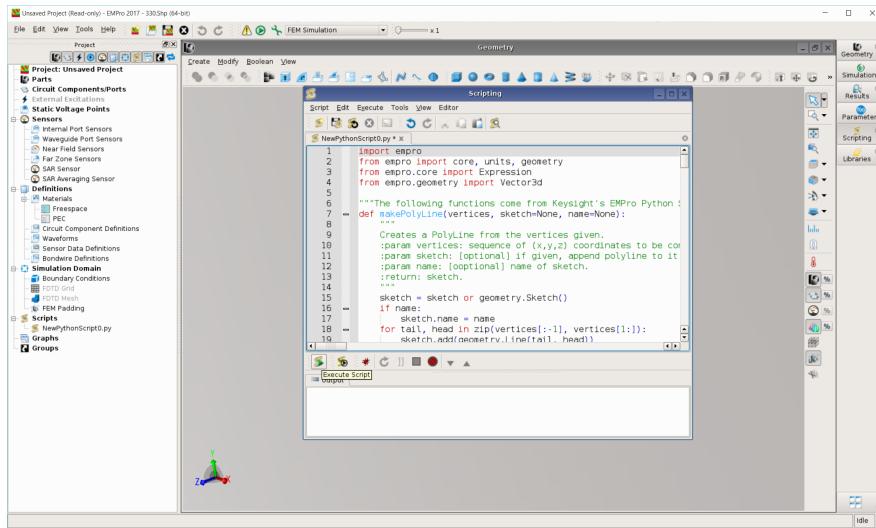


Figure 31: Executing the script.

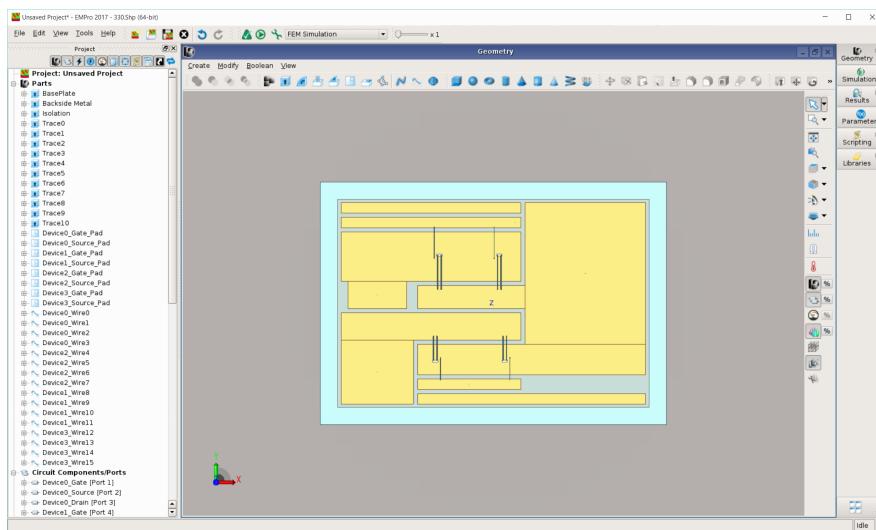


Figure 32: EMPro project creation completed.