

1. Description

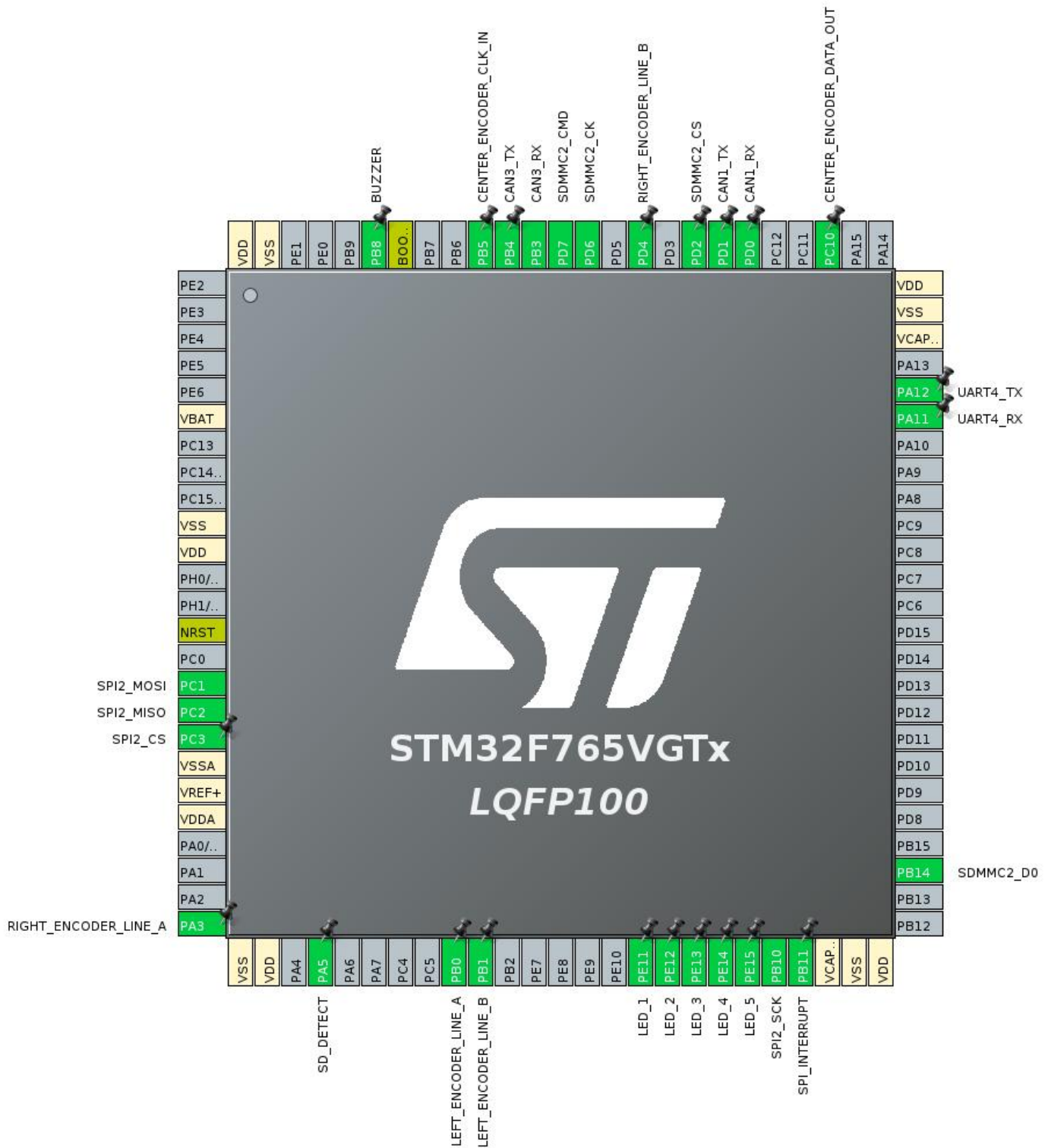
1.1. Project

Project Name	ECU_BRAINv2_VSC
Board Name	custom
Generated with:	STM32CubeMX 5.6.0
Date	05/09/2020

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x5
MCU name	STM32F765VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



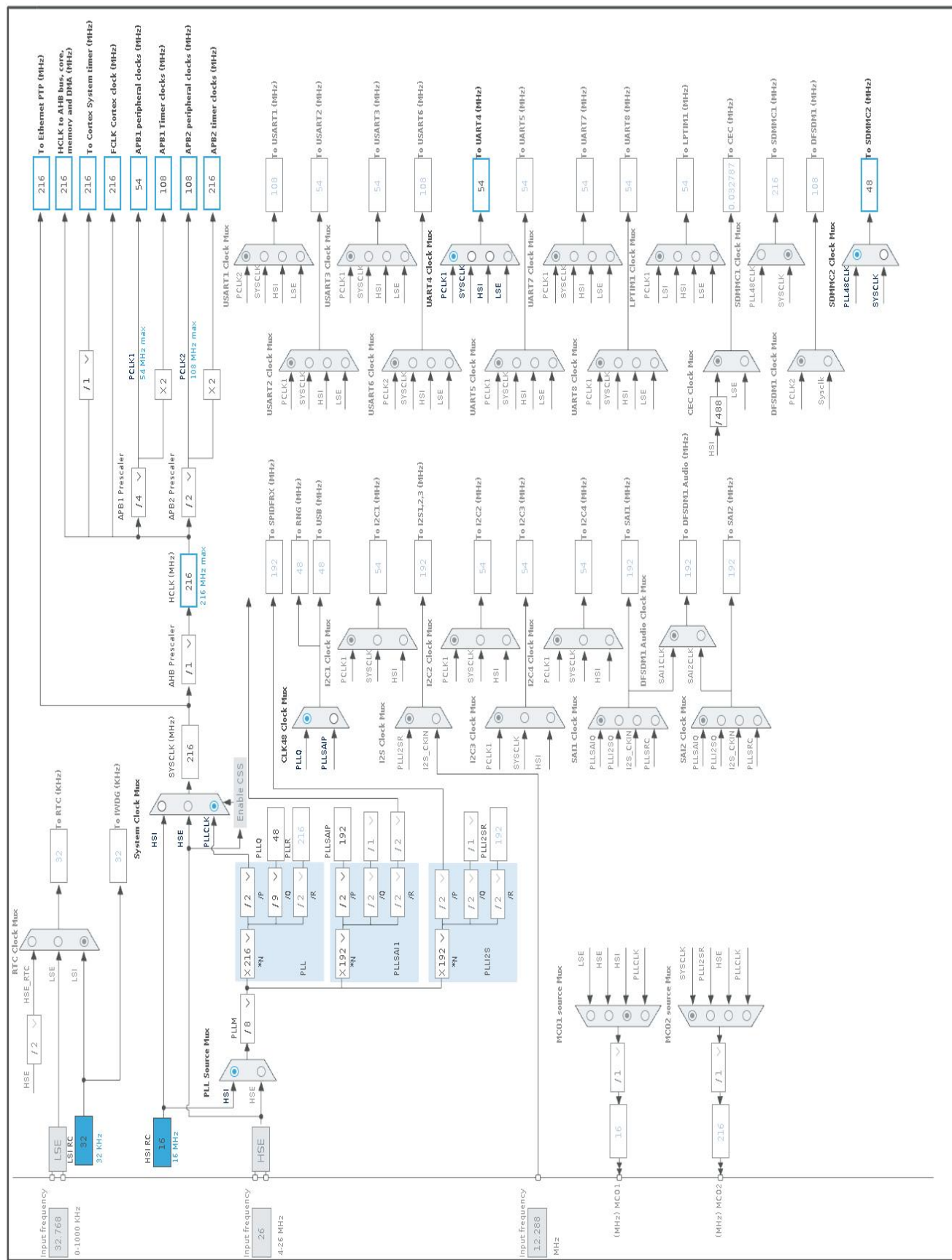
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
14	NRST	Reset		
16	PC1	I/O	SPI2_MOSI	
17	PC2	I/O	SPI2_MISO	
18	PC3 *	I/O	GPIO_Output	SPI2_CS
19	VSSA	Power		
20	VREF+	Power		
21	VDDA	Power		
25	PA3	I/O	GPIO_EXTI3	RIGHT_ENCODER_LINE_A
26	VSS	Power		
27	VDD	Power		
29	PA5 *	I/O	GPIO_Input	SD_DETECT
34	PB0	I/O	GPIO_EXTI0	LEFT_ENCODER_LINE_A
35	PB1	I/O	GPIO_EXTI1	LEFT_ENCODER_LINE_B
41	PE11 *	I/O	GPIO_Output	LED_1
42	PE12 *	I/O	GPIO_Output	LED_2
43	PE13 *	I/O	GPIO_Output	LED_3
44	PE14 *	I/O	GPIO_Output	LED_4
45	PE15 *	I/O	GPIO_Output	LED_5
46	PB10	I/O	SPI2_SCK	
47	PB11 *	I/O	GPIO_Output	SPI_INTERRUPT
48	VCAP_1	Power		
49	VSS	Power		
50	VDD	Power		
53	PB14	I/O	SDMMC2_D0	
70	PA11	I/O	UART4_RX	
71	PA12	I/O	UART4_TX	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
78	PC10	I/O	GPIO_EXTI10	CENTER_ENCODER_DATA_OUT
81	PD0	I/O	CAN1_RX	
82	PD1	I/O	CAN1_TX	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
83	PD2 *	I/O	GPIO_Input	SDMMC2_CS
85	PD4	I/O	GPIO_EXTI4	RIGHT_ENCODER_LINE_B
87	PD6	I/O	SDMMC2_CK	
88	PD7	I/O	SDMMC2_CMD	
89	PB3	I/O	CAN3_RX	
90	PB4	I/O	CAN3_TX	
91	PB5 *	I/O	GPIO_Output	CENTER_ENCODER_CLK_IN
94	BOOT0	Boot		
95	PB8	I/O	TIM10_CH1	BUZZER
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	ECU_BRAINv2_VSC
Project Folder	/home/luca/Documents/git/fenice-sensors/ECU_BRAINv2_VSC
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x5
MCU	STM32F765VGTx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

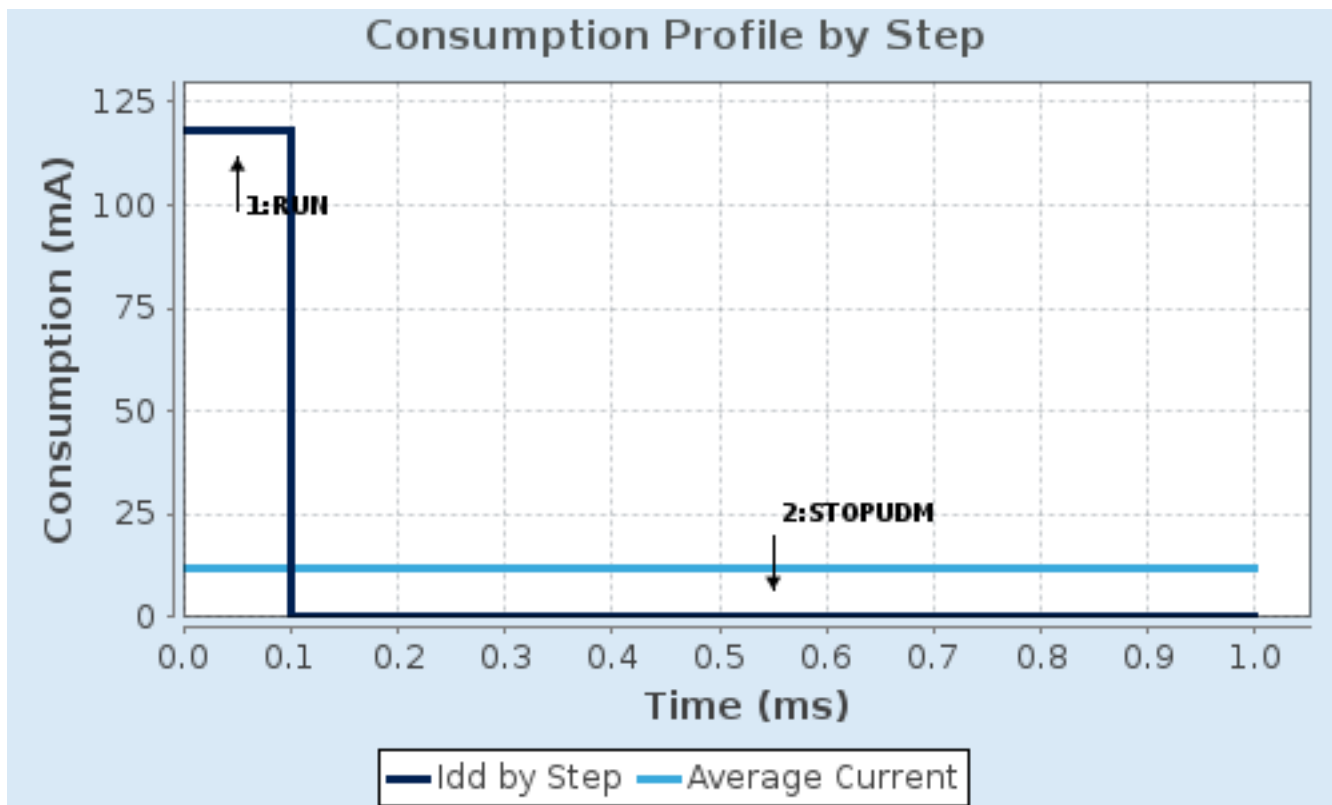
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 μ A
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	88.26	104.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24 DMIPS

6.6. Chart



7. IPs and Middleware Configuration

7.1. CAN1

mode: Mode

7.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	3 *
Time Quantum	55.55555555555556 *
Time Quanta in Bit Segment 1	15 Times *
Time Quanta in Bit Segment 2	2 Times *
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Enable *
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal
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7.2. CAN3

mode: Mode

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	3 *
Time Quantum	55.55555555555556 *
Time Quanta in Bit Segment 1	15 Times *
Time Quanta in Bit Segment 2	2 Times *
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
Automatic Retransmission	Enable *

Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal
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7.3. CORTEX_M7

7.3.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCELERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED
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7.4. GPIO

7.5. RCC

7.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.6. SDMMC2

Mode: SD 1 bit

7.6.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

7.7. SPI2

Mode: Full-Duplex Master

7.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	16 *
Baud Rate	3.375 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.8. SYS

Timebase Source: SysTick

7.9. TIM2

Clock Source : Internal Clock

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	108 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	1000 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.10. TIM4

Clock Source : Internal Clock

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	10800 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	9999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.11. TIM5

mode: Clock Source

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	10800 *
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

7.12. TIM10

mode: Activated

Channel1: PWM Generation CH1

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	216 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	499 *
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.13. UART4

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	2000000 *
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.14. FATFS

mode: SD Card

7.14.1. Set Defines:

Version:

FATFS version	R0.12c
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Function Parameters:

FS_READONLY (Read-only mode)	Disabled
FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	Disabled
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Disabled
FS_TIMEOUT (Timeout ticks)	1000
FS_LOCK (Number of files opened simultaneously)	2

7.14.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance	SDMMC2
Use dma template	Disabled
BSP code for SD	Generic

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
CAN3	PB3	CAN3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB4	CAN3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
SDMMC2	PB14	SDMMC2_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD6	SDMMC2_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD7	SDMMC2_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI2	PC1	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB10	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
TIM10	PB8	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	BUZZER
UART4	PA11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA12	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2_CS
	PA3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	RIGHT_ENCODER_LINE_A
	PA5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SD_DETECT
	PB0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LEFT_ENCODER_LINE_A
	PB1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LEFT_ENCODER_LINE_B
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_1
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_2
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_3
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_4
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_5

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI_INTERRUPT
	PC10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	CENTER_ENCODER_DATA_OUT
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SDMMC2_CS
	PD4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	RIGHT_ENCODER_LINE_B
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CENTER_ENCODER_CLK_IN

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI2_TX	DMA1_Stream4	Memory To Peripheral	High *

SPI2_TX: DMA1_Stream4 DMA request Settings:

Mode: Normal
Use fifo: Disable
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Byte
Memory Data Width: Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line3 interrupt	true	0	0
EXTI line4 interrupt	true	0	0
DMA1 stream4 global interrupt	true	0	0
CAN1 TX interrupts	true	0	0
CAN1 RX0 interrupts	true	0	0
CAN1 RX1 interrupt	true	0	0
CAN1 SCE interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
SPI2 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
UART4 global interrupt	true	0	0
CAN3 TX interrupt	true	0	0
CAN3 RX0 interrupt	true	0	0
CAN3 RX1 interrupt	true	0	0
CAN3 SCE interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
EXTI line1 interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
FPU global interrupt	unused		
SDMMC2 global interrupt	unused		

* User modified value

9. *Predefined Views - Category view : Current*

Middleware						
FATFS ✓						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
CORTEX_M7 ✓		TIM2 ✓	CAN1 ✓			
DMA ✓		TIM4 ✓	CAN3 ✓			
GPIO ✓		TIM5 ✓	SDMMC2 ✓			
NVIC ✓		TIM10 ✓	SPI2 ✓			
RCC ✓			UART4 ✓			
SYS ✓						

10. Software Pack Report