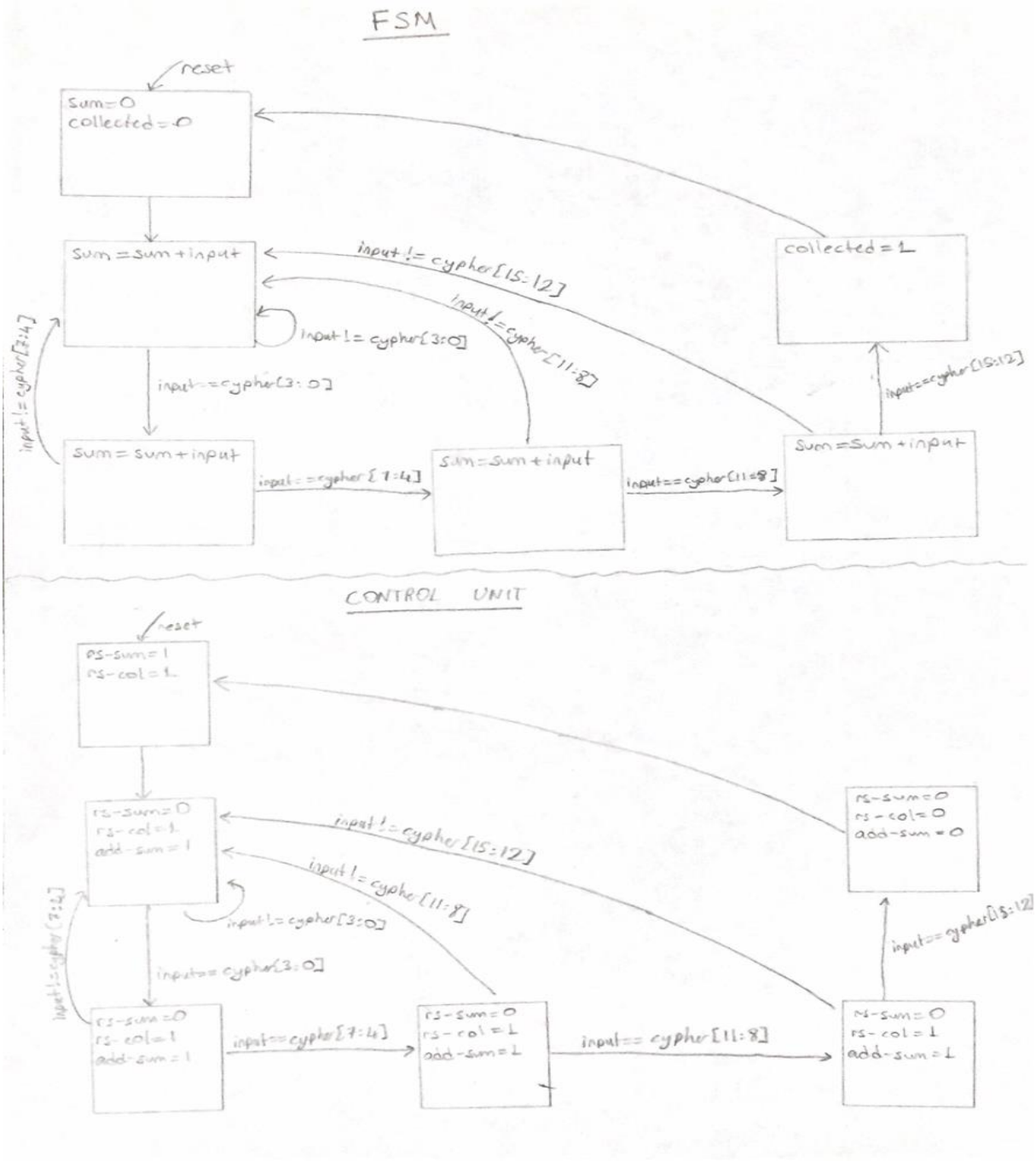
CSE 331 BONUS ASSIGNMENT

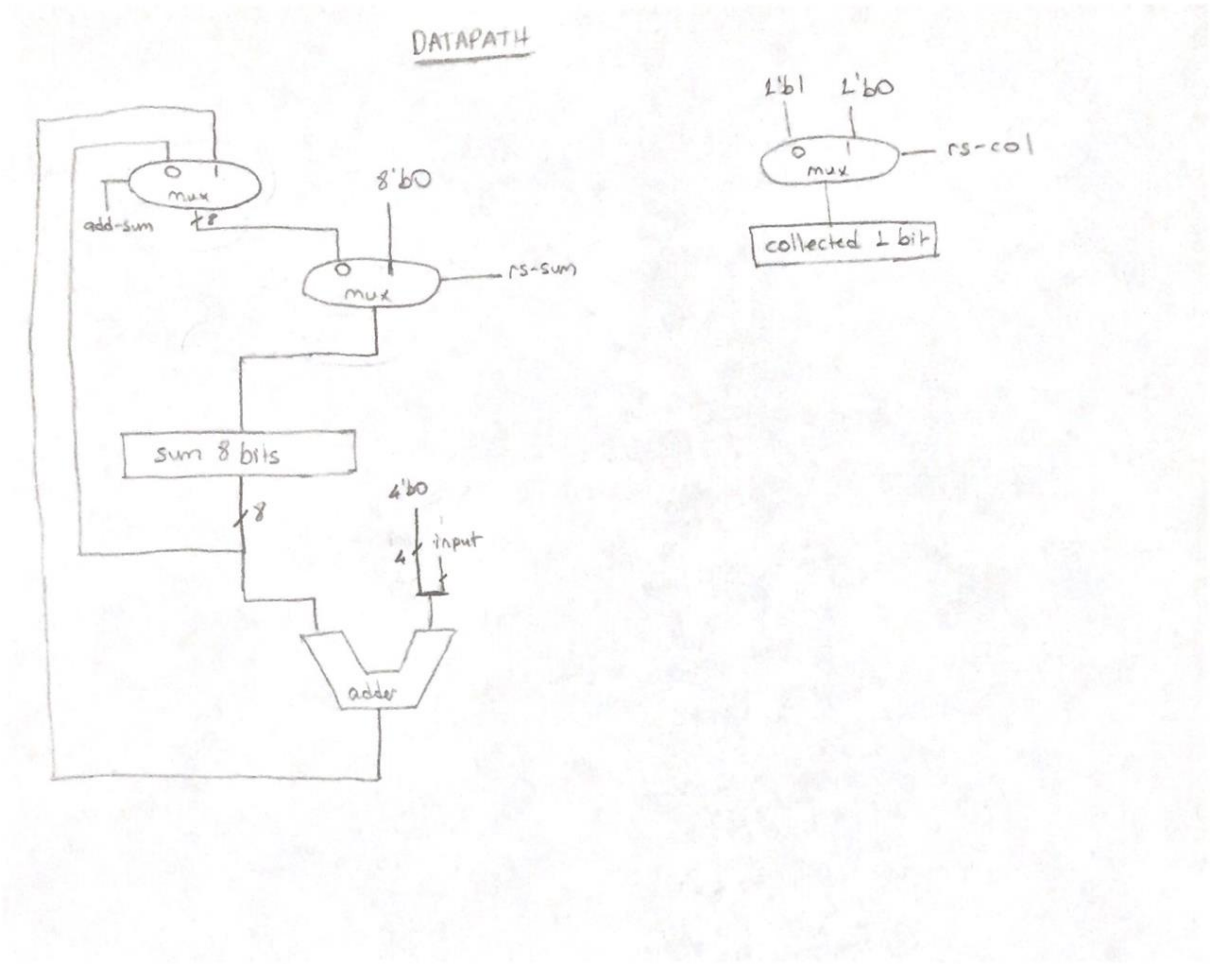
1) Finite State Machine and Control Unit



Clock and read input are neglected in FSM transitions.

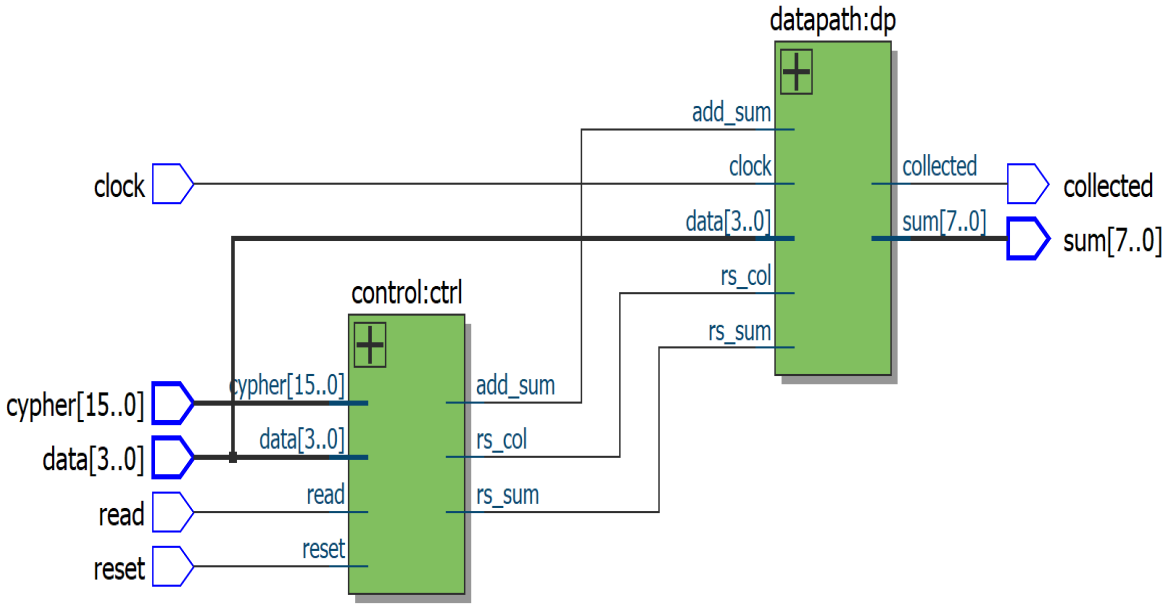
P.S In all states except than first and last states, if the data is not matched with cypher [X: Y], the data must be compared with cypher [3:0], if they are matched, state must be changed to third state. Otherwise, state must be changed to second state. To explain, if the cypher is 0001-0010-0011-0100 and inputs are 0100, 0011, 0010, 0100 respectively, after all inputs are got, current state must be third state.

2) Datapath

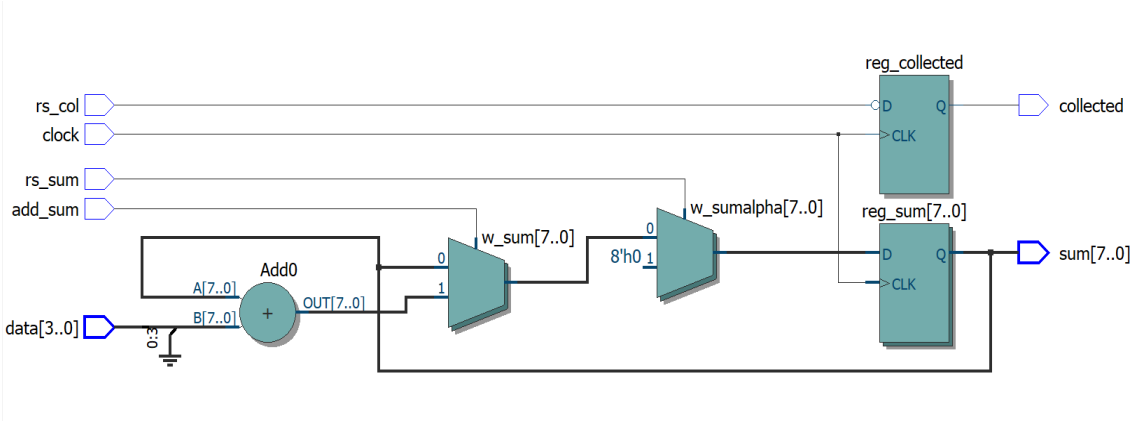


3) RTL Views

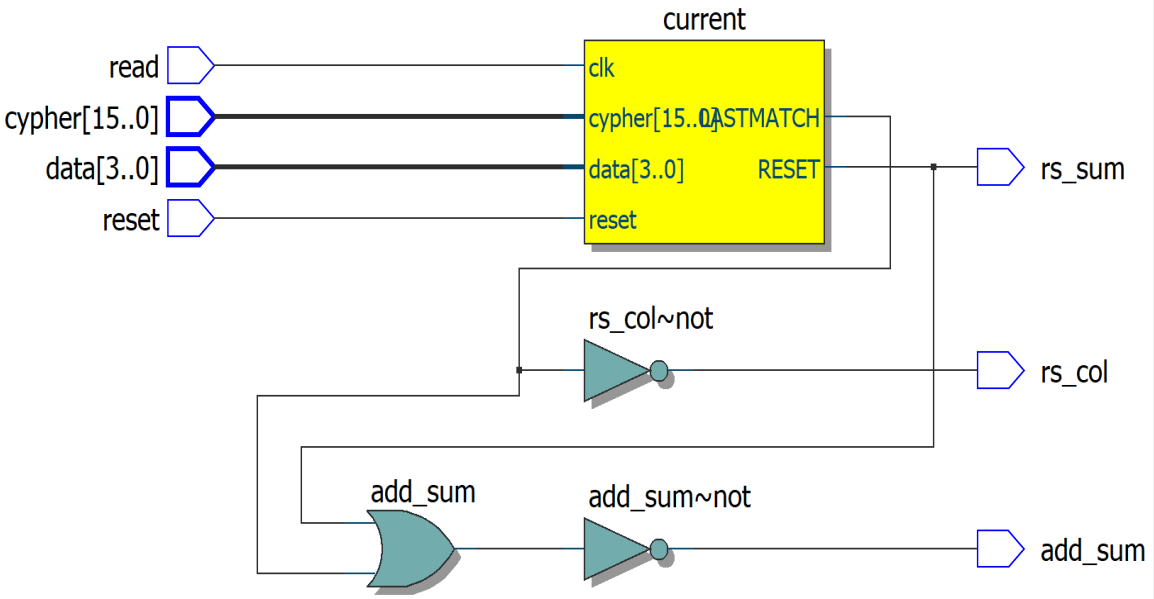
a. cypherDetector



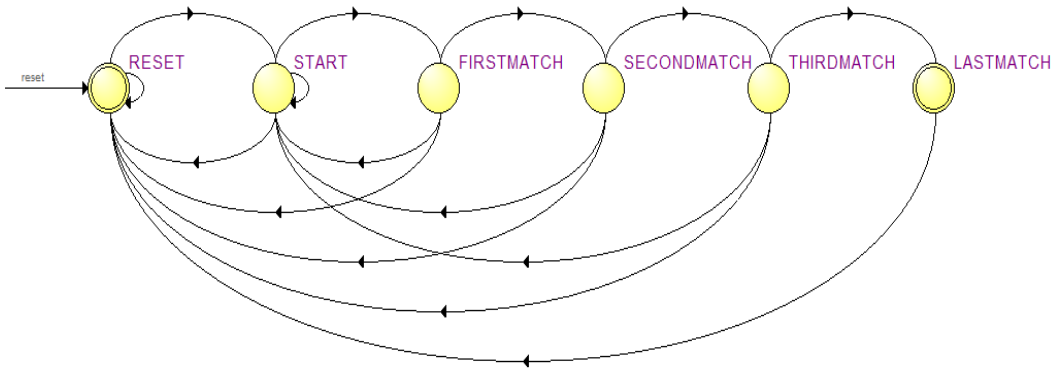
b. datapath



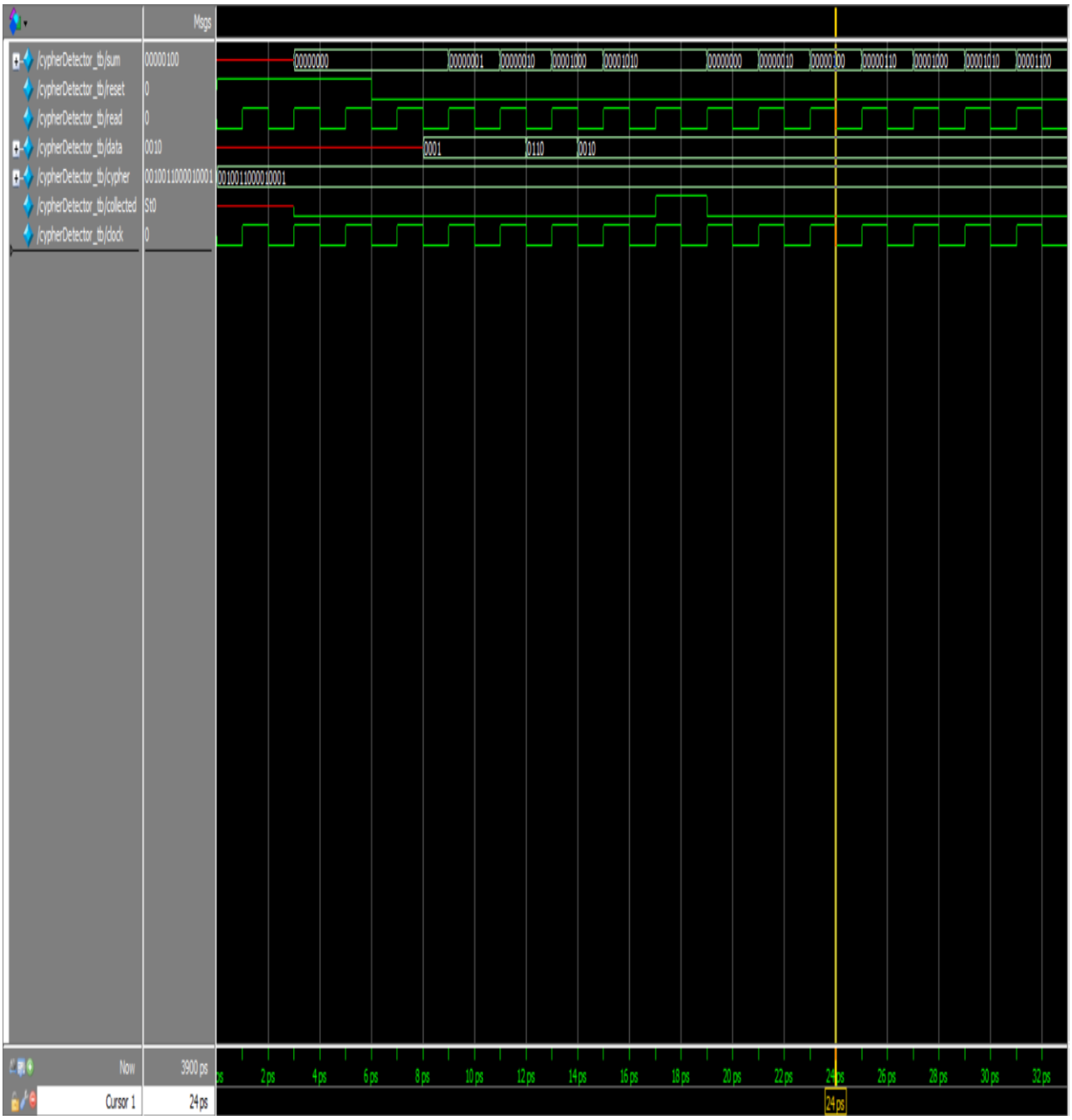
c. control



d. FSM



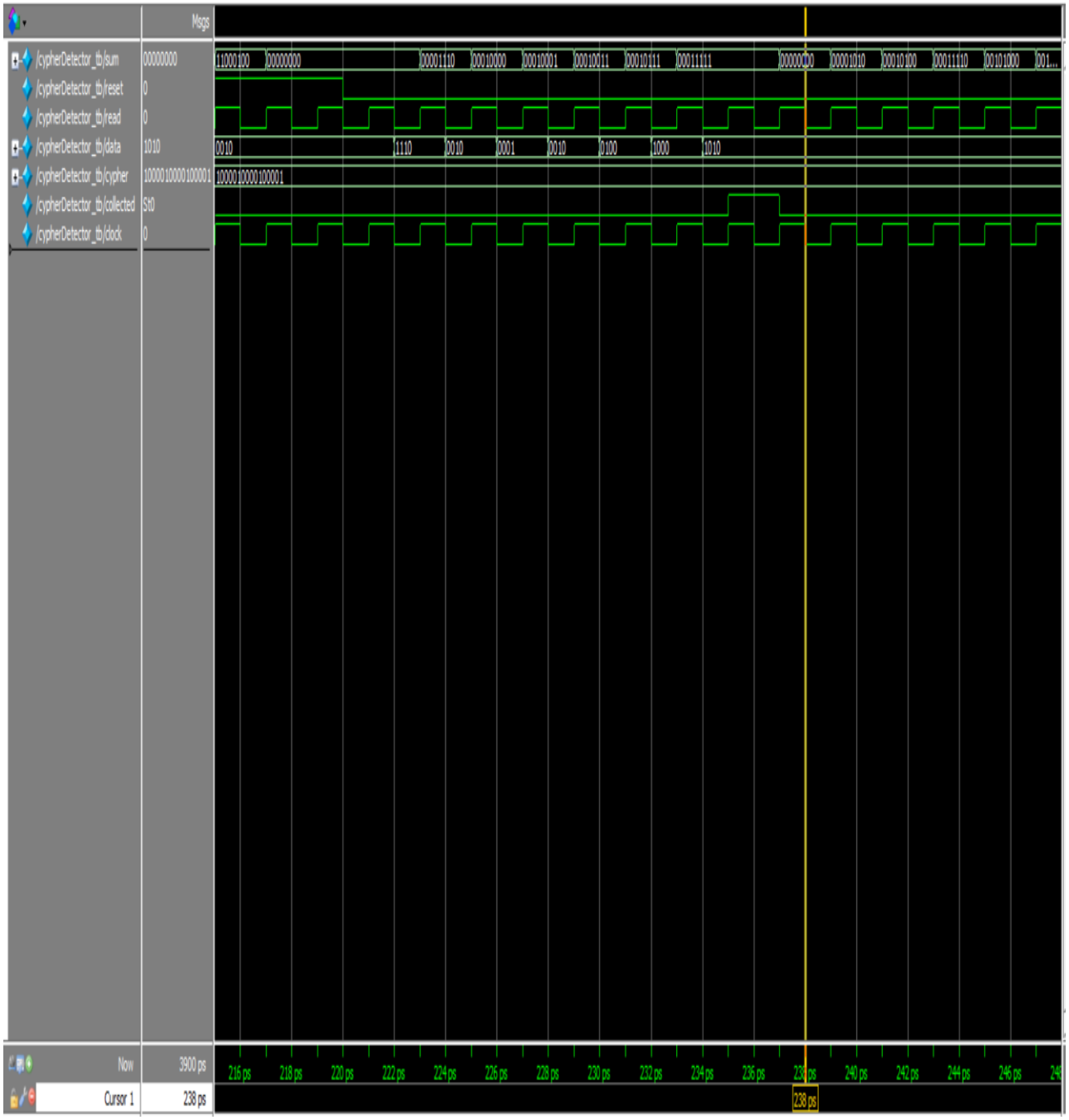
4) Testbench and Result



Cypher is: 0010 0110 0001 0001

Input is: 0001-0001-0110-0010 respectively.

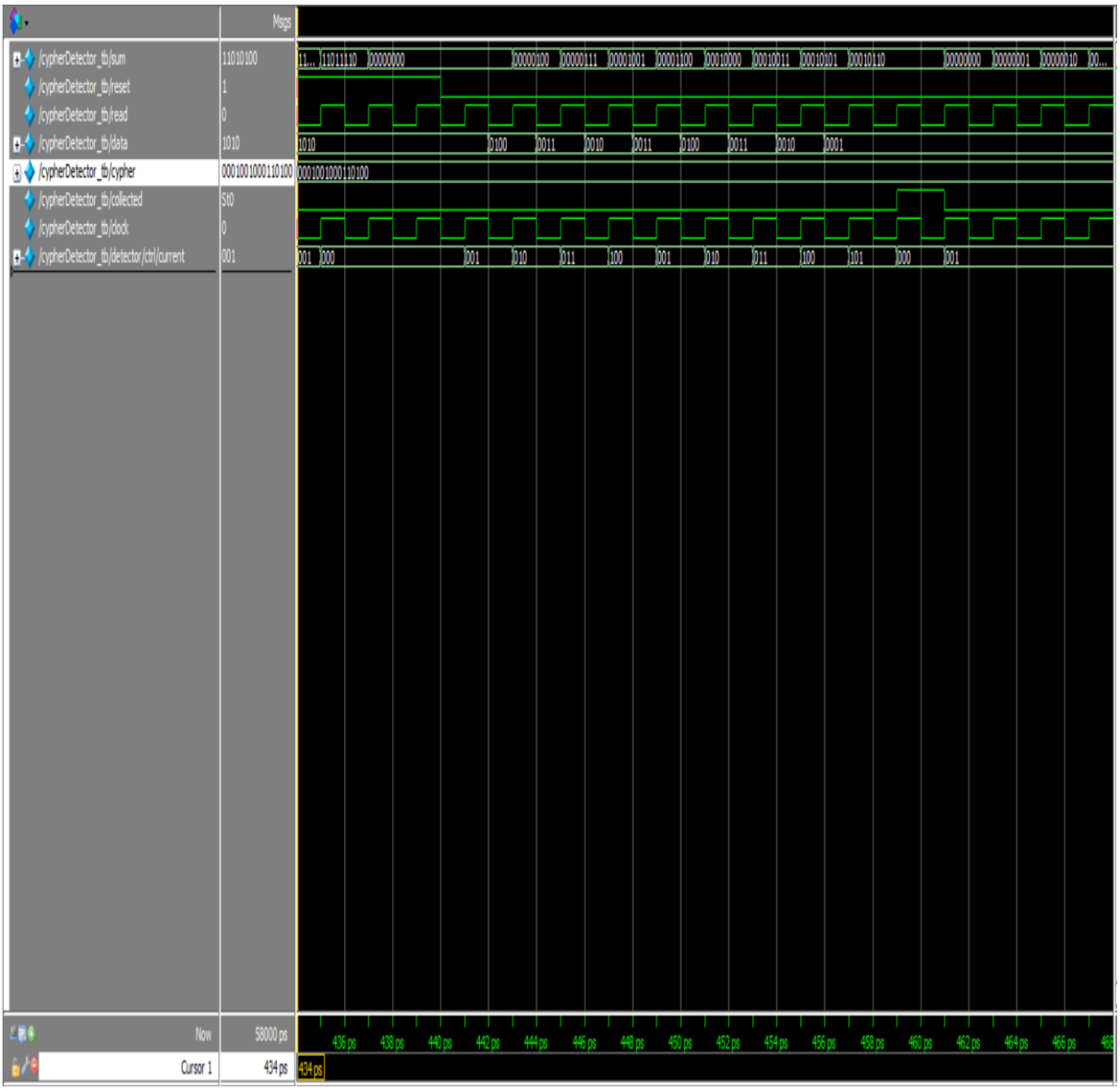
The first three 4-bits of the input are compared with the last three 4-bits of the cypher. After they are matched, the last 4-bits of the input is compared with first 4-bits of the cypher. Because it is matched too, collected is set as 1. At the end of the operation sum is 00001010 which is sum of the 0001, 0001, 0110, and 0010.



Cypher is: 1000 0100 0010 0001

Input is: 1110-0010-0001-0010-0100-1000-1010 respectively.

First two 4-bits of the input are not matched with the last input of the cypher. So, starting from the third 4-bits of the input, rest of the input match with cypher. So collected is set as 1 at the end of the first six 4-bits are got. At the end of the operation sum is 00011111 which is sum of 1110, 0010, 0001, 0010, 0100, 1000.



Cypher is: 0001 0010 0011 0100

Input is: 0100-0011-0010-0011-0100-0011-0010-0001 respectively.

First three 4-bits of the input are matched with the last three 4-bits of the cypher but, fourth 4-bits input is not matched with the last 4-bit of the cypher. So, current state is changed from THIRDMATCH(100) state to START(001) state. Last four 4-bits of the input are matched with the cypher. So, collected is set to 1 at the end of the eighth cycle. At the end of the operation sum is 00010110 which is sum of 0100, 0011, 0010, 0011, 0100, 0011, 0010, 0001.

P.S All pictures are uploaded in another file to see more clear.