EEE4120F YODA

Milestone 2: Conceptual Design- Smoothing Filter

Topic Code: P01- SF: Smoothing Filter

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Role Allocation

CEO: Sindiso Mkhatshwa
Chief Researcher: Maneno Mgwami
Director of Operations: Emmanuel Francis
Director of Support Services: Chris Hill

Project Description and Required Skills

The problem focus for this project is to design and implement a digital smoothing filter. It needs to be able to remove high frequency noise to increase the precision of the data without altering the signal tendency. Skills required include a knowledge of FPGA concepts, the ability to code in Verilog and VHDL, an understanding of Digital Signal Processing and the diligence to follow design principles to implement the solution.

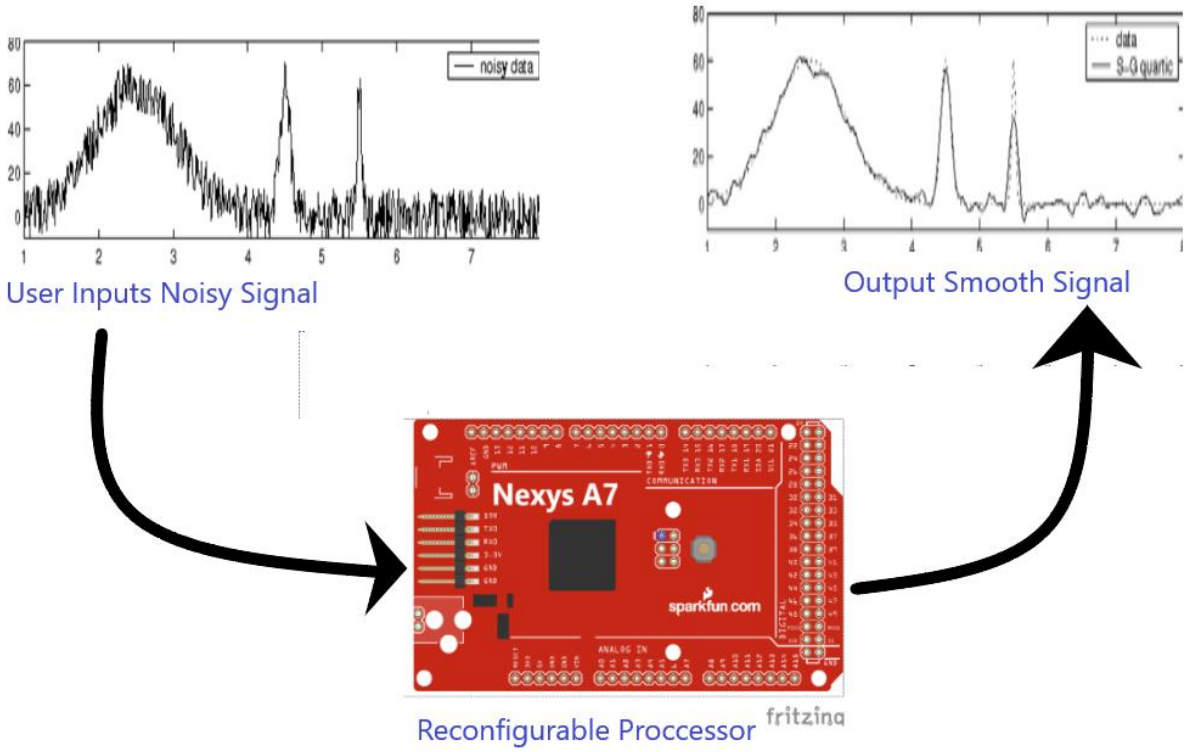


Figure 1: Conceptual Design of Smoothing Filter

Strategy for Evaluating Design Solution

The Smoothing filter will be prototyped on a Nexys4 board, simulating the source and destination addresses in BRAM. The filter will be implemented using the Mean filter smoothing method. This is one of the simplest and fastest smoothing methods [2][4].

Plan A and Plan A extended

The system operates by the user entering the source address for the raw data, data length and destination address to send the processed data (simulated by an array in Verilog, same as the source for the raw data). The simulated source address may contain 2 or 3-dimensional data subject to time. A basic Mean algorithm will be implemented to convert the noising signal entered as input by the user and convert it into a smooth signal output [2][3].

Plan B

It generally covers the same functionality as Plan A, but due to Covid-19 and the strain it has put on our academics, there might not be enough time to implement the solution in its totality. The same idea from Plan A is still portrayed in Plan B, but in this implementation the basic system will operate on one-dimensional digital data as opposed to 2 or 3-dimensional data [2][3].

Methodology of Developing Proposed Solution

Prototyped Specification

- For this prototype it is assumed that the noise data is already in a digital format and stored in the FPGA memory. Hence the smoothing filter must start by loading indicated data from the memory.
- The file of input sample data and the smoothed data will be simulated by memory of two or three arrays of data in BRAM
- The done bit will be indicated by one diode on the FPGA (ON when True and OFF when false)
- The toggle bit will also be indicated by one diode (could do an average of m elements))
- Debounce buttons for the user to set the smoothing factor

Criteria for acceptable solution

Plan B

- Start up
- Have toggle and done working and indicated by diodes
- Able to read 1-dimensional data and store it in memory
- Have buttons debounced to correctly set a single smoothing factor
- Able to produce the output smoothed data of the same length as the 1-dimensional noise data
- The output data should be able to be represented in graphical form.

Plan A

- All of Plan B
- Able to read 2-dimensional data and store it in memory
- Have buttons debounced to correctly set 2 smoothing factors
- Able to produce the output smoothed data of the same length as the 2-dimensional noise data

Plan A- Extended

- All of Plan A
- Able to read 3-dimensional data and store it in memory

- Have buttons debounced to correctly set 3 smoothing factors
- Able to produce the output smoothed data of the same length as the 3-dimensional noise data

Modeling and Analysis

<u>Diagram Showing the Order that the Tasks will be Implemented in</u>

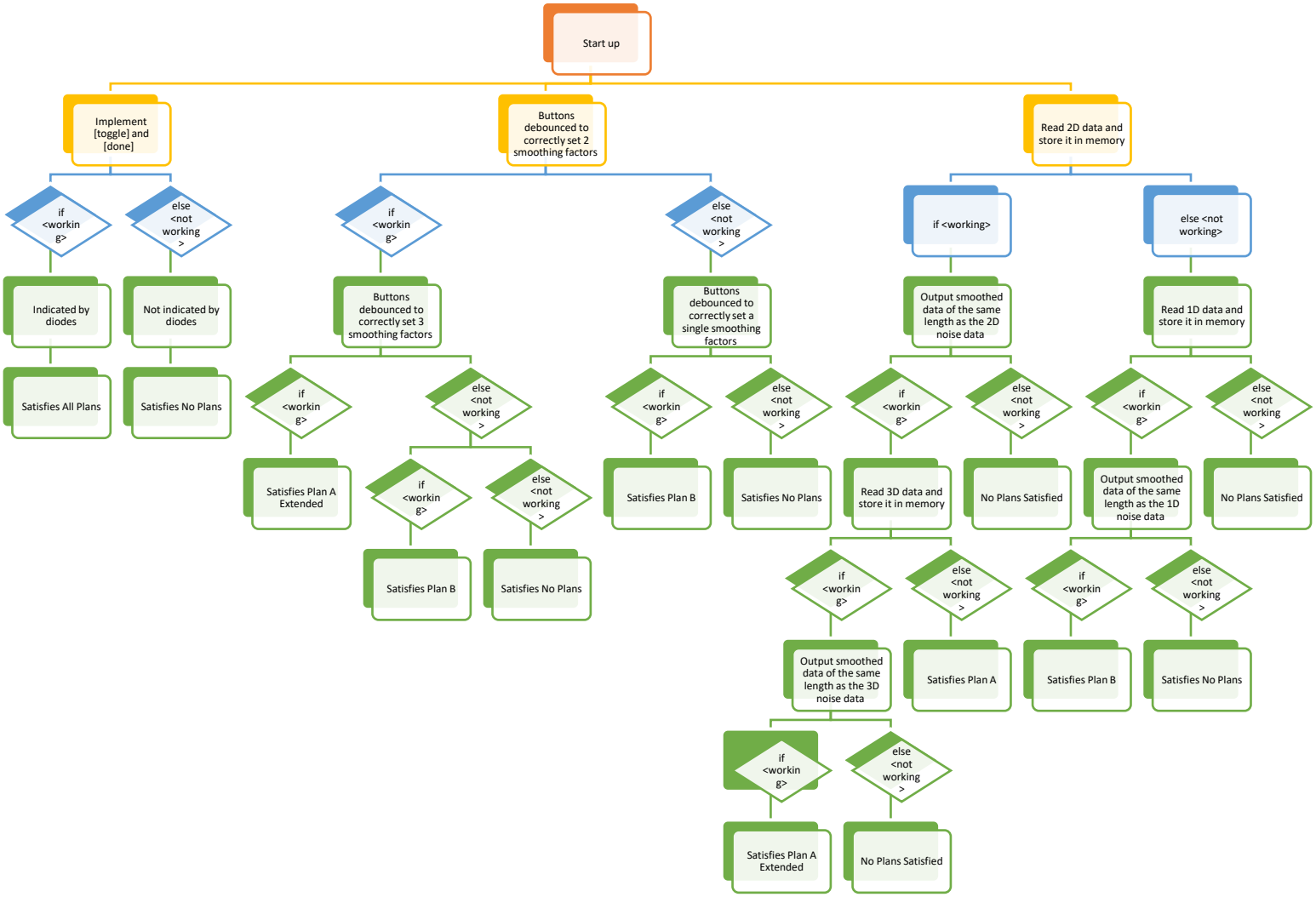
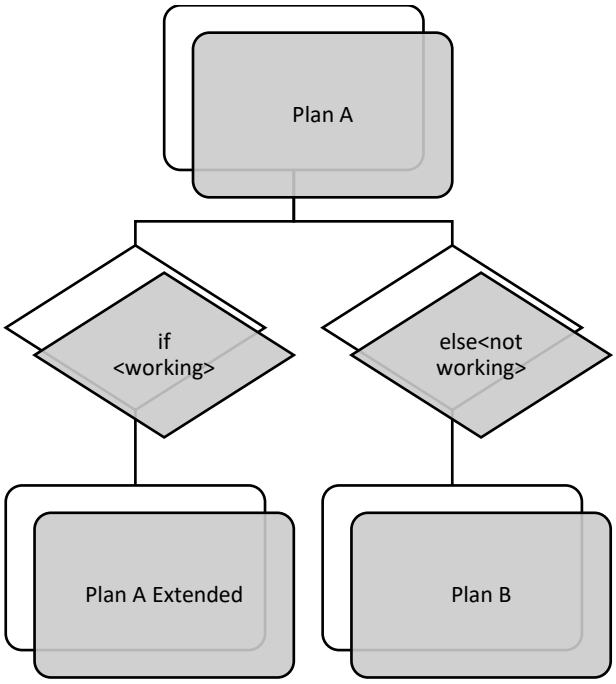
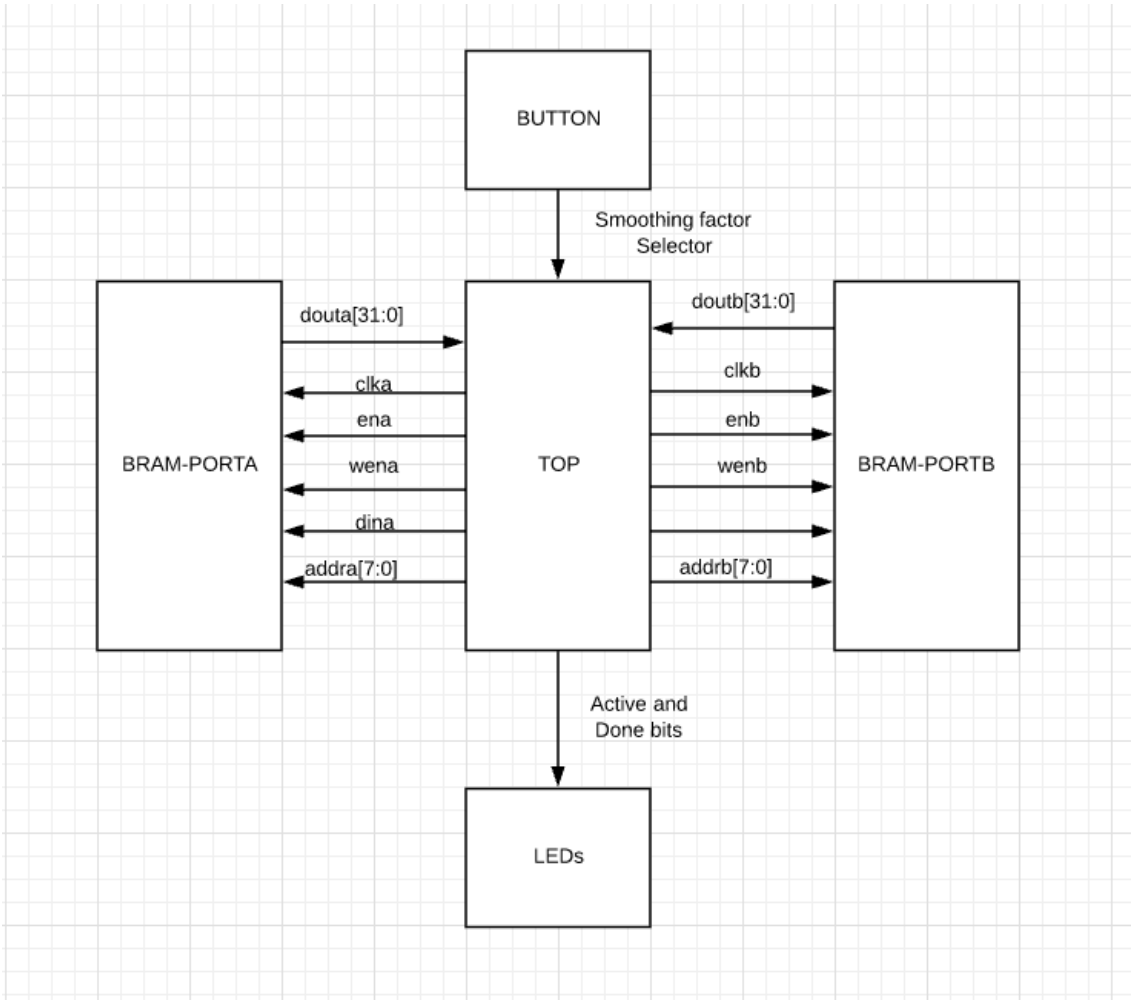


Diagram Showing the Order that the Plans will be Implemented in



Block Diagram of System



Division of Labour and Time Frame

Plan A

CEO Sindiso Mkhatshwa:

- Implement Basic Mean Algorithm on FPGA. (Data processing)
- Toggle done diode when done processing

Complete by 1 June 2020

Director of Operations Emmanuel Francis:

- Set up debounce modules for button input, i.e. Setting smoothing factor

Complete by 24 May 2020

- Implement Basic Mean Algorithm on Vivado

Complete by 1 June 2020

Chief Researcher Maneno Mgwami:

- Create BRAM to store and read data (Simulate input source and output dest addresses)

Complete by 24 May 2020

All team members:

- Start up (basically creating the required program files) by 24 May 2020
- Debugging, Testing and Verification of Plan A from 1st of June 2020 to 7th of June 2020

- Consultation with Director of Support Services-Chris Hill- during the week of 1 June to 7 June 2020.
- Start working on final report (draft report is included in final report) From the 1st of June 2020

Plan A-Extended

CEO Sindiso Mkhatshwa:
- Extend Basic Mean Algorithm on FPGA for 3D data. (Data processing)

Complete by 15 June 2020

Director of Operations Emmanuel Francis:
- Extend Basic Mean Algorithm on FPGA for 3D data. (Data processing)
- Extend debounce modules for button input, i.e. Setting 3 smoothing factors

Complete by 15 June 2020

Chief Researcher Maneno Mgwami:
- Extend Basic Mean Algorithm on FPGA for 3D data. (Data processing)

Complete by 15 June 2020

Submission Deadlines

1. Milestone 2: Conceptual Design 22 May 2020
2. Milestone 3: Status Update 12 June 2020
3. Milestone 4: Draft Paper 15 June 2020
4. Milestone 5: Demonstration 22 June 2020
5. Milestone 6: Final Report 26 June 2020

References

1. Mathworks (2020) Smoothing Filter. Available at https://www.mathworks.com/help/curvefit/smooth_sg2.gif (Accessed 11 May 2020).

2. TerpConnect (2020) Intro to Signal Processing: Smoothing. Available at https://terpconnect.umd.edu/~toh/spectrum/Smoothing.html (Accessed 10 May 2020).

3. AIP (2020) Data Smoothing Using Low-Pass Digital Filters. Available at https://aip.scitation.org/doi/abs/10.1063/1.1134918?journalCode=rsi& (Accessed 11 May 2020).

4. P. Kowalski and R. Smyk, "Review and comparison of smoothing algorithms for one-dimensional data noise reduction," 2018 International Interdisciplinary PhD Workshop (IIPhDW), Swinoujście, 2018, pp. 277-281, doi: 10.1109/IIPHDW.2018.8388373.