PSoC® Creator™
Project Datasheet for SCSI2SD

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Table of Contents

1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C52LP family member PSoC 5 device. For details on all the systems listed above, please refer to the PSoC 5 Technical Reference Manual .

Figure 1. CY8C52LP Device Family Block Diagram

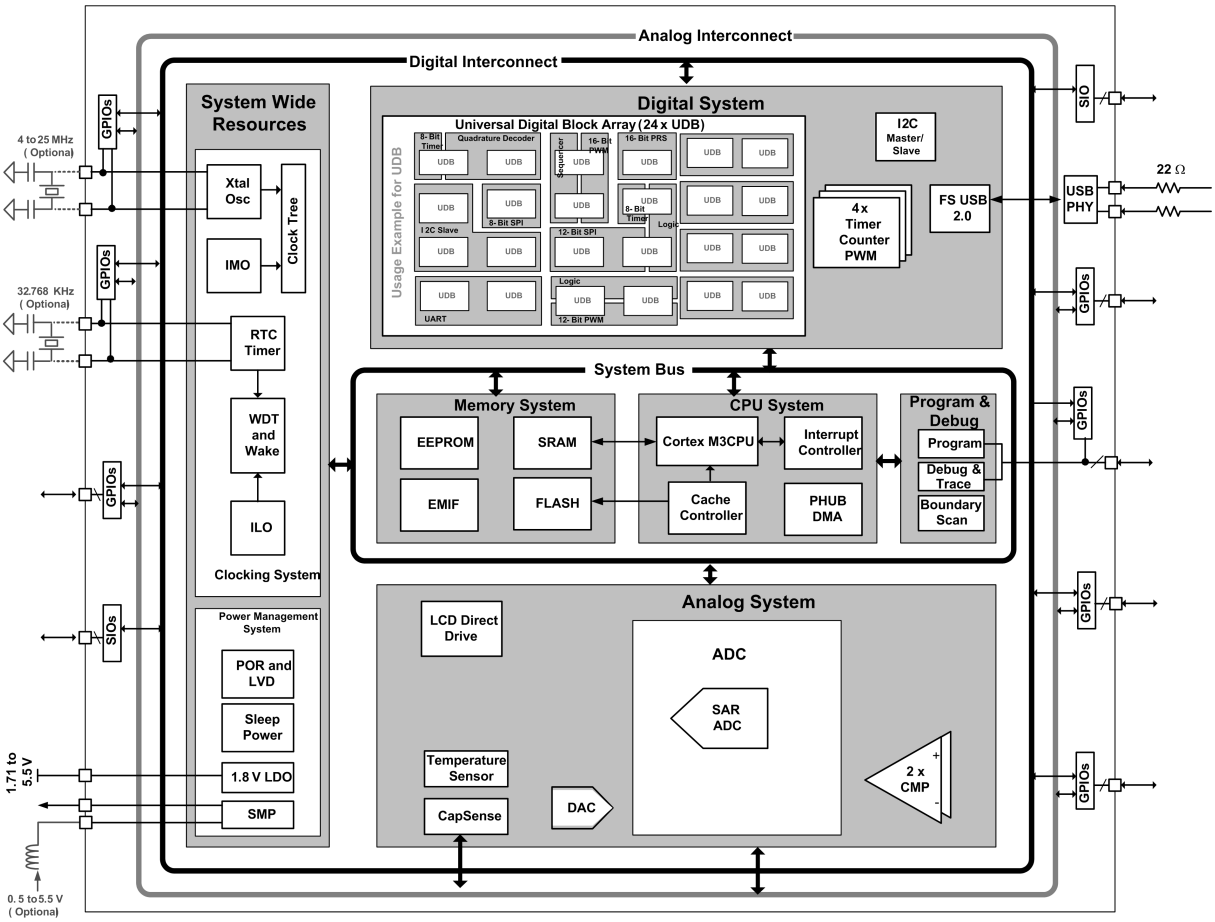


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5267AXI-LP051
Package Name	100-TQFP
Architecture	PSoC 5
Family	CY8C52LP
CPU speed (MHz)	67
Flash size (kBytes)	128
SRAM size (kBytes)	32
EEPROM size (Bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x2E133069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

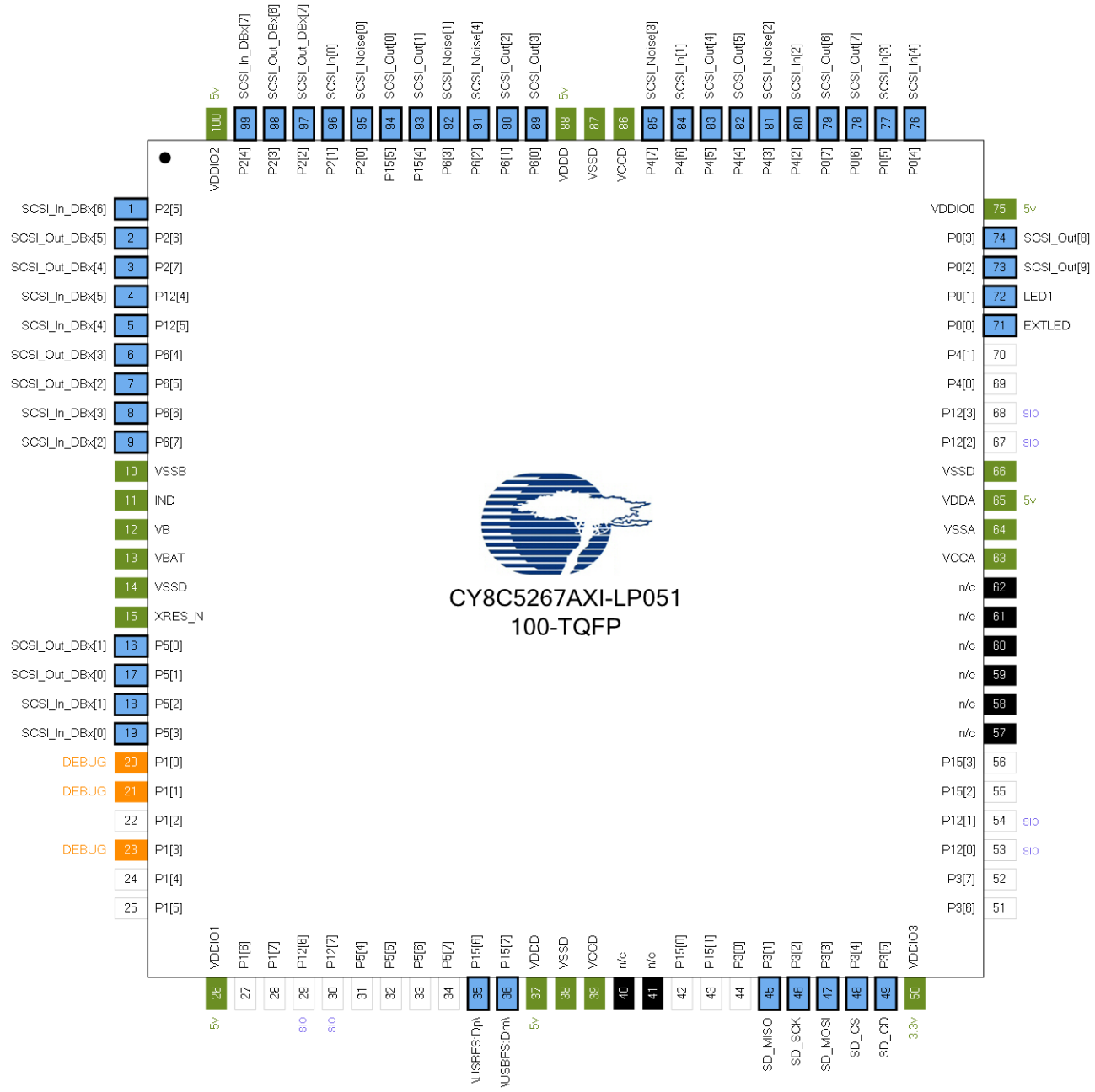
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	3	5	8	37.50 %
Analog Clocks	0	4	4	0.00 %
CapSense Buffers	0	2	2	0.00 %
Interrupts	16	16	32	50.00 %
IO	50	22	72	69.44 %
Segment LCD	0	1	1	0.00 %
I2C	0	1	1	0.00 %
USB	1	0	1	100.00 %
DMA Channels	4	20	24	16.67 %
Timer	1	3	4	25.00 %
UDB				
Macrocells	83	109	192	43.23 %
Unique P-terms	237	147	384	61.72 %
Total P-terms	245			
Datapath Cells	2	22	24	8.33 %
Status Cells	10	14	24	41.67 %
Status Registers	3			
StatusI Registers	2			
Sync Cells (x14)	4			
Routed Count7 Load/Enable	1			
Control Cells	5	19	24	20.83 %
Control Registers	4			
Count7 Cells	1			
Comparator	0	2	2	0.00 %
LPF	0	2	2	0.00 %
SAR ADC	0	1	1	0.00 %
DAC				
VIDAC	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	SCSI_In_DBx[6]	Dgtl In	HiZ digital	HiZ Analog Unb
2	P2[6]	SCSI_Out_DBx[5]	Dgtl Out	Strong drive	HiZ Analog Unb
3	P2[7]	SCSI_Out_DBx[4]	Dgtl Out	Strong drive	HiZ Analog Unb
4	P12[4]	SCSI_In_DBx[5]	Dgtl In	HiZ digital	HiZ Analog Unb
5	P12[5]	SCSI_In_DBx[4]	Dgtl In	HiZ digital	HiZ Analog Unb
6	P6[4]	SCSI_Out_DBx[3]	Dgtl Out	Strong drive	HiZ Analog Unb
7	P6[5]	SCSI_Out_DBx[2]	Dgtl Out	Strong drive	HiZ Analog Unb
8	P6[6]	SCSI_In_DBx[3]	Dgtl In	HiZ digital	HiZ Analog Unb
9	P6[7]	SCSI_In_DBx[2]	Dgtl In	HiZ digital	HiZ Analog Unb
10	VSSB	VSSB	Dedicated		
11	IND	IND	Dedicated		
12	VB	VB	Dedicated		
13	VBAT	VBAT	Dedicated		
14	VSSD	VSSD	Power		
15	XRES_N	XRES_N	Dedicated		
16	P5[0]	SCSI_Out_DBx[1]	Dgtl Out	Strong drive	HiZ Analog Unb
17	P5[1]	SCSI_Out_DBx[0]	Dgtl Out	Strong drive	HiZ Analog Unb
18	P5[2]	SCSI_In_DBx[1]	Dgtl In	HiZ digital	HiZ Analog Unb
19	P5[3]	SCSI_In_DBx[0]	Dgtl In	HiZ digital	HiZ Analog Unb
20	P1[0]	Debug:SWD_IO	Reserved		
21	P1[1]	Debug:SWD_CK	Reserved		
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	Debug:SWV	Reserved		
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	GPIO [unused]			HiZ Analog Unb
26	VDDIO1	VDDIO1	Power		
27	P1[6]	GPIO [unused]			HiZ Analog Unb
28	P1[7]	GPIO [unused]			HiZ Analog Unb
29	P12[6]	SIO [unused]			HiZ Analog Unb
30	P12[7]	SIO [unused]			HiZ Analog Unb
31	P5[4]	GPIO [unused]			HiZ Analog Unb
32	P5[5]	GPIO [unused]			HiZ Analog Unb
33	P5[6]	GPIO [unused]			HiZ Analog Unb
34	P5[7]	GPIO [unused]			HiZ Analog Unb
35	P15[6]	USB:D+	Reserved		
36	P15[7]	USB:D-	Reserved		
37	VDDD	VDDD	Power		
38	VSSD	VSSD	Power		
39	VCCD	VCCD	Power		
42	P15[0]	GPIO [unused]			HiZ Analog Unb
43	P15[1]	GPIO [unused]			HiZ Analog Unb
44	P3[0]	GPIO [unused]			Pulled Up
45	P3[1]	SD_MISO	Dgtl In	HiZ digital	Pulled Up
46	P3[2]	SD_SCK	Dgtl Out	Strong drive	Pulled Up
47	P3[3]	SD_MOSI	Dgtl Out	Strong drive	Pulled Up

Pin	Port	Name	Type	Drive Mode	Reset State
48	P3[4]	SD_CS	Software In/Out	Strong drive	Pulled Up
49	P3[5]	SD_CD	Software Input	HiZ digital	Pulled Up
50	VDDIO3	VDDIO3	Power		
51	P3[6]	GPIO [unused]			Pulled Up
52	P3[7]	GPIO [unused]			Pulled Up
53	P12[0]	SIO [unused]			HiZ Analog Unb
54	P12[1]	SIO [unused]			HiZ Analog Unb
55	P15[2]	GPIO [unused]			HiZ Analog Unb
56	P15[3]	GPIO [unused]			HiZ Analog Unb
63	VCCA	VCCA	Power		
64	VSSA	VSSA	Power		
65	VDDA	VDDA	Power		
66	VSSD	VSSD	Power		
67	P12[2]	SIO [unused]			HiZ Analog Unb
68	P12[3]	SIO [unused]			HiZ Analog Unb
69	P4[0]	GPIO [unused]			HiZ Analog Unb
70	P4[1]	GPIO [unused]			HiZ Analog Unb
71	P0[0]	EXTLED	Software In/Out	HiZ digital	HiZ Analog Unb
72	P0[1]	LED1	Software Output	OD, DL	HiZ Analog Unb
73	P0[2]	SCSI_Out[9]	Dgtl Out	Strong drive	HiZ Analog Unb
74	P0[3]	SCSI_Out[8]	Dgtl Out	Strong drive	HiZ Analog Unb
75	VDDIO0	VDDIO0	Power		
76	P0[4]	SCSI_In[4]	Software Input	HiZ digital	HiZ Analog Unb
77	P0[5]	SCSI_In[3]	Software Input	HiZ digital	HiZ Analog Unb
78	P0[6]	SCSI_Out[7]	Dgtl Out	Strong drive	HiZ Analog Unb
79	P0[7]	SCSI_Out[6]	Software Output	Strong drive	HiZ Analog Unb
80	P4[2]	SCSI_In[2]	Software Input	HiZ digital	HiZ Analog Unb
81	P4[3]	SCSI_Noise[2]	Dgtl In	HiZ digital	HiZ Analog Unb
82	P4[4]	SCSI_Out[5]	Dgtl Out	Strong drive	HiZ Analog Unb
83	P4[5]	SCSI_Out[4]	Software Output	Strong drive	HiZ Analog Unb
84	P4[6]	SCSI_In[1]	Software Input	HiZ digital	HiZ Analog Unb
85	P4[7]	SCSI_Noise[3]	Dgtl In	HiZ digital	HiZ Analog Unb
86	VCCD	VCCD	Power		
87	VSSD	VSSD	Power		
88	VDDD	VDDD	Power		
89	P6[0]	SCSI_Out[3]	Software Output	Strong drive	HiZ Analog Unb
90	P6[1]	SCSI_Out[2]	Software Output	Strong drive	HiZ Analog Unb
91	P6[2]	SCSI_Noise[4]	Dgtl In	HiZ digital	HiZ Analog Unb
92	P6[3]	SCSI_Noise[1]	Dgtl In	HiZ digital	HiZ Analog Unb
93	P15[4]	SCSI_Out[1]	Software Output	Strong drive	HiZ Analog Unb
94	P15[5]	SCSI_Out[0]	Dgtl Out	Strong drive	HiZ Analog Unb
95	P2[0]	SCSI_Noise[0]	Dgtl In	HiZ digital	HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
96	P2[1]	SCSI_In[0]	Dgtl In	HiZ digital	HiZ Analog Unb
97	P2[2]	SCSI_Out_DBx[7]	Dgtl Out	Strong drive	HiZ Analog Unb
98	P2[3]	SCSI_Out_DBx[6]	Dgtl Out	Strong drive	HiZ Analog Unb
99	P2[4]	SCSI_In_DBx[7]	Dgtl In	HiZ digital	HiZ Analog Unb
100	VDDIO2	VDDIO2	Power		

Abbreviations used in Table 3 have the following meanings:

- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- OD, DL = Open drain, drives low

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	71	EXTLED	Software In/Out	HiZ digital	HiZ Analog Unb
P0[1]	72	LED1	Software Output	OD, DL	HiZ Analog Unb
P0[2]	73	SCSI_Out[9]	Dgtl Out	Strong drive	HiZ Analog Unb
P0[3]	74	SCSI_Out[8]	Dgtl Out	Strong drive	HiZ Analog Unb
P0[4]	76	SCSI_In[4]	Software Input	HiZ digital	HiZ Analog Unb
P0[5]	77	SCSI_In[3]	Software Input	HiZ digital	HiZ Analog Unb
P0[6]	78	SCSI_Out[7]	Dgtl Out	Strong drive	HiZ Analog Unb
P0[7]	79	SCSI_Out[6]	Software Output	Strong drive	HiZ Analog Unb
P1[0]	20	Debug:SWD_IO	Reserved		
P1[1]	21	Debug:SWD_CK	Reserved		
P1[2]	22	GPIO [unused]			HiZ Analog Unb
P1[3]	23	Debug:SWV	Reserved		
P1[4]	24	GPIO [unused]			HiZ Analog Unb
P1[5]	25	GPIO [unused]			HiZ Analog Unb
P1[6]	27	GPIO [unused]			HiZ Analog Unb
P1[7]	28	GPIO [unused]			HiZ Analog Unb
P12[0]	53	SIO [unused]			HiZ Analog Unb
P12[1]	54	SIO [unused]			HiZ Analog Unb
P12[2]	67	SIO [unused]			HiZ Analog Unb
P12[3]	68	SIO [unused]			HiZ Analog Unb
P12[4]	4	SCSI_In_DBx[5]	Dgtl In	HiZ digital	HiZ Analog Unb
P12[5]	5	SCSI_In_DBx[4]	Dgtl In	HiZ digital	HiZ Analog Unb
P12[6]	29	SIO [unused]			HiZ Analog Unb
P12[7]	30	SIO [unused]			HiZ Analog Unb
P15[0]	42	GPIO [unused]			HiZ Analog Unb
P15[1]	43	GPIO [unused]			HiZ Analog Unb
P15[2]	55	GPIO [unused]			HiZ Analog Unb
P15[3]	56	GPIO [unused]			HiZ Analog Unb
P15[4]	93	SCSI_Out[1]	Software Output	Strong drive	HiZ Analog Unb
P15[5]	94	SCSI_Out[0]	Dgtl Out	Strong drive	HiZ Analog Unb
P15[6]	35	USB:D+	Reserved		
P15[7]	36	USB:D-	Reserved		
P2[0]	95	SCSI_Noise[0]	Dgtl In	HiZ digital	HiZ Analog Unb
P2[1]	96	SCSI_In[0]	Dgtl In	HiZ digital	HiZ Analog Unb
P2[2]	97	SCSI_Out_DBx[7]	Dgtl Out	Strong drive	HiZ Analog Unb
P2[3]	98	SCSI_Out_DBx[6]	Dgtl Out	Strong drive	HiZ Analog Unb
P2[4]	99	SCSI_In_DBx[7]	Dgtl In	HiZ digital	HiZ Analog Unb
P2[5]	1	SCSI_In_DBx[6]	Dgtl In	HiZ digital	HiZ Analog Unb
P2[6]	2	SCSI_Out_DBx[5]	Dgtl Out	Strong drive	HiZ Analog Unb
P2[7]	3	SCSI_Out_DBx[4]	Dgtl Out	Strong drive	HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P3[0]	44	GPIO [unused]			Pulled Up
P3[1]	45	SD_MISO	Dgtl In	HiZ digital	Pulled Up
P3[2]	46	SD_SCK	Dgtl Out	Strong drive	Pulled Up
P3[3]	47	SD_MOSI	Dgtl Out	Strong drive	Pulled Up
P3[4]	48	SD_CS	Software In/Out	Strong drive	Pulled Up
P3[5]	49	SD_CD	Software Input	HiZ digital	Pulled Up
P3[6]	51	GPIO [unused]			Pulled Up
P3[7]	52	GPIO [unused]			Pulled Up
P4[0]	69	GPIO [unused]			HiZ Analog Unb
P4[1]	70	GPIO [unused]			HiZ Analog Unb
P4[2]	80	SCSI_In[2]	Software Input	HiZ digital	HiZ Analog Unb
P4[3]	81	SCSI_Noise[2]	Dgtl In	HiZ digital	HiZ Analog Unb
P4[4]	82	SCSI_Out[5]	Dgtl Out	Strong drive	HiZ Analog Unb
P4[5]	83	SCSI_Out[4]	Software Output	Strong drive	HiZ Analog Unb
P4[6]	84	SCSI_In[1]	Software Input	HiZ digital	HiZ Analog Unb
P4[7]	85	SCSI_Noise[3]	Dgtl In	HiZ digital	HiZ Analog Unb
P5[0]	16	SCSI_Out_DBx[1]	Dgtl Out	Strong drive	HiZ Analog Unb
P5[1]	17	SCSI_Out_DBx[0]	Dgtl Out	Strong drive	HiZ Analog Unb
P5[2]	18	SCSI_In_DBx[1]	Dgtl In	HiZ digital	HiZ Analog Unb
P5[3]	19	SCSI_In_DBx[0]	Dgtl In	HiZ digital	HiZ Analog Unb
P5[4]	31	GPIO [unused]			HiZ Analog Unb
P5[5]	32	GPIO [unused]			HiZ Analog Unb
P5[6]	33	GPIO [unused]			HiZ Analog Unb
P5[7]	34	GPIO [unused]			HiZ Analog Unb
P6[0]	89	SCSI_Out[3]	Software Output	Strong drive	HiZ Analog Unb
P6[1]	90	SCSI_Out[2]	Software Output	Strong drive	HiZ Analog Unb
P6[2]	91	SCSI_Noise[4]	Dgtl In	HiZ digital	HiZ Analog Unb
P6[3]	92	SCSI_Noise[1]	Dgtl In	HiZ digital	HiZ Analog Unb
P6[4]	6	SCSI_Out_DBx[3]	Dgtl Out	Strong drive	HiZ Analog Unb
P6[5]	7	SCSI_Out_DBx[2]	Dgtl Out	Strong drive	HiZ Analog Unb
P6[6]	8	SCSI_In_DBx[3]	Dgtl In	HiZ digital	HiZ Analog Unb
P6[7]	9	SCSI_In_DBx[2]	Dgtl In	HiZ digital	HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ digital = High impedance digital
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- OD, DL = Open drain, drives low
- Dgtl Out = Digital Output
- Dgtl In = Digital Input

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
EXTLED	P0[0]	Software In/Out	HiZ Analog Unb
GPIO [unused]	P5[4]		HiZ Analog Unb
GPIO [unused]	P15[1]		HiZ Analog Unb
GPIO [unused]	P1[7]		HiZ Analog Unb
GPIO [unused]	P3[0]		Pulled Up
GPIO [unused]	P5[5]		HiZ Analog Unb
GPIO [unused]	P15[3]		HiZ Analog Unb
GPIO [unused]	P15[2]		HiZ Analog Unb
GPIO [unused]	P5[6]		HiZ Analog Unb
GPIO [unused]	P5[7]		HiZ Analog Unb
GPIO [unused]	P1[6]		HiZ Analog Unb
GPIO [unused]	P4[1]		HiZ Analog Unb
GPIO [unused]	P3[6]		Pulled Up
GPIO [unused]	P15[0]		HiZ Analog Unb
GPIO [unused]	P4[0]		HiZ Analog Unb
GPIO [unused]	P1[5]		HiZ Analog Unb
GPIO [unused]	P1[2]		HiZ Analog Unb
GPIO [unused]	P3[7]		Pulled Up
GPIO [unused]	P1[4]		HiZ Analog Unb
LED1	P0[1]	Software Output	HiZ Analog Unb
SCSI_In[0]	P2[1]	Dgtl In	HiZ Analog Unb
SCSI_In[1]	P4[6]	Software Input	HiZ Analog Unb
SCSI_In[2]	P4[2]	Software Input	HiZ Analog Unb
SCSI_In[3]	P0[5]	Software Input	HiZ Analog Unb
SCSI_In[4]	P0[4]	Software Input	HiZ Analog Unb
SCSI_In_DBx[0]	P5[3]	Dgtl In	HiZ Analog Unb
SCSI_In_DBx[1]	P5[2]	Dgtl In	HiZ Analog Unb
SCSI_In_DBx[2]	P6[7]	Dgtl In	HiZ Analog Unb
SCSI_In_DBx[3]	P6[6]	Dgtl In	HiZ Analog Unb
SCSI_In_DBx[4]	P12[5]	Dgtl In	HiZ Analog Unb
SCSI_In_DBx[5]	P12[4]	Dgtl In	HiZ Analog Unb
SCSI_In_DBx[6]	P2[5]	Dgtl In	HiZ Analog Unb
SCSI_In_DBx[7]	P2[4]	Dgtl In	HiZ Analog Unb
SCSI_Noise[0]	P2[0]	Dgtl In	HiZ Analog Unb
SCSI_Noise[1]	P6[3]	Dgtl In	HiZ Analog Unb
SCSI_Noise[2]	P4[3]	Dgtl In	HiZ Analog Unb
SCSI_Noise[3]	P4[7]	Dgtl In	HiZ Analog Unb

Name	Port	Type	Reset State
SCSI_Noise[4]	P6[2]	Dgtl In	HiZ Analog Unb
SCSI_Out[0]	P15[5]	Dgtl Out	HiZ Analog Unb
SCSI_Out[1]	P15[4]	Software Output	HiZ Analog Unb
SCSI_Out[2]	P6[1]	Software Output	HiZ Analog Unb
SCSI_Out[3]	P6[0]	Software Output	HiZ Analog Unb
SCSI_Out[4]	P4[5]	Software Output	HiZ Analog Unb
SCSI_Out[5]	P4[4]	Dgtl Out	HiZ Analog Unb
SCSI_Out[6]	P0[7]	Software Output	HiZ Analog Unb
SCSI_Out[7]	P0[6]	Dgtl Out	HiZ Analog Unb
SCSI_Out[8]	P0[3]	Dgtl Out	HiZ Analog Unb
SCSI_Out[9]	P0[2]	Dgtl Out	HiZ Analog Unb
SCSI_Out_DBx[0]	P5[1]	Dgtl Out	HiZ Analog Unb
SCSI_Out_DBx[1]	P5[0]	Dgtl Out	HiZ Analog Unb
SCSI_Out_DBx[2]	P6[5]	Dgtl Out	HiZ Analog Unb
SCSI_Out_DBx[3]	P6[4]	Dgtl Out	HiZ Analog Unb
SCSI_Out_DBx[4]	P2[7]	Dgtl Out	HiZ Analog Unb
SCSI_Out_DBx[5]	P2[6]	Dgtl Out	HiZ Analog Unb
SCSI_Out_DBx[6]	P2[3]	Dgtl Out	HiZ Analog Unb
SCSI_Out_DBx[7]	P2[2]	Dgtl Out	HiZ Analog Unb
SD_CD	P3[5]	Software Input	Pulled Up
SD_CS	P3[4]	Software In/Out	Pulled Up
SD_MISO	P3[1]	Dgtl In	Pulled Up
SD_MOSI	P3[3]	Dgtl Out	Pulled Up
SD_SCK	P3[2]	Dgtl Out	Pulled Up
SIO [unused]	P12[2]		HiZ Analog Unb
SIO [unused]	P12[6]		HiZ Analog Unb
SIO [unused]	P12[7]		HiZ Analog Unb
SIO [unused]	P12[3]		HiZ Analog Unb
SIO [unused]	P12[0]		HiZ Analog Unb
SIO [unused]	P12[1]		HiZ Analog Unb
USB:D-	P15[7]	Reserved	
USB:D+	P15[6]	Reserved	

Abbreviations used in Table 5 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	False
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x0400
Stack Size (bytes)	0x1000
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

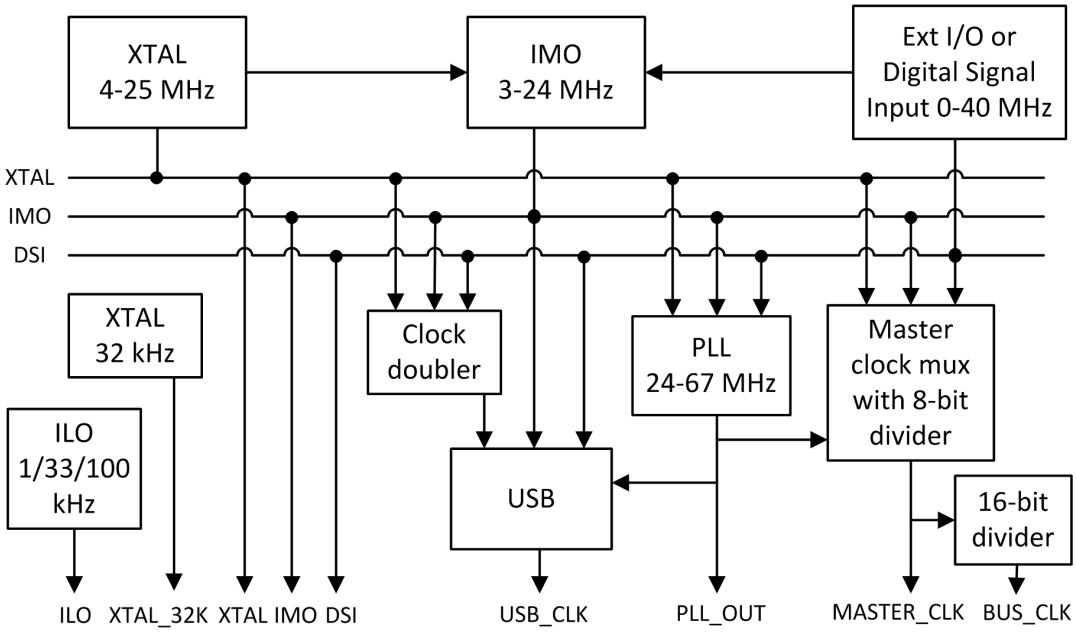
Name	Value
Variable VDDA	False
VDDA (V)	5
VDDD (V)	5
VDDIO0 (V)	5
VDDIO1 (V)	5
VDDIO2 (V)	5
VDDIO3 (V)	3.3
Temperature Range	0C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	50 MHz	±0.25	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	50 MHz	±0.25	True	True
PLL_OUT	DIGITAL	IMO	50 MHz	50 MHz	±0.25	True	True
USB_CLK	DIGITAL	IMO	48 MHz	48 MHz	±0.25	False	True
IMO	DIGITAL		24 MHz	24 MHz	±0.25	True	True
ILO	DIGITAL		? MHz	100 kHz	-55,+100	True	True
XTAL 32kHz	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False
XTAL	DIGITAL		25 MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

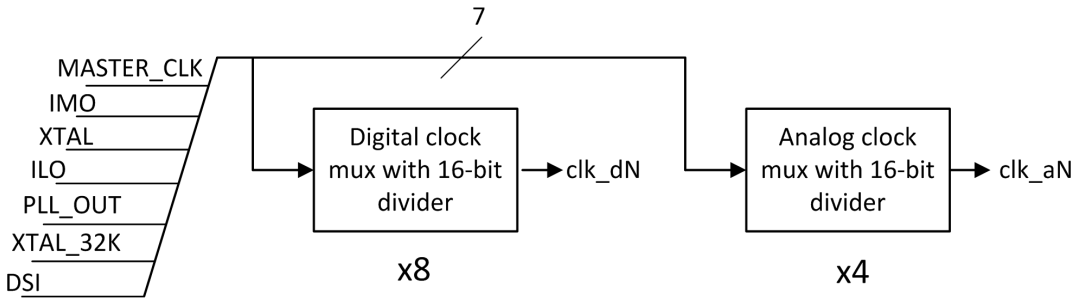


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
Clock_4	DIGITAL	BUS_CLK	? MHz	50 MHz	±0.25	True	True
Clock_3	DIGITAL	BUS_CLK	? MHz	50 MHz	±0.25	True	True
SD_Data_Clk	DIGITAL	MASTER_CLK	50 MHz	50 MHz	±0.25	True	True
SCSI_CLK	DIGITAL	MASTER_CLK	25 MHz	25 MHz	±0.25	True	True
timer_clock	DIGITAL	IMO	1 MHz	1 MHz	±0.25	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - o CyPLL API routines
  - o CyIMO API routines

- CyILO API routines
- CyMaster API routines
- CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Priority	Vector
USBFS_arb_int	6	22
Debug_Timer_Interrupt	7	1
SCSI_RST_ISR	7	2
SCSI_RX_DMA_COMPLETE	7	0
SCSI_SEL_ISR	7	3
SCSI_TX_DMA_COMPLETE	7	4
SD_RX_DMA_COMPLETE	7	5
SD_TX_DMA_COMPLETE	7	6
USBFS_bus_reset	7	23
USBFS_dp_int	7	12
USBFS_ep_0	7	24
USBFS_ep_1	7	7
USBFS_ep_2	7	8
USBFS_ep_3	7	9
USBFS_ep_4	7	10
USBFS_sof_int	7	21

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 12. DMAs

Name	Priority	Channel Number
SD_RX_DMA	0	2
SD_TX_DMA	1	3
SCSI_RX_DMA	2	0
SCSI_TX_DMA	2	1

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the PSoC 5 Technical Reference Manual
- DMA chapter in the System Reference Guide
  - DMA API routines and related registers
- Datasheet for cy_dma component

6 Flash Memory

PSoC 5 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 13 lists the Flash protection settings for your design.

Table 13. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x1FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

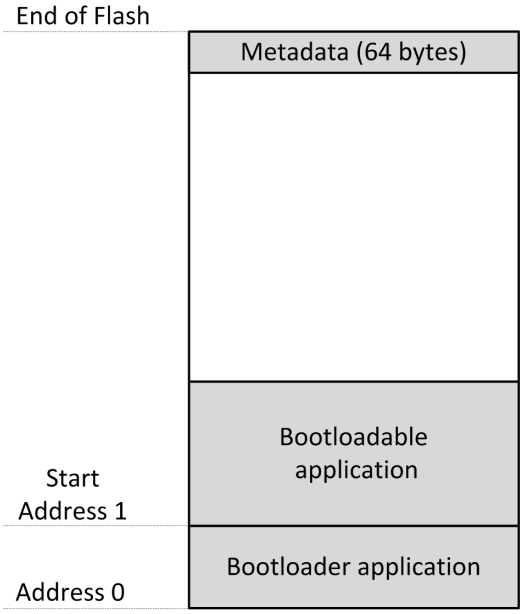
For more information on Flash memory and protection, please refer to:

- Flash Protection chapter in the PSoC 5 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Bootloader and Bootloadable

Figure 5 details the Flash memory map for the bootloader and/or bootloadable application(s) included in this design.

Figure 5. Bootloader Memory Map



7.1 Bootloadable Application

Table 14. Bootloadable Settings

Name	Value
Application Version	0x0450
Application ID	0xD15C
Application Custom ID	0x1
Application Image 1 Start Address	0x0
Application Image 1 End Address	0x1FEFF
Manual Application Image Placement	False

7.2 Bootloader Application

Table 15. Bootloader Settings

Name	Value
Checksum Type	BasicChecksum
Supports Multiple Application Images	False
Application Version	0x0450
Bootloader Start Address	0x0
Bootloader End Address	0x0

For more information on the bootloader and startup please refer to:

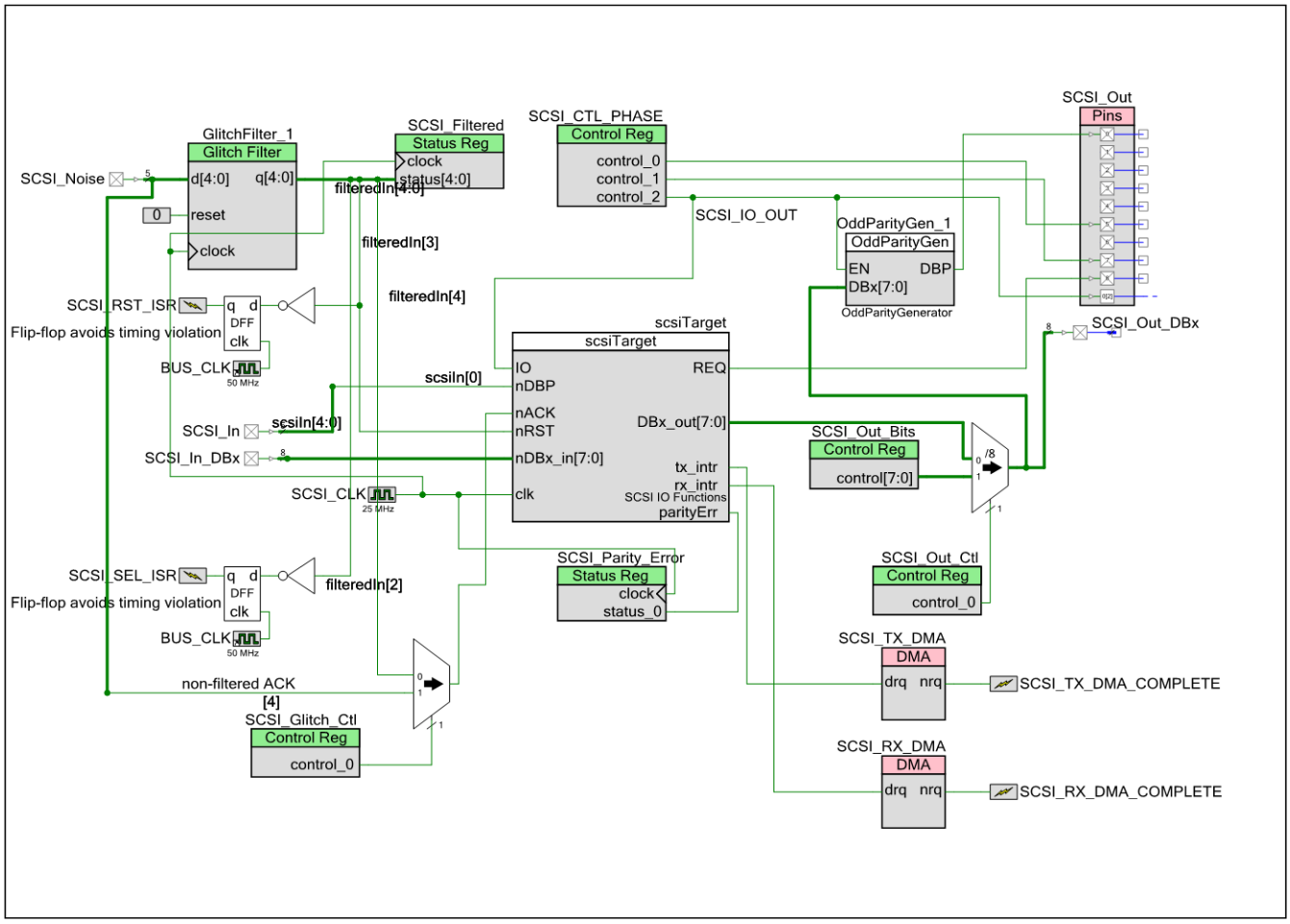
- Startup and Linking chapter in the System Reference Guide
- Datasheet for Bootloader and Bootloadable component

8 Design Contents

This design's schematic content consists of the following 3 schematic sheets:

8.1 Schematic Sheet: SCSI Connections

Figure 6. Schematic Sheet: SCSI Connections

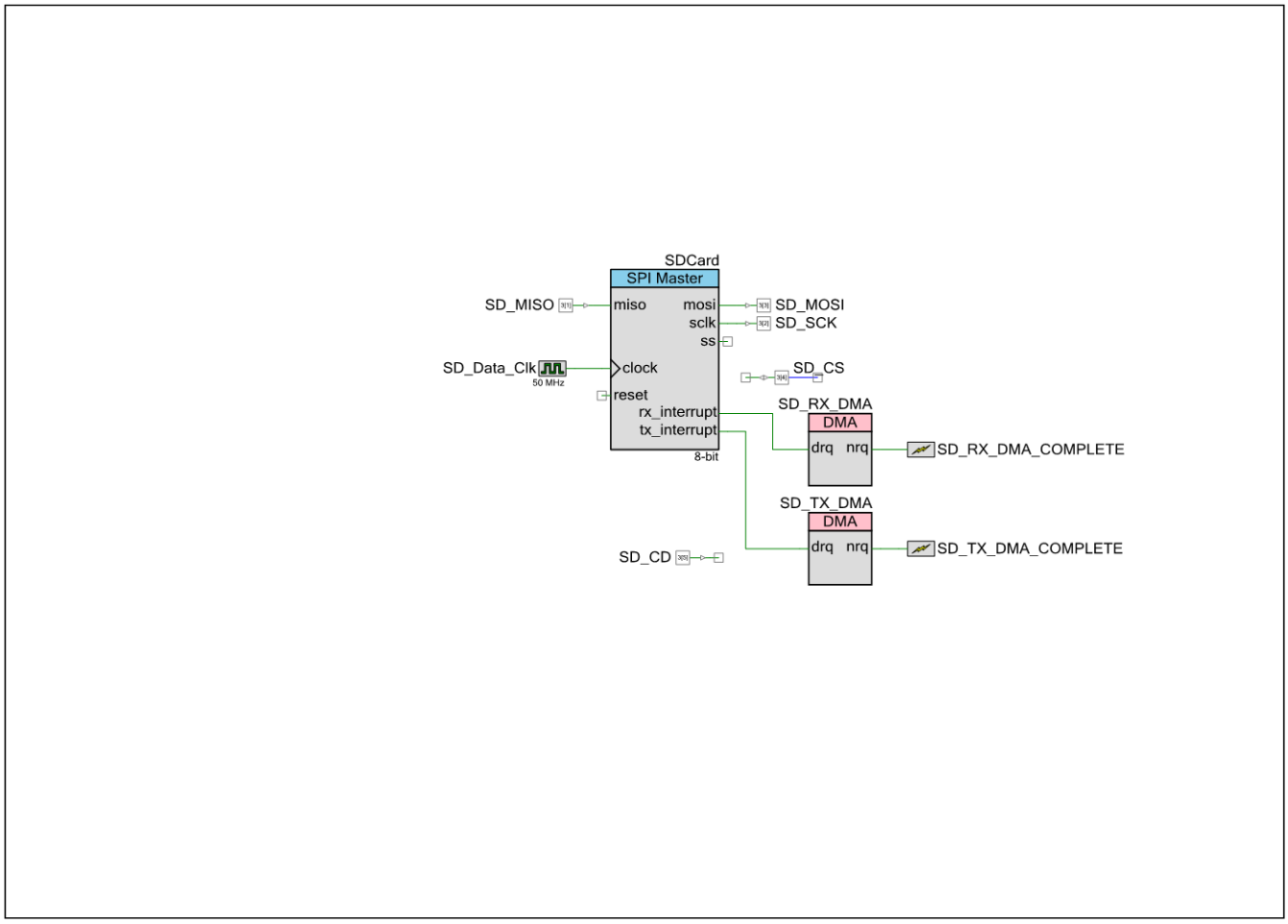


This schematic sheet contains the following component instances:

- Instance GlitchFilter_1 (type: GlitchFilter_v2_0)
- Instance OddParityGen_1 (type: OddParityGen)
- Instance SCSI_CTL_PHASE (type: CyControlReg_v1_80)
- Instance SCSI_Filtered (type: CyStatusReg_v1_90)
- Instance SCSI_Glitch_Ctl (type: CyControlReg_v1_80)
- Instance SCSI_Out_Bits (type: CyControlReg_v1_80)
- Instance SCSI_Out_Ctl (type: CyControlReg_v1_80)
- Instance SCSI_Parity_Error (type: CyStatusReg_v1_90)
- Instance scsiTarget (type: scsiTarget)

8.2 Schematic Sheet: SD Card Connections

Figure 7. Schematic Sheet: SD Card Connections

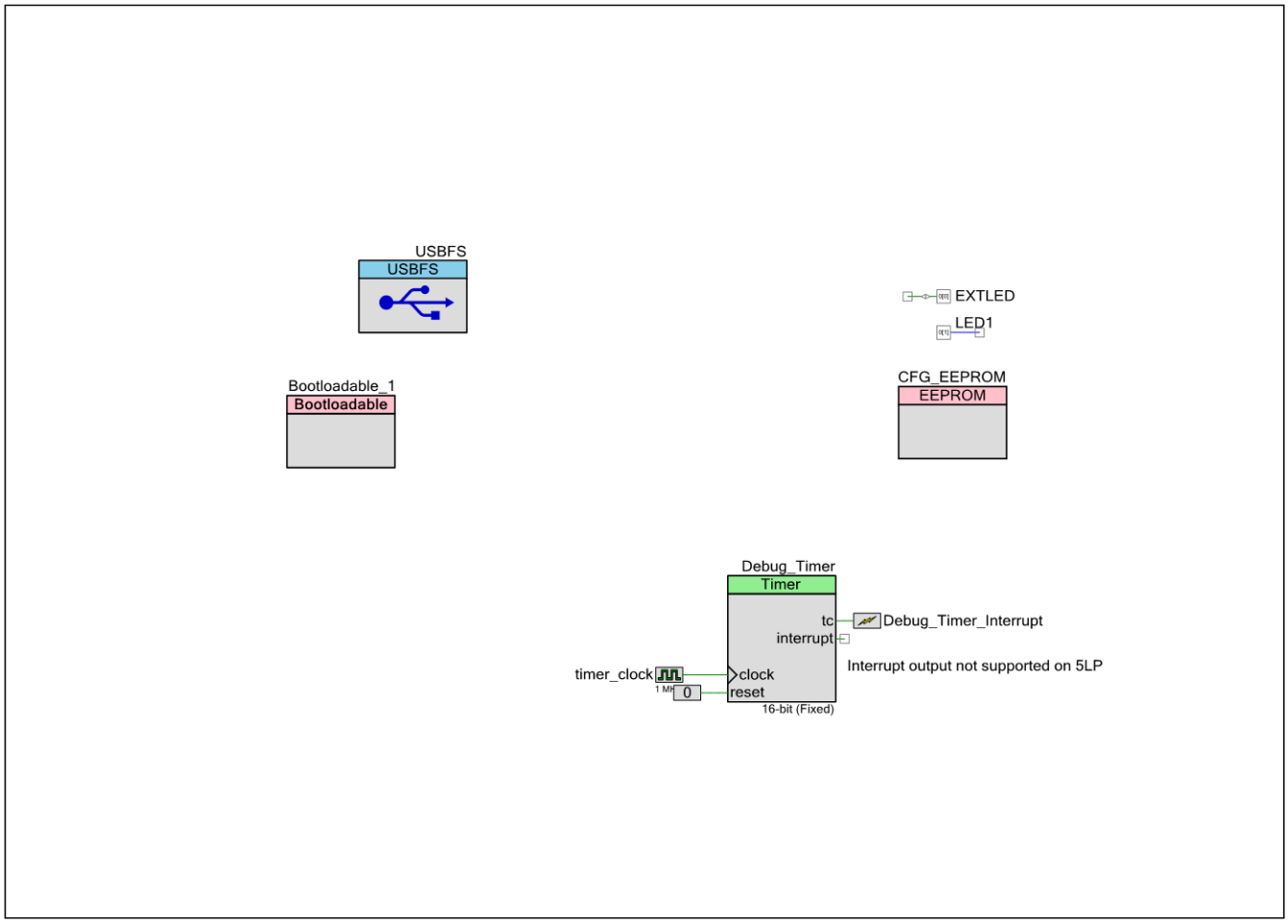


This schematic sheet contains the following component instances:

- Instance SDCard (type: SPI_Master_v2_50)

8.3 Schematic Sheet: MISC Stuff

Figure 8. Schematic Sheet: MISC Stuff



This schematic sheet contains the following component instances:

- Instance Bootloadable_1 (type: Bootloadable_v1_50)
- Instance CFG_EEPROM (type: EEPROM_v3_0)
- Instance Debug_Timer (type: Timer_v2_70)
- Instance USBFS (type: USBFS_v3_0)

9 Components

9.1 Component type: Bootloadable [v1.50]

9.1.1 Instance Bootloadable_1

Description: Provides bootloadable application functionality.
Instance type: Bootloadable [v1.50]
Datasheet: online component datasheet for Bootloadable

Table 16. Component Parameters for Bootloadable_1

Parameter Name	Value	Description
appCustomID	1	Provides a 4 byte custom ID number to represent anything in the Bootloadable application.
appID	53596	Provides a 2 byte number to represent the ID of the bootloadable application.
appVersion	1104	Provides a 2 byte number to represent the version of the bootloadable application.
autoPlacement	true	Provides a method for PSoC Creator to place a Bootloadable application image at a specified location. If true, the image will be placed automatically. If false, the image will be placed at an address specified by the Placement Address option.
checksumExcludeSize	0	Provides a size in bytes of checksum exclude section
elfFilePath	..\..\..\Data Sheets\apple\SCSI2SD\USB_-Bootloader-V4.elf	Provides a reference to the Bootloader application (.elf) that is associated with this Bootloadable application.
hexFilePath	..\..\..\Data Sheets\apple\SCSI2SD\USB_-Bootloader-V4.hex	Provides a reference to the Bootloader application (.hex) that is associated with this Bootloadable application.
placementAddress	0	Allows specifying an address where the bootloadable application will be placed in the memory. Available only if the Automatic Application Image Placement option is true.

9.2 Component type: CyControlReg [v1.80]

9.2.1 Instance SCSI_CTL_PHASE

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 17. Component Parameters for SCSI_CTL_PHASE

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	3	Defines the number of outputs needed (1-8)

9.2.2 Instance SCSI_Glitch_Ctl

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 18. Component Parameters for SCSI_Glitch_Ctl

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.2.3 Instance SCSI_Out_Bits

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 19. Component Parameters for SCSI_Out_Bits

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode

Parameter Name	Value	Description
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	true	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	8	Defines the number of outputs needed (1-8)

9.2.4 Instance SCSI_Out_Ctl

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 20. Component Parameters for SCSI_Out_Ctl

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

9.3 Component type: CyStatusReg [v1.90]

9.3.1 Instance SCSI_Filtered

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.90]
Datasheet: online component datasheet for CyStatusReg

Table 21. Component Parameters for SCSI_Filtered

Parameter Name	Value	Description
Bit0Mode	Transparent	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register

Parameter Name	Value	Description
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	true	Displays the input terminals as bus
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	5	Defines the number of status inputs (1-8)

9.3.2 Instance SCSI_Parity_Error

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.90]
Datasheet: online component datasheet for CyStatusReg

Table 22. Component Parameters for SCSI_Parity_Error

Parameter Name	Value	Description
Bit0Mode	Sticky (Clear on Read)	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	1	Defines the number of status inputs (1-8)

9.4 Component type: EEPROM [v3.0]

9.4.1 Instance CFG_EEPROM

Description: Provides an API to Erase and Write EEPROM.

Instance type: EEPROM [v3.0]
Datasheet: online component datasheet for EEPROM

9.5 Component type: GlitchFilter [v2.0]

9.5.1 Instance GlitchFilter_1

Description: Removes unwanted pulses from a digital signal
Instance type: GlitchFilter [v2.0]
Datasheet: online component datasheet for GlitchFilter

Table 23. Component Parameters for GlitchFilter_1

Parameter Name	Value	Description
BypassFilter	None	Specifies the logic level to be directly propagated to the output.
GlitchLength	3	Defines the number of samples for which input has to be stable before being propagated to the output.
SignalWidth	5	Determines the bus width of d and q terminals.

9.6 Component type: OddParityGen [v0.0]

9.6.1 Instance OddParityGen_1

Description: (custom component)
Instance type: OddParityGen [v0.0]
Datasheet: (not available)

9.7 Component type: scsiTarget [v0.0]

9.7.1 Instance scsiTarget

Description: (custom component)
Instance type: scsiTarget [v0.0]
Datasheet: (not available)

9.8 Component type: SPI_Master [v2.50]

9.8.1 Instance SDCard

Description: Serial Peripheral Interface Master
Instance type: SPI_Master [v2.50]
Datasheet: online component datasheet for SPI_Master

Table 24. Component Parameters for SDCard

Parameter Name	Value	Description
BidirectMode	false	Bidirectional mode setting
ClockInternal	false	Allow use of the internal clock and desired bit rate or an external clock source
DesiredBitRate	12000000	Desired Bit Rate in bps

Parameter Name	Value	Description
HighSpeedMode	true	Enables using of the High Speed Mode
InterruptOnByteComplete	false	Set Initial Interrupt Source to Enable Interrupt on Byte Transfer Complete
InterruptOnRXFull	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Full
InterruptOnRXNotEmpty	true	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Not Empty
InterruptOnRXOverrun	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Overrun
InterruptOnSPIDone	false	Set Initial Interrupt Source to Enable Interrupt on SPI Done
InterruptOnSPIIdle	false	Set Initial Interrupt Source to Enable Interrupt on SPI Idle
InterruptOnTXEmpty	true	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Empty
InterruptOnTXNotFull	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Not Full
Mode	CPHA = 0, CPOL = 0	SPI mode defines the Clock Phase and Clock Polarity desired
NumberOfDataBits	8	Set the Number of Data bits 3-16
RxBufferSize	4	Defines the amount of RAM Set asside for the RX Buffer
ShiftDir	MSB First	Set the Shift Out Direction
TxBufferSize	4	Defines the amount of RAM Set asside for the TX Buffer
UseRxInternalInterrupt	false	Defines whether Rx internal interrupt is used or not
UseTxInternalInterrupt	false	Defines whether Tx internal interrupt is used or not

9.9 Component type: Timer [v2.70]

9.9.1 Instance Debug_Timer

Description: 8, 16, 24 or 32-bit Timer
Instance type: Timer [v2.70]
Datasheet: online component datasheet for Timer

Table 25. Component Parameters for Debug_Timer

Parameter Name	Value	Description
CaptureAlternatingFall	false	Enables data capture on either edge but not until a valid falling edge is detected first.
CaptureAlternatingRise	false	Enables data capture on either edge but not until a valid rising edge is detected first.

Parameter Name	Value	Description
CaptureCount	2	The CaptureCount parameter works as a divider on the hardware input "capture". A CaptureCount value of 2 would result in an actual capture taking place every other time the input "capture" is changed.
CaptureCounterEnabled	false	Enables the capture counter to count capture events (up to 127) before a capture is triggered.
CaptureMode	None	This parameter defines the capture input signal requirements to trigger a valid capture event
EnableMode	Software Only	This parameter specifies the methods in enabling the component. Hardware mode makes the enable input pin visible. Software mode may reduce the resource usage if not enabled.
FixedFunction	true	Configures the component to use fixed function HW block instead of the UDB implementation.
InterruptOnCapture	false	Parameter to check whether interrupt on a capture event is enabled or disabled.
InterruptOnFIFOFull	false	Parameter to check whether interrupt on a FIFO Full event is enabled disabled.
InterruptOnTC	false	Parameter to check whether interrupt on a TC is enabled or disabled.
NumberOfCaptures	1	Number of captures allowed until the counter is cleared or disabled.
Period	31999	Defines the timer period (This is also the reload value when terminal count is reached)
Resolution	16	Defines the resolution of the hardware. This parameter affects how many bits are used in the Period counter and defines the maximum resolution of the internal component signals.
RunMode	Continuous	Defines the hardware to run continuously, run until a terminal count is reached or run until an interrupt event is triggered.
TriggerMode	None	Defines the required trigger input signal to cause a valid trigger enable of the timer

9.10 Component type: USBFS [v3.0]

9.10.1 Instance USBFS

Description: USB 2.0 Full Speed Device Framework
Instance type: USBFS [v3.0]
Datasheet: online component datasheet for USBFS

Table 26. Component Parameters for USBFS

Parameter Name	Value	Description
EnableBatteryChargDetect	false	This parameter allows to detect a charging supported USB host port using the API function USBFS_DetectPortType().
EnableCDCApi	true	Enables additional high level API's that allow the CDC device to be used similar to a UART device.
EnableMidiApi	true	Enables additional high level MIDI API's.
endpointMA	MA_Static	Endpoint memory allocation
endpointMM	EP_Manual	Endpoint memory management
epDMAautoOptimization	false	This parameter enables resource optimization for DMA with Automatic Memory Management mode. Set this parameter value to true only when a single IN endpoint is present in the device. Enabling this parameter in a multi IN endpoint device configuration causes undesired effects.
extern_cls	false	This parameter allows for user or other component to implement his own handler for Class requests. USBFS_-DispatchClassRqst() function should be implemented if this parameter enabled.
extern_vbus	false	This parameter enables external VBUSDET input.
extern_vnd	false	This parameter allows for user or other component to implement his own handler for Vendor specific requests. USBFS_HandleVendorRqst() function should be implemented if this parameter enabled.
extJackCount	0	Max number of External MIDI IN Jack or OUT Jack descriptors
Gen16bitEpAccessApi	false	This parameter defines whether to generate APIs for the 16-bits endpoint access.
HandleMscRequests	true	This parameter is used to enable handling MSC requests and generate MSC APIs.
isrGroupArbiter	High	This parameter defines the interrupt group of the Arbiter Interrupt.

Parameter Name	Value	Description
isrGroupBusReset	Low	This parameter defines the interrupt group of the Bus Reset Interrupt.
isrGroupEp0	Medium	This parameter defines the interrupt group of the Control Endpoint Interrupt (EP0).
isrGroupEp1	Medium	This parameter defines the interrupt group of the Data Endpoint 1 Interrupt.
isrGroupEp2	Medium	This parameter defines the interrupt group of the Data Endpoint 2 Interrupt.
isrGroupEp3	Medium	This parameter defines the interrupt group of the Data Endpoint 3 Interrupt.
isrGroupEp4	Medium	This parameter defines the interrupt group of the Data Endpoint 4 Interrupt.
isrGroupEp5	Medium	This parameter defines the interrupt group of the Data Endpoint 5 Interrupt.
isrGroupEp6	Medium	This parameter defines the interrupt group of the Data Endpoint 6 Interrupt.
isrGroupEp7	Medium	This parameter defines the interrupt group of the Data Endpoint 7 Interrupt.
isrGroupEp8	Medium	This parameter defines the interrupt group of the Data Endpoint 8 Interrupt.
isrGroupLpm	High	This parameter defines the interrupt group of the LPM Interrupt.
isrGroupSof	Low	This parameter defines the interrupt group of the Start of Frame Interrupt.
max_interfaces_num	2	Defines maximum interfaces number
Mode	false	Specifies whether the implementation will create API for interfacing to UART component(s) for a corresponding set of external MIDI connections.
mon_vbus	false	The mon_vbus parameter adds a single VBUS monitor pin to the design. This pin must be connected to VBUS and must be assigned in the pin editor.
MscDescriptors		Mass Storage Class Descriptors
MscLogicalUnitsNum	1	This parameter allows to specify the number of logical units that should be supported by the Mass Storage device.
out_sof	false	The out_sof parameter enables Start-of-Frame output.
Pid	F232	Product ID

Parameter Name	Value	Description
powerpad_vbus	false	This parameter enables VBUS power pad
ProdactName		This string is displayed by the Operating System when it is installing the mass storage device as the Product Name.
ProdactRevision		This string is displayed by the Operating System when it is installing the mass storage device as the Product Revision.
rm_lpm_int	true	Removes LPM ISR
VendorName		This string is displayed by the Operating System when it is installing the mass storage device as the Vendor Name.
Vid	04B4	Vendor ID

10 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5 register map is covered in the PSoC 5 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5 Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine