L1 Cache with Write-back and LRU Policies Python Simulator

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ECE 485 Microprocessor System Design

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Contents

1 Experimental Data and Results

1.1 Impact of cache capacity

Table 1: Trace 1 results.

| Miss ratio	Capacity (KB)
4.8	4
2.8	8
2.1	16
1.8	32
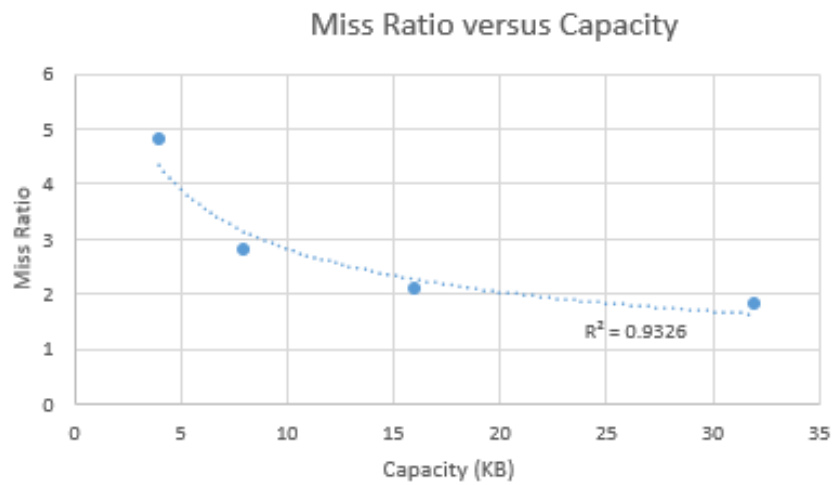
Table 2: Trace 2 results.

Miss ratio	Capacity (KB)
7.4	4
5.9	8
4.8	16
3.1	32

Miss Ratio versus Capacity

$R^2 = 0.9653$
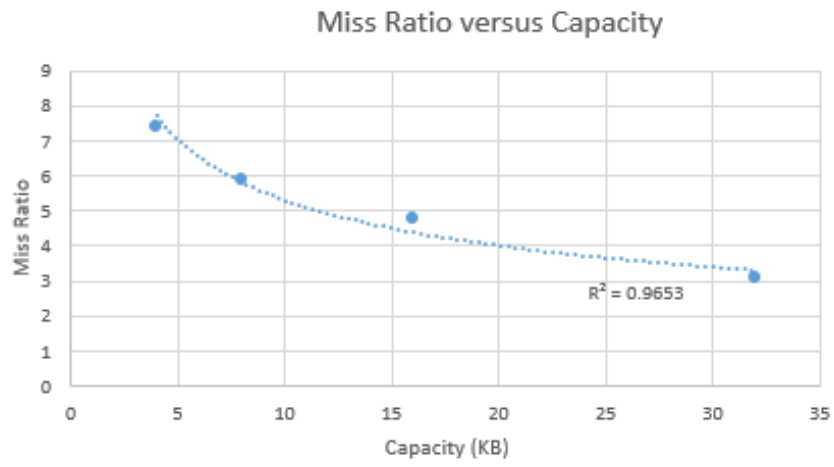
1.2 Impact of associativity

Table 3: Trace 1 results.

Miss ratio	Associativity
4.8	1
1.9	2
1.3	4
1.2	8

Miss Ratio versus Associativity

$R^2 = 0.8496$
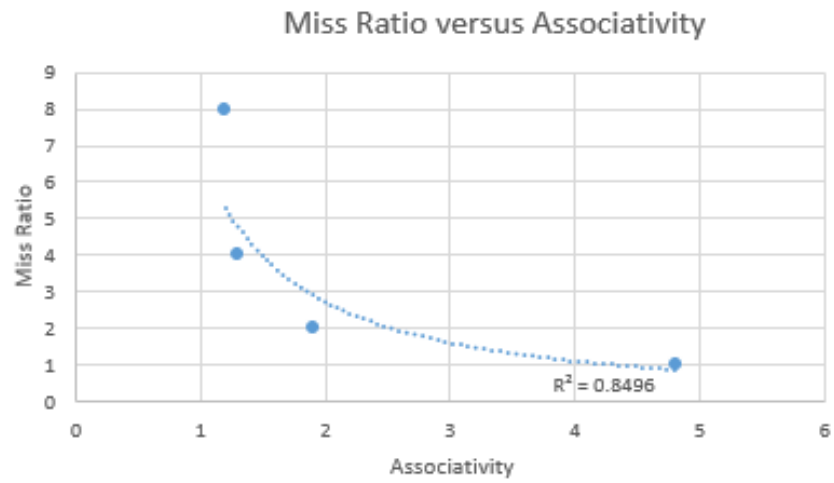
Table 4: Trace 2 results.

Miss ratio	Associativity
7.4	1
4.9	2
3.2	4
1.9	8

Miss Ratio versus Associativity
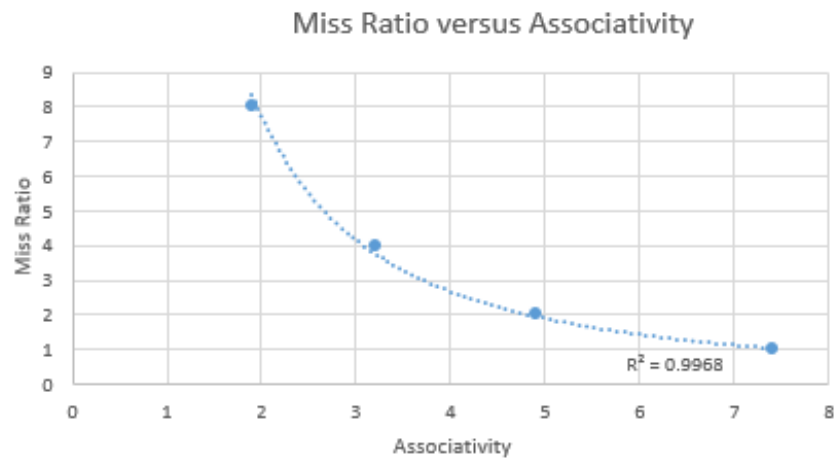
1.3   Impact of line size

Table 5: Trace 1 results.

| Miss ratio	Line Size (B)
8.0	32
4.8	64
2.6	128

Miss Ratio versus Line Size
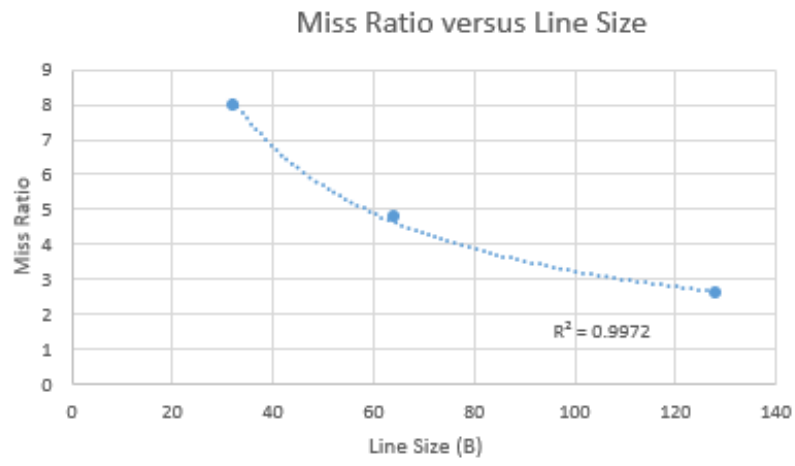
Table 6: Trace 2 results.

Miss ratio	Line Size (B)
15.0	32
7.4	64
4.2	128

Miss Ratio versus Line Size
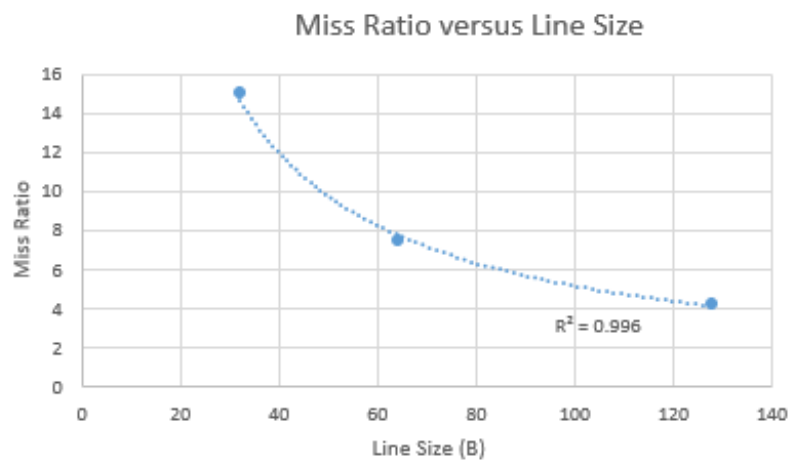
1.4 Working set size

For every pair of averages (e.g. Problem 1: Trace 1 and Trace 2 as shown below) Trace 1 exhibited a lower miss ratio, which implies that there is less memory required for trace 1. This means that Trace 2 requires more memory as it exhibits a larger miss ratio. In other words, Trace 2 is the larger working set size.

Problem 1:

Average MR for Trace 1: $(4.8 + 2.8 + 2.1 + 1.8) / 4 = 2.9$
Average MR for Trace 2: $(7.4 + 5.9 + 4.8 + 3.1) / 4 = 5.3$

Problem 2:

Average MR for Trace 1: $(4.8 + 1.9 + 1.3 + 1.2) / 4 = 2.3$
Average MR for Trace 2: $(7.4 + 4.9 + 3.2 + 1.9) / 4 = 4.4$

Problem 3:

Average MR for Trace 1: $(8 + 4.8 + 2.6) / 3 = 5.1$
Average MR for Trace 2: $(15 + 7.4 + 4.2) / 3 = 8.8$

1.5 Dirty ratio

As shown below in Table 7 and the accompanying plot of Miss Ratio versus Associativity, the dirty ratio tends to increase as a function of the capacity of the cache. For instance, when the capacity changes from 4 KB to 16 KB, the dirty ratio increases from 0.44 to 0.67. However, at the final data point (32 KB cache size and 0.66 dirty ratio), the dirty ratio slightly decreases from the previous value (0.67). This occurs because as the cache size increases there is more space in the cache to be filled and less cache misses, such as conflicts, occur. By definition, the dirty ratio is write-backs divided by evictions. In this particular implementation, the write-backs decreases slightly between data points while the evictions decrease significantly, causing the faction (i.e. the dirty ratio) to grow. The plateau occurs because the write-backs and evictions do not change significantly following the data point (16 KB, 0.67).

Table 7: Trace 1 results.

Dirty ratio	Capacity (KB)
0.44	4
0.59	8
0.67	16
0.66	32

Dirty Ratio versus Capacity

$R^2 = 0.8101$