

## ARM integer cores

- Outline:
  - ➔ **the ARM 3-stage pipeline**
    - the ARM7TDMI core
    - the ARM 5-stage pipeline
    - the ARM9TDMI core
    - the ARM10TDMI core



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## The 3-stage ARM pipeline

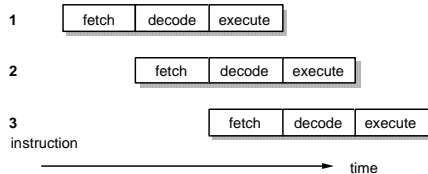
- **fetch**
  - the instruction is fetched from memory
- **decode**
  - the instruction is decoded and the datapath control signals prepared for the next cycle
- **execute**
  - the operands are read from the register bank, shifted, combined in the ALU and the result written back



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## The 3-stage ARM pipeline



- **Single cycle instructions**
  - complete at a rate of one per clock cycle

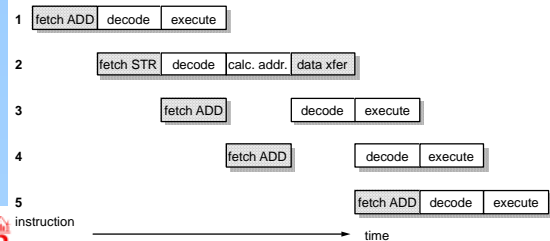


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## The 3-stage ARM pipeline

- **More complex instructions:**



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## The 3-stage ARM pipeline

- **PC behaviour**
  - r15 increments twice before an instruction executes
    - due to pipeline operation
  - therefore r15 = address of instruction + 8
    - (+12 if used after first cycle, though this is architecturally 'undefined')
    - in Thumb code the offset is +4
  - normally the assembler makes the necessary adjustments, e.g. in branches



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## 3-stage ARM organization

- **ARM components:**
  - register bank
    - 2 read ports, 1 write port
    - plus additional read and write ports for r15
  - barrel shifter
  - ALU
  - address register and incrementer
  - memory data registers
  - instruction decoder and control




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[illegible]

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# The ARM7TDMI

- The ARM7TDMI is...
  - an **ARM7** 3-stage pipeline core, with
  - **T** - support for the Thumb instruction set
  - **D** - support for debug
    - the processor can stop on a debug event
  - **M** - support for long multiplies
  - **I** - the EmbeddedICE macrocell
    - provides breakpoint and watchpoint hardware
      - described later



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# ARM7TDMI organization

The diagram illustrates the ARM7TDMI organization and its connections to external components:

- Embedded ICE:** Receives external inputs (extern0, extern1) and provides control signals (opc, r/w, mreq, trans, mas[1:0]) to the processor core. It is connected to scan chain 2.
- processor core:** Receives control signals and provides data signals (A[31:0], D[31:0]) to the JTAG TAP controller. It is connected to scan chain 0 and scan chain 1. It also handles other signals.
- JTAG TAP controller:** Receives data signals (Din[31:0], Dout[31:0]) from the bus splitter and provides control signals (TCK, TMKSTRST, TDI, TDO) to the processor core. It is connected to scan chain 1.
- bus splitter:** Splits the data signals (Din[31:0], Dout[31:0]) between the processor core and the JTAG TAP controller.

Legend:   
TCK TMKSTRST TDI TDO


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# ARM7TDMI

- ARM7TDMI debug support
  - the EmbeddedICE module
    - supports breakpoints and watchpoints
    - controlled via the JTAG test access port
  - EmbeddedICE & JTAG are covered later
- ARM7TDMI characteristics:

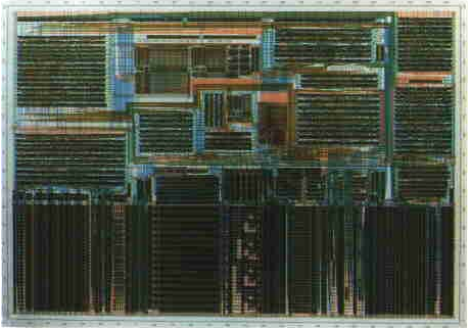
Process	0.35 $\mu\text{m}$	Transistors	74,209 <sub>2</sub>	MIPS	60
Metal layers	3	Core area	2.1 mm <sup>2</sup>	Power	87 mW
Vdd	3.3 V	Clock	0 to 66 MHz	MIPS/W	690



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## ARM7TDMI



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## Getting higher performance

- Increase the clock rate
  - the clock rate is limited by the slowest pipeline stage
    - decrease the logic complexity per stage
    - increase the pipeline depth (number of stages)
- improve the CPI (clocks per instruction)
  - fewer wasted cycles
  - better memory bandwidth



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## The 5-stage ARM pipeline

- Fetch
- Decode
  - instruction decode and register read
- Execute
  - shift and ALU
- Memory
  - data memory access
- Write-back



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## The 5-stage ARM pipeline

- Reducing the CPI
  - ARM7 uses the memory on nearly every clock cycle
    - for either instruction fetch or data transfer
  - therefore a reduced CPI requires **more than one memory access per clock cycle**
- Possible solutions are:
  - separate instruction and data memories
  - double-bandwidth memory (e.g. ARM8)



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## ARM9TDMI

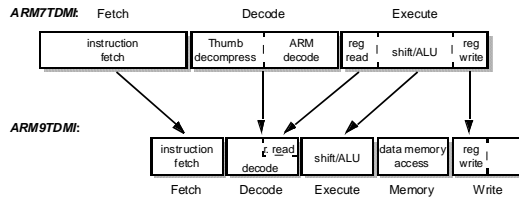
- The ARM9TDMI is...
  - a 'classic' Harvard architecture 5-stage pipeline
    - separate instruction and data memory ports
  - with full support for Thumb and EmbeddedICE debug
  - aimed at significantly higher performance than the ARM7TDMI
    - enhanced pipeline operates at 100-200 MHz



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## ARM9TDMI pipeline



- Thumb instructions are decoded directly

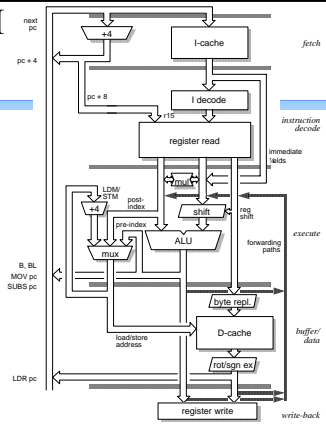


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## ARM9TDMI pipeline

- very similar to StrongARM
  - see CPU section
- no separate branch adder



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## ARM9TDMI

- EmbeddedICE
  - as ARM7TDMI, plus:
    - hardware single-stepping
    - breakpoints on exceptions
- On-chip coprocessor support
  - for floating-point, DSP, and so on

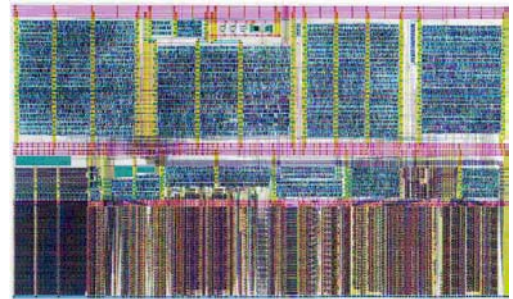
Process	0.25 $\mu\text{m}$	Transistors	111,000	MIPS	220
Metal layers	3	Core area	2.1 mm <sup>2</sup>	Power	150 mW
Vdd	2.5 V	Clock	0-200 MHz	MIPS/W	1,500



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## ARM9TDMI



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## ARM10TDMI

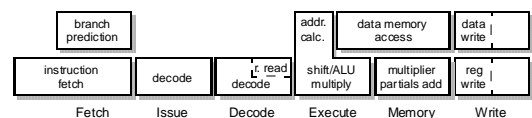
- The ARM10TDMI is...
  - aimed at significantly higher performance than the ARM9TDMI
  - achieved through use of:
    - higher clock rate
    - 64-bit I- and D-memory buses
    - branch prediction
    - hit-under-miss D-memory interface



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## ARM10TDMI pipeline



- Additional time allowed for
  - I- and D-memory accesses
  - instruction decode
- 6-stage pipeline



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