

## UNIT - 1

## REVISION OF LOGIC GATES AND BOOLEAN ALGEBRA

IC - Integrated circuits

SSI Small scale integration logic gates upto 10

MSI Medium Scale integration " " 11 to 100

LSI Large Scale integration " " 101 to  $10^3$ VLSI Very Large Scale integration 1001 to  $10^5$ ULSI Ultra Large Scale integration  $\geq 10^5$ 

Logic gates are made of transistors and diodes

Logic gates :

Basic

AND

OR

NOT

Universal

NAND

NOR

Exclusive

XOR, XNOR

Boolean Algebra :

A, B - i/p

Y - o/p.

$$A \cdot A = A$$

$$A \cdot 0 = 0$$

$$A \cdot \bar{A} = 0$$

$$A \cdot 1 = A$$

$$A + 1 = 1$$

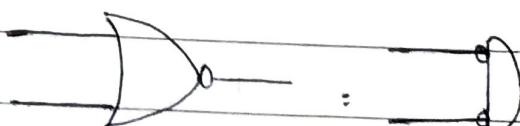
$$A + \bar{A} = 1$$

$$\bar{\bar{A}} = A$$

$$A + \bar{A}B = A + B$$

De Morgan's Theorem

$$i. (\overline{A+B}) = \bar{A} \cdot \bar{B}$$



$$ii. (\overline{A \cdot B}) = \bar{A} + \bar{B}$$



simplify the given boolean eqn

$$\begin{aligned} 1. \quad Y &= A\bar{B}C + A(B + \bar{C}) + A\bar{C} + ABC \\ &= A\bar{B}C + AB + A\bar{C} + A\bar{C} + ABC \\ &= A\bar{B}C + AB + A\bar{C} + ABC \\ &= AC(\bar{B} + B) + AB + A\bar{C} \\ &= AC + AB + A\bar{C} \\ &= A(C + \bar{C}) + AB \\ &= A + AB \\ &= A(1 + B) \\ &= A. \end{aligned}$$

$$\begin{aligned} 2. \quad f &= xyz + \bar{x}\bar{y}z + x(y + \bar{z}) + (\bar{x} + \bar{y}) \\ &= xyz + \bar{x}\bar{y}z + \bar{xy} + xz + \bar{x} \cdot y \\ &= xy(z+1) + \bar{x}\bar{y}z + xz + \bar{xy} \\ &= xy + \bar{x}\bar{y}z + xz + \bar{xy} \\ &= y(x + \bar{x}) + \bar{x}\bar{y}z + xz \\ &= y + z(x + \bar{x}\bar{y}) \quad (\bar{x} + \bar{x}\bar{y}) = \bar{x} + \bar{y} \\ &= y + xz + \cancel{\bar{x}\bar{y}z} \\ &= y(1+z) + xz \quad y + z(y + \bar{y}) + xz \\ &= y + xz \\ &= y + z + xz \\ &= y + z(1+x) \\ &= y + z \end{aligned}$$

SOP and POS expression

Sum of Product (SOP)  $\rightarrow$  NAND  
Product of Sum (POS)  $\rightarrow$  NOR

SOP

Product Term

Min term ( $m$ ): Fundamental product term for which o/p is 1 for given set of i/p's and contain all i/p variable.

$$A = 0 \quad B = 1 \quad C = 0 \quad m_2 = \overline{A} \overline{B} \bar{A} \bar{B} \bar{C}$$

Truth table.

i/p			o/p	
A	B	C	Y	
0	0	0	1	$m_0$
0	0	1	1	$m_1$
0	1	0	0	
0	1	1	0	
1	0	0	1	$m_4$
1	0	1	0	
1	1	0	1	$m_5$
1	1	1	0	

$$Y(A, B, C) = \sum m(0, 1, 4, 5)$$

$$= \overline{A} \overline{B} \bar{C} + \overline{A} \bar{B} C + A \bar{B} \bar{C} + A B \bar{C}$$

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
0	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

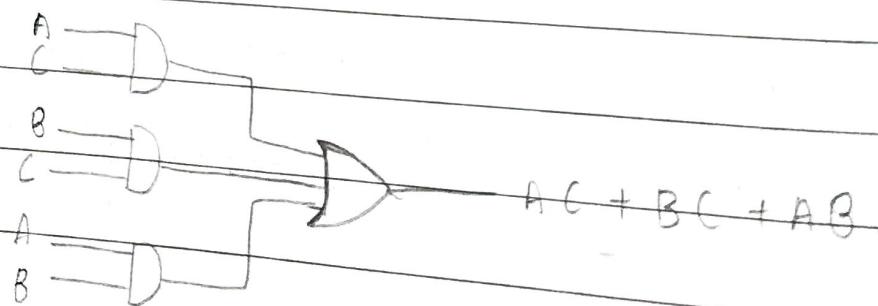
$$Y(A, B, C) = \sum m(3, 5, 6, 7) - \text{SOP}$$

$$Y = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$Y = m_3 + m_5 + m_6 + m_7 - \text{std SOP form.}$$

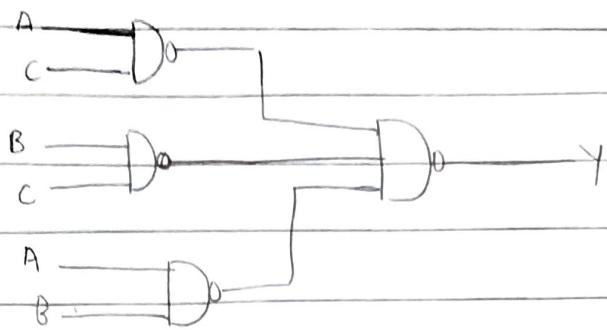
$$\begin{aligned}
 Y &= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC \\
 &= (\bar{A} + A)BC + A\bar{B}C + AB\bar{C} \\
 &= BC + A\bar{B}C + AB\bar{C} \\
 &= \bar{A}BC + A\bar{B}C + AB(\bar{C} + C) \\
 &= \bar{A}BC + A\bar{B}C + AB. \\
 &= \bar{A}BC + A(B + \bar{B}C) \\
 &= \bar{A}BC + A(B + C) \\
 &= \bar{A}BC + AB + AC. \\
 &= C(A + \bar{A}B) + AB \\
 &= C(A + B) + AB \\
 &= AC + BC + AB
 \end{aligned}$$

logic ckt:



$$Y = [AC + BC + AB]$$

$$Y = \overline{AC} \cdot \overline{BC} \cdot \overline{AB}$$



$$f(A, B, C) = \sum m(0, 1, 4, 5, 7)$$

$$= m_0 + m_1 + m_4 + m_5 + m_7$$

$$= \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}C + ABC$$

$$= \overline{A}\overline{B}(\overline{C} + C) + A\overline{B}(\overline{C} + C) + ABC$$

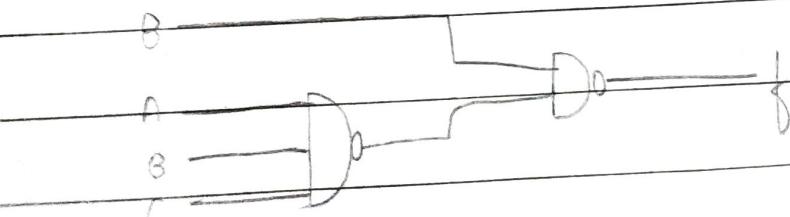
$$= \overline{A}\overline{B} + A\overline{B} + ABC$$

$$= \overline{B}(\overline{A} + A) + ABC$$

$$= \overline{B} + ABC.$$

$$\bar{f} = [\overline{\overline{B} + ABC}]$$

$$: [B \leftarrow \overline{ABC}]$$



$$f(A, B, C, D) = \sum m(0, 1, 4, 5, 12, 13)$$

	A	B	C	D	y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	0

$$Y = m_0 + m_1 + m_4 + m_5 + m_{12} + m_{13}.$$

$$= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \cancel{\bar{A}B\bar{C}\bar{D}} + \cancel{\bar{A}B\bar{C}D} + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} +$$

$$= \bar{A}\bar{B}\bar{C}(\bar{D}+D) + \bar{A}B\bar{C}(\bar{D}+D) + AB\bar{C}(\bar{D}+D)$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C}$$

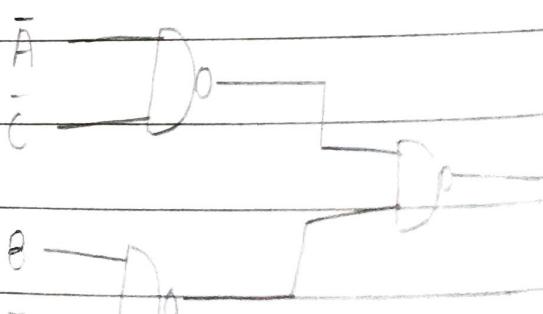
$$= \bar{A}\bar{B}\bar{C} + B\bar{C}(A+\bar{A})$$

$$= \bar{A}\bar{B}\bar{C} + B\bar{C}$$

$$= \bar{C}(B+\bar{A}\bar{B})$$

$$= \bar{C}(B+\bar{A})$$

$$= B\bar{C} + \bar{A}\bar{C}$$



# K Map Simplification for SOP expression.

K Map Karnaugh Map

3 variable

1 " "

$$2^3 : 8$$

$$2^4 : 16$$

$$4 \times 2, 2 \times 4$$

$$4 \times 4$$

3 variable.

AB \ C	0	1
00	$m_0$	$m_1$
01	$m_2$	$m_3$
11	$m_6$	$m_7$
10	$m_4$	$m_5$

AB \ C	00	01	11	10
00	$m_0$	$m_1$	$m_3$	$m_2$
01	$m_4$	$m_5$	$m_7$	$m_6$

Simplify the given boolean fun. using K-Map method and realise the ctrl by using NAND gates only :

$$f(A, B, C) = \sum m(0, 1, 5, 6, 7)$$

A \ BC	00	01	11	10
0	1	1	0	0
1	0	1	1	1

$$f = \bar{A}\bar{B} + AC + AB$$

$$= m_0 + m_1 + m_5 + m_6 + m_7$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}C + ABC + A\bar{B}\bar{C}$$

$$= \bar{A}\bar{B}(\bar{C} + \bar{C}) + A\bar{B}C + AB(C + \bar{C})$$

$$= \bar{A}\bar{B} + A\bar{B}C + AB$$

$$= \bar{A}\bar{B} + A(\bar{B} + \bar{B}C) = \bar{A}\bar{B} + AB + AC$$

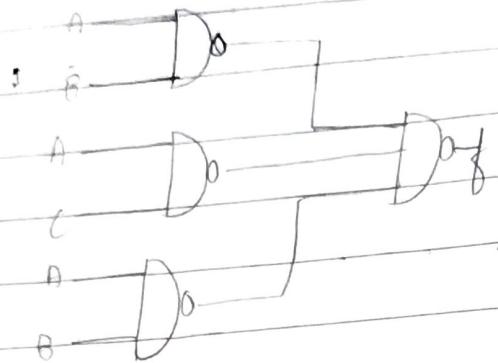
NAND "realisat"

f

$$\bar{A}\bar{B} + \bar{A}C + AB$$

f

$$\bar{A}\bar{B} \cdot \bar{A}C + \bar{A}B$$



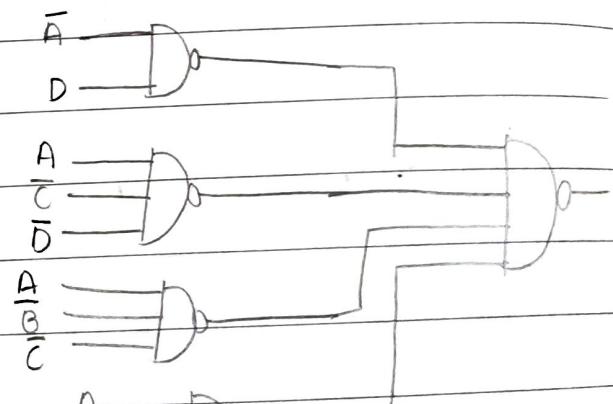
Simplify the given boolean and realise by using  
NAND gates only.

$$2 \quad f(A, B, C, D) = \sum m(1, 3, 5, 7, 8, 9, 10, 12)$$

$$= m_1 + m_3 + m_5 + m_7 + m_8 + m_9 + m_{10} + m_{12}$$

= A

AB \ CD	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	0
10	1	1	0	1



$$f = \bar{A}D + \bar{A}\bar{C}\bar{D} + A\bar{B}\bar{C} + A\bar{B}\bar{D}$$

$$f = \bar{A}D + \bar{A}\bar{C}\bar{D} + A\bar{B}\bar{C} + A\bar{B}\bar{D}$$

$$\bar{A}D \cdot \bar{A}\bar{C}\bar{D} \cdot A\bar{B}\bar{C} \cdot A\bar{B}\bar{D}$$

3  $f(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 6, 8, 12) + d(3, 7)$

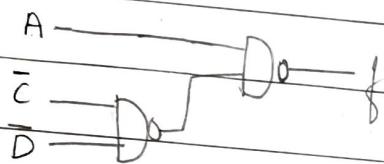
$\begin{matrix} d \\ x \\ \emptyset \end{matrix}$  } don't care inputs.

$x = 0 \text{ or } 1$

$A \backslash B$	CD	00	01	10	11
00	1	1	x	1	1
01	1	1	x	1	1
11	1	0	0	0	0
10	1	0	0	0	0

$$\bar{A} + \bar{C}\bar{D}$$

$$\bar{f} = \overline{\bar{A} + \bar{C}\bar{D}}$$



$$= A + \overline{\bar{C}\bar{D}}$$

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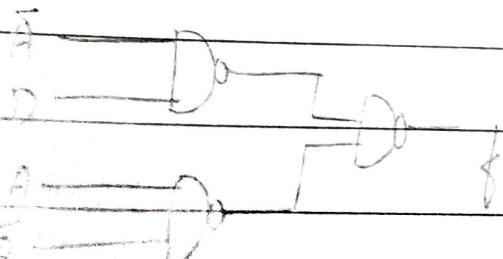
4  $f(A, B, C, D) = \sum m(1, 3, 5, 7, 8, 9, 10) + d(6)$

$A \backslash B$	CD	00	01	11	10
00	0	1	1	0	
01	0	1	1	x	
11	0	0	0	0	
10	1	1	x	1	

$$f = \bar{A}D + A\bar{B}$$

$$\bar{f} = \overline{\bar{A}D + A\bar{B}}$$

$$f = \overline{\bar{A}D} \cdot \overline{A\bar{B}}$$



5 For a given K-Map find out boolean expression in SOP canonical form

	$\bar{C}\bar{B}$	00	01	11	10
$\bar{A}B$	00	1	0	1	1
A $\bar{B}$	01	1	0	0	X
A $B$	11	1	0	1	1
$AB$	10	X	0	0	1

$$f = \bar{D} + \bar{A}\bar{B}C + ABC.$$

POS - Product of sums.

Sum term -

Max term - M - It is fundamental sum term which output is 0 for given i/p's & contain all variables in sum term.

NOR gates are used for realisation of POS exp

	A	B	C	Y	
0	0	0	0	1	
0	0	0	1	1	
0	1	0	0	0	- M <sub>2</sub>
0	1	1	1	0	- M <sub>3</sub>
1	0	0	0	1	
1	0	1	0	0	- M <sub>5</sub>
1	1	0	0	0	- M <sub>6</sub>
1	1	1	1	0	- M <sub>7</sub>

$$\bar{A} + \bar{B} + C$$

$$\bar{A} + \bar{B} + \bar{C}$$

$$\bar{A} + \bar{B} + \bar{C}$$

$$Y(A, B, C) = \pi M(2, 3, 5, 6, 7)$$

$\therefore M_2, M_3, M_5, M_6, M_7$  - std POS exp.

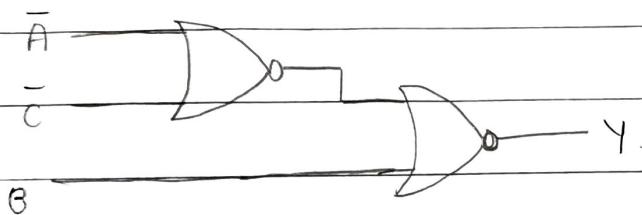
$$\begin{aligned} & \cdot (A + \bar{B} + C) \cdot (A + \bar{B}\bar{C}) \cdot (\bar{A} + B + C) \cdot (\bar{A} + \bar{B} + C) \\ & \cdot (\bar{A} + \bar{B} + \bar{C}) \end{aligned}$$

A	BC		00	01	11	10
	0	1				
0	1	1	0	0		
1	1	0	0	0		

$$Y = (\bar{B}) \cdot (\bar{A} + \bar{C}) \quad - \text{Simplified } \cancel{\text{POS}}$$

$$\overline{\overline{Y}} = (\overline{\bar{B}}) \cdot (\overline{\bar{A} + \bar{C}})$$

$$= \overline{\overline{\bar{B}}} + \overline{\overline{\bar{A} + \bar{C}}} = B + (\bar{A} + \bar{C})$$



$$(A, B, C, D) = \sum m(0, 1, 2, 4, 5, 8, 9, 10, 12, 15)$$

$$= \pi M(3, 6, 7, 11, 13, 14)$$

D	CD		00	01	11	10
	00	01				
00	1	1	0	1		
01	1	1	0	0		
11	1	0	0	1	0	
10	1	1	0	1		

$$f = \overline{\overline{B}} \cdot (\bar{A} + \bar{B} + C + \bar{D}) \cdot (B + \bar{C} + \bar{D})$$

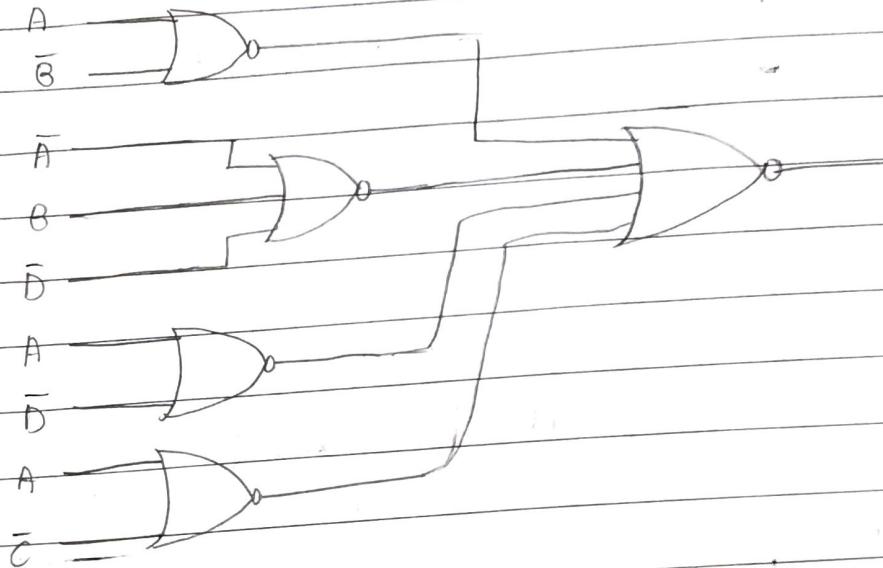
$$(A + \bar{C} + \bar{D}) \cdot (\bar{B} + \bar{C} + D)$$

3 For given K-Map write boolean fun. in POS  
Simplify it & realise the eqn and realise the eqn  
using NOR gates only.

$A \setminus B$	CD	00	01	11	10
00	1	0	0	0	
01	0	0	0	X	
11	X	1	0	1	0
10	1	0	0	1	

$$Y = \pi M(1, 2, 3, 4, 5, 7) + d(6, 12)$$

$$Y = (A + \bar{B}) \cdot (\bar{A} + B + \bar{D}) \cdot (A + \bar{D}) \cdot (A + \bar{C})$$



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Quine McClusky Method for Simplification. (Ta)

$$f(A, B, C, D) = \sum m(0, 1, 4, 5, 12, 13, 15)$$

A	B	C	D	min term	
0	0	0	0	0 ✓	- 0 1's
0	0	0	1	1 ✓	
0	1	0	0	4 ✓	1 1's

A	B	C	D	min term	
0	1	0	1	5 ✓	2 1's
1	1	0	0	12 ✓	
1	1	0	1	13 ✓	3 1's
1	1	1	1	15	4 1's

1<sup>st</sup> level of grouping.

0.1 (1)<sup>2</sup> difference of (0, 1)

0.4 (4) ✓ " " (0, 4)

1 5 (4) ✓ "

4 5 (1) —

4 12 (8) ✓

5 13 (8) ✓

12 13 (1) ✓

13. 15 (2) — R:

2<sup>nd</sup> level of grouping  
(compon. of difference)

0.1. 4. 5 (1. 4)

4. 5. 12. 13 (13. 8) —

P, Q, R are prime implicant

A	B	C	D
8	4	2	1

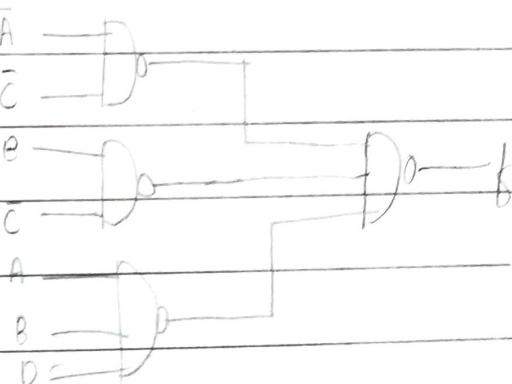
0	0	0	0
1	0	0	1
4	0	1	0
5	0	1	1

A	B	C	D
R	1	1	0
15	1	1	1
R = ABD			

$$f = P + Q + R = \bar{A}\bar{C} + B\bar{C} +$$

$$P = \bar{A}\bar{C}$$

4	0	1	0	0
5	0	1	0	1
12	1	1	0	0
13	1	1	0	1



$$Q = B\bar{C}$$

The prime implicant in a Quine-McCluskey method is a product term for which output is 1

The group of 2 minterm  
 The group of 4 minterm  
 eliminates  
 " " 1 variable  
 " " 2  
 " " 3 "

$$f(A, B, C, D) = \sum m(1, 3, 5, 7, 9, 11, 12, 13, 15)$$

$\begin{matrix} A \\ B \\ C \\ D \end{matrix}$	minterm	1 <sup>st</sup> grouping
0 0 0 1	1 ✓	{1, 3} (2) ✓
0 0 1 1	3 ✓	1, 5 (4) ✓
0 1 0 1	5 ✓	1, 9 (8) ✓
1 0 0 1	9 ✓	3, 7 (4) ✓
1 1 0 0	12 ✓	3, 11 (8) ✓
0 1 1 1	7 ✓	5, 7 (2) ✓
1 0 1 1	11 ✓	5, 13 (8) ✓
1 1 0 1	13 ✓	9, 11 (2) ✓
1 1 1 1	15 ✓	9, 13 (4) ✓
		12, 13 (1) — Q

2<sup>nd</sup> level of grouping.

$$1, 3, 5, 7 (2, 4) ✓$$

$$7, 15 (8) ✓$$

$$1, 3, 9, 11 (2, 8) ✓$$

$$11, 15 (4) ✓$$

$$\underline{1, 5, 9, 13 (4, 8)} ✓$$

3<sup>rd</sup> level of grouping

$$\underline{\underline{3, 7, 11, 15 (4, 8)}} ✓$$

$$5, 7, 13, 15 (2, 8) ✓$$

$$1, 3, 5, 7, 9, 11, 13, 15 (2)$$

$$9, 11, 13, 15 (2, 4) ✓$$

↓ P

P and Q are PI

$$P = D$$

$$Q = ABC\bar{C}$$

$$f = P + Q$$

$$= D + ABC\bar{C}$$

3 Simplify the given boolean fun<sup>n</sup>, using AM method  
 list the prime implicants and find necessary prime  
 implicants and find simplified SOP exp. and realise the  
 same using NAND gates.

$f(A \oplus CD) = \sum m(1, 2, 3, 5, 7, 10, 11) + d(6, 9)$	
A    B    C    D    m	1 <sup>st</sup> level of grouping
0    0    0    1    1 ✓	1, 3 (2)
0    0    1    0    2 ✓	1, 5 (4)
0    0    1    1    3 ✓	1, 9 (8)
0    1    0    1    5 ✓	2, 3 (1)
0    1    1    0    6 ✓	2, 6 (4)
1    0    0    1    9 ✓	2, 10 (8)
1    0    1    0    10 ✓	3, 7 (4)
0    1    1    1    7 ✓	3, 8 (11)
1    0    1    1    11 ✓	5, 7 (2)
	6, 7 (1)
	9, 11 (2)

2<sup>nd</sup> level

1    3    5    7    (2, 4)	- P	10, 11 (1)
1    3    9    11    (2, 8)	- Q	
8    0    0    0    (08,		
2    3    6    7    (1, 4)	- R	P - $\bar{A}D$ , Q - $\bar{B}P$
8    3    0    0    (00		R - $\bar{A}C$ S = $\bar{B}C$ .
2    3    10    11    (1, 8)	- S.	

P Q R S are prime implicants.

1	2	3	5	7	9	10	11
X	X	(X) X					
X	X				X		
X	X	X					

P and S are essential

$$f = P + S$$

$$\bar{A}D + \bar{B}C$$

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	A	B	C	D	m
AB	00	01	10	11	10
CD	00	01	10	11	0
	00	01	10	11	1
	10	11	00	01	5

$$f(A, B, C, D) = \sum m(0, 5, 7, 8, 9, 10) + d(1, 13, 11)$$

	A	B	C	D	min term		2 <sup>nd</sup> level
0	0	0	0	0	0 ✓		
10	0	0	0	1	1 1	P - 0	1 8 9
10	0	0	1	0	1 8	Q - 1	5 9 13
0	1	0	0	1	5 ✓	R - 8	9 10 11
1	0	0	0	1	9 ✓	8 - 10	5 7 11
1	0	1	0	0	10 ✓		
0	1	1	1	1	7 ✓		
1	0	1	1	1	11 ✓		
1	1	0	1	1	13 ✓	0 5 7 8 9	10

### 1<sup>st</sup> level

$$0 1 (1) ✓$$

$$P \text{ (X)}$$

$$0 8 (8) ✓$$

$$Q \text{ (X)}$$

$$\cancel{0} \cancel{8} (8e)$$

$$S \text{ (X)}$$

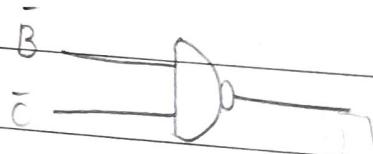
$$1 9$$

$$1 5 (4) ✓$$

$$f = P + Q + S \\ = \bar{B}\bar{C} + A\bar{B} + \bar{A}BC.$$

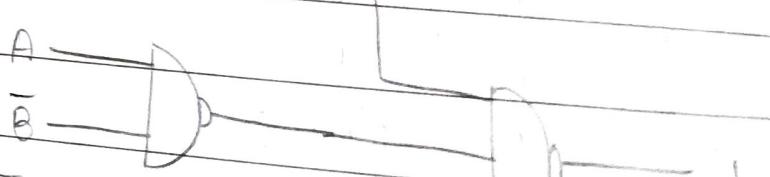
$$1 9 (8) - ✓$$

$$8 9 (1) ✓$$



$$8 10 (2) ✓$$

$$5 7 (2) - S$$



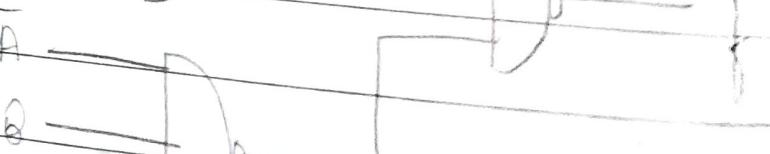
$$5 13 (8) ✓$$



$$9 11 (2) ✓$$



$$9 13 (4) ✓$$



$$10 11 (1) ✓$$

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classmate

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Page \_\_\_\_\_

$$f(A, B, C, D) = \pi M(0, 2, 4, 6, 8, 9, 10, 14, 15) \\ \sum m(1, 3, 5, 7, 11, 12, 13)$$

A	B	C	D	minterms.	1 <sup>st</sup> level of grouping
0	0	0	1	1 ✓	
0	0	1	1	3 ✓	1, 3' (2) ✓
0	1	0	1	5 ✓	1, 5 (4) ✓
1	1	0	0	12 ✓	3, 7 (4) ✓
0	1	1	1	7 ✓	8, 11 (8) — a
1	0	1	1	11 ✓	5, 7 (2) ✓
1	1	0	1	13 ✓	5, 13 (8) — a
					12, 13 (1) — s

2<sup>nd</sup> level of grouping

$$1, 3, 5, 7 (2, 4) - P$$

P Q R S are PI

$$P - \bar{A}D$$

$$Q - \bar{B}CD$$

$$R - B\bar{C}D$$

$$S - A\bar{B}\bar{C}$$

$$f = \bar{A}D + \bar{B}CD + B\bar{C}D + A\bar{B}\bar{C}$$

1 3 5 7 11 12 13

P (x) x x (x)

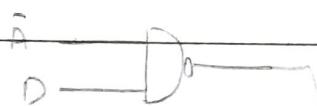
Q x (x)

R x (x)

S (x) x

$$f = P + Q + S$$

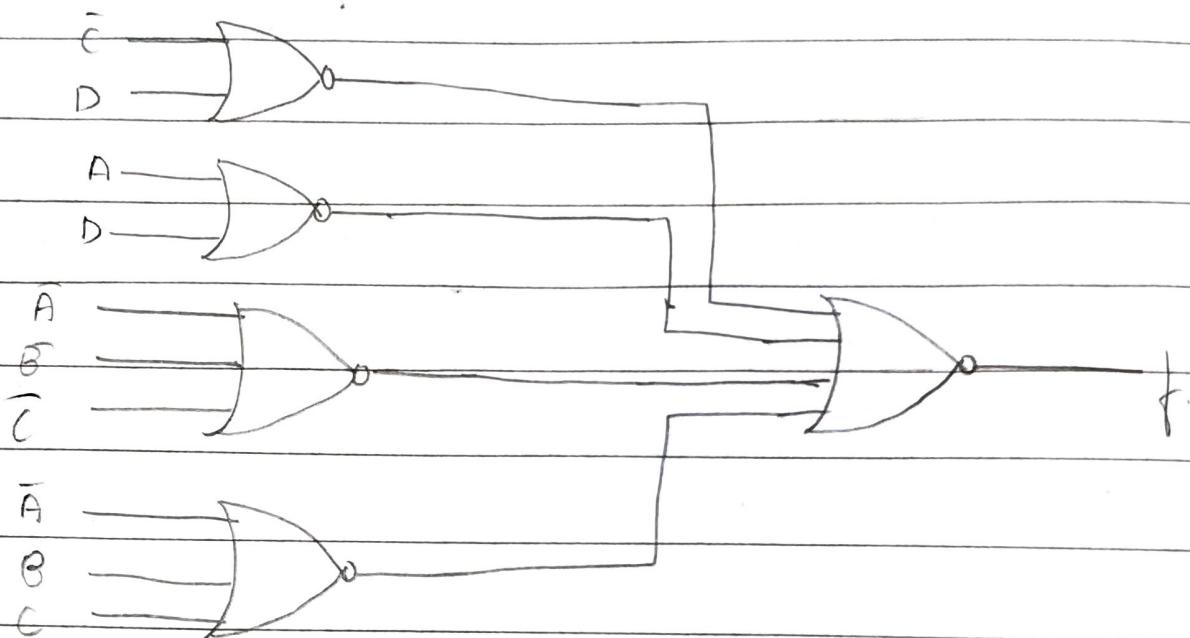
$$= \bar{A}D + \bar{B}CD + A\bar{B}\bar{C}$$



$A \bar{B}$	$C \bar{D}$	00	01	11	10
00	0	0	1	0	0
01	0	1	1	0	0
11	1	1	0	0	0
10	0	0	1	0	0

$$f = AB\bar{C} + \bar{B}CD + \bar{A}D$$

$$\text{POS} \rightarrow (\bar{C} + D) \cdot (A + D) \cdot (\bar{A} + \bar{B} + \bar{C}) \cdot (\bar{A} + B + C)$$



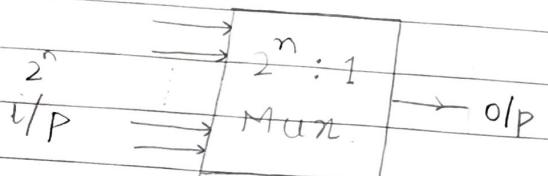
## UNIT - 2

### DATA PROCESSING CIRCUITS.

Multiplexers :  $2^n$  inputs & 1 output.

and each input have particular time slot.

- It is a combinational logic ckt having  $2^n$  or less inputs and 1 output.
- Each input is connected to output by time sharing principle.
- The select inputs are used to connect input to output.



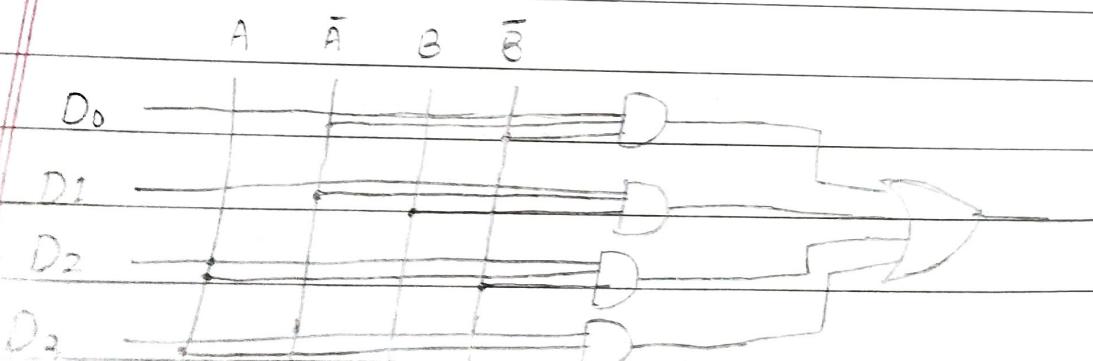
$4 : 1$  Multiplexer

$2^2 = 4$ , 2 select i/p's

		Truth		$0/P$
		A	B	
$\rightarrow D_0$		0	0	$D_0$
$\rightarrow D_1$	$4:1$	0	1	$D_1$
$\rightarrow D_2$	Mux	1	0	$D_2$
$\rightarrow D_3$		1	1	$D_3$

$$Y = \bar{A}\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + AB\bar{D}_3$$

Logic diagram for  $4 : 1$  multiplexer.



26/8/19

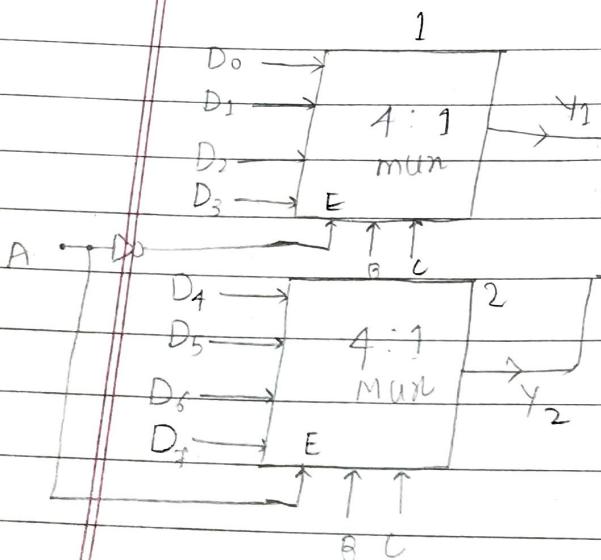
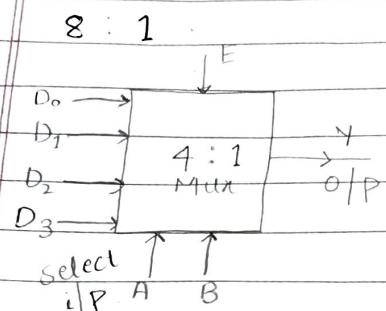
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Construct 8:1 multiplexer using 4:1 multiplexers.

Enable input :

- active high - 1
- active low - 0

$E$  if the logic is AND active high  
for NAND Ckt it is active low.



Select i/p	A	B	C	O/p
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	0	0
1	1	1	1	1

$$Y = Y_1 + Y_2$$

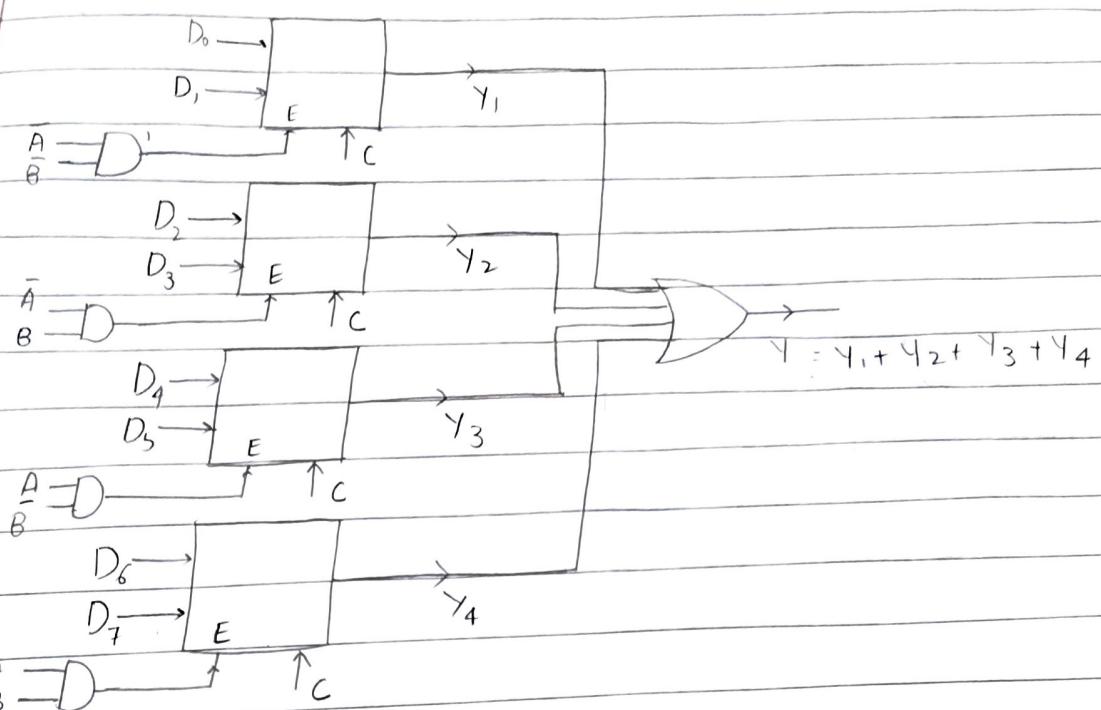
$$\begin{aligned} &= \bar{A}\bar{B}\bar{C}D_0 + \bar{A}\bar{B}CD_1 + \bar{A}B\bar{C}D_2 + \bar{A}BCD_3 + A\bar{B}\bar{C} \\ &\quad + A\bar{B}CD_5 + A{B}\bar{C}D_6 + ABCD_7. \end{aligned}$$

Boolean expression for 8:1 mux in SOP

multiplexer

ID  
high it is

Construct 8:1 multiplexer using 2:1 multiplexer by using 2:1 multiplexer with enable input.



Select i/p      O/p.

A    B    C

0    0    0

0    0    1

Mux 1 is selected

0    1    0

0    1    1

Mux 2

1    0    0

1    0    1

Mux 3

1    1    0

1    1    1

Mux 4

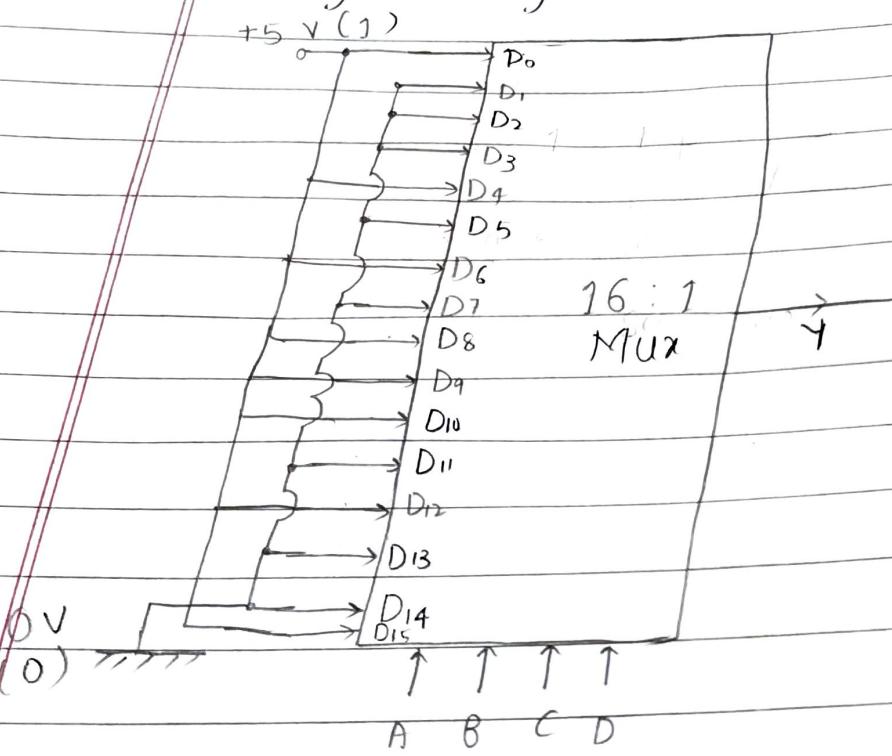
Construct 16:1 Mux using 4:1 Multiplexer with enable input.

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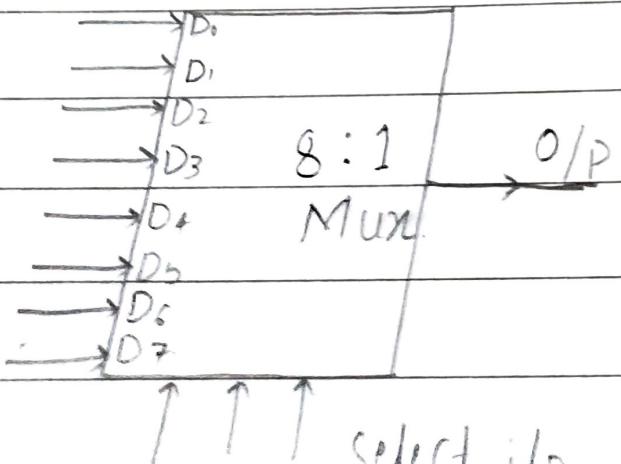
Implement boolean function in SOP form using suitable Multiplexer.

1.  $f(A, B, C, D) = \sum m(0, 4, 6, 8, 9, 10, 12, 15)$

1. Use 16 : 1 multiplexer logic diagram



2. Method 2 : Use 8 : 1 mux



$$f(A, B, C, D) = \sum(0, 4, 6, 8, 9, 11, 14, 15)$$

$\wedge$  as MIV - map en laud variable

Implementation table : A as MEV

I/P	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
$\bar{A}$	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
1	A	0	A	$\bar{A}$	0	1	A	

I/P	A	B	C	D
0	0	0	0	0
0001	0	0	1	0

0000	0	0	1	1
0001	0	0	1	1

0010	0	0	1	1
0011	0	0	1	1

0100	0	1	0	0
0101	0	1	0	1

0110	0	1	1	0
0111	0	1	1	1

1000	1	0	0	0
1001	1	0	0	1

1010	1	0	1	0
1011	1	0	1	1

1100	1	1	0	0
1101	1	1	0	1

1110	1	1	1	0
1111	1	1	1	1

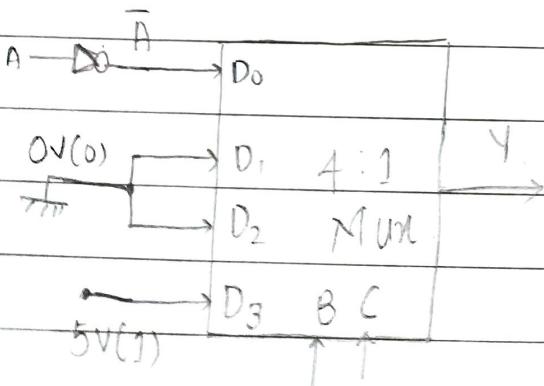
$$f(A, B, C) = \sum m(0, 3, 7)$$

$$A = 1$$

Implementation  $A$  as MEV.

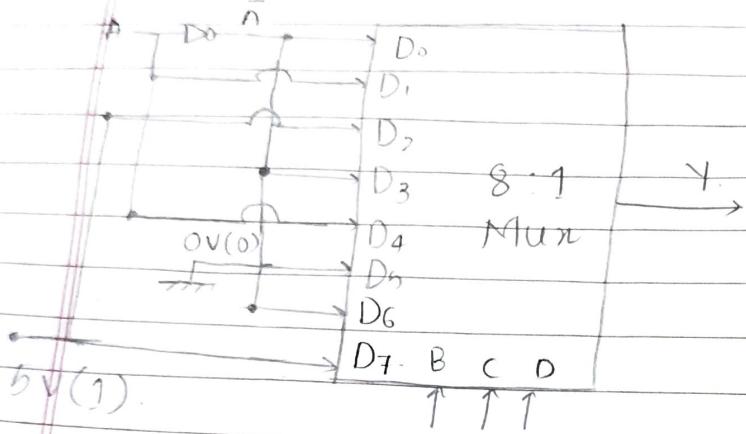
	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
$\bar{A}$	0	1	2	3
A	4	5	6	7

$$A \quad 0 \quad 0 \quad 1$$



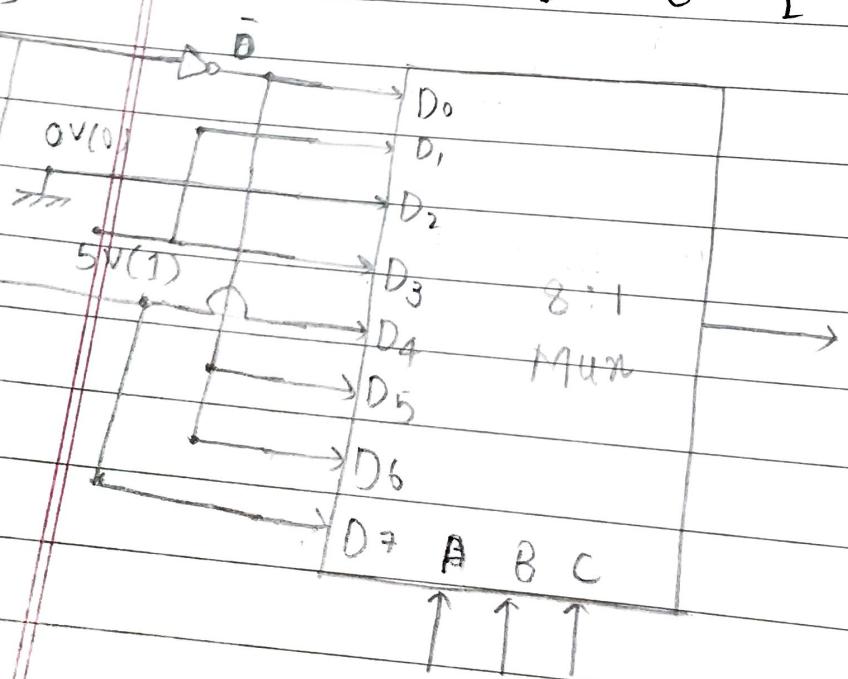
Implementation table A as MEV

J/P	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
A	(0)	1	(2)	(3)	4	5	(6)	(7)
A	8	(9)	(10)	(11)	(12)	(13)	(14)	(15)
A	A	1	A	A	0	A	A	1



D as MEV

J/P	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>
D	(0)	(2)	4	(6)	8	(10)	(12)	14
D	1	(3)	5	(7)	(9)	11	13	(15)
D	D	1	0	1	D	D	D	D

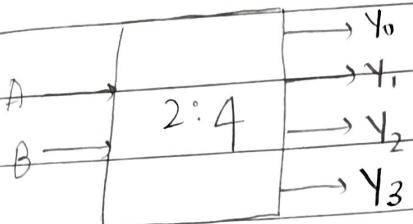


19  
 Decoder: It is a combination logic ckt having n input and  $2^n$  output at any time the selected one is active.

Out of  $2^n$  outputs, 1 o/p is active and that depends on inputs.

- Decoders finds application in memory ckt's to select 1 register out of many for read write operation.  
 The decoder is implemented by AND ckt or NAND ckt.  
 Basically decoder generates min terms which is used to implement boolean func.

### 2:4 decoder



active high (1) - AND  
 active low - NAND

### Truth table

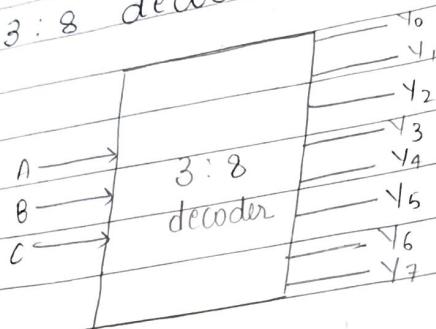
i/p		o/p				E	+5V	$\bar{A}$	$\bar{B}$	D	$Y_0 = \bar{A}\bar{B}$
A	B	$Y_0$	$Y_1$	$Y_2$	$Y_3$						
0	0	1	0	0	0						
0	1	0	1	0	0						
1	0	0	0	1	0						
1	1	0	0	0	1						

Enable input : E - active high - for AND

2

	$A$	$B$	$C$	$Y_0$	$Y_1$	$Y_2$	$Y_3$
0	0	x	x	0	0	0	0
1	0	0	0	1	0	0	0
1	0	1	0	0	1	0	0
1	1	0	0	0	0	1	0
1	1	1	1	0	0	0	1

3:8 decoder



$$\bar{A} \quad \bar{B} \quad \bar{C} \rightarrow Y_0 = \bar{A}\bar{B}\bar{C}$$

$$\bar{A} \quad B \quad C \rightarrow Y_1 = \bar{A}\bar{B}C$$

$$\bar{A} \quad B \quad \bar{C} \rightarrow Y_2 = \bar{A}BC$$

$$\bar{A} \quad B \quad C \rightarrow Y_3 = \bar{ABC}$$

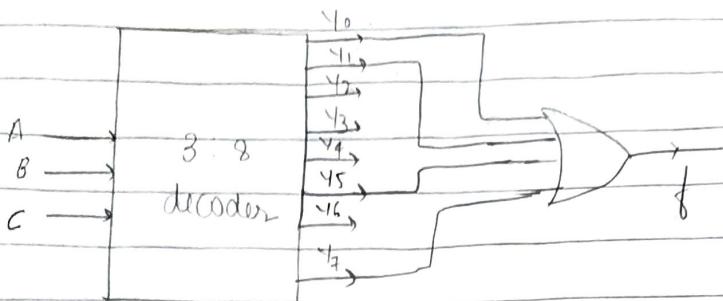
$$A \quad B \quad C \rightarrow Y_7 = ABC$$

Implementation of Boolean funct<sup>n</sup> using de Codex.

$$f(A, B, C) = \Sigma(0, 1, 5, 7)$$

$$= m_0 + m_1 + m_5 + m_7$$

$$= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC \rightarrow SOP$$



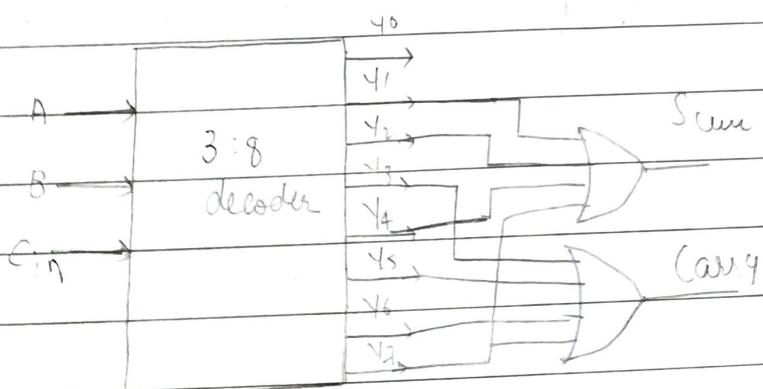
Implement full adder circuit by using decoder

Full Ladder :

	A →	Full Adder	Sum	Truth table
	B →			A B Cin S Co.
	Cin →		Carryout	0 0 0 0 0
Carryin				0 0 1 1 0
A - 1 0 1 1				0 1 0 1 0
B 1 0 1 0				0 1 1 0 1
Carryout ← 1 0 1 0 1 ← Sum				1 0 0 1 0
Carryout				1 0 1 0 1

$$S(A, B, Cin) = \sum m(1, 2, 4, 7)$$

$$C_0(A, B, Cin) = \sum m(3, 5, 6, 7)$$



$$Sum = m_1 + m_2 + m_4 + m_7$$

$$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$\therefore \bar{A}(B \oplus C) + A(\bar{B} \oplus C) = A \oplus (\bar{B} \oplus C) = A \oplus B \oplus C.$$

2

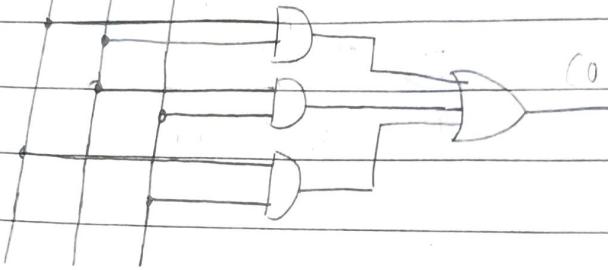
$$C_0 = m_3 + m_5 + m_6 + m_7 \\ \bar{A}BC + A\bar{B}C + ABC\bar{C} + ABC$$

$$C(\bar{A}B + A\bar{B}) + \bar{B}BC \\ C(A \oplus B) + AB$$

- $\bar{A}BC + A\bar{B}C + ABC\bar{C} + ABC$
- $\bar{A}BC + A\bar{B}C + A\bar{B}(C + C)$
- $\bar{A}BC + A\bar{B}C + AB$
- $\bar{A}BC + A(\bar{B}C + B)$
- $\bar{A}BC + A(B + C)$
- $\bar{A}BC + AB + AC$
- $BC(\bar{A} + AB) + AC$
- $\bar{A}BC + BC + AC$

A    B    Cin

0    0    0



1/19 Implementation of full subtractor using decoder

D    B

1    1    1

$$0 - 0 = 0 \quad 0$$

$$0 - 1 = 1 \quad 1$$

$$1 - 0 = 1 \quad 0$$

$$1 - 1 = 0 \quad 0$$

$$A - 1010$$

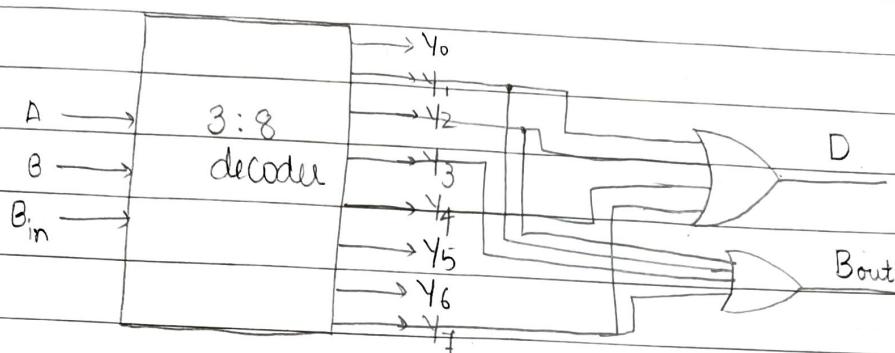
$$B \quad \underline{0111}$$

$$D \quad 011$$

Truth table

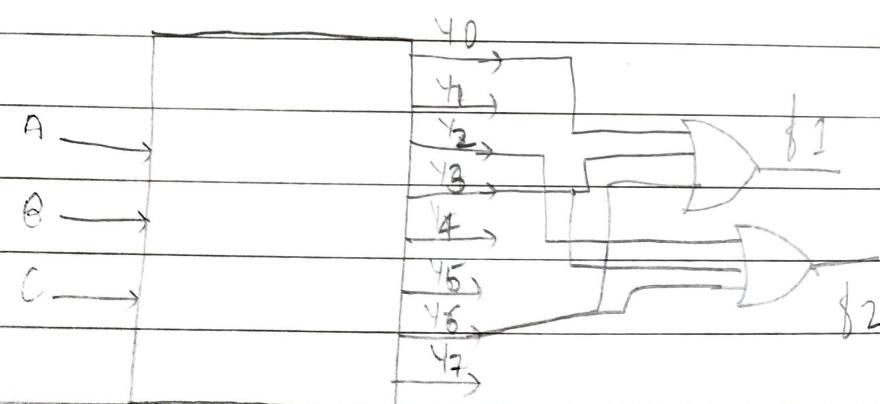
A	B	Bin	D	B <sub>0</sub>
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D(A, B, B_{in}) = \Sigma m(1, 2, 4, 7)$$

Implement following boolean funct<sup>n</sup> using decoder

$$\begin{aligned} f_1(A, B, C) &= \Sigma(0, 3, 6) \\ &= m_0 + m_3 + m_6 \\ &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + AB\bar{C} \end{aligned}$$

$$\begin{aligned} f_2(A, B, C) &= \Pi(0, 1, 4, 5) \\ f_2(A, B, C) &= \Sigma(2, 3, 6) \\ &= m_2 + m_3 + m_6 \\ &= \bar{A}B\bar{C} + \bar{A}BC + ABC \end{aligned}$$



Binary coded Decimal  
Design BCD to decimal decoder and implement  
ctrl with min. no. of gates

9/9/19

I/P  $\rightarrow$  BCD 0 to 9 digits  
4 i/p variable  
O/P  $\rightarrow$  decimal (10 o/p's)

T/I/P	O/P												
A	B	C	D	$y_0$	$y_1$	$y_2$	$y_3$	$y_4$	$y_5$	$y_6$	$y_7$	$y_8$	$y_9$
0	0	0	0	1	0	—	—	—	—	—	—	—	0
0	0	0	1	0	1	0	—	—	—	—	—	—	0
0	0	1	0	0	0	1	0	—	—	—	—	—	0
0	0	1	1	0	0	0	1	0	—	—	—	—	0
0	1	0	0	0	0	0	0	1	0	—	—	—	0
0	1	0	1	0	0	0	0	0	1	0	—	—	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	—	—	—	—	—	—	—	0	1

The i/p combination 10 to 15 are used as don't care

$$y_0(A, B, C, D) = \sum m(0) + d(10 \text{ to } 15)$$

$$y_1(A, B, C, D) = \sum m(1) + d(10 \text{ to } 15)$$

		AB \ CD			
		00	01	11	10
Y <sub>0</sub>	00	1	0	0	0
	01	0	0	0	0
	11	X	X	X	X
	10	0	0	X	X

$$Y_0 = \bar{A}\bar{B}\bar{C}\bar{D}$$

19/19

## Magnitude Comparator :

It is a combinational logic ckt for which there are 2 <sup>binary</sup> inputs A & B. It compares magnitude/value of A and B and produce 1 result out of 3 outputs. The input A is compared with B and based on value of A the result is decided

Mag.	$A < B = L$
Comparison	$A = B = E$
ckt	$A > B = G$

$$A \rightarrow 1101 - 13$$

$$B \quad 1011 - 11$$

$$A > B \rightarrow G = 1$$

Design 1 bit magnitude comparator and implement using logic gates.

Truth table

I/P

O/P

A	B	G	E	L
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

$$G = A\bar{B}$$

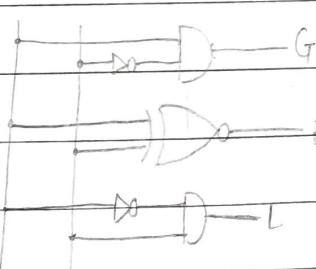
$$E = \bar{A}\bar{B} + AB = A \oplus B = (A \oplus B)$$

$$L = \bar{A}B$$

XNO

D0

A    B



2  
2 bit 2 bit magnitude comparator

	$A_1$	$A_0$	$B_1$	$B_0$	G	E	L	D/P
$A = 0$	0	0	0	0	0	1	0	
	0	0	0	1	0	0	1	
	0	0	1	0	0	0	1	
	0	0	1	1	0	0	1	
	0	1	0	0	1	0	0	
	0	1	0	1	0	1	0	
	0	1	1	0	0	0	1	
	0	1	1	1	0	0	1	
	1	0	0	0	1	0	0	
	1	0	0	1	1	0	0	
$A = 1$	1	0	1	0	0	1	0	
	1	1	1	0	0	0	1	
	1	1	1	1	0	0	1	
	1	0	0	0	1	0	0	
	1	0	0	1	1	0	0	
$A = 2$	1	0	1	0	0	1	0	
	1	1	0	0	1	0	0	
	1	1	0	1	1	0	0	
	1	0	1	1	0	0	1	
$A = 3$	1	1	1	0	1	0	0	
	1	1	1	1	1	0	0	
	1	0	1	0	1	0	0	
	1	0	1	1	0	1	0	

$$E(A, A_1, A_0, B_1, B_0) = \Sigma(0, 5, 10, 15)$$

$$G(A, A_1, A_0, B_1, B_0) = \Sigma(4, 8, 9, 12, 13, 14)$$

$$L(A_1, A_0, B_1, B_0) = \Sigma(1, 2, 3, 6, 7, 11)$$

$$\begin{aligned}
 E &= \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0 + A_1 A_0 B_1 B_0 \\
 &= \bar{A}_1 \bar{B}_1 (\bar{A}_0 B \bar{B}_0) + \\
 &= \bar{A}_1 \bar{B}_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0) + A_1 B_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0) \\
 &= \bar{A}_1 \bar{B}_1 (A_0 \oplus B_0) \\
 &= \bar{A}_1 \bar{B}_1 (A_0 \odot B_0) + A_1 B_1 (A_0 \odot B_0) \\
 &= (A_0 \odot B_0) (A_1 \oplus B_1)
 \end{aligned}$$

Truth tabl

$$E_n = E_{n-1} \cdot E_{n-2} \cdot \dots \cdot E_1 \cdot E_0$$

G		B <sub>1</sub> B <sub>0</sub>			
		00	01	11	10
A <sub>1</sub> A <sub>0</sub>	00	0	0	0	0
	01	1	0	0	0
	11	1	1	0	1
	10	1	1	0	0

K-map for G o/p.

$$G(A_1, A_0, B_1, B_0) = \sum m(4, 8, 9, 12, 13, 14)$$

$$G = A_1 \bar{B}_1 + A_0 \bar{B}_1 \bar{B}_0 + A_1 A_0 \bar{B}_0$$

L		B <sub>1</sub> B <sub>0</sub>			
		00	01	11	10
A <sub>1</sub> A <sub>0</sub>	00	0	1	1	1
	01	0	0	1	1
	11	0	0	0	0
	10	0	0	1	0

$$L = \sum m(1, 2, 3, 6, 7, 11)$$

K-map for L o/p.

$$D \text{ for } L = \bar{A}_1 B_1 + \bar{A}_1 \bar{A}_0 B_0 + \bar{A}_0 B_1 B_0$$

Parity Generator and checker ckt

Parity → count 1's in given data  
 To odd parity : 1101, 1100 (5 1's)  
 even parity : 1100, 1100 (4 1's)

Design even parity generator for 3 bit binary no.  
 and draw the logic ckt:

3 bit data + 1 extra bit for parity

I/P			O/p
A	B	C	P <sub>even</sub>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$P_{\text{even}}(A, B, C) = \sum m(1, 2, 4, 7)$$

$$= m_1 + m_2 + m_4 + m_7$$

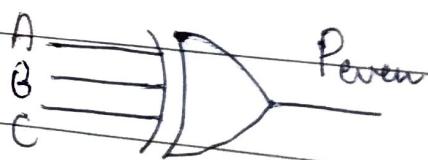
$$\begin{array}{|c|c|c|c|} \hline 0 & 1 & 0 & 1 \\ \hline \end{array} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC.$$

$$\begin{array}{|c|c|c|c|} \hline 1 & 0 & 1 & 0 \\ \hline \end{array} = \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + B\bar{C})$$

$$= \bar{A}(B \oplus C) + A(B \oplus C)$$

$$= A \oplus (B \oplus C)$$

$$= A \oplus B \oplus C$$



Exclusive OR gate (XOR)  $\overset{\text{classmate}}{\Rightarrow} Y = A \oplus B$

Truth table

T/I/P	Y/I/P	
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$$Y = \bar{A}B + A\bar{B}$$

$$= A \oplus B$$

Exclusive NOR Gate (XNOR)  $\overset{\text{classmate}}{\Rightarrow} Y = (\overline{A \oplus B})$

$$Y = \overline{\bar{A}B + A\bar{B}}$$

$$= (\overline{\bar{A}B}) \cdot (\overline{A\bar{B}})$$

$$= (\overline{\bar{A} + \bar{B}}) \cdot (\overline{\bar{A} + B})$$

$$= (A + \bar{B}) \cdot (\bar{A} + B)$$

$$= A\bar{A} + \bar{A}\bar{B} + AB + B\bar{B}$$

$$= \bar{A}\bar{B} + AB$$

$$= A \odot B$$

Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Design 4 bit odd parity generator and draw the logic circuit

A	B	C	D	P <sub>odd</sub>
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0

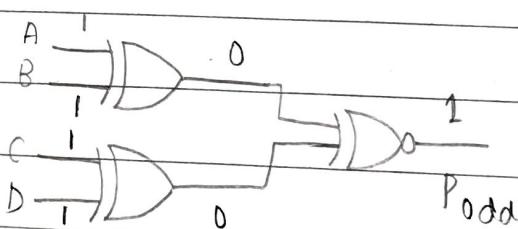
A	B	C	D	P <sub>odd</sub>
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

$P_{\text{odd}}(n, B, C, D) \in m(0, 3, 5, 6, 9, 10, 12, 15)$

AB	CD	00	01	11	10
00		1	0	1	0
01		0	1	0	1
10		1	0	1	0
11		0	1	0	1

If (0's and 1's are alternating)  
 $\downarrow$   
XNOR  
if 1<sup>st</sup> position 1  
XOR - if 1<sup>st</sup> position 0.

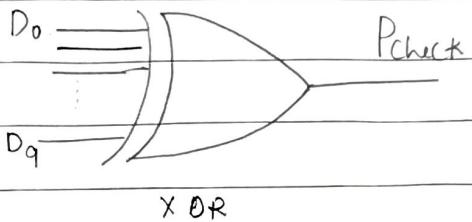
$$\begin{aligned}
P_{\text{odd}} &= m_0 + m_2 + m_5 + m_6 + m_9 + m_{10} + m_{12} + m_{15} \\
&= \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{ABC}\bar{D} + A\bar{B}\bar{C}D + A\bar{B}C \\
&\quad AB\bar{C}\bar{D} + ABCD \\
&= \bar{A}\bar{B}(\bar{C}\bar{D} + CD) + \bar{A}B(\bar{C}D + C\bar{D}) + A\bar{B}(\bar{C}D + C\bar{D}) \\
&\quad + AB(\bar{C}\bar{D} + CD) \\
&= \bar{A}\bar{B}(C\bar{D}) + \bar{A}B(C\oplus D) + A\bar{B}(C\oplus D) + ABC \\
&= (C\bar{D})(\bar{A}\bar{B} + AB) + (\bar{C}\oplus D)(\bar{A}B + A\bar{B}) \\
&= (\bar{C}\bar{D})(A\oplus B) + (C\oplus D)(A\oplus B) \\
&= \bar{x}\bar{y}x\bar{y} \\
&= (C\oplus D)\odot(A\oplus B) \\
&= A\oplus B \odot C\oplus D
\end{aligned}$$



- For even parity generator the parity bit ( $P_{\text{even}}$ ) is exclusive-OR operation of input data bits.
- For odd parity generator the parity bit ( $P_{\text{odd}}$ ) is exclusive-NOR operation of input data bits.

- In K-Map if 0's and 1's are alternate to each other row wise and column wise, it will lead to  $\oplus$  XOR or  $\ominus$  XNOR expression.
- If there is 1 at  $0^{\text{th}}$  input expression is XNOR.
- XNOR or XOR gates are available with multiple inputs.
- Even they can be implemented by using 2 input gates.
- In parity generator or checker ckt only XOR or XNOR gates are required.

### Parity checker



The parity check will check the parity of received data. If the received data is odd parity, the  $P_{\text{check}}$  will be 1 and for even parity  $P_{\text{check}}$  will be 0.

- 1 XOR gate with  $n$  inputs is enough to check the parity of receive data.

Eg : 1011, 1100

$P_{\text{check}} = 1$  indicates odd parity

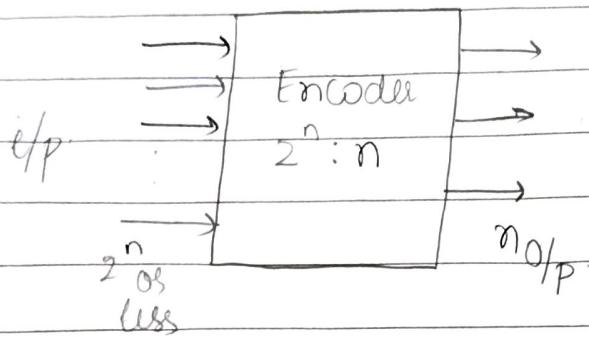
if i/p : 1100, 0011

$P_{\text{check}} = 0$  indicates even parity.



Encoder : Opp. of decoder

- It is a combinational logic ckt having  $2^n$  inputs and  $n$  outputs.
  - For each input there is  $n$ -bit binary output.
  - Basically this is used to convert decimal, hexadecimal, octal digit into binary output.
  - The encoder is a part of input device.



## Octal to binary encoder

I/p (0-7)

O/p - 3 bit

## Truth table

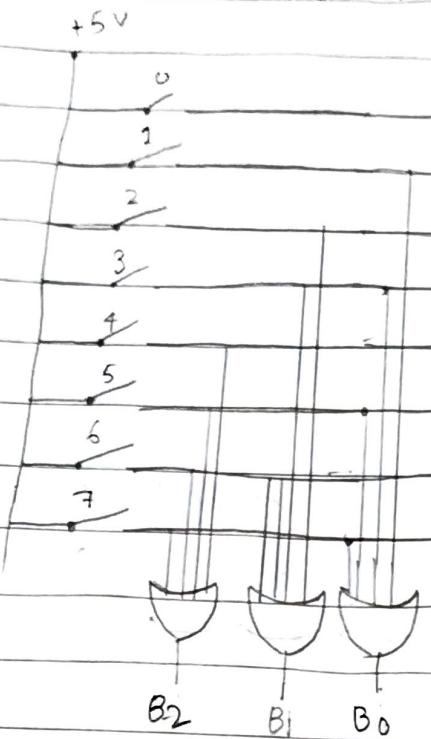
I/P

I/P								O/P.					
D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	B <sub>0</sub>	B <sub>1</sub>	B <sub>2</sub>	B <sub>3</sub>	B <sub>4</sub>	B <sub>5</sub>
1	0						0	0	0	0	0		
0	1	0					0	0	0	1			
0	0	1	0				0	0	1	0			
0	0	0	1				0	0	1	1			
0		0	1				0	1	0	0			
0		0	1	0	0			1	0	1			
0			0	1	0			1	1	0			
0				0	1			1	1	1			

$$B_0 = D_1 + D_3 + D_5 + D_7$$

$$B_1 = D_2 + D_3 + D_6 + D_7$$

$$B_2 = D_4 + D_5 + D_6 + D_7$$



## Decimal Encoder

I/P

O/P

D

B<sub>3</sub> B<sub>2</sub> B<sub>1</sub> B<sub>0</sub>

0

0 0 0 0

1

0 0 0 1

$$B_0 = D_1 + D_3 + D_5$$

2

0 0 1 0

$$B_1 = D_2 + D_3 + D_6 +$$

3

0 0 1 1

$$B_2 = D_4 + D_5 + D_6$$

4

0 1 0 0

$$B_3 = D_8 + D_9$$

5

0 1 0 1

6

0 1 1 0

7

0 1 1 1

8

1 0 0 0

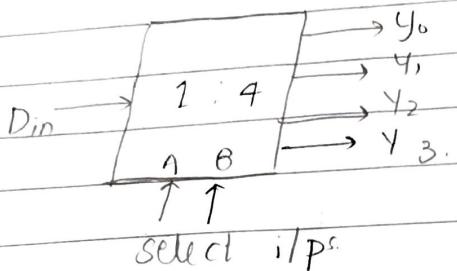
9

1 0 0 1

2

- Demultiplexer: opp of multiplexer.
- It is a combinational logic circuit in which single input has  $2^n$  outputs and  $n$  select i/p.
  - The input is connected to selected o/p lines. The same i/p is connected to any 1 of the o/p which depends on select i/p.

### 1 : 4 demultiplexer



$$Y_0 = \bar{A} \bar{B} D_{in}$$

$$Y_1 = \bar{A} B D_{in}$$

$$Y_2 = A \bar{B} D_{in}$$

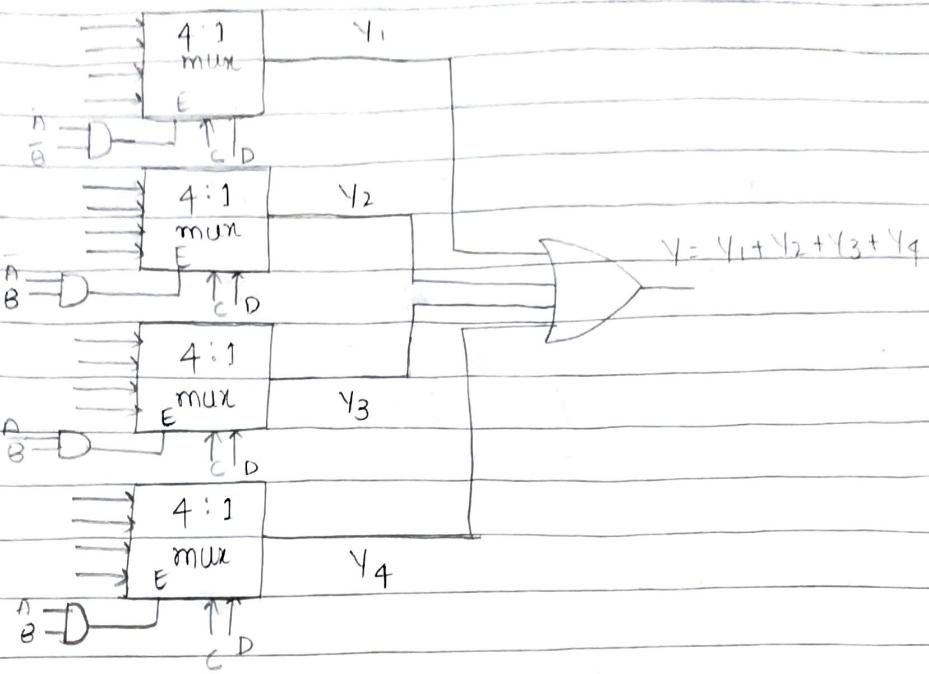
$$Y_3 = A B D_{in}$$

Truth table :

select i/p	o/p				
A	B	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
0	0	D	0	0	0
0	1	0	D	0	0
1	0	0	0	D	0
1	1	0	0	0	D

Logic cat.





A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

## PAL and PLA - Single Chip IC's

- Programmable array logic
- AND gates programmable + OR gate fixed inputs
- For implementation of boolean function in SOP form various logic cells are used
  - i Use of only basic logic gates
  - ii "universal"
  - iii Combination of logic gates
  - iv multiplexer
  - v decoder
  - vi programmable logic devices in the form PAL and PLA

PAL and PLA are available in single IC with array of AND gates generating minterms, and set of OR gates for summation of minterms.

The AND gates and OR gates are programmable here no. of inputs to the AND gate and no. of connections to OR gates are programmable.

By using single IC any SOP expression of n variable can be implemented

There are diff sizes available for PLD (Programmable Logic Device)

Eg: PAL Size  $\rightarrow 16 \times 4 \rightarrow 4$  OR gates

$\downarrow$   
16 AND gates

No. of inputs = 4 ( $2^4 = 16$ )

These devices are mainly used for implementation of boolean functions

PAL - Programmable Array Logic.

- AND gates are programmable and OR gates have fixed i/p

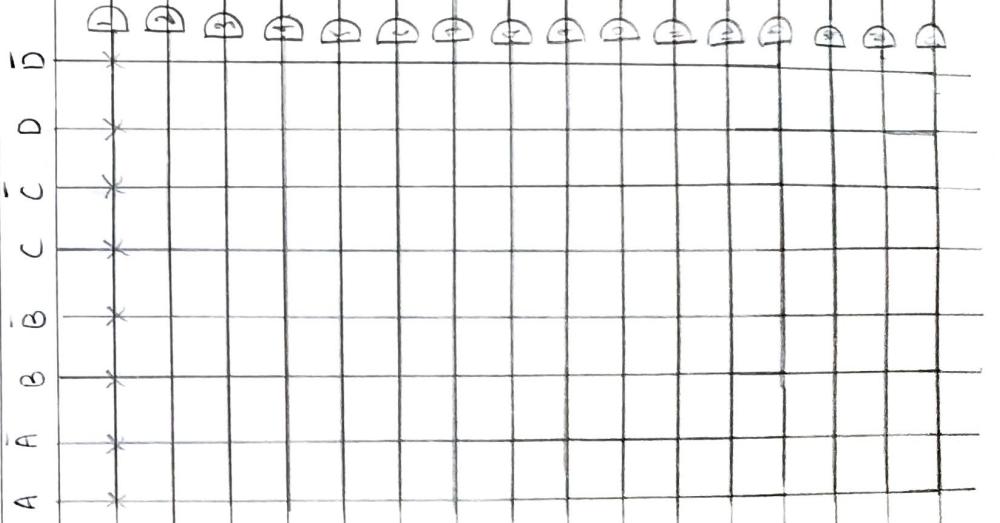
Before programming fuses are present for all the I/Ps and during programming the unwanted I/Ps are disconnected by using current which melts the fuse

Consider PAL  $\rightarrow 16 \times 4$

X - fusible link.

- solid connection fixed

of



no.  
ns to

e can

Implement following boolean funct<sup>n</sup> by using suitable  
Size PAL

$$Y_1 = A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}$$

$$Y_2 = A\bar{B}\bar{C} + A\bar{B}CD + \bar{A}BCD + AD$$

$$Y_3 = A\bar{B}\bar{C}\bar{D} + ABC$$

$$Y_4 = A\bar{B}\bar{C}\bar{D} + A\bar{B}C + ACD$$

4 o/p equ<sup>n</sup> so 4 OR gate

4 i/p variable so 2<sup>4</sup> = 16 AND gates

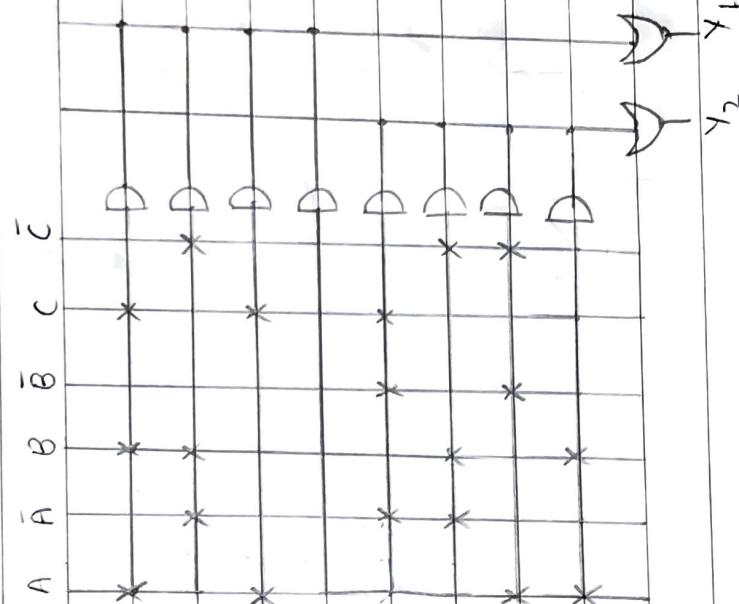
: Size of PAL  $\rightarrow 16 \times 4$

{ equ<sup>n</sup> has more than 4, express<sup>n</sup> reduce to 4 or less

Implement following "funct" by using suitable size  
PAL

$$Y_1 = ABC + \bar{A}\bar{B}\bar{C} + AC$$

$$\begin{aligned} Y_2 &= \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C + ABC \\ &= \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB \end{aligned}$$



$\gamma_2$

$\gamma_1$

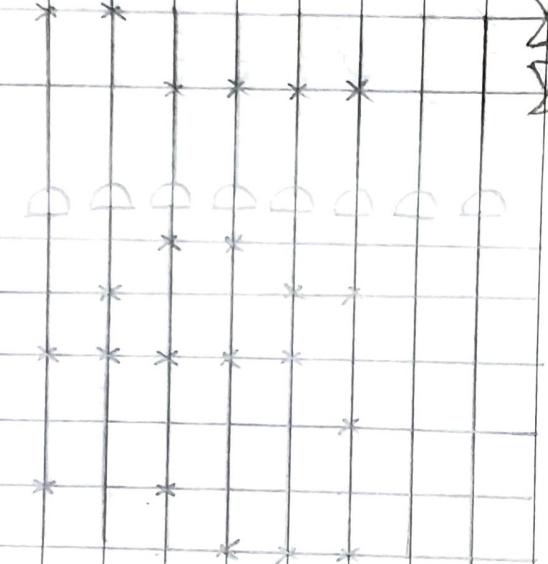
PLA - both AND gates and OR gates are programmable  
Implement following funct by using suitable size PLA

$$\begin{aligned} f_1(A, B, C) &= \sum m(0, 1, 5) \\ f_2(A, B, C) &= \sum m(0, 4, 5, 7) \end{aligned}$$

$$\begin{aligned} f_1 &= m_0 + m_1 + m_5 &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC \\ f_2 &= m_0 + m_4 + m_5 + m_7 &= \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AC \end{aligned}$$

$$\begin{aligned}
 f_1 &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}C \\
 &= \bar{A}\bar{B}\cancel{C} + A\bar{B}C \\
 &= \bar{B}(\bar{A} + AC) \\
 &= \bar{B}(\bar{A} + C) \\
 &= \bar{A}\bar{B} + \bar{B}C.
 \end{aligned}$$

①

A  $\bar{A}$  B  $\bar{B}$  C  $\bar{C}$ 

- ② Only 4 AND gates are connected

## UNIT - III

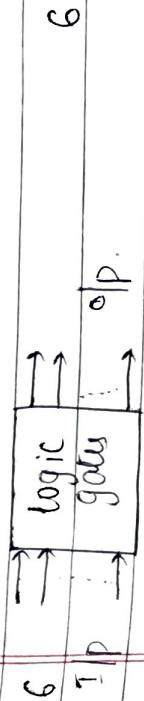
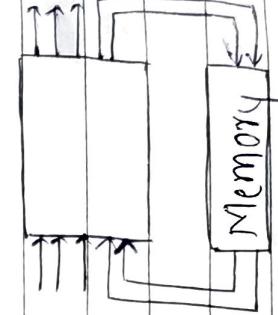
## CLOCK AND FLIP FLOPS

Digital Ckt's :

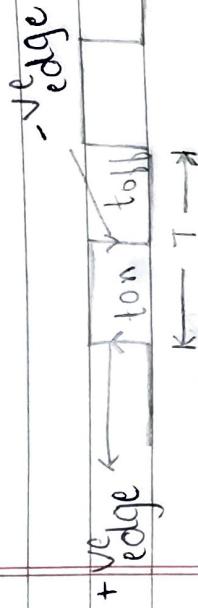
Combinational logic ckt

Sequential logic ckt

- 1 In combinational logic ckt the o/p is funct<sup>n</sup> of present i/p's. It does not depend on previous value of o/p.
  2. Ckt is designed by using combinational logic gates only
  - 3 No memory element is present
  - 4 No clock signal
  - 5 Address, subtractor, decoder, encoder, magnitude comparator etc.
  6. logic op.
1. The o/p is funct<sup>n</sup> of present value of i/p and previous state of o/p's
  2. Ckt is designed by using flip flops and logic gates only
  3. Memory is present
  4. Clock signal is must
  5. Flip flops, shift register, counter, are the examples.
  6. Memory



## CLOCK :



$T$  = time period for one clock cycle = cycle time

$$T = t_{on} + t_{off}$$

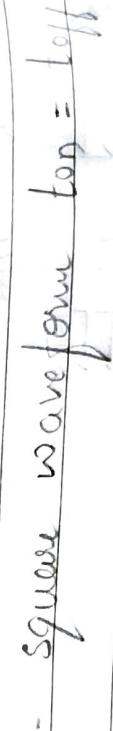
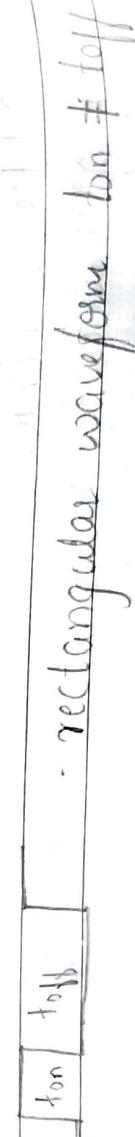
$$\% \text{ Duty cycle} = \frac{t_{on}}{T} \times 100$$

if duty cycle = 50%  $\rightarrow$  square wave  $\rightarrow t_{on} = t_{off}$   
 $\neq 50\%$   $\rightarrow$  rectangular wave.

$$\text{frequency } f = \frac{1}{T}$$

$T$  = Sec, ms,  $\mu$ sec, nsec, psec.

$$f = Hz, kHz, MHz, GHz$$



$$1 \quad f = 500 kHz, T = ?$$

$$T = \frac{1}{500 \times 10^3} = 0.2 \times 10^{-5} \text{ sec}$$

$$= 2 \times 10^{-6} \text{ sec.}$$

$$= 2 \mu \text{sec}$$

0.4 ms

$$\therefore D = \frac{0.4}{T} \times 100 = \frac{0.4 \times 10^3}{1 \times 10^{-3}} \times 100 = 40\%$$

$$f = \frac{1}{T} = \frac{1}{1 \times 10^{-3}} = 10^3 \text{ Hz} = 1 \text{ kHz}$$

$$3. f = 49 \text{ Hz. } T = ?$$

$$T = \frac{1}{4 \times 10^9} = 0.25 \times 10^{-9} \text{ s. } 0.25 \text{ ns} \\ = 250 \mu\text{s. } 250 \text{ ps.}$$

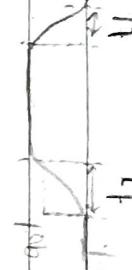
$$4. t_{on} = 50 \text{ nsec} \quad t_{off} = 150 \mu\text{sec} \\ \text{what is } f \text{ and } D$$

$$D = \frac{50 \times 10^{-9}}{200 \times 10^{-8}} \times 100 \\ = \frac{1}{4} \times 100 \\ : 25\%$$

$$f = \frac{1}{200 \times 10^{-6}} = 0.005 \times 10^6 = 5 \times 10^3 \\ = 5 \text{ kHz}$$

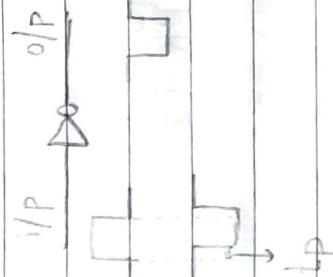
Characteristics of a clock:

- Ideal clock.



$t_r$  - rise time.  $t_f$  - fall time

## 2 Propagation Delay delay - time gap

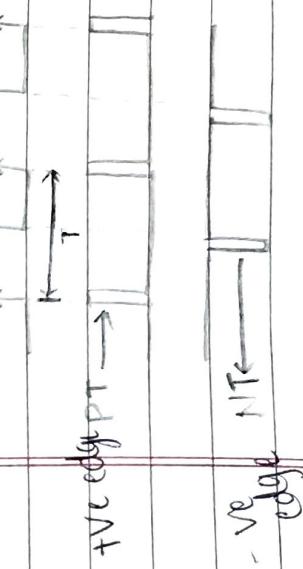


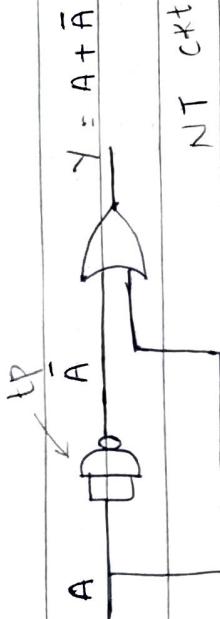
$$1C - 7400 \text{ TTL}$$
$$t_P = 10 \text{ nsec}$$

$$\text{Speed} = \frac{1}{t_P} = \frac{1}{10 \times 10^{-9}}$$
$$= 0.1 \times 10^9 \text{ Hz}$$
$$= 100 \text{ MHz.}$$

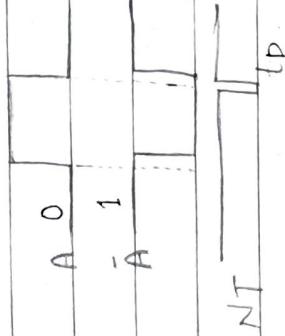
$$t_P = \frac{t_{PHL} + t_{PLH}}{2}$$

## 3 PT and NT





NT Ckt



PT Ckt



23/9/19

## Flip flops.

Depending on characteristics there are 3 devices.

- 1 Bistable  $\rightarrow$  O/p being high (1) or low (0) is stable
- 2 Monostable  $\rightarrow$  O/p <sup>unstable</sup>  $\xrightarrow{\text{stable}} \text{high} \xrightarrow{\text{tp}} \text{low} \xrightarrow{\text{tp}} \text{high}$
- 3 Astable  $\rightarrow$  both states are not stable.

Eg: clock ckt

Flip flop : It is a bistable device having 2 stable state (op being 0 or 1)

- The stable state is changed to another stable state by applying external signal called trigger.
- Usually trigger is short duration pulse going from high to low.
- Bistable device / FF finds application in memory device RAM, registers and counters.
- Basically they are used to store binary info.
- The info. will change upon application of trigger.

Types of flip flops.

- 1 S-Q FF
- 2 D FF
- 3 T FF
- 4 J-K FF.

Set - op is 1 (high)  
Reset/clear - make op 0 (low)

S & FF using NOR gate  $\rightarrow$  Basic FF (Clatch)



Previous State

Present State

Next State

P<sub>11</sub> S P<sub>12</sub> S $Q_t \rightarrow P.S$  $Q_{t-1} Q_t 1 \rightarrow P.S$  $Q_{t+1} Q_t 1 \rightarrow N.S$ 

Truth table of SR FF.

T/P      O/P      Remark

S      R      Q       $\bar{Q}$ 

0	0	2	No	No change of state
0	1	3	0	Reset condition
1	0	1	1	Set condition
1	1	4	Ambiguous	Now allowed O/P forbidden O/P

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Basic SR FF using NAND Gates :-

S	R	Q	$\bar{Q}$	O/P	O/P
0	0	1	0	0	No change of state
0	1	0	1	1	Reset condition
1	0	1	0	1	Set condition
1	1	1	1	1	Ambiguous Not allowed. O/P

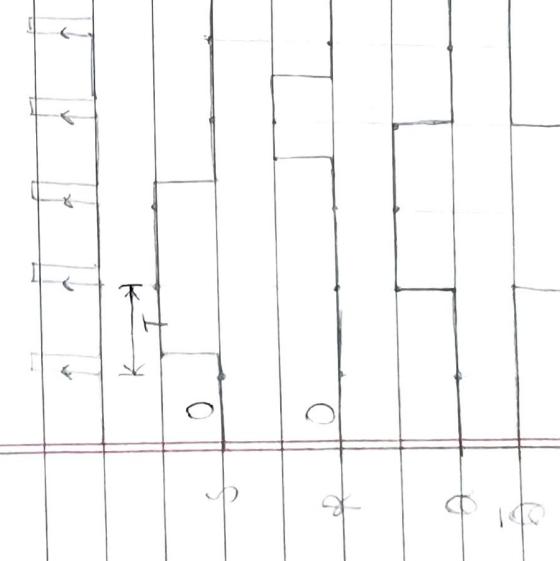
Clocked SR FF  $\rightarrow$   
Gated

Truth table

S	R	Q	i/p	O/P
EN	S	R		Q
P	$\bar{Q}$	0	X	$\bar{Q}$
↑	0	0		No change of state
↑	1	0	.	1
↑	1	0	.	0
			Set	
↑	0	1	0	1
			Reset	

↑ 1 1 1 ambiguity  
not allowed

Timing diagram for clocked SR FF (Waveforms)



D - FF  $\rightarrow$  Data FF

Clocked.

D - data delay  
memory device register

## Truth table

	D	S	Q	I/P	O/P
	clock	*	$\bar{Q}$	CLK	D
0	X			0	X
0				No change	

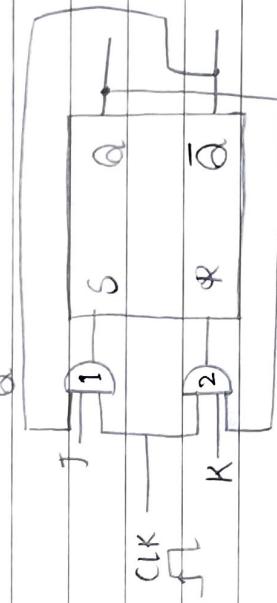
Also called as 1-bit register.  
1-bit memory.

Set ↑ 0 0 1 (Reset)

Reset ↑ 1 1 0 Set.

26/9/19

Clocked J-K FF using SR - FF



Truth table :

	CLK	J	K	Q	$\bar{Q}$	I/P	O/P
	0	X	X	"	"	No change of state	
↑	0	0	0	"	"	Reset condition	
↑	0	1	0	1	0	Set condition	
↑	1	0	1	0	1	toggle action : O/P is complement of prev. state.	
↑	1	1	1	1	0		

Waveform for JK FF



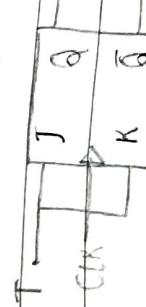
$$J = K = 1$$

Q = 0

10

$$\begin{aligned} T_a(T_{d\text{lop}}) &:= 2 \cdot T_{\text{clock}} \\ f_a &= \frac{1}{2} f_{\text{clock}} \end{aligned}$$

$T$ -FF  $\rightarrow$  Toggle flip flop:



Truth table		$\text{off}$	
CLK	$i/p$	T	$A \quad \bar{A}$
0	X		N.C. of state
↑	0	" "	" "

↑ 1 " toggle condit" -  $Q/p$  is compliment of prev state.

Characteristic Equations for FF :

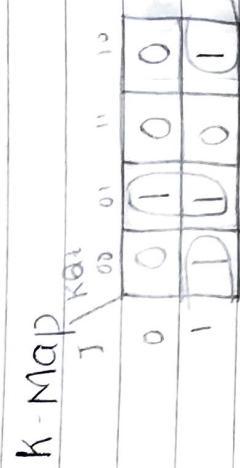
Next State  $\rightarrow Q_{t+1}$  as a function of present state  $Q_t$  and FF ips.

SR - FF

S	R	$i/p$	Previous State		Q/p		Next State	
			$Q_t$	$Q_{t+1}$	0	1	0	1
0	0	0	0	0	S	R	00	01
0	0	1	1	1	0	0	01	11
0	1	0	0	0	0	1	00	10
0	1	1	0	1	1	1	11	X
1	0	0	1	1	1	0	00	01
1	0	1	1	0	1	1	10	11
1	1	0	X	X	1	1	X	X
1	1	1	X	X	1	1	X	X

J-K FF

J		K	$Q_t$	$i/p$	Q/p		$Q_{t+1}$		$i/p$
J		K	$Q_t$	$Q_{t+1}$	0	1	0	1	0
N.C.	0	0	0	0	Set	{ 1	0	0	1
	0	0	1	1		{ 1	0	1	1
Reset	0	1	0	0	0	1	1	0	1
	0	1	1	X	toggle	{ 1	1	0	1
Set	1	0	0	1		{ 1	1	0	0
	1	0	1	1		{ 1	1	1	0
Invert	1	1	0	X		{ 1	1	1	0
	1	1	1	X		{ 1	1	1	0



$$Q_{t+1} = T\bar{Q}_t + \bar{T}Q_t$$

T - FF

I/p.      O/p.

	T	Q <sub>t</sub>	Q <sub>t+1</sub>
No Change	0	0	0
0	1	1	1
Toggle	1	0	1
1	1	1	0

$$Q_{t+1} = \bar{T}Q_t + T\bar{Q}_t$$

$$Q_{t+1} = T \oplus Q_t$$

D - FF

I/p      O/p

	D	Q <sub>t</sub>	Q <sub>t+1</sub>
0	0	0	0
0	1	0	0
1	0	1	1
1	1	1	1

$$\therefore Q_{t+1} = D$$

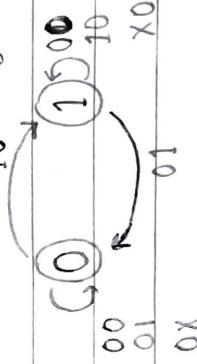
$$Q_{t+1} = \bar{D}\bar{Q}_t + DQ_t$$

$$Q_{t+1} = D$$

state diagram of FF (i.e.) SR - FF

State diagram is pictorial (visual) representation of various states of FF/circuits and interconnection between them

- The transition between 2 states is shown by  $\rightarrow$
- The flip flop i/p's which are responsible to change the state are indicated along with line



### State Transition table or Excitation

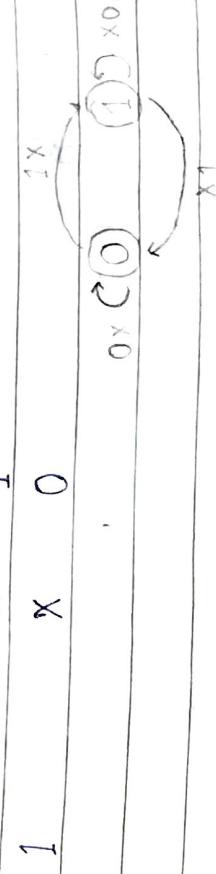
P.S	N.S	i/p	O/p
At	Q <sub>t+1</sub>	FF i/p's	X $\rightarrow$ O or 1
0	0	S X	S R
0	1	0 1	0 1 - NC 0 1 - Reset
1	0	0 1	1
1	1	X 0	1 X

30/9/19

State Diagram and State Excitation table of JK FF.

State excitation table.

P.S	N.S	FF i/p's	J	K
At	Q <sub>t+1</sub>	J K	0	1
0	0	0 X	1	0
0	1	1 X	1	1
1	0	X 1	1 X	1
1	1	X 0	1 X	1 X



State diagram

## State Diagram and State Excitation Table for 'T' FF

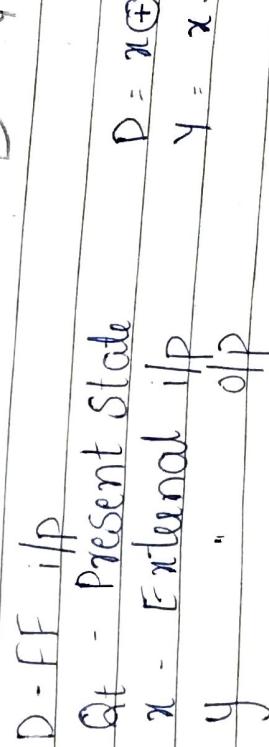
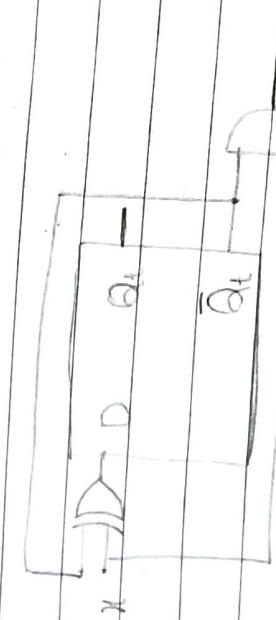
State Excitation table

PS	NS	FF i/p
Q <sub>t</sub>	Q <sub>t+1</sub>	T
0	0	0
0	1	1
1	0	1
1	1	0

State Diagram and State Excitation Table for 'D' FF

PS	NS	FF i/p
Q <sub>t</sub>	Q <sub>t+1</sub>	D
0	0	0
0	1	1
1	0	0
1	1	1

1 Analysis of Sequential Circuits :



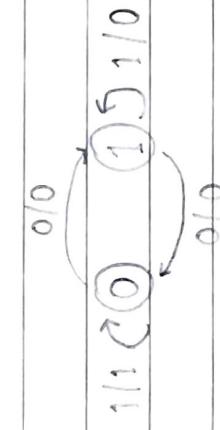
$$D = x \oplus \bar{Q}_t$$

$$Y = x \cdot \bar{Q}_t$$

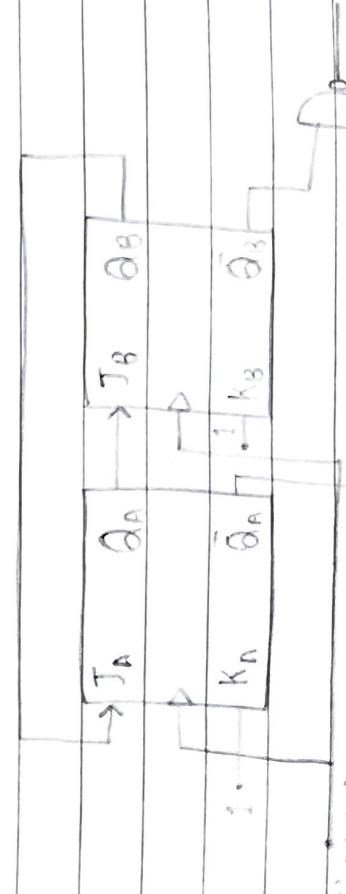
## State Excitation table

$x$	$Q_t$	Next State				
		Ext. i/p	PS	FF i/p	NS	O/P
0	0	1	1	1	0	
0	1	0	0	0	0	
1	0	0	0	0	1	
1	1	1	1	1	0	
						Sum : $Q_A$
						D i/p

State Diagram: iplop. n/y



2 Analyse the given sequential ckt:

 $Q_A, Q_B \rightarrow \text{State Variables}$ 

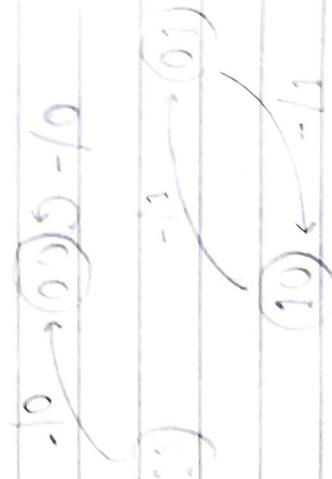
$$J_A = \underline{Q_B} \quad J_B = Q_A \quad K_A = K_B = 1$$

$$\begin{aligned} y &= \underline{Q_A} \cdot \bar{Q_B} \\ &= Q_A + Q_B \end{aligned}$$

## State Transition table

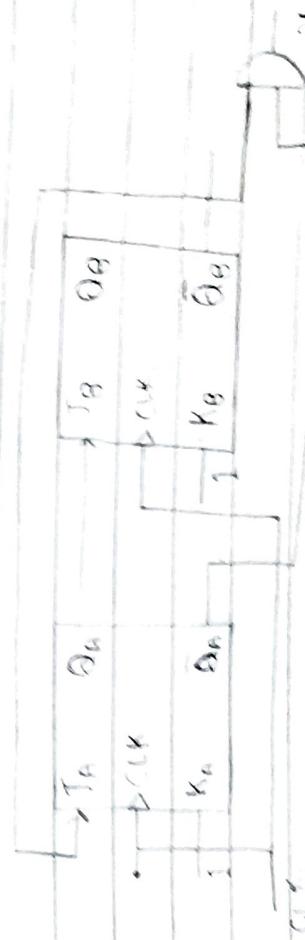
		Q <sub>t+1</sub>									
		P.S			FF i/p			N.S		N.S o/p	
		Q <sub>A</sub>	Q <sub>B</sub>	T <sub>A</sub>	K <sub>A1</sub>	T <sub>B</sub>	K <sub>B1</sub>	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>A</sub> , Q <sub>B</sub>	N.Y
		Q <sub>A</sub>	Q <sub>B</sub>	T <sub>A</sub>	K <sub>A1</sub>	T <sub>B</sub>	K <sub>B1</sub>	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>A</sub> , Q <sub>B</sub>	N.Y
0	0	0	0	1	0	1	0	0	0	0	0
0	1	1	1	1	0	1	1	0	1	1	1
1	0	0	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0	0	0	0	0

State Diagram :



3-10-19

3 Analyse given sequential Ckt



$$T_A = \bar{Q}_B \quad T_B = \bar{Q}_A \quad K_A = K_B = 1$$

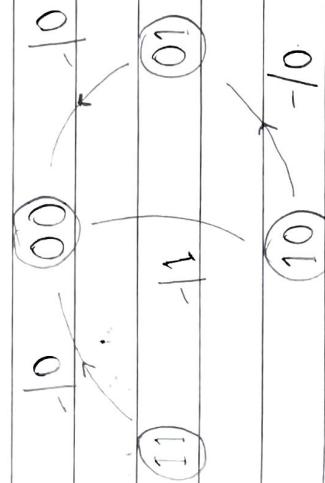
$$Y = \bar{Q}_A \bar{Q}_B$$

$$Y = (\bar{Q}_A + \bar{Q}_B)$$

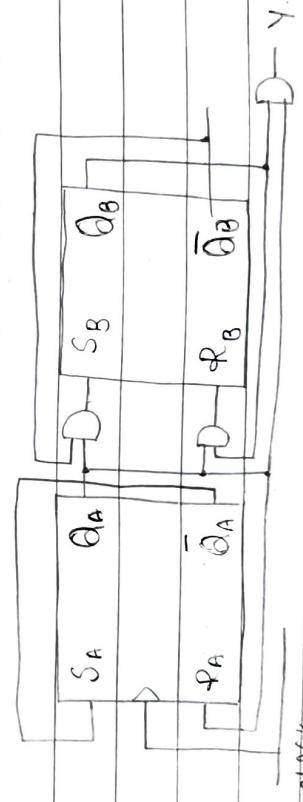
$Q_A$  and  $Q_B$  are state variables.

State Transition table.

		PS( $Q_t$ )				FF ips.				NS( $Q_{t+1}$ )				Present O/p	
$Q_A$	$Q_B$	$J_A$	$K_A$	$J_B$	$K_B$	$Q_A$	$Q_B$	$Q_A$	$Q_B$	$Q_A$	$Q_B$	$Q_A$	$Q_B$	$y = Q_A + Q_B$	
0	0	1	1	0	1	1	0	1	0	1	0	1	0	1	
0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	
1	0	1	1	1	1	0	1	0	1	0	1	0	0	0	
1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	



Mod 3 down counter.



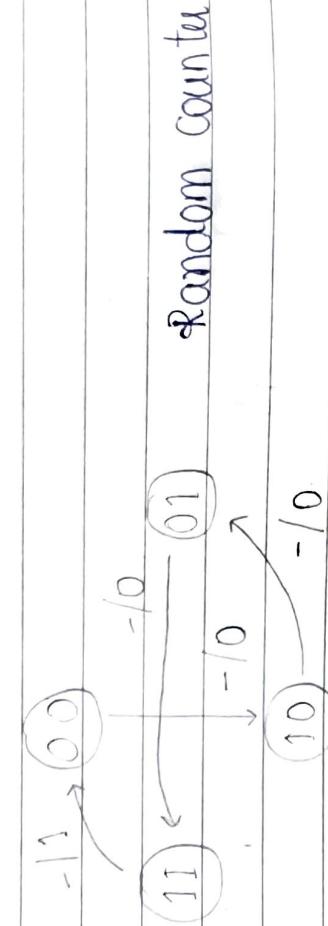
$$S_A = \bar{Q}_A \quad \bar{Q}_A = Q_A \quad S_B = Q_A \cdot \bar{Q}_B \quad \bar{Q}_B = Q_A \cdot Q_B$$

$$y = Q_B \cdot Q_A$$

## State Transition Table

		P.S.		FF flip-flops		N S		Q <sub>t+1</sub>		Present Q.P	
Q <sub>t</sub>	Q <sub>t+1</sub>	S <sub>A</sub>	R <sub>A</sub>	S <sub>B</sub>	R <sub>B</sub>	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>A</sub>	Q <sub>B</sub>
0	0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	1	1	1	0	0
1	0	0	1	1	0	0	1	0	1	0	0
1	1	0	1	0	1	0	0	1	0	0	1

State diagram



9/10/19

Conversion of flip-flops:

Convert SR FF into JK FF

Design / construct JK FF using SR FF:

State Transition Table:

		FF flip-flops		P.S		N S		FF flip-flops	
No	Change	J	K	Q <sub>t</sub>	Q <sub>t+1</sub>	S	R	S	R
0	0	0	0	→ 0	0	0	x	0	x
0	0	1	1	→ 1	1	x	0	x	0
0	1	0	0	→ 0	0	0	x	0	x
0	1	1	0	→ 0	0	1	0	1	0

J	K	$Q_t$	$Q_{t+1}$	S	$\bar{Q}_t$
1	0	0	1	1	0
set {	1	0	1	$\rightarrow$	1
1	1	0	1	$\rightarrow$	X
toggle {	1	1	0	1	0
1	1	1	0	0	1

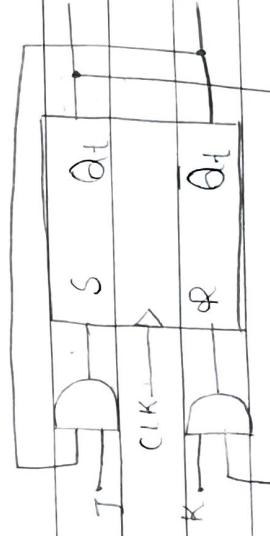
K - Map for S    K - Map for  $\bar{Q}_t$

J	K	00	01	11	10
0	0	0	X	0	0
1	1	X	0	1	1

J	K	00	01	11	10
0	0	X	0	1	X
1	0	0	1	1	0

$$S = J \cdot \bar{Q}_t \quad \bar{Q} = K \cdot Q_t$$

Logic diagram of JK FF using SR FF.



2 Construct T FF by using JK FF

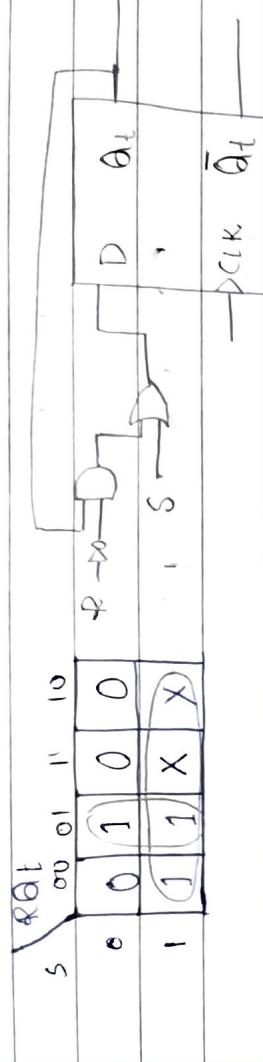
## State Transition Table

	FF i/p s	PS	NS	FF i/p s
T	$Q_t$	$Q_{t+1}$	$J$	K
No Change	0	0	0	X
Toggle	0	1	X	0
	1	0	1	
	1	1	0	

Construct SR FF using D - FF

	FF i/p s	PS	NS	FF i/p s
S	$Q_t$	$Q_t$	$Q_{t+1}$	D
0	0	0	0	0
NC	0	0	1	1
	0	1	0	0
	0	1	1	0
	1	0	0	1
	1	0	1	1
Set	1	1	0	X
Reset	1	1	1	X

K - Map for D input.



$$D = \bar{R}Q_t + S$$

10/10/19

Convert SRFF to T FF.

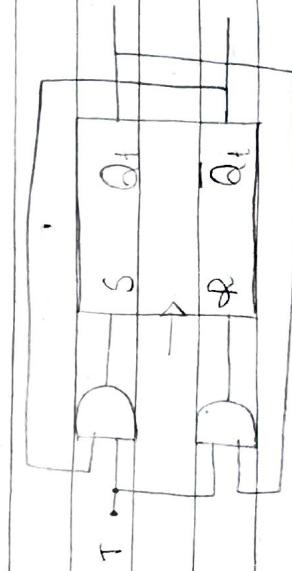
State Transition Table :

T	$Q_t$	$Q_{t+1}$	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

Equ" for S - R.

T	$Q_t$	$Q_{t+1}$	T	$Q_t$	$Q_{t+1}$
0	0	X	0	X	0
1	1	0	1	0	1

$$S = T \bar{Q}_t \quad R = T Q_t$$



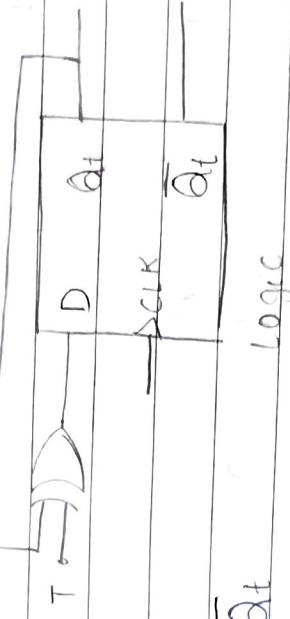
Construct T & FF using D FF.

State transition table :

	FF flip	PS	NS	FF flip
T	$Q_t$	$Q_{t+1}$	D	
0	0	0	0	
0	1	1	1	
N.C				
1	0	1	1	
Toggle	1	0	0	
1	1	0	0	

Equ' for D

T	$Q_t$	0	1
0	0	1	
1	1	0	



$$D = \bar{T}Q_t + T\bar{Q}_t$$

- $\bar{T} \oplus Q_t$

Types of Registers and

Registers is group of D-flip flop used to store binary info. 0 and 1.

- 1 - D flip flop is required to store 1-bit info.
- Clock is connected to all D-flip flops in register
- Memory is array of register
- Each register has unique address
- During R/W operation the data from register is

available on system data bus or copied from the data bus to memory.

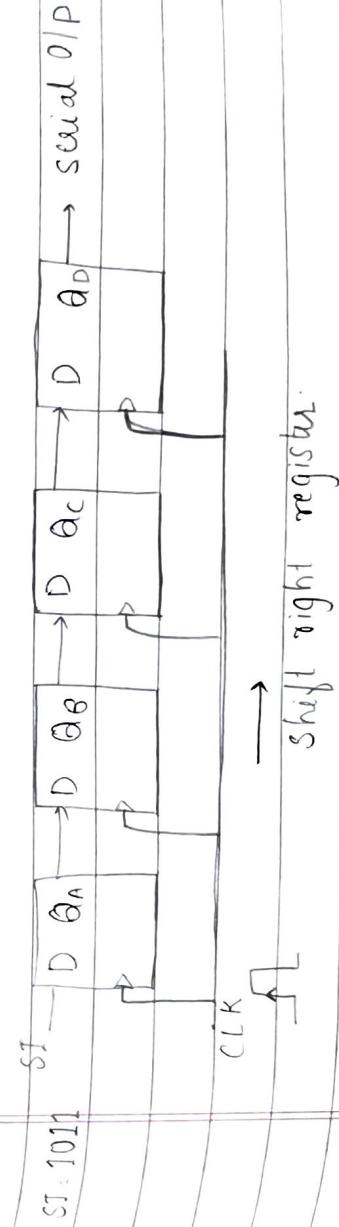
- D-FF is called as 1-bit register
- Depending on the I/p and O/p mode of data transfer there are 4 types of registers.
  - 1 Serial - in - Serial - out (SISO)
  - 2 Serial - in - Parallel - Out (SIPO)
  - 3 Parallel - in - Serial out (PISO)
  - 4 Parallel - in - Parallel - Out (PIPO)

### Shifting of data

- 1 Shift right  $\Rightarrow$  MSB  $\rightarrow$  LSB
- 2 Shift left  $\Rightarrow$  MSB  $\leftarrow$  LSB.

Parallel data - n bit data with single clock cycle / pulse  
 Serial data - 1 bit per clock

- 1 SISO register (4 bits)



- In SISO register 1 bit of data is applied with 1 clock pulse
- For n-bit register n-clock cycles are required to insert the data in register

- The clock is common to all FF
- The Q o/p of FF is same as D i/p.
- The data transfer takes place with positive trigger

P1

CLK pulse      Data

	Qn	Qn	Qn	Qn
0	0	0	0	0
1 <sup>st</sup> CP	1	0	0	0
2 <sup>nd</sup> CP	1	1	0	0
3 <sup>rd</sup> CP	0	1	1	0
4 <sup>th</sup> CP	1	0	1	1

Waveforms for SISO and register



For 12-bit SISO register what is time taken with 1 MHz clock

Soln: 12 bit register  
 $f = 1 \text{ MHz}$

$$\text{Time} = n \times T$$

$$= n \times \frac{1}{f}$$

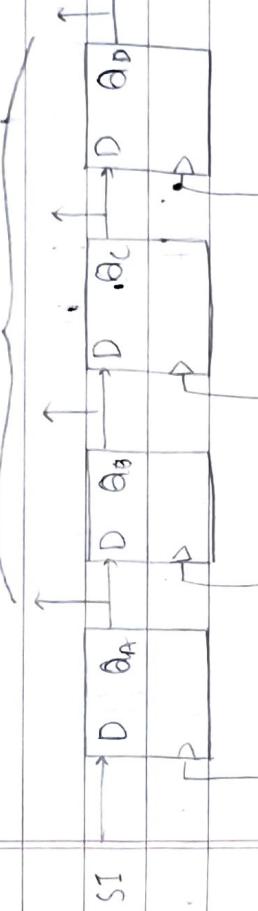
$$= 12 \times \frac{1}{10^6}$$

$$= 12 \times 10^{-6} \text{ s}$$

$$= 12 \mu\text{s.}$$

## 2. SIPO

Parallel input

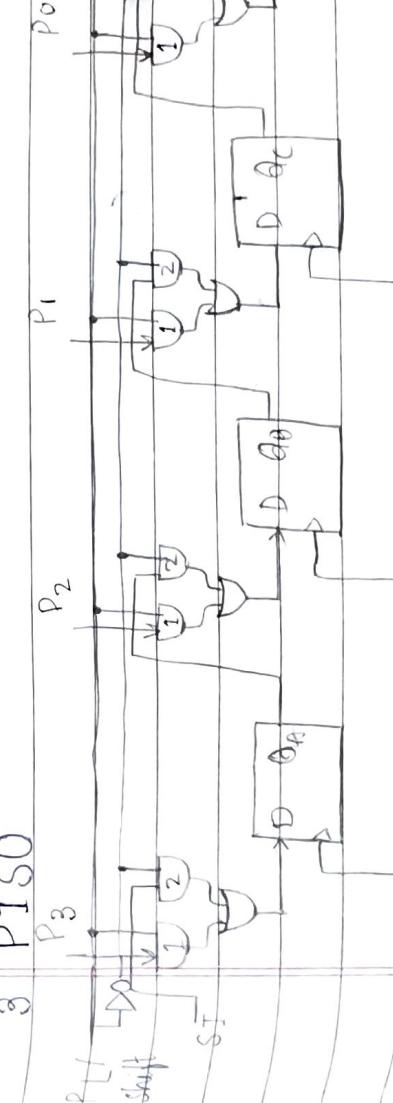


Clk  
pulse

Shift right register

Similar to STSO

## 3. PTSO



PL - Parallel Load active high

Shift - active low

ST - Serial I/P. SO - Serial O/P

$P_3 P_2 P_1 P_0 \rightarrow 4$  bit parallel i/p

- In PTSO register the i/p data is parallel and o/p is serial
- There are 2 operations in above ckt:
  1. Parallel loading of data
  2. Serial shifting of data from MSB to LSB
- To do 2 operations the additional control logic is designed by using AND, OR gates.
- The parallel load is active high and Shift is active low
- Initially PL is high so the parallel data  $P_3$  to  $P_0$  is inserted through AND 1 in the register.
- Later PL is made low so no change in the parallel data and data is shifted serially through AND gate
- 2, 1-bit per clock cycle
- The no. of clock cycles taken to o/p serially is equal to n-bits.

Count sequence

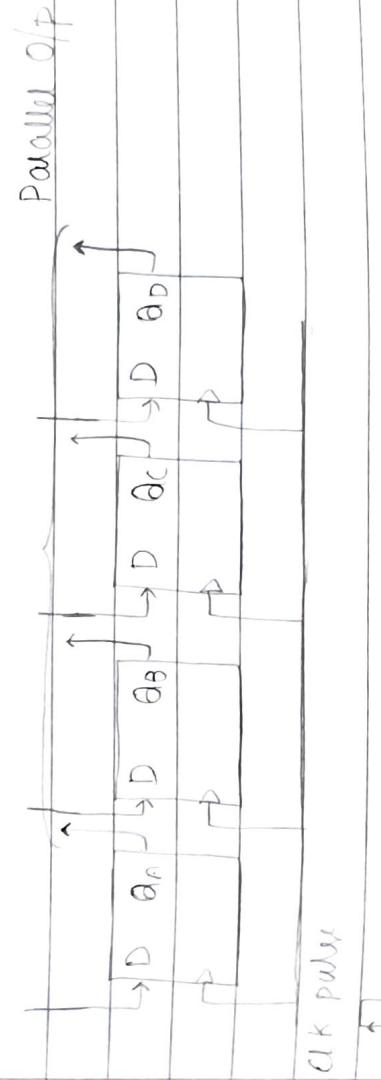
PL / Shift	$Q_A$	$Q_B$	$Q_C$	$Q_D$
-	0	0	0	0
PL	$P_3$	$P_2$	$P_1$	$P_0$
0	ST	$P_3$	$P_2$	$P_1$
0	ST	ST	$P_3$	$P_2$
0	ST	ST	ST	$P_3$

$$P_3 P_2 P_1 P_0 = 1010$$

$$SI = 0$$

CLK	$Q_{15} Q_{14} Q_{13} Q_{12}$	$Q_{11} Q_{10} Q_{9} Q_{8}$	$Q_7 Q_6 Q_5 Q_4$	$Q_3 Q_2 Q_1 Q_0$
Initial	0 0 0 0	1 0 1 0	0 1 0 1	0 0 1 0
PL = 1	1 1 CP	1 0 1 0	0 1 0 1	0 0 0 1
PL = 0	2	0 1 0 1	0 0 1 0	0 0 0 1
	3	0 0 1 0	0 0 0 1	0 0 0 0
	4	0 0 0 1		
	5	0 0 0 0		

#### 4 PIP0 register



If parallel i/p  $\rightarrow 1011$  then with one clock pulse  
 Parallel o/p  $\rightarrow Q_{15} Q_{14} Q_{13} Q_{12} = 1011$

- In PIP0 register the i/p and o/p is parallel.
- The i/p databus is connected to D inputs of all FF's and the Q o/p is connected to o/p databus
- 4 bits are transferred in 1 CLK cycle so the speed of transfer is very high and same as system clock
- These registers are present in memory devices and within CPU