USN | | | | | | | | | | |

16CS34/18CS/IS35

Third Semester B.E. Makeup Examination, January 2020

COMPUTER ORGANIZATION / COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions:
1. *Answers must be brief and to the point.*
2. *Suitable data may be assumed, with better reasoning.*
3. *Draw diagrams, wherever necessary.*
4. *Write question number properly.*
5. *Answer any FIVE full questions choosing at least one from each unit.*

UNIT - I

			L	CO	PO	M
1	a.	With the block diagram of connections between the processor and memory, identify typical steps of execution of an instruction.	(2)	(1)	(1)	(06)
	b.	Define performance of a computer. How slower memory affecting performance is overcome? Define processor clock, with a waveform.	(1)	(1)	(1)	(06)
	c.	Program execution time, T, is to be examined for a certain high-level language program. The program is run on a R or a C computer. The value of S in the T expression for the RISC machine is 1.2, but it is only 1.5 for the CISC machine. Both machines have the same clock rate, R. Calculate the largest allowable value for N, the number of instructions executed on the C machine, expressed as a percentage of the N value for the R machine, if time for execution on the C machine is to be no longer than that on the R machine?	(3)	(2)	(2)	(08)

OR

2	a.	Calculate overall SPEC rating, with the running time data, of reference computer and computer under test.	(3)	(1)	(2)	(05)
	b.	Explain Straight-line and Branching sequencing; with example - addition of n number program.	(2)	(2)	(1)	(05)
	c.	For all 10 addressing modes, identify examples of assembly language instructions, and list them all.	(2)	(2)	(1)	(10)

Running time in μS	Suite 1	Suite 2	Suite 3	Suite 4
Reference Computer	600μS	100 μS	200 μS	800 μS
Computer under test	400 μS	80 μS	210 μS	500 μS

UNIT – II

			L	CO	PO	M
3	a.	Develop an ALP that reads one line from the keyboard, stores it in memory buffer, and echoes it back to the display, using pseudo code.	(3)	(2)	(1)	(06)
	b.	Summarize the sequence of events involved in handling an interrupt request from a single device.	(2)	(1)	(1)	(06)
	c.	Explain all three methods of handling multiple devices, with neat sketches and brief operation.	(2)	(1)	(1)	(08)

OR

4	a.	Explain the different registers used in a DMA interface. Illustrate the use of DMA controllers in a computer system.	(2)	(1)	(1)	(06)
	b.	Explain Centralized bus Arbitration scheme with neat sketch.	(2)	(1)	(1)	(06)

c. Assume that two devices, A and B, having ID numbers 5_{10} $(0101)_2$ and 6_{10} $(0110)_2$, respectively. Point out which device is selected by distributed arbitration. (4) (3) (2) (08)

L CO PO M

UNIT - III

6 a. With the help of relevant circuit diagram for static RAM cell, explain how a Read and Write can be performed on it. (2) (2) (1) (06)

b. Show the configuration of a ROM cell and compare the different ROM memories. (1) (2) (1) (05)

c. Illustrate the different mapping functions of cache. (2) (2) (1) (09)

OR

6 a. Build an organization of a 1K x 1 memory cell and explain its working. (3) (2) (1) (06)

b. Explain direct memory mapping technique. (2) (2) (1) (06)

c. Explain the internal organization of a 2M x 8 asynchronous DRAM chip. (2) (2) (1) (08)

L CO PO M

UNIT - IV

7 a. Solve using Booth's Algorithm, the multiplication of +15 and -8 (4) (3) (2) (08)

b. Solve using Bit – pair Algorithm, the multiplication of +13 and -6 (4) (3) (2) (08)

c. Explain n – binary Addition – Subtraction logic network. (2) (3) (1) (04)

OR

8 a. Solve using Restoring Algorithm, the Divide 8 by 3 (4) (3) (2) (08)

b. Solve using Non – Restoring Algorithm, the Divide 12 by 5 (4) (3) (2) (08)

c. With neat sketch show a 4 bit carry look ahead binary adder (1) (3) (1) (04)

L CO PO M

UNIT -V

9 a. Explain Single – bus organization of the data path inside a process. (2) (4) (1) (0[illegible])

b. Illustrate with a diagram, input and output gating for registers, for the expressions:

1. $R1_{out}$, Y_{in}
2. $R2_{out}$, SelectY, Add, Z_{in}
3. Z_{out}, $R3_{in}$

(3) (4) (1) (06)

c. Rewrite the control sequence for the instruction: Add (R3), R1 (2) (4) (1) (08)

OR

10 a. Explain Three – bus organization of the datapath inside a process. (2) (4) (1) (10)

b. Sketch the organization of control unit to allow conditional branching in the micro-program. (3) (4) (1) (10)

COLLEGE OF TECHNOLOGY BELAGAVI

USN | | | | | | | | | | |

18CS/IS35/16CS34

Third Semester B.E. Semester End Examination, Dec./Jan. 2019-20

COMPUTER ORGANIZATION / COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions: 1. *Answer any FIVE full questions choosing at least one from each unit.*
2. *All questions carry equal marks*

GOVT. INSTITUTE OF TECHNOLOGY (GIT) BELAGAVI

UNIT - I

			L	CO	PO	M
1	a.	With a neat diagram show connection between memory & the processor. Also explain the typical operational steps in executing an instruction.	(2)	(1)	(1)	(06)
	b.	Explain the basic performance equation and SPEC rating.	(2)	(1)	(1)	(06)
	c.	Explain the addressing modes giving its i) Assembler syntax ii) EA calculation with an example in each case.	(2)	(2)	(1)	(08)
		OR				
2	a.	What is straight line sequencing ? Explain with example.	(2)	(1)	(1)	(06)
	b.	Discuss about byte addressability, Big-endian and Little-endian assignment.	(2)	(2)	(1)	(06)
	c.	Explain the different methods to measure performance of a Computer system.	(2)	(2)	(1)	(08)

UNIT – II

			L	CO	PO	M
3	a.	What is an interrupt? With example illustrate the concept of interrupts.	(2)	(2)	(1)	(06)
	b.	With a neat block diagram explain Daisy Chain Interrupt Priority Scheme for handling simultaneous requests.	(2)	(2)	(1)	(06)
	c.	What is DMA? Why is bus Arbitration required? Explain with a neat block diagram Distributed bus arbitration approach.	(2)	(2)	(1)	(08)
		OR				
4	a.	What is an interrupt? Explain with a diagram, how interrupt request from several I/O devices can be communicated to a processor through a single INTR line.	(2)	(2)	(1)	(06)
	b.	Discuss different ways to enable and disable interrupts in a system.	(2)	(2)	(1)	(06)
	c.	What is DMA? Explain in brief simple arrangement for a centralized bus arbitration approach.	(2)	(2)	(1)	(08)

UNIT - III

			L	CO	PO	M
5	a.	Discuss internal organization of memory chip: 1K x 1 semiconductor RAM chip, with a block diagram.	(2)	(4)	(1)	(08)
	b.	Explain different memories in ROM family, with diagrams and key points.	(2)	(1)	(1)	(06)
	c.	Distinguish Speed, Size and Cost of Memory, in a computer, using memory hierarchy.	(2)	(1)	(1)	(06)
		OR				
6	a.	Explain, with neat diagram, Direct Mapping, for a cache consisting of 128 blocks of 16 words each, for a total of 20148 (2K) words. Assume that the main memory is addressable by 16 - bits address. Calculate Tag, Block and Word bits for the same.	(2)	(3)	(1)	(10)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

b. Describe, with neat diagram, Associative Mapping, for a cache consisting of 128 blocks of 16 words each, for a total of 20148 (2K) words. Assume that the main memory is addressable by 16 - bits address. Calculate Tag, and Word bits for the same.

	L	CO	PO	M
	(2)	(3)	(1)	(10)

UNIT – IV

		L	CO	PO	M
7	a. Make use of a block diagram to explain the sequential binary multiplier.	(3)	(3)	(4)	(06)
	b. Explain with diagram n bit ripple-carry adder.	(2)	(3)	(4)	(06)
	c. Build the circuit arrangement for binary division. Solve the given binary numbers 1000 % 0011 using non-restoring division.	(3)	(3)	(4)	(08)

OR

		L	CO	PO	M
8	a. How do you design FAST ADDERS? Explain a 4 bit carry look ahead adder.	(2)	(3)	(4)	(06)
	b. Apply Booth's algorithm to multiply the numbers -13 and +11.	(3)	(3)	(4)	(06)
	c. Build the circuit arrangement for binary division. Solve the given binary numbers 1000 % 0011 using restoring division algorithm.	(3)	(3)	(4)	(0[illegible])

UNIT –V

		L	CO	PO	M
9	a. With a neat sketch of single bus organization of the data path inside a processor, explain the three steps to be performed by the processor to execute an instruction	(2)	(4)	(4)	(10)
	b. Write the control sequence for the instruction MOVE (R1), R2.	(1)	(4)	(4)	(10)

OR

		L	CO	PO	M
10	a. Write and explain the control sequences for execution of an unconditional branch instruction.	(2)	(4)	(4)	(10)
	b. With a block diagram explain hardwired control.	(2)	(4)	(4)	(10)

GOGTE INSTITUTE OF TECHNOLOGY BELAGAVI

3rd sem
CS & IS

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

1 Set CS

16CS/IS34

Third Semester B.E. Fast Track Semester End Examination, July/August 2019

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions: 1. *Each Question carry 20 Marks*
2. *UNIT II and UNIT V are compulsory.*
3. *Answer three full questions from the remaining units*

GCT INSTITUTE OF TECHNOLOGY BELAGAVI

UNIT - I

			L	CO	PO	M
1	a.	Explain with diagram, the communication between processor and the memory. Write sequence of steps for memory read and write operations.	(1)	(1)	(2)	(08)
	b.	Discuss how single bus structure is used to connect different components of computer system. Explain different types of buses.	(1)	(1)	(2)	(06)
	c.	Discuss the Basic Performance Equation. Explain the parameters which affect the performance of computer system.	(1)	(1)	(2)	(06)

OR

2	a.	What is byte addressability? Write Big Endian and Little Endian address assignments for 2A,2B,4C,4D,5E,EF	(3)	(2)	(1)	(08)
	b.	What is an addressing mode? Explain addressing modes with syntax and an example.	(2)	(2)	(1)	(12)

UNIT – II (compulsory)

			L	CO	PO	M
3	a.	What is an Interrupt? Discuss with diagram Interrupt priority schemes.	(2)	(2)	(1)	(10)
	b.	Discuss with diagram the two approaches to bus arbitration.	(2)	(2)	(1)	(10)

UNIT - III

4	a.	Explain with diagram, the internal organization of 2M X 8 dynamic memory chip whose cells are organized as 4K X 4K array.	(3)	(2)	(1)	(12)
	b.	Draw and Explain the memory hierarchy of a computer system. Discuss the parameters speed, size and cost w.r.t. memory hierarchy.	(2)	(2)	(1)	(08)

OR

5	a.	Consider a cache consisting of 128 blocks of 16 words each, and main memory consists of 4K blocks of 16 words each. Apply set associative mapped cache with four blocks per set and generate Main memory address. Draw the diagram to show the mapping.	(3)	(3)	(1)	(10)
	b.	Explain Hit Rate and Miss Penalty. Assume that 30% of the instructions in a typical program perform a read or a write operation. It takes 17 clock cycles to load the data from main memory in case of cache miss and 1 clock cycle if it is available in cache. Given that the hit rate in the cache are 0.95 for instructions and 0.9 for data. Estimate average access time experienced by the processor.	(4)	(3)	(1)	(10)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

UNIT - IV

		L	CO	PO	M
	a. Explain how Booth's algorithm is used to multiply two signed numbers. Discuss its best case, average case and worst case multiplier.	(2)	(3)	(1)	(10)
	b. Explain with diagram IEEE floating point representation for single precision and double precision numbers	(2)	(3)	(1)	(10)

OR

7	a. Compute (24) *(-8), applying bit pair recoding algorithm.	(4)	(3)	(1)	(10)
	b. Draw and explain circuit arrangement for restoring binary division.	(3)	(3)	(1)	(10)

UNIT – V (compulsory)

		L	CO	PO	M
8	a. Explain the stages of pipeline. Show with the diagram pipelined and non pipelined concept and discuss their performance.	(2)	(4)	(2)	(12)
	b. Explain with an example dependencies in pipelined processor.	(2)	(4)	(1)	(08)

GOGTE INSTITUTE OF TECHNOLOGY, BELAGAVI

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

USN | | | | | | | | | | |

CS34/16IS/CS34

Third Semester B.E. Makeup Examination, January 2019

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions:
1. *Accurate answers expected.*
2. *Unit I & Unit II are compulsory. Answer one full question from the remaining units*
3. *Data, if necessary, may be assumed.*
4. *Diagrams, when required, may be drawn.*

UNIT - I

			L	CO	PO	M
1	a.	Interpret Basic Operational concepts showing connections between the processor and memory with a neat block diagram.	(2)	(1)	(1)	(06)
	b.	Perform the following operations on the 5 bit signed numbers using 2's complement representation system. Analyze whether an overflow occurs. (i)(-10) + (-13) (ii)(-10) - (+4) (iii)(+7) - (-15) (iv)(+8) + (+10)	(4)	(1)	(1)	(08)
	c.	Define addressing mode and explain any four addressing modes with a suitable example.	(1,2)	(2)	(1)	(06)

UNIT – II

			L	CO	PO	M
2	a.	Analyze with a program that reads a line from the keyboard, stores in memory buffer, and echoes it back to the display.	(4)	(4)	(1)	(06)
	b.	Examine all three methods of handling multiple devices, with neat sketches and function.	(4)	(2)	(1)	(06)
	c.	Illustrate distributed bus arbitration, assume two devices, A and B, with ID's 5_{10} and 6_{10} (0101_2 and 0110_2) for the sake of explanation.	(2)	(2)	(2)	(08)

UNIT - III

			L	CO	PO	M
3	a.	Explain the internal organization of a memory chip for 1Kx1 memory chip, using decoder and multiplexer.	(2)	(3)	(1)	(10)
	b.	With internal organization diagram of a 2Mx8 dynamic memory chip, explain asynchronous DRAM's.	(2)	(3)	(1)	(10)

OR

4	a.	What is Cache? Explain any two cache mapping functions with neat sketches.	(1,2)	(3)	(1)	(10)
	b.	Summarize the memory hierarchy with respect to speed, size and cost.	(2)	(3)	(1)	(06)
	c.	Briefly summarize the different types of Read Only Memory (ROM).	(2)	(3)	(1)	(04)

UNIT - IV

			L	CO	PO	M
5	a.	Explain with block diagram: ADDER/SUBTRACTOR circuit. Explain how subtraction is achieved with an example.	(2)	(2)	(1)	(06)
	b.	Explain sequential circuit multiplication, using a suitable block diagram	(2)	(2)	(1)	(06)

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

	c.	Solve for Quotient and Reminder, using Restoring Division Algorithm: 14 divide by 3.	(3)	(4)	(2)	(08)
			L	CO	PO	M
		OR				
6	a.	Define Bit-stage cell. Using Bit-stage cell explain a 4-bit binary Carry-Look-Ahead adder.	(2)	(1)	(1)	(06)
	b.	Explain the non-restoring division algorithm Perform the division of number 8 by 3 (8÷3) using .the same.	(2)	(2)	(1)	(08)
	c.	Solve for the product using Booth's Algorithm. (+15) x (-9)	(3)	(4)	(2)	(06)
			L	CO	PO	M
		UNIT -V				
7	a.	Define computer Architecture. Illustrate seven dimensions of an ISA.	(1,2)	(4)	(1)	(10)
	b.	Explain the following in brief (i) Amdahl's Law (ii) Dependability	(2)	(4)	(1)	(10)
		OR				
8	a.	Demonstrate the working of a classic five stage pipeline for a RISC processor.	(2)	(4)	(2)	(10)
	b.	Explain data hazards and methods to minimize data hazards with examples.	(2)	(4)	(2)	(10)

KLS GOGTE INSTITUTE OF TECHNOLOGY, BELAGAVI

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

USN | | | | | | | | | | |

CS34/16CS/IS34

Third Semester B.E. Semester End Examination, Dec/Jan 2018-19

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions: 1. *UNIT-I and UNIT-II are compulsory*
2. *Answer any one full question from remaining units*

UNIT - I

			L	CO	PO	M
1	a.	With the block diagram showing connection between the processor and memory, explain the functions of MAR and MDR.	(2)	(1)	(1)	(06)
	b.	List first 8 generic addressing modes, brief about - name of address mode-syntax-addressing functioncontaining effective address (EA), for each one.	(1)	(2)	(1)	(06)
	c.	For two computers R and C, with same execution time (T) and clock rate (R), solve for largest allowable value of number of instructions (N), if the effective value of basic steps (S) is 1.2 for computer R and 1.5 for computer C. Given that number of instructions (N) for computer R is 10.	(3)	(3)	(2)	(08)

UNIT – II

			L	CO	PO	M
2	a.	With neat sketches explain a method for handling interrupts from multiple devices	(2)	(2)	(1)	(10)
	b.	What is DMA? Explain in brief the simple arrangement for a centralized bus arbitration approach.	(1,2)	(2)	(1)	(10)

UNIT - III

			L	CO	PO	M
3	a.	Explain Synchronous DRAM with a block diagram.	(2)	(2)	(1)	(06)
	b.	Compare precisely ROM family: PROM, EPROM, EEPROM, Flash Memory, Flash Cards, Flash Drives	(2)	(1)	(1)	(06)
	c.	Assume you have 32 bit addresses, 32 KB of cache, 64 byte lines and 4 way set associative. Demonstrate with a block diagram.	(2)	(4)	(2)	(08)

OR

			L	CO	PO	M
4	a.	Illustrate organization of 1K x 1 memory chip for semiconductor RAM.	(2)	(4)	(2)	(06)
	b.	Compare the parameters: Speed, Size and Cost of memory hierarchy.	(2)	(1)	(1)	(06)
	c.	Explain Direct mapped cache for 128 blocks of 16 words each, a total of 2048(2K) words with 16 – bit address bus.	(2)	(4)	(2)	(08)

UNIT - IV

			L	CO	PO	M
5	a.	Explain the design of 4-bit Carry Look Ahead adder.	(2)	(3)	(2)	(08)
	b.	Multiply (+14) and (-6) using Booth's algorithm.	(3)	(3)	(2)	(07)
	c.	Perform the division of number 8 by 3 (8÷3) using restoring division method.	(3)	(3)	(2)	(05)

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

KLS GOGTE INSTITUTE OF TECHNOLOGY BELGAUM

OR

6 a. Explain sequential circuit binary multiplier with an example. (2) (3) (2) (10)

b. Explain the non-restoring division algorithm Perform the division of number 8 by 3 (8÷3) using the same. (2) (3) (2) (10)

UNIT -V

			L	CO	PO	M
7	a.	Explain the following with respect to classes of parallelism and parallel architecture: a. Types of parallelism in applications b. Major ways of parallelism. c. Categories of data-level parallelism.	(2)	(2)	(1)	(10)
	b.	Interpret computer performance, with respect to a. Measuring with three kinds of benchmarks b. Reporting performance results c. Summarizing performance results	(2)	(2)	(1)	(10)

OR

8	a.	Explain seven dimensions of an ISA.	(2)	(2)	(1)	(10)
	b.	Exemplify, a. data hazard with an example b. how it is minimized by forwarding (or bypassing or short circuiting)	(2)	(2)	(1)	(10)

KLS GOGTE INSTITUTE OF TECHNOLOGY, BELAGAVI

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

USN | | | | | | | | | | |

CS/IS/34/16CS/IS34

Third Semester B.E. Semester End Examination, Dec/Jan 2017-18

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions:
1. *Unit I and IV are COMPULSORY.*
2. *Answer ANY one full question from remaining each units.*
3. *Suitable data can be assumed giving justification.*
4. *Accuracy does matter.*

UNIT - I

1 a. Interpret Basic Operational Concepts showing connections between the processor and memory with a neat block diagram. (Level [2], CO [1], PO [1]) **06 M**

b. Convert the following pairs of decimal numbers to 5bit signed 2's complement binary numbers & add them. Analyze whether an overflow occurs.
i)+16 & +2 ii) -4 & +6 iii) -15 & +11 iv) -10 & -8. (Level [4], CO [2], PO [2]) **08 M**

c. Contrast straight-line sequencing and branching, with a program to add 10 numbers. (Level [4], CO [2], PO [1]) **06 M**

UNIT – II

2 a. Find Effective Addresses (EA) in all the Addressing Modes. (Level [1], CO [3], PO [2]) **08 M**

b. Interpret, with a neat sketch, Distributed Arbitration. (Level [2], CO [3], PO [1]) **06 M**

c. Contrast Synchronous and Asynchronous Buses with the help of relevant timing waveforms. (Level [2], CO [3], PO [1]) **06 M**

OR

3 a. Multiple Devices are connected to the processor. Distinguish the three approaches to handle such a situation, using interrupts, with diagrams, if any. (Level [4], CO [3], PO [1]) **08 M**

b. Plan a program that reads one line from the keyboard, stores it in memory buffer, and echoes it to the display, with comment lines. (Level [3], CO [3], PO [1]) **06 M**

c. Interpret, with a neat sketch, Centralized Arbitration. (Level [2], CO [3], PO [1]) **06 M**

UNIT – III

4 a. With internal organization diagram of a 2M x 8 dynamic memory chip, explain asynchronous DRAMs. (Level [2], CO [3], PO [2]) **08 M**

b. Explain Set-associative-mapped cache with two blocks per set, with neat sketch. Assume bits for tag 5, set 6 and word 4. (Level [2], CO [3], PO [2]) **06 M**

c. Summarize the memory hierarchy with respect speed, size and cost. (Level [2], CO [1], PO [1]) **06 M**

OR

5 a. Explain the internal organization of a memory chip for 1K x 1 memory chip, using decoder and multiplexer. (Level [2], CO [2], PO [1]) **08 M**

b. Explain Read Write operations with respect to Static Memories, with diagrams of a SRAM cell. (Level [2], CO [2], PO [1])

c. Explain a Read Only Memory (ROM) cell. Summarize its four types. 06 M

(Level [2], CO [2], PO [1])

UNIT – IV

6 a. Demonstrate Booth's Algorithm for signed multiplication of $+15_{10}$& -15_{10}. 06 M

(Level [4], CO [4], PO [2])

b. Evaluate product, using fast multiplication algorithm - bit-pair algorithm / method, of 14_{10} and 11_{10} 06 M

(Level [5], CO [4], PO [2])

c. Illustrate how you calculate quotient and remainder when 10_{10} is divided by 02_{10}, applying Restoring Division algorithm. 08 M

(Level [2], CO [4], PO [2])

UNIT - V

7 a. Define Computer Architecture. Outline seven dimensions of an ISA. 08 M

(Level [2], CO [1], PO [1])

b. Explain the following in Brief i) Amdahl's Law ii) Dependability. 06 M

(Level [2], CO [1], PO [1])

c. Explain Measuring, Reporting and Summarizing performance of a computer architecture. 06 M

(Level [2], CO [2], PO [2])

OR

8 a. Demonstrate the working of a classic five stage pipeline for a RISC processor. 10 M

(Level [2], CO [4], PO [2])

b. Explain data hazards and methods to minimize data hazards with examples. 10 M

(Level [2], CO [4], PO [2])

KLS GOI INSTITUTE

16CS34 / CS34 /16IS34 / IS34

Third Semester B.E. Makeup Examination, January 2018

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions:
1. *Unit I & IV are compulsory.*
2. *Answer any five full Questions.*
3. *Suitable data can be assumed giving justification.*
4. *Accuracy does matter.*

UNIT - I

1 a. With a neat diagram show the connection between memory & processor and explain typical operational steps in executing an instruction. **08 M**
(Level [2], CO [1], PO [1])

b. Convert the following pairs of decimal no's to 5 bit signed 2's complement binary numbers & add them. Analyze whether an overflow/underflow occurs. **06 M**
i) 7 & 13 ii) -5 & 7 iii) -14 & 11 iv) -10 & -13
(Level [4], CO [2], PO [2])

c. Define Addressing Mode and explain any four addressing modes with a suitable example. **06 M**
(Level [1,2], CO [1], PO [1])

UNIT – II

2 a. What is an interrupt? With a neat block diagram explain Daisy Chain Interrupt Priority Scheme for handling simultaneous requests. **10 M**
(Level [1,2], CO [2], PO [2])

b. What is DMA? Explain in brief simple arrangement for a centralized bus arbitration approach. **10 M**
(Level [1,2], CO [1], PO [1])

OR

3 a. Explain the following in brief: **10 M**
i)Program controlled I/O ii) Enabling & Disabling Interrupts
(Level [2], CO [2], PO [1])

b. Make use of a neat sketch to explain the timing diagram of Synchronous Bus for input operation **10 M**
(Level [3], CO [2], PO [2])

UNIT – III

4 a. Make use of a relevant circuit diagram for static RAM cell and explain how a Read and Write operations can be performed on it. **10 M**
(Level [3], CO [2], PO [1])

b. Make use of a suitable example and Explain Set Associative Mapping technique **10 M**
(Level [3], CO [2], PO [2])

OR

5 a. Explain the following: i) PROM ii) EPROM **05 M**
(Level [2], CO [1], PO [1])

b. Distinguish between i) SRAM ii) DRAM **05 M**
(Level [4], CO [3], PO [2])

c. With a suitable example, Explain Direct Mapping cache memory technique. **10 M**
(Level [2], CO [2], PO [1])

UNIT – IV

6 a. Give the steps of Booth's Algorithm. Evaluate the product by multiplying the following pairs of 4 bit signed 2's complement numbers using the same. **07 M**

M= +14 & Q= -10

(Level [5], CO [2], PO [2])

b. Solve usingRestoring integer Division method, the following example: $8 \div 3$ 08 M

(Level [2,3], CO [2], PO [2])

c. Explain FOUR bit Carry Look Ahead Adder. 05 M

(Level [2], CO [2], PO [1])

UNIT –V

7 a. Define Computer Architecture. Illustrate seven dimensions of an ISA. 10 M

(Level [1,2], CO [1], PO [1])

b. Explain the following in brief i) Amdahl's law ii) Dependability 10 M

(Level [2], CO [2], PO [1])

OR

8 a. What is Pipelining? List Pipeline hazards & explain any one in detail. 10 M

(Level [1], CO [1], PO [1])

b. Explain the following in brief i) Measuring ii) Quantitative principles of Computer Design 10 M

(Level [2], CO [2], PO [2])