

## Unit-IV

★ Convert SR f/f to JK f/f:-

Excitation table:-

Step 1)

$$Q_n \rightarrow Q_{n+1}$$

S R J K

0	0	0	X	0	X
0	1	1	0	1	X
1	X	0	0	X	1
1	1	Y	X	X	0

Step 2)

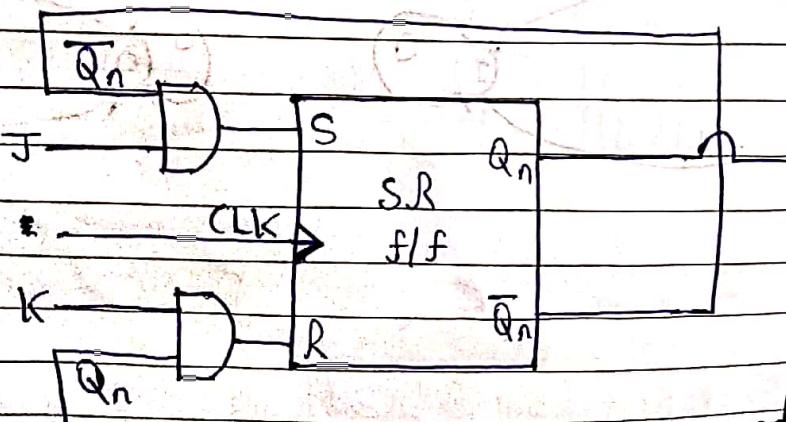
K-Map for S:-

Q <sub>n</sub>		JK				S = $\overline{Q}_n J$
		00	01	11	10	
0	0	0	1	1	X	
1	X	0	0	X		

K-Map for R:-

Q <sub>n</sub>		JK				R = $Q_n K$
		00	01	11	10	
0	X	X	0	0	X	
1	0	0	1	1	0	

Step 3) Logic block diagram:-

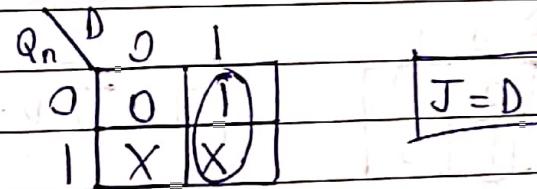


\* Convert JK f/f into D f/f :-

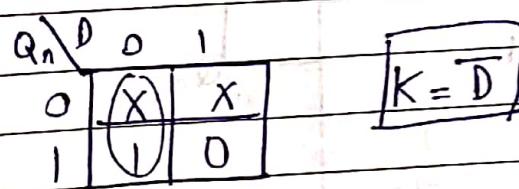
Step 1) Excitation table:-

$Q_n$	$Q_{n+1}$	J	K	D
0	0	0	X	0
0	1	1	X	1
1	0	X	1	0
1	1	X	0	1

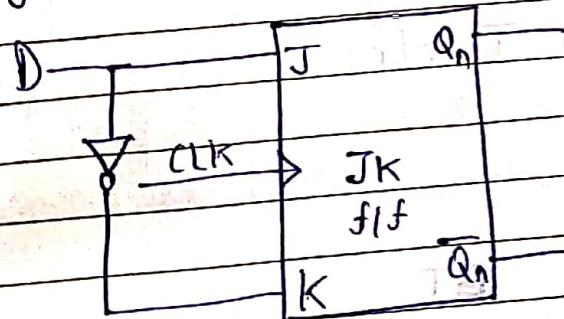
Step 2) K-Map for J:-



K-Map for K:-



Step 3) Logic block diagram:-

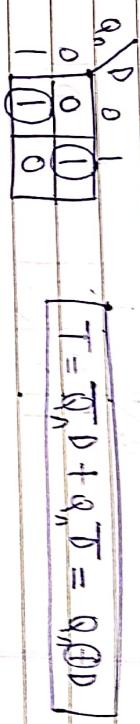


★ Convert T flip-flop into D flip-flop:-

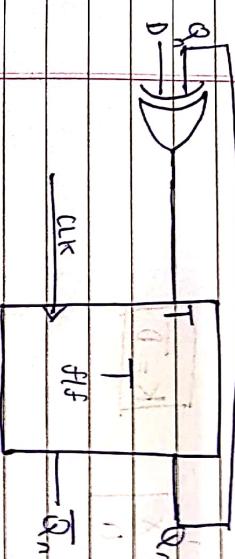
Step 2) Excitation table:-

$Q_n$	$Q_{n+1}$	T	D
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

Step 2) K-Map for T:-



Step 3) Logic block diagram:-



★ Convert JK flip-flop into T flip-flop:-

Step 2) Excitation table:-

$Q_n$	$Q_{n+1}$	J	K	T
0	0	0	X	0
0	1	1	X	1
1	0	X	1	1
1	1	X	0	0

Step 2) K-Map for J :-

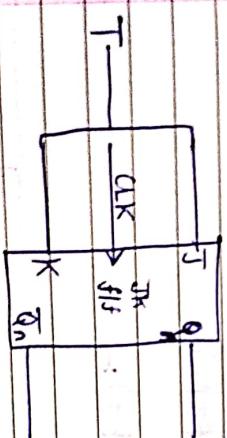
$Q_n \backslash T_n$	0	1
0	0	X
1	X	0

$$J = T$$

K-Map for K :-

$Q_n \backslash T_n$	0	1
0	X	X
1	0	0

Step 3) Logic block diagram:-



★ - Dif: betw. Combinational & sequential circuits:-

Combinational

Sequential

- In Combinational circuits, the output variable depends not only on the present set of variables but also on past history.
- Construction of input variables.
- Memory unit is not required.

Ex: Parallel adder

Fast

Easy to design.

Ex: Serial adder

Slow

Difficult to design.

## ★ Synchronous & Asynchronous Sequential Circuits :-

### Synchronous Sequential Circuit

i) Memory elements are clocked flip-flop.

ii) Change in input signals can affect memory element upon applying clock pulse.

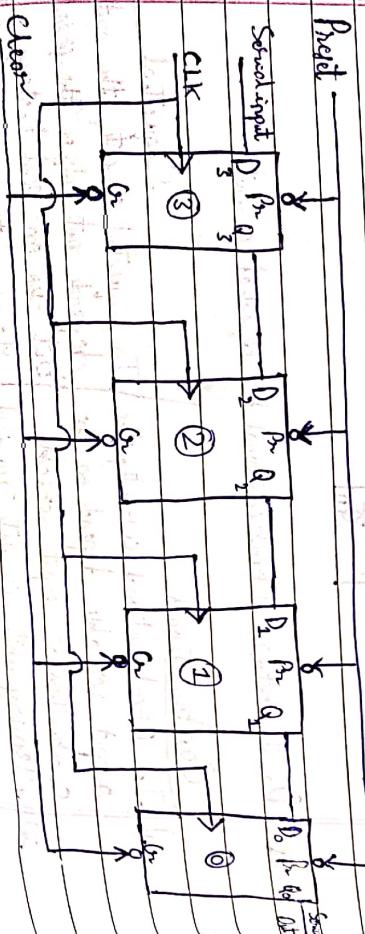
Asynchronous sequential circuit

Memory elements are randomly flip-flop.

### ★ Shift registers:-

1. Serial In Serial Out (SISO)
2. Serial In Parallel Out (SIPO)
3. Parallel In Serial Out (PISO)
4. Parallel In Parallel Out (PIPO)

### 1. SISO Shift Register (4bit) :-



Note A n-bit shift register (SISO) requires  $2n-1$  number of clock pulses to load & read the data serially.

Truth Table  
Ex: 2019

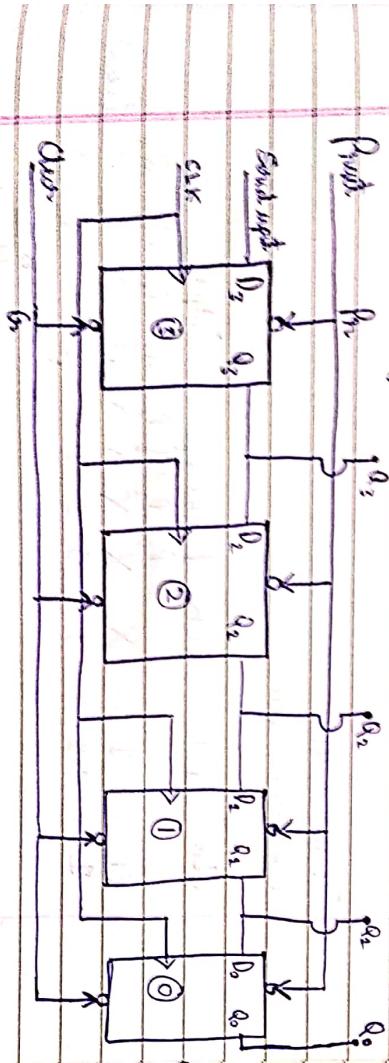
CLR P.R CLK

Serial shift

Output

Q	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	Q <sub>4</sub>	Output
1	1	X	X	X	0, 0, 0, 0 (0 <sub>out</sub> )
1	1	1	1	1	1, 0, 0, 0
1	1	1	1	0	1, 1, 0, 0
1	1	1	0	1	0, 1, 1, 0
1	1	0	1	1	1, 0, 1, 1
1	0	1	1	1	X, 1, 0, 1
1	1	0	X	X	X, X, 1, 0
1	1	1	X	X	X, X, X, 1

2. Shift Register (4-bit):-



Truth Table Ex: 2019

CLR P.R CLK Serial Out (Q<sub>i</sub>) Output

Q 1 X X 0 0 0 0 (0<sub>out</sub>)

1 1 1 1 1 0 0 0 0 (0<sub>out</sub>)

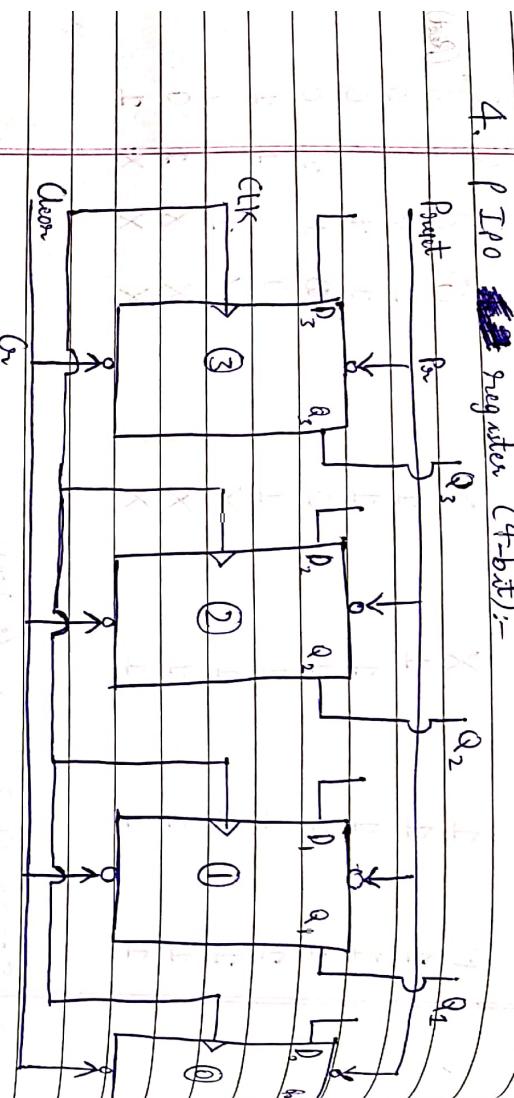
1 1 1 0 1 0 0 0 0 (0<sub>out</sub>)

1 1 2 1 1 1 0 0 0 (1<sub>out</sub>)

Parallel output

Note: For an n-bit SIPO shift register, n clock pulses are required to load & read the data.

4. P IPO register (4-bit):-



Truth Table:-

Ex.: Storing 0110

CLR    PRE    CLK    Parallel input    Output

0	1	X	$D_3\ 0\ 0\ 0$	$Q_3\ Q_2\ Q_1\ Q_0$ (Ans)
1	· 1	1	$0\ 1\ 1\ 0$	$0\ 1\ 1\ 0$

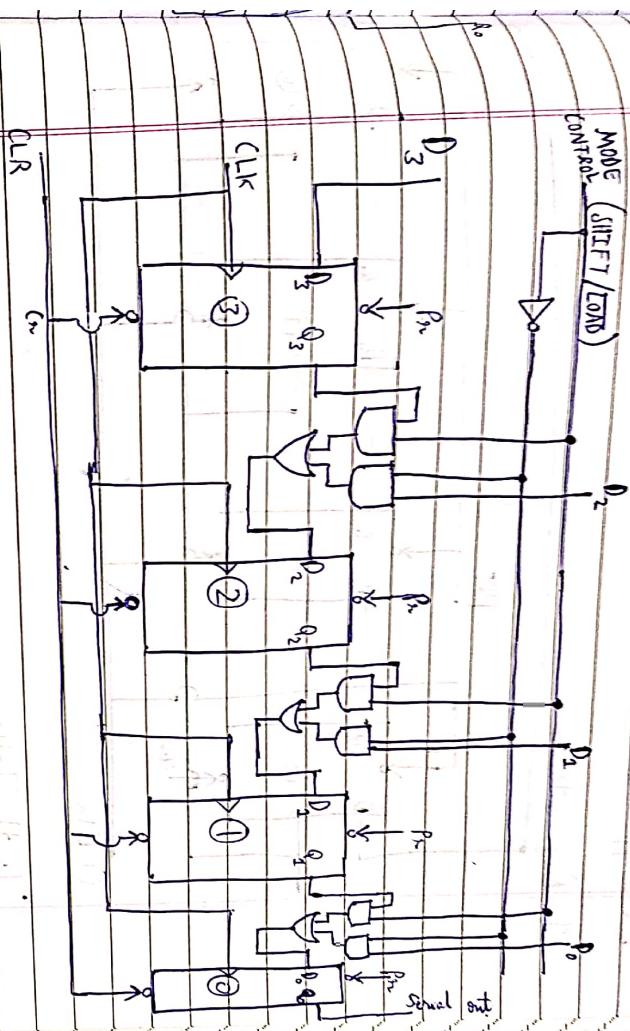
Parallel outputs

Note: For an n-bit PIPO register, only 1 clock pulse is required to load & read the data.

Q3	Q2	Q1	Q0	Parallel input	Parallel output
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	0	0
1	0	0	0	0	1

### 3. PISO Shift register (4-bit) :-

Good Luck Page No. 69  
Date 5/10/29



Truth table:-

Ex: Shifting 1011

MODE	CLR	PRE	CLK	Parallel input	Output
X	0	1	X	X X X X	0 0 0 0 (Initial)
0	1	1	1	1 0 1 1	1 0 1 1 (Input)
1	1	1	X	X X X X	X X X X (Shifted)
1	1	1	X	X X X X	X X X X (Final)

Note: For an n-bit PISO shift register, n clock pulses are required to

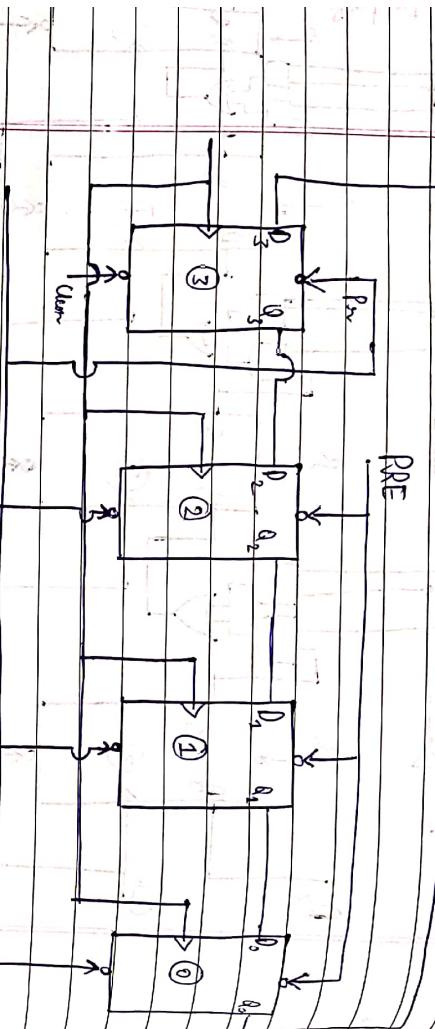
load & read the data.

MODE → 0 means load  
MODE → 1 means shift

CLR

## Applications Of Shift Registers

1. Ring Counter:-

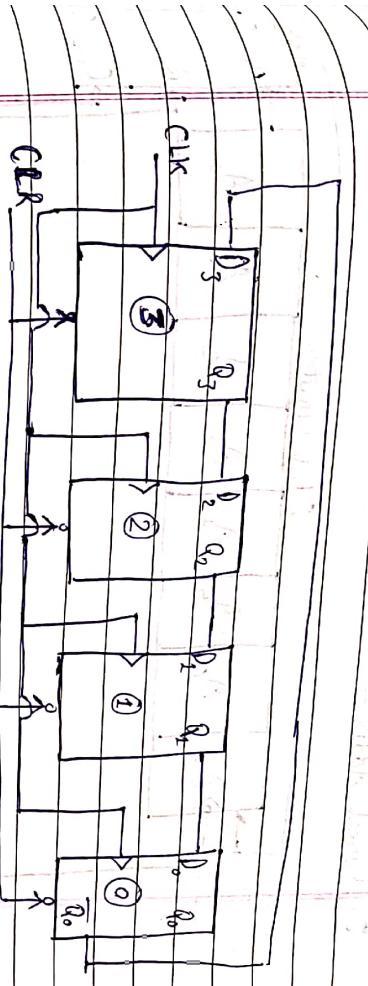


Truth Table:-

PRE	CLR	CLK	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	1	X	1	X	X	X
1	0	X	0	1	0	0
1	1	0	1	0	1	0
1	1	1	1	0	1	0
1	1	1	0	0	1	0
1	1	1	0	0	0	1
1	1	1	1	0	0	0
1	1	1	0	1	0	0
1	1	1	0	0	1	0
1	1	1	1	0	0	0
1	1	1	0	1	0	0
1	1	1	0	0	1	0
1	1	1	1	0	0	0

2. Johnson Counter:-

Goodluck  
Page No. 71  
Date 10 / 10 / 19



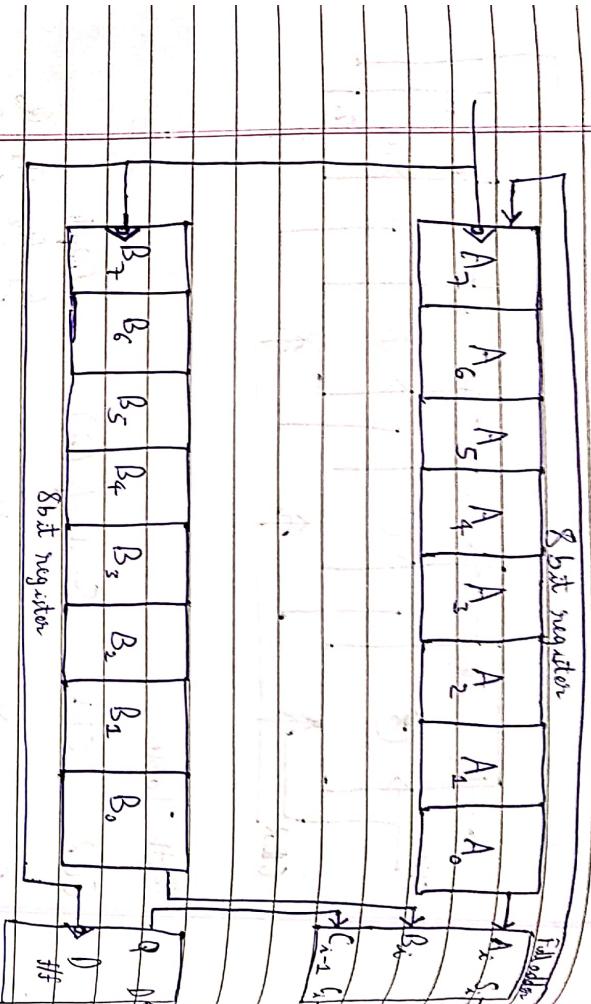
Truth Table:-

CLR      CLK      Serial Input ( $D_3$ )      Output

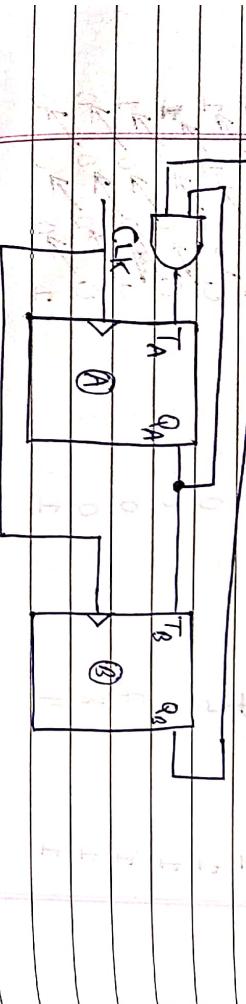
			$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	X	X	0	0	0	0
1	1	1	1	0	0	0
1	2	1	1	1	0	0
1	3	1	1	1	1	0
1	4	1	0	1	1	1
1	5	0	0	1	1	1
1	6	0	0	0	1	1
1	7	0	0	0	0	1
1	8	0	0	0	0	0
1	9	1	1	0	0	0

P.T.O.

3) Serial Address:-



\* Analyze given sequential circuit using state table & show the state transition diagram:-



→ INPUTS.

$$\overline{T_A} = Q_A \cdot Q_B \quad ; \quad T_B = Q_A$$

**State Table:**

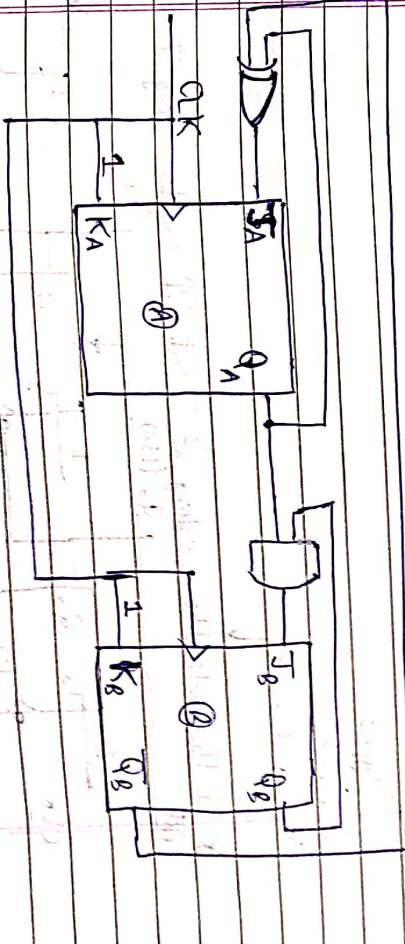
Present State	Flip-flop inputs	Next State			
$Q_A$	$Q_B$	$\bar{J}_A$	$\bar{J}_B$	$\bar{Q}_A^+$	$\bar{Q}_B^+$
0	0	0	0	0	0
0	1	0	0	0	1
1	0	0	1	1	1
1	1	1	1	0	0

(01)

(00)

(11)

(10)



**A** Analyze given sequential circuit using state table & show the state transition diagram:-

→ Inputs:

$$J_A = Q_A \oplus \bar{Q}_B$$

$$K_A = 1$$

$$J_B = Q_A \cdot \bar{Q}_B$$

$$K_B = 1$$

State Table:

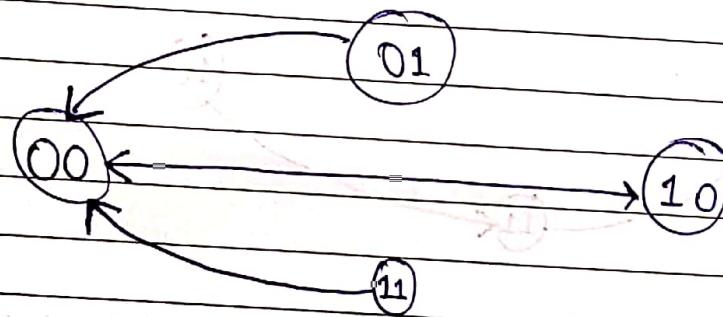
Present State

$Q_A$	$Q_B$
0	0
0	1
1	0
1	1

Flip flop inputs

$J_A$	$K_A$	$J_B$	$K_B$
1	1	0	1
0	1	0	1
0	1	0	1
1	1	1	1

Next State
$Q_A^+$
$Q_B^+$
1
0
0
0
0
0

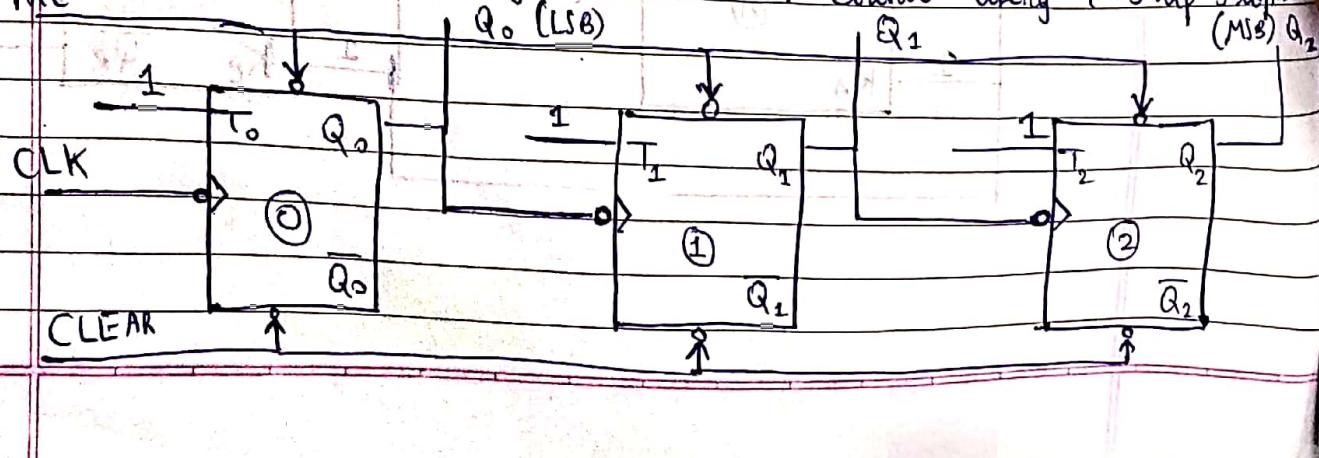


### ★ Counters:-

Types:-

- i) Synchronous
- ii) Asynchronous

\* Illustrate the working of 3 bit UP counter using T flip-flop:-

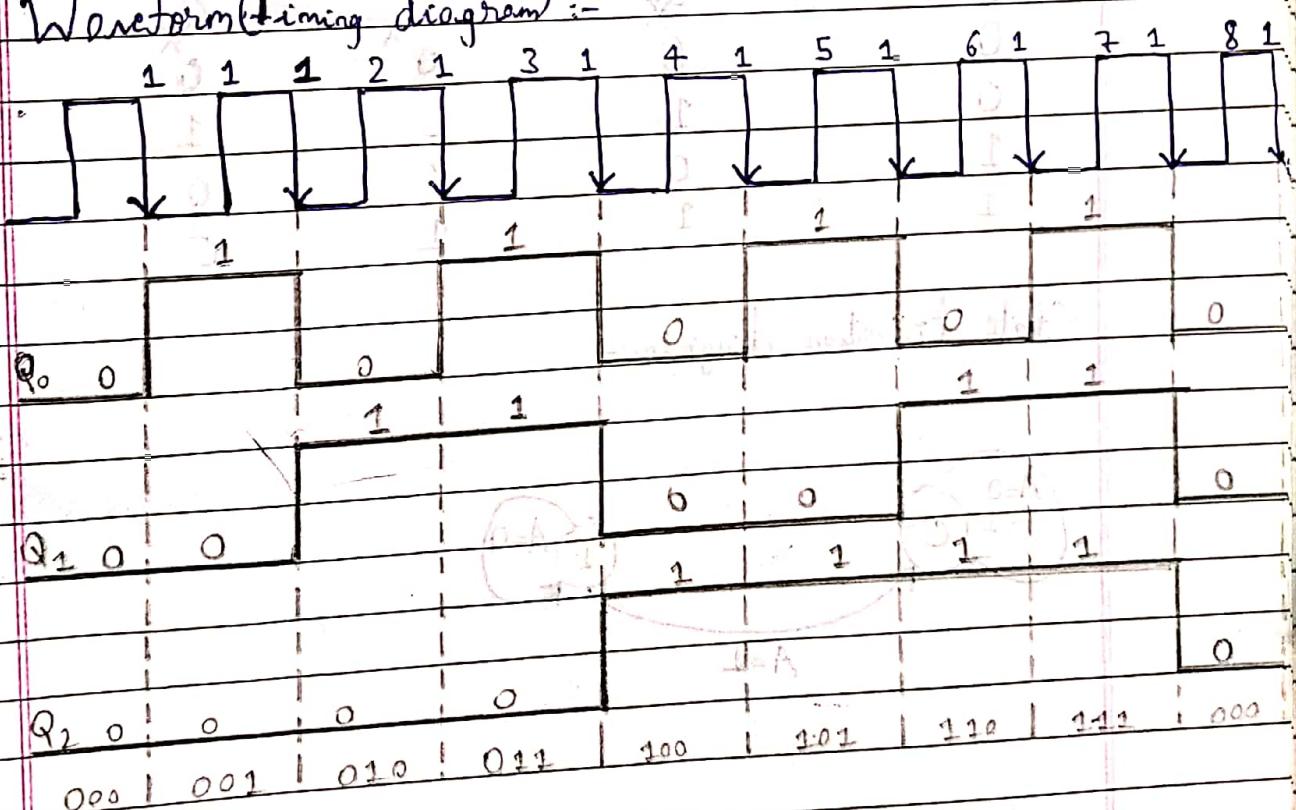


## Waveforms (Timing Diagram) :-

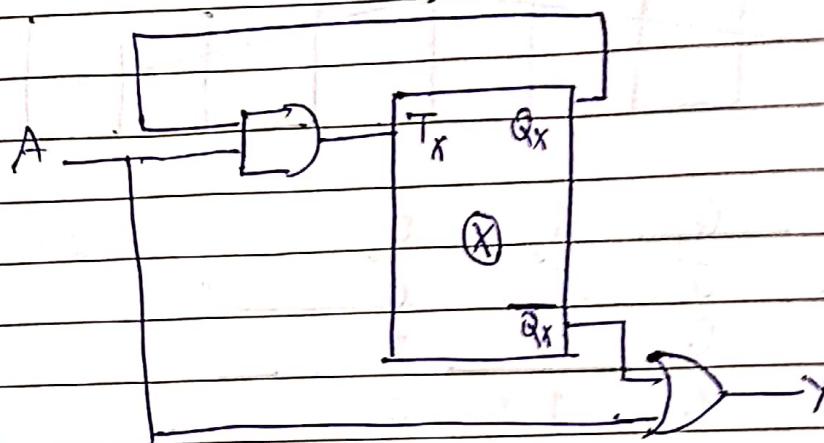


CLR	CLK	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	X	0	0	0
1	1	0	0	1
1	2	0	1	0
1	3	0	1	1
1	4	1	0	0
1	5	1	0	1
1	6	1	1	0
1	7	1	1	1
1	8	0	0	0

## \* Waveform (Timing diagram) :-



\* Analyze given sequential circuit & draw state transition diagram.



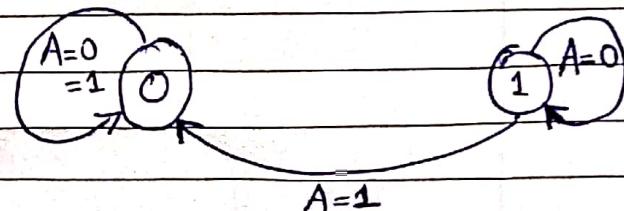
$\rightarrow$  I/P: O/P:

$$T_X = A \cdot Q_X \quad \text{&} \quad Y = \overline{Q_X} + A$$

State table:-

External input	Present state	f/f inputs	Next state	External output
A	$Q_X$	$T_X$	$Q_X^+$	Y
0	0	0	0	1
0	1	0	1	0
1	0	0	0	1
1	1	1	0	1

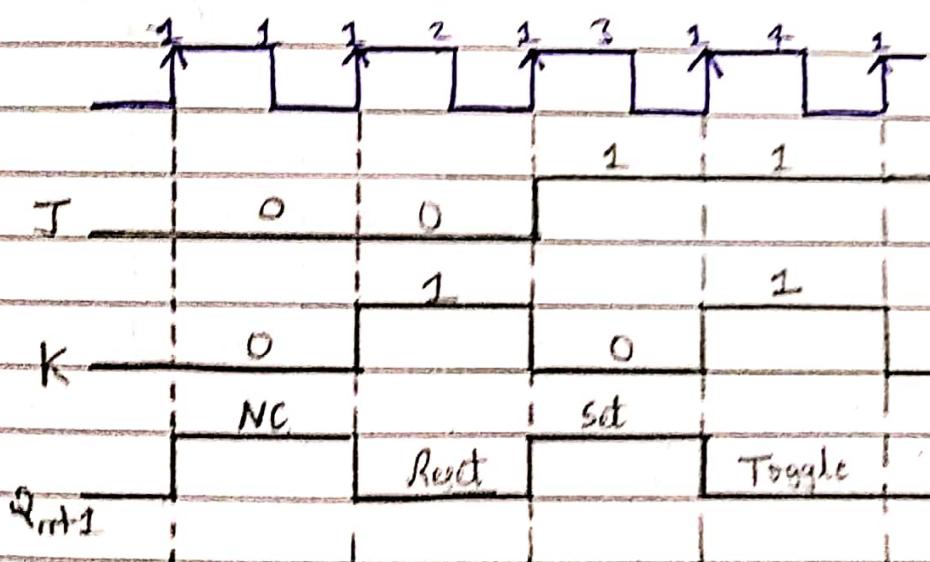
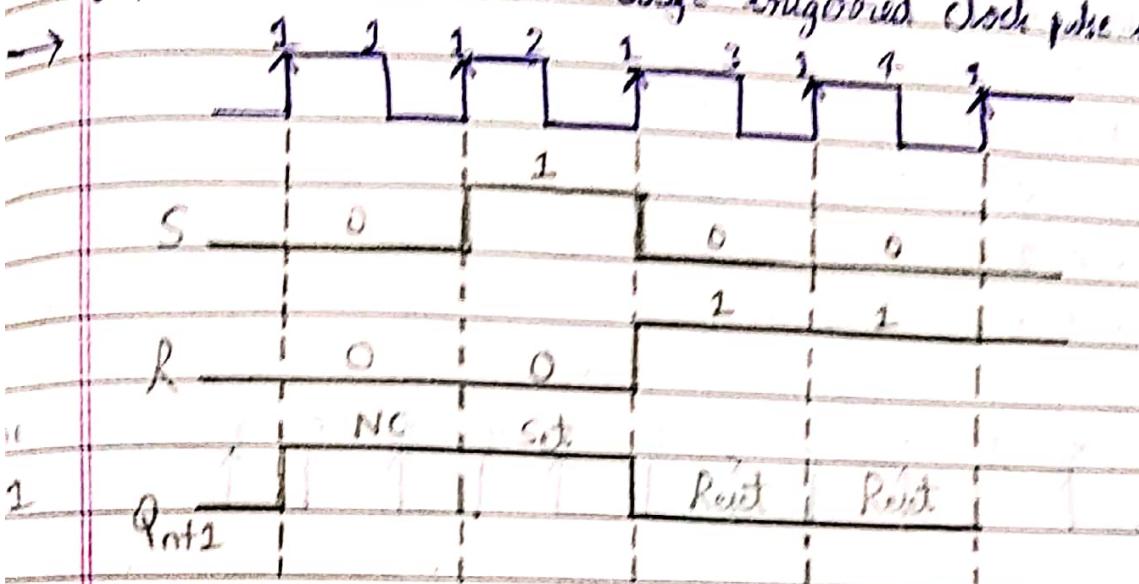
State transition diagram:-



Topic 15.10.19

\* Draw timing diagrams for JK, SR, T & D flip-flops.

Assume that Positive edge triggered clock pulse is used.





Waveform for ring counter:-

$Q_3 \ Q_2 \ Q_1 \ Q_0$

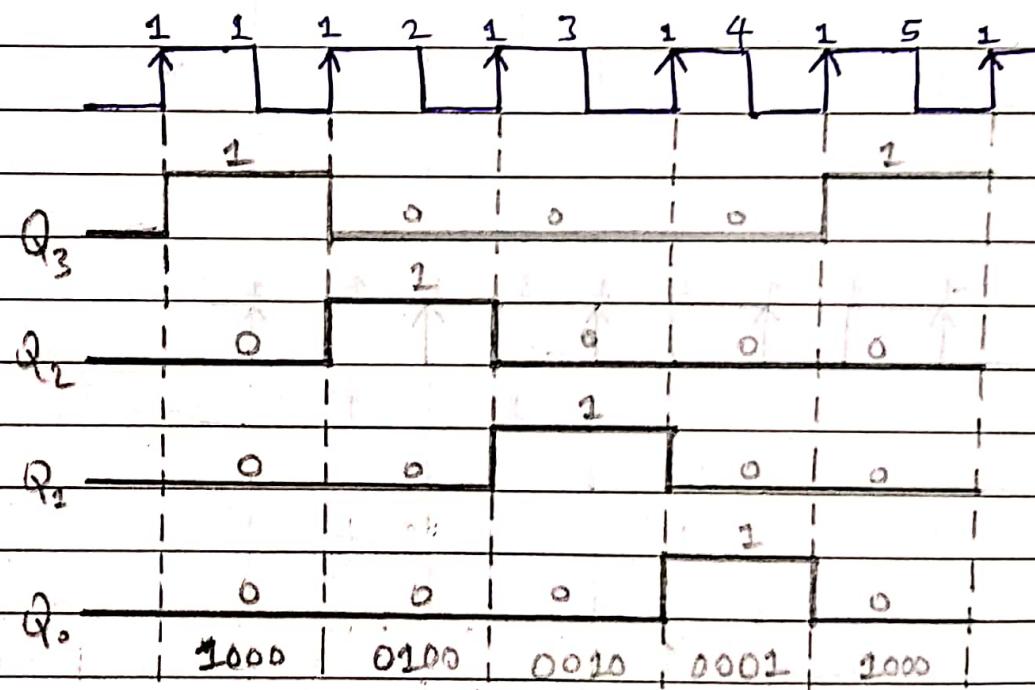
1. 1 0 0 0

2. 0 1 0 0

3. 0 0 1 0

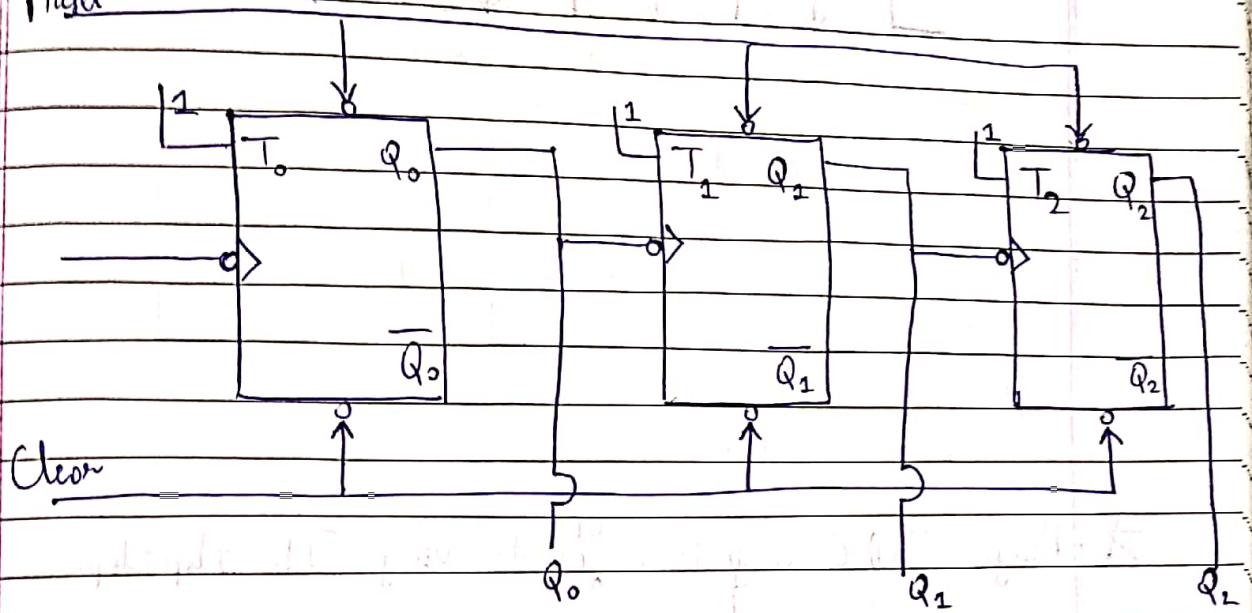
4. 0 0 0 1

5. 1 0 0 0



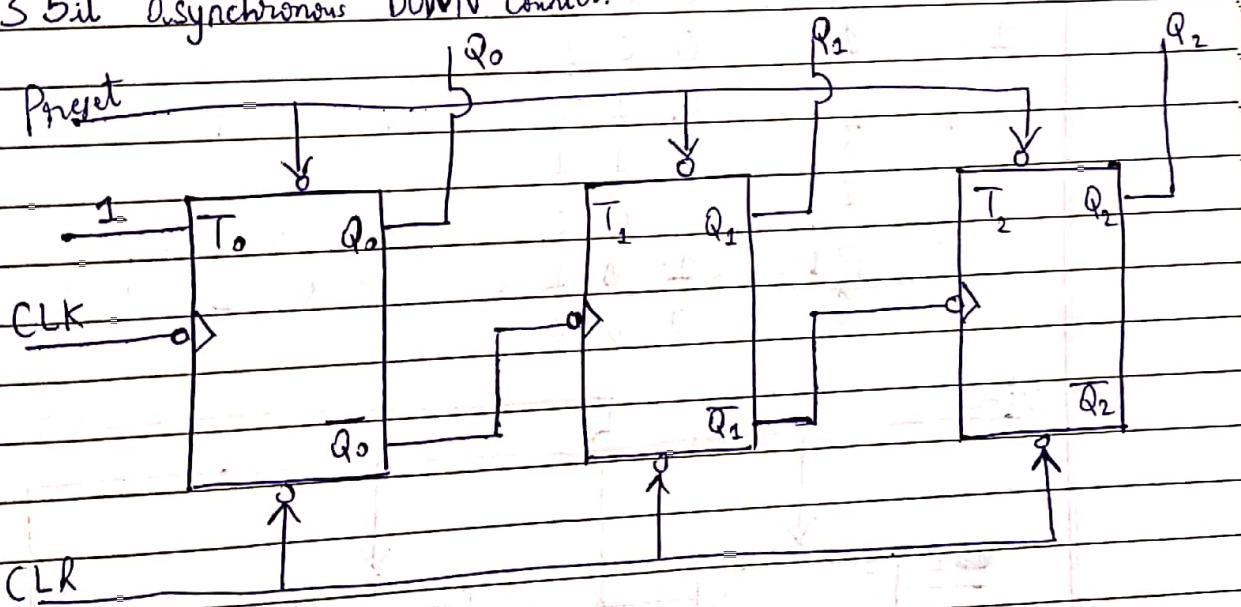
**★ 3-bit asynchronous UP Counter (repeated):-**

Pre-set



**★ 3 bit asynchronous DOWN counter:-**

Pre-set



CLR	CLK	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	X	0	0	0
1	1	1	1	1
2		1	1	0
3		1	0	1
4		1	0	0
5		0	1	1
6		0	1	0
7		0	0	1
8		0	0	0

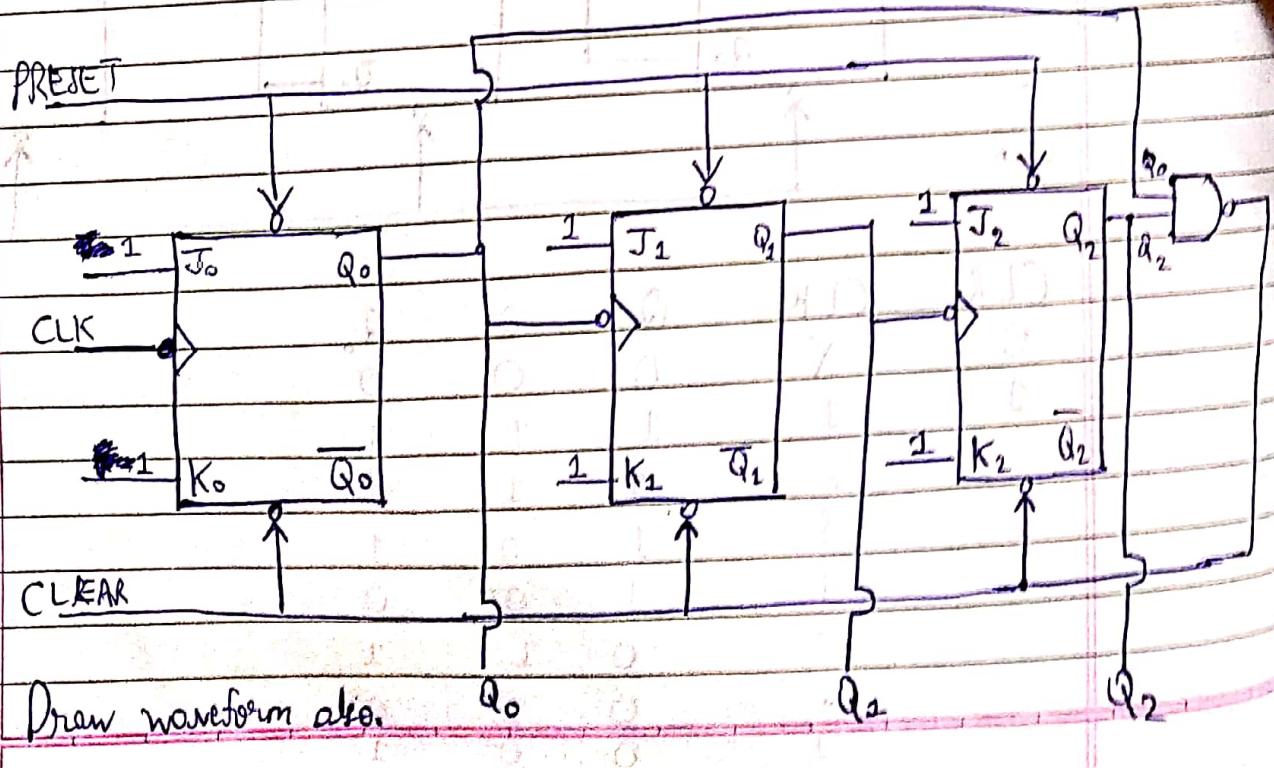
MOD  $\Rightarrow$  UP counting

Good Luck Page No. 80  
Date 22/10/19

	1	2	3	4	5	6	7
CLK	1	1	1	1	1	1	1
$Q_2$ (MSB)	0	1	1	0	1	0	0
$Q_1$	0	1	1	0	1	1	1
$Q_0$ (LSD)	0	0	1	0	1	0	1
(Count)	000	111	110	101	100	011	010

★ Design MOD 6 up synchronous counter using JK flipflop:-

CLR	CLK	$Q_2$	$Q_1$	$Q_0$
0	X	0	0	0
1	1	0	0	1
2		0	1	0
3		0	1	1
4		1	0	0
5		1	0	1
6		0	0	0



**★ MOD 5** asynchronous UP counter using JK flip flop:-

Sheet No. 81  
Date 24-10-29

	CLR	CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	X	0	0	0	0
1	1	1	0	0	1	
2			0	1	0	
3			0	1	1	
4			1	0	0	
5			0	0	0	
1000						

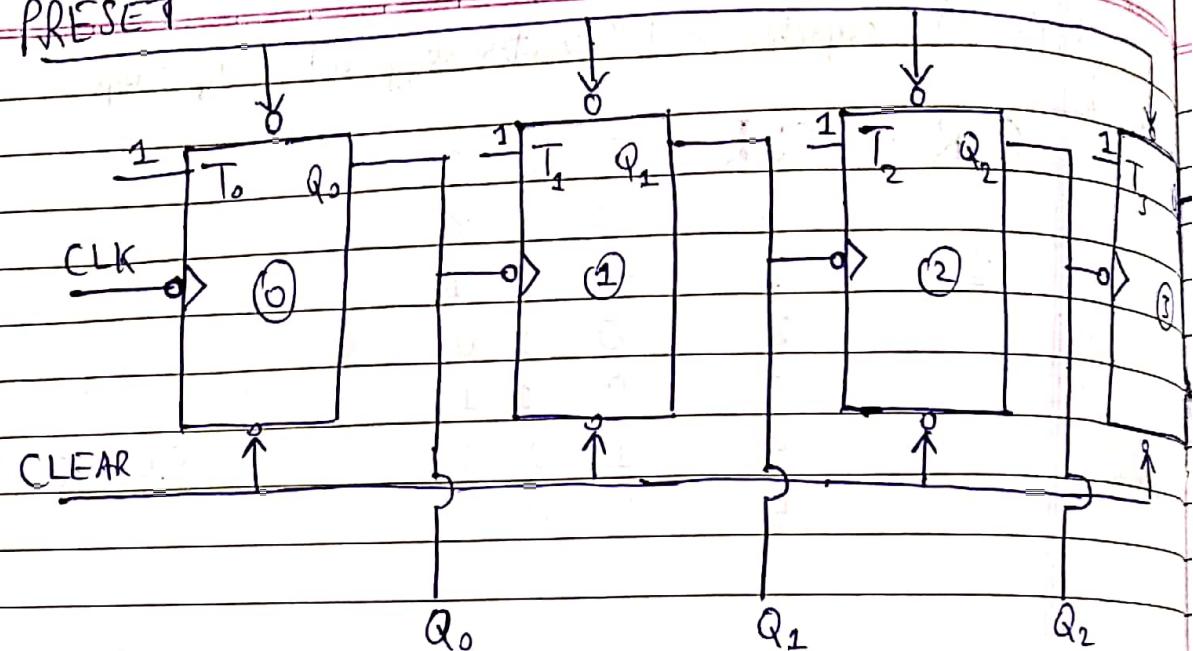
Sols.  $Q_2 = \boxed{\square} Q_0 = \boxed{\square}$

**★ MOD 16** asynchronous counter (4-bit asynchronous UP counter):-

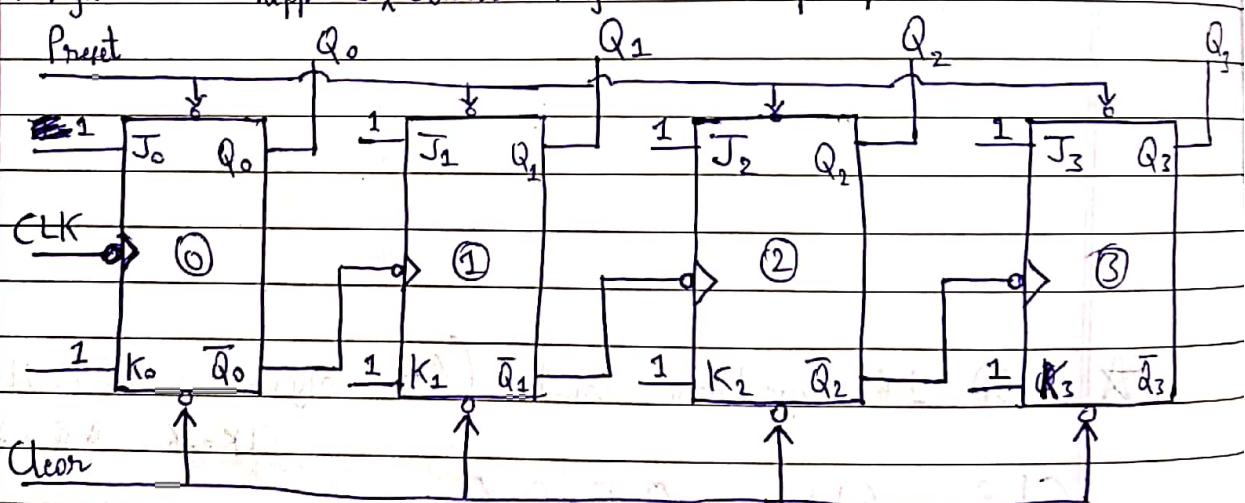
$CLK = 16, Q_3 Q_2 Q_1 Q_0 = 0000$

	CLR	CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	X	0	0	0	0
1	1	1	0	0	0	1
2			0	0	1	0
3			0	0	1	1
4			0	1	0	0
5			0	1	0	1
6			0	1	1	0
7			0	1	1	1
8			1	0	0	0
9			1	0	0	1
10			1	0	1	0
11			1	0	1	1
12			1	1	0	0
13			1	1	0	1
14			1	1	1	0

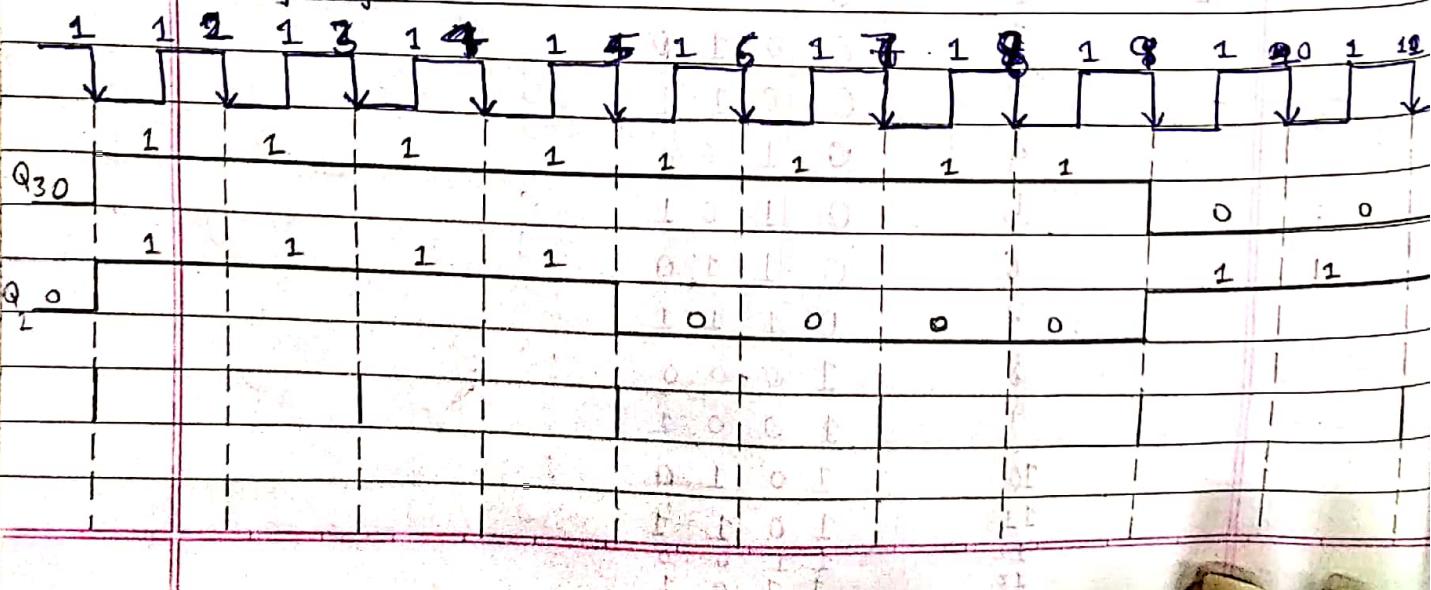
### PRESET



★ Design 4 bit Ripple  $D\overline{D}_X^{WN}$  Counter using JK flipflop:-

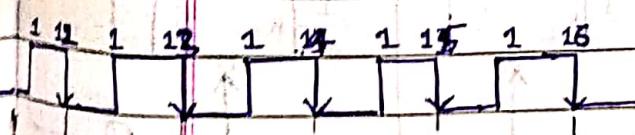


Timing diagram:-



### Truth Table:-

CLR	CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	X	0	0	0	0
1	1	1	1	1	1
2		1	1	1	0
3		1	1	0	1
4		1	1	0	0
5		1	0	1	1
6		1	0	1	0
7		1	0	0	1
8		1	0	0	0
9		0	1	1	1
10		0	1	1	0
11		0	1	0	1
12		0	1	0	0
13		0	0	1	1
14		0	0	1	0
15		0	0	0	1
16		0	0	0	0



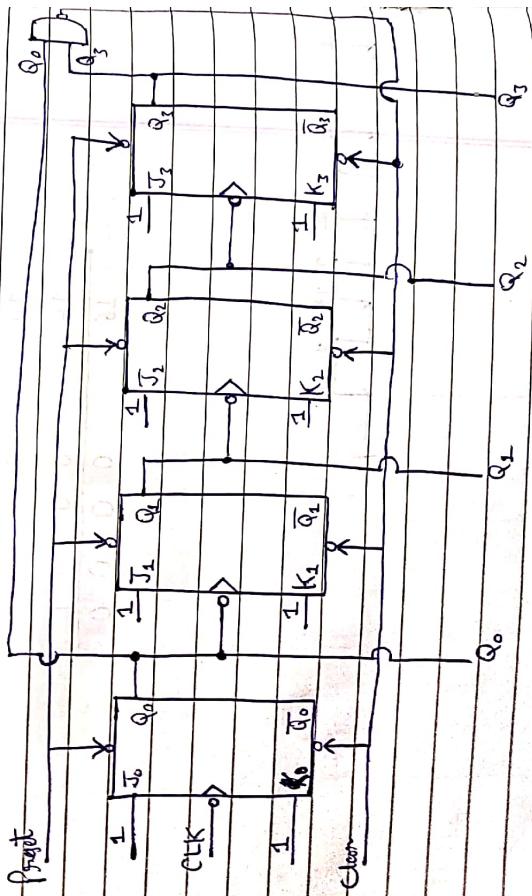
0	0	0	0	0
1	1	0	0	0

**A** Design Mod 10 Counter using JK flipflop:-

Truth Table:-

	CLR	CLK	$Q_3 Q_2 Q_1 Q_0$
0	X		0 0 0 0
1	1	0	0 0 0 1
2	2	0	0 0 1 0
3	3	0	0 0 1 1
4	4	0	1 0 0 0
5	5	0	1 0 0 1
6	6	0	1 1 0 0
7	7	0	1 1 1 0
8	8	1	0 0 0 0
9	9	1	0 0 0 1
10	10	1	0 0 0 0

Logic diagram:-  
Project



### \* Synchronous Counter:-

\* Design 2-bit Synchronous UP counter using JK flip-flops.

Truth Table:-

CLK	Present state	Next state	Flip-flop inputs
0	Q <sub>1</sub> Q <sub>0</sub>	Q <sub>1</sub> ' Q <sub>0</sub>	J <sub>1</sub> K <sub>1</sub> J <sub>0</sub> K <sub>0</sub>
1	0 0	0 1	0 X 1 X
2	0 1	1 0	1 X X 1
3	1 1	0 0	X 0 1 X

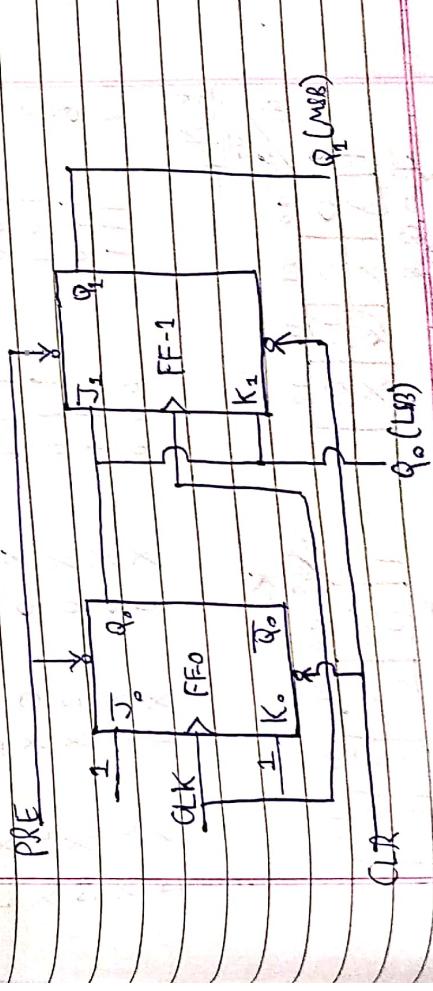
K-Map:-

J <sub>1</sub> :		K <sub>1</sub> :		J <sub>0</sub> :		K <sub>0</sub> :	
Q <sub>1</sub>	Q <sub>0</sub>						
0	0	0	0	0	0	0	0
1	X	X	X	1	0	1	X

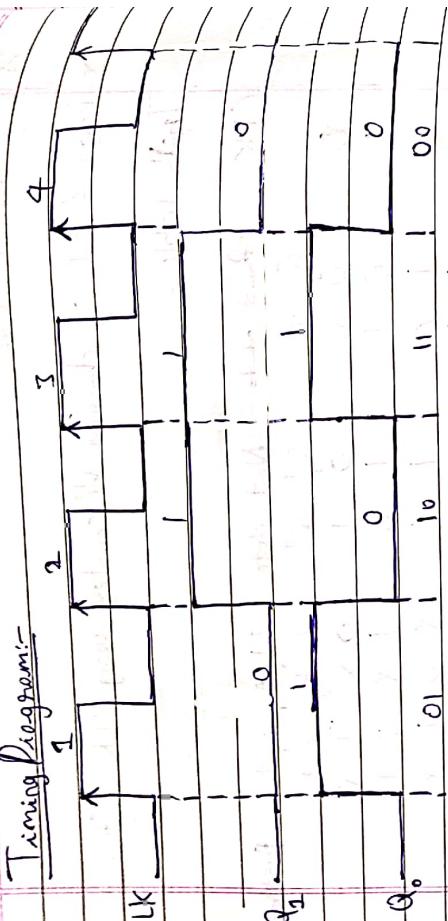
$\therefore \overline{J_1} = Q_0$        $K_1 = Q_0$

$J_0 = 1$

Block diagram:-



### Timing Diagram:



\* Design 3 bit Synchronous Up Counter Using JK flip-flops:-

J T :-

CLK	Present State	Next State	F/F input
(Initial)	Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	Q <sub>2</sub> <sup>+</sup> Q <sub>1</sub> <sup>+</sup> Q <sub>0</sub> <sup>+</sup>	J <sub>2</sub> K <sub>2</sub> , J <sub>1</sub> K <sub>1</sub> , J <sub>0</sub> K <sub>0</sub>
1	0 0 0	0 0 1	X X 0 X 1 X
2	0 1 0	0 1 1	0 X X 0 X 1 X
3	0 1 1	1 0 0	1 X X 1 X 1 X
4	1 0 0	1 0 1	X 0 0 X -1 X
5	1 0 1	1 1 0	X 0 1 X 1 X
6	1 1 0	1 1 1	X 0 X 0 -1 X
7	1 1 1	0 0 0	X 1 X 1 X 1

K-Map:-

J <sub>2</sub> :		K <sub>2</sub> :	
Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>2</sub> Q <sub>1</sub> 0 1	Q <sub>2</sub> Q <sub>1</sub> 0 0 1 0
0	0	0 0	0 0 0 1
1	X	X 0	X 0 X 1

$$\overline{J_2} = Q_1 Q_0$$

$$J_2 = Q_1 \bar{Q}_0$$

3 input 8 output  
 $J_1, J_2, Q_1, Q_2, K_1, K_2$

$J_1:$

$Q_1$	$Q_2$	00	01	11	10
0	0	X	X	X	0
1	0	X	X	X	1

$\bar{J}_1 = Q_0$

$J_2:$

$Q_1$	$Q_2$	00	01	11	10
0	0	X	X	X	0
1	1	X	X	X	1

$\bar{J}_2 = 1$

$K_1:$

$Q_1$	$Q_2$	00	01	11	10
0	0	X	X	X	0
1	0	X	X	X	1

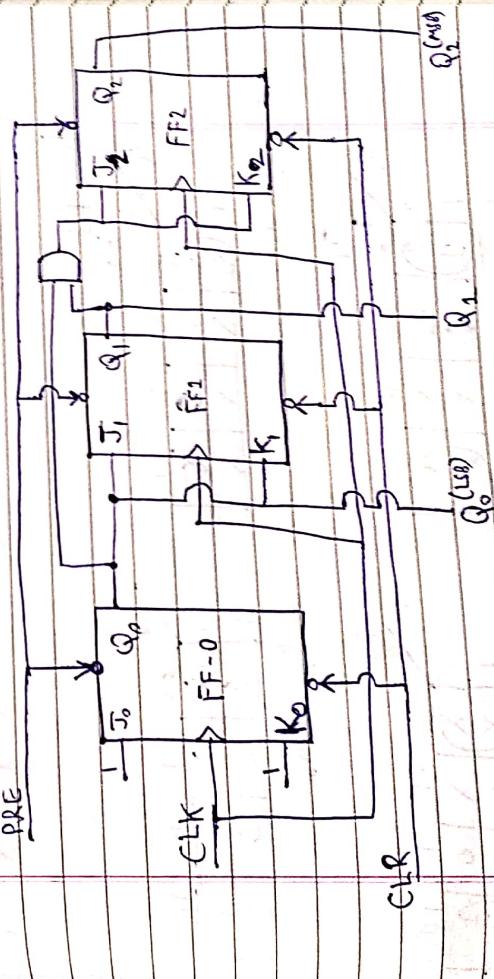
$K_1 = Q_0$

$K_2:$

$Q_1$	$Q_2$	00	01	11	10
0	0	X	X	X	0
1	1	X	X	X	1

$K_2 = 1$

Block Diagram:-



### \* Design 3bit Synchronous Down Counter Using JK flip-flops

<u>CLK</u>	<u>Present State</u>	<u>Next State</u>	<u>E/F Inputs</u>
0	Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	Q <sub>2</sub> <sup>+</sup> Q <sub>1</sub> <sup>+</sup> Q <sub>0</sub> <sup>+</sup>	J <sub>2</sub> K <sub>2</sub> J <sub>1</sub> K <sub>1</sub>
1	1 0 0	1 1 0	1 X 2 X 1 X
2	X 1 0	0 1 0	X 0 X 0
3	1 0 1	1 0 0	X 0 X 1
4	1 0 0	0 1 1	X 1 1 X
5	0 1 1	0 1 0	0 X X 0
6	0 1 0	0 0 1	0 X X <sub>2</sub> 1 X
7	0 0 1	0 0 0	0 X 0 X X <sub>2</sub>

<u>K-Map:</u>		<u>J<sub>2</sub>:</u>		<u>K<sub>2</sub>:</u>		<u>J<sub>1</sub>:</u>		<u>K<sub>1</sub>:</u>	
Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	0 0 0	0 1	1 0	0 0	0 1	1 1	1 0	Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	0 0 0
0	0	(1) 0	0	0	(X)	X	X	0	0 1
1	1	(X) X	X	1	(1) 0	0	0	1	1 0

$J_2 = \overline{Q}_2 \overline{Q}_0$

$K_2 = \overline{Q}_2 \overline{Q}_0$

$J_1 = Q_0$

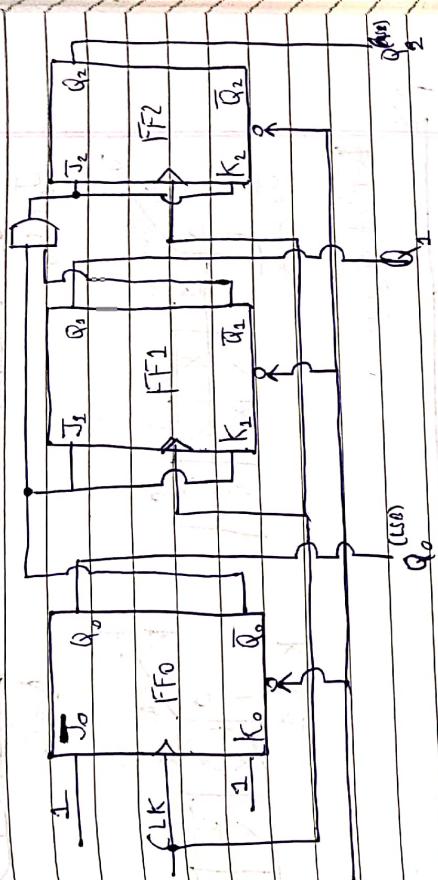
$K_1 = \overline{Q}_0$

<u>K<sub>0</sub>:</u>	
Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	0 0 0
0	(1) 0
1	(1) X

$J_0 = 1$

$Q \rightarrow Q'$   
 $J_0 = 0, K_0 = 0$   
 $J_1 = 0, K_1 = 0$   
 $J_2 = 0, K_2 = 0$

Block diagram:-



\* Design Mod-5 Synchronous counter (by JK f/f's):-

L.L:-

CLK	Present State	Next State	F/F input
0	Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	Q <sub>2</sub> ' Q <sub>1</sub> ' Q <sub>0</sub>	J <sub>2</sub> K <sub>2</sub>
1	0 0 1	0 1 0	J <sub>1</sub> K <sub>1</sub>
2	0 1 0	0 0 1	J <sub>0</sub> K <sub>0</sub>
3	0 1 1	X 1 X	
4	0 0 0	X 1 0	

L.L:-

Q0  
Q1  
Q2  
Q3

State  
S = 111 + 110

		Q <sub>1</sub> Q <sub>0</sub>	00	01	10	11	10
		Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	000	001	010	011	110
J <sub>1</sub>	J <sub>0</sub>	0	0	X	X	X	0
		1	0	X	X	X	X

$$J_1 = Q_0$$

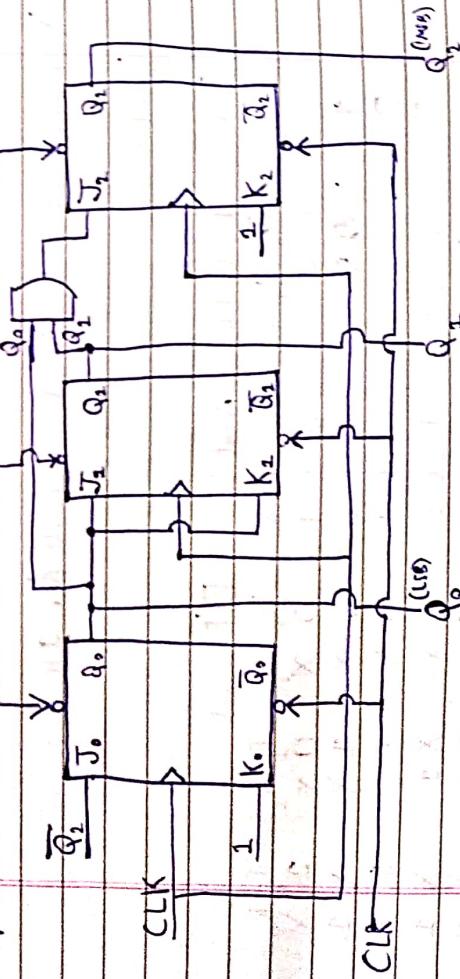
		Q <sub>1</sub> Q <sub>0</sub>	00	01	10	11	10
		Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	000	001	010	011	110
J <sub>0</sub>	K <sub>0</sub>	0	0	X	X	X	0
		1	0	X	X	X	X

$$J_0 = \overline{Q}_2$$

$$K_0 = 1$$

Block diagram:

PRE



\* Design 3-bit Synchronous Up Counter using SR flip-flops.

CLK	Present State	Next State	S/F inputs
	$Q_2 Q_1 Q_0$	$Q_2^+ Q_1^+ Q_0^+$	
0 (clr)	0 0 0	0 0 1	$S_2 R_2$
1	0 0 1	0 1 0	$Q_2 X$
2	0 1 0	0 1 1	$Q_2 X$
3	0 1 1	1 0 0	$X 0$
4	1 0 0	1 0 1	$X 0$
5	1 0 1	1 1 0	$X 0$
6	1 1 0	1 1 1	$X 0$
7	1 1 1	0 0 0	$X 0$

K-Map:-

$S_2$ :		$R_2$ :	
$Q_2$	$Q_1 Q_0$	$Q_2$	$Q_1 Q_0$
0	0 0	0 0	0 0
1	X X	0 1	1 1
		X 0	0 X

$$S_2 = \overline{Q}_2 Q_1 Q_0$$

$$R_2 = Q_2 Q_1 Q_0$$

$S_1$ :		$R_1$ :	
$Q_2$	$Q_1 Q_0$	$Q_2$	$Q_1 Q_0$
0	0 0	0 0	0 0
1	0 1	0 1	1 1
	X 0	X 0	0 X

$$S_1 = \overline{Q}_1 Q_0$$

$$R_1 = Q_1 Q_0$$

$S_0$ :		$R_0$ :	
$Q_2$	$Q_1 Q_0$	$Q_2$	$Q_1 Q_0$
0	0 0	0 0	0 0
1	0 1	0 1	1 1
	X 0	X 0	0 X

$$S_0 = \overline{Q}_0$$

$$R_0 = Q_0$$

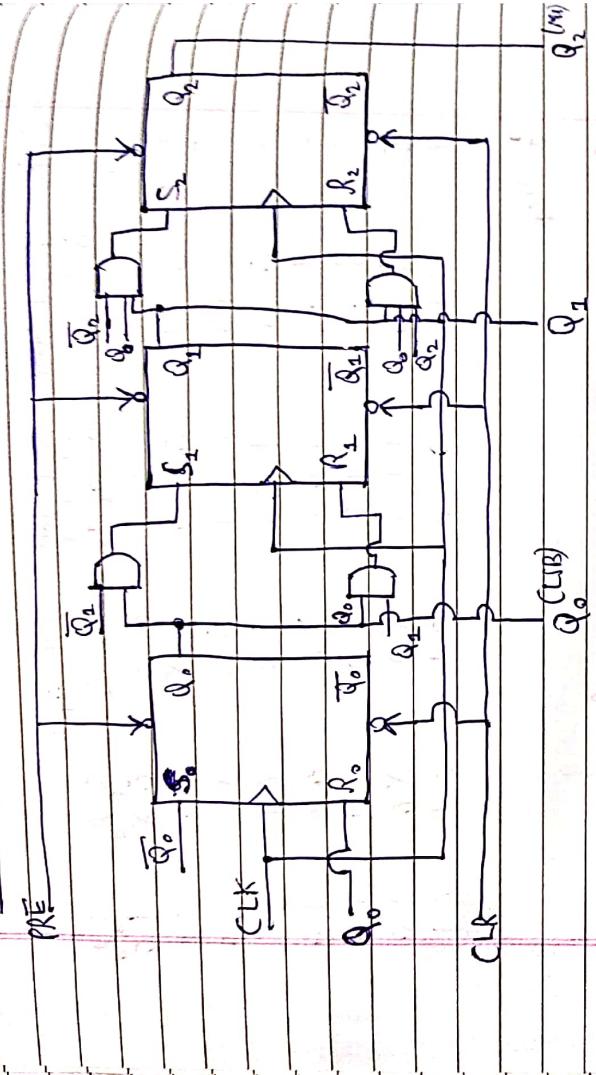
M<sub>11</sub>L

Goodluck  
Date 5/11/29

Page No. 92

For Counter, draw state transition diagram :-

Block Diagram:-



Waveform:-



Q<sub>n</sub> → Q<sub>n+1</sub>      T  
 0      0      0  
 0      1      1  
 1      0      0  
 1      1      1

Design a Counter generate following pattern 000, 010, 100, 110  
 using T flip-flops.

→ Truth Table:-

CLK	Present State	Next State	E/F Input
(Clear)	Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	Q <sub>2</sub> ' Q <sub>1</sub> ' Q <sub>0</sub> '	T <sub>2</sub> T <sub>1</sub> T <sub>0</sub>
0	0 0 0	0 1 0	0 1 0
1	0 1 0	0 0 0	1 1 0
2	1 0 0	1 1 0	0 1 0
3	1 1 0	0 0 0	1 0 0

K-Map:-

T <sub>2</sub>	Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	00	01	11	10
0	0 0 0	X	X	X	0
1	0 0 1	X	X	X	0

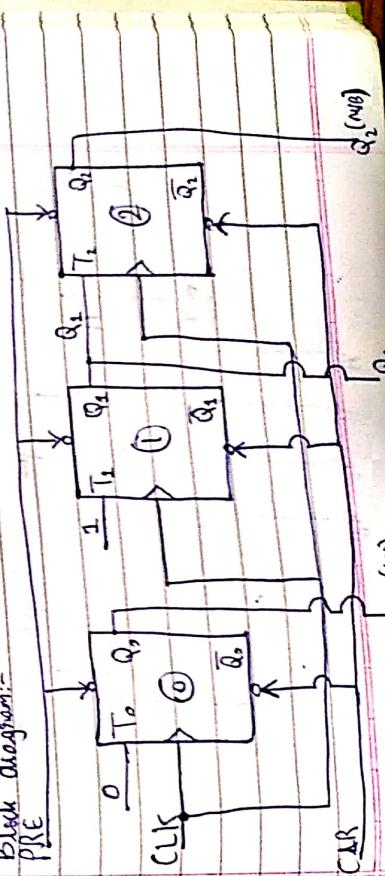
$$T_2 = \underline{\underline{Q_2}}$$

$$T_0 :$$

T <sub>2</sub> T <sub>1</sub>	Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub>	00	01	11	10
0 0	0 0 0	X	X	X	0
1 0	0 0 1	X	X	X	0

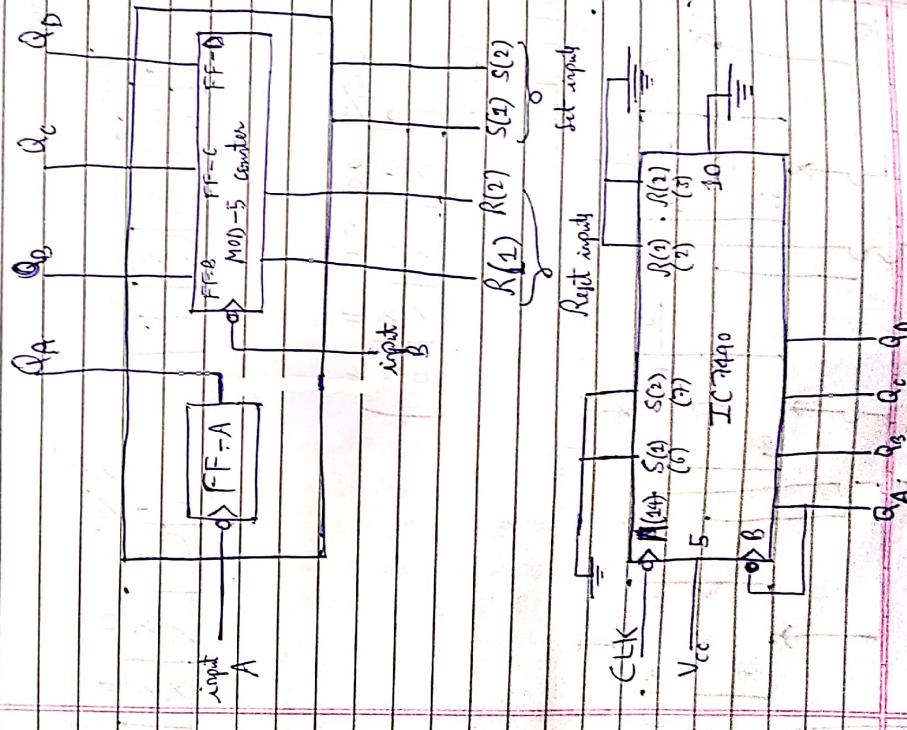
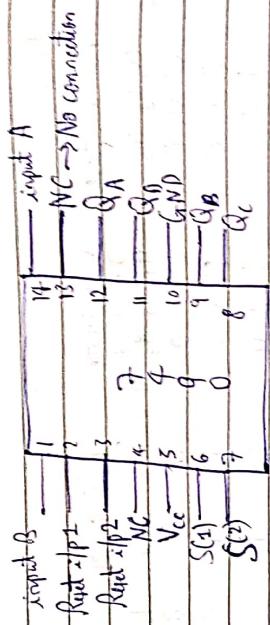
$$T_0 = \underline{\underline{Q_2}}$$

Block diagram:-



Good luck  
Lau 7/11/29

$\star$  IC 7490 (Decade Counter):-



## Unit V : VHDL, ADC & Introduction To HOL

\* Introduction To HOL (Hardware Description Language):-

\* Describing I/O in VHDL:-



module testkit(a,b,c,x,y); // module name with port list

input a,b,c;

output x,y;

// module body begins next describing logic relation

// module body ends  
endmodule

\* Implementation Model in HOL :-

- Data flow

- Behavioural.

\* Operators:-

i) Relational: <, <=, >, >=

ii) Logical: !, &&, ||

iii) Bitwise: ~, &, |

iv) Arithmetic: +, -, \*, /

\* Example:-

i) Develop a Verilog code for a simple SOP eq. i) given below:

```

Y = AB + CD
module SOP(A,B,C,D,Y);
    input A,B,C,D;
    output Y;
begin
    Y = ((A&B) | (C&D));
endmodule

```

ii) Develop a Verilog code to implement 4-to-1 MUX using data flow modeling.

```

module 4to1MUX(A,B,D0,D1,D2,D3);
    input A,B,D0,D1,D2,D3;
    output Y;
begin
    Y = (A&B&D0) | (~A&B&D1) | (~A&B&D2) | (A&B&D3);
endmodule

```

```
// assign Y = A ? [B ? (D3:D2) : (B ? (D1:D0))];
```

iii) Develop Verilog code to implement 3-to-8 line decoder using data flow modeling. Assume active high enable pin.

```

module 3to8decoder(output [0:7] Y, input A,B,C,enable);
    output [7:0] Y[0] = (~A & ~B & ~C & enable),
                Y[1] = (~A & ~B & C & enable),
                Y[2] = (~A & B & ~C & enable),
                Y[3] = (~A & B & C & enable),
                Y[4] = (A & ~B & ~C & enable),
                Y[5] = (A & ~B & C & enable),
                Y[6] = (A & B & ~C & enable),
                Y[7] = (A & B & C & enable);
endmodule

```

Good Luck Page No. 97

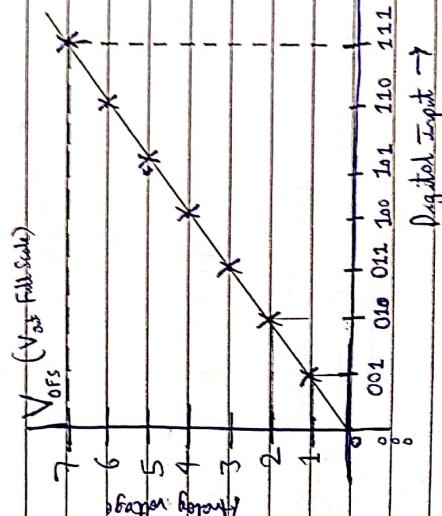
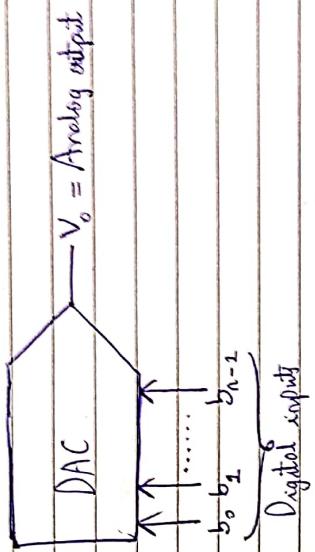
Date 11 11 19

iv) Develop Verilog code for 1-bit full adder.

**★ ADC & DAC :-**



**★ DAC :-**



$$\text{Step size} = 1V$$

**★ Performance parameters of DAC :-**

- i) Resolution.
- ii) Accuracy.

i) Resolution - It is the number of diff. analog output values that can be provided by a DAC. It is given by the eqn:

$$\text{Resolution} = \frac{1}{2^n}$$

$$\text{Resolution} \text{ is given by } = \frac{V_{\text{FS}}}{2^n-1}, \text{ Resolution} = \frac{V_{\text{FS}}}{2^n-1}$$

Resolution is also defined as the ratio of the change in output voltage resulting from a change of 1 LSB of the digital inputs. For an n-bit DAC, resolution is expressed as Resolution =  $\frac{V_{\text{FS}}}{2^n-1}$

- ii) Accuracy - It is a comparison of actual output voltage with expected output. It is expressed in %age. Accuracy =  $(V_{\text{out}} / V_{\text{FS}}) \times (1/2)$
- Note: Ideally, the accuracy of DAC should be at worst  $\pm \frac{1}{2}$  of LSB.

★ Problem:-

8 bit DAC in 2 ways. Assume  $V_{\text{FS}} = 10.2 \text{ V}$

$$1) \text{ Determine Resolution of } \xrightarrow{n=8} \text{ DAC in } 2 \text{ ways.}$$

$$\rightarrow \Delta = \delta, V_{\text{FS}} = 10.2 \text{ V}$$

$$1) \text{ Resolution} = \frac{1}{2^n} = \frac{1}{2^8} = \frac{1}{256}$$

$$2) \text{ Resolution} = \frac{V_{\text{FS}}}{2^n-1} = \frac{10.2 \text{ V}}{2^8-1} = \frac{10.2 \text{ V}}{255} = \underline{\underline{0.04 \text{ V}}} = \underline{\underline{40 \text{ mV}}}$$

$$2) \text{ Determine the accuracy of } 8 \text{ bit DAC assuming } V_{\text{FS}} = 10.2 \text{ V.}$$

$$\rightarrow \text{Accuracy} = \frac{V_{\text{FS}}}{2^n-1} \times \frac{1}{2} = \frac{10.2 \text{ V}}{2^8-1} \times \frac{1}{2} = \frac{4.0 \text{ mV}}{2} = \underline{\underline{20 \text{ mV}}}$$

P.T.O.

3) An 8-bit DAC has an O/P voltage range of 0-2.55V. Define its resolution in 2 ways.

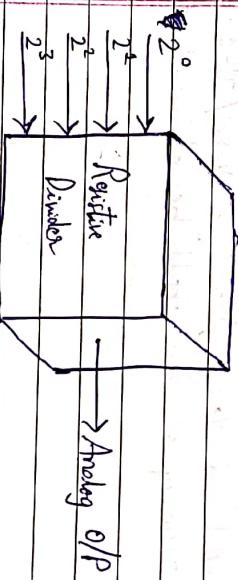
$$\rightarrow V_{O_{ES}} = 2.55V, N=8$$

$$i) \text{Resolution} = \frac{1}{2^8} = \frac{1}{256}$$

$$ii) \text{Resolution} = \frac{V_{O_E}}{2^{N-1}} = \frac{2.55V}{2^8-1} = \frac{2.55}{255} = \underline{\underline{10mV}}$$

### ★ Types of DAC:-

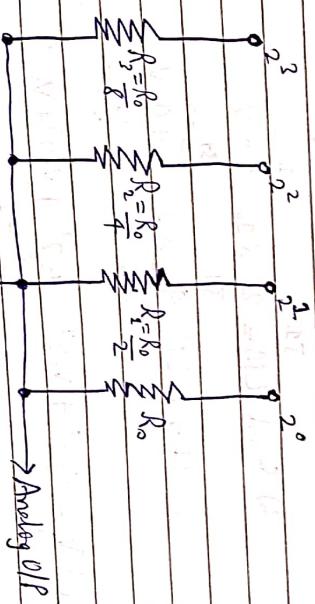
#### 1) Resistive Divider Type:-



Bit	Weight (Assuming $V_{O_E} = +1.5V$ )
0	$2^0/15 = 1/15$
1	$2^1/15 = 2/15$
2	$2^2/15 = 4/15$
3	$2^3/15 = 8/15$

Digital I/P      Analog O/P voltage

0 0 0 0	+1V
0 0 1 0	+2V
0 0 1 1	+3V
0 1 0 0	+4V
0 1 0 1	+5V
0 1 1 0	+6V
0 1 1 1	+7V
1 0 0 0	+8V
1 0 0 1	+9V
1 0 1 0	+10V
1 0 1 1	+11V
1 1 0 0	+12V
1 1 0 1	+13V
1 1 1 0	+14V
1 1 1 1	+15V



$$N_A = \frac{V_o 2^0 + V_1 2^1 + V_2 2^2 + \dots + V_{n-1} 2^{n-2}}{2^{n-1}}$$

Drawback - MSB bit has to handle large no. of word  
It's not possible to get accurate result

Date 16/11/19  
Page No. 19

### ★ Problem:-

1) For a 5-bit negative number type DAC, determine the following.

i) Weight assigned to the LSB.

ii) " " " " Second & third LSB.

iii) Change in O/P voltage due to change in the LSB, the second LSB & the third LSB.

iv) O/P voltage for a digital I/P of 10101.

Assume  $V_{oE}$  = 10V.

$$\rightarrow \text{ii) LSB bit weight} = \frac{2^0}{2^{n-1}} = \frac{1}{2^{5-1}} = \frac{1}{32} \text{ V}$$

$$\text{i) Second LSB weightage} = \frac{2^1}{2^{n-1}} = \frac{2}{2^{5-1}} = \frac{2}{32} \text{ V}$$

$$\text{iii) Third LSB weightage} = \frac{2^2}{2^{n-1}} = \frac{4}{2^{5-1}} = \frac{4}{32} \text{ V}$$

iv) Change in O/P voltage due to change in:

$$\text{a) LSB} = \frac{1}{32} \times 10 \text{ V} = \frac{10}{32} \text{ V}$$

$$\text{b) Second LSB} = \frac{2}{32} \times 10 = \frac{20}{32} \text{ V}$$

$$\text{c) Third LSB} = \frac{4}{32} \times 10 = \frac{40}{32} \text{ V}$$

$$\text{iv) } V_A = V_o 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + V_4 2^4 \quad (10101-\text{IP})$$

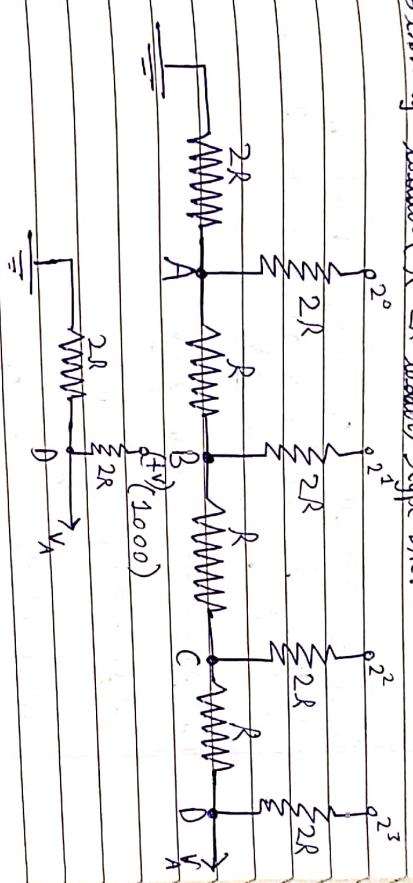
$$= \frac{10}{32} + \frac{40}{32} + \frac{160}{32} \text{ V}$$

$$= \frac{210}{32} \text{ V}$$

(When i/p bit is 1, multiply  $V_{oE}$  with  $2^{n-1}$  terms of multiplying factor.)

$$Ex: 10101 \Rightarrow \underline{10} \times 2^0 + \underline{0} \times 2^1 + \underline{10} \times 2^2 + \underline{0} \times 2^3 + \underline{10} \times 2^4$$

Binary ladder ( $R-2R$  ladder) type DAC:-



$$V_A = V \times \frac{2R}{2R+2R} = \frac{V}{2}$$

for (0100)

$$\begin{array}{c} 2R \\ \parallel \\ 2R \\ \parallel \\ 2R \end{array} \rightarrow V_A = \frac{2R}{4R} \times \frac{V}{2} = \frac{V}{4}$$

Bit position      Binary weight      O/P voltage

1st MSB	$\frac{1}{2}$	$\frac{V}{2}$
2nd MSB	$\frac{1}{4}$	$\frac{\sqrt{V}}{4}$
3rd MSB	$\frac{1}{8}$	$\frac{\sqrt[4]{V}}{8}$
LSB	$\frac{1}{16}$	$\frac{\sqrt[8]{V}}{16}$

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \dots + V_{n-1} 2^{n-1}}{2^n}$$

D.T.B.

## A Problem

1) What one O/P voltage Coupled by each bit in a 5 bit binary ladder if the input binary one  $D = 0V$ ,  $I = +10V$ ?  
 $\rightarrow$  Ans.  $M_{MSB} = \frac{1}{2} V = 5V$

(ii) Ans 2<sup>nd</sup> MSB =  $\frac{1}{4} V = 2.5V$

(iii) Ans 3<sup>rd</sup> MSB =  $\frac{1}{8} V = 1.25V$

(iv) Ans 4<sup>th</sup> MSB =  $\frac{1}{16} V = 0.625V$

v) Ans LSB =  $\frac{1}{32} V = 0.3125V$

2) Find the O/P voltage from a 5 bit ladder that has digital input of 11010. Assume  $0 = 0V$ ,  $1 = +10V$ .

$$\rightarrow V_A = \sqrt{2^0} + \sqrt{2^1} + \dots + \sqrt{2^4}$$

$$= \frac{0 \times 2^0 + 1 \times 2^1 + 0 \times 2^2 + 1 \times 2^3 + 1 \times 2^4}{2^5}$$

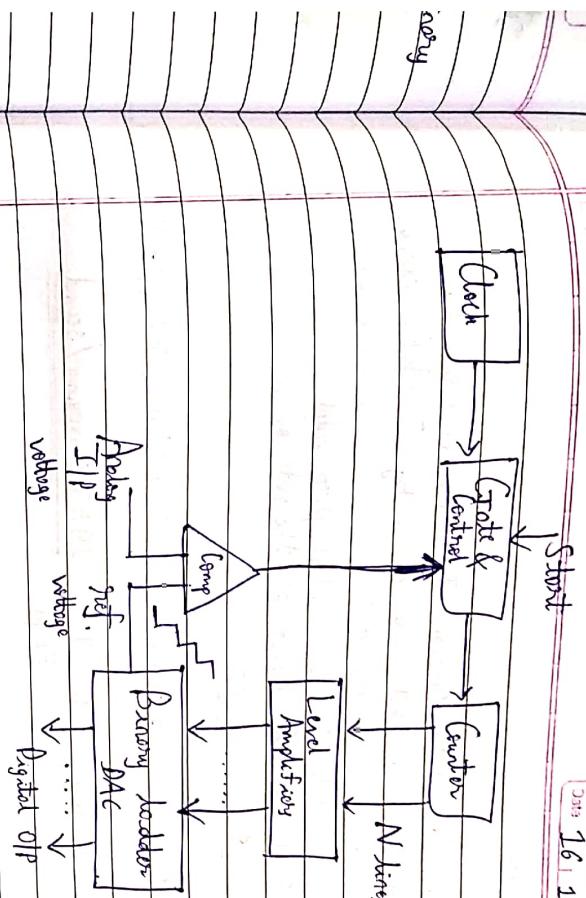
$$= \frac{20 + 80 + 160}{32}$$

$$= \frac{260}{32} V = 8.125V$$

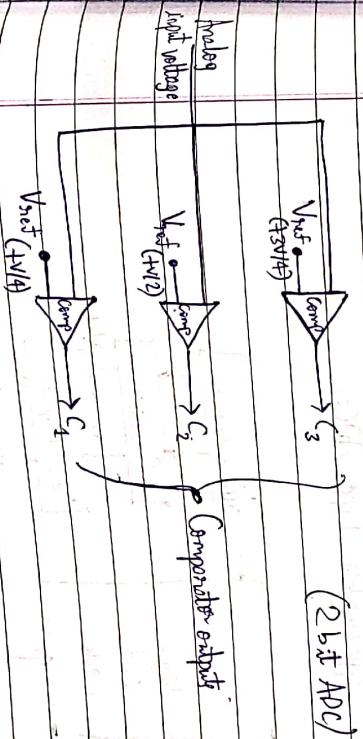
## ★ ADC Converters:-

1) Counter type ADC:-





Ques:- 2) Simultaneous Conversion Type ADC:— → Allie called parallel ADC.



Input voltage	Comparator C <sub>1</sub>	Comparator C <sub>2</sub>	Output
0 → +V/4	L	L	→ 00
+V/4 → +V/2	H	L	→ 01
+V/2 → +3V/4	H	H	→ 10
+3V/4 → +V	H	H	→ 11

## ★ Problem:-

1) Find the Max. conversion time, Avg. conversion time & max. conv. rate for an 8 bit ADC driven by 500kHz clock.

→ We have for 8 bit ADC:

Total  $2^8 = 256$  clock pulses needed.

i) 500Hz clock advance at the rate of:

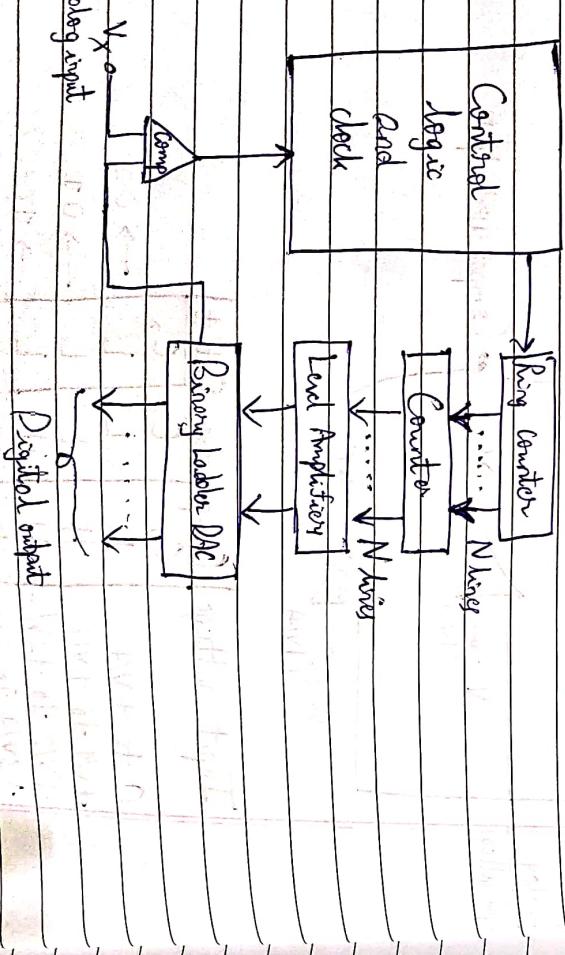
$$\frac{1}{500\text{kHz}} = \underline{\underline{2\mu\text{s}}}$$

∴ For 256 clock cycles, it is  $256 \times 2\mu\text{s} = \underline{\underline{512\mu\text{s}}} = \text{Max. conversion time}$

$$\frac{1}{512\mu\text{s}} = \underline{\underline{1953 \text{ conversions/second}}}$$

$$\text{Avg. conversion time} = \frac{1}{2} \times \text{Max. conversion time} = \frac{1}{2} \times 512\mu\text{s} = \underline{\underline{256\mu\text{s}}}$$

## ★ Successive Approximation Type ADC:-



Good Luck	Page no 107
Date 28	11 19

Problem -

1) Calc. Conversion time of 10 bit successive approximation type ADC operating with 1 MHz clock.

$$\rightarrow \text{Conversion rate } T = \frac{1}{1 \times 10^6} = 10^{-6} \text{ sec} = \underline{\underline{1 \mu\text{s}}}$$

$$\text{Conversion time} = n \times T = 10 \times 10^{-6} \text{ s} = \underline{\underline{10 \mu\text{s}}}$$