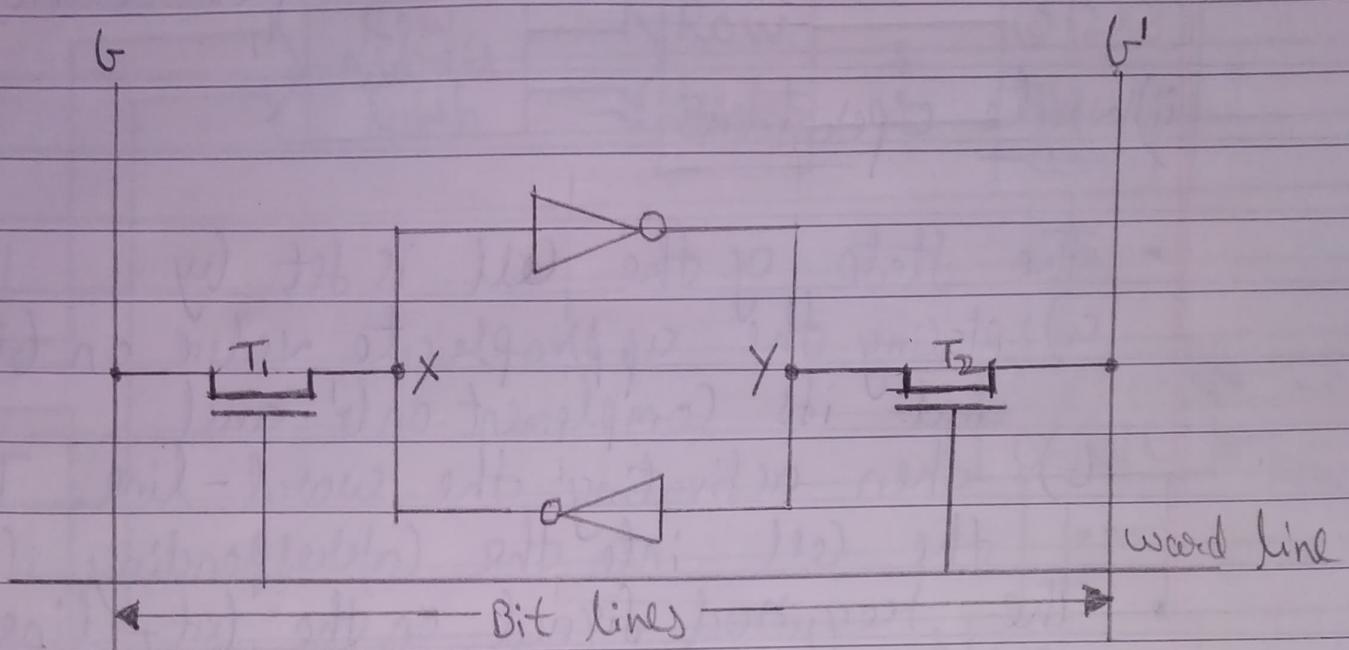


Static RAM Cell :-



Memories consists of circuit capable of retaining their states as long as power is applied are known.

Two inverters are cross connected to form a latch.

The latch is connected to 2-bit-lines by transistors T_1 and T_2 .

The transistors act as switches that can be opened / closed under the control of the word-line.

When the word-line is at ground level, the transistors are turned off and the latch retains its state.

i) Read operation :-

- To read the state of the cell, the word-line is activated to close switches T_1 and T_2 .
- If the cell is in State 1, the signal on bit-line b is high and the signal on the bit line b' is low.

- Sense/write circuit:-

- a) monitors the state of b and b' and
- b) sets the output accordingly

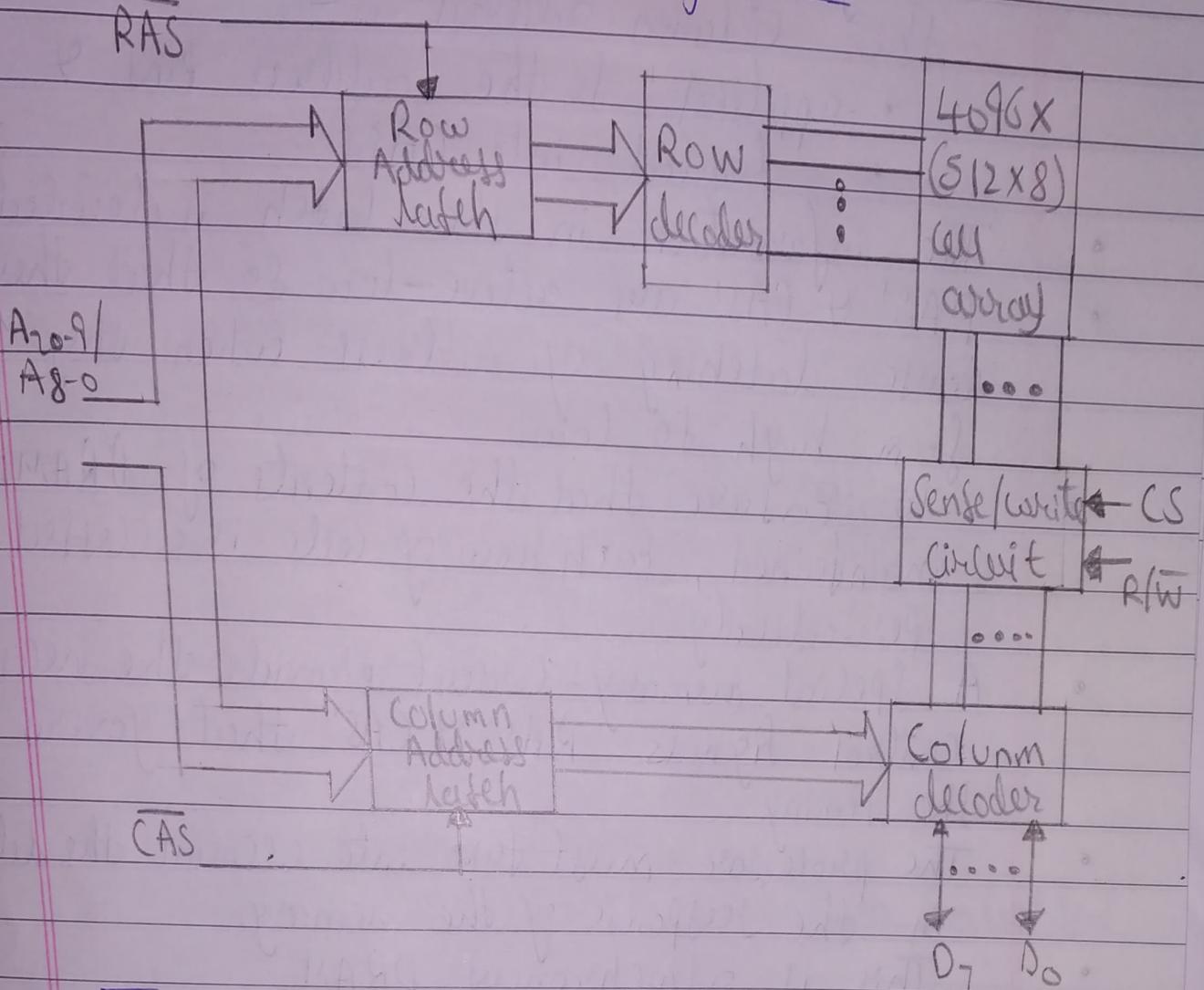
- ii) Write operations :-

- The state of the cell is set by

- a) placing the appropriate value on bit line b and its complement on b' and
- b) then activating the word-line. This forces the cell into the corresponding state.

- The required signal on the bit-lines is generated by sense/write circuit.

Asynchronous DRAM Memory Chip :-



- The 4 bit cells in each row are divided into 512 groups of 8.
- 21 bit address is needed to access a byte in the memory. 21 bit is divided as follow:
 - i) 12 address bits are needed to select a row i.e. A₈₋₀ → Specifies Row-address of a byte
 - ii) 9 bits are needed to specify a group of 8 bits in the selected row.
i.e A₂₀₋₉ → Specifies Column-address of a byte
- During Read/write operation,
 - a) Row-address is applied first.
 - b) Row-address is loaded into Row-latch in response to a signal pulse on RAS' input of chip.
- When a Read-operation is initiated, all cells on the selected row are read and latched.

- Shortly after the row-address is loaded, the column address is -
 - applied to the address pins &
 - loaded into CAS.
- The information in the latch is decoded.
- RAS' & CAS' are active-low so that they cause latching of address when they change from high to low.
- To ensure that the contents of DRAMs are maintained, each row of cells is accessed periodically.
- A special memory-circuit provides the necessary control signals RAS' & CAS' that govern the timing.
- The professor must take into account the delay in the response of the memory.
This is asynchronous DRAM.

ROM Cell :-

- Both SRAM and DRAM Chips are volatile, i.e. They lose the stored information if power is turned off.
- Many applications requires non-volatile memory which retains the stored information if power is turned off.
- For ex:-

OS software has to be loaded from disk to memory i.e. it requires non-volatile memory.

- Non-Volatile memory is used in Embedded System.
- Since the normal operation involves only reading of stored data, a memory of this is called ROM.

i) At logic value '0' :- Transistor (T) is connected to the ground point (P).

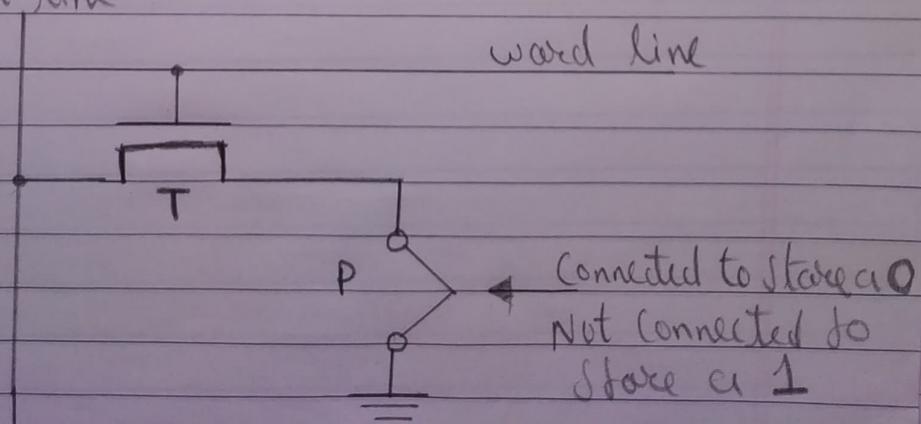
Transistor switch is closed & voltage on bit-line nearly drops to zero.

ii) At logic value '1' :- Transistor switch is open.

The bit-line remains at high voltage

Bit line

word line



- To read the state of the cell, the word line is activated.
- A sense circuit at the end of the bit line generates the proper output value.

Different types of non-volatile memory are:-

i) PROM (Programmable ROM) :-

- PROM allows the data to be loaded by the user.
- Programmability is achieved by inserting a 'fuse' at point P in a Rom cell.
- Before PROM is programmed, the memory contains all 0's.
- User can insert 1's at required location by burning-out fuse using high current pulse.
- This process is irreversible.

Advantages :-

- a) It provides flexibility
- b) It is faster
- c) It is less expensive because they can be programmed directly by user.

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ii) EPROM (Erasable Reprogrammable Rom) :-

- EPROM allows the stored data to be erased and new data to be loaded.
- In an EPROM cell, a connection to ground is always made at 'P' and a special transistor is used, which has the ability to function either as a normal transistor or as a disabled transistor that is always turned off.
- This transistor can be programmed to behave as a permanently open switch, by injecting charge into it that becomes trapped inside.
- Erasure requires dissipating the charges trapped in the transistor of memory cells.
- This can be done by exposing the chip to ultra violet light, so that EPROM chips are mounted in packages that have transparent windows.

iii) EEPROM (Electrically Erasable ROM) :-

- EEPROM is a type of non-volatile memory used in computers and other electronics devices to store small amounts of data that must be saved when power is removed e.g.: - Calibration tables or device configuration.

Advantages :-

- It can be both programmed and erased electrically
- It allows the erasing of all cell contents selectively.

Disadvantages :-

- It requires different voltage for erasing, writing and reading the stored data.

Speed, size and Cost :-

Below given are some of the RAMs with their's Speed, size and cost :-

i) Static RAM :-

It is very fast, expensive, because a basic SRAM cell has a complex circuit making it is impossible to pack a large number of cells onto a single chip, hence its size is large.

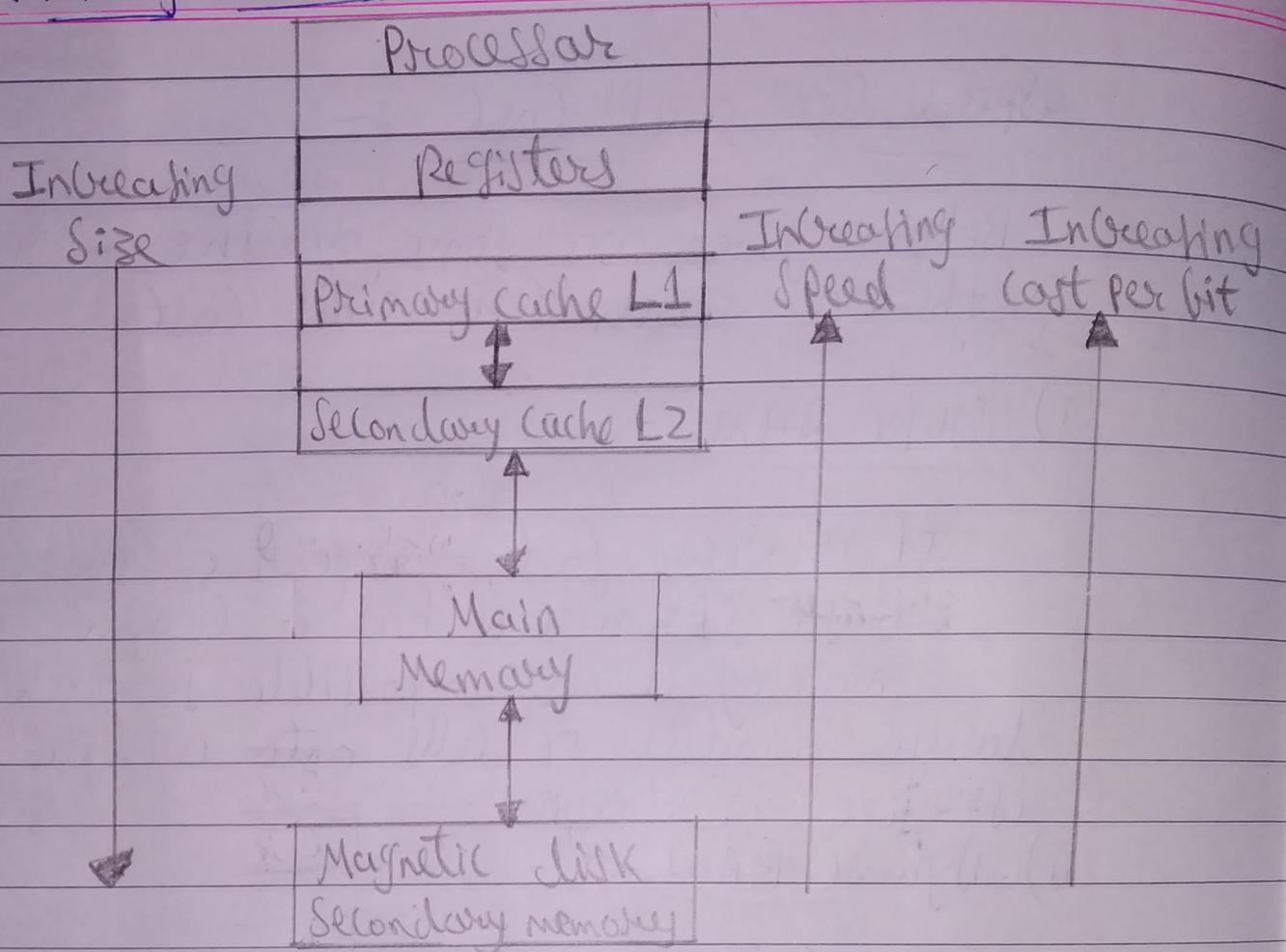
ii) Dynamic RAM :-

Simpler basic cell circuit, hence are much less expensive, but significantly slower than SRAMs and smaller in size.

iii) Magnetic Disks :-

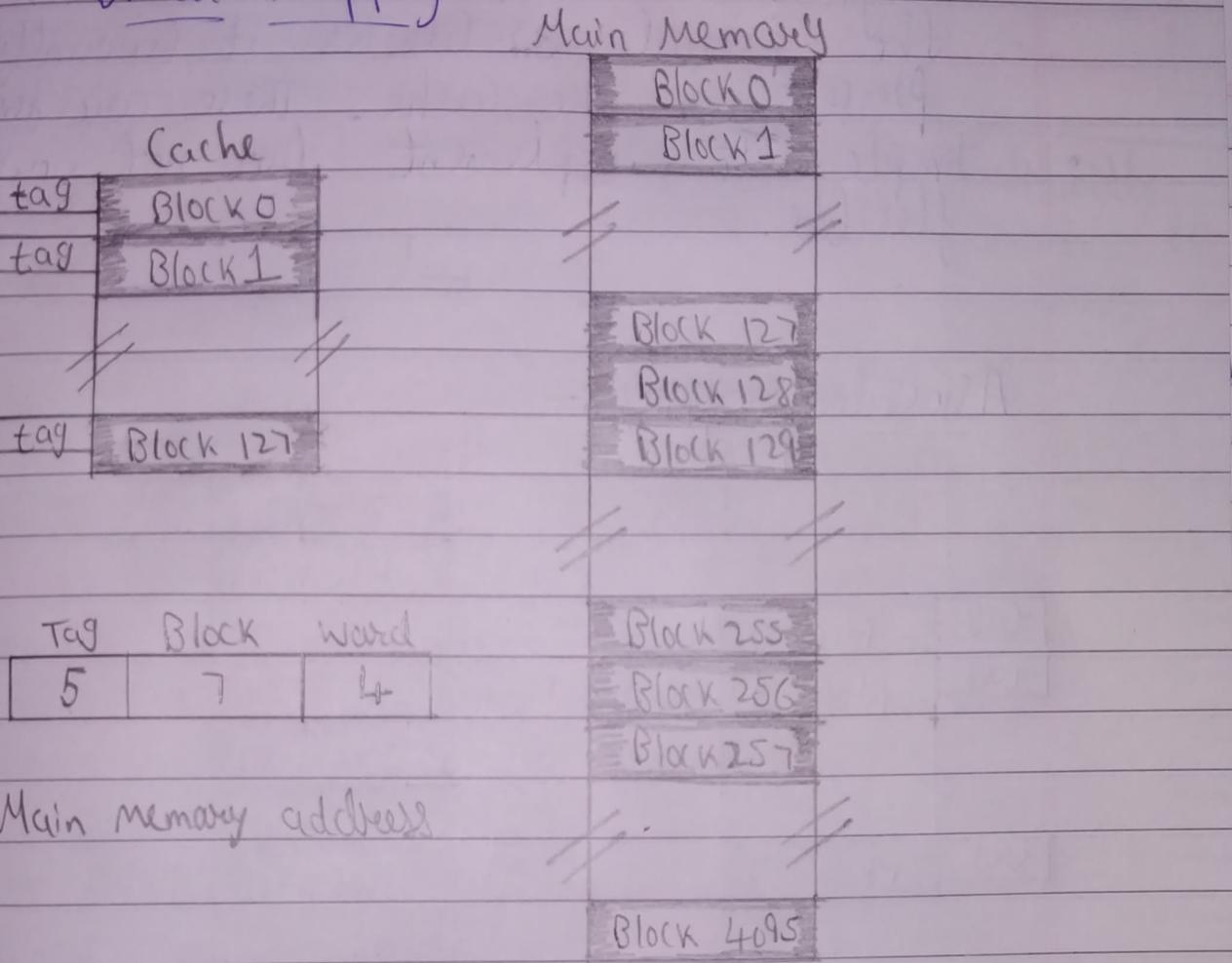
- Storage provided by DRAMs is higher than SRAMs, but still less than what is necessary.
- Secondary storage such as magnetic disks provide a large amount of storage but it is much slower than DRAMs.

Memory hierarchy:-



- Fastest access is to the data held in processor registers. Registers are at the top of the memory hierarchy.
- Relatively small amount of memory that can be implemented on the processor chip. This is processor cache.
- Two levels of cache, Level 1 (L1) cache is on the processor chip. Level 2 (L2) cache is in between main memory and processor.
- Next level is main memory, implemented as SIMMs. Much larger, but much slower than cache memory.
- Next level is magnetic disks. Huge amount of inexpensive storage.
- Speed of memory access is critical, the idea is to bring instructions and data that will be used in the near future as close to the processor as possible.

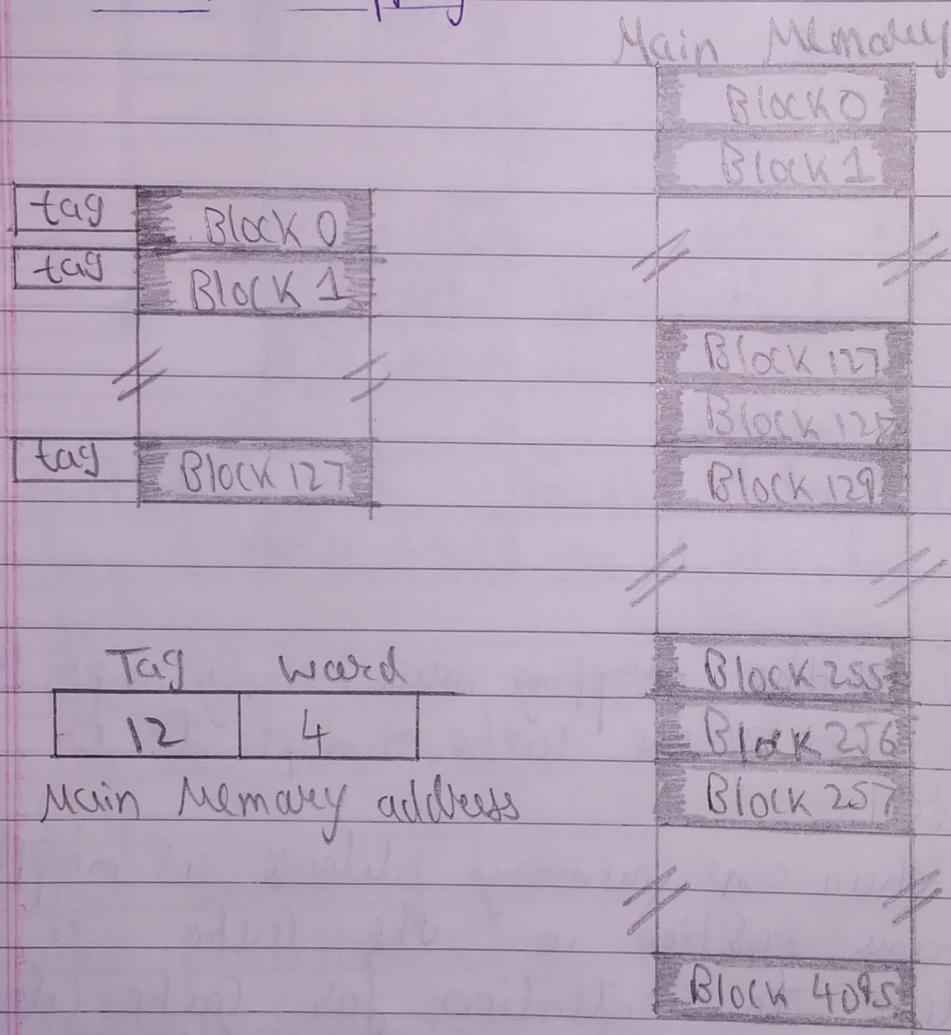
Direct Mapping :-



- Block j of the mapping main memory maps to j models 128 of the Cache. 0 maps to 0, 129 maps to 1.
- More than one memory block is mapped onto the same position in the Cache.
- May lead to contention for Cache blocks even if the Cache is not full.
- Resolve the contention by allowing new block to replace the old block, leading to a trivial replacement algorithm.
- Memory address is divided into three fields:-
 - Low order 4 bits determine one of the 16 words in the blocks.
 - When a new block is brought into the cache the next 7 bits determine which Cache block this new block is placed in.

- High order 5 bits determine which of the possible 32 blocks it currently present in the cache. These are tag bits.
- Simple to implement but not very flexible.

Associative mapping :-



- Main memory block can be placed into any cache position.
- Memory address is divided into two fields:-
 - Low order 4 bits identify the word within a block.
 - High order 12 bits or tag bits identify a memory block when it is resident in the cache.

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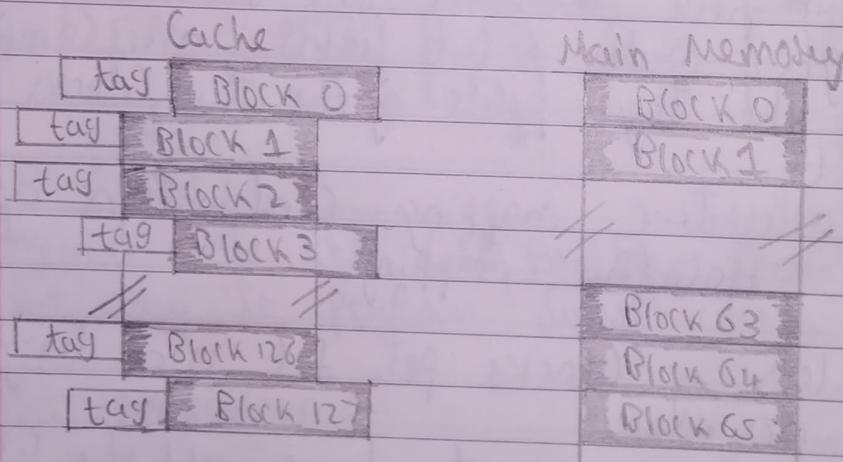
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- Flexible, and uses Cache Space definitely
- Replacement algorithm can be used to efficiently replace an existing block in the cache when the cache is full.
- Cost is higher than direct-mapped cache because of the need to search all 128 patterns to determine whether a given block is in the cache.

Set-Associative mapping :-



Tag	Block	word
5	7	4

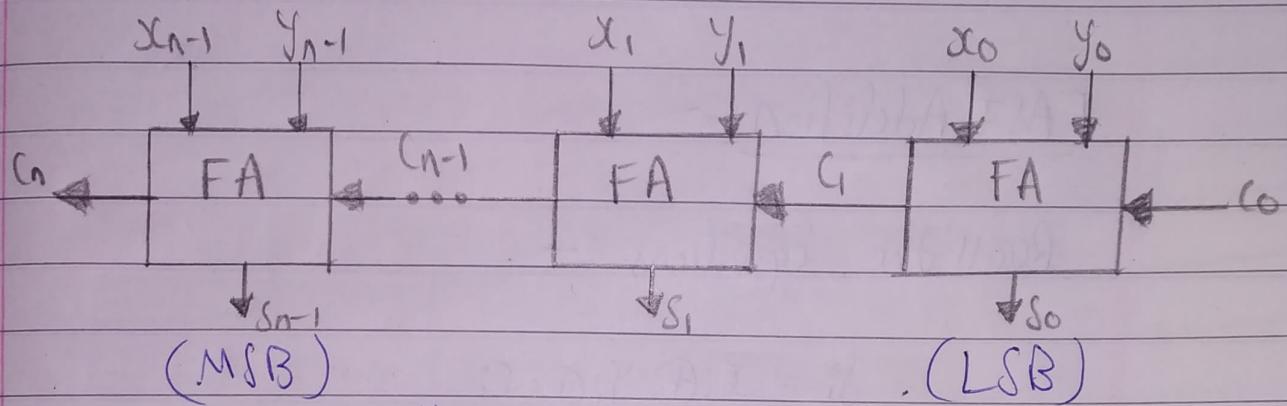
Main memory address

Block 127
Block 128
Block 129
Block 129

- Blocks of Cache are grouped into sets.
- Mapping function allows a block of the main memory to reside in any block of a specific set.
- Divide the Cache into 64 sets, with two blocks per set.
- Memory block 0, 64, 128 etc. map to block 0, and they can occupy either of the pointer positions.
- Memory address is divided into three fields:
 - 6 bit field determine the set number.
 - Higher order 6 bit fields are compared to the tag fields of the two blocks in a set.
- Set-associative mapping combination of direct and associative mapping.
- Number of blocks per set is a design parameter:
 - one extreme is to have all the blocks in one set, requiring no set bits (fully associative mapping).
 - Other extreme is to have one block per set, is the same as direct mapping.

n-Bit Ripple Carry Adder :-

- Cascaded connection of n-full-adder blocks can be used to add 2-bit adder numbers.
- Since carries must propagate (or ripple) through cascade, the configuration is called an n-bit Ripple Carry adder.



Carry-in to the LSB position provides a convenient way to perform subtraction.

Logic Specification :-

x_i	y_i	Carry-in c_i	Sum s_i	Carry-out c_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$(c_i = \text{carry in})$$

$$s_i = \overline{x_i} \overline{y_i} c_i + \overline{x_i} y_i c_i + x_i \overline{y_i} c_i + x_i y_i c_i$$

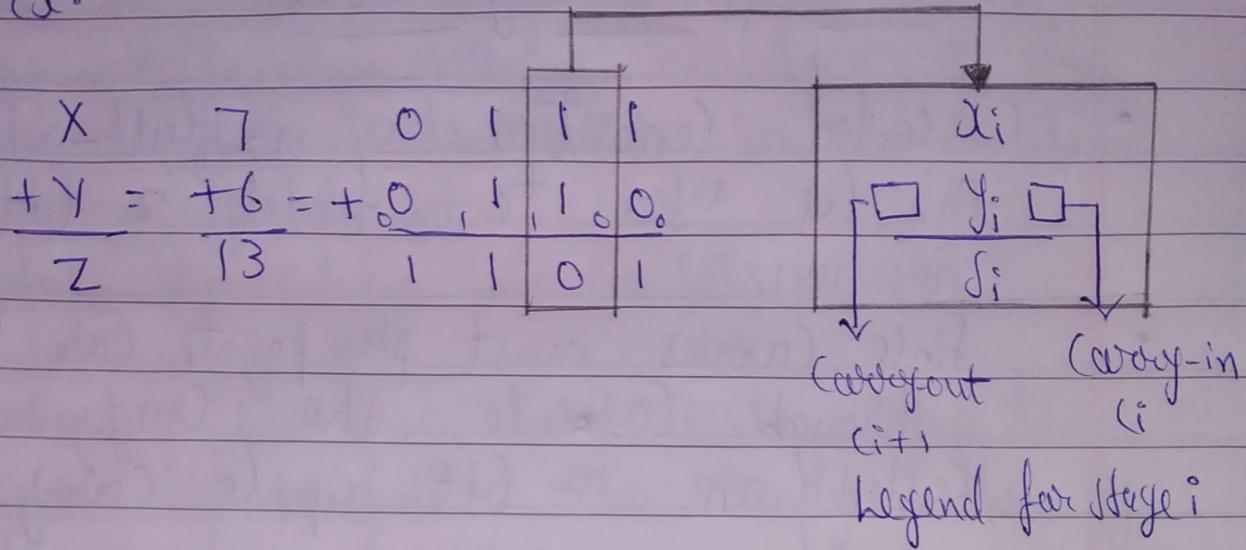
$$s_i = \text{sum}$$

$$s_i = x_i \oplus y_i \oplus c_i$$

$$c_{i+1} = \text{carry out}$$

$$c_{i+1} = y_i c_i + x_i c_i + x_i y_i$$

Ex:-



FAST Addition :-

Recall the Equations :-

$$S_i = x_i \oplus y_i \oplus C_i$$

$$C_{i+1} = x_i y_i + x_i C_i + y_i C_i$$

Second Equation can be written as :-

$$C_{i+1} = G_i + P_i C_i$$

we can write :-

$$G_i = x_i y_i$$

where; $G_i = x_i y_i$ and $P_i = x_i + y_i$

- G_i is called generate function and P_i is called propagate function.
- G_i and P_i are counted only from x_i and y_i and not C_i thus they can be computed in one gate delay after X and Y are applied to the inputs of an n-bit adder.

Carry Lookahead :-

$$C_{i+1} = G_i + P_i C_i$$

$$C_i = G_{i-1} + P_{i-1} C_{i-1}$$

$$\Rightarrow C_{i+1} = G_i + P_i (G_{i-1} + P_{i-1} C_{i-1})$$

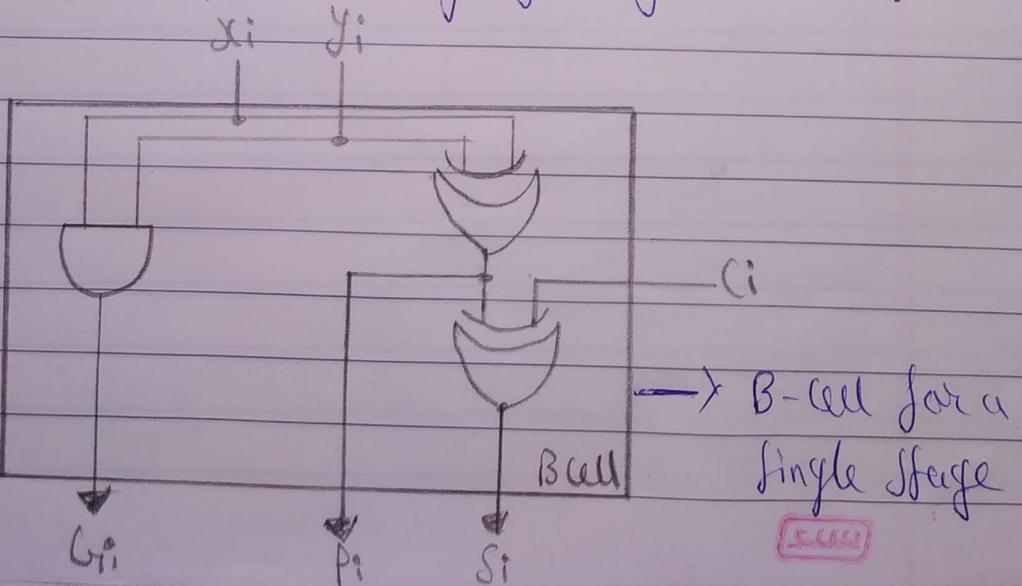
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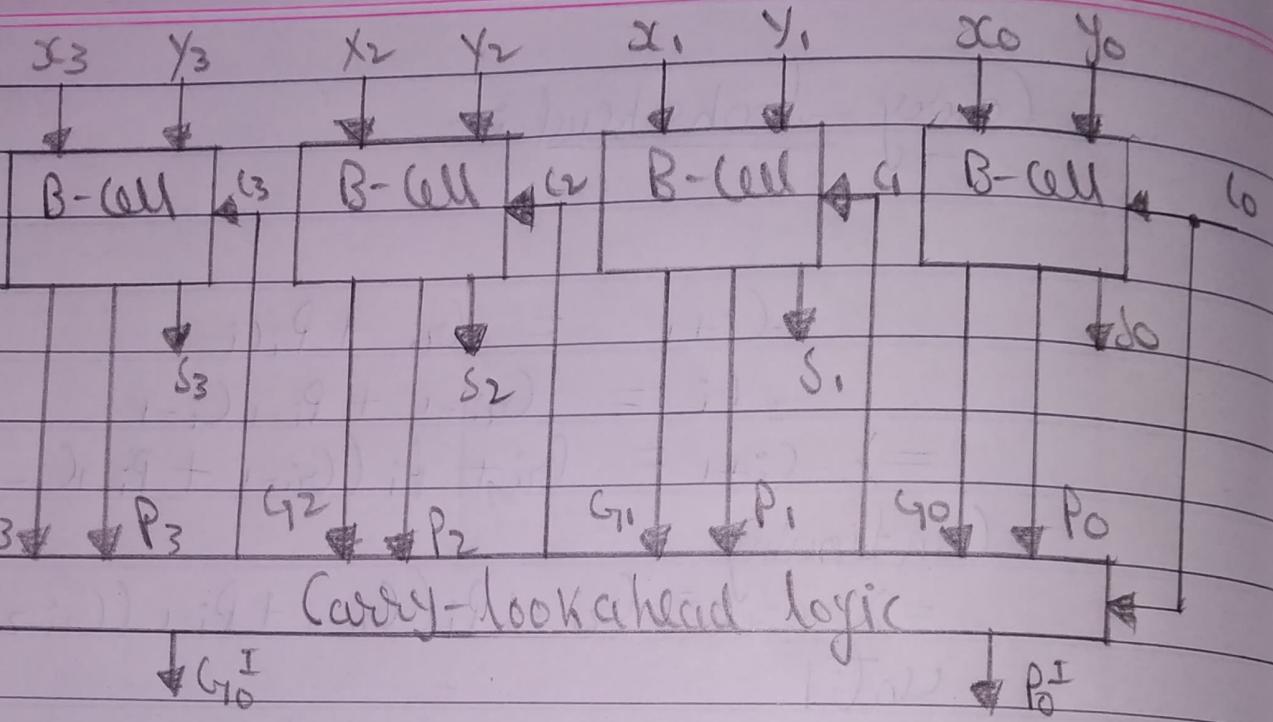
$$\Rightarrow C_{i+1} = G_i + P_i (G_{i-1} + P_{i-1} (G_{i-2} + P_{i-2} C_{i-2}))$$

until

$$C_{i+1} = G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + \dots + P_i P_{i-1} \dots \\ \dots P_1 G_0 + P_i P_{i-1} \dots P_0 C_0$$

- All Carries can be obtained 3 gate delays after X, Y and co are applied
 - One gate delay for P_i and G_i
 - Two gate delays in the AND-OR circuit for C_{i+1}
- All Sums can be obtained 1 gate delay after the carries are computed.
- Independent of n, n-bit addition requires only 4-gate delays.
- This is called Carry lookahead adder
- Limitation: If we try to extend the carry lookahead adder for longer operands, we run into a problem of gate fan-in constraint.



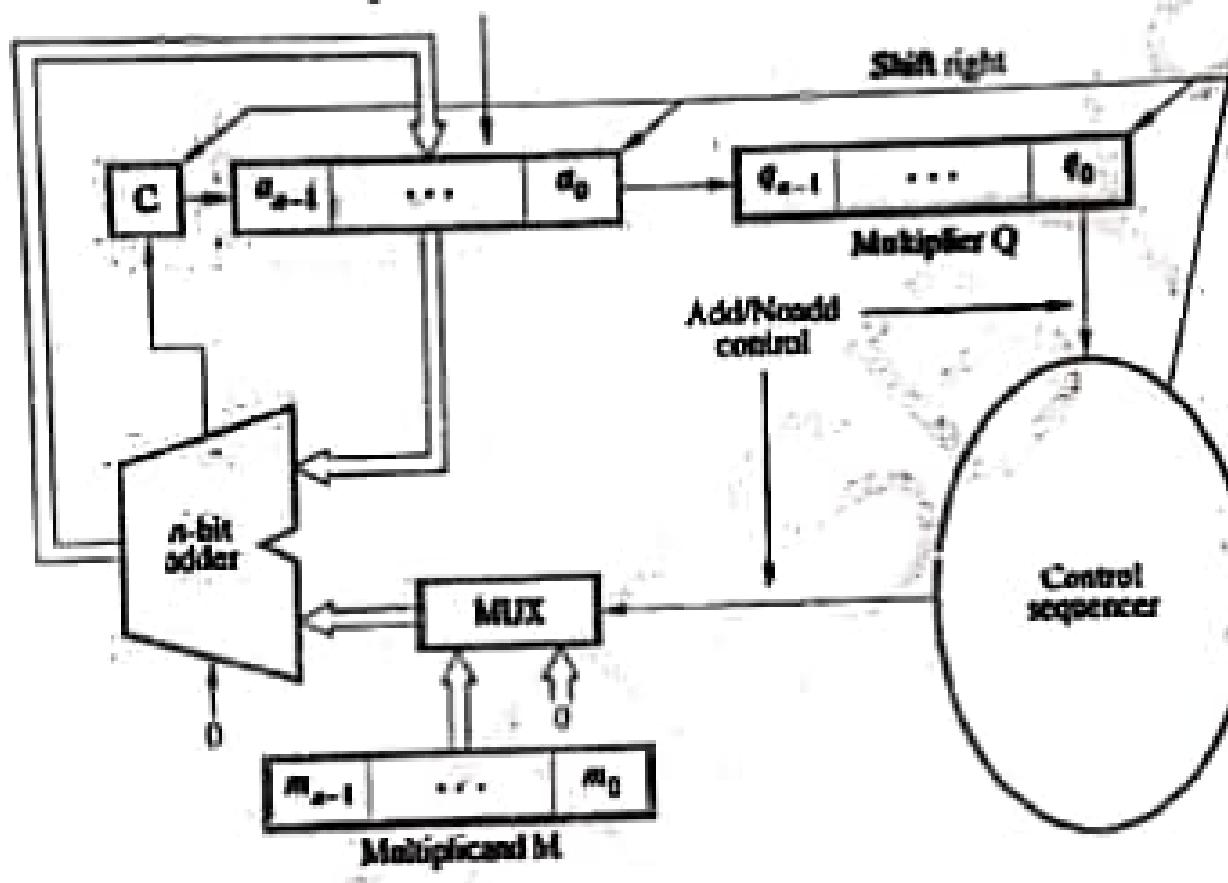


4-bit-Carry look ahead adder

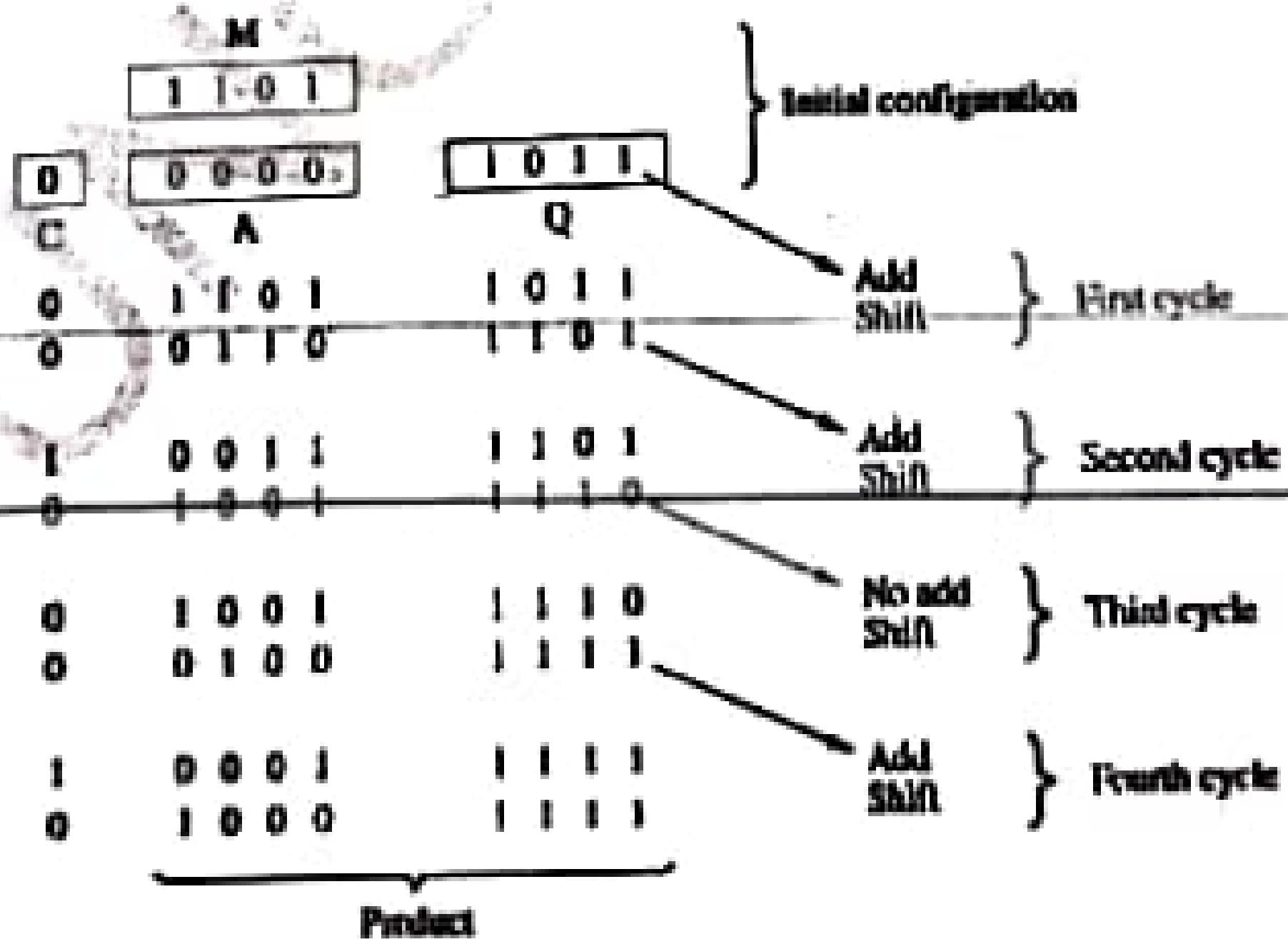
SEQUENTIAL CIRCUIT BINARY MULTIPLIER

- Registers A and Q combined hold PP_i(partial product) while the multiplier bit q_i generates the signal Add/Noadd.
 - The carry-out from the adder is stored in flip-flop C (Figure 9.7).
 - Procedure for multiplication:
 - 1) Multiplier is loaded into register Q,
Multiplicand is loaded into register M and
C & A are cleared to 0.
 - 2) If q₀=1, add M to A and store sum in A. Then C, A and Q are shifted right one bit-position.
If q₀=0, no addition performed and C, A & Q are shifted right one bit-position.
 - 3) After n cycles, the high-order half of the product is held in register A and
the low-order half is held in register Q.

Register A (Continuity 0)



(a) Register configuration



(a) Multiplication example

Figure 9.7 Sequential circuit binary multiplier.

ADDITION/SUBTRACTION LOGIC UNIT

- The n-bit adder can be used to add 2's complement numbers X and Y (Figure 9.3).
- Overflow can only occur when the signs of the 2 operands are the same.
- In order to perform the subtraction operation $X-Y$ on 2's complement numbers X and Y; we form the 2's complement of Y and add it to X.
- Addition or subtraction operation is done based on value applied to the Add/Sub input control-line.
- Control-line=0 for addition, applying the Y vector unchanged to one of the adder inputs.
Control-line=1 for subtraction, the Y vector is 2's complemented.

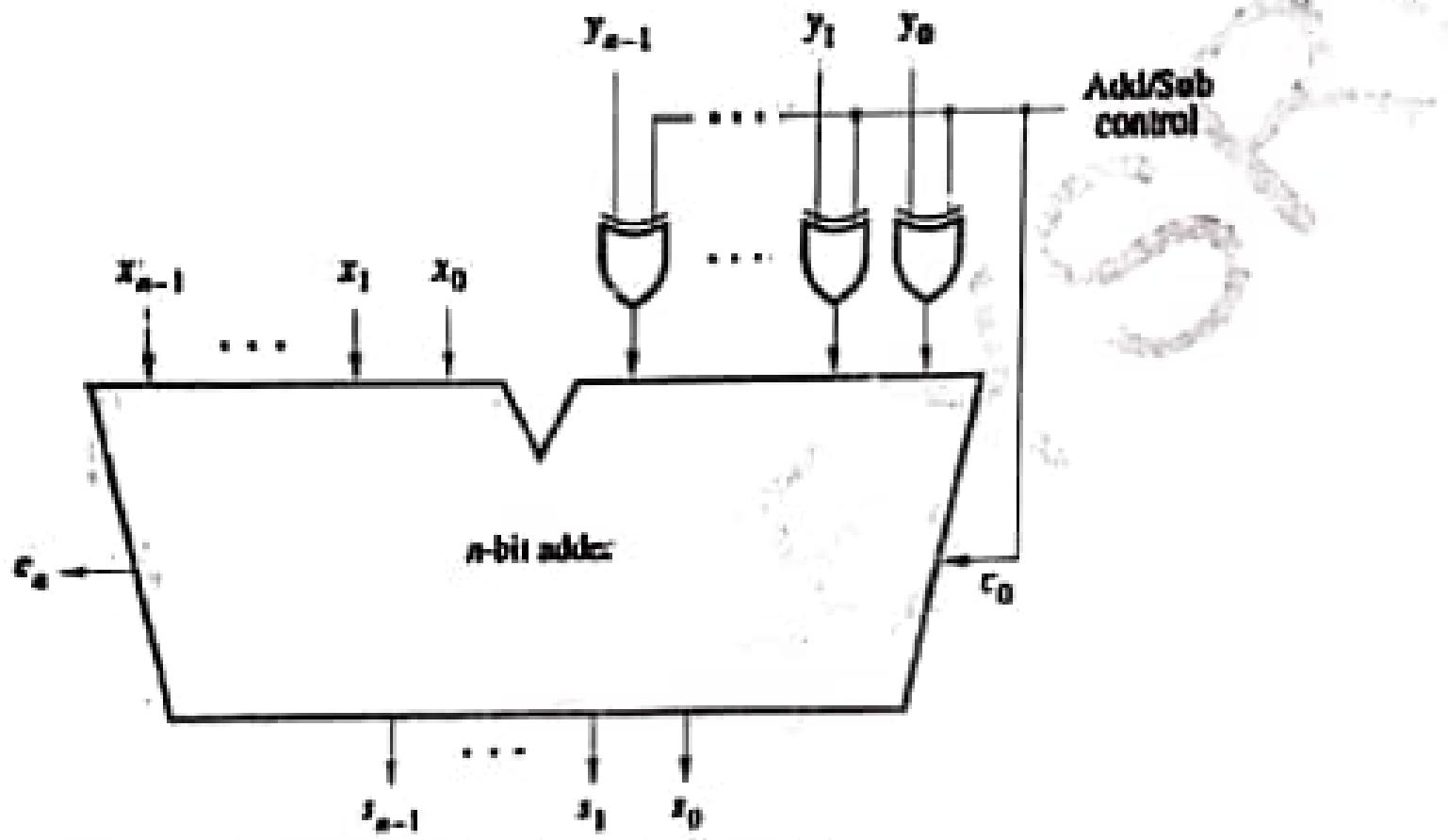


Figure 9.3 Binary addition/subtraction logic circuit.

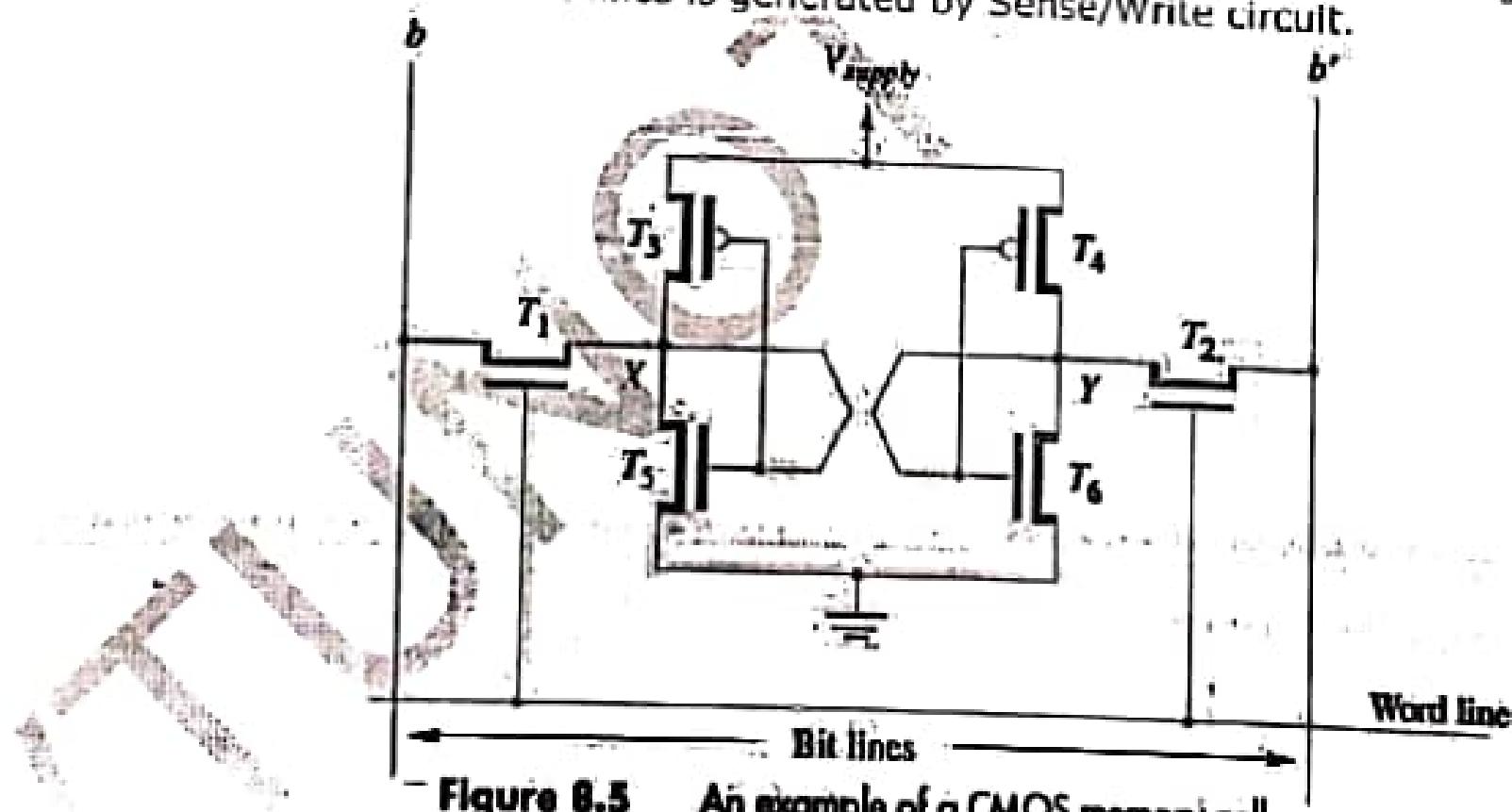


Figure 8.5 An example of a CMOS memory cell.

CMOS Cell

- Transistor pairs (T_3, T_5) and (T_4, T_6) form the inverters in the latch (Figure 8.5).
- In state 1, the voltage at point X is high by having T_5, T_6 ON and T_4, T_5 are OFF.
- Thus, T_1 and T_2 returned ON (Closed), bit-line b and b' will have high and low signals respectively.
- **Advantages:**
 - 1) It has low power consumption 'cause the current flows in the cell only when the cell is active.
 - 2) Static RAM's can be accessed quickly. Its access time is few nanoseconds.
- **Disadvantage:** SRAMs are said to be volatile memories 'cause their contents are lost when power is interrupted.

- Transistor pairs (T3, T5) and (T4, T6) form the inverters in the latch.
- In state 1, the voltage at point X is high by having T3, T6 on and T4, T5 are OFF.
- Thus T1 and T2 returned ON (Closed), bit line b and b' will have high and low signals respectively.
- The CMOS requires 5V (in older version) or 3.3.V (in new version) of power supply voltage.
- The continuous power is needed for the cell to retain its state.

Merit:

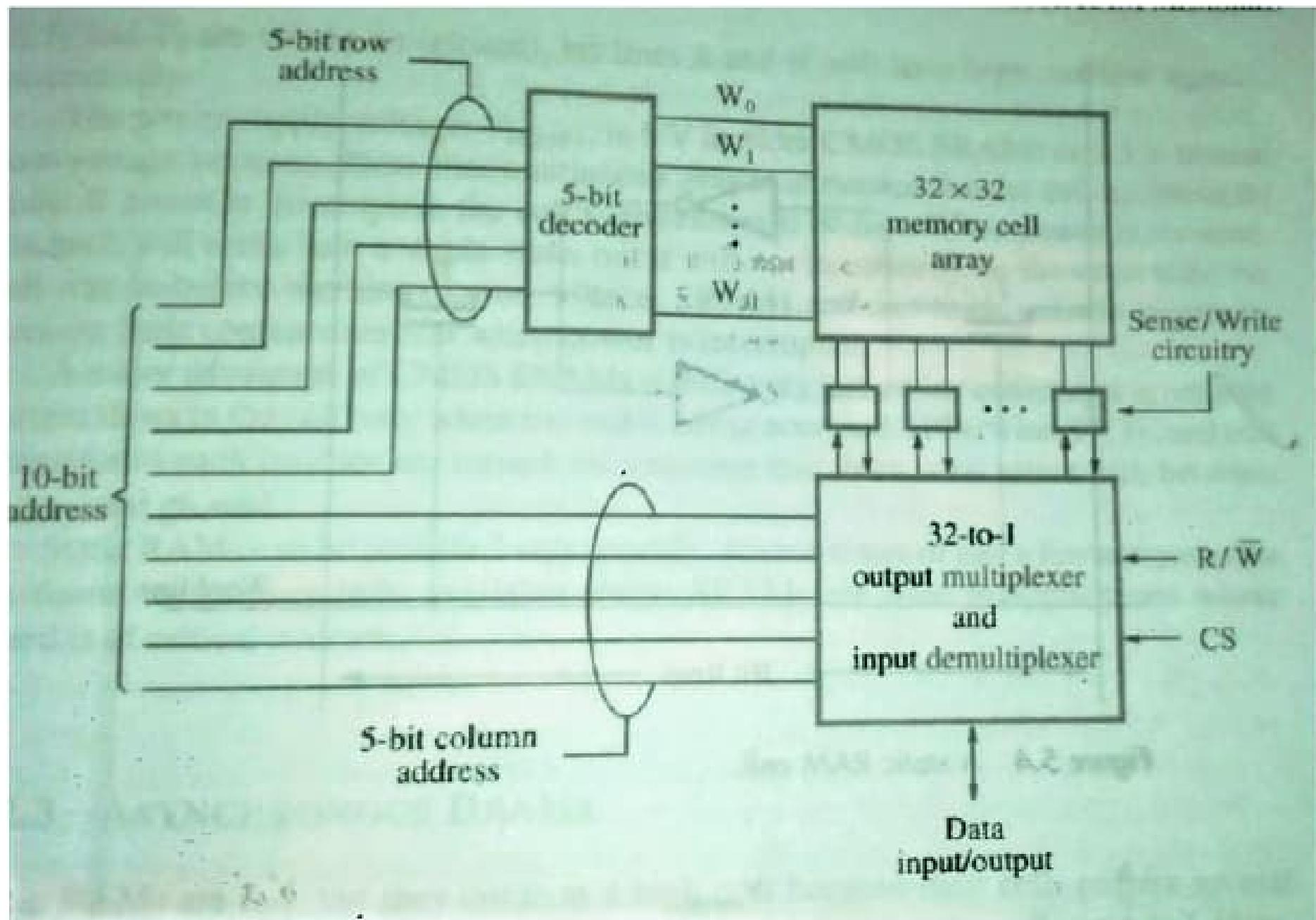
- ◆ It has low power consumption because the current flows in the cell only when the cell is being accessed.
- ◆ Static RAMs can be accessed quickly. Its access time is few nanoseconds.

Demerit:

- ◆ SRAMs are said to be volatile memories because their contents are lost when the power is interrupted.



Organization of 1K X 1 Memory Chip



- Memory chip consisting of 16 words of 8 bit each.
- This is referred to as a **16x8** organization.
- It can store 128 bits and requires 14 external connections for address, data and control lines.
- It also needed 2 lines for power supply and ground.
- Consider a memory circuit with **1K** cells.
 - ◆ this can be organized as a **128x8** memory.
 - ◆ Requiring a total of **19** external connections

◆ Same can be organized into a **1Kx1** format

- 10 bit address is needed
 - But there is only one data line.
 - Requiring a total of **15 external** connections
- ◆ The required 10-bit address is divided into 2 groups of 5-bits each to form a row and column addresses for the cell array.
- ◆ Row address selects a row of 32 cells, all of which are selected in parallel
- ◆ According to the column address only one of these cells is connected to the external data line by the output multiplexer and the input demultiplexer