

Introduction to HDL:

- This is textual description of a digital circuit
- HDL is an acronym for Hardware Description Language
- Its features are
 - i) Describe a large complex design requiring hundreds of logic gates in a convenient manner, in a smaller space
 - ii) Use software test bench to detect functional errors, if any, and correct it (called simulation and
 - iii) get hardware implementation details (called synthesis)

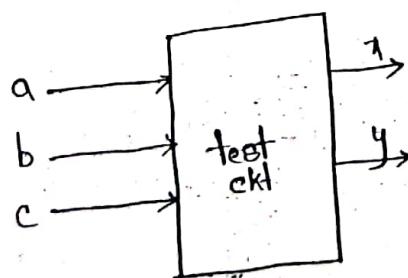
→ There are two widely used HDLs

- Verilog
- VHDL

Verilog HDL:

→ simulation and verification tool

Describing Input/Output:



```

module testckt(x,y,a,b,c); // module
                           // name with
                           // port list
   input a, b, c; // defines input
                  // ports
   output x, y; // defines output
                  // ports
   // module body begins next describing
   // logic relation
   // module body ends
   // endmodule
  
```

- These, module, endmodule, input and output are keywords for Verilog.
- A module describes a design entity with a name or identifier selected by user followed by input output port list.
- endmodule need not to be terminated by ;

2. HDL implementation models

- There are two implementation models
 - i) Dataflow modeling
 - ii) Behavioral modeling (statements are executed sequentially following algorithmic description)

i) Dataflow modeling:

- is also known as gate level modeling.
- consumes more space in describing a circuit and is unsuitable for large, complex designs.
- Verilog provides a keyword assign and a set of operators to describe a circuit through its behavior or function.
- Gate structures need not be defined explicitly using and, or etc. Also not necessary to use intermediate variables through wire to show gate level interconnections.
- Verilog compiler handles this while compiling such a model.
- All assign statements are concurrent i.e., tasks in which they appear do not interact and also continuous i.e., any change in a variable on the right hand side will immediately affect left hand side output.

→ Table below shows a partial list of Verilog operators. (2)

Relational operation Symbol

Less than <

Less than or equal to <=

Greater than >

Equal to ==

Not equal to !=

Logical operation Symbol
(for expressions)

Logical NOT !

" AND &&

" OR ||

Bitwise operation Symbol

Bit-wise NOT ~

" AND &

" OR |

" EX-OR ^

Arithmetic operation Symbol

Binary addition +

" subtraction -

" multiplication *

" division /

Ex: 1) Dataflow model Verilog code for simple SOP equation,

$$Y = (AB) + (CD)$$

```
module sopEquation (A, B, C, D, Y);
```

```
    input A, B, C, D;
```

```
    output Y;
```

```
    assign Y = (A & B) + (C & D);
```

```
endmodule
```

Ex: 2) Verilog code for 1 to 1 MUX using dataflow modeling.

```
module mux1to1 (A, B, D0, D1, D2, D3, Y);
```

```
    input A, B, D0, D1, D2, D3;
```

```
    output Y;
```

```
    assign Y = A ? (B ? D3 : D2) : (B ? D1 : D0);
```

```
endmodule.
```

Ex: 3) Verilog code for D flip-flop using dataflow modeling.

~~module dflipflop (output q, qbbar, input D, clk);~~

~~assign q = (D & clk),~~

~~qbbar = (~q);~~

~~endmodule~~

f) Verilog code for 3 to 8 line decoder using dataflow modeling. (3)

```
module decoder_df (output [0:7]D, input A,B,C, enable);
assign D[0] = (~A & ~B & ~C & enable),
      D[1] = (~A & ~B & C & enable),
      D[2] = (~A & B & ~C & enable),
      D[3] = (~A & B & C & enable),
      D[4] = (A & ~B & ~C & enable),
      D[5] = (A & ~B & C & enable),
      D[6] = (A & B & ~C & enable),
      D[7] = (A & B & C & enable);
endmodule
```

Digital to Analog converters; and Analog to Digital converters

1. Introduction:

- Most of the information carrying signals such as voltage, current, charge, temperature, pressure and time are available in the analog form.
- However, for processing, transmission and storage purposes, it is often more convenient to express such signals in the digital form.
- When expressed in the digital form, they provide better accuracy and reduce noise.
- Moreover, the development in the microprocessor technology has made it compulsory to process data in the digital form.
- Since digital system such as microprocessors use a binary system of ones and zeros, we have to convert signal from analog form to digital (A/D) converter.
- Once the signal is measured it is used to
 - i) Compare with set value and determine the control signal in the process control system or
 - ii) Generate the desired output by processing the signal.
- Fig. 1 shows the basic elements of digital signal processing system.

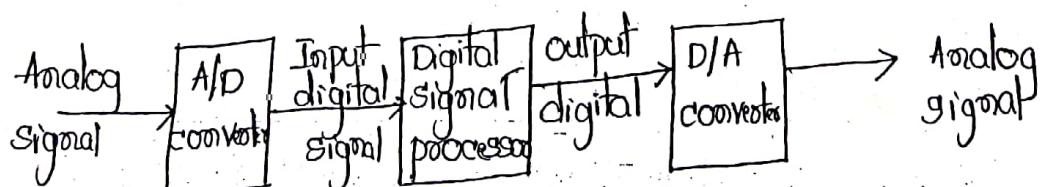


Fig. 1 Basic elements of digital signal processing.

- Most of the signals generated are analog in nature. Hence these signals are converted to digital form by the analog to digital converter.
- Thus the A/D converter generates an array of samples

and gives it to the digital signal processor. This error samples (or sequence of samples) is the digital equivalent of input analog signal. It is called digital signal.

→ The digital signal processor performs signal processing operation like filtering, multiplication, transformation, amplification etc over this digital signal and generates another digital signal at its output.

→ Digital signal processor:

Eg: High speed digital computer

2. D/A converters:

→ A DAC (Digital to Analog converter) accepts an n-bit input word $b_1, b_2, b_3 \dots b_n$ in binary and produce an analog signal proportional to it.

→ Fig. 2 shows circuit symbol and input-output characteristics of a 4-bit DAC.

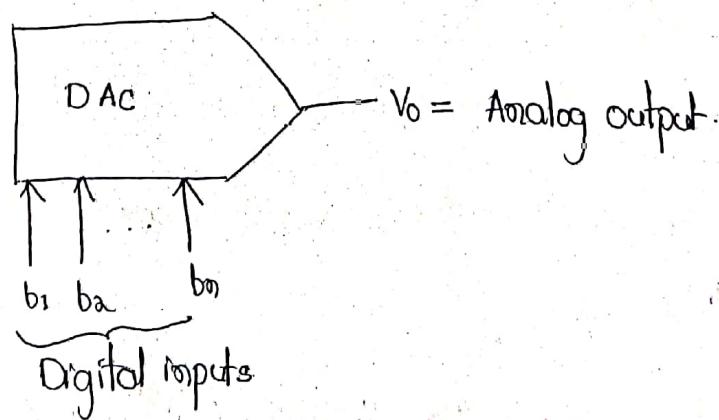
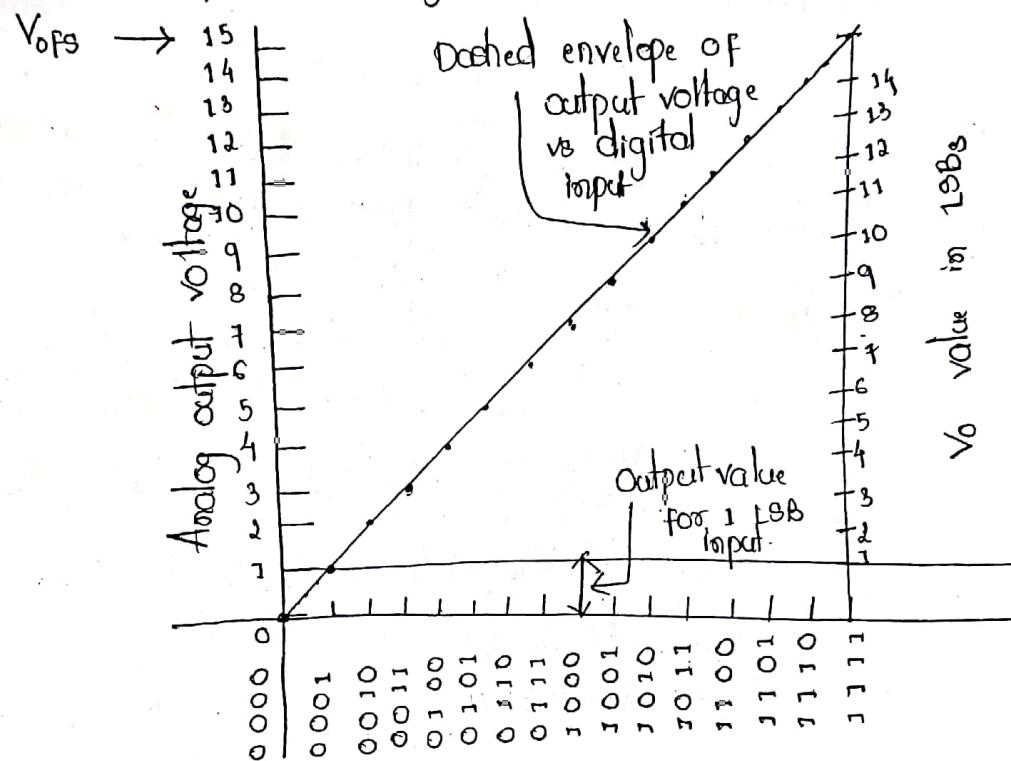


Fig. 2. DAC circuit symbol.

→ There are 4-digital inputs, indicating 4-bit DAC. Each digital input represents an electrical signal representing either a logic 1 or a logic 0.

→ The b_3 is the least significant bit, LSB, whereas b_1 is the most significant bit, MSB.

→ Fig. 3 shows analog output voltage V_o is plotted against all 16 possible digital input words. (4)



3. Performance parameters of DAC:

1) Resolution:

→ Resolution is the number of different analog output values that can be provided by a DAC. For an n -bit DAC

$$\boxed{\text{Resolution} = 2^n} \quad (1)$$

→ Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n -bit DAC it can be given as

$$\boxed{\text{Resolution} = \frac{V_{oFS}}{2^n - 1}} \quad (2)$$

where V_{oFS} = Full scale output voltage

→ From eqn(1), we can say that, the resolution can be determined

by the number of bits in the input binary
 → For an 8-bit DAC resolution can be given as

$$\text{Resolution} = \frac{V_{FS}}{2^7} = \frac{V_{FS}}{2^8}$$

$$= 2.56$$

→ If the full scale output voltage is 10.2V, then by second definition the resolution for an 8-bit DAC can be given as

$$\begin{aligned}\text{Resolution} &= \frac{V_{FS}}{2^7 - 1} = \\ &= \frac{10.2}{2^8 - 1} \\ &= \frac{10.2}{255} \\ &= 40\text{mV/LSB}\end{aligned}$$

→ Therefore, we can say that an input change of 1 LSB causes the output to change by 40mV.

→ From the resolution we can obtain the input-output equation for a DAC

$$\text{Thus, } V_o = \text{Resolution} \times D$$

where D = Decimal value of the digital input

$$V_o = \text{output voltage}$$

The resolution takes care of changes in the input

a) Accuracy:

→ It is a comparison of actual output voltage with expected output. It is expressed in percentage.

→ Ideally, the accuracy of DAC should be, at least, $\pm 1\%$ of its LSB. If the full scale output voltage is 10.2V then for an 8-bit DAC accuracy can be given as

(5)

$$\text{Accuracy} = \frac{V_{OFS}}{(2^n - 1) \times 2}$$

$$= \frac{10.2}{255 \times 2}$$

$$= \underline{\underline{20\text{mV}}}$$

Ex: 1) An 8 bit DAC has an output voltage range of 0-2.55V. Define its resolution in two ways.

Solⁿ: i) $n = \text{No. of bits} = 8$

$$\text{Resolution} = 2^n = 2^8 = 256$$

i.e., the output voltage can have 256 different values including zero

$$\text{ii) Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{2.55}{255} = 10\text{mV/LSB}$$

Thus an input change of 1 LSB causes the output to change by 10mV.

Ex: 2) The digital input for a 4-bit DAC is 0110. calculate its final output voltage.

Solⁿ: For a given DAC $n = 4$
 $\therefore V_{OFS} = 15\text{V}$

$$\therefore \text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{15}{15} = 1\text{V/LSB}$$

$$V_o = \text{Resolution} \times D$$

$$D = (0110)_2 = 6$$

$$V_o = 1\text{V/LSB} \times 6 = \underline{\underline{6\text{V}}}$$

1.1. Variable, Resistor Networks:

- The basic problem in converting a digital signal into an equivalent analog signal is to change the n digital voltage levels into one equivalent analog voltage.
- This can be most easily accomplished by designing a resistive network that will change each digital level into an equivalent binary weighted voltage (or current).

Binary equivalent weight.

- Suppose that we want to change the eight possible digital signals in the table below into equivalent analog voltages.

2^2	2^1	2^0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

- The smallest number represented is 000, let us make this equal to 0V. The largest number is 111 if it is made equal to +7V.

- This then establishes the range of the analog signal to be developed.

- Note that between 000 and 111 there are seven discrete levels to be defined.

→ It is convenient to divide the analog signal into 7 levels.

→ The smallest incremental change in the digital signal is represented by the least-significant bit (LSB), 2^0 .

→ LSB bit cause a change in the analog output that is equal to one-seventh of the full-scale analog output voltage.

i.e., $d^0 \rightarrow +\frac{1}{7} \times \frac{1}{7} = +\frac{1}{49}V$ at the output ($\frac{1}{7}$)

$d^1 \rightarrow +\frac{1}{7} \times \frac{2}{7} = +\frac{2}{49}V$ " " " ($\frac{2}{7}$)

$d^2 \rightarrow +\frac{1}{7} \times \frac{4}{7} = +\frac{4}{49}V$ ($\frac{4}{7}$)

$d^3 \rightarrow +\frac{1}{7} \times \frac{8}{7} = +\frac{8}{49}V$

→ Notice that the sum of the weights must equal 1. Thus

$$\frac{1}{7} + \frac{2}{7} + \frac{4}{7} = \frac{7}{7} = 1$$

→ In general, the binary equivalent weight assigned to the LSB is $\frac{1}{(2^n-1)}$, where 'n' is the number of bits. The remaining weights are found by multiplying by 2, 4, 8 and so on.

∴

$$\boxed{\text{LSB weight} = \frac{1}{(2^n-1)}}$$

Ex: 1) Find the binary equivalent weight of each bit in a 4-bit system.

Sol: The LSB has weight of $\frac{1}{2^4-1} = \frac{1}{15}$, or 1 part in

→ 2nd LSB $\rightarrow \frac{1}{15} \times 2 = \frac{2}{15}$

$$\text{2nd LSB} \rightarrow \frac{1}{15}$$

$$1^{\text{st}} \text{SB} \rightarrow \frac{8}{15}$$

$$\frac{1}{15} + \frac{2}{15} + \frac{4}{15} + \frac{8}{15} = 15/15 = 1.$$

Bit	Weight
2^0	$1/15$
2^1	$2/15$
2^2	$4/15$
Sum	$7/15$

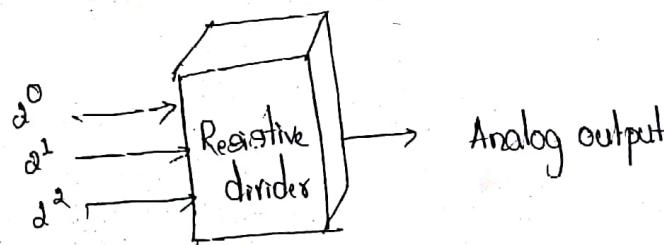
i. (a)

3-bit binary equivalent weights

Bit	Weight
2^0	$1/15$
2^1	$2/15$
2^2	$4/15$
2^3	$8/15$
Sum	$15/15$

i. (b)

4-bit binary equivalent weights



ii. (a)

Digital input	Analog output
0 0 0	+0V
0 0 1	+1V
0 1 0	+2V
0 1 1	+3V
1 0 0	+4V
1 0 1	+5V
1 1 0	+6V
1 1 1	+7V

ii. (b)

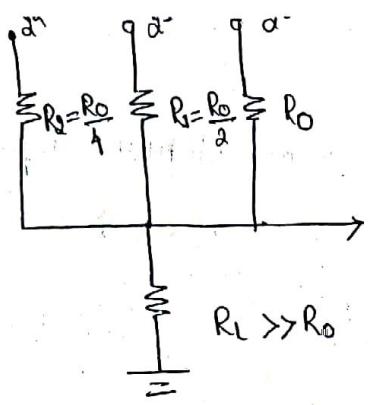
Digital input	Analog output
0 0 0	+0V
0 0 1	+1V
0 1 0	+2V
0 1 1	+3V
1 0 0	+4V
1 0 1	+5V
1 1 0	+6V
1 1 1	+7V

ii. (b)

Resistive Divider:

(4)

- A resistive divider that has three digital inputs and one analog output as shown in fig. 12.8a.
- Assume that the digital input levels are $0=0V$ and $1=+1V$. Now, for an input of 001, output will be $+1V$, for 010 output is $+2V$ and for 100, output is $+4V$.
- The digital input 011 is seen to be a combination of the signals 001 and 010.
 - i. e., $011 \rightarrow 001 + 010$
 - $\rightarrow 1V + 2V$
 - $\rightarrow 3V$
- The other desired voltage levels are shown in fig. 12.8b. They too are additive combinations of voltages.
- Thus the resistive divider must do two things in order to change the digital input into an equivalent analog output voltage.
 1. The a^0 bit must be changed to $+1V$, and a^1 bit must be changed to $+2V$, and a^2 bit must be changed to $+4V$.
 2. These three voltages representing the digits bits must be summed together to form the analog output voltage.
- A resistive divider that performs these functions is shown in fig. 3. a
- Resistors R_0 , R_1 , and R_2 form the divider network. Resistance R_L represents the load to which the divider is connected & is considered to be large enough that it does not load the divider network.



Analog output

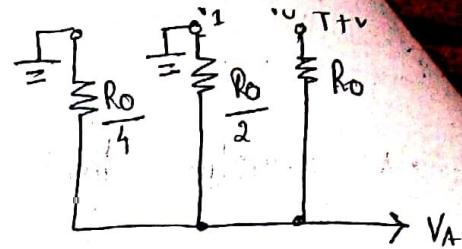


Fig. 3.10

Fig. 3.9

- Assume that the digital input signal 001 is applied to this network.
- Recalling that 0 = 0V and 1 = +V, we can draw the equivalent circuit as shown in fig 3.10
- Resistance R_L is considered large and is neglected. The analog output voltage V_A can be most easily found by use of Millman's theorem, which states that voltage appearing at any node in a resistive network is equal to the summation of the currents entering the node divided by the summation of the conductances connected to the node.

→ In equation form, Millman's theorem is

$$V = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3 + \dots}{1/R_1 + 1/R_2 + 1/R_3 + \dots}$$

- Applying Millman's theorem to fig. 3.10, in 3.10, we obtain

$$V_A = \frac{V_0/R_0 + V_1/(R_0/2) + V_2/(R_0/4)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)}$$

$$\Rightarrow V_A = \frac{\frac{1}{2}V_0 + \frac{1}{2}V_1 + \frac{1}{4}V_2}{\frac{1}{2}R_0 + \frac{1}{2}R_0 + \frac{1}{4}R_0} = \frac{\frac{1}{2}V_0 + \frac{1}{2}V_1 + \frac{1}{4}V_2}{\frac{5}{4}R_0} = \frac{1}{5}V$$

→ To summarize, a resistive divider can be used to change a digital voltage into an equivalent analog voltage. (8)

→ The following criteria can be applied to this divider:

1. There must be one input resistor for each digital bit.
2. Beginning with the LSB, each following resistor value is one-half the size of the previous resistor.
3. The full scale output voltage is equal to the positive voltage of the digital input signal.
4. The LSB has a weight of $1/(2^n - 1)$, where 'n' is the number of input bits.
5. The change in the output voltage due to change in the LSB is equal to $v/(2^n - 1)$, where 'v' is the digital input voltage level.
6. The output voltage V_A can be found for any digital input signal by using the following modified form of Millman's theorem:

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + \dots + V_{n-1} 2^{n-1}}{2^n - 1}$$

where $V_0, V_1, V_2 \dots V_{n-1}$ are the digital input voltage levels (0 or v) and 'n' is the no. of input bits.

Drawbacks of resistive divider:

1. Each resistor in the network has different value and hence more expensive.
2. Resistor used for the MSB is required to handle a much greater current than that used for the LSB resistor.

→ too large values, values type up to obtain more called a ladder has been developed.

Ex:2: For a 5-bit resistive divider, determine the following:

- a) the weight assigned to the LSB
- b) the weight assigned to the second & third LSB.
- c) the change in output voltage due to a change in the LSB, the second LSB, and the third LSB
- d) the output voltage for a digital input of 10101.

Assume $0 = 0V$ and $1 = +10V$.

Sol² a) The LSB weight is $\frac{1}{(2^n - 1)} = \frac{1}{(2^5 - 1)}$

$$= \underline{\underline{\frac{1}{31}}}$$

b) The second LSB weight is $2/31$, and the third LSB weight is $4/31$

c) The LSB causes a change in the output voltage of $10/31V$.
The second LSB causes an output voltage change of $20/31V$,
and the third LSB causes an output voltage change of $40/31V$.

d) The output voltage for a digital input of 10101 is

$$V_A = \frac{10 \times 2^0 + 0 \times 2^1 + 10 \times 2^2 + 0 \times 2^3 + 10 \times 2^4}{2^5 - 1}$$

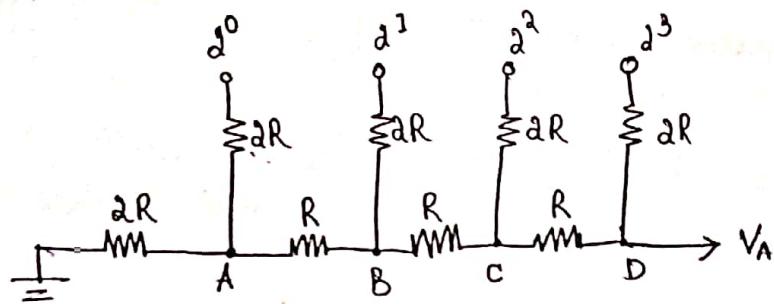
$$= \frac{10(1+4+16)}{31} = \underline{\underline{\frac{210}{31}}} = 16.77V$$

Binary Ladder:

→ The binary ladder is a resistive network whose output voltage is a properly weighted sum of the digital inputs

→ such a ladder, designed for 4-bits is shown in fig. 7

4. a

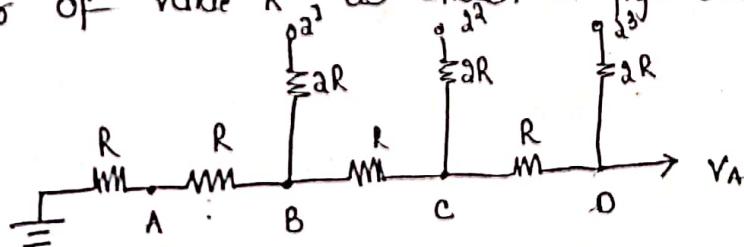


→ It is constructed of resistors that have only two values & thus overcomes one of the objections to the resistive divider discussed previously.

→ The left end of ladder is terminated in a resistance of $2R$ and the right end is open-circuited.

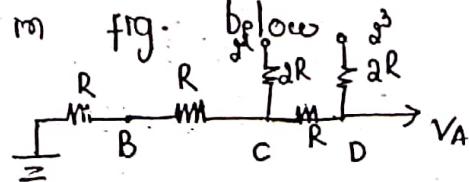
→ Examining the resistive properties of the network

i) All digital inputs are at ground. Beginning at node A, the total resistance looking into the terminating resistor is $2R$. The total resistance looking out toward the a^0 input is also $2R$. These two resistors can be combined to form an equivalent resistor of value R , as shown in fig. below

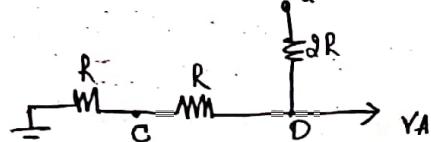


ii) Moving to node B, the total resistance looking into the branch toward node A is $2R$, as is the total resistance looking out toward the a^1 input.

These two resistors can be combined to simplify the network as shown in fig. below

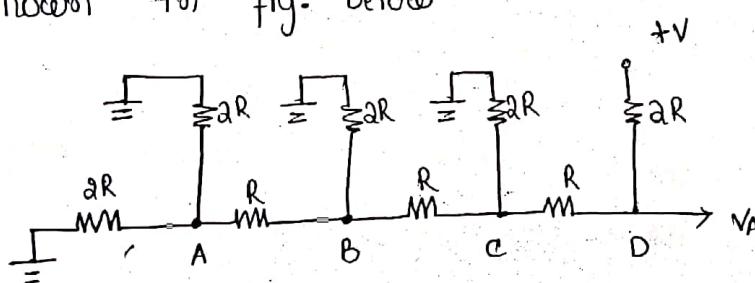


iii) Similarly, for node C, a^2

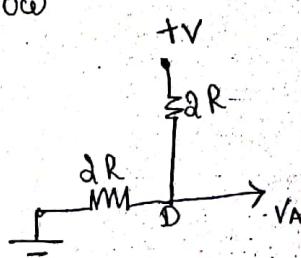


iv)

- From this equivalent circuit, it is clear that the resistance looking back toward node C is αR , as is the resistance looking out toward the A^3 input.
- To summarize, the total resistance looking from any node back toward the terminating resistor or out toward the digital input is αR .
- This is true regardless of whether the digital inputs are at ground or +V.
- The resistance characteristics of the ladder can be used to determine the output voltages for the various digital inputs.
- With various input signals, the binary ladder can be drawn as shown in fig. below



- Since there are no voltage sources to the left of node D, the entire network to the left of this node can be replaced by a resistance of αR to form the equivalent circuit as shown in fig. below



- From this equivalent circuit, it can be easily seen that the output voltage is

$$V_A = V \times \frac{\alpha R}{\alpha R + \alpha R} = \frac{V}{2}$$

- Thus a 1 in the MSB position will provide an output voltage

of $\frac{+V}{2}$.

(10)

→ To determine the output voltage due to the second MBB, assume a digital input signal of 0100. This is represented as shown in fig. below.

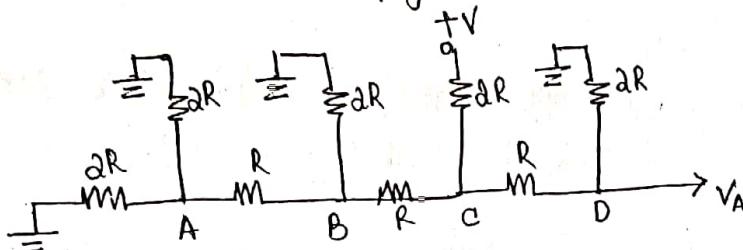


Fig (a)

→ Since there are no voltage sources to the left of node C, the entire network to the left of this node can be replaced by a resistance of $2R$, as shown in fig. below.

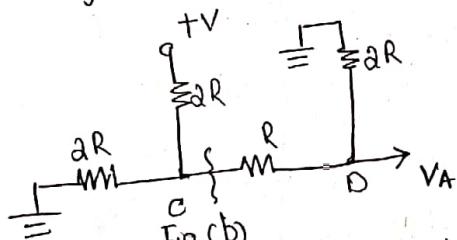


Fig (b)

→ Let us now replace the network to the left of node C with its Thvenin equivalent by cutting the circuit on the jagged line shown in fig (b).

→ The Thvenin equivalent is clearly a resistance R in series with a voltage source $\frac{+V}{2}$.

→ The final equivalent circuit with the Thvenin equivalent included is as shown in fig (c)

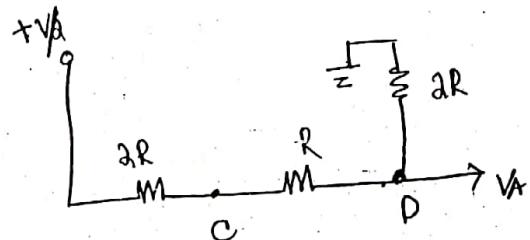


Fig. (c)

→ From this circuit, the output voltage is clearly

$$\begin{aligned} V_A &= \frac{+V}{2} \times \frac{2R}{R+R+2R} \\ &= \frac{+V}{2} \times \frac{2R}{4R} = \frac{+V}{2} \cdot \frac{1}{2} = \frac{+V}{4} \end{aligned}$$

→ This process can be continued, and it can be seen, the third MSB provides an output voltage of $+V/8$, the fourth MSB provides an output voltage of $+V/16$ and so on.

→ The output voltages for the binary ladder are summarized in fig. below.

→ Notice that each digital input is transformed into a properly weighted binary output voltage.

Bit position	Binary weight	Output voltage
MSB	$1/2$	$V/2$
2nd MSB	$1/4$	$V/4$
3rd MSB	$1/8$	$V/8$
4th MSB	$1/16$	$V/16$
n th MSB	$1/2^n$	$V/2^n$

→ In equation form, the output voltage is given by

$$V_A = \frac{V}{2} + \frac{V}{4} + \frac{V}{8} + \dots + \frac{V}{2^n} \quad \rightarrow (1)$$

where 'n' is the total number of bits at the input

→ Eqn (1) can be modified as

$$V_A = \frac{V_0}{2^0} + \frac{V_1}{2^1} + \frac{V_2}{2^2} + \dots + \frac{V_{n-1}}{2^{n-1}}$$

2^n

→ (a)

where v_0, v_1, v_2, \dots are the original input voltages. (11)

→ Eqn (a) can be used to find the output voltage from the ladder for any digital input signal.

Ex: 1) What are the output voltages caused by each bit in a 5-bit ladder if the input levels are $0 = 0V$ and $1 = +10V$.

$$\text{Sol: } \text{First MSB } V_A = \frac{V}{2} = \frac{10}{2} = 5V$$

$$\text{Second MSB } V_A = \frac{V}{4} = \frac{10}{4} = 2.5V$$

$$\text{Third MSB } V_A = \frac{V}{8} = \frac{10}{8} = 1.25V$$

$$\text{Fourth MSB } V_A = \frac{V}{16} = \frac{10}{16} = 0.625V$$

$$\text{Fifth MSB = LSB } V_A = \frac{V}{32} = 0.3125V$$

Ex: 2) Find the output voltage from a 5-bit ladder that has a digital input of 11010 . Assume that $0 = 0V$ and $1 = +10V$

$$\text{Sol: } V_A = \frac{v_0 2^0 + v_1 2^1 + v_2 2^2 + v_3 2^3 + v_4 2^4}{2^5}$$

$$= \frac{0 \times 2^0 + 1 \times 2^1 + 0 \times 2^2 + 10 \times 2^3 + 10 \times 2^4}{32}$$

$$= \frac{10(0 + 2 + 0 + 8 + 16)}{32}$$

$$= \frac{10 \times 26}{32}$$

$$\boxed{V_A = +8.125V}$$

Ex: 3) What is the full scale output voltage of the 5-bit ladder in example (2)

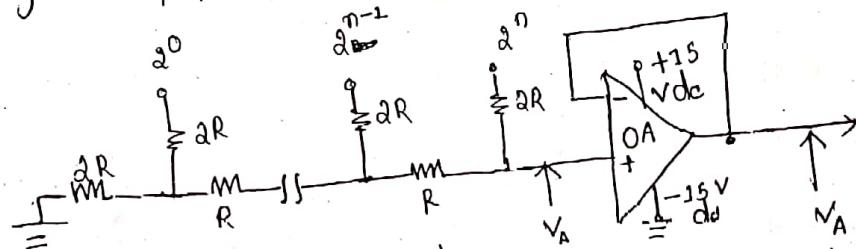
$$\text{Sol: } V = 5 + 2.5 + 1.25 + 0.625 + 0.3125 = +\underline{\underline{9.6875V}}$$

The full scale voltage is simply the sum of the individual bit voltages

→ The full scale voltage

$$V_A = V \left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \dots + \frac{1}{2^n} \right)$$

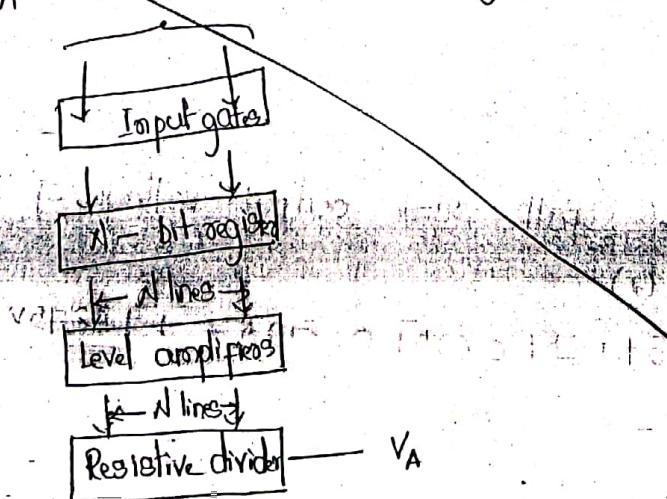
- To keep the ladder in perfect balance and to maintain symmetry, the output of the ladder should be terminated in a resistance of $2R$.
- The operational amplifier is connected as a unity gain non-inverting amplifier as shown in fig. below



- It has a very high input impedance, and the output voltage is equal to the input voltage.
- It is thus a good buffer amplifier for connection to the output of a resistive ladder.
- It will not load down the ladder and thus will not disturb the ladder output voltage V_A ; V_A will then appear at the output of the OA.

D/A converters:

- A complete D/A converter in block-diagram form is shown in fig. below



i) A/D converter: — Simultaneous conversion

→ The process of converting an analog voltage into an equivalent digital signal is known as analog-to-digital (A/D) conversion.

→ A/D conversion is complicated than D/A conversion

→ Simultaneous method or flash type is the simplest A/D converter

→ Simultaneous conversion type A/D converter using three comparative circuits is shown fig. below

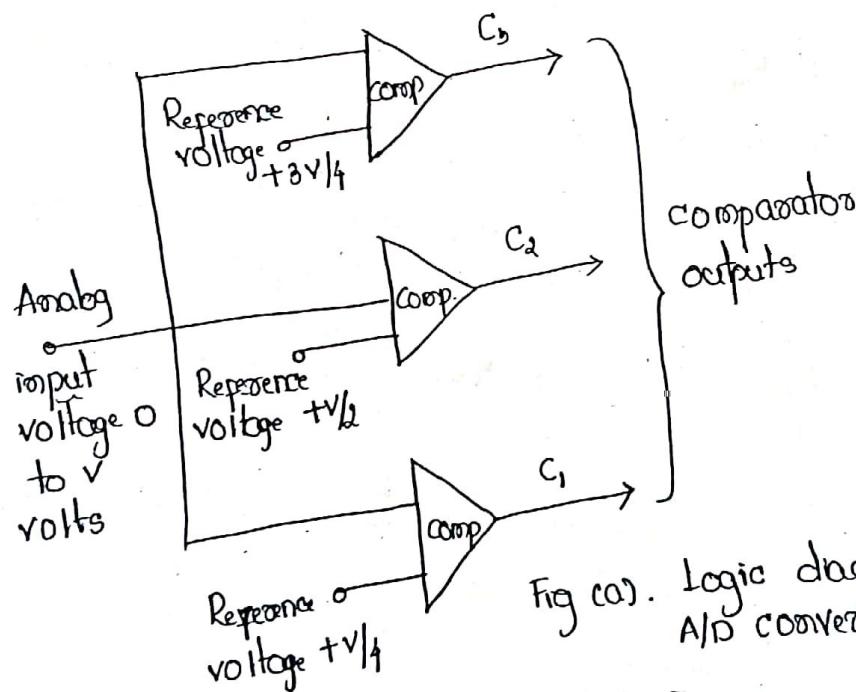
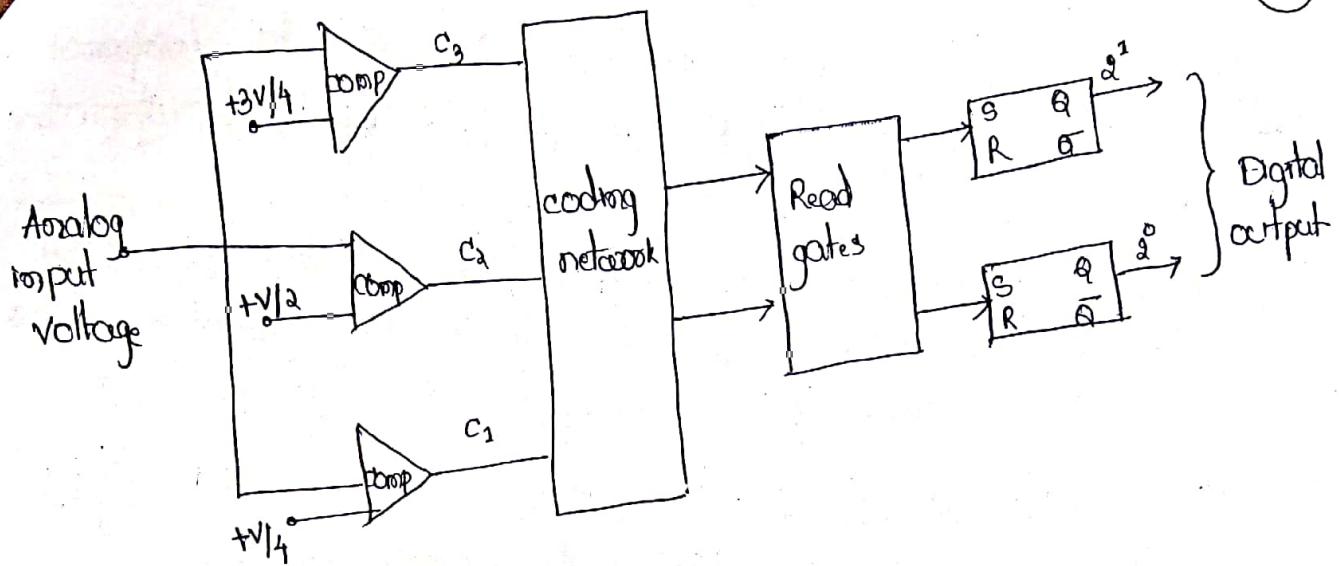


Fig (a). Logic diagram simultaneous A/D conversion

Input voltage	Comparator output		
	C_1	C_2	C_3
0 to $+V/4$	LOW	LOW	LOW
$+V/4$ to $+V/2$	HIGH	LOW	LOW
$+V/2$ to $+3V/4$	HIGH	HIGH	LOW
$+3V/4$ to $+V$	HIGH	HIGH	HIGH

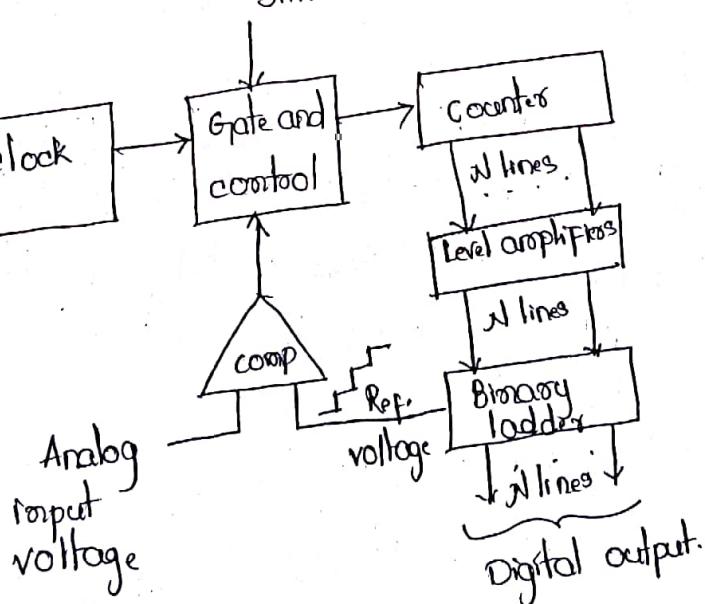
Fig. (b): Comparator outputs for input voltage ranges

- The analog signal to be digitized serves as one of the inputs to each comparator.
- The second input is a standard reference voltage. The reference voltages used are $+V_4$, $+V_2$, and $+3V_4$.
- The system is then capable of accepting an analog input voltage between 0 and $+V$.
- If the analog input signal exceeds the reference voltage to any comparator, that comparator turns on.
- Now, if all the comparators are off, the analog input signal must be between 0 and $+V_4$.
- The table illustrates the comparator output values for various ranges of input voltages.
- From the table, it is clear that there are four voltage ranges that can be detected by three converters.
- Four ranges can be effectively discerned by two binary digits (bits).
- Three comparators outputs can then be fed into a coding network to provide a bit which are equivalent to the input analog voltage.
- The bits of the coding network can then be entered into a flip-flop register for storage.
- The complete block diagram for such an A/D converter is shown in fig. below.



a) Counter-type ADC:

The block diagram of counter-type A/D converter is as shown in fig. below



The operation of the counter is as follows. First the counter is reset to all 0s.

Then, when a convert signal appears on the START line, the gate opens and clock pulses are allowed to pass through to the input of the counter.

The counter advances through its normal binary count sequence, and the staircase waveform is generated at the

output of the ladder.

- This waveform is applied to one side of the comparator and the analog input voltage is applied to the other side.
- When the difference voltage equals (or exceeds) the input analog voltage, the gate is closed, the counter stops and the conversion is complete.
- The number stored in the counter is now the digital equivalent of the analog input voltage.
- Notice that this converter is composed of a D/A converter (the counter, level amplifier, and binary ladder), one comparator, a clock, and the gate and control circuitry.
- This can be considered as a closed-loop control system. An error signal is generated at the output of the comparator by taking the difference between the analog input signal and the feedback signal (staircase reference voltage).
- The error is detected by the control circuit, and the clock is allowed to advance the counter. The counter advances in such a way as to reduce the error signal by increasing the feedback voltage.
- When the error is reduced to zero, the feedback voltage is equal to the analog input signal, the control circuitry stops the clock from advancing the counter, and the system comes to rest.
- The counter-type A/D converter provides a very good method for digitizing to a high resolution.

→ This method is much simpler than the simultaneous conversion time method. For high resolution, but the conversion time required is longer.

→ Since the counter always begins at zero and counts through its normal binary sequence, as many as 2^n counts may be necessary before conversion is complete. The average conversion time is, of course, $2^n/2 = 2^{n-1}$ counts.

→ The counter advances one count for each cycle of the clock, and the clock therefore determines the conversion rate.

→ For ex., for a 10-bit converter, 1024 clock cycles are required for a full scale count. If 1-MHz clock is used, the counter advances 1 count every microsecond. Thus, full scale counting requires $1024 \times 10^{-6} = 1.024 \text{ ms}$.

→ The converter reaches one-half full scale in half this time, or in 0.512 ms .

→ The time required to reach one-half full scale can be the average conversion time for a large number of conversions.

Ex: 1) Find the max. conversion time, average conversion time and max. conversion rate for 8-bit converter driven by 500-kHz clock.

sol: 1) Max. conversion time:

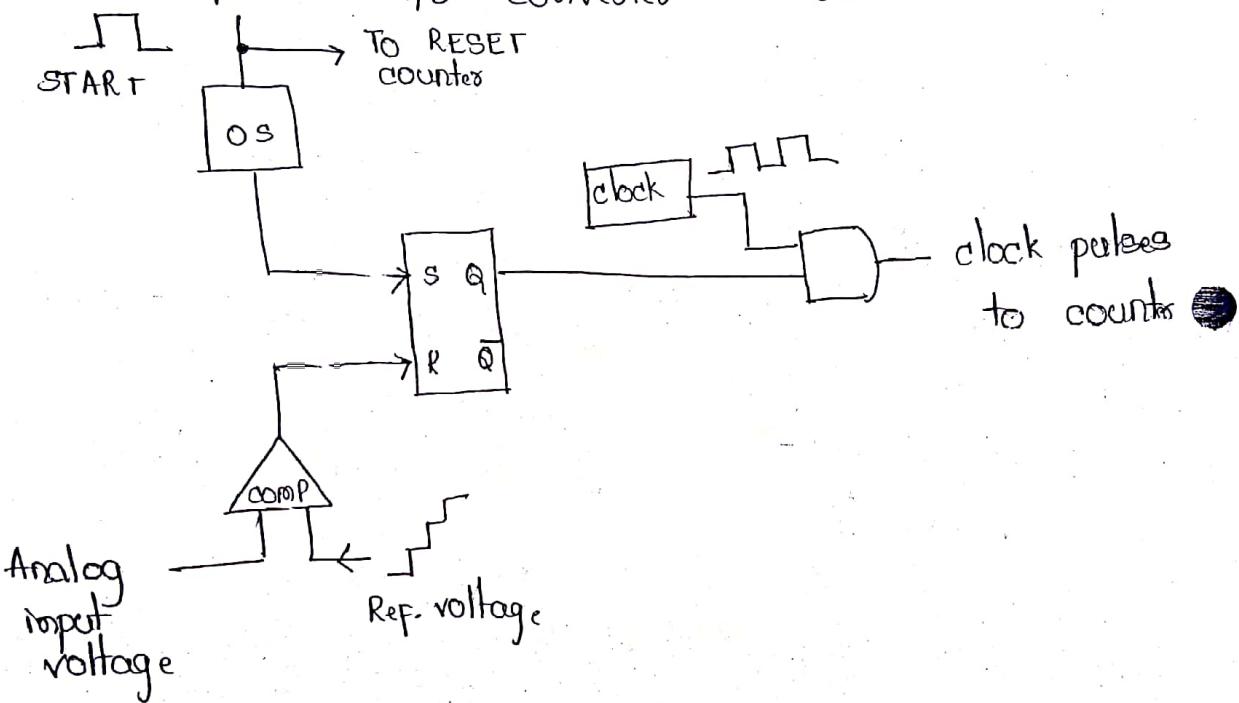
8-bit converter has a maximum of $2^8 = 256$ counts. 500-kHz clock advances at the rate of $(\frac{1}{500\text{kHz}})^{256}$. To advance 256 count requires $256 \times 2 \times 10^{-6} = 512 \text{ ns}$

ii) Average conversion time is half the maximum.

$$\text{time} := \frac{512 \text{ NS}}{2} = \underline{\underline{256 \text{ NS}}}$$

iii) Max. conversion rate = $\frac{1}{512 \text{ NS}} = 1953$ conversions per second.

→ Control of the A/D converter is as shown below

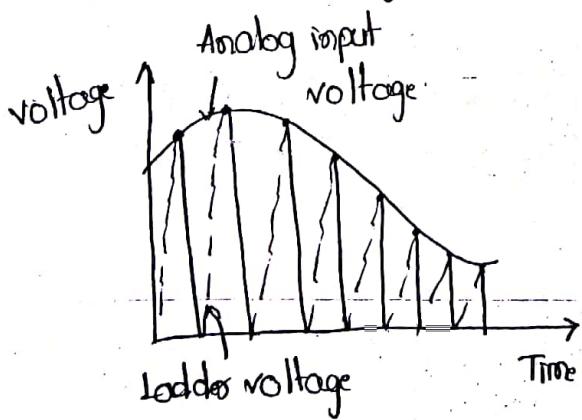


- The positive edge of START pulse is used to reset all the flip-flops in the counter and to trigger the one shot.
- The output of the one shot sets the control flip flop which makes the AND gate true and allows clock pulses to advance the counter.
- The delay between the RESET pulse to the flip-flops and the beginning of the clock pulses (ensured by the one shot) is to ensure that all flip-flops are idle before counting begins. This avoids racing problems.

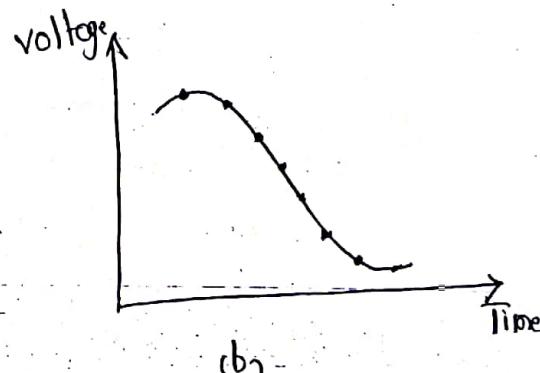
With the control flip-flop set, the counter advances through its normal count sequence until the staircase voltage from the ladder is equal to the analog input voltage. (16)

- At this time, the comparator output changes state, generating a positive pulse which resets the control flip-flop.
- Thus the AND gate is closed and counting ceases. The counter now holds a digital number which is equivalent to the analog input voltage.
- The converter remains in the state until another conversion signal is received.
- If a new start signal is generated immediately after each conversion is completed, the converter will operate at its maximum rate.

→ The converter could then be used to digitize a signal as shown in fig. below



(a)
Digitizing an analog voltage

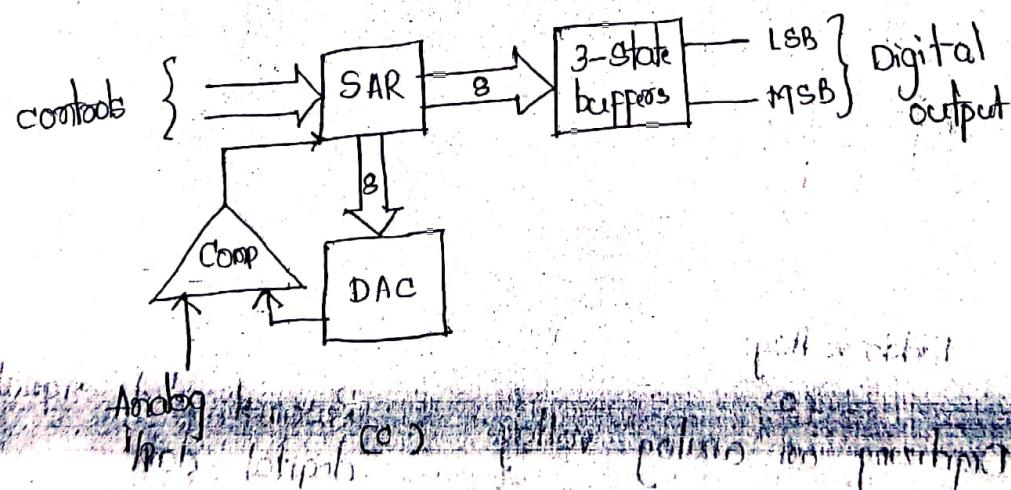
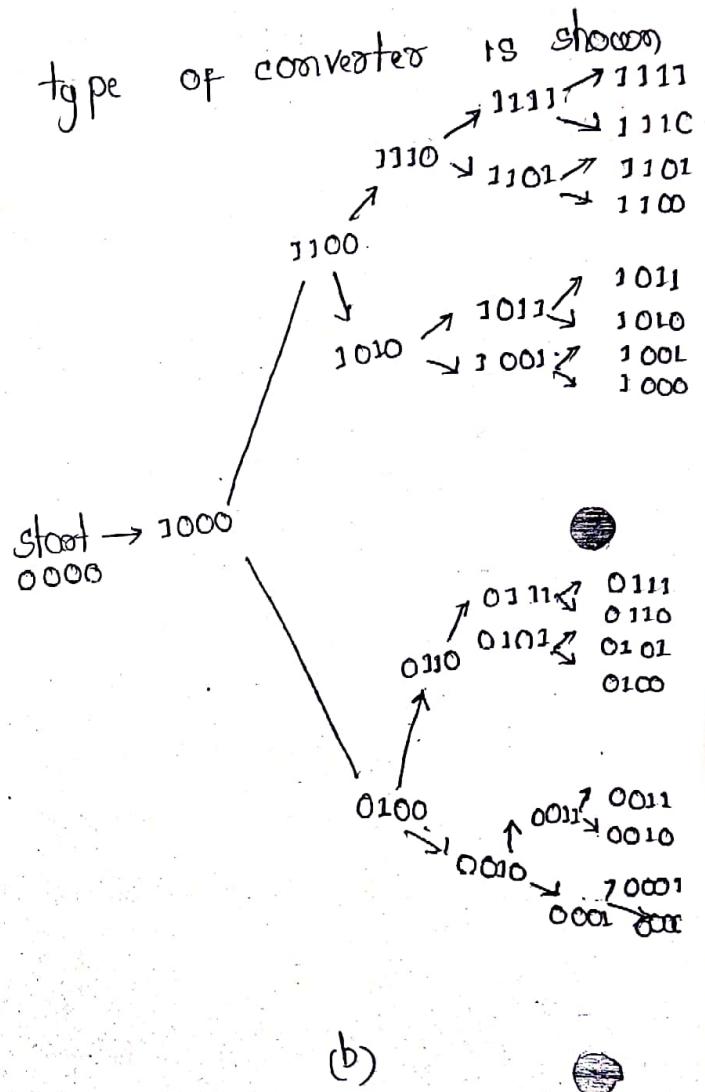
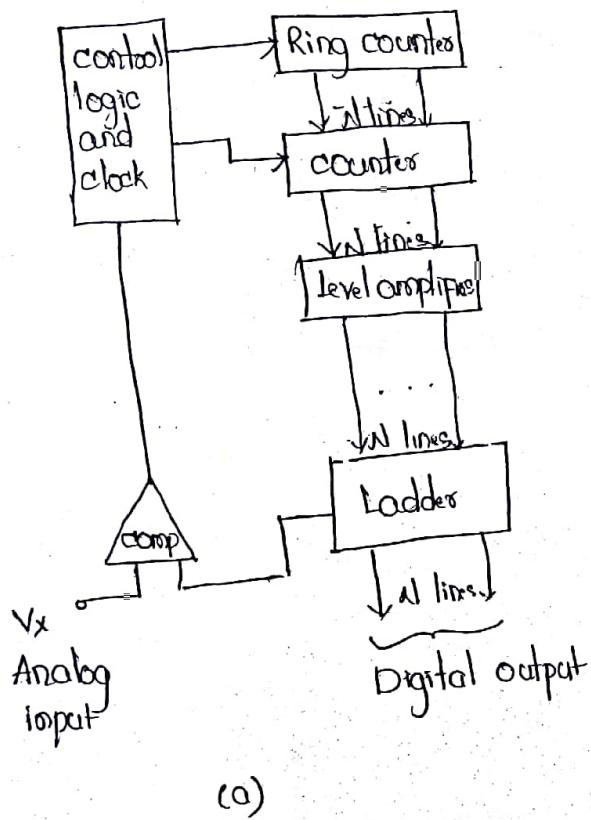


(b)
Reconstructed signal from the digital data

→ The conversion times in digitizing this signal are not constant but depend on the amplitude of the input signal.

3) Successive Approximation type ADC:

- If multiplexing is required, the successive approximation converter is most useful.
- The block diagram for this type of converter is shown in fig. below



The converter operates by successively dividing the voltage ranges in half.

(JF)

- The counter is first set to all 0s, and the MSB is then set. The MSB is then left in or taken out (by resetting the MSB flip-flop) depending on the output of the comparator.
- Then the second MSB is set in, and a comparison is made to determine whether to reset the second MSB flip-flop.
- The process is repeated down to the LSB, and at this time the desired number is in the counter.
- Since the conversion involves operating on one flip-flop at a time, beginning with the MSB, a ring counter may be used for flip-flop selection.
- The successive approximation method thus is the process of approximating the analog voltage by toying 1 bit at a time beginning with the MSB.
- The operation is shown in fig b. It can be seen that each conversion takes the same time and requires one conversion cycle for each bit.
- Thus the total conversion time is equal to the number of bits, n , times the time required for one conversion cycle.
- One conversion cycle normally requires one cycle of the clock.
- As an example, a 10-bit converter operating with a 1-MHz clock has a conversion time of $10 \times 10^{-6} = 10^{-5}$ sec.
- Other delays in the system such as switching time of the multiplexer, settling time of the ladder network, comparator delay, and settling time has to be considered.