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CS34/16IS/CS34

Third Semester B.E. Makeup Examination, January 2019
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours

Max. Marks: 100

Instructions:
1. *Accurate answers expected.*
2. *Unit I & Unit II are compulsory. Answer one full question from the remaining units*
3. *Data, if necessary, may be assumed.*
4. *Diagrams, when required, may be drawn.*

UNIT - I

			L	CO	PO	M
1	a.	Interpret Basic Operational concepts showing connections between the processor and memory with a neat block diagram.	(2)	(1)	(1)	(06)
	b.	Perform the following operations on the 5 bit signed numbers using 2's complement representation system. Analyze whether an overflow occurs. (i)(-10) + (-13) (ii)(-10) - (+4) (iii)(+7) - (-15) (iv)(+8) + (+10)	(4)	(1)	(1)	(08)
	c.	Define addressing mode and explain any four addressing modes with a suitable example.	(1,2)	(2)	(1)	(06)

UNIT – II

			L	CO	PO	M
2	a.	Analyze with a program that reads a line from the keyboard, stores in memory buffer, and echoes it back to the display.	(4)	(4)	(1)	(06)
	b.	Examine all three methods of handling multiple devices, with neat sketches and function.	(4)	(2)	(1)	(06)
	c.	Illustrate distributed bus arbitration, assume two devices, A and B, with ID's 5_{10} and 6_{10} (0101_2 and 0110_2) for the sake of explanation.	(2)	(2)	(2)	(08)

UNIT - III

			L	CO	PO	M
3	a.	Explain the internal organization of a memory chip for 1Kx1 memory chip, using decoder and multiplexer.	(2)	(3)	(1)	(10)
	b.	With internal organization diagram of a 2Mx8 dynamic memory chip, explain asynchronous DRAM's.	(2)	(3)	(1)	(10)

OR

4	a.	What is Cache? Explain any two cache mapping functions with neat sketches.	(1,2)	(3)	(1)	(10)
	b.	Summarize the memory hierarchy with respect to speed, size and cost.	(2)	(3)	(1)	(06)
	c.	Briefly summarize the different types of Read Only Memory (ROM).	(2)	(3)	(1)	(04)

UNIT - IV

			L	CO	PO	M
5	a.	Explain with block diagram: ADDER/SUBTRACTOR circuit. Explain how subtraction is achieved with an example.	(2)	(2)	(1)	(06)
	b.	Explain sequential circuit multiplication, using a suitable block diagram	(2)	(2)	(1)	(06)

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

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c. Solve for Quotient and Reminder, using Restoring Division Algorithm: 14 divide by 3.

	(3)	(4)	(2)	(08)
	L	CO	PO	M

OR

6 a. Define Bit-stage cell. Using Bit-stage cell explain a 4-bit binary Carry-Look-Ahead adder.

	(2)	(1)	(1)	(06)

b. Explain the non-restoring division algorithm Perform the division of number 8 by 3 (8÷3) using .the same.

	(2)	(2)	(1)	(08)

c. Solve for the product using Booth's Algorithm. (+15) x (-9)

	(3)	(4)	(2)	(06)
	L	CO	PO	M

UNIT -V

7 a. Define computer Architecture. Illustrate seven dimensions of an ISA.

	(1,2)	(4)	(1)	(10)

b. Explain the following in brief (i) Amdahl's Law (ii) Dependability

	(2)	(4)	(1)	(10)

OR

8 a. Demonstrate the working of a classic five stage pipeline for a RISC processor.

	(2)	(4)	(2)	(10)

b. Explain data hazards and methods to minimize data hazards with examples.

	(2)	(4)	(2)	(10)

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Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

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CS32/16CS/IS32

Third Semester B.E. Semester End Examination, Dec/Jan 2018-19

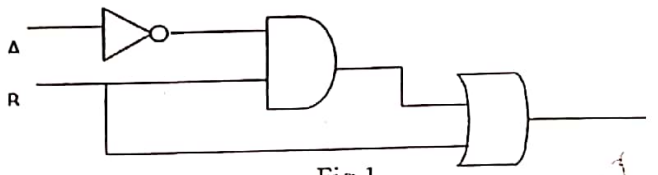
LOGIC DESIGN AND APPLICATIONS

Time: 3 Hours

Max. Marks: 100

Instructions: 1. *Unit I and III are compulsory.*
2. *Answer one full question from remaining units.*

UNIT - I

			L	CO	PO	M
1	a.	Write the truth table for fig 1. And realize the same using NOR universal gate.  Fig.1.	(3)	(1)	(1)	(04)
	b.	Using K-map reduction technique, simplify the given expression and realize the circuit using basic gates. $F(w,x,y,z) = \sum m(0,2,4,6,8,10,12,14)+d(1,3,15)$	(3)	(1)	(2)	(08)
	c.	Apply Quine McClusky reduction method to simplify the given expression $F(w, x, y, z) = \sum m(1,3,5,7,9,11,13,15)+d(0,2)$	(3)	(1)	(2)	(08)

UNIT – II

			L	CO	PO	M
2	a.	Define a Demultiplexer and explain the working of a 1:4 Demultiplexer with a neat circuit diagram and truthtable.	(2)	(2)	(1)	(06)
	b.	Illustrate and design an odd parity generator for 3 bit binary data with a neat diagram.	(3)	(2)	(2)	(06)
	c.	Distinguish between a Decoder and a Demultiplexer and realize the following Boolean functions using 3:8 Decoder and OR gates. $F1(A,B,C) = \sum m(1,2,4,7)$ $F2(A,B,C) = \sum m(0,3,5,6)$	(3)	(2)	(1)	(08)

OR

			L	CO	PO	M
3	a.	Design a 2 bit Magnitude comparator with a truth table and a neat logic diagram.	(3)	(2)	(1,4)	(08)
	b.	With a neat circuit diagram illustrate the working of a Full adder and write the Boolean expressions for the outputs.	(2)	(2)	(2)	(06)
	c.	Make use of PLA to implement the following Boolean functions. $F1(A,B,C) = \sum m(4,5,7)$ $F2(A,B,C) = \sum m(3,5,7)$	(3)	(2)	(1)	(06)

UNIT - III

4	a.	Realize the SR flip flop using NAND gates. Explain its working with help of truth table.	(3)	(3)	(1)	(06)
	b.	Explain working of (i) gated JK flip flop (ii) gated D flip flop	(2)	(3)	(1)	(06)
	c.	Derive the characteristic equations for SR, JK flip flops with state transition diagram and write the excitation tables.	(3)	(3)	(2)	(08)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

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UNIT - IV

			L	CO	PO	M
5	a.	Analyze the given sequential circuit and write the state analysis table and state transition diagram shown in fig 5a.	(4)	(3)	(2)	(06)

Fig 5a

	b.	Explain with neat waveform Johnson counter.	(2)	(3)	(1)	(06)
	c.	Design a MOD-5 synchronous counter using JK flip flop. Draw the logic diagram for the same.	(3)	(3)	(2)	(08)

OR

6	a.	Show how SR flip flop is converted to JK flip flop.	(2)	(3)	(2)	(06)
	b.	With a neat diagram and waveform explain MOD 8 (3-bit) asynchronous counter using JK flip flops.	(2)	(3)	(1)	(06)
	c.	Explain SISO and PISO types of shift registers with neat diagrams.	(2)	(3)	(1)	(08)

UNIT -V

			L	CO	PO	M
7	a.	With neat sketch explain the working of 4 bit R-2R binary ladder DAC.	(2)	(3)	(1)	(06)
	b.	Determine the output voltages for the inputs 11000 and 10010 if Logic 0=0V and 1=+10V.	(2)	(3)	(2)	(06)
	c.	Explain the working of successive approximation ADC with neat circuit diagram.	(2)	(3)	(1)	(08)

OR

8	a.	Explain the working of 2 bit parallel comparator A/D Converter with neat circuit diagram.	(2)	(3)	(1)	(08)
	b.	With neat sketch explain the working of 4 bit R-2R binary ladder DAC.	(2)	(3)	(1)	(08)
	c	Define resolution of D/A converter. What is resolution for 8 bit DAC if V=+5V.	(1)	(3)	(1)	(04)

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16CS/IS35

Third Semester B.E. Semester End Examination, DEC/JAN 2018-19

DATA STRUCTURES USING C

Time: 3 Hours

Max. Marks: 100

Instructions:
1. *UNIT I and UNIT II are compulsory.*
2. *Answer any one full question from remaining units.*
3. *Write assumptions for the programs if any.*
4. *Write comments and sample input/output where ever required.*

			L	CO	PO	M
		UNIT - I				
1	a.	Illustrate the use of pointer to pointer with program example.	(2)	(2)	(3)	(05)
	b.	List out the differences between Structures and Unions	(2)	(3)	(1)	(06)
	c.	Write a C program to read and print the student records.Name, USN,sem,marks of 3 subjects are read from the user. Calculate the average and print the result with appropriate headings. Calculate for `n` number of students. Use appropriate data structure.	(3)	(1)	(3)	(09)
		UNIT – II	L	CO	PO	M
2	a.	Differentiate between stack and queue.	(2)	(1)	(1)	(04)
	b.	What are the limitations of linear queue? Give alternate approach to overcome these limitations of linear queue with the help of code for insert and delete operations.	(2)	(2)	(2)	(06)
	c.	i. Convert the following infix expression to its postfix forms, show the conversion steps using tabulation method ((A+B)/C-((D*(E-F))/G))*Y ii. Evaluate the following postfix expression, show the evaluation steps using tabulation method and also write a final value of expression. 6 8 4 * 3 + 6 / - 9 + 3 - 4 +	(3)	(1)	(2)	(10)
		UNIT - III	L	CO	PO	M
3	a.	Write a C function for the following – (i) Insert a node at the front end of the singly linked list. (ii) Delete a node from the rear end of the singly linked list. (iii) Display the contents of the singly linked list	(3)	(1)	(2)	(09)
	b.	Explain the following with help of C code and example diagram- (i) Concatenate two singly linked lists. (ii) Reverse the given list without creating new node.	(3)	(2)	(2)	(06)
	c.	Write a C code for the following operation on circular singly linked list- (i) Insert a node at the front end. (ii) Deletion of a node at the rear end.	(3)	(2)	(2)	(05)
		OR				
4	a.	List out the differences between singly linked list and doubly linked list.	(2)	(3)	(1)	(03)
	b.	Illustrate the following using Doubly Linked list with C-Code. (i) Insert a node at front end. (ii) Insert a node at rear end. (iii) Delete a node from rear end. (iv) Delete a node from front end.	(2)	(2)	(3)	(08)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

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c. Consider a scenario where singly linked list contains the nodes 10,15,25,30,45,50. Insert node with data 12 at the front end. Insert node with data 55 at the front end. Delete a node from the rear end. Explain the insertion and deletion process step by step using appropriate code and diagram.

(3) (1) (3) (09)

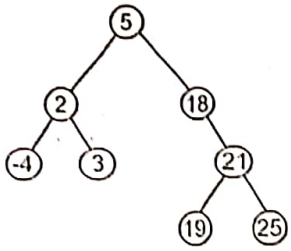
L CO PO M

UNIT - IV

5 a. Write a function in C to insert a node at proper position in a sorted list of integer numbers in ascending order implemented using doubly linked list.

(3) (2) (3) (06)

b. Write recursive functions for tree traversals and trace the functions using following tree:



(3) (4) (3) (08)

c. What is heap? Construct a max heap for the following set of numbers and show all the steps of construction: 56,34,78,44,22,38,74,89,100,99,200.

(3) (4) (3) (06)

OR

6 a. Prove the following properties of Binary Tree:

i. The maximum number of nodes on level "i" of a binary tree is 2^{i-1}, $i \geq 1$.

ii. The maximum number of nodes in a binary tree of depth "k" is 2^k-1, $k \geq 1$.

(3) (4) (1) (06)

b. How binary tree can be stored in array? Explain with the help of example.

(2) (4) (1) (06)

c. Write a function in C to insert a node in a binary search tree and trace the function for the following set of inputs 56,34,78,44,22,38,74,89,100,99,200.

(3) (3) (3) (08)

L CO PO M

UNIT -V

7 a. Define Graph. With example discuss how the graph is represented using adjacency matrix.

(2) (3) (3) (08)

b. Write a C function which illustrates Depth First Search Concept.

(2) (3) (3) (06)

c. Define spanning tree. Explain in detail with simple example.

(2) (1) (1) (06)

OR

8 a. Write a C program which illustrates Breadth First Concept.

(2) (3) (3) (08)

b. Explain in detail DFS with example.

(3) (2) (2) (06)

c. What is minimum cost spanning tree? Explain in detail with simple example.

(2) (4) (2) (06)

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16CS/IS32

Third Semester B.E. Makeup Examination, January 2019

LOGIC DESIGN AND APPLICATIONS

Time: 3 Hours

Max. Marks: 100

Instructions: 1. *Unit I and Unit III are compulsory*
2. *Answer One complete question from remaining UNITS*
3. *Assume missing data if any*

UNIT - I

			L	CO	PO	M
1	a.	Simplify the following Boolean Expression and draw the logic circuit using NAND gates only. Assume inverted input is available. $Y = A + A'B + AB$	(3)	(1)	(1)	(06)
	b.	Apply K-Map reduction technique to obtain the reduced SOP expression for the given Boolean function. $F(A,B,C,D) = \sum m(0,1,5,9,13,14,15) + d(3,4,7,10,11)$	(3)	(1)	(2)	(06)
	c.	Solve the given Boolean function by using Quine Mc Clusky method and find all the essential prime implicants. $F(A,B,C,D) = \sum m(0,1,2,3,10,11,12,13,14,15)$	(3)	(1)	(2)	(08)

UNIT – II

			L	CO	PO	M
2	a.	Design a suitable decoder for the given SOP functions $F1(A,B,C)=\sum m(0,1,4,5)$ $F2(A,B,C)=\sum m(2,5,7)$ $F3(A,B,C)=AB + A'B'$	(3)	(2)	(2)	(06)
	b.	Design 1 bit magnitude comparator	(3)	(2)	(2)	(08)
	c.	Define demultiplexer. Explain the working of 1 to 4 demultiplexer with neat circuit diagram.	(2)	(2)	(2)	(06)

OR

3	a.	Differentiate between PAL and PLA. Realize full adder using suitable size PAL.	(3)	(2)	(2)	(06)
	b.	Explain the working of parity generator and parity checker with suitable examples.	(2)	(2)	(2)	(06)
	c.	Design the following circuits using basic logic gates (i) Full adder circuit (ii) Half Subtracter circuit	(3)	(2)	(1)	(08)

UNIT – III

			L	CO	PO	M
4	a.	Define system clock, explain the characteristics of an ideal clock.	(1,2)	(2)	(1)	(06)
	b.	Explain the working of a JK flip flop with a neat circuit diagram..	(2)	(2)	(1,4)	(06)
	c.	Derive the characteristic equations for JK, SR, T and D flip flops and draw state transition diagrams for each.	(3)	(2)	(1,4)	(08)

UNIT - IV

			L	CO	PO	M
5	a.	Differentiate between synchronous and asynchronous counters. Construct a 4 bit ripple counter using JK flip flops and show the timing diagram.	(3)	(3)	(2)	(10)
	b.	Design a circuit for mod 7 synchronous up counter using JK flip flop	(3)	(3)	(2)	(10)

Note: L (Level), CO (Course Outcome), PO (Programme Outcome), M (Marks)

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OR

			L	CO	PO	M
6	a.	Explain the working of (i) SISO (ii) PIPO with waveform.	(2)	(3)	(1)	(06)
	b.	Explain the working of (i) Jhonsons counter (ii) Serial Adder	(2)	(3)	(1)	(08)
	c	Convert SR flip flop into D flip flop.	(3)	(3)	(2)	(06)

UNIT -V

			L	CO	PO	M
7	a.	Define Resolution and Accuracy of Digital to Analog converter. What is the Resolution of 10 bit for ladder type DAC? What is voltage resolution if full scale output is +5volts?	(1)	(3)	(1,4)	(06)
	b.	Explain 4-bit R-2R ladder Digital to Analog converter.	(2)	(3)	(1,4)	(06)
	c.	With a neat diagram explain 2-bit parallel comparator type Analog to digital converter. How many comparators are required for 4-bit ADC?	(2,1)	(3)	(1,4)	(08)

OR

			L	CO	PO	M
8	a.	Explain 2-bit Simultaneous A/D converter with a neat block diagram.	(2)	(3)	(1)	(06)
	b.	Explain the working of Successive Approximation ADC and find out the conversion time of a 12-bit Successive Approximation A/D converter using 1 MHZ clock.	(1,2)	(4)	(1,4)	(06)
	c.	Explain 3-bit R-2R ladder DAC. What is the output for 5-bit DAC when input is 11000 and voltage v = +5v.	(2)	(3)	(1,4)	(08)

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CS34/16CS/IS34

Third Semester B.E. Semester End Examination, Dec/Jan 2018-19
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours

Max. Marks: 100

Instructions: 1. *UNIT-I and UNIT-II are compulsory*
2. *Answer any one full question from remaining units*

UNIT - I

			L	CO	PO	M
1	a.	With the block diagram showing connection between the processor and memory, explain the functions of MAR and MDR.	(2)	(1)	(1)	(06)
	b.	List first 8 generic addressing modes, brief about - name of address mode-syntax-addressing functioncontaining effective address (EA), for each one.	(1)	(2)	(1)	(06)
	c.	For two computers R and C, with same execution time (T) and clock rate (R), solve for largest allowable value of number of instructions (N), if the effective value of basic steps (S) is 1.2 for computer R and 1.5 for computer C. Given that number of instructions (N) for computer R is 10.	(3)	(3)	(2)	(08)

UNIT – II

			L	CO	PO	M
2	a.	With neat sketches explain a method for handling interrupts from multiple devices	(2)	(2)	(1)	(10)
	b.	What is DMA? Explain in brief the simple arrangement for a centralized bus arbitration approach.	(1,2)	(2)	(1)	(10)

UNIT - III

			L	CO	PO	M
3	a.	Explain Synchronous DRAM with a block diagram.	(2)	(2)	(1)	(06)
	b.	Compare precisely ROM family: PROM, EPROM, EEPROM, Flash Memory, Flash Cards, Flash Drives	(2)	(1)	(1)	(06)
	c.	Assume you have 32 bit addresses, 32 KB of cache, 64 byte lines and 4 way set associative. Demonstrate with a block diagram.	(2)	(4)	(2)	(08)

OR

			L	CO	PO	M
4	a.	Illustrate organization of 1K x 1 memory chip for semiconductor RAM.	(2)	(4)	(2)	(06)
	b.	Compare the parameters: Speed, Size and Cost of memory hierarchy.	(2)	(1)	(1)	(06)
	c.	Explain Direct mapped cache for 128 blocks of 16 words each, a total of 2048(2K) words with 16 – bit address bus.	(2)	(4)	(2)	(08)

UNIT - IV

			L	CO	PO	M
5	a.	Explain the design of 4-bit Carry Look Ahead adder.	(2)	(3)	(2)	(08)
	b.	Multiply (+14) and (-6) using Booth's algorithm.	(3)	(3)	(2)	(07)
	c.	Perform the division of number 8 by 3 (8÷3) using restoring division method.	(3)	(3)	(2)	(05)

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

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OR

6 a. Explain sequential circuit binary multiplier with an example. (2) (3) (2) (10)

b. Explain the non-restoring division algorithm Perform the division of number 8 by 3 (8÷3) using.the same. (2) (3) (2) (10)

L CO PO M

UNIT -V

7 a. Explain the following with respect to classes of parallelism and parallel architecture:

a. Types of parallelism in applications
b. Major ways of parallelism.
c. Categories of data-level parallelism. (2) (2) (1) (10)

b. Interpret computer performance, with respect to

a. Measuring with three kinds of benchmarks
b. Reporting performance results
c. Summarizing performance results (2) (2) (1) (10)

OR

8 a. Explain seven dimensions of an ISA. (2) (2) (1) (10)

b. Exemplify,

a. data hazard with an example
b. how it is minimized by forwarding (or bypassing or short circuiting) (2) (2) (1) (10)

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Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (M...

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16CS/IS35

Third Semester B.E. Makeup Examination, January 2019

DATA STRUCTURES USING C

Time: 3 Hours

Max. Marks: 100

Instructions:
1. *UNIT-I and UNIT-II are compulsory.*
2. *Answer any one question from remaining units.*
3. *Write comments in the program wherever necessary.*
4. *Draw necessary diagrams wherever necessary.*

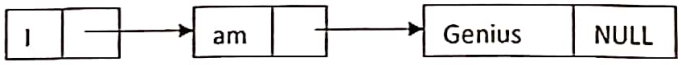
UNIT - I

			L	CO	PO	M
1	a.	What is pointer in C? Explain the concept of Null pointer and dangling pointer?	(2)	(2)	(1)	(06)
	b.	What is structure in C? How it is different from union? Exemplify different ways of declaring structures and unions in C.	(1)	(1)	(1)	(06)
	c.	Consider an application in which data related to set of "N" people applying for ration card is captured in an array of structures which includes name, age, aadhar number and annual income. Write a function in C which receives this array as argument and return the memory address of the structure containing information of a person whose annual income is minimum among all people.	(3)	(2)	(3)	(08)

UNIT – II

			L	CO	PO	M
2	a.	Explain the conceptof stack using dynamic arrays. Write C function for Push and Pop operations for the same..	(2)	(2)	(1)	(06)
	b.	Convert the following infix expression to postfix expression form using tabular method (i) (A + B – (C*(A+B)/D)) (ii) ((2+3)*5)-(8/2)	(3)	(1)	(1)	(08)
	c.	Write C functions for the various operations that are performed on the stack.	(2)	(1)	(3)	(06)

UNIT - III

			L	CO	PO	M
3	a.	Discuss the disadvantages of arrays. How they are overcome using linked list?	(2)	(2)	(1)	(06)
	b.	Write a function in C to find duplicate nodes in a linked list and delete them assuming the linked list is already created, it has minimum of 2 nodes and the nodes are arranged in ascending order.	(3)	(2)	(3)	(06)
	c.	Write a function in C to reverse the linked list which contains string as information. Display contents of the list after reverse operation. Example :  Output: Genius am I	(3)	(2)	(3)	(08)

OR

4	a.	Insertion and deletion operations on linked list are efficient compared to arrays. Justify the above statement.	(2)	(2)	(2)	(04)
	b.	Explain how polynomials are stored using linked list. With the help of example show the addition of two polynomials using linked list.	(2)	(2)	(2)	(08)

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

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c. Write a functions in C to perform following operation with singly linked list:
   i. Insert a node at front
   ii. Insert a node at rear
   iii. Delete a node with specific key element.
   iv. Display the contents of list.

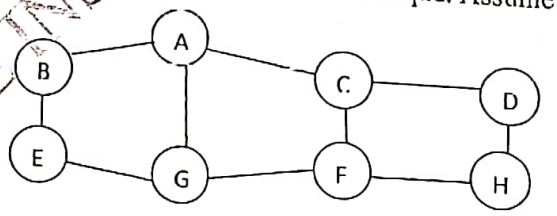
			(3)	(2)	(3)	(08)

UNIT – IV

			L	CO	PO	M
5	a.	Write a C functions for different tree traversal techniques.	(3)	(1)	(3)	(09)
	b.	Construct a Binary search tree for the following data explaining each step- (i) 100,50,60,125,69,110,101,59,68 (ii) 210,56,200,220,226,229,98,75,80	(2)	(3)	(2)	(06)
	c.	What are heaps? Build a max heap for the following set of numbers 75,90,30,25,50,95. Show all intermediate steps for the heap construction.	(3)	(4)	(1)	(05)
		OR				
6	a.	Explain the following terms with respect to binary tree with example- (i) Siblings (ii) Ancestors (iii) Level (iv) Leaf node (v) Root (vi) Degree.	(2)	(1)	(3)	(06)
	b.	Construct the Binary search tree for the given traversals INORDER-WSXQYTZPURV PREORDER-PQSWXTYZRUV	(2)	(3)	(2)	(06)
	c.	Explain min-heap in detail with example.	(3)	(2)	(2)	(08)

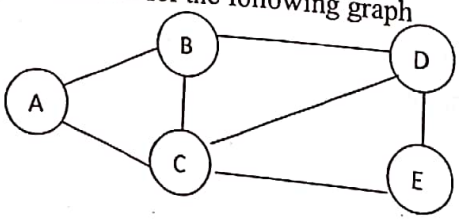
UNIT –V

			L	CO	PO	M
7	a.	Explain any two methods of representation of graph with example	(2)	(4)	(1)	(06)
	b.	Write BSF algorithm and trace the same for one input graph.	(2)	(4)	(3)	(06)
	c.	Traverse the graph given below using DFS technique. Assume A as a source node.				



OR

8	a.	What is spanning tree? Discuss with example and also give its applications.	(3)	(4)	(2)	(08)
	b.	Give adjacency list representation for the following graph	(2)	(3)	(1)	(06)



Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

			(3)	(4)	(2)	(06)

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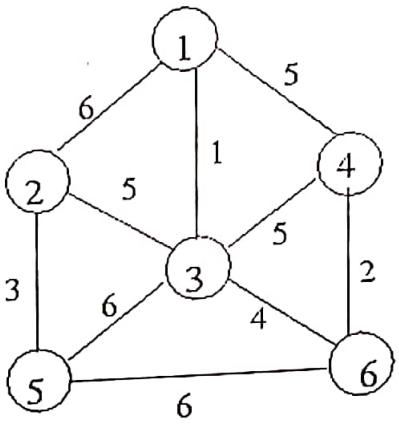
c. Find the minimum cost spanning tree for the following graph:



(3) (3) (3) (08)

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16MAT31/MAT31

Third Semester B.E. Makeup Examination, January 2019

STATISTICAL-NUMERICAL-FOURIER TECHNIQUES / ENGINEERING MATHEMATICS - III

Time: 3 Hours

Max. Marks: 100

Instructions: 1. *UNIT III and V are compulsory.*
2. *Answer any one question from remaining each unit.*

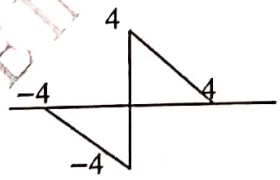
UNIT - I

			L	CO	PO	M
1	a.	Use Regula falsi method to extract the root of the equation $x + ln(x) - 2 = 0$ up to 4 decimals.	(2)	(1)	(1)	(6)
	b.	Apply Newton Raphson method to obtain the root of the equation $x - \operatorname{cosec} x = 0$ upto three decimals	(2)	(1)	(2)	(7)
	c.	Illustrate fixed point iteration method to find the positive root of the equation $x^3 + x - 1 = 0$ upto three decimals.	(2)	(1)	(1)	(7)

OR

2	a.	Use Taylors series method up to 5th derivative term to obtain y (0.1) for the differential equation $\frac{dy}{dx} = xy + 1$, $y(0) = 1$.	(2)	(1)	(2)	(6)
	b.	Apply Euler's modified formula to solve the differential equation $\frac{dy}{dx} = 2(1 + y^2)$, $y(0) = 0$ at h = 0.05 in 2 steps.	(3)	(1)	(1)	(7)
	c.	Illustrate Runge Kutta fourth order method to solve $\frac{dy}{dx} = \frac{4x}{y-xy}$, $y(0) = 3$, at $x = 0.2$.	(2)	(1)	(1)	(7)

UNIT – II

			L	CO	PO	M
3	a.	Construct Fourier series for the function $\begin{cases} x, & 0 \le x \le \pi \\ 2\pi - x, & \pi \le x \le 2\pi \end{cases}$	(3)	(2)	(1)	(6)
	b.	Test whether the function given below is even or odd or neither even nor odd. Find its Fourier series 	(2)	(2)	(1)	(7)
	c.	Represent the following functions in Fourier series up to first harmonic.	(2)	(2)	(1)	(7)

x	0	2	4	6	8	10	12
Y	9.0	18.2	24.4	27.8	27.5	22.0	9.0

OR

4	a.	Construct Fourier series for the function $f(x) = e^{-x}, -l \le x \le l$	(3)	(2)	(1)	(6)
	b.	Transform the given function $f(x) = (x-1)^2$, $0 < x < 1$ into half-range Fourier cosine series.	(2)	(2)	(1)	(7)

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c. Represent the following function in Fourier sine series up to second term.

θ	0	π/6	2π/6	3π/6	4π/6	5π/6
T	0	5.2224	8.097	7.850	5.499	2.626

(2) (2) (1) (7)
L CO PO M

UNIT - III

5 a. Evaluate Fourier transform of the function $f(x) = 1 - |x|$, $-1 \le x \le 1$. Hence deduce the value of $\int_0^\infty \frac{\sin^2 t}{t^2}\, dt$

(2) (3) (1) (6)

b. Solve the integral equation $\int_0^\infty f(\theta) \cos \alpha\theta \, d\theta = \begin{cases} 1-\alpha, & 0 \le \alpha \le 1 \\ 0, & \alpha > 1 \end{cases}$

(2) (3) (1) (7)

c. Evaluate Fourier Sine Transform of the function $f(x) = \frac{x}{1+x^2}$

(2) (3) (1) (7)
L CO PO M

UNIT - IV

6 a. If the following represents valid p.d.f. then calculate *k*, mean and standard deviation given

x	-2	-1	0	1	2	3
p(x)	0.1	k	0.2	2k	0.3	k

(2) (4) (1) (6)

b. Demonstrate that mean and variance of Poisson distribution are equal.

(2) (4) (1) (7)

c. Under the normal distribution the mean weight of 500 students during a medical examination was found to be 50 kgs and S.D weight 6 kgs. Find the number of students having weight.
(i) Between 40 kgs & 50 kgs (ii) more than 60 kgs given Ø(1.67) = 0.4525

(2) (4) (1) (7)

OR

7 a. If the following represents valid p.d.f. then calculate *k*, $p(1 < x < 2)$, $p(x \le 1)$, $p(x > 1)$, mean & variance . $f(x) = \begin{cases} kx^2, & 0 < x < 3 \\ 0, & otherwise \end{cases}$

(2) (4) (2) (6)

b. Fit a Binomial distribution for the following data and compare the theoretical frequencies with the actual once.

x	0	1	2	3	4	5
p(x)	2	14	20	34	22	8

(2) (4) (1) (7)

c. If the conversation on telephone is an Exponential variate with mean 3 min, calculate the probability that (i) conversation lasts for more than 1 min. (ii) conversation lasts between 1 and 2 min.

(2) (4) (1) (7)
L CO PO M

UNIT -V

8 a. The joint distribution of two random variables X and Y are given by

X \ Y	2	3	4
1	0.06	0.15	0.09
2	0.14	0.35	0.21

Determine the individual distributions of X and Y. Also verify whether X and Y are stochastically independent.

(2) (5) (1) (6)

b. A man's smoking habits are as follows. If he smokes filter cigarettes one week, he switches to non filter cigarettes the next week with probability 0.2.On the other hand if he smokes non filter cigarettes one week there is a probability of 0.7 that he will smoke non filter cigarettes the next week as well. In the long run how often does he smoke filter cigarettes?

(2) (5) (2) (7)

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

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c. Define a stochastic matrix. Find unit fixed probability vector for the stochastic matrix P.

$$P=\begin{bmatrix} 0 & \frac{1}{2} & \frac{1}{2} \\ \frac{1}{3} & \frac{2}{3} & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

(2) (5) (1) (7)

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16DIPMAT31

Third Semester B.E. Makeup Examination, January 2019

CALCULUS, FOURIER ANALYSIS AND LINEAR ALGEBRA

Time: 3 Hours Max. Marks: 100

Instructions: 1. *Questions from Unit II and Unit III are COMPULSORY.*
2. *Answer any ONE FULL question from each of the other units.*
3. *Max. Marks will be scaled to 50 marks for SGPA and CGPA calculations.*

			L	CO	PO	M
		UNIT - I				
1	a.	Find the Taylor's series of $f(x) = 2x^3 + 7x^2 + x - 6$ in the powers of $(x-1)$ upto fourth degree term.	(1)	(1)	(1)	(06)
	b.	For $u = e^{ax-by}\sin(ax+by)$, demonstrate that $b\frac{\partial u}{\partial x} - a\frac{\partial u}{\partial y} = 2abu$.	(1)	(1)	(1)	(07)
	c.	If $u = f(x-y, y-z, z-x)$, prove that $\frac{\partial u}{\partial x} + \frac{\partial u}{\partial y} + \frac{\partial u}{\partial z} = 0$.	(1)	(1)	(1)	(07)
		OR				
2	a.	Show that the curves $r = (1+\cos\theta), r = (1-\cos\theta)$ cut orthogonally	(1)	(1)	(1)	(06)
	b.	If $z = xy + yz + zx, x = at, y = 4at, z = 2at$ find the total derivative $\frac{dz}{dt}$. Express final answer in terms of t.	(1)	(1)	(1)	(07)
	c.	If $u = e^{xyz}$ then verify that $\frac{\partial^2 u}{\partial x \partial y} = \frac{\partial^2 u}{\partial y \partial x}$.	(1)	(1)	(1)	(07)
			L	CO	PO	M
		UNIT – II				
3	a.	Solve $\cos^2 x\frac{dy}{dx} + y = \tan x$.	(1)	(2)	(1)	(06)
	b.	Construct the orthogonal trajectory of the family of curves $r^n = a\sin(n\theta)$.	(2)	(2)	(1)	(07)
	c.	Solve $(D^2 - 6D + 9)y = 6e^{3x} + 7e^{-2x} - \log 2$	(1)	(2)	(1)	(07)
			L	CO	PO	M
		UNIT - III				
4	a.	Obtain Fourier Series of $f(x) = x^2$ in $(0, 2\pi)$.	(1)	(3)	(1)	(06)
	b.	Apply harmonic analysis to find Fourier Series up to first harmonic and also find the amplitude of first harmonic for the data:	(2)	(3)	(1)	(07)
	c.	Find the Fourier cosine transform of $f(x) = \begin{cases} 1; & 0 \le x \le 2 \\ 0; & x \ge 2 \end{cases}$	(1)	(3)	(1)	(07)
			L	CO	PO	M
		UNIT - IV				
5	a.	Apply Regula – Falsi method to find a real root of the equation $\cos x = 3x - 1$, correct upto three decimal places.	(1)	(4)	(1)	(06)

x	0	1	2	3	4	5
y	4	8	15	7	6	2

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b. Use Taylors's series method to obtain the approximate value of y at $x = 0.2$ for the differential equation $\frac{dy}{dx} = 2y + e^{3x}, y(0) = 0$ to find $y(0.2)$. Perform three iterations. (1) (4) (1) (07)

c. Apply Euler's Modified method to solve $y' = x + y,\ y(0) = 1$ at $y(0.4)$, take h = 0.2. (1) (4) (1) (07)

OR

6 a. Apply Newton - Raphson method to find a real root of the equation $x^3 - 3x + 4 = 0$, correct to three decimal places. (1) (4) (1) (06)

b. Apply fixed point iteration method to solve $sin(x) = e^{-x}$ by performing three iterations. (1) (4) (1) (07)

c. Apply Runge - Kutta method of fourth order to solve $\frac{dy}{dx} = 3x + y^2,\ y(1) = 1.2$ at $x = 1.1$. Execute three iterations. (1) (4) (1) (07)

UNIT -V

L CO PO M

7 a Find the rank of the matrix $\begin{bmatrix} 1 & 2 & 3 & 0 \\ 2 & 4 & 3 & 2 \\ 3 & 2 & 1 & 3 \\ 6 & 8 & 7 & 5 \end{bmatrix}$ by matrix operations. (1) (5) (1) (06)

b. Solve by Gauss – Jordan method the simultaneous linear equations $2x - 3y + z = -1,\ \ x + 4y + 5z = 24,\ \ 3x - 4y + z = -2$. (1) (5) (1) (07)

c. Use Rayleigh's method to find dominant eigenvalue and corresponding eigenvector of the matrix $\begin{bmatrix} 1 & 6 & 1 \\ 1 & 2 & 0 \\ 0 & 0 & 3 \end{bmatrix}$. Taking initial vector as $X^{(0)} = [1,\ 1,\ -1]^T$. Perform five iterations. (1) (5) (1) (07)

OR

8 a. For what value of λ the rank of the matrix $\begin{bmatrix} 1 & 2 & 1 \\ 1 & 3 & 4 \\ 3 & 6 & \lambda \end{bmatrix}$ will be equal to TWO. Use elementary transformations to establish. (1) (5) (1) (06)

b. Solve by Gauss – Seidel method the linear simultaneous equations

$2x + y + 6z = 9,\ \ 8x + 3y + 2z = 13,\ \ x + 5y + z = 7$. (1) (5) (1) (07)

c. Find all the eigenvalues and the eigenvectors of the matrix $\begin{bmatrix} 1 & 1 & 3 \\ 1 & 5 & 1 \\ 3 & 1 & 1 \end{bmatrix}$. (1) (5) (1) (07)

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16MAT31/MAT31

Third Semester B.E. Semester End Examination, Dec/Jan 2018-19
STATISTICAL-NUMERICAL-FOURIER TECHNIQUES / ENGINEERING MATHEMATICS - III

Time: 3 Hours

Max. Marks: 100

Instructions: *1. Units III and V are compulsory.*
2. Answer any one full question from remaining units.

UNIT - I

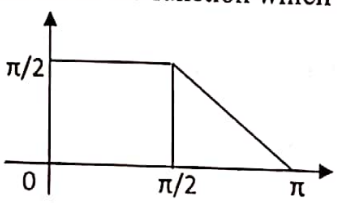
			L	CO	PO	M
1	a.	Compute the real root of the equation $x\log_{10}x-1.2=0$ by the method of false position. Carry out three iterations.	(2)	(1)	(1)	(07)
	b.	Using Runge-Kutta method of fourth order, find $y(0.2)$ for the equation $\frac{dy}{dx}=\frac{y-x}{y+x}$ with $y(0)=1$ taking $h=0.2$.	(1)	(1)	(1)	(07)
	c.	Find a real root of the equation $x^3+x+1=0$ by fixed point iteration method.	(1)	(1)	(1)	(06)

OR

2	a.	Find a real root of the equation $xe^x-\cos x=0$ applying Newton-Raphson's method correct to four decimal places.	(1)	(1)	(1)	(07)
	b.	Use modified Euler's method to solve $\frac{dy}{dx}=x+\lvert y\rvert$ in the range $0\le x\le 0.4$ by taking $h=0.2$ given that $y(0)=1$ initially.	(2)	(1)	(1)	(07)
	c.	Employ Taylor's series method to find y at $x=0.1$ and 0.2 correct to three places of decimal in step size of 0.1 for the linear differential equation $\frac{dy}{dx}-2y=3e^x$ with $y(0)=0$.	(1)	(1)	(1)	(06)

UNIT – II

			L	CO	PO	M
3	a.	Obtain Fourier expansion of $f(x)=\begin{cases}-\pi & -\pi<x<0\\ x & 0<x<\pi\end{cases}$. Hence deduce that $\sum\frac{1}{(2n-1)^2}=\frac{\pi^2}{8}$	(2)	(2)	(1)	(07)
	b.	Find the Fourier cosine series of the function which is expressed graphically as follows				



	c.	Obtain the Fourier series up to second harmonics to the following data.	(2)	(2)	(1)	(07)

x :	0	1	2	3	4	5
y :	4	8	15	7	6	2

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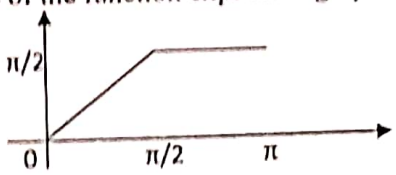
OR

4 a. Draw the graph of the function $f(x)=\begin{cases}\pi x & 0\le x\le 1\\ \pi(2-x) & 1\le x\le 2\end{cases}$ also find the Fourier expansion of $f(x)$

(2) (2) (1) (07)

b. Find half range sine series of the function expressed graphically



(2) (2) (1) (07)

c. Obtain the constant term and first three coefficients in the fourier cosine series of y using the following table

x:	0	1	2	3	4	5
y:	4	8	15	7	6	2

(1) (2) (1) (06)

L CO PO M

UNIT - III

5 a. Find the Fourier transform of $f(x)=\begin{cases}1-|x| & in\ |x|<1\\ 0 & otherwise\end{cases}$. Hence evaluate $\int_0^\infty \frac{\sin^2 x}{x^2}dx$.

(2) (3) (1) (07)

b. Find Fourier sine transform of $e^{-|x|}$. Hence evaluate $\int_0^\infty \frac{x\sin mx}{1+x^2}dx$.

(1) (3) (1) (07)

c. Find $f(x)$ given that $F_c\{f(x)\}=\frac{1}{1+s^2}$.

(2) (3) (1) (06)

L CO PO M

UNIT – IV

6 a. A random variable X has following probability function for various values of x

x:	0	1	2	3	4	5	6	7
y:	0	k	2k	2k	3k	k^2	$2k^2$	$7k^2+k$

(i) Find k (ii) Evaluate $p(x<6)$, $p(x\ge 6)$ and $p(3<x\le 6)$. Also find mean.

(1) (4) (1) (07)

b. Derive mean and standard deviation of binomial distribution.

(2) (4) (1) (07)

c. The marks of 1000 students in an examination follow normal distribution with mean 70 and standard deviation 5. Find the number of students whose marks will be (i) less than 65 (ii) more than 75 (iii) between 65 and 75.

(2) (4) (1) (06)

OR

7 a. Verify whether the function $p(x)=\begin{cases}6x(1-x) & ,0\le x\le 1\\ 0 & ,otherwise\end{cases}$

(i) is a probability density function or not and (ii) Also determine mean and standard deviation.

(1) (4) (1) (07)

b. While forming 36-digit binary numbers a malfunctioning digital computer is found to form a digit incorrectly about 1 times in 1000. Assuming the errors in forming different digits to be independent, find the probability of having (i) zero, (ii) one, (iii) more than one and (iv) less than five incorrect digits in a given 36-digit number.

(2) (4) (1) (07)

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c. Obtain the equation of the normal probability curve that may be fitted to the following data:

Variable (x) :	6	7	8	9	10	11	12
Frequency (f) :	3	6	9	13	8	5	4

(4) (4) (1) (06)
L CO PO M

UNIT-V

8 a. A joint probability distribution is given by the following table

X \ Y	−8	2	4
1	0.1	0.2	0.2
3	0.3	0.1	0.1

Find the marginal distribution of X and Y and Cov(X, Y). Are they independent?

(2) (5) (1) (07)

b. Assume that a computer system is in one of three states: busy, idle or undergoing repair denoted by states 0, 1, 2 respectively. It is found that the system approximately behaves like a Markov chain with the transition probability matrix $P=\begin{bmatrix} 0.6 & 0.2 & 0.2 \\ 0.1 & 0.8 & 0.1 \\ 0.6 & 0.0 & 0.4 \end{bmatrix}$. Prove that the chain is irreducible, and determine the steady state probability vector.

(2) (5) (1) (07)

c. Define i) State classification of Markov chain. (ii) covariance and correlation of X and Y.

(1) (5) (1) (06)

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16DIPMAT31

Third Semester B.E., Semester End Examination, Dec/Jan 2018-19

CALCULUS, FOURIER SERIES AND LINEAR ALGEBRA

Time: 3 Hours

Max. Marks: 100

Instructions: 1. UNIT II & III ARE COMPULSORY

			L	CO	PO	M
		UNIT - I				
1	a.	Using Taylor's series, express $2x^3 + 7x^2 + x - 6$ in powers of (x-1) upto fourth degree term.	1	1	1	(06)
	b.	Find the angle between polar curves $r = a(1 + \cos\theta)$ and $r = b(1 - \cos\theta)$.	2	1	1	(07)
	c.	If $u = f(x - y, y - z, z - x)$, then prove that $\frac{\partial u}{\partial x} + \frac{\partial u}{\partial y} + \frac{\partial u}{\partial z} = 0$.	2	1	1	(07)
		OR				
2	a.	Using Maclaurin's series, expand *sinx* upto the term containing x^4.	1	1	1	(06)
	b.	Find first and second partial derivatives of $z = \log(x^2 + y^2)$.	1	1	1	(07)
	c.	Find the total derivative of $u = xy + yz + zx$ at x = at, y = 4at and z = 2at, find $\frac{du}{dt}$.	1	1	1	(07)
		UNIT – II				
3	a.	Solve $\cos^2 x \frac{dy}{dx} + y = \tan x$.	1	2	1	(06)
	b.	Find the orthogonal trajectories of the family of parabolas $y^2 = 4ax$.	2	2	1	(07)
	c.	Solve $y'' - 2y' + 10y = 0$, given $y(0) = 4$, $y'(0) = 1$.	2	2	1	(07)
		UNIT - III				
4	a.	Obtain Fourier series for $f(x) = x^2$ in the interval $0 < x < 2\pi$.	1	3	1	(06)
	b.	Compute the first two harmonics of the Fourier series of f(x) given in the following table:	2	3	1	(07)
	c.	Find the Fourier sine transform of $e^{-\lvert x\rvert}$.	2	3	1	(07)
		UNIT - IV				
5	a.	Use Regula – falsi method to find the real root of the equation $xe^x = \cos x$, correct to three decimal places.	1	4	1	(06)
	b.	Employ Taylor's series method to obtain approximate value of y at x=0.2 for the differential equation $\frac{dy}{dx} = x^2y - 1$.	2	4	1	(07)
	c.	Use Runge-Kutta method to find y(0.1), given $\frac{dy}{dx} = x + y^2$, y(0)=1.	2	4	1	(07)

x:	0	$\pi/3$	$2\pi/3$	π	$4\pi/3$	$5\pi/3$	2π
f(x):	1.0	1.4	1.9	1.7	1.5	1.2	1.0

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

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OR

6 a. Obtain value of $\sqrt{N}$, using Newton-Raphson method and hence evaluate $\sqrt{28}$. 1 4 1 (06)

b. Solve $sinx = e^{-x}$, using fixed point iteration method. 2 4 1 (07)

c. Using modified Euler's method find an approximate value of y when x=0.2 and x=0.4, given that $\frac{dy}{dx} = \log(x+y)$, y(0)=2. 2 4 1 (07)

UNIT -V

7 a. Determine the rank of the matrix $\begin{bmatrix} 2 & 3 & -1 & -1 \\ 1 & -1 & -2 & -4 \\ 3 & 1 & 3 & -2 \\ 6 & 3 & 0 & -7 \end{bmatrix}$ by elementary transformations. 1 5 1 (06)

b. Solve the equations $2x - 3y + z = -1$, x+4y+5z = 25, 3x-4y+z = 2 by Gauss-Jordan method. 2 5 1 (07)

c. Obtain numerically largest eigenvalue and the corresponding eigenvector of the matrix $\begin{bmatrix} 1 & 6 & 1 \\ 1 & 2 & 0 \\ 0 & 0 & 3 \end{bmatrix}$ by power method . Taking the initial vector$[1 \quad 0 \quad 0]^T$. Carryout five iterations. 2 5 1 (07)

OR

8 a. For what value of λ the rank of the matrix $\begin{bmatrix} 1 & 2 & 1 \\ 1 & 3 & 4 \\ 3 & 6 & \lambda \end{bmatrix}$ will be equal to TWO. Use elementary transformations. 2 5 1 (06)

b. Solve by Gauss – Seidel method the linear simultaneous equations $10x + y + z = 12; 2x + 10y + z = 13; 2x + 2y + 10z = 104$. 2 5 1 (07)

c. Find all the eigenvalues and eigenvectors of the matrix $\begin{bmatrix} 1 & 1 & 3 \\ 1 & 5 & 1 \\ 3 & 1 & 1 \end{bmatrix}$. 2 5 1 (07)

Note: L (Level),CO (Course Outcome), PO (Programme Outcome), M (Marks)

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Third Semester B.E. Semester End Examination, Dec/Jan 2017-18

LOGIC DESIGN AND APPLICATIONS

Time: 3 Hours Max. Marks: 100

Instructions: 1. *Unit I and Unit III are compulsory*
2. *Answer one full question from remaining Units*

UNIT – I

1 a. Realize the following expression using basic gates and universal NOR gate. 04 M
Y(A,B,C)= AB + C'
(Level [3], CO [1], PO [1])

b. Simplify the given Boolean function in the SOP form using K-Map reduction technique and realize using NAND gates only. 08 M
(W,X,Y,Z)=∑m(1,2,4,5,8,9,10,12,13) +d(0,3,6,7,15)
(Level [3], CO [1], PO [2])

c. Apply Quine McClusky reduction technique to simplify the given Boolean expression. 08 M
F(A,B,C,D) = ∑m (1,4,6,9,10,11,14,15) + d(0,3)
(Level [3], CO [1], PO [2])

UNIT – II

2 a. Define Multiplexer and De-multiplexer. Show how 4:1 multiplexer can be obtained using only 2:1 multiplexer. 06 M
(Level [1,3], CO [2], PO [1])

b. Show how suitable decoder and multi input OR gates can be used to realize the following Boolean expressions simultaneously. 08 M
F1(A,B,C)=AB+A'C'
F2(A,B,C) = BC
F3(A,B,C) = ∑m (1,4,6,7)
(Level [3], CO [2], PO [2])

c. Design 4-bit parity generator using *XOR* gates. 06 M
(Level [3], CO [2], PO [2])

OR

3 a. Explain the working of (i)Decimal to BCD encoder (ii) 1 to 10 Decoder 08 M
(Level [2], CO [2], PO [2])

b. Design a 2 bit magnitude comparator. 08 M
(Level [3], CO [2], PO [2])

c. List and explain the differences between PLA and PAL. 04 M
(Level [1, 2], CO [2], PO [2])

UNIT - III

4 a. Obtain the characteristic equation, state transition diagram and Excitation table for JK and D flip flops. 08 M
(Level [3], CO [3], PO [2])

b. Explain the working of positive edge triggered RS flip flop with waveforms. 06 M
(Level [2], CO [3], PO [2])

c. Explain the working of JK Master Slave flip flop and realize the same using NAND gates only. 06 M
(Level [2,3], CO [3], PO [2])

UNIT – IV

5 a. Convert the following with neat sketch: 08 M
i. SR flip flop to JK flip flop
ii. JK flip flop to T flip flop
iii. JK flip flop to D flip flop
(Level [3], CO [3], PO [2])

b. List the differences between Serial and Parallel counters. Design a 4 bit asynchronous UP counter using JK flip flop and represent the output with waveforms. 06 M
(Level [1,3], CO [3], PO [2])

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c. Explain the working of 4 bit Serial In Serial Out (SISO) shift register with suitable waveforms. (Level [2], CO [3], PO [2]) 06 M

OR

6 a. Construct Mod-6 synchronous up counter. Realize the same using D flip flop only. (Level [3], CO [3], PO [2]) 10 M

b. Explain the working of 4 bit Johnson counter with it's state table. (Level [2], CO [3], PO [2]) 05 M

c. Design a serial adder using shift registers to perform addition of two 8-bit numbers. (Level [3], CO [3], PO [2]) 05 M

UNIT – V

7 a. Define Accuracy and Resolution. With neat sketch explain the working of 4 bit R -2R binary ladder. Determine the output voltages caused by each bit in a 6 bit ladder if the input levels are 0= 0V and 1=+15V. (Level [1,2], CO [3], PO [2]) 10 M

b. List and Explain the different types of HDL models. (Level [1,2,], CO [4], PO [4]) 10 M

OR

8 a. With a neat diagram explain successive approximation type ADC. The counter type ADC is 8 bits and driven by 500KHz clock. Find maximum conversion time and average conversion time. (Level [2,3], CO [3], PO [2]) 10 M

b. Develop HDL code for
(i) 4 to 1 multiplexer
(ii) Adder
(Level [3], CO [4], PO [4]) 10 M

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16CS32 / CS32 / 16IS32 / IS32

Third Semester B.E. Makeup Examination, January 2018

LOGIC DESIGN AND APPLICATIONS

Time: 3 Hours

Max. Marks: 100

Instructions: 1. *UNIT I and III are compulsory.*
2. *Answer one full question from remaining Units*

UNIT – I

1 a. Apply K-Map reduction technique to obtain the reduced SOP expression for the given Boolean function and realize using basic gates. **06 M**

$F(A,B,C,D) = \Sigma m(0,2,4,6,8,9,14,15) + d(1,11)$

(Level[3], CO[1], PO[1])

b. For a given expression Y=ABC' + BC'+A'B', write the truth table, find the min terms, and draw the circuit using basic gates. **06 M**

(Level[3], CO[1], PO[1])

c. Solve the given Boolean function to obtain reduced expression using Quine McClusky reduction technique. **08 M**

$F(A,B,C,D) = \Sigma m(0,2,3,4,6) + d(1)$

(Level[3], CO[1], PO[1])

UNIT – II

2 a. Explain 4:1 Multiplexer and implement the given Boolean function using suitable Multiplexer $F(A,B,C) = \Sigma m(0,1,4,6,7)$ **06 M**

(Level[2, 3], CO[2], PO[1])

b. Define Decoder. Design a suitable decoder for the given SOP functions. **06 M**

$F1(A,B,C) = \Sigma m(0,1,4,6,7)$, $F2(A,B,C) = AB+A'B$

(Level[1, 3], CO[2], PO[1])

c. Differentiate between PAL and PLA. Make use of PLA to implement the following Boolean functions. **08 M**

F1= ABC'D'+ AB'CD+AB'C'D+ABCD

F2= A'B'CD+AB'C'D+ABC'D+ABCD

(Level[2,3], CO[2], PO[1])

OR

3 a. With neat sketch explain Decimal to Binary Encoder. **06 M**

(Level[2], CO[2], PO[1])

b. Draw the logic diagram of 8:1 Multiplexer. Implement 8:1 Multiplexer using 4:1 Multiplexer. **06 M**

(Level[1,3], CO[2], PO[1,4])

c. Design 2-bit Magnitude comparator and draw the logic diagram for the same. **08 M**

(Level[3], CO[2],PO [1,4])

UNIT – III

4 a. What is clock? List out the properties of Clock. Find the frequency of the clock if T=0.2ms **06 M**

(Level[1,3], CO[2], PO[1,4])

b. Explain the basic SR Latch using NAND/NOR gate realization. Explain the working of clocked SR flip flop. **06 M**

(Level[2], CO[2], PO[1,4])

c. Derive the characteristic equation for JK and SR flip flop. Draw the state transition diagram and write the excitation table for both. **08 M**

(Level[3], CO[2], PO[1,4])

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UNIT – IV

5 a. Design MOD-5 synchronous counter using JK flip flop and draw the logic circuit for the same. **06 M**

(Level[3], CO[3], PO[1])

b. Explain the working of 3-bit asynchronous UP counter and draw the waveform for the same. **06 M**

(Level[2], CO[3], PO[1,4])

c. Analyze the given sequential circuit in the figure below. **08 M**

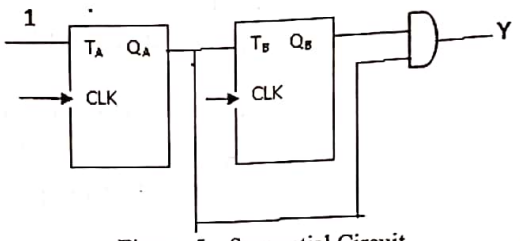

Figure. 5.c Sequential Circuit

(Level[4], CO[3], PO[1,4])

OR

6 a. Explain the working of master slave JK flip flop. Design the same using NAND gates only. **06 M**

(Level[3],CO[3],PO[1,4])

b. Convert SR flip flop into JK flip flop. **06 M**

(Level[3], CO[3], PO[1,4])

c. Explain with a neat diagram and waveform the following. **08 M**

i) Serial in Parallel out (SIPO) register.

ii) Johnson Counter

(Level[2], CO[3], PO[1])

UNIT –V

7 a. Explain 4-bit R-2R binary ladder Digital to Analog Converter (DAC). What is the output of DAC when binary input is 1100? Given V=10 volts. **06 M**

(Level[2], CO[3], PO[1,4])

b. Develop the HDL code for the following. **06 M**

i) 4:1 Multiplexer

ii) Full Adder.

(Level[3], CO[4], PO[1,4])

c. Explain with a neat diagram the working of Successive Approximation type ADC. The Counter type ADC is 10-bit and driven by 500kHz clock. Find the maximum conversion time and average conversion time. **08 M**

(Level[1, 2], CO[3], PO[1,4])

OR

8 a. Explain 3-bit resistive divider network DAC. For 5 bit resistive divider, determine the weight of LSB and output when binary input is 11001. **06 M**

(Level[2,3], CO[3], PO[1,4])

b. Develop the HDL code for the following. **06 M**

i) 2:1 Multiplexer.

ii) SR flip flop

(Level[3], CO[4], PO[1,4])

c. Explain 2-bit parallel comparator type ADC. How many comparators are required for 3-bit ADC? Find the conversion time for 8 bit Successive Approximation type ADC. **08 M**

(Level[1, 2], CO[3], PO[1])

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CS/IS/34/16CS/IS34

Third Semester B.E. Semester End Examination, Dec/Jan 2017-18

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions:
1. *Unit I and IV are COMPULSORY.*
2. *Answer ANY one full question from remaining each units.*
3. *Suitable data can be assumed giving justification.*
4. *Accuracy does matter.*

UNIT - I

1 a. Interpret Basic Operational Concepts showing connections between the processor and memory with a neat block diagram. 06 M
(Level [2], CO [1], PO [1])

b. Convert the following pairs of decimal numbers to 5bit signed 2's complement binary numbers & add them. Analyze whether an overflow occurs. 08 M
i)+16 & +2 ii) -4 & +6 iii) -15 & +11 iv) -10 & -8.
(Level [4], CO [2], PO [2])

c. Contrast straight-line sequencing and branching, with a program to add 10 numbers. 06 M
(Level [4], CO [2], PO [1])

UNIT – II

2 a. Find Effective Addresses (EA) in all the Addressing Modes. 08 M
(Level [1], CO [3], PO [2])

b. Interpret, with a neat sketch, Distributed Arbitration. 06 M
(Level [2], CO [3], PO [1])

c. Contrast Synchronous and Asynchronous Buses with the help of relevant timing waveforms. 06 M
(Level [2], CO [3], PO [1])

OR

3 a. Multiple Devices are connected to the processor. Distinguish the three approaches to handle such a situation, using interrupts, with diagrams, if any. 08 M
(Level [4], CO [3], PO [1])

b. Plan a program that reads one line from the keyboard, stores it in memory buffer, and echoes it to the display, with comment lines. 06 M
(Level [3], CO [3], PO [1])

c. Interpret, with a neat sketch, Centralized Arbitration. 06 M
(Level [2], CO [3], PO [1])

UNIT – III

4 a. With internal organization diagram of a 2M x 8 dynamic memory chip, explain asynchronous DRAMs. 08 M
(Level [2], CO [3], PO [2])

b. Explain Set-associative-mapped cache with two blocks per set, with neat sketch. Assume bits for tag 5, set 6 and word 4. 06 M
(Level [2], CO [3], PO [2])

c. Summarize the memory hierarchy with respect speed, size and cost. 06 M
(Level [2], CO [1], PO [1])

OR

5 a. Explain the internal organization of a memory chip for 1K x 1 memory chip, using decoder and multiplexer. 08 M
(Level [2], CO [2], PO [1])

b. Explain Read Write operations with respect to Static Memories, with diagrams of a SRAM cell. 06 M
(Level [2], CO [2], PO [1])

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c. Explain a Read Only Memory (ROM) cell. Summarize its four types. 06 M

(Level [2], CO [2], PO [1])

UNIT – IV

6 a. Demonstrate Booth's Algorithm for signed multiplication of $+15_{10}$& -15_{10}. 06 M

(Level [4], CO [4], PO [2])

b. Evaluate product, using fast multiplication algorithm - bit-pair algorithm / method, of 14_{10} and 11_{10} 06 M

(Level [5], CO [4], PO [2])

c. Illustrate how you calculate quotient and remainder when 10_{10} is divided by 02_{10}, applying Restoring Division algorithm. 08 M

(Level [2], CO [4], PO [2])

UNIT - V

7 a. Define Computer Architecture. Outline seven dimensions of an ISA. 08 M

(Level [2], CO [1], PO [1])

b. Explain the following in Brief i) Amdahl's Law ii) Dependability. 06 M

(Level [2], CO [1], PO [1])

c. Explain Measuring, Reporting and Summarizing performance of a computer architecture. 06 M

(Level [2], CO [2], PO [2])

OR

8 a. Demonstrate the working of a classic five stage pipeline for a RISC processor. 10 M

(Level [2], CO [4], PO [2])

b. Explain data hazards and methods to minimize data hazards with examples. 10 M

(Level [2], CO [4], PO [2])

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16CS34 / CS34 /16IS34 / IS34

Third Semester B.E. Makeup Examination, January 2018

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions: 1. *Unit I & IV are compulsory.*
2. *Answer any five full Questions.*
3. *Suitable data can be assumed giving justification.*
4. *Accuracy does matter.*

UNIT - I

1 a. With a neat diagram show the connection between memory & processor and explain typical operational steps in executing an instruction. (Level [2], CO [1], PO [1]) **08 M**

b. Convert the following pairs of decimal no's to 5 bit signed 2's complement binary numbers & add them. Analyze whether an overflow/underflow occurs.
i) 7 & 13 ii) -5 & 7 iii) -14 & 11 iv) -10 & -13 (Level [4], CO [2], PO [2]) **06 M**

c. Define Addressing Mode and explain any four addressing modes with a suitable example. (Level [1,2], CO [1], PO [1]) **06 M**

UNIT – II

2 a. What is an interrupt? With a neat block diagram explain Daisy Chain Interrupt Priority Scheme for handling simultaneous requests. (Level [1,2], CO [2], PO [2]) **10 M**

b. What is DMA? Explain in brief simple arrangement for a centralized bus arbitration approach. (Level [1,2], CO [1], PO [1]) **10 M**

OR

3 a. Explain the following in brief:
i)Program controlled I/O ii) Enabling & Disabling Interrupts (Level [2], CO [2], PO [1]) **10 M**

b. Make use of a neat sketch to explain the timing diagram of Synchronous Bus for input operation (Level [3], CO [2], PO [2]) **10 M**

UNIT – III

4 a. Make use of a relevant circuit diagram for static RAM cell and explain how a Read and Write operations can be performed on it. (Level [3], CO [2], PO [1]) **10 M**

b. Make use of a suitable example and Explain Set Associative Mapping technique (Level [3], CO [2], PO [2]) **10 M**

OR

5 a. Explain the following: i) PROM ii) EPROM (Level [2], CO [1], PO [1]) **05 M**

b. Distinguish between i) SRAM ii) DRAM (Level [4], CO [3], PO [2]) **05 M**

c. With a suitable example, Explain Direct Mapping cache memory technique. (Level [2], CO [2], PO [1]) **10 M**

UNIT – IV

6 a. Give the steps of Booth's Algorithm. Evaluate the product by multiplying the following pairs of 4 bit signed 2's complement numbers using the same. **07 M**

M= +14 & Q= -10

(Level [5], CO [2], PO [2])

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b. Solve usingRestoring integer Division method, the following example: $8 \div 3$ 08 M

(Level [2,3], CO [2], PO [2])

c. Explain FOUR bit Carry Look Ahead Adder. 05 M

(Level [2], CO [2], PO [1])

UNIT –V

7 a. Define Computer Architecture. Illustrate seven dimensions of an ISA. 10 M

(Level [1,2], CO [1], PO [1])

b. Explain the following in brief i) Amdahl's law ii) Dependability 10 M

(Level [2], CO [2], PO [1])

OR

8 a. What is Pipelining? List Pipeline hazards & explain any one in detail. 10 M

(Level [1], CO [1], PO [1])

b. Explain the following in brief i) Measuring ii) Quantitative principles of Computer Design 10 M

(Level [2], CO [2], PO [2])

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CS/IS35/16CS/IS35

Third Semester B.E. Semester End Examination, Dec/Jan 2017-18

DATA STRUCTURES USING C

Time: 3 Hours

Max. Marks: 100

Instructions:
1. *UNIT-I and UNIT- II are Compulsory.*
2. *Answer any one question from remaining units.*
3. *Write comments in the programs where ever necessary.*
4. *Write sample input/output for the program where ever necessary.*

UNIT - I

1 a. Define the word data structures and discuss its importance for computer science. **04 M**
(Level [2], CO [3], PO [1])

b. Write a C program to demonstrate the use of stack for a CD/DVD case of capacity 10 such that, we should not insert more than 10 discs, should not remove disc from empty case and display no. of discs at any point of time. **10 M**
(Level [3], CO [3], PO [1])

c. Demonstrate along with code snippets insertion and deletion operation of circular queue using arrays. **06 M**
(Level [2], CO [3], PO [1])

UNIT – II

2 a. Differentiate between arrays and linked lists. Write a function to create a linked list by adding nodes at rear of list. **08 M**
(Level[4], CO[2], PO[8])

b. Write functions for the following: **06 M**
i. to reverse the list
ii. to display odd and even node elements on two different lines.
(Level[3], CO[2], PO[12])

c. Discuss how the polynomials are represented using circular linked list? With example and block diagram explain addition of two polynomials using the circular list. **06 M**
(Level[3], CO[2], PO[2])

UNIT III

3 a. Illustrate the working of Doubly linked list for insertion and deletion of element from a given position in the program **10 M**
(Level [2], CO [2], PO [3])

b. Explain with code the working of inorder, preorder and post order traversals in binary trees. Illustrate with examples. **10 M**
(Level [2], CO [3], PO [1,3])

OR

4 a. Demonstrate with a sample code the method of inserting an element into a binary search tree. **10 M**
(Level [2], CO [3], PO [3])

b. Build a max heap and min heap for set of numbers 10,8,6,7,12,14 **10 M**
(Level [3], CO [4], PO [1])

UNIT IV

5 a. What is AVL tree? Explain with example. **06 M**
(Level[2], CO[3], PO[2])

b. Illustrate how collision occurs and explain any two methods to resolve it. **10 M**
(Level[2], CO[4], PO[2])

c. Explain open addressing method for overflow handling. **04 M**
(Level[2], CO[4], PO[12])

OR

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6 a. Discuss any two hash functions. 06 M

(Level[2], CO[4], PO[8])

b. Compare quadratic probing and pseudo random collision resolution methods. 06 M

(Level[4], CO[4], PO[2])

c. Explain liner probing method of overflow handling with the help of example. 08 M

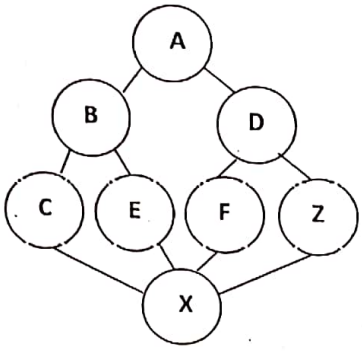
(Level[2], CO[4], PO[2])

UNIT - V

7 a. Define graph. With example discuss how the graph is represented using Adjacency Matrix 06 M

(Level[2],CO[4],PO[8])

b. Draw an adjacency list for a given graph: 06 M



(Level[2], CO[4], PO[8])

c. Write recursive function for depth first search operation on graph. 08 M

(Level[3], CO[4], PO[12])

OR

8 a. What is spanning tree? Explain with example 06 M

(Level[2],CO[4],PO[12])

b. Draw Depth-first and breadth-first spanning trees for the graph given in 7b. 06 M

(Level[2], CO[4], PO[12])

c. Write function for breadth first search operation on graph. 08 M

(Level[3], CO[4], PO[12])

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16MAT31 / MAT31

Third Semester B.E. Semester End Examination, Dec/Jan 2017-18
STATISTICAL-NUMERICAL-FOURIER TECHNIQUES / ENGINEERING MATHEMATICS-III)

Time: 3 Hours

Max. Marks: 100

Instructions: 1. *UNIT III and V are compulsory.*
2. *Answer any one question from remaining each unit.*

UNIT - I

1 a. Use Regula falsi method to extract the root of the equation $2x - \log_{10} x = 7$ upto 3 decimals. **06 M**
(Level [2], CO [1], PO [1])

b. Apply Newton-Raphson's method to obtain the non-zero root of the equation $f(x) = xe^x - \cos x = 0$ upto 3 decimals. **07 M**
(Level [2], CO [1], PO [2])

c. Illustrate fixed point iteration method to find the root of the equation $x = \frac{1}{2} + \sin x$ upto 3 decimals. **07 M**
(Level [2], CO [1], PO [1])

OR

2 a. Use Taylor's series method up to 5th derivative term to obtain y (0.3) for the differential equation $\frac{dy}{dx} = x + y^2,\ y(0) = 1.$ **06 M**
(Level [2], CO [1], PO [2])

b. Apply Euler's modified method to solve the differential equation $\frac{dy}{dx} = x^2 - y^2, y(0) = 1$ at $x = 0.4$ in 2 steps. **07 M**
(Level [3], CO [1], PO [1])

c. Illustrate Runge-Kutta's fourth order method to solve $\frac{dy}{dx} = e^x + y,\ y(0) = 0$ at $x = 0.1$ in 1 step. **07 M**
(Level [2], CO [1], PO [1])

UNIT – II

3 a. Construct Fourier series for the function $f(x) = 2\pi x,\ 0 \le x \le 2$ **06 M**
(Level [3], CO [2], PO [1])

b. Transform the function $f(x) = \begin{cases} x^2, 0 < x < \frac{\pi}{2} \\ x, \frac{\pi}{2} < x < \pi \end{cases}$ into half-range sine series. **07 M**
(Level [2], CO [2], PO [2])

c. Represent the following function in Fourier series up to first harmonic. **07 M**

t sec	0	T/6	T/3	T/2	2T/3	5T/6	T
A amp	1.98	1.3	1.05	1.3	-0.88	-0.25	1.98

(Level [2], CO [2], PO [1])

OR

4 a. Construct Fourier series for the function $f(t) = 1 - t^2,\ -1 \le t \le 1.$ **06 M**
(Level [3], CO [2], PO [2])

b. Transform the function $f(x) = x \cos x,\ 0 \le x \le 2$ into half- range Fourier cosine series. **07 M**
(Level [2], CO [2], PO [1])

c. Represent the following function in Fourier cosine series up to second term. **07 M**

x	0	1	2	3	4	5
y	2	8	12	10	9	6

(Level [2], CO [2], PO [2])

UNIT – III

5 a. Evaluate Fourier Transform of the function $f(t) = a^2 - t^2,\ -a \le t \le a$. Hence deduce the **06 M**

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value of $\int_0^\infty \frac{t\cos t - \sin t}{t^3}\,dt$

(Level [2], CO [3], PO [2]) 07 M

b. Solve the integral equation $\int_0^\infty f(x)\sin(tx)\,dx = \begin{cases} 1, & 0 \le t \le 1 \\ 2, & 1 \le t \le 2 \\ 0, & t \ge 2. \end{cases}$

(Level [2], CO [3], PO [1]) 07 M

c. Evaluate Fourier Cosine Transform of the function

$$f(x) = \begin{cases} \cos x, & 0 < x < a \\ 0, & x \ge a. \end{cases}$$

(Level [2], CO [3], PO [2])

UNIT IV

6 a If the following represents valid p.d.f. then calculate k, Mean and Standard deviation given 06 M

X	0.5	1.5	2.5	3.5	4.5
P(X)	$2k$	k	$4k$	k	$2k$

Level [2], CO [4], PO [1])

b. Demonstrate that mean and variance of Binomial distribution are np and npq respectively. 07 M

(Level [2], CO [4], PO [1])

c. Under the Normal distribution 31% are below 35 and 9 % are above 60, identify the mean and Standard deviation of the distribution. Given A(z =0.5) = 0.19 and A(z =1.4) = 0.42. 07 M

(Level [2], CO [4], PO [1])

OR

7 a. If the following represents a valid p.d.f. then calculate k, P (0 < x <3), P(x > 2) given 06 M

$$p(x) = \begin{cases} \frac{kx^2}{1+x}, & 1 < x < 5 \\ 0, & \text{elsewhere} \end{cases}$$

(Level [2], CO [4], PO [2])

b. If the conversation on telephone is a Poisson variate with mean 4 mins.,then calculate the probability that 07 M

(i) conversation lasts for more than 1 min.

(ii) conversation lasts between 2 and 3 mins.

(Level [2], CO [4], PO [1])

c. The Mean of an Exponential distribution is 8,then identify $E(x^2)$, P(1< x < 4), P(x > 5). 07 M

(Level [2], CO [5], PO [2])

UNIT –V

8 a. The joint distribution of two random variables X and Y are given by 06 M

X \ Y	1	2	3	4
1	0.06	0.05	.09	0.2
2	0.14	0.15	0.21	0.1

Determine the individual distributions of X and Y. Also verify whether X and Y are stochastically independent.

(Level [2],CO [5], PO[1])

b. A software engineer goes to his work place every day by motor bike or car. He never goes by same mode on two successive days; but if he goes by car on a day then he is equally likely to go by bike or car on the next day. Represent the transition matrix of his mode of transport. If he uses car on the first day of the week, find the probability that (i)bike is used (ii) car is used, on the fifth day. 07 M

(Level [2],CO[5], PO[2])

c. Define a stochastic matrix. Find unit fixed probability vector for the stochastic matrix P. 07 M

$$P = \begin{bmatrix} 0 & 1 & 0 \\ \frac{1}{8} & \frac{1}{2} & \frac{1}{8} \\ 0 & \frac{1}{2} & \frac{1}{2} \end{bmatrix}$$

(Level [2], CO [5], PO [1])

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MAT31

B.E. Fast Track Examination, JULY / AUG. 2016-17

ENGINEERING MATHEMATICS-III

Time: 3 Hours **Max. Marks: 100**

Instructions:
1. *Questions from unit III and V are compulsory.*
2. *Answer any ONE Full question from each of other units.*
3. *Max marks will be scaled to 50 for SGPA & CGPA calculations.*

UNIT - I

1 a. Using Regula-falsi method, compute a real root of the equation $2x - \log_{10} x = 7$ in the interval $[3, 4]$ correct to three decimal places. **06 M**

(Level[3], CO[1],PO[1])

b. Find root of the equation $2x = cosx + 3$ corrected to three decimal places using iteration method. **07 M**

(Level[1], CO[1], PO[1])

c. ApplyModifiedEuler's method to find $y(0.2)$ and $y(0.4)$ for $y' = y + e^x$, given $y(0) = 0$ **07 M**

(Level[3], CO[1], PO[1])

OR

2 a. Use Newton-Raphson method to compute cube root of 13 up to four iterations. **06 M**

(Level[3], CO[1], PO[2])

b. Employ Taylor's method to obtain approximate value of y at $x = 0.2$ for differential equation $\frac{dy}{dx} = 2y + 3e^x, y(0) = 0$. Compare with exact solution. **07 M**

(Level[2], CO[1], PO[1])

c. Apply Runge-Kutta method of fourth order to find an approximate value of y at $x = 0.2$ if $\frac{dy}{dx} = x + y^2$, given that $y = 1$ when $x = 0$ **07 M**

(Level[3], CO[1], PO[1])

UNIT – II

3 a. Find the Fourier series expansion for f(x), if $f(x) = \begin{cases} -\pi, & -\pi < x < 0 \\ x, & 0 < x < \pi \end{cases}$ **06 M**

(Level[1], CO[2], PO[1])

b. Obtain a half range cosine series for $f(x) = \begin{cases} kx, & -\pi \le x \le \frac{l}{2} \\ k(l - x), & \frac{l}{2} \le x \le l \end{cases}$ **07 M**

Deduce the sum of the series $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \cdots\cdots\cdots\infty$

(Level[4], CO[2], PO[2])

c. The turning moment T is given for a series of values of the crank angle $\theta^o = 75^o$ **07 M**

θ^o :	0	30	60	90	120	150	180
T :	0	5224	8097	7850	5499	2626	0

Obtain the first four terms in a series of sines to represent T and calculate T for $\theta = 75^o$

(Level[2], CO[2], PO[1])

OR

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4 a. Find the Fourier series expansion of $f(x) = 2x - x^2$ in$(0, 3)$ and hence deduce that $\frac{1}{1^2} - \frac{1}{2^2} + \frac{1}{3^2} - \frac{1}{4^2} \cdots\cdots\cdots\cdots \infty = \frac{\pi^2}{12}$ **06 M**

(Level[1], CO[2], PO[1])

b. Obtain Fourier series for the function f(x) given by $f(x) = \begin{cases} 1 + \frac{2x}{\pi}, & -\pi \le x \le 0 \\ 1 - \frac{2x}{\pi}, & 0 \le x \le \pi \end{cases}$ **07 M**

Deduce that $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + \cdots\cdots\cdots\cdots \infty = \frac{\pi^2}{0}$

(Level[4], CO[2], PO[2])

c. Draw graph of $f(x) = \begin{cases} x, & 0 \le x \le \frac{\pi}{2} \\ \pi - x, & \frac{\pi}{2} \le x \le \pi \end{cases}$ and show that $f(x) = \frac{4}{\pi}[sinx - \frac{1}{3^2}sin3x + \frac{1}{5^2}sin5x - \cdots\cdots\cdots\cdots]$ **07 M**

(Level[1], CO[2], PO[2])

UNIT - III

5 a. If P is the pull required to lift a load W by means of a pulley block, find a linear law of the form $P = mW + c$ connecting P and W, using the following table: **06 M**

P:	12	15	21	25
W:	50	70	100	120

Where P and W are taken in kg-wt. compute P when W=150 kg-wt.

(Level[2], CO[3], PO[2])

b. The voltage v across a capacitor at time t seconds is given by following data: **07 M**

t:	0	2	4	6	8
v:	150	63	28	12	5.6

Use the method of least squares to fit a curve of the form $v = ae^{kt}$ to this data.

(Level[3], CO[3], PO[1])

c. The regression equations of variables x and y are $x = 0.7y + 5.2$, $y = 0.3x + 2.8$. Findmean of variables and coefficient of correlation between them. **07 M**

(Level[1], CO[3], PO[1])

UNIT – IV

6 a. If $f(x) = \begin{cases} k(x+1), & -1 \le x \le 1 \\ 0, & otherwise \end{cases}$ determine the value of k so that $f(x)$ is pdf. Also find $P(0 < x < 1)$, Also evaluate $P(x \le 0 \; and \; x \ge 1)$, $E(X = x)$, var(X). **06 M**

(Level[1], CO[4], PO[1])

b. In a certain factory turning out razor blades, there is a small chance of 0.002 for any blade to be defective. The blades are supplied in packets of 10, use Poisson distribution to calculate the approximate number of packets containing no defective, one defective and two defective blades respectively in a consignment of 10,000 packets. **07 M**

(Level[4], CO[4], PO[2])

c. In a test on 2000 electric bulbs, it was found that the life of a particular make, was normally distributed with an average life of 2040 hours and S.D. of 60 hours. Estimate the number of bulbs likely to burn for **07 M**

i. More than 2150 hours
ii. Less than 1950 hours
iii. More than 1920 hours but less than 2160 hours.

(Level[2], CO[4], PO[1])

OR

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7 a. A fair coin is tossed three times. Let X denote the number of heads showing up. Find the distribution of X. also its mean, variance and standard deviation. **06 M**

(Level[1], CO[4], PO[1])

b. In a large number of parts manufactured by a machine, the mean number of defective in a sample of 20 is 2. Out of 1500 such samples, how many would be expected to contain at least 2 defective parts. **07 M**

(Level[1], CO[4], PO[2])

c. After the appointment of a new sales manager, the sales in a two-wheeler showroom is exponentially distributed with mean 4. If two days are selected at random what is the probability that **07 M**

i. On both days the sales is over 5 units

ii. The sales is over 5 units on atleast one of the two days?

(Level[2], CO[4], PO[1])

UNIT -V

8 a. A coin is tossed three times. X=0 or 1 according to Tail of Head occuring on the First toss, Y= Number of Tails. Determine **06 M**

i. The marginal distributions of X and of Y

ii. Joint P.D.F of "X and Y"

iii. Expected values of X+Y and XY.

(Level[4], CO[5], PO[1])

b. Define Probability vector with an example. Show that Markov chain with transition matrix $P = \begin{bmatrix} 0 & 2/3 & 1/3 \\ 1/2 & 0 & 1/2 \\ 1/2 & 1/2 & 0 \end{bmatrix}$ is irreducible. **07 M**

(Level[1], CO[5], PO[1])

c. A student's study habits are as follows. If he studies one night he is 60% sure not to study the next night. If he does not study one night he is 80% sure to study the next day. In the long run how often does he study? **07 M**

(Level[2], CO[5], PO[2])

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CS/IS32

B.E. Fast Track Examination, JULY / AUG. 2016-17

LOGIC DESIGN AND APPLICATIONS

Time: 3 Hours

Max. Marks: 100

Instructions: 1. *Answer any FIVE full questions.*
2. *UNIT I and III are compulsory.*

UNIT - I

1 a. Show that (A + B) (A + C) = A + BC using rules of Boolean algebra and implement the expression using basic gates . (Level [2], CO [1], PO[1,3]) 06 M

b. Solve the following SOP Boolean function using K-MAP technique and design the circuit using NAND gates.
$F(A,B,C) = \sum m(1,3,5,6,7)$
(Level [3], CO [1], PO [1,2]) 06 M

c. Identify all the prime and essential prime implicants of the following Boolean function using Quine Mc Clusky method.
$F(A,B,C,D) = = \sum m(1,3,4,5,7,8,15)$
(Level [3], CO [1], PO [1,4]) 08 M

UNIT – II

2 a. Define multiplexer and explain the working of 2X1 multiplexer with a neat diagram and truth table. (Level [1,2], CO [2], PO [1,3]) 06 M

b. How a PAL is different from PLA? Realize the following functions using PAL.
$Y1= A\hat{}BC\hat{} + A\hat{}BC + AB\hat{}C + ABC\hat{}$
$Y2 = ABC$
(Level [1], CO [2], PO [1,3]) 08 M

c. Illustrate the working of odd parity generator with a neat diagram. (Level [2], CO [2], PO [1,3]) 06 M

OR

3 a. Build up a 32X1 multiplexer using two 16X1 multiplexers and one 2X1 multiplexer. (Level [3], CO[2], PO [1,3]) 06 M

b. Analyze the working of 1-to-16 Demultiplexer using basic gates. (Level [4], CO[2], PO [1,3]) 08 M

c. Define Decoder and realize the following functions using 3:8 Decoder and multi-input OR gates.
$F1(x,y,z) = \sum m(0,1,2,6)$
$F2(x,y,z) = \sum m(3,7)$
(Level [1], CO [2], PO [1,3]) 06 M

UNIT – III

4 a. Explain the working principle of a positive edge triggered JK flip flop and draw a neat sketch of its output waveform. (Level [2], CO [3], PO [1,3]) 06 M

b. Determine the characteristic equations of SR, T and D flip flops. (Level [5], CO [3], PO [1,3]) 06 M

c. What are the advantages of Master-Slave flip flop? Illustrate the working of Master-Slave JK flip flop with a neat circuit diagram and draw the output waveform. (Level [1,2], CO [3], PO [1,3]) 08 M

UNIT - IV

5 a. Develop the logic diagram of a 4 bit Serial In Parallel Out shift register and explain its working. (Level [3], CO[3], PO[1,3]) 06 M

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b. Illustrate the working of a 4-bit Ripple upcounter using JK flip flops with a neat block diagram and truth table. **06 M**

(Level [2], CO [3], PO [1,4])

c. Construct a MOD-3 synchronous upcounter using JK flip flops and explain its working with neat diagram and truth table. **08 M**

(Level [3], CO [3], PO [1,3,4])

OR

6 a. Explain how a shift register can be used as a sequence detector and draw a basic block diagram of the same. **06 M**

(Level [2], CO [3], PO [1,3,4])

b. How to convert JK flip flop into T flip flop and explain the steps with a neat diagram and state synthesis table. **06 M**

(Level [1,2], CO [3], PO [1,3])

c. Illustrate the working of a 4-bit Johnson counter with a neat block diagram and truth table. **08 M**

(Level [2], CO [3], PO [1,3,4])

UNIT - V

7 a. Explain Digital to Analog conversion using Binary Ladders. **06 M**

(Level [2], CO[3], PO[1,4])

b. A 5-bit D/A converter produces the Vout= 0.2V for a digital input of 00001. Find the value of Vout for an input of 11111. **06 M**

(Level [1], CO[3], PO [1,4])

c. Develop an HDL code for the following circuits. **08 M**

i) AB^C + A^C + ABC

ii) JK flip flop

(Level [3], CO [3], PO [1,4])

OR

8 a. Explain the working of a Counter type Analog to Digital converter with a neat block diagram. **08 M**

(Level [2], CO [3], PO [1,4])

b. Define Accuracy and Resolution of an A/D converter and find the value of the following of a Counter type A/D converter, driven by a 500KHZ clock. **06 M**

i) Maximum conversion time

ii) Average conversion time

(Level [1], CO [3], PO [1,4])

c. Illustrate different types of HDL models in brief. **06 M**

(Level [2], CO [3], PO [1,4])

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CB34/IB34

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B.E. Fast Track Examination, JULY / AUG. 2016-17

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours **Max. Marks: 100**

Instructions: *1. Unit I and IV are compulsory.*
2. Answer any one full question from remaining each units.

UNIT– I

1 a. How to measure the performance of the computer? Explain. (Level[1,2], CO[1], PO[1]) **06 M**

b. Write a note on big-endian and little-endian assignment. (Level[1], CO[1], PO[1,2]) **04 M**

c. Convert the following pairs of decimal numbers to 5-bit, signed, 2's- complement, binary numbers and add them. State whether or not overflow occurs in each case.
a) 7 &13 b) -14 & 11 c) -5 & 7 d) -3 & -8 e) -10 & -13 (Level[3], CO[1], PO[1]) **10 M**

UNIT- II

2 a. Draw the arrangement of a single bus structure and brief about memory mapped I/O. (Level[1], CO[2], PO[1,2]) **06 M**

b. What is an interrupt? With example illustrate the concept of interrupts. (Level[1], CO[2], PO[2]) **06 M**

c. Explain the two approaches for bus arbitration. (Level[2], CO[2], PO[2,3]) **08 M**

OR

3 a. With neat sketches, explain various methods for handling multiple interrupt requests. (Level[2], CO[2], PO[2]) **10 M**

b. What is the necessity of DMA? Explain the two modes in which DMA interface operates to transfer data. (Level[1,2], CO[2], PO[1,2]) **10 M**

UNIT– III

4 a. Explain 16X8 memory chip with a neat diagram. (Level[2], CO[2], PO[2,3]) **06 M**

b. Explain the working of a dynamic memory cell. (Level[2], CO[2], PO[2]) **06 M**

c. Explain about direct mapping cache memory. (Level[2], CO[2],PO [3]) **08 M**

OR

5 a. Discuss the internal organization of a 2M X 8 asynchronous DRAM chip. (Level[6], CO[2], PO[2,3]) **10 M**

b. Define static memories. Explain static RAM cell and CMOS memory cell. (Level[1,2], CO[2], PO[2]) **10 M**

UNIT– IV

6 a. Find the multiplication of signed 2's complement numbers using Booth's algorithm. A = 010111 and B = 110110. A is the multiplicand and B is the multiplier. (Level[1], CO[3], PO[3]) **06 M**

b. Solve the given signed 2's complement numbers using bit pair recoding method. M = 110101 Q = 011011 (Level[3], CO[3], PO[3]) **06 M**

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c. Write the circuit arrangement for binary division. Perform the restoring division for the given binary numbers 1000/0011 , show all the cycles. **08 M**

(Level[1], CO[3], PO[4])

UNIT –V

7 a. Define and discuss Amdahl's law **07 M**

(Level[5], CO[4], PO[1])

b. Demonstrate the working of a classic five stage pipeline for a RISC processor. **06 M**

(Level[2], CO[1], PO[1])

c. Explain data hazards and methods to minimize data hazards with example. **07 M**

(Level[2], CO[4], PO[4])

OR

8 a. Define Computer Architecture. Illustrate the seven dimensions of an ISA **10 M**

(Level[2], CO[1], PO[1])

b. List the major hurdles of pipelining. Explain the branch hazards in detail. **10 M**

(Level[4], CO[4], PO[4])

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CS35 / IS35

B.E. Fast Track Examination, JULY / AUG. 2016-17

DATA STRUCTURES WITH C

Time: 3 Hours **Max. Marks: 100**

Instructions:
1. *UNIT-I and UNIT- II are Compulsory.*
2. *Answer any one question from remaining units.*
3. *Write comments in the programs where ever necessary.*
4. *Write sample input/output for the program where ever necessary.*

UNIT - I

1 a. Explain dynamic memory management functions in C. **06 M**
(Level[2], CO[1], PO[1])

b. Write a recursive function to find Greatest Common Deviser of two numbers. **07 M**
(Level[3], CO[1], PO[2])

c. Give various ways of declaring structures also differentiate structure and union. **07 M**
(Level[2], CO[1], PO[11])

UNIT – II

2 a. What is Stack? Write functions for basic operations on stack. **04 M**
(Level[2], CO[1], PO[2])

b. Give the postfix form of the following infix expressions: **08 M**
i. a+b-(c*(a+b)/d)
ii. 4+3-5*6/2
Evaluate the following postfix expressions:
iii. 63/835+2**+
iv. 53*5/4+25*2/-
(Level[3], CO[1], PO[11])

c. Write functions to implement insert and delete operations for circular queue. **08 M**
(Level[3], CO[2], PO[11])

UNIT – III

3 a. Differentiate between arrays and linked lists. **04 M**
(Level[2], CO[2], PO[2])

b. Write functions for the following: **08 M**
i. to create linked list by adding node at the front of the list
ii. to display the contents of the list.
(Level[3], CO[2], PO[2])

c. Write a function to concatenate two lists. **08 M**
(Level[3], CO[2], PO[2])

OR

4 a. Write a program to implement linear queue using linked list. **10 M**
(Level[3], CO[2], PO[11])

b. Write a program to count number of nodes in a given linked list. **04 M**
(Level[3], CO[2], PO[11])

c. What are the advantages of doubly linked list over singly linked list? Explain. **06 M**
(Level[2], CO[2],PO [2])

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UNIT - IV

5 a. Define binary search tree and explain tree traversal functions with the help of code. **07 M**
(Level[1], CO[2], PO[11])

b. Construct a binary search tree for given traversals **07 M**
In-order : WSXQYTZPURV
Pre-order : PQSWXTYZRUV
(Level[3], CO[2], PO[11])

c. Explain the array and linked representation of binary search tree. **06 M**
(Level[1], CO[2], PO[11])

OR

6 a. What are heaps? Which are the different types of heaps? Discuss the applications of heaps. **06 M**
(Level[2], CO[2], PO[2])

b. Explain the concept of threaded binary tree with example and also give the steps for construction. **06 M**
(Level[2], CO[2], PO[2])

c. What is AVL tree? Explain with example. **08 M**
(Level[2], CO[2], PO[11])

UNIT – V

7 a. What is priority queue? Give an application for the same. **04 M**
(Level[2], CO[3], PO[11])

b. Explain Hashing. Explain any two hashing techniques in brief. **08 M**
(Level[2], CO[3], PO[2])

c. What is collision in hashing? Explain liner probing method for overflow handling. **08 M**
(Level[2], CO[3], PO[2])

OR

8 a. Differentiate between single ended and double ended priority queue. **06 M**
(Level[2],CO[3],PO[11])

b. Explain quadratic probing collision resolution method. **06 M**
(Level[2], CO[3], PO[1])

c. Write short notes on binomial heaps. **08 M**
(Level[3], CO[3], PO[11])

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CS36 / IS36

B.E. Fast Track Examination, JULY / AUG. 2016-17

OOP WITH JAVA

Time: 3 Hours **Max. Marks: 100**

Instructions: *1. Unit-I and Unit-II questions are compulsory.*
2. Attempt any one from remaining Unit.

UNIT – I

1 a. Explain the following 1. Data Encapsulation 2.Inheritance 3.Polymorphism **10 M**
(Level[2], CO[2], PO[1])

b. List the operators used in JAVA and explain briefly with an example. **10 M**
(Level[1], CO[2], PO[1])

UNIT – II

2 a. Write JAVA program to create class simple interest. It has data member principal, rate of Interest and duration and member function calculate simple interest and display interest. **10 M**
(Level[2], CO[1], PO[2])

b. What is constructor? Explain different forms constructor with an example.Write JAVA program to demonstrate constructor. **10 M**
(Level[2], CO[2], PO[2])

UNIT – III

3 a. Explain the concept of method overloading? Write a java program to illustrate method overloading. **10 M**
(Level[2], CO[3], PO[2])

b. Write a JAVA program to implement a linear search function by using method overloading concept for an array of integers and double elements. **10 M**
(Level[3], CO[3], PO[2])

OR

4 a. What is visibility modifiers. Explain visibility of the following key words 1. public 2. protected 3.private **10 M**
(Level[2], CO[1], PO[1])

b. Explain static and final keyword in java. **10 M**
(Level[2], CO[2], PO[2])

UNIT – IV

5 a. What is inheritance and explain the different forms of Inheritance. **10 M**
(Level[2], CO[3], PO[2])

b. Write a JAVA program to illustrate inheritance hierarchy. **10 M**
(Level[3], CO[3], PO[2])

OR

6 a. Explain with an example the concept of Inheritance in JAVA with proper syntax. **10 M**
(Level[2],CO[3],PO[2])

b. Explain super keyword in java. Briefly explain the usage of super with a program. **10 M**
(Level[3], CO[3], PO[2])

UNIT –V

7 a. Explain the exception and benefits of exception handling. **10 M**
(Level[2], CO[4], PO[2])

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b. Explain try –catch concept. List some most common types of exceptio ...t might occur in Java. Give examples. **10 M**

(Level[3], (... PO[2])

OR

8 a. Explain the following **10 M**

i) Exception in JAVA ii) finally

(Level[2], (... PO[2])

b. Write JAVA program to illustrate the null pointer exception. **10 M**

(Level[3], (... PO[2])

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15CS/IS34

Third Semester B.E. Semester End Examination, Nov. / Dec. 2016-17
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours Max. Marks: 100

Instructions: 1. *Unit I and II are compulsory.*
2. *Answer any one full question from remaining each units.*

UNIT – I

1 a. With a neat diagram show connection between memory & the processor and explain typical operational steps in executing an instruction. (Level[1], CO[1], PO[3]) 06 M

b. Write a note on byte addressability, big-endian & little-endian assignment. (Level[1], CO[1], PO[2,4]) 05 M

c. Define and Explain any five addressing modes giving its i) Assembler syntax ii) EA calculation with an example in each case. (Level[1,2], CO[1], PO[3]) 09 M

UNIT – II

2 a. What is an interrupt? With example illustrate the concept of interrupts. (Level[1], CO[2], PO[3]) 07 M

b. What is DMA? Explain in brief simple arrangement for a centralized bus arbitration approach (Level[1], CO[2], PO[3]) 06 M

c. With a neat block diagram explain Daisy Chain Interrupt Priority Scheme for handling simultaneous requests. (Level[2], CO[2], PO [3]) 07 M

UNIT - III

3 a. With the help of relevant circuit diagram for static RAM cell, explain how a Read and Write can be performed on it. (Level[2], CO[2], PO[3]) 05 M

b. Illustrate the different mapping functions of cache. (Level[2], CO[2], PO[3]) 10 M

c. Show with diagram the memory hierarchy with respect to speed, size and cost. (Level[1], CO[2], PO[3]) 05 M

OR

4 a. Explain the internal organization of a 2M x 8 asynchronous DRAM chip. (Level[2], CO[2], PO[3]) 10 M

b. Show the configuration of a ROM cell and compare the different ROM memories. (Level[1, 2], CO[2], PO[3]) 10 M

UNIT - IV

5 a. Explain the sequential binary multiplier with the use of block diagram. (Level[2], CO[3], PO[4]) 10 M

b. Write the circuit arrangement for binary division. Solve for the given binary numbers 1000 % 0011 using the restoring division algorithm. (Level[1], CO[3], PO[4]) 10 M

OR

6 a. How do you design FAST ADDERS? Explain a 4 bit carry look ahead adder. (Level[2],CO[3],PO[4]) 05 M

b. Solve the given binary numbers 1000 % 0011 using non-restoring division. (Level[1], CO[3], PO[4]) 10 M

c. Find multiplication of -13 and +11 using booths algorithm. (Level[1], CO[3], PO[4]) 05 M

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UNIT –V

7 a. Define Amdahl's law. Evaluate an expression for overall speedup
(Level[5], CO[4], PO[1]) 07 M

b. Demonstrate the working of a classic five stage pipeline for a RISC processor.
(Level[2], CO[4], PO[1]) 06 M

c. Explain data hazards and methods to minimize data hazards with example. [L2]
(Level[2], CO[4], PO[4]) 07 M

OR

8 a. Define Computer Architecture. Illustrate the seven dimensions of an ISA.
(Level[2], CO[4], PO[1]) 10 M

b. List the major hurdles of pipelining. Explain the branch hazards in detail.
(Level[4], CO[4], PO[4]) 10 M

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15CS/IS35

Third Semester B.E. Semester End Examination, Nov. / Dec. 2016-17

DATA STRUCTURES USING C

Time: 3 Hours

Max. Marks: 100

Instructions: 1. *Answer five full question choosing one from each unit.*
2. *UNIT-I and UNIT-II are compulsory.*
3. *Answer any ONE full question from remaining each UNITS*

UNIT - I

a. With syntax and example, compare the two dynamic memory allocation functions. 04 M
(Level[5], CO[1], PO[1])

b. Design a program to store n given integers in an array and print their average. The array should be accessed only through its pointer. 08 M
(Level[6], CO[2], PO[2])

c. Explain the recursive definition of GCD. Hence design a recursive C function to compute the GCD of two integers. 08 M
(Level[6], CO[1], PO[1])

UNIT - II

a. Develop C functions for the following tasks in a circular queue: 08 M
i) queuefull ii) queueempty iii) addqueue iv) deletequeue
(Level[6], CO[3], PO[1])

b. Construct a C program to convert infix expression to postfix expression 08 M
(Level[3], CO[2], PO[1])

c. Find postfix forms of the following expressions: 04 M
i) $-a + b - c + d$ ii) $(a + b) * d + e / (f + a * d) + c$
(Level[1], CO[1], PO[1])

UNIT-III

a. Define a linked list. List its advantages and disadvantages. 04 M
(Level[1], CO[3], PO[1])

b. Develop a C function for the following: Let *P* be a pointer to the first node in a singly linked list. The first, third, fifth,.... nodes should be deleted. 08 M
(Level[6], CO[2], PO[2])

c. Explain doubly linked list. Develop a C function to traverse the doubly linked list from left to right printing out the contents of the data field of each node 08 M
(Level[6], CO[1], PO[2])

OR

a. Explain a circular singly linked list with an example. 06 M
(Level[2], CO[2], PO[1])

b. Develop a function to invert a singly linked list. 08 M
(Level[6], CO[2], PO[2])

c. The following C function takes a singly-linked list as input argument. It modifies the list by moving the last element to the front of the list and returns the modified list. Some part of the code is left blank. Determine the statement(s) to replace the blank line. 06 M

```
typedef struct node
{
 int value;
 struct node *next;
}Node;
Node *move_to_front(Node *head)
{
 Node *p, *q;
 if ((head == NULL: || (head->next == NULL))
  return head;
 q = NULL; p = head;
 while (p-> next !=NULL)
```

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```
}
{
  q = p;
  p = p->next;
}
return head;
}
```

(Level[5], CO[2],PO [1])

UNIT -IV

5 a. Show the tree corresponding to the following notation: 06 M
(A(B(E(K,L),F),C(G),D(H(M),I,J)))

(Level[2], CO[1], PO[1])

b. Prove that a full binary tree of depth k is a binary tree of depth k having 2^k-1 nodes where k>=0 06 M

(Level[5], CO[3], PO[2])

c. Show the inorder, preorder, postorder and levelorder traversals for the binary tree of figure Q5(c) 08 M

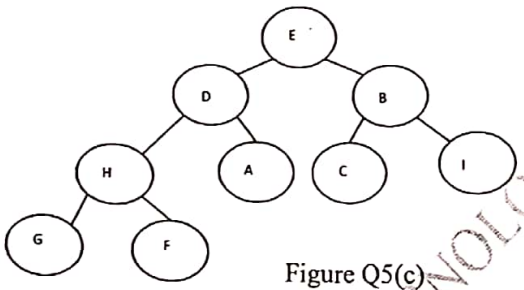

Figure Q5(c)

(Level[2], CO[1], PO[1])

OR

6 a. Construct the binary tree and write the post-order traversal whose in- and pre- order traversals are as follows: 08 M
In-order traversal GHFDAECBI
Pre-order traversal EDHGFABCI

(Level[6], CO[3], PO[2])

b. Suppose that we have the following key values: 7,16,49,82,5,31,6,2,44 08 M
i) Construct the max heap after each value is inserted into the heap
ii) Construct the min heap after each value is inserted into the heap

(Level[6], CO[3], PO[2])

c. Define balance factor of a node in a binary tree. Illustrate with an example. 04 M

(Level[2], CO[1], PO[2])

UNIT - V

7 a. Explain the concept of priority queues. 06 M

(Level[2], CO[3], PO[1])

b. Illustrate how collisions occur and list the methods to resolve them. 08 M

(Level[2], CO[4], PO[1])

c. Develop a step wise procedure to delete the minimum element from binary heap. 06 M

(Level[6], CO[4], PO[1])

OR

8 a. Define and explain the binomial heap with example. 04 M

(Level[2],CO[4],PO[1])

b. Compare quadratic probing and pseudorandom collision resolution methods. 08 M

(Level[5], CO[4], PO[1])

c. Using the linked list method, store the keys shown below in an array with 19 elements. List the number of collisions that occur. 08 M

224562	137456	214562
140145	214576	162145
144467	199645	234534

(Level[4], CO[4], PO[2])

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15CS/IS36

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Third Semester B.E. Semester End Examination, Nov. / Dec. 2016-17

OBJECT ORIENTED PROGRAMMING WITH JAVA

Time: 3 Hours Max. Marks: 100

Instructions: 1. *Unit-I and Unit-II are Compulsory.*
2. *Answer any one full question from remaining each units.*

UNIT – I

1 a. Explain the object oriented principles with an example. (Level[2], CO[2], PO[1]) 10 M

b. Explain the following with respect to JAVA programming 10 M
i) Portable
ii) Object-Oriented
iii) Distributed
iv) Multithreaded
v) Byte code

(Level[2], CO[2], PO[1])

UNIT – II

2 a. Explain the syntax of declaring a *class* and an *object* in JAVA with an example. Write a JAVA program to create a class Circle, which has data member radius and member functions to compute the area of circle and display the area. (Level[2], CO[1], PO[2]) 10 M

b. What is a constructor? Explain different forms of constructor with an example. Write a JAVA program to demonstrate parameterized constructor. (Level[2], CO[2], PO[2]) 10 M

UNIT – III

3 a. Explain access control specifiers in JAVA with examples (Level[2], CO[1], PO[2]) 10 M

b. Write a JAVA program to carry out following operations on a string object: 10 M
a) Reverse a string
b) Find the number of occurrences of a sub string

(Level[3], CO[1], PO[1])

OR

4 a. Write a JAVA program to implement a linear search function by using method overloading concept for an array of integers and double elements. (Level[3], CO[3], PO[2]) 10 M

b. What is method overloading? Explain the features of method overloading in Java. Write a Java program to overload a method called "ADD" that adds and returns the result of adding two integer values, two double values. (Level[2], CO[3], PO[2]) 10 M

UNIT – IV

5 a. What is inheritance and explain the different forms of Inheritance. (Level[2], CO[3], PO[2]) 10 M

b. Write a JAVA program Implement inheritance hierarchy for students, UG student and PG student and also implement methods to find top scorer in UG and PG students. Demonstrate the program for at least 10 students. (Level[3], CO[3], PO[2]) 10 M

OR

6 a. Explain with an example the concept of Inheritance in JAVA with proper syntax. (Level[2], CO[3], PO[2]) 10 M

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b. Write a JAVA program to implement inheritance. The program has a class called Shape2D and Data members length and breadth, member function area. Class called Shape3D extends Shape2D which it has data member height and member function volume of shape. Display area of Shape2D and volume of Shape3D. **10 M**

(Level[3], CO[3], PO[2])

UNIT –V

7. a. What is an exception? List some most common types of exceptions that might occur in Java. Give examples. **10 M**

(Level[1], CO[4], PO[2])

b. Create a try block that is likely to generate three types of exceptions and then incorporate necessary catch blocks to catch and handle them appropriately. **10 M**

(Level[3], CO[4], PO[2])

OR

8 a. Explain the following **10 M**

i) Exception in JAVA ii) Try and catch block

(Level[2], CO[4], PO[2])

b. Write a JAVA program to illustrate : **10 M**

i) Arithmetic exception. ii) Array Index Out Of Bound Exception.

(Level[3], CO[4], PO[2])

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15MAT31

Third Semester B.E. Semester End Examination, Nov. / Dec. 2016-17

ENGINEERING MATHEMATICS III

Time: 3 Hours **Max. Marks: 100**

Instructions: 1. *Answer FIVE full questions.*
2. *Units III and V are compulsory*
3. *choose one full question from each the remaining units*

UNIT - I

1 a. Use Regula falsi method to find a real root of the equation $x^3 - 2x - 5 = 0$. Correct to three decimal places. **06 M**

(Level[3], CO[1], PO[1])

b. Find the real root of the equation $3x = \cos x + 1$ using Newton-Rophson method taking initial approximation $x_0 = 0.6$. Perform three iterations. **07M**

(Level[1], CO[1], PO[1])

c. Apply fixed point iteration method to find the root of the equation $\cos x = 2x - 3$ up to 3 decimal places. **07 M**

(Level[3], CO[1], PO[1])

OR

2 a. Use Taylor's series method up to 4th derivatives to obtain y(0.1), given that $\frac{dy}{dx} = xy + 1, y(0) = 1$ **06 M**

(Level[3], CO[1], PO[1])

b. Use Euler's modified method to find the solution at $x = 0.1$ correct to four decimal places of the differential equation $\frac{dy}{dx} = x + y$, and y=1 when $x = 0$ **07 M**

(Level[3], CO[1], PO[1])

c. Apply Runge-Kutta method of fourth order to solve $\frac{dy}{dx} = x + y^2$ given that y=1 when $x = 0$ at $x = 0.2$ in one step. **7 M**

(Level[2], CO[1], PO[1])

UNIT – II

3 a. Construct Fourier series for the function $f(x) = x + x^2 \quad -\pi \le x \le \pi$ **07 M**

(Level[3], CO[2], PO[2])

b. Transform the function $f(x) = x \sin x \quad 0 < x < \pi$ into half range Fourier sine series **07 M**

(Level[2], CO[1], PO[1])

c. Represent the following function in Fourier series up to first harmonic. **06 M**

x	0	π/3	2π/3	π	4π/3	5π/3	2π
y	1	1.4	1.9	1.7	1.5	1.2	1

(Level[2], CO[2], PO[2])

OR

4 a. Construct Fourier series for the function $f(t) = 1 + t^2 \quad -1 \le t \le 1$ **07 M**

(Level[3], CO[2], PO[1])

b. Transform the function $f(x) = x \sin x \quad 0 \le x \le \pi$ into half range Fourier sine series **07 M**

(Level[2], CO[2,] PO[2])

c. Represent the following function in Fourier sine series up to second term. **06 M**

x	0	1	2	3	4	5	6
y	5	6	9	7	4	11	5

(Level[2], CO[2], PO [1])

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UNIT – III

5 a. Fit a straight line $y = a + bx$ by least square method to the data **06 M**

x:	50	70	100	120
y:	12	15	21	25

(Level[2], CO[3], PO[1])

b. Find the parabola of the form $y = a + bx + cx^2$ which fits the following data by the method of least squares. **07 M**

x:	-3	-2	-1	0	1	2	3
y:	4.63	2.11	0.67	0.09	0.63	2.15	4.58

(Level[2], CO[3], PO[1])

c. Find the correlation coefficient and the lines of regression for the following data **07 M**

x:	1	2	3	4	5
y:	2	5	3	8	7

(Level[2], CO[3], PO[1])

UNIT – IV

6 a. If the following represents valid p.d.f. then calculate k, mean and s.d. **07 M**

X	0	1	2	3	4	5	6
P(X)	k	$3k$	$5k$	$7k$	$9k$	$11k$	$13k$

(Level[1], CO[4], PO[2])

b. Demonstrate that mean and variance of an exponential distribution are $1/\alpha$ and $1/\alpha^2$ respectively **07 M**

(Level[2], CO[4], PO[1])

c. Under the normal distribution 7% are below 35 and 89% are less than 60 identify the mean and standard deviation . Given A(z =1.2263)=0.39 and A(z =1.4757)=0.43 **06 M**

(Level[3], CO[4], PO[2])

OR

7 a. If the following represents a valid p.d.f. then compute k , P (0<x<1), P(–0.3< x <0.3) **07 M**

$$p(x) = k(x+1) \quad -1 \le x \le 1$$
$$= 0 \quad \text{elsewhere.}$$

(Level[1], CO[4], PO[1])

b. Demonstrate that mean and variance of a binomial distribution are 'np' and 'npq' respectively **07 M**

(Level[2], CO[4], PO[2])

c. The mean of an exponential distribution is 5, identify $E(x^2)$, $P(1 < x < 4)$, $P(x > 5)$ **06 M**

(Level[2], CO[4], PO[1])

UNIT –V

8 a. The joint distribution of two random variables x and y is given by the following table **06 M**

x/y	0	1
0	0.1	0.2
1	0.4	0.2
2	0.1	0

Determine the marginal distribution of x and y
Verify whether x and y are independent.

(Level[2], CO[5], PO[1])

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b. Each year a company executive changes his car. If he has a car of make A, he changes over to car of make B. If he has a car of make B, he changes over to car of make C. If he has a car of make C, he is just likely to change over to a car of make C. He is just likely to change over to a car of make C, B or A. Find transition matrix. If he uses the car C on the first year find the probability that he has car i) A, ii) B, iii) C on third year. **07 M**

(Level[2], CO[5], PO[1])

c. Define stochastic process with an example. Also state the four types of stochastic process. **07 M**

(Level[2], CO[5], PO[1])

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15CS/IS35

Third Semester B.E. Makeup Examination, Dec. 2016-17

DATA STRUCTURES USING C

Time: 3 Hours

Max. Marks: 100

Instructions:
1. *Answer one full question from each UNIT.*
2. *UNIT-I and UNIT-II are compulsory*
3. *Answer any ONE full question from remaining each UNITS.*

UNIT - I

1 a. Explain the dynamic memory allocation functions with syntax and an example each. **08 M**

(Level[2], CO[2], PO[1])

b. Construct the following function to printout all possible permutations of the string *list* and trace the function for the string set {a,b,c}. **08 M**

*void perm(char *list, int i ,int n)*

{ _____

_____

}

(Level[6], CO[1], PO[2])

c. Define ADT. Hence develop ADT for array. **04 M**

(Level[6], CO[1], PO[1])

UNIT – II

2 a. Define Stack. Develop a modular C program to implement stack using dynamic array. **08 M**

(Level[6], CO[3], PO[1])

b. Build the following table according steps in the comments column pertaining to simple queue: **06 M**

front	rear	Q[0]	Q[1]	Q[2]	Q[3]	Comments
-1	1	J1	J2			Initial status
-1	2	J1	J2	J3		J3 is added
-1	3	J1	J2	J3	J4	J4 is added
0	3		J2	J3	J4	J5 is added
1	3			J3	J4	Delete
1	4				J5	Delete
						Add J5

(Level[3], CO[3], PO[1])

c. Evaluate the postfix expression **6 2 / 3 – 4 2 * +** where each operand is a single digit positive integer. Show the steps in the form of a table. **06 M**

(Level[5], CO[2], PO[2])

UNIT-III

3 a. List the capabilities to make linked representations possible. **04 M**

(Level[1], CO[1], PO[2])

b. Construct a C function for the following: *P* is a pointer to the first node of a singly linked list that stores a word. Each letter is stored in a node. Determine whether the word pointed to by *P* is a palindrome or not. **08 M**

(Level[6], CO[2], PO[1])

c. Develop C functions for the following operations in a linked stack: **08 M**

i) push an item *x* in to the stack

ii) pop an item from the stack

(Level[6], CO[1], PO[2])

OR

4 a. Explain the linked list concept with example **04 M**

(Level[2], CO[1], PO[1])

b. The following C function takes a single-linked list of integers as a parameter and rearranges the elements of the list. The function is called with the list containing the integers 1, 2, 3, 4, 5, 6, 7 in the given order. What will be the contents of the list after the function completes execution? **08 M**

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```
struct node
{
 int value;
 struct node *next;
};
void rearrange(struct node *list)
{
 struct node *p, * q;
 int temp;
 if ((!list) || !list->next)
    return;
 p = list;
 q = list->next;
 while(q)
 {
  temp = p->value;
  p->value = q->value;
  q->value = temp;
  p = q->next;
  q = p?p->next:0;
 }
}
```

(Level[6], CO[1], PO[1])

c. Develop a C function to print the contents of each node in a singly linked list and also to print the number of nodes. **08 M**

(Level[6], CO[3],PO [2])

UNIT - IV

5 a. Define a binary tree and give an example. **04 M**

(Level[2], CO[1], PO[1])

b. Show that for any non empty binary tree T, if n_0 is the number of leaf nodes and n_2 is the number of nodes of degree 2, then $n_0 = n_2 + 1$. **08 M**

(Level[2], CO[2], PO[2])

c. Define max heap. Develop a C function to insert into a max heap. **08 M**

(Level[6], CO[3], PO[2])

OR

6 a. Explain the concept of threaded binary tree with a diagram. **06 M**

(Level[2], CO[2], PO[1])

b. Develop a C function to insert an element into a binary search tree. **08 M**

(Level[6], CO[1], PO[2])

c. Define and explain the height balanced binary tree with an example. **06 M**

(Level[2], CO[1], PO[1])

UNIT - V

7 a. Distinguish between single ended priority queue and double ended priority queues **06 M**

(Level[4], CO[1], PO[1])

b. Explain hashing. List the various hashing methods. **08 M**

(Level[2], CO[4], PO[2])

c. What is hash collision? Explain the linear probing method of hash collision. **06 M**

(Level[2], CO[4], PO[1])

OR

8 a. Explain the operations supported by DEPQ. **04 M**

(Level[2],CO[4],PO[1])

b. Summarize the direct hashing method with an example. **08 M**

(Level[2], CO[4], PO[2])

c. Using the modulo division method and linear probing, store the keys shown below in an array with 19 elements. List the number of collisions that occur. **08 M**

224562	137456	214562
140145	214576	162145
144467	199645	234534

(Level[4], CO[4], PO[2])

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Fourth Semester B.E. Degree Examination, June/July 2016
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. List the steps needed to execute the machine instruction given below in terms of transfers between the components of processor, memory and some control commands. ADD LOCA, R0. Assume the instruction is stored in memory location 'INSTR'. **(05 Marks)**

b. Perform the following operations on the 5-bit signed numbers using 2's complement representation system. Further indicate whether overflow has occurred.
i) (-10) + (-13) ii) (-10) – (+4) iii) (+7) – (-15) iv) (+8) + (+10). **(10 Marks)**

c. Write the basic performance equation. Explain the role of each of the parameters in the equation on the performance of the computer. **(05 Marks)**

2 a. Define addressing mode and explain any four addressing modes with an example for each. **(09 Marks)**

b. What is subroutine linkage? With examples explain different ways of passing parameters to subroutine. **(06 Marks)**

c. Explain in detail encoding of machine instructions into 32-bit words. Assume that there are 16 registers in the processor. **(05 Marks)**

3 a. Define interrupt. What are the overheads incurred in handling interrupts? **(04 Marks)**

b. With neat sketches explain a method for handling interrupts from multiple devices. **(10 Marks)**

c. What is bus arbitration? With a neat diagram, explain any one approach used for bus arbitration. **(06 Marks)**

4 a. With a block diagram, explain a general 8-bit parallel interface. **(10 Marks)**

b. List out widely used bus standards in a computer system. Further, explain the READ operation using PCI bus with a timing diagram. **(10 Marks)**

PART – B

5 a. What is a cache? Explain any two cache mapping functions with neat sketches. **(10 Marks)**

b. What is a virtual memory? With a neat diagram, explain the method for translating virtual address to physical address. **(10 Marks)**

6 a. Explain the design of a 4-bit carry-look ahead adder. **(08 Marks)**

b. Multiply (+14) and (-6) using Booth's algorithm. **(07 Marks)**

c. Perform the division of number 8 by 3 (8 ÷ 3) using restoring division method. **(05 Marks)**

7 a. Write the sequence of control steps to execute the instruction, ADD (R_3), R_1 on single bus architecture. **(07 Marks)**

b. With a block diagram, describe the organization of a micro programmed control unit. **(10 Marks)**

c. Bring out the differences between micro programmed control and Hard-Wired control. **(03 Marks)**

8 a. Explain any two shared memory multiprocessor models. **(10 Marks)**

b. Briefly explain SISD and SIMD architectures with neat diagrams. **(10 Marks)**

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10CS33

Third Semester B.E. Degree Examination, June/July 2016
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Name universal gates. Realize basic gates using NAND gate only. **(08 Marks)**

b. Prove that symmetrical signal has a duty cycle of 50% and find the frequency, low and high duty cycles for asymmetrical signal if it is high for 3 ms and low for 4 ms. **(08 Marks)**

c. Explain the structure of VHDL/Verilog program. **(04 Marks)**

2 a. Find the SOP of the following Boolean function using K – map :

i) $f(p\ q\ r\ s) = \Sigma m(6, 7, 9, 10, 11, 13) + d(0, 1, 8, 12)$

ii) $f(a\ b\ c\ d) = \pi m\ (1, 2, 4, 9, 10, 12) + d(0, 3, 5)$. **(08 Marks)**

b. Simplify $f(A\ B\ C\ D) = \Sigma m(0, 1, 2, 3, 5, 8, 12, 14, 15)$ using Quine – McClusky method. **(12 Marks)**

3 a. Design a 16 : 1 multiplexer using two 8 : 1 multiplexers and one 2 : 1 multiplexers with expressions. **(06 Marks)**

b. With relevant diagram explain n-bit magnitude comparator. **(08 Marks)**

c. Give HDL implementation for 4 : 1 MUX using 'case' statement. **(06 Marks)**

4 a. What do you mean by characteristic equation of 'Flip-flop'? Draw the logic diagram, truth table and explain working of 'JK – Flip – Flop' and implement the same using NAND gate. **(12 Marks)**

b. With state table and state transition diagram, analyse the behaviour of sequential circuit shown in Fig. Q4(b). **(08 Marks)**

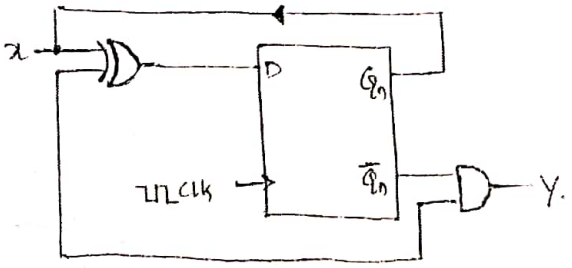

Fig. Q4(b)

PART – B

5 a. With a neat logic and timing diagram, explain the working of a 4 – bit SISO register. **(10 Marks)**

b. Design two 4 – bit number serial adder. **(06 Marks)**

c. Write verilog HDL code for 4 – bit SIPO shift register. **(04 Marks)**

6 a. Design synchronous modulus – 5 (mod -5) counter using JK – Flip-Flop. **(10 Marks)**

b. Explain, design of 4 – bit binary ripple – up counter using negative edge triggered JK – flip-flops with block diagram and timing diagram. **(10 Marks)**

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7 a. With neat diagram explain and compare Mealay and Moore machine. **(10 Marks)**

b. Reduce state transition diagram (Moore model) of Fig. Q7(b) by i) Row elimination method ii) implication table method. **(10 Marks)**

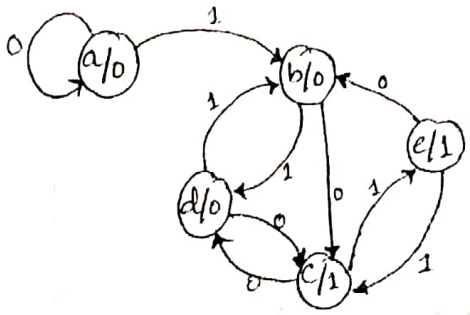

Fig. Q7(b)

8 a. Discuss the two drawbacks of resistive divider used in converting D/A. Draw the schematic for a 4–bit binary ladder and explain how the digital to analog conversion is achieved using it. **(10 Marks)**

b. Discuss the working of following A/D converters :

i) Successive approximation A/D

ii) Counter type A/D. **(10 Marks)**

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10CS35

Third Semester B.E. Degree Examination, June/July 2016
Data Structures with C

Time: 3 hrs. Max. Marks:100

Note: *Answer any FIVE full questions, selecting atleast TWO questions from each part.*

2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

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PART – A

1 a. Write a recursive function to print the permutation of a string (ABC) passed to it as an argument. **(06 Marks)**

b. What is the purpose of using free( )? With an example explain the problem that occur when free( ) is not used. **(04 Marks)**

c. Obtain the step count for the C – function to add two matrices of M × N size using counting method and tabular method.

```
void add_matrix(int a[ ][MAX_SIZE], int b[ ][MAX_SIZE], int c[ ][MAX_SIZE], int m, int n)
{ int i, j ;
    for (i = 0 ; i < m; i ++)
    {
        for (j = 0 ; j < n; j++)
        {
            C[i][j] = a[i][j] + b[i][j] ;
        }
    }
}
```

(04 Marks)

d. Explain how memory can be dynamically allocated using realloc( ). **(06 Marks)**

2 a. Explain how address calculation is done in row major ordering for a 2–dimensional array. Also generalize for n–dimension. **(04 Marks)**

b. Describe unions used in C. How is it different from structures? **(06 Marks)**

c. Design an algorithm to add two polynomials using ADT polynomial. **(05 Marks)**

d. With the help of an example, explain sparse matrix. How the sparse matrix is represented in memory. Design the algorithm to transpose a given matrix represented as triples in a 1–D array. **(05 Marks)**

3 a. Write an algorithm to evaluate a postfix expression. Use a stack to evaluate the following postfix arithmetic expression. Show the changing status of the stack in tabular form. (AB + C – B A + C $–)for given A = 1, B = 2, C = 3. **(06 Marks)**

b. Differentiate between stack and queue. How are they related to LIFO and FIFO concept? **(06 Marks)**

c. Write a program to check whether a given string is palindrome or not using stack. **(04 Marks)**

d. What is the disadvantage of queue which is implemented using array and how to overcome it? **(04 Marks)**

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4 a. Write a program that create a linked list consisting of nodes of the following struct type and searches the record of a student whose roll_number is given by the user.

```
sturct student
{
    char name [15];
    int roll_no ;
    struct student *next ;
} ;
```

(10 Marks)

b. List out the difference between singly linked list and doubly linked list. What are the advantages of circular list? **(05 Marks)**

c. Explain how to reverse and invert a given singly linked list with an example and write its C-function. **(05Marks)**

PART – B

5 a. Write a C – function to insert an item into a binary tree based on direction. **(06 Marks)**

b. Define max-heap and min-heap. How will you represent a max-heap as an array? Write an algorithm to insert an element to a max-heap. Create a max-heap : 100 200 –10 –30 –60 80 90 300. **(08 Marks)**

c. List various types of threaded binary trees. Explain in-threaded binary tree. **(06 Marks)**

6 a. Suppose the following list of number is inserted in order into an empty binary search tree(BST) 70 80 60 65 50 45 55,

i) Construct the binary search tree

ii) Find in order, pre-order and pos-order traversal of BST created

iii) Is the BST constructed at AVL tree? State reasons for your claim. Further if your answer is negative balance the tree so that it becomes an AVL tree. **(10 Marks)**

b. Explain the activities to be performed to delete a node from a binary tree and write C–function to delete an item from the tree. **(10 Marks)**

7 a. Obtain the shortest(x) and weight(x) for each node in the following binary trees and identify which is height – based leftist tree and which is weight–based leftist tree. **(10 Marks)**

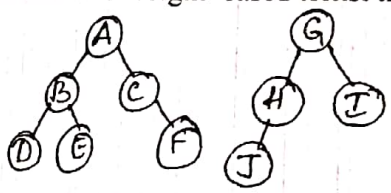

Fig. Q7(a)

b. Construct an AVL tree by inserting the elements MAR, MAY, NOV, AUG, APRIL, JAN, DEC, JULY, FEB, JUNE, OCT, SEPT. **(10 Marks)**

8 a. Obtain the optimal binary search tree for the following items and associated probability.

Keys	10	15	20	25
Probability	3	3	1	1.

(10 Marks)

b. Define RED–BLACK trees. Consider the red–black tree shown below and insert the item 50 into the tree and write the final red–black tree. **(10 Marks)**

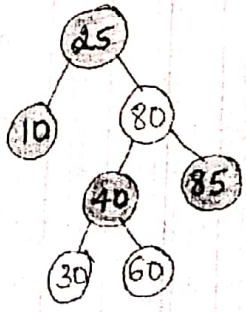

Fig. Q8(b)

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Fourth Semester B.E. Degree Examination, June/July 2018
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. With a neat diagram, explain the different processor registers. **(08 Marks)**
b. List and explain the technological features and devices improvement made during different generations of computers. **(08 Marks)**
c. What are the factors that affect the Performance? Explain any four. **(04 Marks)**

2 a. What is an addressing mode? Explain any four addressing modes, with an example for each. **(08 Marks)**
b. Explain shift and rotate operations with example. **(08 Marks)**
c. Explain Big – endian and Little – endian method of byte addressing with an example. **(04 Marks)**

3 a. Define Exceptions. Explain two kinds of exceptions. **(04 Marks)**
b. Define bus arbitration. Explain in detail any one approach of bus arbitration. **(08 Marks)**
c. Draw and explain the general 8 bit parallel processing. **(08 Marks)**

4 a. Explain the following with respect to USB : i) USB Architecture ii) USB Addressing iii) USB Protocols. **(09 Marks)**
b. Briefly discuss the main phases involved in the operation of SCSI bus. **(06 Marks)**
c. Explain distributed Bus arbitrations. **(05 Marks)**

PART - B

5 a. Define : i) Memory Latency ii) Memory bandwidth iii) Hit – rate iv) Miss - Penalty. **(04 Marks)**
b. Explain the different cache mapping functions. **(10 Marks)**
c. Explain any one feature of memory design that leads to improved performance of computer. **(06 Marks)**

6 a. With a neat diagram, explain the virtual memory organization. **(08 Marks)**
b. Design a logic circuit to perform addition / subtraction of two 'n' bit numbers X and Y. **(04 Marks)**
c. Explain Booth Algorithm. Apply Booth Algorithm to multiply the signed numbers +13 and -6. **(08 Marks)**

7 a. Explain the different arithmetic operations on floating point numbers. **(06 Marks)**
b. Perform division of number 8 by 3 (8 ÷ 3) using the restoring division algorithm. **(06 Marks)**
c. Explain the process of fetching a word from memory along with a timing diagram. **(08 Marks)**

8 a. Briefly explain the structure of General Purpose Multiprocessor. **(08 Marks)**
b. List different types of Networks. Explain any four. **(08 Marks)**
c. Give a brief description on performance consideration with an example. **(04 Marks)**

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10ES33

Third Semester B.E. Degree Examination, Dec.2015/Jan.2016
Logic Design

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. Define combinational logic. Two motors M_2 and M_1 are controlled by three sensors S_1, S_2 and S_3. One motor M_2 is to run any time when all three sensors are on. The other motor (M_1) is to run whenever sensors S_2 or S_1 but not both are on and S_3 is off. For all sensors combinations where M_1 is on, M_2 is to be off, except when all sensors are off and then both motors remain off. Construct the truth table and write the Boolean output equation. **(05 Marks)**

b. The following Boolean function into their proper canonical form in decimal notation.
i) $M = p(q' + s)$
ii) $N = (w' + x)(y + z)$ **(07 Marks)**

c. Reduce the following Boolean function using K-map and realize the simplified expression using NAND gates.
$T = f(a,b,c,d) = \sum m(1,3,4,5,13,15) + \sum d(8,9,10,11)$ **(08 Marks)**

2 a. Simplify the following function using Quine-McClusky method and realize the simplified using NOR gates.
$P = f(w,x,y,z) = \sum m(7,9,12,13,14,15) + \sum d(4,11)$ **(12 Marks)**

b. Simplify $f(a,b,c,d) = \sum m(0,4,5,6,13,14,15) + \sum d(2,7,8,9)$ using MEV technique using basic gates. **(08 Marks)**

3 a. Design a combinational circuit to find the 9's complement of a single digit BCD number. Realize the circuit using suitable logic gates. **(08 Marks)**

b. Draw the logic diagram for 2 to 4 line decoder with an active low encoder enable and active high data output. Construct a truth table and describe the circuit function with logic symbol (74139IC's) for the decoder. **(06 Marks)**

c. Design a 4 to 16 line decoder using 2 to 4 line decoder which has the active low outputs and active low enable input. Explain its operation. **(06 Marks)**

4 a. Design a binary full adder using only two input NAND gates. Write a truth table. **(06 Marks)**

b. Implement the following Boolean function using 4 : 1 multiplexer (MUX)
$Y = f(A,B,C,D) = \sum m(0,1,2,4,6,9,12,14)$ **(06 Marks)**

c. Define magnitude comparator. Design a two-bit binary comparator and implement with suitable logic gates. **(08 Marks)**

PART – B

5 a. Discuss the difference between a flip flop and latch. Explain the operation of gated SR latch with a logic diagram, truth table and logic symbol. **(06 Marks)**

b. Explain the working of Master Slave JK flip flops with functional table and timing diagram. Show how race around condition is overcome. **(08 Marks)**

c. Obtain the characteristic equation of JK and SR flipflops. **(06 Marks)**

2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

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6 a. Describe the block diagram of a MOD-7 twisted ring counter and explain its operation with the count sequence table and decoding logic used to identify the various states. **(08 Marks)**

b. Design a mod-6 synchronous counter using clocked JK flipflops, the count sequence being 0, 2, 3, 6, 5, 1, 0, 2..... **(12 Marks)**

7 a. With a suitable block diagram, explain the Mealy and Moore model, in a sequential circuit analysis. **(10 Marks)**

b. Explain 4 bit universal shift Register using 4 : 1 MUX with help of logic diagram. Write a mode control table. **(10 Marks)**

8 a. Describe the following terms with respect to sequential machines:
i) State ii) Present states iii) Next states. **(06 Marks)**

b. A sequential circuit has one input one output. The state diagram is shown in Fig. Q8 (b). Design a sequential circuit with T flip flops. **(14 Marks)**

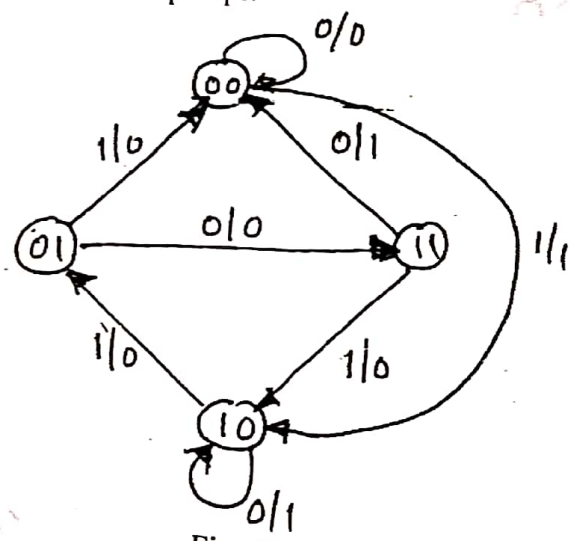

Fig. Q8 (b)

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10CS35

Third Semester B.E. Degree Examination, Dec.2015/Jan.2016
Data Structures with C

Time: 3 hrs. Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. Explain the functions supported by C to carry out dynamic memory allocation with example. **(06 Marks)**

b. What is recursion? What are the various types of recursion? Write a recursive function to implement binary search. **(07 Marks)**

c. Define the term "Space and time complexity". Determine the time complexity of an iterative and recursive functions that adds n elements of an array using tabular method. **(07 Marks)**

2 a. Write a note on dynamically allocated array's with example. **(06 Marks)**

b. How would you represent two sparse polynomials using array of structures and also write a function to add two polynomials and give the analysis of the function. **(10 Marks)**

c. For the given sparse matrix A and its transpose, give the triplet representation 'A' is the given sparse matrix and 'B' will be its transpose.

$$\text{Sparse matrix } A = \begin{bmatrix} 25 & 0 & 0 & 11 & 0 & -10 \\ 0 & 12 & 3 & 0 & 0 & 0 \\ 0 & 0 & 0 & 6 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 81 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -18 & 0 & 0 & 0 \end{bmatrix}.$$ **(04 Marks)**

3 a. Define stack. Implement push and pop functions for stacks using arrays. **(05 Marks)**

b. Write the postfix form of the following expressions using stack:

i) A$B * C – D + E / F / (G + H)

ii) A – B/(C * D$E) **(06 Marks)**

c. What is the advantage of circular queue over linear queue? Write insert and delete functions for circular implementation of queues. **(05 Marks)**

d. Evaluate the following postfix expression 6 2 3 + - 3 8 2 / + * 2 $ 3 + using stack. **(04 Marks)**

4 a. Write C functions to implement the insert and delete operations on a queue using linked list. **(08 Marks)**

b. With the node structure show how would you store the given polynomials a and b in linked list? Write a C function for adding 2 polynomials using linked lists. **(08 Marks)**

c. Write a note on doubly linked list. How is it different from single linked list? **(04 Marks)**

PART – B

5 a. What is binary tree? State its properties. How it is represented using array and linked list? Give example. **(08 Marks)**

b. Show the binary tree with the arithmetic expression A / B * C * D + E. Give the algorithm for inorder, preorder, postorder traversals and show the result of these traversals. **(08 Marks)**

c. What is heap? Explain different types of heap. **(04 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

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6 a. Define binary search tree. Draw the binary search tree for the following input 14, 15, 4, 9, 7, 18, 3, 5, 16, 4, 20, 17, 9, 14, 5 (07 Marks)

b. Construct a binary tree having the following sequences:
   i) Preorder seq ABCDEFGHI
   ii) Inorder seq BCAEDGHFI (05 Marks)

c. Write a iterative search routine for a binary search tree. (05 Marks)

d. Define the following terms:
   i) Forests
   ii) Graphs
   iii) Winner trees. (03 Marks)

7 a. Briefly explain the following with examples:
   i) HBLT ii) WBLT (08 Marks)

b. Write short notes on:
   i) Priority queues ii) Binomial heaps iii) Priority heaps iv) Fibonacci heaps. (12 Marks)

8 Write short notes on:
a. AVL trees.
b. Red-black trees.
c. Optimal binary search trees.
d. Splay trees. (20 Marks)

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10CS46

Fourth Semester B.E. Degree Examination, Dec.2013/Jan.2014
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

a. Explain with necessary block diagram the basic functional unit of a computer. **(10 Marks)**
b. Explain in detail the generation of computers. **(10 Marks)**

a. Big-Endian and Little-Endian assignments, explain with necessary figure. **(05 Marks)**
b. List the name, assembler syntax and addressing functions for the different addressing modes. **(10 Marks)**
c. Explain logical and arithmetic shift instructions with an example. **(05 Marks)**

a. Draw the arrangement of a single bus structure and brief about memory mapped I/O. **(05 Marks)**
b. Explain: i) Interrupt enabling; ii) Interrupt disabling; iii) Edge triggering, with respect interrupts. **(10 Marks)**
c. Draw the arrangement for bus arbitration using a daisy chain and explain in brief. **(05 Marks)**

a. Draw the hardware components needed for connecting a keyboard to a process and explain in brief. **(10 Marks)**
b. Explain the use of PCI bas in a computer system with necessary figure. **(05 Marks)**
c. List the SCSI bus signals with their functionalities. **(05 Marks)**

PART – B

a. Draw for 1K × 1 memory chip with neat figure. **(10 Marks)**
b. Show with diagram the memory hierarchy with respect to speed, size and cost. **(05 Marks)**
c. With figure explain about direct mapping cache memory. **(05 Marks)**

a. Explain with figure the design of a 4-bit carry look ahead adder. **(10 Marks)**
b. With figure explain circuit arrangements for binary division. **(05 Marks)**
c. IEEE standard for floating point numbers, explain. **(05 Marks)**

a. Draw and explain the single-bus organization of the data path inside a processor. **(10 Marks)**
b. Write the control sequence for an un-conditional branch instruction. **(05 Marks)**
c. Draw the block diagram of the control unit organization and describe in brief. **(05 Marks)**

a. Explain in brief about multiprocessor systems. **(05 Marks)**
b. Explain about memory organization in multiprocessors. **(10 Marks)**
c. What are the classifications of parallel processing? **(05 Marks)**

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10CS33

Third Semester B.E. Degree Examination, Dec. 2013/Jan. 2014
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With the aid of the circuit diagram, explain the operation of 2 – input TTL NAND gate. (08 Marks)

b. What are universal gates? Implement the following function using universal gates only $\left(\overline{(A+B)\,C}\right)D$. (06 Marks)

c. Write the truth table of the logic circuit having 3 input A, B and C and output output expressed as $y = A\overline{B}C + ABC$. Also simplify the expression using Boolean expression and implement the logic circuit using NAND gates? (06 Marks)

2 a. Using Q – M method, simplify the expressions f(A, B, C, D) = Σ(0, 3, 5, 6, 7 11, 14). Write the gate diagram for the simplified expression using NAND – NAND gates. (10 Marks)

b. A digital system is to be designed in which the month of the year is given as input is four bit form. The month January is represented as '0000' February '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0' consider the excess numbers in the input beyond '1011' as don't care conditions for system of four variables (A, B, C, D) find the following :

i) Boolean expression in Σm and πm form
ii) Write the truth table
iii) Using K – map, simplify the Boolean expression of canonical minterm form
iv) Implement the simplified equation using NAND – NAND gates. (10 Marks)

3 a. Write a 4: 1 MUX verilog program using conditional 'assign' and 'case' statement. (06 Marks)

b. What are static hazards? How to design hazards free circuit? Explain with an example. (06 Marks)

c. Explain IV – bit magnitude comparator. (08 Marks)

4 a. Draw the logic diagram of clock D – flip/flop write its truth table and characteristic equation, state diagram and excitation table, what is the draw back JK flip/flop. (10 Marks)

b. Differentiate between combinational circuit and sequential circuits. (05 Marks)

c. Show how a SR flip/flop can be converted into T – flip/flop. (05 Marks)

PART – B

5 a. Using negative edge triggered JK flip/flop, draw the logic diagram of a 4-bit serial-in-serial-out shift register. Draw the waveform to shift the binary number 1010 into this register. Also draw the waveform for 4 clock transistor when J = K = 0. (08 Marks)

b. Explain the working of mod – 4 ring counter. (06 Marks)

c. Explain with a neat diagram, how shift register can be applied for serial addition. (06 Marks)

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6 a. With the help of neat block diagram and timing diagram, explain the working ripple counter constructed using the edge triggered JK- flip/flop.

b. Design asynchronous counter for the sequence $0 \rightarrow 4 \rightarrow 1 \rightarrow 2 \rightarrow 6 \rightarrow 0$ flip-flop.

7 a. Design a sequence detector that receives bindery data stream as its input when a combinations '011' arrives at the input by making its output. Y high remain line consider data is coming from left, i. e the first bit to be identified 1 and third 0 from the input sequence. Design mealy model?

b. Realize the sequential circuit for the state diagram.

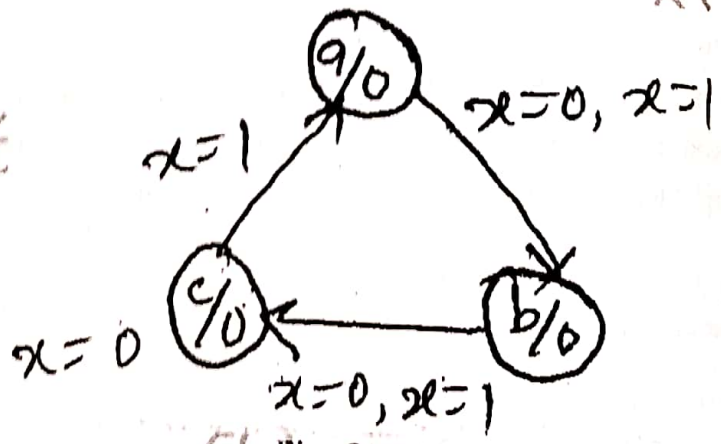

Fig. Q7(b)

8 a. Explain 2-bit simultaneous A/D converter.

b. What is binary ladder? Explain the binary ladder with a digital input of 1000.

c. What is accuracy and resolution of the D/A converter? What is the resolution converter which uses binary ladder? If the full scale output is + 10 V, what is in volts?

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10CS46

Fourth Semester B.E. Degree Examination, Dec.2015/Jan.2016

Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the function of processor registers with a block diagram. **(08 Marks)**

b. Derive the basic performance equation. Discuss the measures to improve the performance. **(08 Marks)**

c. List the different systems used to represent of signed number and give one example for each. **(04 Marks)**

2 a. What is an addressing mode? Explain only four addressing modes with an example for each. **(10 Marks)**

b. Registers R_1 and R_2 of computer, contain the decimal values 1200 and 4600. What is EA of the memory opened in each of the following instructions?

i) Load 20 (R_1), R_5 ii) Move # 3000, R_5

iii) Store R_5, 30(R_1, R_2) iv)Add – (R_2) R_5 v) Subtract (R_1)+, R_5 **(05 Marks)**

c. What is subroutine linkage? Explain with an example subroutine linkage using linkage register. **(05 Marks)**

3 a. What is interrupt? Explain polling and vectored interrupts. **(07 Marks)**

b. What is bus arbitration? Explain the centralized arbitration with a neat diagram. **(07 Marks)**

c. What is DMA? Explain the registers in a DMA interface. **(06 Marks)**

4 a. Explain with block diagram a general 8 bit parallel interface. **(10 Marks)**

b. Describe how a read operation is performed on the PCI bus. **(10 Marks)**

PART – B

5 a. Draw the organization of a 1K × 1 memory cell and explain its working. **(08 Marks)**

b. Show with diagram the memory hierarchy with respect to speed, size and cost. **(05 Marks)**

c. With a block diagram explain about direct mapping cache memory. **(07 Marks)**

6 a. Discuss the Booth's multiplication algorithm, with an example. **(10 Marks)**

b. With figure, explain circuit arrangements for binary division. **(05 Marks)**

c. Illustrate the steps for non – restoring division algorithm on the following data : dividend = 1000, divisor = 11. **(05 Marks)**

7 a. List out the actions needed to execute the instruction add (R_3), R_1. Write and explain sequence of control steps for the execution of the same. **(08 Marks)**

b. Write a control sequence for on unconditional branch instructions. **(04 Marks)**

c. Explain the 3 bus organization of the processor. **(08 Marks)**

8 a. With a neat diagram, explain the organization of a shared memory multiprocessor. **(08 Marks)**

b. What is hardware multithreading? Explain the different approaches to hardware multithreading. **(08 Marks)**

c. Explain single instruction stream, multiple data stream (SIMD). **(04 Marks)**

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