

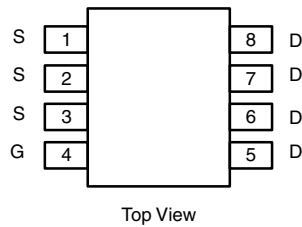


## P-Channel 30 V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ ) Max.	$I_D$ (A) <sup>d</sup>	$Q_g$ (Typ.)
- 30	0.0060 at $V_{GS} = - 10$ V	- 25.7	65 nC
	0.0080 at $V_{GS} = - 4.5$ V	- 22.3	

SO-8


**Ordering Information:**

Si4101DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

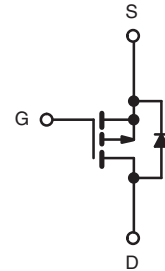
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- 100 %  $R_g$  and UIS Tested
- Material categorization:  
For definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
 FREE

### APPLICATIONS

- Adaptor Switch, Load Switch
- Power Management
- Notebook Computers and Portable Battery Packs



P-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current ( $t = 300$ $\mu$ s)	$I_{DM}$	- 70	A
Continuous Source-Drain Diode Current	$I_S$	- 5	
		- 2.4 <sup>a, b</sup>	
Avalanche Current	$I_{AS}$	- 30	mJ
Single-Pulse Avalanche Energy	$E_{AS}$	45	
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, c</sup>	$R_{thJA}$	36	43	°C/W
Maximum Junction-to-Foot	$R_{thJF}$	16	21	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

 b.  $t = 10$  s.

c. Maximum under steady state conditions is 84 °C/W.

 d. Based on  $T_C = 25$  °C.

## Si4101DY

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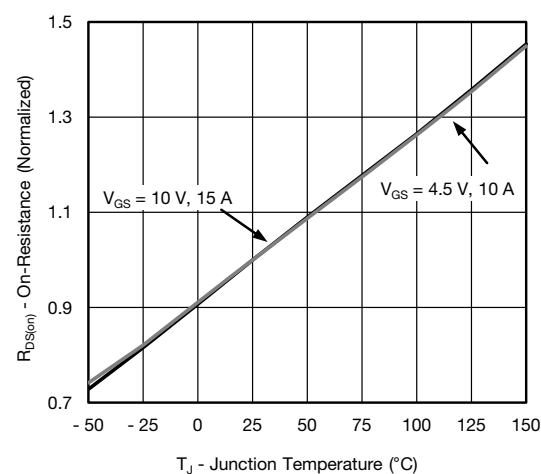
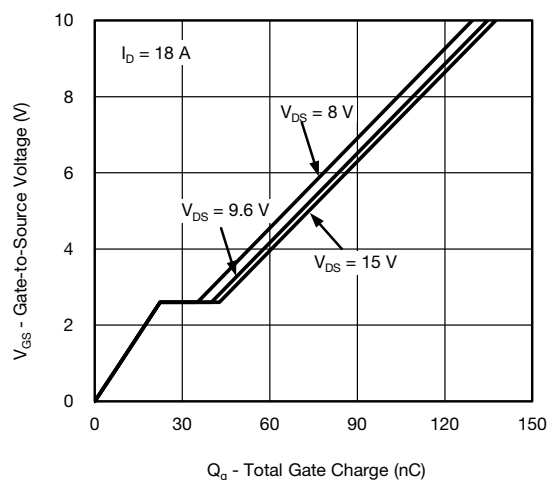
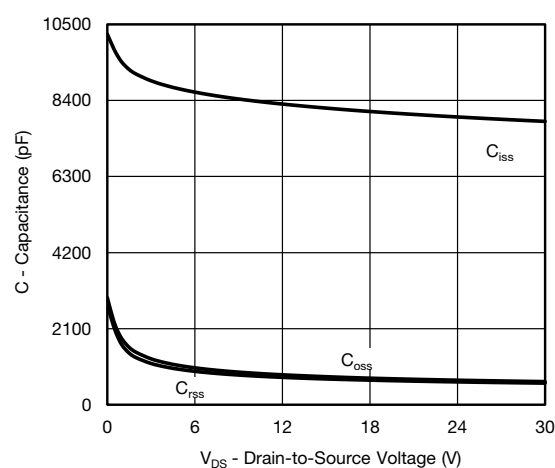
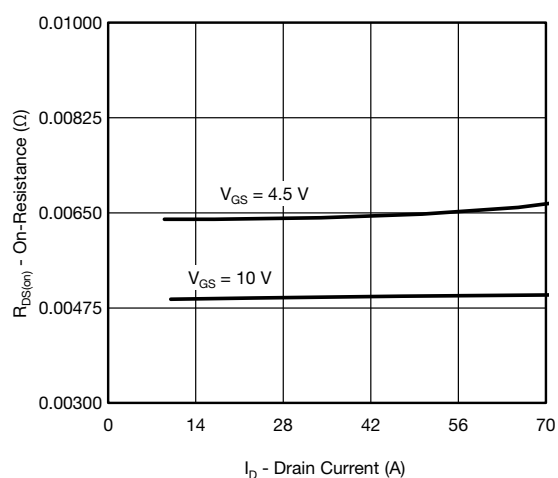
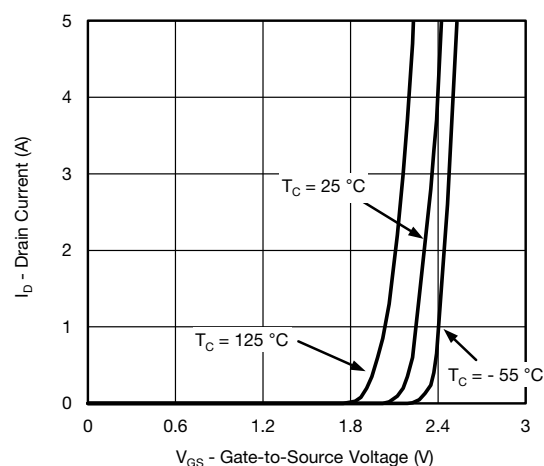
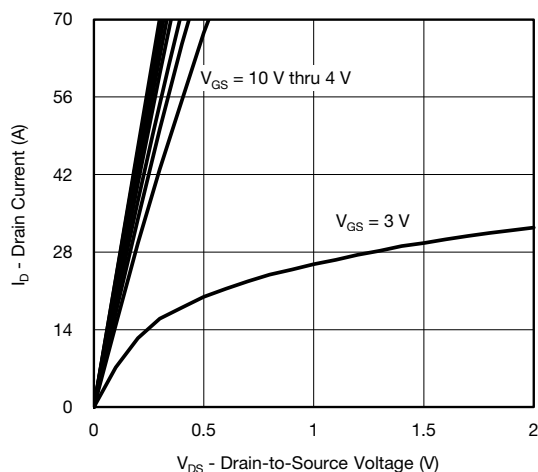


SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 30			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 20		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			5.3		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 1		- 2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			- 5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ - 10 V, V <sub>GS</sub> = - 10 V	- 30			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 15 A		0.0050	0.0060	Ω
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 10 A		0.0066	0.0080	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 15 A		72		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		8190		pF
Output Capacitance	C <sub>oss</sub>			772		
Reverse Transfer Capacitance	C <sub>rss</sub>			715		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 18 A		135	203	nC
		V <sub>DS</sub> = - 15 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 18 A		65	85	
Gate-Source Charge	Q <sub>gs</sub>			22.5		
Gate-Drain Charge	Q <sub>gd</sub>			17.6		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.4	2	4	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 10 V, R <sub>g</sub> = 1 Ω		20	30	ns
Rise Time	t <sub>r</sub>			9	18	
Turn-Off DelayTime	t <sub>d(off)</sub>			80	120	
Fall Time	t <sub>f</sub>			11	20	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 15 V, R <sub>L</sub> = 1.5 Ω I <sub>D</sub> ≅ - 10 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		72	108	
Rise Time	t <sub>r</sub>			60	90	
Turn-Off DelayTime	t <sub>d(off)</sub>			60	90	
Fall Time	t <sub>f</sub>			23	35	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 5	A
Pulse Diode Forward Current	I <sub>SM</sub>				- 70	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 3 A, V <sub>GS</sub> = 0 V		- 0.78	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 10 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		29	45	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			19	29	nC
Reverse Recovery Fall Time	t <sub>a</sub>			13		ns
Reverse Recovery Rise Time	t <sub>b</sub>			16		

Notes:

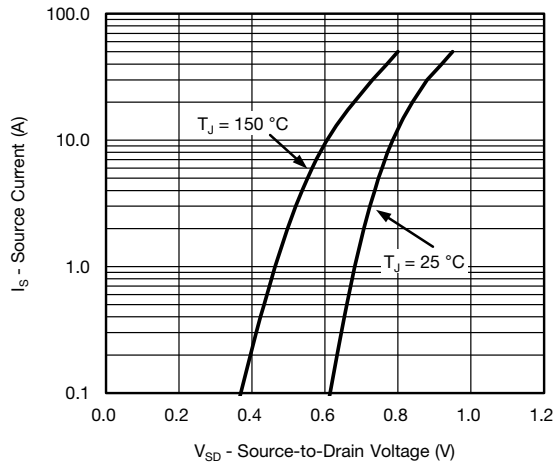
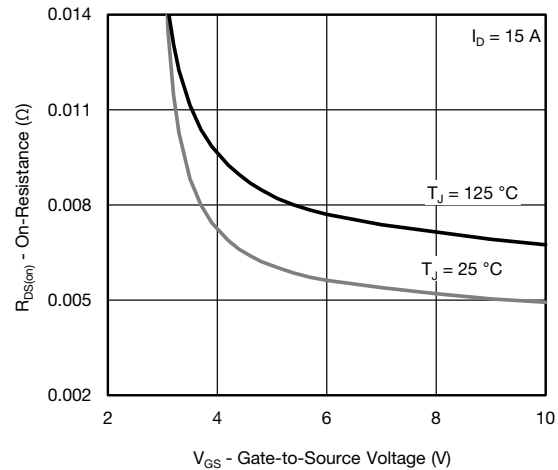
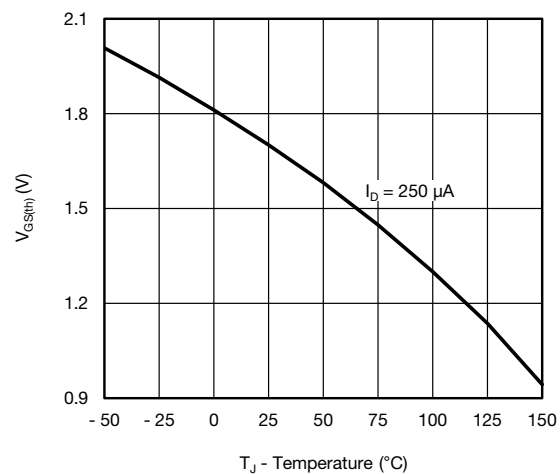
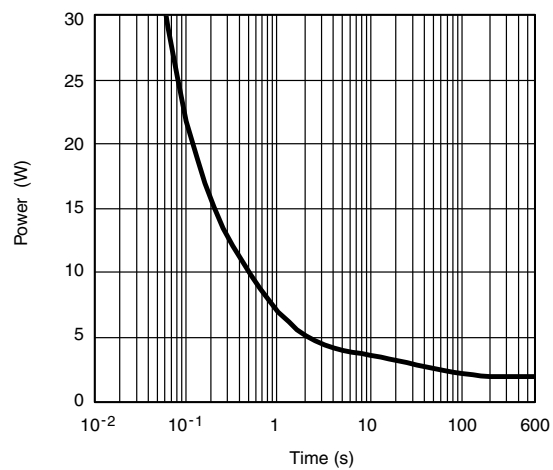
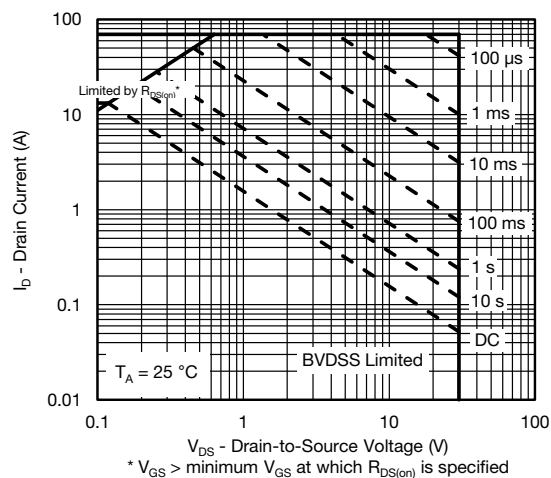
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

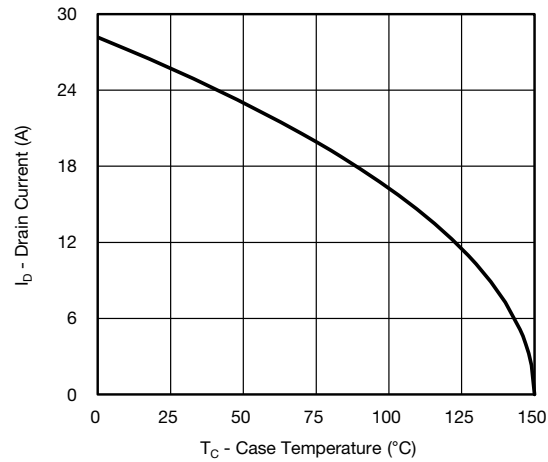
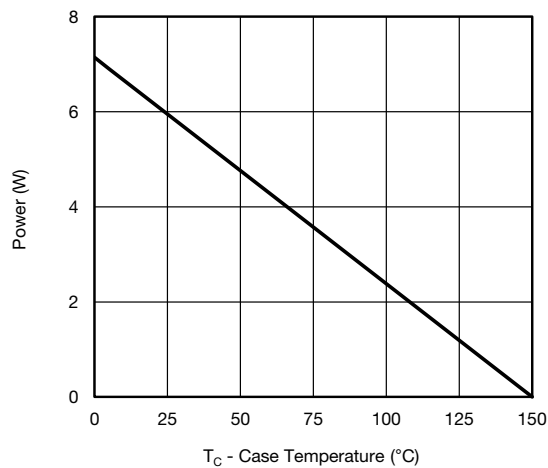
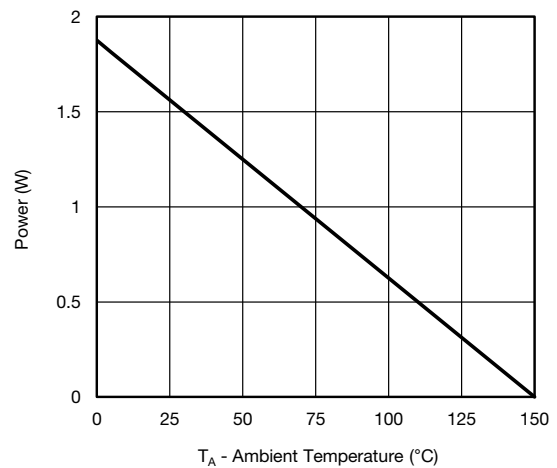
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


**Si4101DY**

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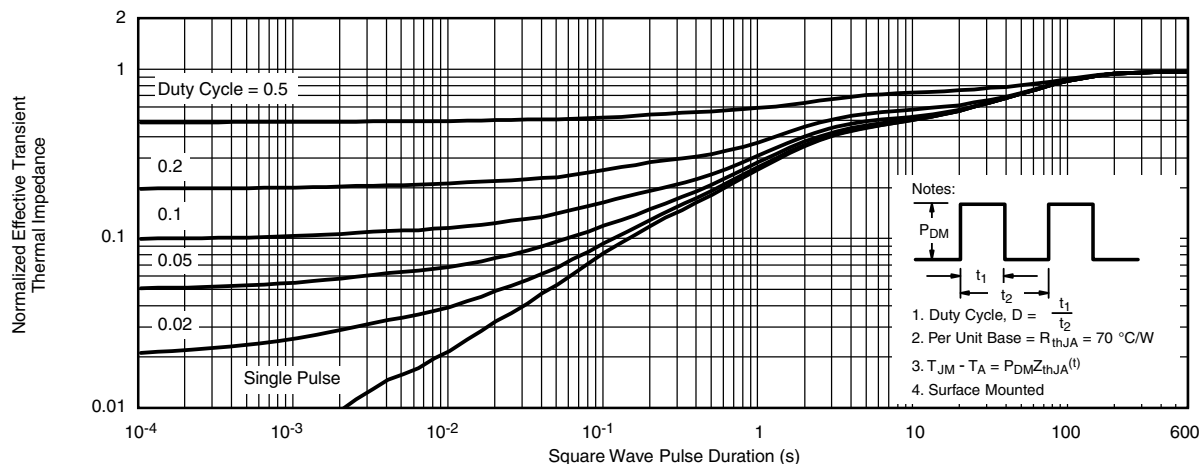
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient****Safe Operating Area**


**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating\***

**Power Derating, Junction-to-Foot**

**Power Derating, Junction-to-Ambient**

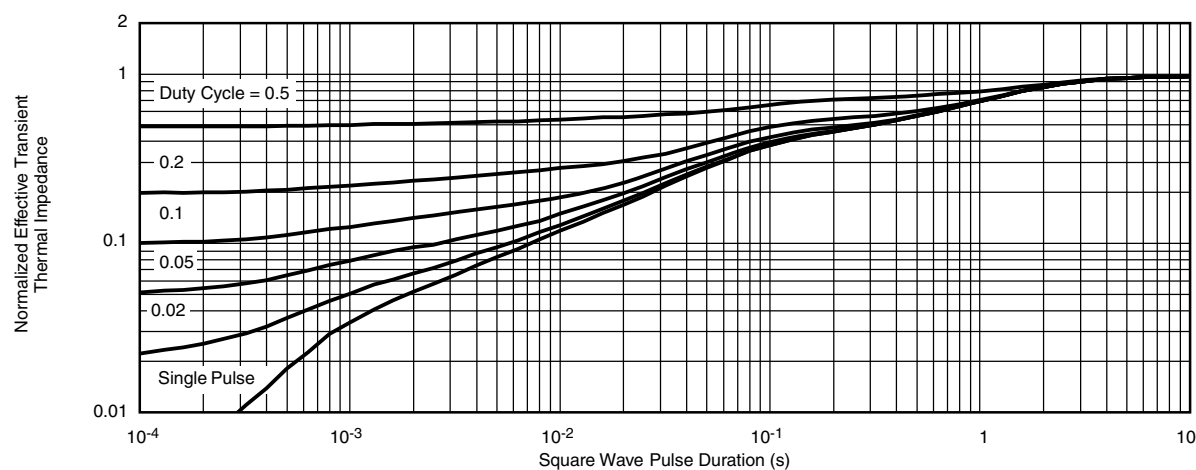
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## Si4101DY

Vishay Siliconix

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62828](http://www.vishay.com/ppg?62828).



## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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