BLG 212E Microprocessor Systems Homework 1

Due: Tuesday, November 1, 2022

Lecturer: Ayşe Yılmazer CRN: 12629

Fatih Baskın
150210710

Contents

Problem 1

In this problem, a 32K8 memory should be designed using:

- Six 2K8 memory chips
- One 4K8 memory chip
- One 16K8 memory chip

There are 16 address bits. Memory addresses should start from **$0000** and continue without spaces.

a) Memory Map

2K8 chips will have 11 bits for address selection inside chips since $2^{11} = 2K$, 12 bits for 4K8 chip ($2^{12} = 4K$) and 14 bits for 16K8 chip ($2^{14} = 16K$). The table for the memory map is on the next page.

$0000 $07FF	2K8#1
$0800 $0FFF	2K8#2
$1000 $17FF	2K8#3
$1800 $1FFF	2K8#4
$2000 $27FF	2K8#5
$2800 $2FFF	2K8#6
$3000 $3FFF	4K8#1
$4000 $7FFF	16K8#1
	Memory adresses after $8000 (inclusive) are not spanned by these memory chips

Figure 1: Memory map of those chips

Problem 1 continued on next page...

Chip Type	Chip Name	Starting Address(bin)	Ending Address(bin)	Address Range(hex)
2K8	2K8#1	0000 0000 0000 0000	0000 0111 1111 1111	$0000 - $07FF
2K8	2K8#2	0000 1000 0000 0000	0000 1111 1111 1111	$0800 - $0FFF
2K8	2K8#3	0001 0000 0000 0000	0001 0111 1111 1111	$1000 - $17FF
2K8	2K8#4	0001 1000 0000 0000	0001 1111 1111 1111	$1800 - $1FFF
2K8	2K8#5	0010 0000 0000 0000	0010 0111 1111 1111	$2000 - $27FF
2K8	2K8#6	0010 1000 0000 0000	0010 1111 1111 1111	$2800 - $2FFF
4K8	4K8#1	0011 0000 0000 0000	0011 1111 1111 1111	$3000 - $3FFF
16K8	16K8#1	0100 0000 0000 0000	0111 1111 1111 1111	$4000 - $7FFF

Table 1: Memory chips and their memory spans, red bits are used for chip selection.

b) Chip Select Functions and Memory Circuit

The bits shown in red should be used in the chip selection process. When 0 signal arrives chip select, that chip is selected ($\overline{CS_x}$), also address bit A_{15} is always 0 in address selection, so for the chip selection, address bits $A_{14} - A_{11}$ can be used in the decoder, then the decoder output can be logical **AND**ed with $\bar{A_{15}}$ since A_{15} was always 0 in chip selection. For the chip select, the output should be 0, so complementing the **AND** operation, effectively **NAND**ing should give 0 in the correct input combinations. Since **NAND**ing is effectively complementing **OR** gate's inputs, we can complement decoder outputs take A_{15} directly, zero signal would be provided in the correct input combinations. Decoder inputs are 4 bits, $A_{14} - A_{11}$ and outputs are $O_{15} - O_0$ (4 to 16 decoder).

- $\overline{CS_{2K8\#1}} = \overline{\bar{A_{15}} \cdot O_0} = A_{15} + \bar{O_0}$
- $\overline{CS_{2K8\#2}} = \overline{\bar{A_{15}} \cdot O_1} = A_{15} + \bar{O_1}$
- $\overline{CS_{2K8\#3}} = \overline{\bar{A_{15}} \cdot O_2} = A_{15} + \bar{O_2}$
- $\overline{CS_{2K8\#4}} = \overline{\bar{A_{15}} \cdot O_3} = A_{15} + \bar{O_3}$
- $\overline{CS_{2K8\#5}} = \overline{\bar{A_{15}} \cdot O_4} = A_{15} + \bar{O_4}$
- $\overline{CS_{2K8\#6}} = \overline{\bar{A_{15}} \cdot O_5} = A_{15} + \bar{O_5}$
- $\overline{CS_{4K8\#1}} = \overline{\bar{A_{15}} \cdot (O_6 + O_7)} = A_{15} + (\bar{O_6} \cdot \bar{O_7})$
- $\overline{CS_{16K8\#1}} = \overline{\bar{A_{15}} \cdot OR(O_{15} - O_8)}$
  $= A_{15} + (\bar{O_8} \cdot \bar{O_9} \cdot \bar{O_{10}} \cdot \bar{O_{11}} \cdot \bar{O_{12}} \cdot \bar{O_{13}} \cdot \bar{O_{14}} \cdot \bar{O_{15}})$

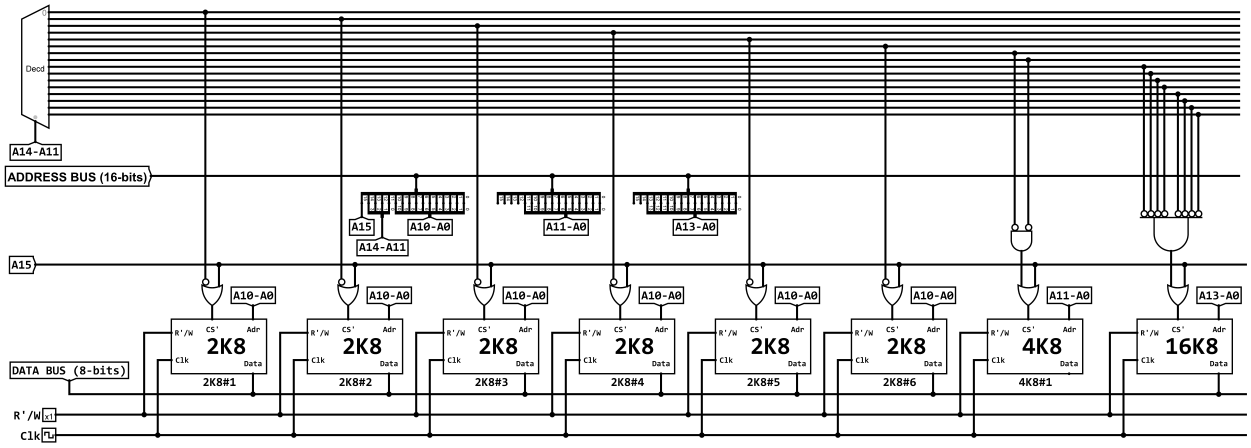

Figure 2: Memory circuit (*Zoom in to see better, high resolution picture*)

Problem 2

In this problem, using 4K4 $\bar{R}/W$ chips, 16K8 memory should be implemented. Memory space should start from **$8000**, there are 16 address bits and 8 data bits.

a) Memory Address Range

Since chips are 4-bits wide, there should be 2 chips per same address range, those chips will be called "L" and "H", meaning the lowest significant half-byte and highest significant half-byte respectively. Since these chips are all 4Ks, $2^{12} = 4K$ so 12 bits will be spared for address selection inside the chip, and the remaining 4 bits will be used for chip selection. This means using 4 to 16 decoder. Since each address range requires 2 chips and there are 4 address ranges ($16K/4K = 4$) there will be 8 chips in total.

Chip Type	Chip Name	Starting Address(bin)	Ending Address(bin)	Address Range(hex)
4K4	4K4#1H & 4K4#1L	1000 0000 0000 0000	1000 1111 1111 1111	$8000 - $87FF
4K4	4K4#2H & 4K4#2L	1001 0000 0000 0000	1001 1111 1111 1111	$9000 - $97FF
4K4	4K4#3H & 4K4#3L	1010 0000 0000 0000	1010 1111 1111 1111	$A000 - $A7FF
4K4	4K4#4H & 4K4#4L	1011 0000 0000 0000	1011 1111 1111 1111	$B000 - $B7FF

Table 2: Memory chips and their memory spans, red bits are used for chip selection.

b) Memory Circuit

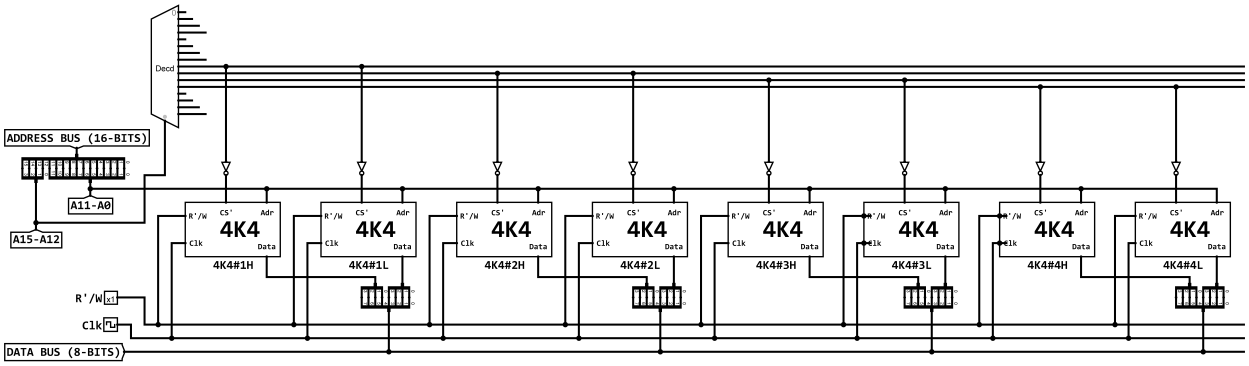

Figure 3: Memory circuit (*Zoom in to see better, high resolution picture*)