Faculty of Computer and Informatics Engineering

BLG 212E
Microprocessor Systems
Due date: 01.11.2022

Homework #1

1. Design a **32Kx8** memory map using the following memory units in the given order.

   - Six 2Kx8
   - One 4Kx8
   - One 16Kx8

   The data bus is **8 bits**, and the address bus is **16 bits**.

   a) Draw the memory map. Make sure to indicate the starting and ending addresses for each unit. Start with the address **$0000** and **leave no spaces** between blocks.
   b) Write the simplified address decoder output functions (CSx) for each memory component in terms of the decoder inputs. Draw the memory design by showing all necessary connections. (Note that the chip selection inputs are active high/zero (0). For example, memory unit M1 is selected when CS1 is 0, and all other CSx are 1.)

2. We have **4Kx4 R/W** memory chips. Using these chips, design a **16Kx8** memory that starts from the memory address **$8000** and **leave no spaces** between blocks. The data bus is **8 bits**, and the address bus is **16 bits**.
   a) Calculate the memory address range for all chips.
   b) Draw the memory design by showing all necessary connections. (Address bus, Data bus, Chip select signals, CPU connections). Use an address decoder (determine its type) and logic gates.

Submission: Prepare a pdf file containing your solutions. Show each step of your solution and make comments where necessary. You should type your name and student ID at the top of the pdf file. You must submit your homework through the Ninova system before the due date.

Late submissions will not be accepted.

Assignments have to be made individually. If any plagiarism issue is detected, the disciplinary regulations of the university will apply.

Note: If you have any questions about the homework, you can contact the following research assistants of the course.

Ayşe Sayın, sayinays@itu.edu.tr

Yağmur Yiğit, yigity20@itu.edu.tr