GURUNATH KADAM

• gurunath.kadam@gmail.com •

OBJECTIVE

Well versed in CPU/GPU architecture and FPGAs. Seeking to address security and reliability challenges in the emerging computing systems.

EDUCATION

The College of William and Mary — Williamsburg, VA, USA
Ph.D. candidate in Computer Science. **Advisor:** Prof. Adwait Jog — Expected May 2021.
Dissertation Title: *"Low Overhead Techniques for Secure and Reliable GPU Computing"*

Technical University of Darmstadt — Darmstadt, Germany
M.Sc. in Information & Communication Engineering. — Nov 2012.
Thesis Title: *''Wireless NoC based on XHiNoC"*

University of Mumbai — Mumbai, India
B.E. in Electrical Engineering. — May 2006.

PUBLICATIONS

Conference Publications:

[HPCA 2020] Gurunath Kadam, Danfeng Zhang, Adwait Jog. *BCoal: Bucketing-based Memory Coalescing for Efficient and Secure GPUs*. In the Proceedings of The 26^{th} International Symposium on High-Performance Computer Architecture, San Diego, USA, February, 2020.

[HPCA 2018] Gurunath Kadam, Danfeng Zhang, Adwait Jog. *RCoal: Mitigating GPU Timing Attack via Subwarp-based Randomized Coalescing Techniques*. In the Proceedings of The 24^{th} International Symposium on High-Performance Computer Architecture, Vienna, Austria, February, 2018.

[ITC 2016] Gurunath Kadam, Markus Rudack, Krishnendu Chakrabarty, Juergen Alt. *Supply-voltage optimization to account for process variations in high-volume manufacturing testing*. In the Proceedings of The 47^{th} IEEE International Test Conference, Forth Worth, USA, 2016.

RESEARCH EXPERIENCE

The College of William and Mary — Williamsburg, VA, USA
Graduate Researcher in Computer Science Department. — Aug 2016 - present.

- Investigating HW-based reliability measures for the Machine Learning Workloads.
- Investigating the memory faults and their impact on the reliable operation of GPUs.
- Implemented HW-based measures against a proven timing channel attack on GPUs.

Intel Labs — Hillsboro, OR, USA
Graduate Research Intern. — Aug 2018 - Dec 2018.

- Investigated the security vulnerabilities in multi-tenancy on FPGAs.
- Built a tool to visualize the FPGA resource utilization of an application bitstream.

Intel Deutschland GmbH — Munich, Germany
Graduate Intern Technical in Design-for-Test. — Mar 2013 - July 2016.

- Implemented an innovative methodology for determining voltage guard-band for product testing.
- Statistical modelled the on-wafer process variations using Design of Experiments (DoE).
- Validated the methodology by testing the silicon chips on ATE and performing scan diagnosis.

TEAMWORK EXPERIENCE

Reliance Ports and Terminals Ltd. Navi Mumbai, India
Design Engineer: Electrical. Jan 2008 - Sept 2010.

- Modelled and Analyzed Electrical System using ETAP for relay setting and co-ordination.
- Prepared of Electrical layouts, MTO Sheets, Load Summaries, PCC and MCC Schedules.

Semikron Electronics Pvt. Ltd. Navi Mumbai, India.
Trainee Design Engineer: Power Electronics. Nov 2006 - Dec 2007.

- Designed power converter stacks.
- Performed converter stack assembly, quality assurance and stack testing.

AWARDS, GRANTS and HONORS

- **Graduate Studies and Research Recruitment Fellowship**, The College of William and Mary, 2016-18.
- **Graudate Assistantship**, The College of William and Mary, 2016-17.
- **Student Travel Grant**, MICRO 2017, HPCA 2018, HPCA 2019, DSN 2019.

SKILLS

Languages: C/C++, SystemC, Python, LaTex, SystemVerilog, Spectre/MDL, HSPICE.
Software: Intel Quartus Prime, Cadence ADE, Synopsys DC, JMP, Matlab, Keil uVision.

PROFESSIONAL MEMBERSHIPS

IEEE: Graduate Student Member (# 94627736).

REFERENCES

Available upon request.