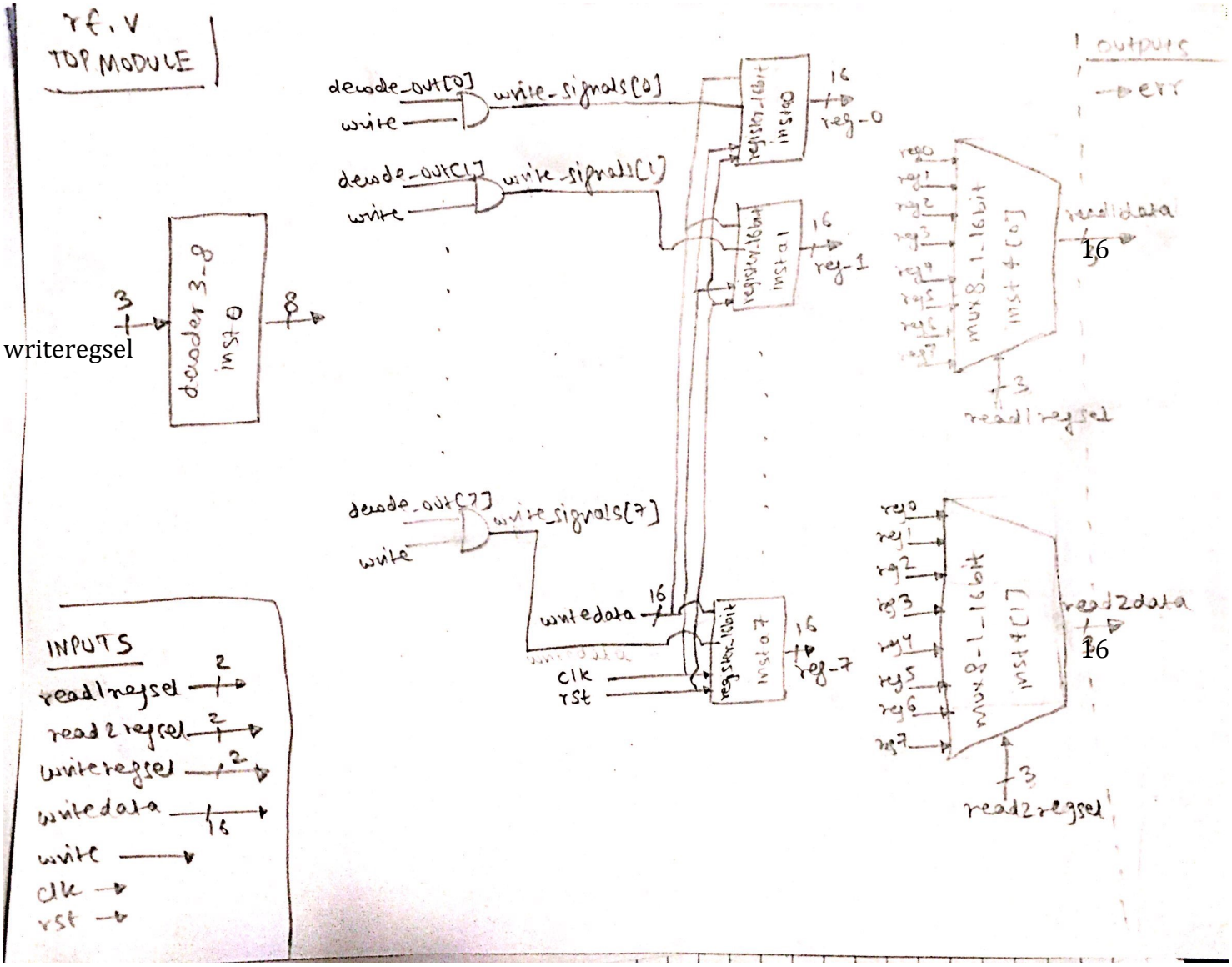
rf.v
TOP MODULE
outputs
err
decoder 3-8
inst 0
writeregsel
3
8
decode_out[0]
write
write_signals[0]
register_16bit
inst 0
16
reg_0
decode_out[1]
write_signals[1]
inst 1
reg_1
decode_out[7]
write_signals[7]
inst 7
reg_7
writedata
clk
rst
mux 8_1_16bit
inst 4 [0]
reg0
reg1
reg2
reg3
reg4
reg5
reg6
reg7
readdata
read1regsel
inst 4 [1]
read2data
read2regsel
INPUTS
read1regsel
read2regsel
writeregsel
writedata
write
clk
rst