Notes: (Unless Otherwise Specified)

1. General Requirement:
   a. Fabricate to meet IPC-2221, IPC-6011, and IPC-6012 (latest revisions) Class 2, except where otherwise specified.

   b. Board shall be electrically tested per current revision of IPC 6012 and IPC 9252 class II. Completed electrical test Boards must be marked in permanent non-conductive ink next to supplier UL recognition mark. Use Net Tie Report (if supplied) for identifying deliberate shorts in netlist.

   c. Configuration of the printed circuit board not specifically dimensioned on the drawing shall be controlled by the gerber data.

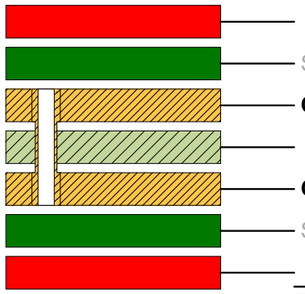
   d. PCB fabrication process and materials must be compliant with the Hazardous Substances(ROHS) Directive and compatible with Pb Free assembly process.
2. Material
   a. Glass epoxy, natural color, laminated Nanya NP 175 or equivalent.
3. Surface Finish:
   a. ALL external metal finish not covered by soldermask shall be plate 118-250 micro-inches of Electroless Nickel and 2 - 8 microinches of Immersion Gold (ENIG)
4. Theiving patter shall not be added to PCB unless explicitly approved.
5. Layer to layer registration shall be within 0.15mm (0.005 in) of gerber data.
6. Drilling
   a. All hole symbols may not be shown in the drawing. See Drill chart for details.

   b. Diameters in the drill table are finished hole sizes with +/-0.003" tolerance unless otherwise specified in the drill table.
7. Marking:
   a. Soldermask,photo-imaged liquid polymer on both sides of boards in accordance with IPC-SM-840, Type B, Class 2, over bare copper. Soldermask color to be BLUE

   b. Component Marking: Silkscreen both sides with non-conductive epoxy ink. Lands and exposed plated areas to be free of ink. Silk color to be WHITE

   c. Identification: Fab vendor logo and part number with current revision to be etched on the top side. Silkscreen date code on solder side near part number. Supplier shall not add any text or marking in the copper.
8. Nets intentionally shorted:
   a. NONE
9. Plating shall be ENIG per IPC-4552 (latest revision).
10. The materials and process used to fabricate this part are to be consistent with the directive 2011/65/EU restriction of hazardous substances in electrical and electronics equipment (ROHS). the findished part to be accompanied by a signed certificate of compliance to the directive 2011/65/EU.
11. If any REACH SVHC'S are ustiized in the materials and or process used to fabricate this part, the weight of the SVHC'S must be provided.
12. Via:
    Tent vias per Gerber files.
13. Board Outline contained in Gerber File (.GM3)

Layer Stack Legend



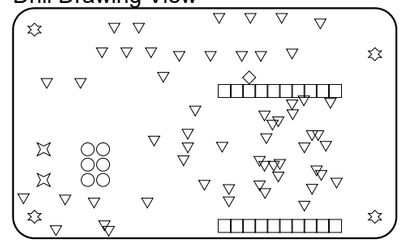
Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
Copper	**Top Layer**	**0.04mm**		**Signal**	**GTL**
		1.51mm	*FR-4*	*Dielectric*	
Copper	**Bottom Layer**	**0.04mm**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.60mm

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
□	20	0.80	Plated	
☆	4	3.10	Plated	
○	6	1.20	Plated	
⛝	2	1.60	Non-Plated	
▽	57	0.50	Plated	
◇	1	0.71	Plated	

Drill Drawing View



Top Layer (Scale: 1:1)