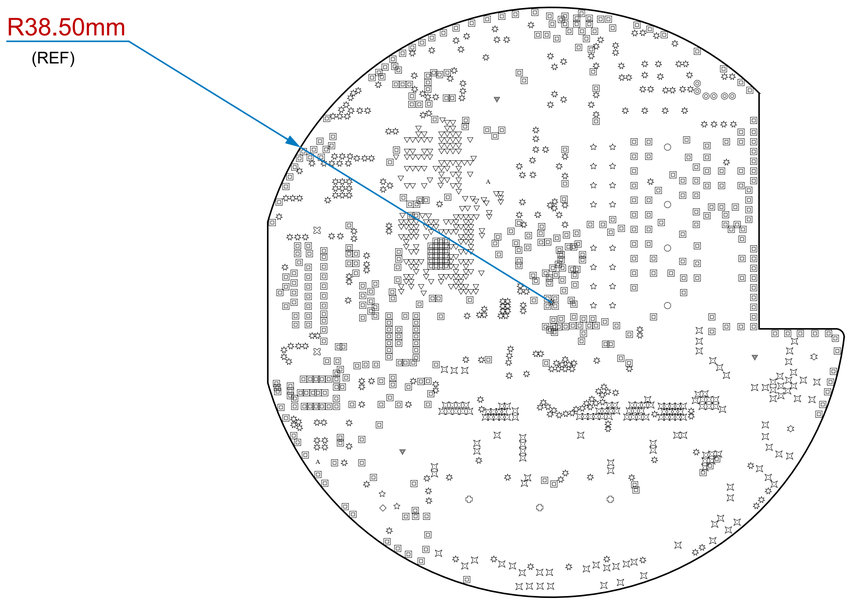
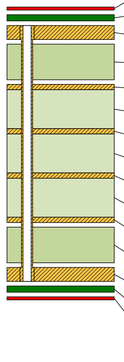


Layer Stack Legend



Layer	Type	Gerber	Copper Weight
Top Overlay	Legend	GTO	
Top Solder	Solder Mask	GTS	
Top Layer	Signal	GTL	1/2 oz + Plating
	Dielectric		
GND	Signal	G1	1/2 oz
	Dielectric		
SL1	Signal	G2	1/2 oz
	Dielectric		
SL2	Signal	G3	1/2 oz
	Dielectric		
PWR	Signal	G4	1/2 oz
	Dielectric		
Bottom Layer	Signal	GBL	1/2 oz + Plating
Bottom Solder	Solder Mask	GBS	
Bottom Overlay	Legend	GBO	

Total thickness: .062" +/-10%

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
▽	199	0.15mm	Plated	+0.00mm/-0.15mm
▨	470	0.20mm	Plated	+0.00mm/-0.20mm
☼	272	0.25mm	Plated	+0.00mm/-0.25mm
◎	6	0.30mm	Plated	+0.00mm/-0.30mm
⌑	159	0.38mm	Plated	+/-0.08mm
▵	2	1.02mm	Plated	+/-0.08mm
⌬	3	1.19mm	Plated	+/-0.08mm
☆	18	1.22mm	Plated	+/-0.08mm
◇	1	1.32mm	Non-Plated	+/-0.05mm
○	4	1.60mm	Non-Plated	+/-0.05mm
⊠	2	1.65mm	Non-Plated	+/-0.05mm
☼	2	1.70mm	Plated	+/-0.08mm
▿	3	3.30mm	Plated	+/-0.08mm
	1141 Total			

Notes: (Unless Otherwise Specified)

1. General Requirement:
   a. Fabricate to meet IPC-2221, IPC-6011, and IPC-6012 (latest revisions) Class 2, except where otherwise specified.

   b. Board shall be electrically tested per current revision of IPC 6012 and IPC 9252 class II. Completed electrical test Boards must be marked in permanent non-conductive ink next to supplier UL recognition mark. Use Net Tie Report (if supplied) for identifying deliberate shorts in netlist.

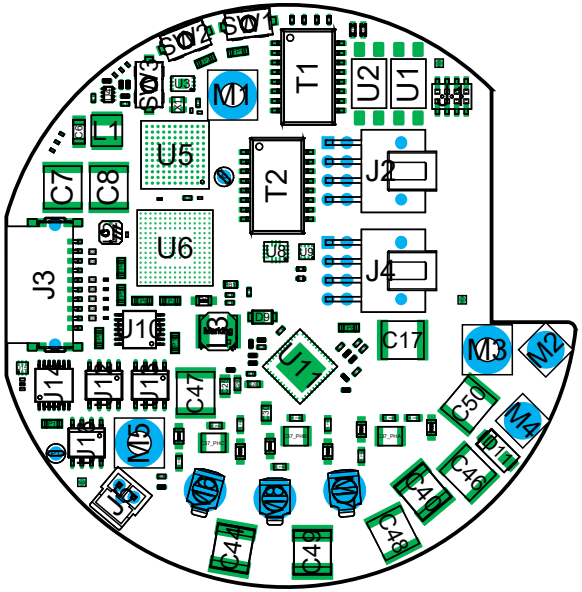
   c. Configuration of the printed circuit board not specifically dimensioned on the drawing shall be controlled by the gerber data.

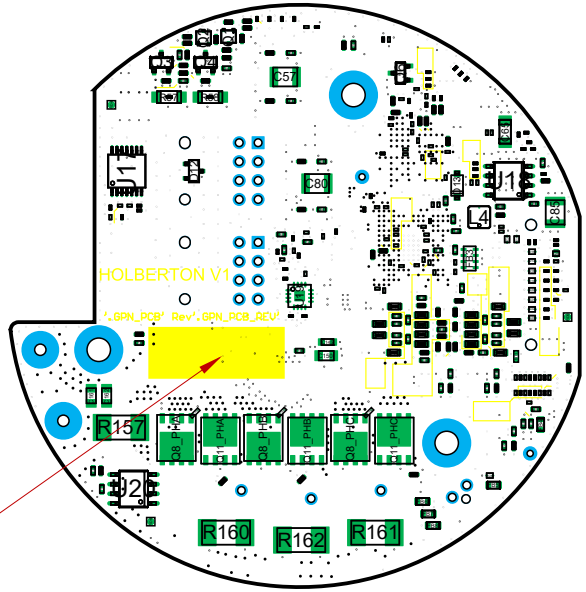
   d. PCB fabrication process and materials must be compliant with the Hazardous Substances(ROHS) Directive and compatible with Pb Free assembly process.
2. Controlled Impedance Nets: 100 Ohm Differential +/- 10% referenced to GND internal plane on the layer directly adjacent. Traces have 6.1mil width and 8 mil gap and are located on the TOP and BOT layers.
   ECAT_R0(P/N)
   ECAT_R1(P/N)
   ECAT_T0(P/N)
   ECAT_T1(P/N)
   ECATPHY0_T(P/N)
   ECATPHY0_R_(P/N)
   ECATPHY1_T(P/N)
   ECATPHY1_R_(P/N)
3. Material
   a. Glass epoxy, natural color, laminated Nanya NP 175 or equivalent.
4. Surface Finish:
   a. ALL external metal finish not covered by soldermask shall be plate 118-250 micro-inches of Electroless Nickel and 2 - 8 microinches of Immersion Gold (ENIG)
5. Theiving patter shall not be added to PCB unless explicitly approved.
6. Layer to layer registration shall be within 0.15mm (0.005 in) of gerber data.
7. Via:
   Tent vias per Gerber files.
8. Drilling
   a. All hole symbols may not be shown in the drawing. See Drill chart for details.

   b. Diameters in the drill table are finished hole sizes with +/-0.003" tolerance unless otherwise specified in the drill table.
9. Marking:
   a. Soldermask,photo-imaged liquid polymer on both sides of boards in accordance with IPC-SM-840, Type B, Class 2, over bare copper. Soldermask color to be BLUE

   b. Component Marking: Silkscreen both sides with non-conductive epoxy ink. Lands and exposed plated areas to be free of ink. Silk color to be WHITE

   c. Identification: Fab vendor logo and part number with current revision to be etched on the top side. Silkscreen date code on solder side near part number. Supplier shall not add any text or marking in the copper.
10. Nets intentionally shorted:
    a. AGND - GND at NT1
    b. SNA - GND at NT3_PHA
    c. SNB - GND at NT3_PHB
    d. SNC - GND at NT3_PHC
11. Plating shall be ENIG per IPC-4552 (latest revision).
12. The materials and process used to fabricate this part are to be consistent with the directive 2011/65/EU restriction of hazardous substances in electrical and electronics equipment (ROHS). the findished part to be accompanied by a signed certificate of compliance to the directive 2011/65/EU.
13. If any REACH SVHC'S are ustiized in the materials and or process used to fabricate this part, the weight of the SVHC'S must be provided.
14. Board Outline contained in Gerber File (.GM3)





ASSEMBLY NOTES:

1. ASSEMBLE PER IPC-A-610, CLASS 2 (LATEST REVISION).
2. ASSEMBLE BOARD WITH LEAD FREE SOLDER.
3. DO NOT WASH ASSEMBLY. COMPONETS MIC1 AND MIC2 ARE MOISTURE SENSITIVE.
4. SERIALIZE AT LOCATION SPECIFIED WITH MEDIUM SIZE LABEL AS DEFINED IN DOCUMENT 991-00897-00. MAX LABEL SIZE IS 1 IN X 3 IN. MANUFACTURER SHALL KEEP TRACEABILITY INFORMATION FOR EVERY ASSEMBLY MANUFACTURED. TRACEABILITY INFORMATION SHALL INCLUDE PART NUMBERS AND REVISIONS; ANY SERIAL NUMBERS, DATE AND LOT CODES; DATE MANUFACTURED; MANUFACTURING LOCATION; AND PRODUCTION, INSPECTION, TEST, AND REWORK HISTORY. TRACEABILITY INFORMATION SHALL BE RETAINED FOR 5 YEARS.
5. PCBA SHALL MAINTAIN OUTLINE DIMENSIONAL TOLERANCE AFTER DEPANELING.
6. PCBA SHALL BE SHIPPED IN ESD SAFE PACKAGING WITH VISIBLE LABELING ON THE ESD PACKAGING AND VISIBLE LABELING ON THE SHIPPING BOX PER DOCUMENT 991-00897-00.
7. THE MATERIALS AND PROCESS USED TO FABRICATE THIS PART ARE TO BE CONSISTENT WITH THE DIRECTIVE 2011/65/EU RESTRICTION OF HAZARDOUS SUBSTANCES IN ELECTRICAL AND ELECTRONIC EQUIPMENT (ROHS). THE FINISHED PART TO BE ACCOMPANIED BY A SIGNED CERTIFICATE OF COMPLIANCE TO DIRECTIVE 2011/65/EU.
8. IF ANY REACH SVHC'S ARE UTILIZED IN THE MATERIALS AND/OR PROCESS USED TO FABRICATE THIS PART, THE WEIGHT OF THE SVHC'S MUST BE PROVIDED.
9. A CONFLICT MINERALS REPORTING TEMPLATE (CMRT) MUST BE AVAILABLE UPON REQUEST AT A PART LEVEL FOR ALL SUPPLIED PARTS.
10. HOMOGENEOUS SUBSTANCE INFORMATION TO ACCOMPANY THE FABRICATED PART PER IPC-1752 (LATEST REV) DATA STANDARDS.