

Space Vector Modulation with DC-Link Voltage Balancing Control for Three-Level Inverters

Kalpesh H. Bhalodi, *Member, IEEE*, and Pramod Agrawal, *Member, IEEE*

Abstract--The DC-link voltage balancing scheme for three-level inverter is proposed in this paper. Dependence of the DC-link capacitor voltage deviation on DC-link current and inverter switching states is established for proposed three-level inverter. Pulse pattern rearrangements for space vector PWM (SVPWM) using degree of freedom available in choice of redundant space vectors, sequencing of vectors, and splitting of duty cycles of vector are best exploited. Self neutral-point voltage deviation control in feed forward and simplified closed loop scheme are proposed in this paper. The effectiveness of proposed scheme is verified by computer simulations.

Index Terms--Diode-clamped inverter, Multilevel inverter, Space-vector modulation, Voltage source inverter.

I. INTRODUCTION

MULTILEVEL inverters have gained much attention for the next generation medium voltage and high power applications. Three-level diode-clamped inverter also known as neutral point clamped (NPC) inverter is most favorable among various multilevel configurations explored in the literature. The three-level NPC inverter is used in this paper. Problems due to neutral-point voltage-unbalance and its various balance control methods are discussed at length [1], [2]. DC-link unbalance may overstress the capacitors and devices during a sudden regenerative load increase, and it can also cause nuisance over voltage or under voltage trips. Active front-end converter with coordinated control from grid end and load end for DC-link balancing control is proposed [1].

The effect of capacitor voltage unbalance during transient and steady state condition are analyzed in this paper. In the worst case of unbalance one capacitor is fully charged to full DC-link voltage that results in double stress on the capacitor

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Kalpesh H. Bhalodi is with Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee - 247667 INDIA (e-mail: kalpeshbhalodi@yahoo.co.in).

Pramod Agrawal is with Department of Electrical Engineering, Indian Institute of Technology Roorkee, Roorkee - 247667 INDIA (e-mail: pramgfee@iitr.ernet.in).

and the switching devices, reducing output waveforms to two-level from normal three-level. The effect of the zero sequence voltage on the neutral point variation and the dependence of DC-link voltage unbalance on the system parameters like load currents, load power factor, value of capacitance of capacitor, and modulation index have been extensively analyzed for three-level NPC inverter [3], [4]. The neutral point balancing schemes, for the three-level neutral point clamped inverter, are based on the effective use of the redundant switching states of the inverter voltage vectors. The redundant switching states are used alternately such that the neutral point voltage unbalance caused by the first switching state combination is compensated by another state; thus, bringing the total unbalance in one switching cycle to zero [5]-[7]. Detailed study of NPC inverter, space vectors, dwell timings, and pulse pattern arrangement with division of middle regions for neutral point balance and even harmonic elimination scheme are addressed [6]. Neutral point voltage control is achieved by utilizing the phase current polarity and distribution of the redundant voltage vectors. A control strategy is proposed to maintain average current drawn from neutral-point to the minimum [8], [9]. Hysteresis control for DC-link variation control and common mode voltage elimination in an open end winding induction motor fed from two three-level inverters from either side is investigated [10]. ANN based neutral-point self-voltage balancing SVPWM is discussed for NPC inverter [11]. Mathematical modeling and neutral-point control with charge balance is proposed for four-level voltage source inverter [12].

II. THREE-LEVEL INVERTER

Fig. 1 shows the simplified circuit diagram of a popular three-level neutral point clamped (NPC) inverter. The inverter leg ‘a’ is composed of four IGBT switches S_1 to S_4 with four antiparallel diodes D_1 to D_4 . On the DC side of the inverter, the DC bus capacitor is split into two, providing a neutral point ‘n’. When switches S_2 and S_3 are turned on, the inverter output terminal ‘a’ is connected to the neutral point through one of the clamping diodes D_{n1} and D_{n2} . Ideally, the voltage across each of the DC capacitors is $V_{dc}/2$, which is half of the total DC-link voltage V_{dc} . With a finite value for C_1 and C_2 , the capacitors can be charged or discharged by neutral current i_2 , causing neutral-point voltage deviation. The important problem of voltage unbalance between upper and lower capacitors in three-level NPC inverter is discussed further.

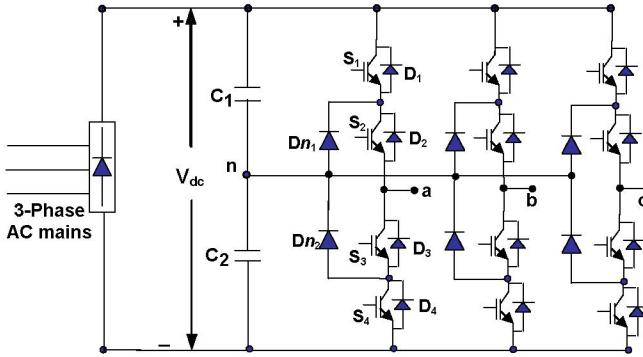


Fig. 1. Three-level neutral-point clamped inverter topology.

As indicated earlier, the neutral-point voltage V_n varies with the operating condition of the NPC inverter. If the neutral-point voltage deviates too far, an uneven voltage distribution takes place, which may lead to premature failure of the switching devices and cause an increase in the harmonic of the inverter output voltage [1].

The operating status of the switches in the NPC inverter can be represented by the switching states shown in Table I. Switching state ‘P’ denotes that the upper two switches in leg ‘a’ are on and the inverter pole voltage V_a , which is ideally $+V_{dc}/2$, whereas ‘N’ indicates that the lower two switches conduct, leading to $V_a = -V_{dc}/2$. Switching state ‘O’ signifies that the inner two switches S_2 and S_3 are on and V_a is clamped to zero through the clamping diodes. Depending on the direction of the load current i_a , one of the two clamping diodes is turned on. For instance, a positive load current ($i_a > 0$) forces D_{n1} to turn on, and the terminal ‘a’ is connected to the neutral point ‘n’ through the conduction of D_{n1} and S_2 . The switches S_1 and S_3 operate in a complementary manner similar to switches S_2 and S_4 .

TABLE I
DEFINITION OF SWITCHING STATES

Switching State	Device Switching Status (Phase a)				V_a
	S_1	S_2	S_3	S_4	
P	On	On	Off	Off	$+V_{dc}/2$
O	Off	On	On	Off	0
N	Off	Off	On	On	$-V_{dc}/2$

As indicated earlier, the operation of each inverter phase lag can be represented by three switching states P, O, and N. Taking all three phases in account, the inverter has a total of 27 possible combinations of switching states. Fig. 2 shows space vector diagram of total 27 switching states corresponding to 19 voltage vectors for three-level NPC inverter. Fig. 3 shows vector placement in a sector A. Based on magnitude, the voltage vectors can be divided into four groups: Zero vector (\underline{u}_o), Small vector (\underline{u}_s), Medium vector (\underline{u}_M), and Large vectors (\underline{u}_L). All zero vectors have zero magnitude, small vectors have a magnitude of $V_{dc}/\sqrt{3}$, medium vectors have magnitude of $V_{dc}/\sqrt{3}$ and large vectors have

magnitude of $2V_{dc}/3$. Each small vector has two switching states, one containing P and other containing N, and therefore can be further classified into a P-type or N-type vector.

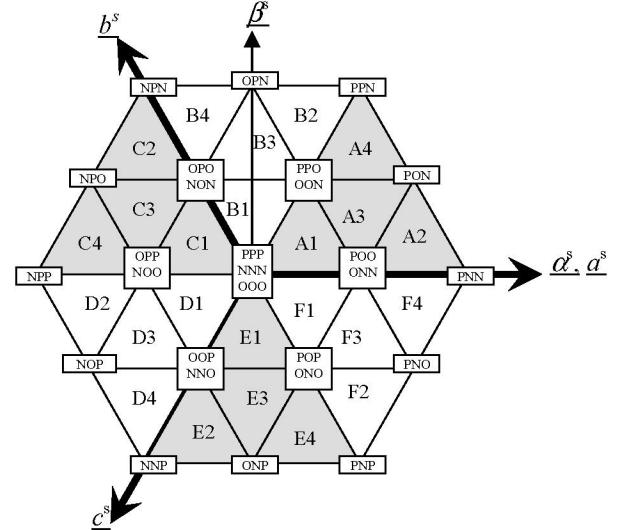


Fig. 2. Space-vector diagram showing switching states.

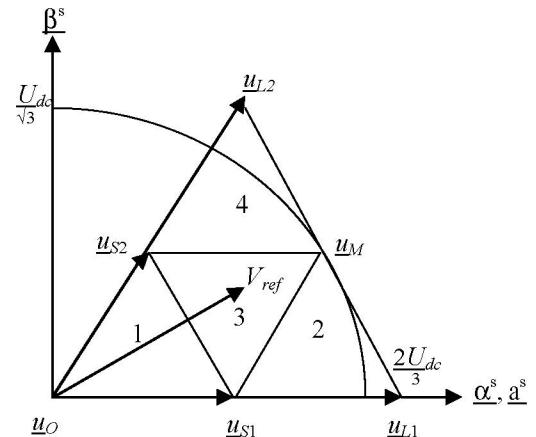


Fig. 3. Vector placement for SVPWM in sector A.

II. EFFECT OF SWITCHING STATES ON NEUTRAL-POINT VOLTAGE DEVIATION

The effect of switching states on neutral voltage deviation is illustrated in fig. 4. When the inverter is operated with switching state [PPP] of zero vector \underline{u}_o , the upper two switches in each of the three inverter legs are turned on, connecting the inverter terminals a, b, and c to the positive DC bus as shown in fig. 4(a). Since the neutral point ‘n’ is left unconnected, this switching state does not affect V_n . Similarly, the other zero switching states [OOO] and [NNN] do not cause V_n to shift either. Fig 4(b) shows the inverter operation with P-type switching state [POO] of small vector \underline{u}_{sp} . Since the three-phase load is connected between the positive DC bus and neutral point ‘n’, the neutral current i_n flows in ‘n’, causing V_n to increase. On the contrary, the N-type switching state [ONN] of small vector \underline{u}_{sn} makes V_n to decrease as shown in fig. 4(c). For medium vector \underline{u}_M with switching state [PON] in fig. 4(d),

load terminals a, b, and c are connected to the positive bus, the neutral point, and the negative bus, respectively. Depending on the inverter operating conditions, the neutral-point voltage V_n may rise or drop. Considering a large vector \underline{u}_L with switching state [PNN] as shown in fig. 4(e), the load terminals are connected between the positive and negative DC buses. The neutral point 'n' is left unconnected and thus the neutral voltage is not affected.

It is summarized that zero and large vectors do not affect the neutral point voltage. Medium vectors affect V_n , but the direction of voltage deviation is undefined so, redundant small vectors having dominant influence on V_n are used for neutral point voltage control. Above discussion is made under the assumption that the inverter is in motoring mode. In addition to the influence of switching states, the neutral-point voltage may also be affected by a number of other factors like unbalanced DC capacitors due to manufacturing tolerances, inconsistency in switching device characteristics, unbalanced three-phase operation, motoring/regenerative mode of operation etc. As compared to motoring mode, an opposite capacitor voltage charging-discharging action takes place in the regenerative mode due to the reversal of current.

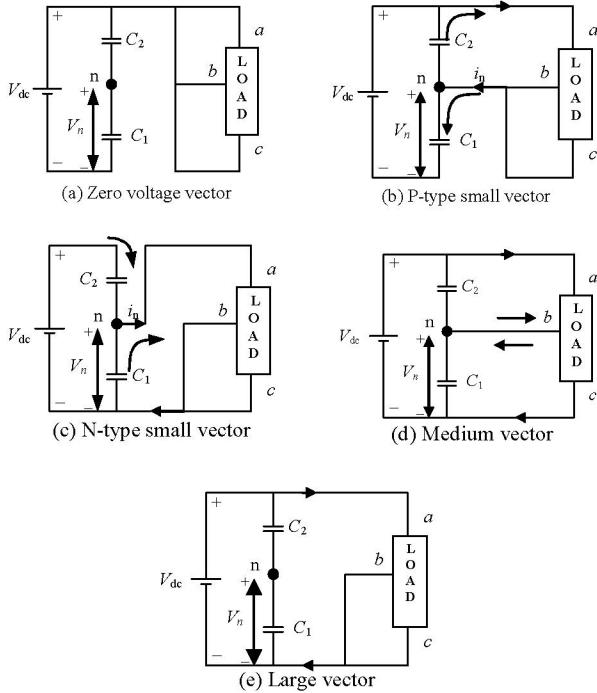


Fig. 4. Effect of switching states on Neutral point voltage deviation.

IV. MATHEMATICAL MODELLING OF THREE-LEVEL INVERTER

The terminology in this paper is explained with reference to fig. 5, in which DC bus structure and each inverter phases is modeled as 3-pole switch. The inverter switching functions S_a , S_b , and S_c assume value equal to 1, 2 or 3, which means that the pole of the switch in connected to bottom, middle or top DC-link respectively. The load currents are denoted as i_a , i_b , and i_c while the currents drawn by the inverter from bottom,

middle and top rails of the DC-link are i_1 , i_2 , and i_3 respectively.

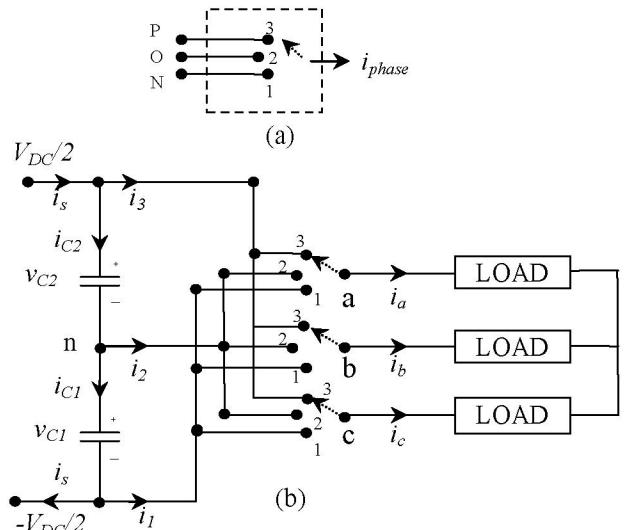


Fig. 5. Three-level inverter and load system model.

In general the inverter pole voltage with respect to the negative DC bus can be written in terms of capacitor voltages and the switching functions as

$$\begin{aligned} v_{a1}(S_a) &= \delta(S_a - 1)v_{C1} + \delta(S_a - 2)(v_{C1} + v_{C2}) \\ v_{b1}(S_b) &= \delta(S_b - 1)v_{C1} + \delta(S_b - 2)(v_{C1} + v_{C2}) \\ v_{c1}(S_c) &= \delta(S_c - 1)v_{C1} + \delta(S_c - 2)(v_{C1} + v_{C2}) \end{aligned} \quad (1)$$

In (1) $\delta(\cdot)$ is the Dirac delta function, v_{C1} and v_{C2} are the voltage across lower and upper capacitors. The currents drawn from the DC-link nodes can be represented in terms of the motor currents as shown in (2)

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} \delta(S_a - 1) & \delta(S_b - 1) & \delta(S_c - 1) \\ \delta(S_a - 2) & \delta(S_b - 2) & \delta(S_c - 2) \\ \delta(S_a - 3) & \delta(S_b - 3) & \delta(S_c - 3) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2)$$

For the three wire load,

$$\begin{aligned} i_a + i_b + i_c &= 0 \\ i_1 + i_2 + i_3 &= 0 \end{aligned} \quad (3)$$

Substituting $i_c = -(i_a + i_b)$ and removing the dependent variable i_3 , (2) gets reduced to

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} [\delta(S_a - 1) - \delta(S_c - 1)] \\ [\delta(S_a - 2) - \delta(S_c - 2)] \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \quad (4)$$

The current flowing through capacitor is given by

$$\begin{aligned} i_{C2} &= i_s - i_3 = i_s - (-i_2 - i_1) = i_s + i_2 + i_1 \\ i_{C1} &= i_s + i_1 \end{aligned} \quad (5)$$

$$\therefore \begin{bmatrix} i_{C2} \\ i_{C1} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_s \\ i_2 \\ i_1 \end{bmatrix} \quad (6)$$

Thus, the currents flowing through capacitors is directly related to the voltage across the capacitors and the relationship is given by

$$\begin{bmatrix} v_{C2} \\ v_{C1} \end{bmatrix} = \frac{1}{C} \int \left\{ \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{C2} \\ i_{C1} \end{bmatrix} dt \right\} = \frac{1}{C} \int \left\{ \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_s \\ i_2 \\ i_1 \end{bmatrix} dt \right\} \quad (7)$$

Let Δv_C be the change in the capacitor voltage. Substituting value from (4) into (6), results in

$$\Delta v_C = v_{C2} - v_{C1}$$

$$\therefore \Delta v_C = \frac{1}{C} \int i_2 dt \quad (8)$$

Thus the load current drawn from the middle node of the DC-link is responsible for the variation in the capacitor voltages. Whenever switching functions S_a , S_b , and S_c assume value equal to 2, there exists a tendency of capacitor voltage unbalancing.

V. DC-LINK CAPACITOR VOLTAGE BALANCING SCHEME

Various space vector modulation (SVM) schemes have been proposed for the three-level NPC inverter using either open loop scheme or closed loop scheme [6].

A. Open loop capacitor voltage self balancing scheme

This section proposes modified SVM scheme for better neutral point stabilization. To reduce neutral-point voltage deviation, the dwell time of a given small vector can be equally distributed between the P-type and N-type switching states over a sampling period. For nearest three vectors (NTV) selection SVM either one small vector or two small vectors among the three selected vectors are available according to the triangular regions in which the reference vector V_{ref} lies. When the reference vector V_{ref} is in region 2 or 4, only one small vector is in NTV where as in region 1 or 3 two small vectors are in NTV as shown in fig. 3. In conventional SVM seven segment pulse pattern is chosen for all regions. Its pulse pattern arrangement for region A1 is shown in fig. 6. Seven segment SVM divides dwell time of only one small vector in P-type and N-type out of two small sectors available in region 1 and 3. So, neutral point deviation is not minimized in these regions. To reduce neutral-point voltage deviation according to location of region, optimized pulse pattern arrangement is proposed here. Negative sequences of modified SVM pulse pattern arrangement for regions A1, A2, A3, and A4 of sector A are shown in fig 7. Here, two small vectors are used for neutral point voltage control for regions 1 and 3. As shown in fig. 8 negative sequence (NEG_SEQ) pulse patterns are arranged in exact reverse order of positive sequence (POS_SEQ) pulse pattern and vice versa. Positive sequence and negative sequence are switched alternatively. Switching sequence in opposite sectors (A-D, B-E and C-F) is selected to be of a complimentary nature for neutral point balancing.

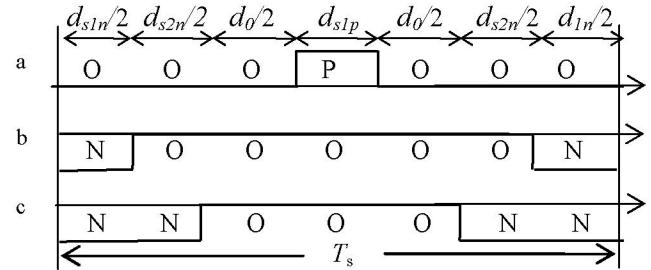


Fig. 6. Pulse pattern arrangement for conventional seven-segment SVPWM in region A1.

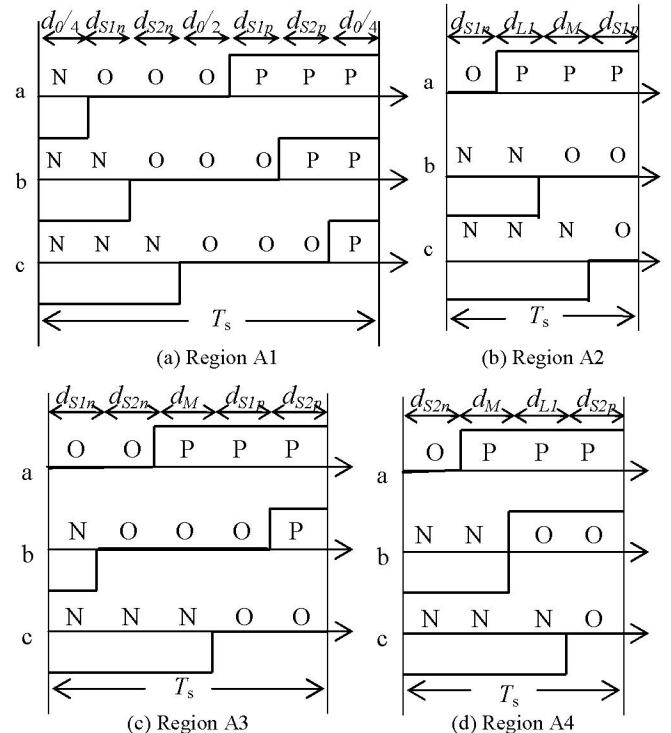


Fig. 7. Pulse pattern arrangement of modified SVPWM in sector A.

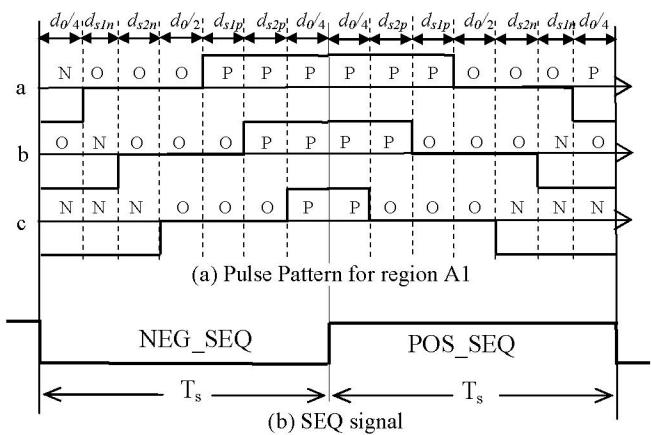


Fig. 8. The sequence of various switching combinations.

Number of switching per phase in sampling period T_s for modified SVM are one in region 2 or 4, two in region 1 and one or two in region 3. In conventional SVM as shown in fig.

6 two switching per phase are required in sampling period T_s . Here, T_s is sum of dwell times of NTV in a sequence.

B. Linear closed loop capacitor voltage balancing scheme

There always exists a small-voltage vector in each switching sequence, whose dwell time is divided into subperiods, one for its P-type and the other for its N-type switching state. For instance, the dwell time d_{S1} for \underline{u}_{S1P} and d_{S1n} for \underline{u}_{S1n} , which is half/half split normally, can be distributed as

$$d_{S1} = d_{S1P} + d_{S1n}$$

where d_{S1P} and d_{S1n} are given by

$$d_{S1P} = d_{S1} / 2(1+\Delta t) \text{ and}$$

$$d_{S1n} = d_{S1} / 2(1-\Delta t) \text{ where } -1 \leq \Delta t \leq 1 \quad (9)$$

The deviation of the neutral point voltage can be further reduced by adjusting the incremental time interval Δt in (9) according to the detected DC capacitor voltages v_{C1} and v_{C2} . The input to the voltage balancing scheme is the difference in capacitor voltages Δv_C where, $\Delta v_C = v_{C2} - v_{C1}$. For instance, if Δv_C is greater than the maximum allowed DC voltage deviation ΔV_m for some reasons, we can increase d_{S1P} and decrease d_{S1n} by Δt ($\Delta t > 0$) simultaneously for the drive in a motoring mode. A reverse action ($\Delta t < 0$) should be taken when the drive is in a regenerative mode. The relationship between the capacitor voltages and the incremental time interval Δt is summarized in Table II.

TABLE II
RELATIONSHIP BETWEEN CAPACITOR VOLTAGES AND
INCREMENTAL TIME INTERVAL Δt

Neutral-point deviation level	Motoring mode	Regenerating node
$(v_{C2} - v_{C1}) > \Delta V_m$	$\Delta t > 0$	$\Delta t < 0$
$(v_{C2} - v_{C1}) < \Delta V_m$	$\Delta t < 0$	$\Delta t > 0$
$ v_{C2} - v_{C1} < \Delta V_m$	$\Delta t = 0$	$\Delta t = 0$
ΔV_m - maximum allowed DC voltage deviation ($\Delta V_C > 0$)		

VI. RESULTS AND DISCUSSIONS

Here, DC-link voltage value of 200 V and inductive load with power factor value of 0.9 is used in all schemes. Fig. 9 shows the variation in the DC-link capacitor voltages, phase voltage, and phase current when open loop DC-link balancing control is on with modulation index value of 0.8. Fig. 10 shows the variation in the DC-link capacitor voltages, phase voltage, and phase current when open loop DC-link balancing control is off with modulation index value of 0.8. As soon as DC-link voltages become unbalanced, the quality of output phase voltage, and current waveform deteriorates. The variation in the DC-link capacitor voltages, phase voltage, and phase current when open loop and closed loop DC-link balancing control is on are shown in fig. 11 with modulation index value of 0.55. The average value of DC-link capacitor

voltages settles towards half the DC-link voltage, hence output voltage and current waveform quality is increased even after slight unsymmetrical pulse pattern due to slight unequal dwell time of P-type and N-type small vectors. Control of proposed scheme is more effective in region 1 and 3, where two small vectors are utilized for pulse pattern arrangement. Linear close loop control accelerates the neutral-point voltage control and improves average DC-link capacitor voltages.

The robustness and effectiveness of the both open loop and close loop control is illustrated in fig. 12 with modulation index value 0.8. In fig. 12, from time $t = 6.76$ to 13.21 (rad) feed forward and feed back controls are off, in rest of the time controls are made on. As soon as the controls are made effective the deviation in capacitor voltages sharply reduces. Thus, the proposed balancing scheme is capable of fundamentally redistributing charges amongst the DC capacitors.

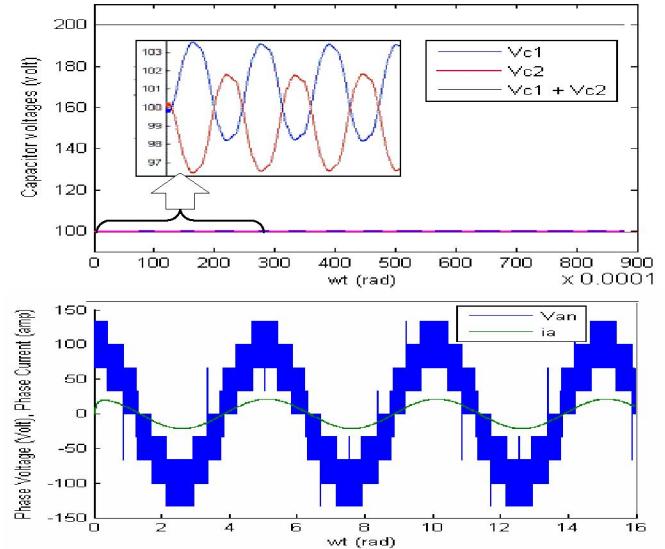


Fig. 9. The variation in the capacitor voltages, phase voltage, and phase current when open loop DC-link balancing control is on.

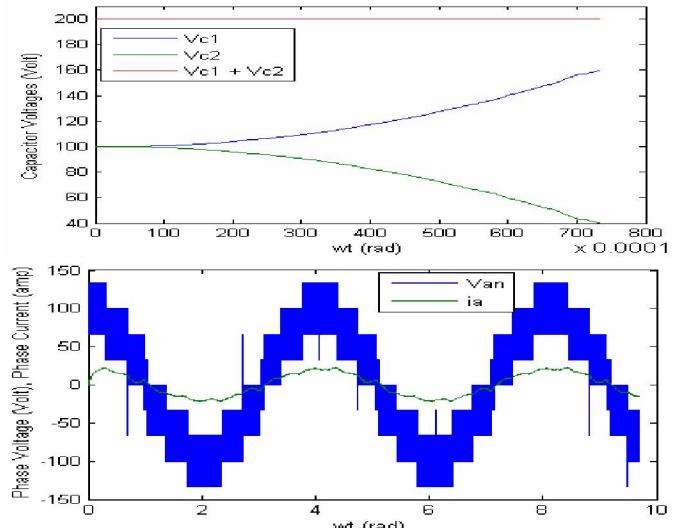


Fig. 10. The variation in the capacitor voltages, phase voltage, and phase current when open loop DC-link balancing control is off.

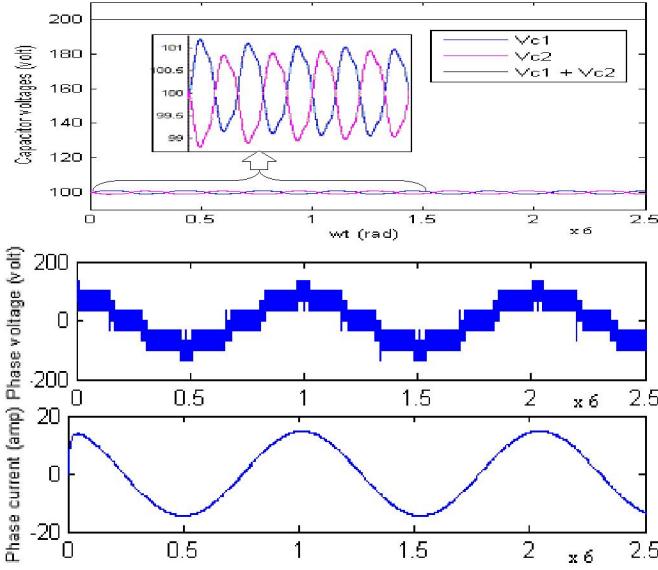


Fig. 11. The variation in the capacitor voltages, phase voltage, and phase current when open loop and closed loop DC-link balancing control is on.

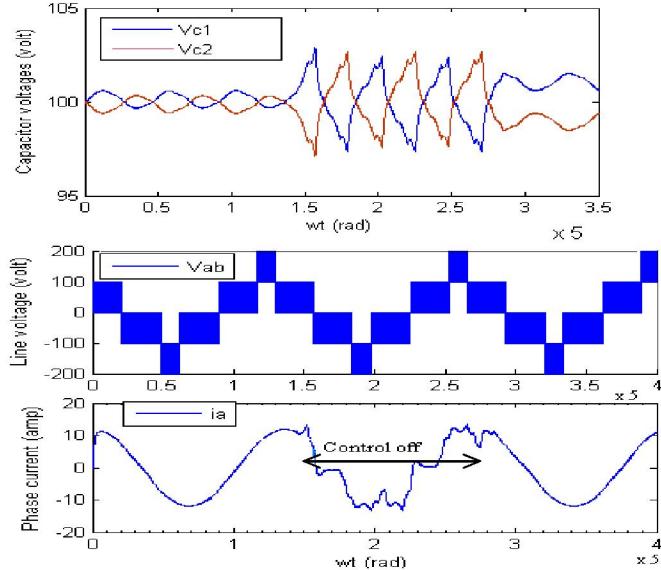


Fig. 12. The variation in the capacitor voltages, line voltage, and phase current when open loop and close loop DC-link balancing control is on or off

VII. CONCLUSION

The DC-link voltage balancing scheme for three-level diode clamping inverter is investigated in this paper. The detailed analysis investigates the DC-link voltage control behavior of proposed scheme and popular SVPWM scheme. The closed loop scheme is used with simple control technique. Redundant space vectors, its sequencing, and splitting of its duty cycle are used for control. Thus, single front-end rectifier can be used with reduced rating DC-link capacitors. Large unbalance in the load can be addressed further.

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IX. BIOGRAPHIES

Kalpesh H. Bhalodi received his Bachelor's and Master's degree in Electrical Engineering Department from L. D. College of Engineering, Ahmedabad, India. He is presently pursuing his Ph.D. in Electrical Engineering Department from Indian Institute of Technology Roorkee, India. He is a faculty member in the department of Electrical Engineering, S. P. College of Engineering, Visnagar, India. His fields of interest include Power Electronics, Electric Drives, Multilevel Inverters, and Microcomputer based Control.

Pramod Agarwal obtained his Bachelor's degree in Electrical Engineering from University of Roorkee now, Indian Institute of Technology Roorkee, India. He received his PG and completed his Ph.D in Electrical Engineering from the same institute in 1985 and 1995 respectively. He is currently Professor in the department of Electrical Engineering, Indian Institute of Technology Roorkee, India. His special fields of interest include Electrical Machines, Power Electronics, Electric Drives, Power quality, Microcomputer Controlled Electric Drives, and Multilevel Converters.