NUM	DATE	DESIGNER	SCH REVISION	PCB REVISION	CAUSE	DESCRIPTION
01	2020-7-13	YangKangquan	V1.0.0	V1.0.0	初次设计	
02	2020-12-8	YangKangquan	V1.0.1	V1.0.1	芯片数据手册更变	1、删除LDOU33_OUT电源 2、增加模拟地pin 3、删除GPIO32 4、PIN66/67改为NC 5、增加U4和U5电路
03	2021-5-7	YangKangquan	V1.0.2	V1.0.1	功率电感描述有误	修改L1/L2/L3的描述
04	2021-6-22	YangKangquan	V1.0.3	V1.0.1	1、优化成本 2、增加注释	1、删减部分电容 2、增加相关注意点

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Page Name	Size	Rev
CHAANGEHISTORY.SchDoc	A4	V1.0.3

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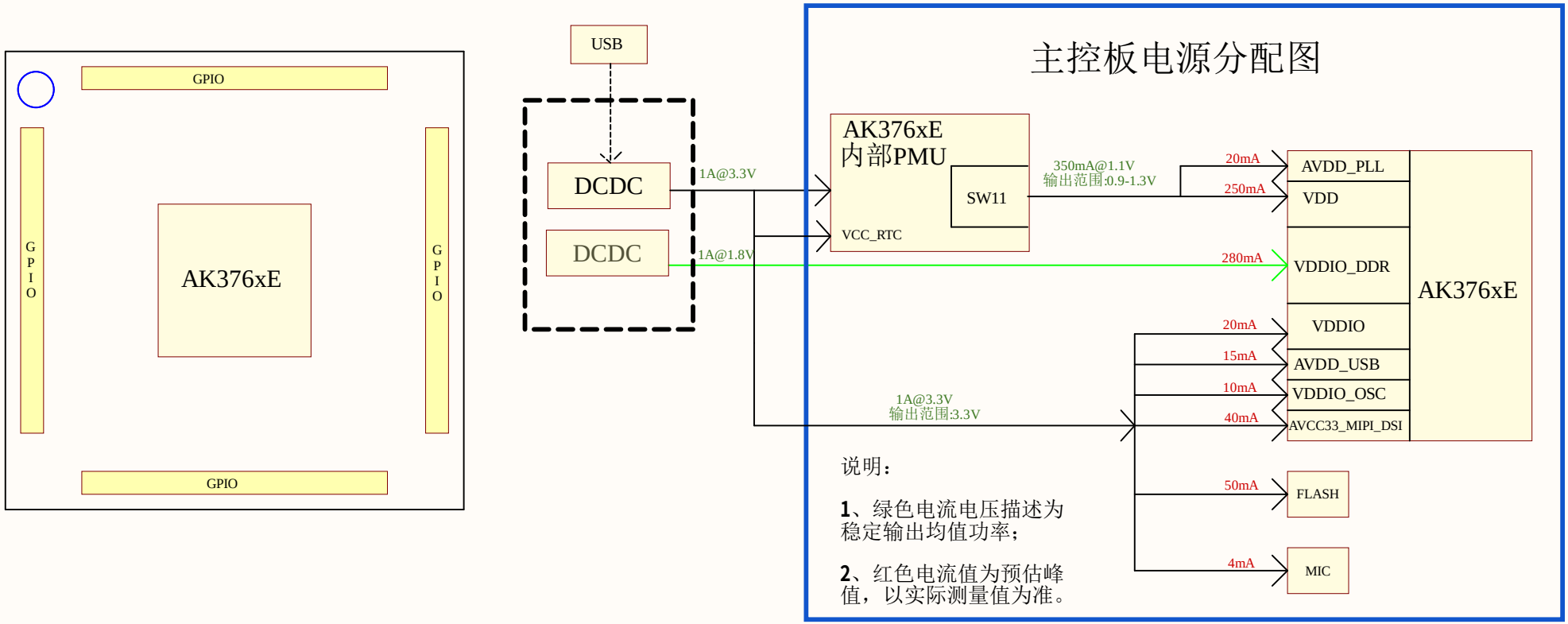

说明：虚线框表示开发板底板

实线" ____ "表示PCB连线，虚线"-------"表示其它连线方式（如排针，线缆，FPC等）。

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BLOCK_DIAGRAM.SchDoc	A4	V1.0.3	
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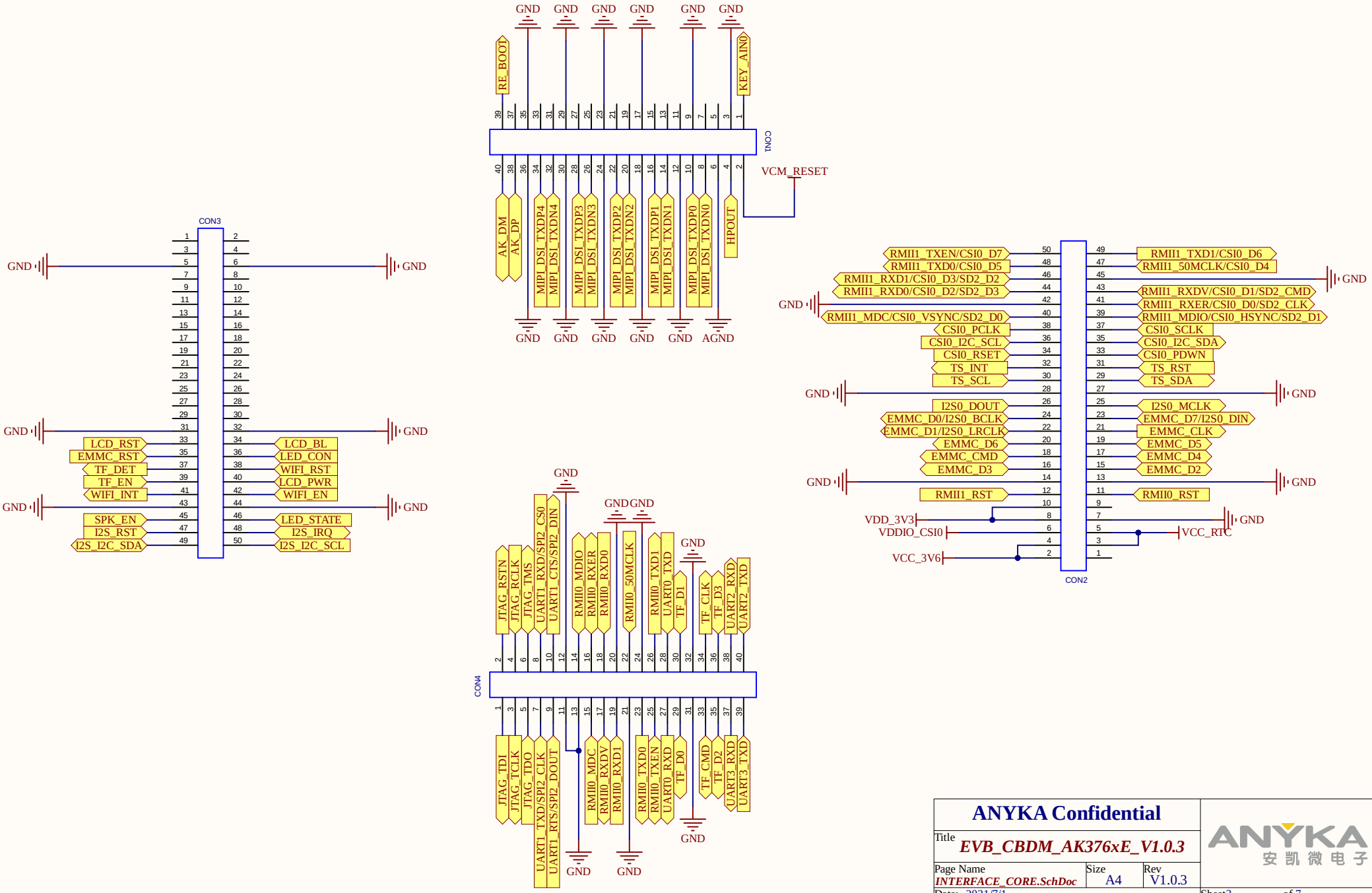

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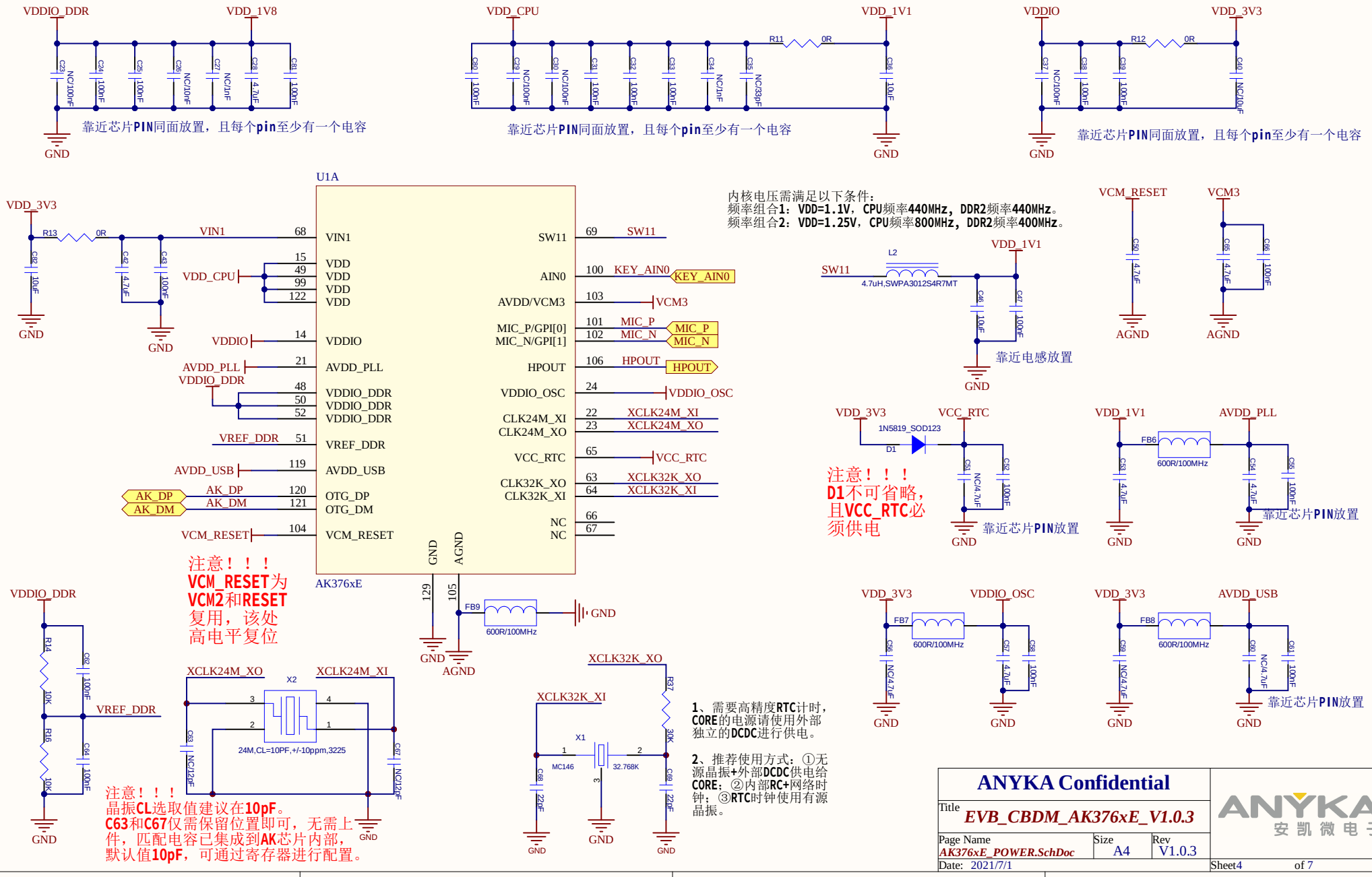
VDDIO_DDR
VDD_1V8
C22 NC/100nF
C24 100nF
C25 100nF
C26 NC/10nF
C27 NC/1nF
C28 4.7uF
C81 100nF
GND
靠近芯片PIN同面放置，且每个pin至少有一个电容
VDD_CPU
VDD_1V1
R11 0R
C80 100nF
C29 NC/100nF
C30 NC/100nF
C31 100nF
C32 100nF
C33 100nF
C34 NC/1nF
C35 NC/33pF
C36 10uF
GND
靠近芯片PIN同面放置，且每个pin至少有一个电容
VDDIO
VDD_3V3
R12 0R
C37 NC/100nF
C38 100nF
C39 100nF
C40 NC/10uF
GND
靠近芯片PIN同面放置，且每个pin至少有一个电容
U1A
VDD_3V3
R13 0R
C82 10uF
C42 4.7uF
C43 100nF
GND
VIN1
VDD_CPU
VDDIO
AVDD_PLL
VDDIO_DDR
VREF_DDR
AVDD_USB
AK_DP
AK_DM
VCM_RESET
VIN1 68
VDD 15
VDD 49
VDD 99
VDD 122
VDDIO 14
AVDD_PLL 21
VDDIO_DDR 48
VDDIO_DDR 50
VDDIO_DDR 52
VREF_DDR 51
AVDD_USB 119
OTG_DP 120
OTG_DM 121
VCM_RESET 104
AK376xE
SW11 69
AIN0 100
KEY_AIN0
AVDD/VCM3 103
VCM3
MIC_P/GPI[0] 101
MIC_N/GPI[1] 102
MIC_P
MIC_N
HPOUT 106
VDDIO_OSC 24
CLK24M_XI 22
CLK24M_XO 23
VCC_RTC 65
CLK32K_XO 63
CLK32K_XI 64
NC 66
NC 67
XCLK24M_XI
XCLK24M_XO
XCLK32K_XI
XCLK32K_XO
GND
AGND
129
105
FB9
600R/100MHz
内核电压需满足以下条件：
频率组合1：VDD=1.1V，CPU频率440MHz，DDR2频率440MHz。
频率组合2：VDD=1.25V，CPU频率800MHz，DDR2频率400MHz。
SW11
L2
4.7uH,SWPA3012S4R7MT
VDD_1V1
C46 10uF
C47 100nF
靠近电感放置
GND
VCM_RESET
VCM3
C50 4.7uF
C66 4.7uF
C66 100nF
AGND
AGND
VDD_3V3
VCC_RTC
1N5819_SOD123
D1
C51 NC/4.7uF
C52 100nF
注意！！！
D1不可省略，
且VCC_RTC必
须供电
靠近芯片PIN放置
GND
VDD_1V1
AVDD_PLL
FB6
600R/100MHz
C53 4.7uF
C54 4.7uF
C55 100nF
靠近芯片PIN放置
GND
GND
注意！！！
VCM_RESET为
VCM2和RESET
复用，该处
高电平复位
VDDIO_DDR
R14 10K
R16 10K
C62 100nF
C64 100nF
VREF_DDR
GND
XCLK24M_XO
XCLK24M_XI
X2
24M,CL=10PF,+/-10ppm,3225
C65 NC/22pF
C67 NC/22pF
GND
注意！！！
晶振CL选取值建议在10pF。
C63和C67仅需保留位置即可，无需上
件，匹配电容已集成到AK芯片内部，
默认值10pF，可通过寄存器进行配置。
XCLK32K_XO
XCLK32K_XI
R37 30K
X1
MC146
32.768K
C68 22pF
C69 22pF
GND
GND
GND
1、需要高精度RTC计时，
CORE的电源请使用外部
独立的DCDC进行供电。
2、推荐使用方式：①无
源晶振+外部DCDC供电给
CORE；②内部RC+网络时
钟；③RTC时钟使用有源
晶振。
VDD_3V3
VDDIO_OSC
FB7
600R/100MHz
C56 NC/4.7uF
C57 4.7uF
C58 100nF
GND
GND
VDD_3V3
AVDD_USB
FB8
600R/100MHz
C59 NC/4.7uF
C60 NC/4.7uF
C61 100nF
靠近芯片PIN放置
GND
GND
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注意！！！
相关注意事项请查看硬件设计指南**Ethernet**接口

U1B

AK376xE

VDDIO_OSC

GPIO0_PU/RMII0_MDIO/SD2_D1/I2S0_DIN/I2C0_SCL
GPIO1_PD/RMII0_MDC/SD2_D0/I2S0_LRCLK/I2C0_SDA
GPIO2_PD/RMII0_RXER/SD2_CLK/I2S0_BCLK/PWM5
GPIO3_PD/RMII0_RXDV/SD2_CMD/I2S0_MCLK/PWM4
GPIO4_PD/RMII0_RXD0/SD2_D3/I2S0_DOUT
GPIO5_PD/RMII0_RXD1/SD2_D2/PWM3
GPIO6_PU/OPCLK0/I2C3_SCL/PWM2/I2S1_LRCLK
GPIO7_PD/RMII0_TXD0/I2C3_SDA/PWM1/I2S1_BCLK
GPIO8_PD/RMII0_TXD1/UART3_RXD/PDM_CLK/I2S1_MCLK
GPIO9_PD/RMII0_TXEN/UART3_TXD/PDM_DATA/I2S1_DIN

GPIO23_PU/UART0_TXD/PWM5
GPIO22_PU/UART0_RXD/PWM4

GPIO32_PU/I2C1_SCL
GPIO68_PU/CSI1_SCLK/SD0_D2/SPI2_CS0
GPIO69_PU/CSI1_PCLK/SD0_D3/SPI2_HOLD
GPIO70_PU/CSI1_HSYNC/SD0_D4/SPI2_DIN/UART1_RXD
GPIO71_PU/CSI1_VSYNC/SD0_CMD/SPI2_SCLK/UART1_TXD
GPIO72_PU/CSI1_D0/SD0_D5/SPI2_WP/UART1_CTS
GPIO73_PU/CSI1_D1/SD0_CLK/SPI2_DOUT/UART1_RTS
GPIO74_PU/CSI1_D2/SD0_D6/RGB_D23/SPI2_CS1
GPIO75_PU/CSI1_D3/SD0_D7/RGB_D22/I2S0_DIN
GPIO76_PU/CSI1_D4/SD0_D1/RGB_D21/I2S0_LRCLK
GPIO77_PU/CSI1_D5/SD0_D0/RGB_D20/I2S0_BCLK
GPIO78_PU/CSI1_D6/I2C2_SCL/RGB_D19/I2S0_MCLK
GPIO79_PU/CSI1_D7/I2C2_SDA/RGB_D18/I2S0_DOUT

VDDIO

GPIO84_PU/I2C2_SDA/SPI2_SCLK/UART2_TXD/I2S1_BCLK
GPIO85_PU/I2C3_SCL/SPI2_DIN/UART3_RXD/I2S1_MCLK
GPIO86_PU/I2C3_SDA/SPI2_DOUT/UART3_TXD/I2S1_DIN

VDDIO

GPIO82_PU/PWM0/SPI0_CS1/SPI1_CS1
GPIO14_PU/SPI0_WP
GPIO15_PU/SPI0_DOUT
GPIO12_PU/SPI0_DIN
GPIO10_PU/SPI0_CS0
GPIO13_PU/SPI0_SCLK
GPIO11_PU/SPI0_HOLD

VDDIO_CSI0

GPIO31_PU/I2C0_SDA
GPIO30_PU/I2C0_SCL
GPIO56_PU/CSI0_SCLK/UART3_RXD
GPIO57_PU/CSI0_PCLK/UART3_TXD
GPIO58_PU/CSI0_HSYNC/RMII1_MDIO/SD2_D1
GPIO59_PU/CSI0_VSYNC/RMII1_MDC/SD2_D0
GPIO60_PU/CSI0_D0/RMII1_RXER/SD2_CLK
GPIO61_PU/CSI0_D1/RMII1_RXDV/SD2_CMD
GPIO62_PU/CSI0_D2/RMII1_RXD0/SD2_D3
GPIO63_PU/CSI0_D3/RMII1_RXD1/SD2_D2
GPIO64_PU/CSI0_D4/OPCLK1/I2C2_SCL/I2S1_LRCLK
GPIO65_PU/CSI0_D5/RMII1_TXD0/I2C2_SDA/I2S1_BCLK
GPIO66_PU/CSI0_D6/RMII1_TXD1/PDM_CLK/I2S1_MCLK
GPIO67_PU/CSI0_D7/RMII1_TXEN/PDM_DATA/I2S1_DIN

GPIO16_PU/SPI1_CS0/SD1_D1/I2C1_SCL/PWM1
GPIO17_PU/SPI1_DIN/SD1_D0/I2C1_SDA/PWM4
GPIO18_PD/SPI1_SCLK/SD1_CLK
GPIO19_PU/SPI1_DOUT/SD1_CMD
GPIO20_PU/SPI1_WP/SD1_D3/UART2_RXD/PWM3
GPIO21_PU/SPI1_HOLD/SD1_D2/UART2_TXD/PWM2
GPIO83_PU/I2C2_SCL/SPI2_CS0/UART2_RXD/I2S1_LRCLK

RMII0_MDIO 36
RMII0_MDC 37
RMII0_RXER 38
RMII0_RXDV 39
RMII0_RXD0 40
RMII0_RXD1 41
RMII0_50MCLK R9 33R 42
RMII0_TXD0 43
RMII0_TXD1 44
RMII0_TXEN 45

UART0_TXD 46
UART0_RXD 47

GPIO32 71
EMMC_D2 72
EMMC_D3 73
EMMC_D4 74
EMMC_CMD 75
EMMC_D5 76
EMMC_CLK 77
EMMC_D6 78
EMMC_D7/I2S0_DIN 79
EMMC_D1/I2S0_LRCLK 80
EMMC_D0/I2S0_BCLK 81
I2S0_MCLK 82
I2S0_DOUT 83

VDDIO 70

GPIO84 60
GPIO85 61
GPIO86 62

1 SPI0_CS1
123 SPI0_WP
124 SPI0_DOUT
125 SPI0_DIN
126 SPI0_CS0
127 SPI0_SCLK
128 SPI0_HOLD

98 VDDIO_CSI0

84 CSI0_I2C_SDA
85 CSI0_I2C_SCL
86 CSI0_SCLK
87 CSI0_PCLK
88 RMII1_MDIO/CSI0_HSYNC/SD2_D1
89 RMII1_MDC/CSI0_VSYNC/SD2_D0
90 RMII1_RXER/CSI0_D0/SD2_CLK
91 RMII1_RXDV/CSI0_D1/SD2_CMD
92 RMII1_RXD0/CSI0_D2/SD2_D3
93 RMII1_RXD1/CSI0_D3/SD2_D2
94 RMII1_50MCLK/CSI0_D4 R15 33R
95 RMII1_TXD0/CSI0_D5
96 RMII1_TXD1/CSI0_D6
97 RMII1_TXEN/CSI0_D7

53 TF_D1
54 TF_D0
55 TF_CLK
56 TF_CMD
57 TF_D3
58 TF_D2
59 GPIO83

注意！！！
默认启动为**SPI0_CS0**

VDDIO_CSI0
C72 100nF
GND

CSI0_I2C_SDA
CSI0_I2C_SCL
CSI0_SCLK
CSI0_PCLK
RMII1_MDIO/CSI0_HSYNC/SD2_D1
RMII1_MDC/CSI0_VSYNC/SD2_D0
RMII1_RXER/CSI0_D0/SD2_CLK
RMII1_RXDV/CSI0_D1/SD2_CMD
RMII1_RXD0/CSI0_D2/SD2_D3
RMII1_RXD1/CSI0_D3/SD2_D2
RMII1_50MCLK/CSI0_D4
RMII1_TXD0/CSI0_D5
RMII1_TXD1/CSI0_D6
RMII1_TXEN/CSI0_D7

TF_D1
TF_D0
TF_CLK
TF_CMD
TF_D3
TF_D2

TF_CLK R17 NC/1K TF_DET → TF_DET
GPIO32 R18 0R

GPIO83 R33 0R UART2_RXD → UART2_RXD
R34 NC/0R CSI0_RSET → CSI0_RSET

GPIO84 R35 0R UART2_TXD → UART2_TXD
R36 NC/0R CSI0_PDWN → CSI0_PDWN

GPIO85 R21 0R RMII0_RST → RMII0_RST
R22 NC/0R UART3_RXD → UART3_RXD

GPIO86 R23 0R RMII1_RST → RMII1_RST
R24 NC/0R UART3_TXD → UART3_TXD

SPI_FLASH_3V3
VDD_3V3
FB1 600R/100MHz
R1 4.7K
R2 4.7K
R3 4.7K
C1 100nF
C2 4.7uF
GND

U2
SPI0_CS1 R29 NC/0R
SPI0_CS0 R30 0R
SPI0_DIN
SPI0_WP
SPI0_HOLD
SPI0_SCLK
SPI0_DOUT
CE# VDD SO HOLD# WP# SCK VSS SI
GD25Q64ESIG
R4 100R RE_BOOT

SPI_FLASH_3V3
R19 4.7K
SPI0_CS0 R31 NC/0R
SPI0_CS1 R32 0R
U3
#CE VDD SO #HOLD #WP CLK VSS SI
GD5F1GQ5UEYIG
C70 100nF
GND

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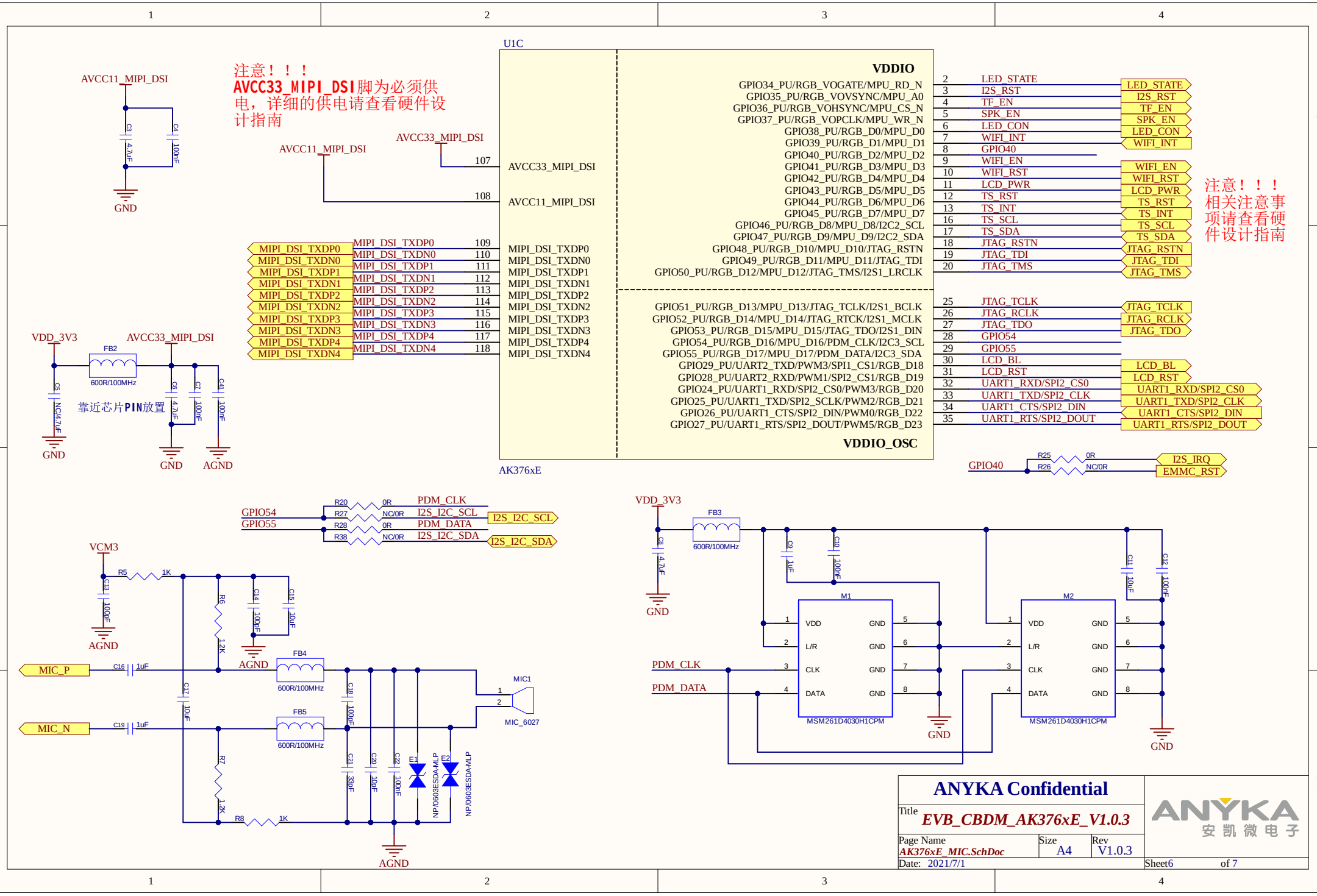
注意！！！
AVCC33_MIPI_DSI脚为必须供电，详细的供电请查看硬件设计指南
AVCC11_MIPI_DSI
AVCC33_MIPI_DSI
U1C
AK376xE
VDDIO
VDDIO_OSC
注意！！！
相关注意事项请查看硬件设计指南
靠近芯片PIN放置
VDD_3V3
GND
AGND
VCM3
MIC_P
MIC_N
MIC1
MIC_6027
PDM_CLK
PDM_DATA
GPIO40
GPIO54
GPIO55
I2S_I2C_SCL
I2S_I2C_SDA
M1
M2
MSM261D4030H1CPM
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V1.0.3
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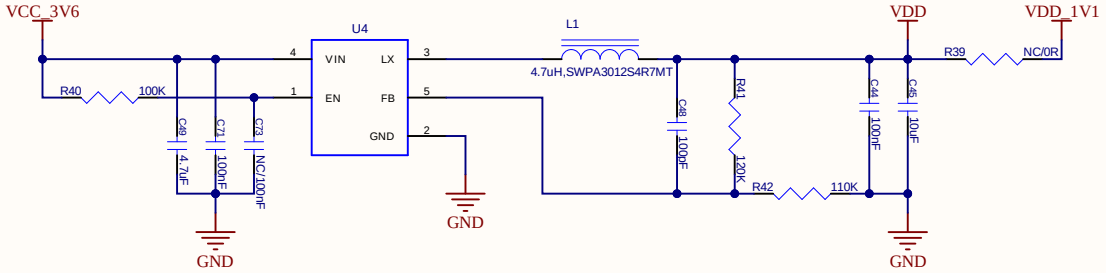
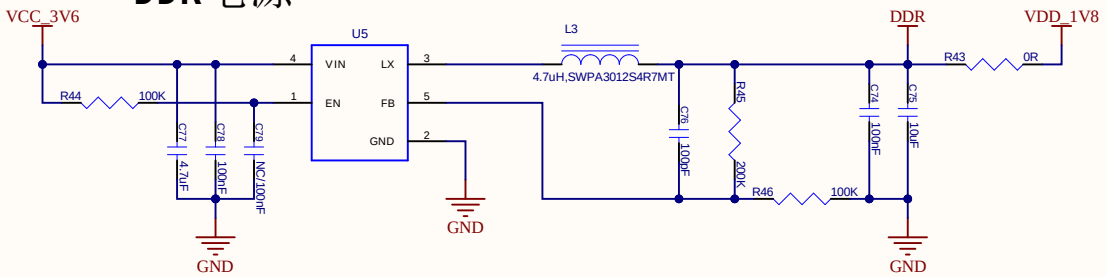
CORE电源

使用外部独立DCDC供电给CORE时，将PMU中SW11输出的电感（L2）去掉即可。



DDR电源



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