

1	2	3	4
A			A
B			B
C			C
D			D

NUM	DATE	DESIGNER	SCH REVISION	PCB REVISION	CAUSE	DESCRIPTION
01	2021-1-19	YangKangquan	V1.0.0	V1.0.0	初次设计	

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Title

EVB_CAD_GC0308_V1.0.0

Page Name

*CHAA**NGEHISTORY.SchDoc*

Date:

2021/1/20

Size

A4

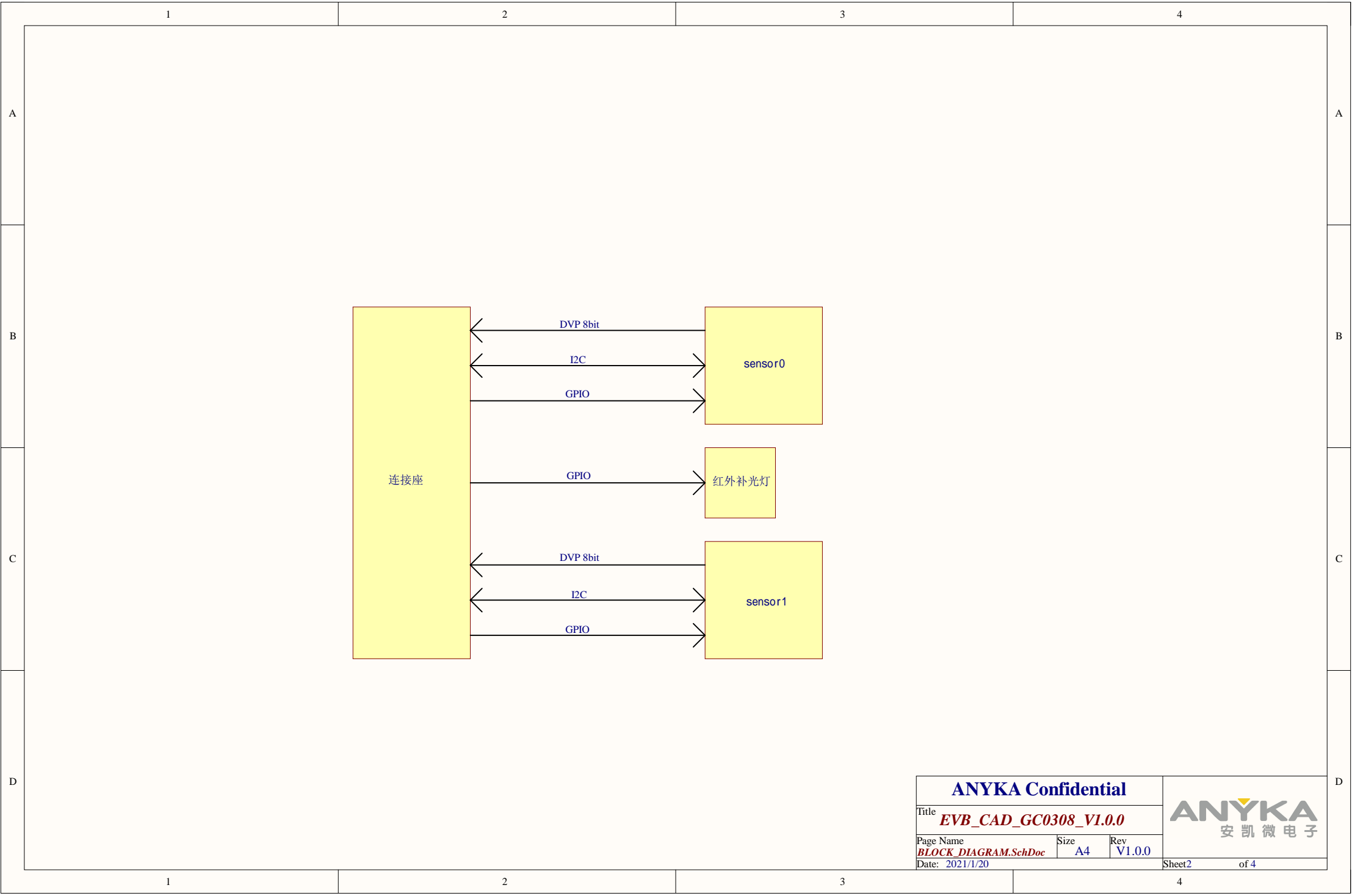
Rev

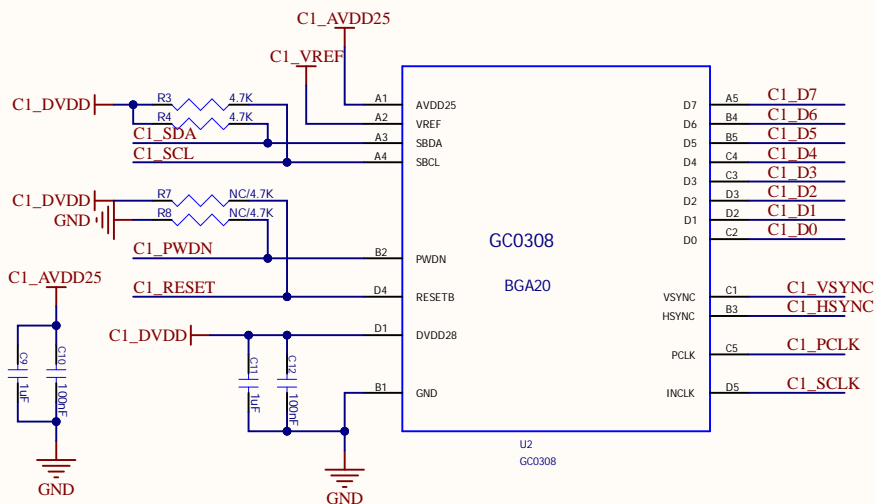
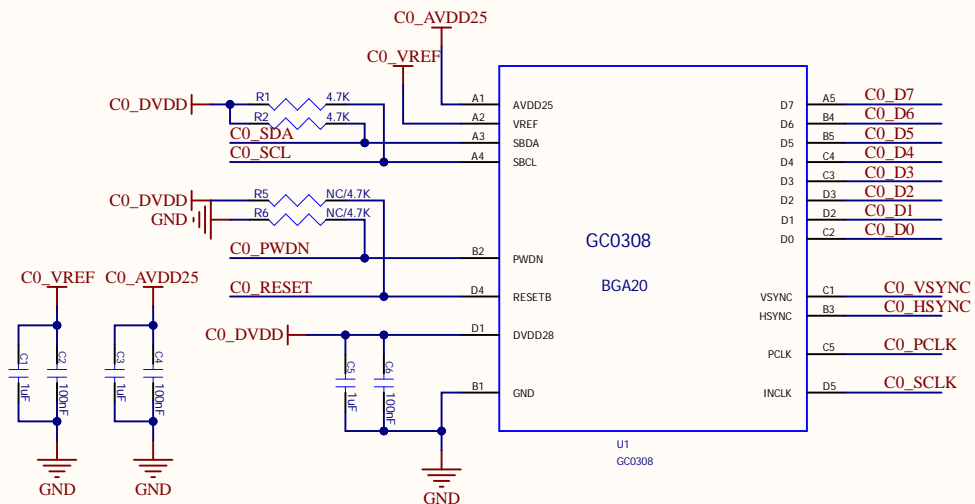
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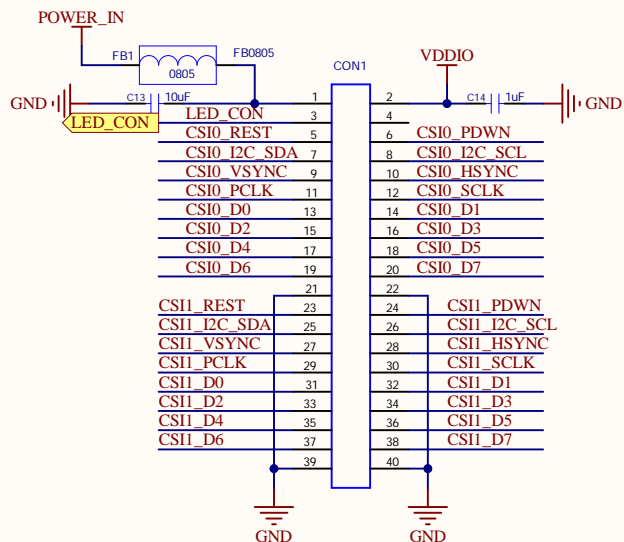
安凯微电子

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CAMERA接口



CS10_D7 R14 0R C0_D7
 CS10_D6 R16 0R C0_D6
 CS10_D5 R18 0R C0_D5
 CS10_D4 R20 0R C0_D4
 CS10_D3 R21 0R C0_D3
 CS10_D2 R23 0R C0_D2
 CS10_D1 R25 0R C0_D1
 CS10_D0 R27 0R C0_D0

CS10_VSYNC R29 0R C0_VSYNC
 CS10_HSYNC R31 0R C0_HSYNC
 CS10_PCLK R33 0R C0_PCLK
 CS10_SCLK R34 0R C0_SCLK

CS10_I2C_SDA R37 0R C0_SDA
 CS10_I2C_SCL R38 0R C0_SCL

CS10_PWDN R39 0R C0_PWDN
 CS10_RESET R40 0R C0_RESET

CS11_D7 R9 0R C1_D7
 CS11_D6 R10 0R C1_D6
 CS11_D5 R11 0R C1_D5
 CS11_D4 R12 0R C1_D4
 CS11_D3 R13 0R C1_D3
 CS11_D2 R15 0R C1_D2
 CS11_D1 R17 0R C1_D1
 CS11_D0 R19 0R C1_D0

CS11_VSYNC R22 0R C1_VSYNC
 CS11_HSYNC R24 0R C1_HSYNC
 CS11_PCLK R26 0R C1_PCLK
 CS11_SCLK R28 0R C1_SCLK

CS11_I2C_SDA R30 0R C1_SDA
 CS11_I2C_SCL R32 0R C1_SCL

CS11_PWDN R35 0R C1_PWDN
 CS11_RESET R36 0R C1_RESET

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Page Name **SENSOR.SchDoc** Size **A4** Rev **V1.0.0**
 Date: 2021/1/20

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