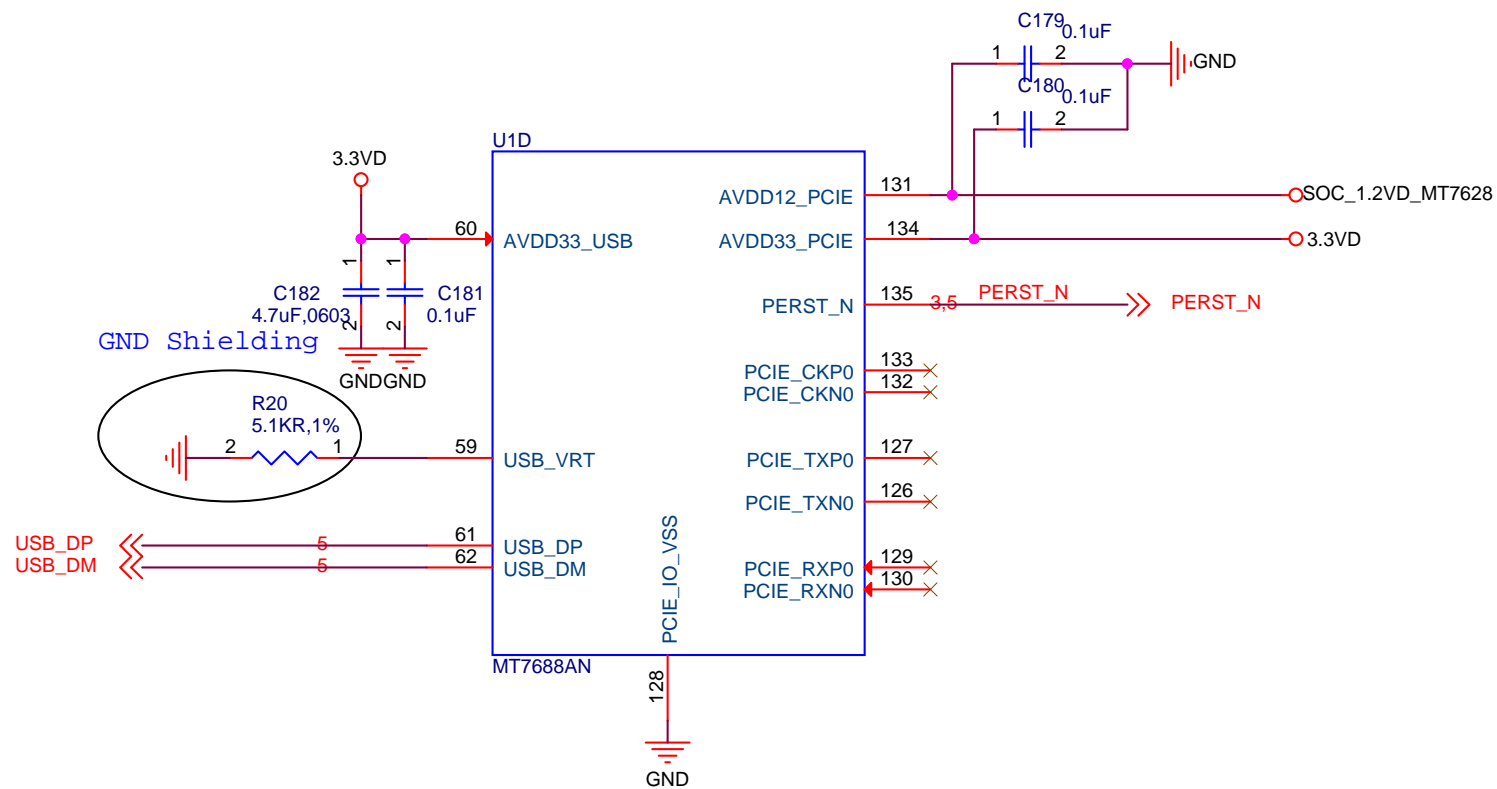


Bootstrapping Pins Description

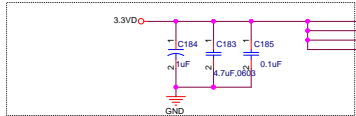
Pin Name	Bootstrapping Signal Name	Description
UART_TXD1	DBG_JTAG_MODE	0: JTAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.
[SPI_MOSI, SPI_CLK, SPI_CS1]	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)

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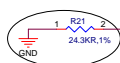


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Close to MT7688A



Close to MT7688A



- GPIO_39 139
- GPIO_40 140
- GPIO_41 141
- GPIO_42 142
- GPIO_43 143

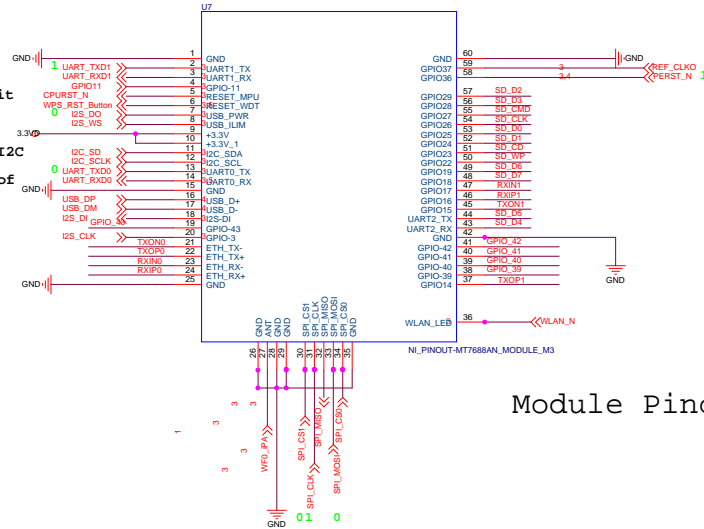
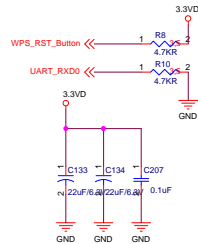
U1E
MT7688AN

- AVDD33_TX_P0 32
- AVDD33_COM 38
- AVDD33_TX_P1234_1 41
- AVDD33_TX_P1234_2 45
- MDI_TN_P4 57
- MDI_TP_P4 58
- MDI_RN_P4 59
- MDI_RP_P4 54
- SD_D2 57
- SD_D3 58
- SD_CMD 59
- SD_CLK 54
- SD_CD 50
- SD_WP 49
- SD_D0 52
- SD_D1 51
- SD_D4 48
- SD_D5 47
- SD_D6 46
- SD_D7 45
- TXON1 42
- TXOP1 40
- RXIN1 44
- RXIP1 43
- TXON0 36
- TXOP0 35
- RXIN0 34
- RXIP0 33
- EPHY_VRT 39
- EPHY_LED4_N_JTRST_N 139
- EPHY_LED3_N_JTCLK 140
- EPHY_LED2_N_JTMS 141
- EPHY_LED1_N_JTDI 142
- EPHY_LED0_N_JTDO 143

Power on Reset Circuit

Require pull up of I2C bus on BaseBoard
Require pull down of RXD0 on BaseBoard

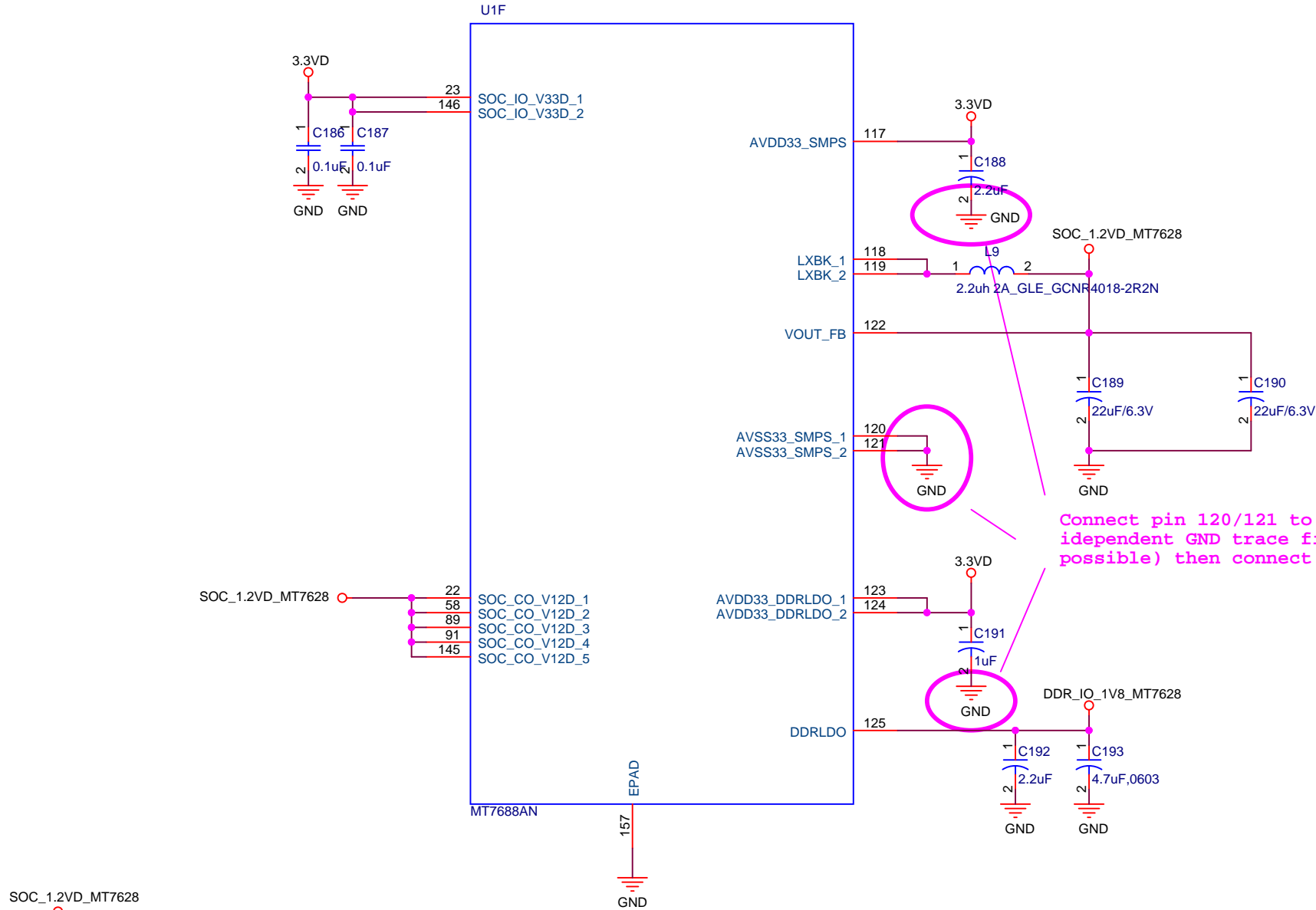
EHT0_LED_N



Module Pinout

Bootstrapping Pins Description

Pin Name	Boot Strapping Signal Name	Description
UART_TXD1	DBG_ITAG_MODE	0: ITAG_MODE 1: EPHY_LED (default)
PERST_N	XTAL_FREQ_SEL	0: 25 MHz DIP 1: 40 MHz SMD
I2S_SDO	DRAM_TYPE	1: DDR1 0: DDR2 [note] This pin is valid for MT7628AN only. It needs to be pull-low for 7628KN which only supports DDR1.
[SPI_MOSI, SPI_CLK, SPI_CS1]	CHIP_MODE[2:0]	A vector to set chip function/test/debug modes. 000: Boot from PLL (boot from SPI 3-Byte Addr) 001: Boot from PLL (boot from SPI 4-Byte Addr) 010: Boot from XTAL (boot from SPI 3-Byte Addr) 011: Boot from XTAL (boot from SPI 4-Byte Addr)
PAD_TXD0	EXT_BGCK	1: Test Mode 0: Normal (default)



Connect pin 120/121 to C86/C88 GND pin with independent GND trace first (as short as possible) then connect to other GND plane

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MDATA[0:15]

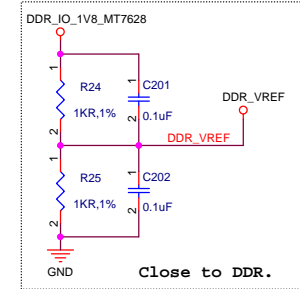
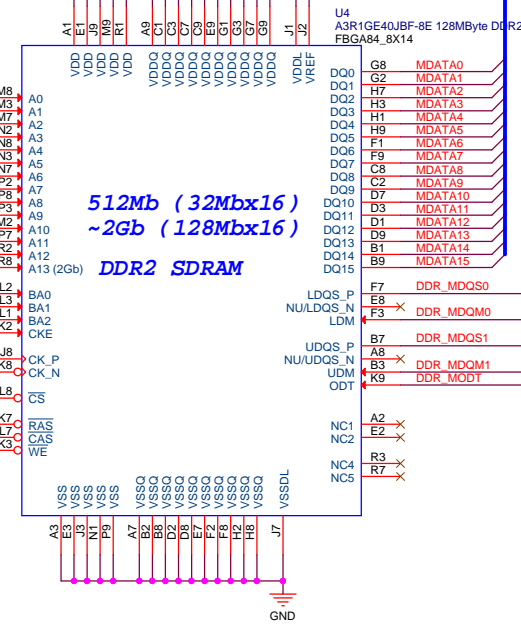
MADDR[0:13]

DDR_BA0
DDR_BA1
DDR_BA2
DDR_MCKE

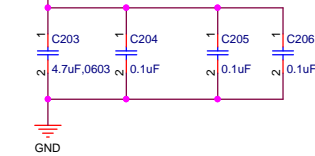
DDR_CSN
DDR_RASN
DDR_CASN
DDR_WEN

CLK_P
CLK_N

DDR_IO_1V8_MT7628



DDR_IO_1V8_MT7628



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