DisplayID v2.0 Errata E6
Published 3/15/20

This errata contains all SCRs published through 3/15/20.

The following SCRs are included in DisplayID_v2.0_E6:

- Timing Formula Field Clarification in Type IX Timing Descriptor
- Missing Data Block Payload Length in Table B-1
- Appendix A Detailed Timing Corrections
- Appendix A ColorCorrections
- Support DisplayID version 2 section as a base EDID extension
- Appendix A Color Signaling Capabilities
- Color Depth Mode Support and YCbCr 420 clarification
- DSC pass-through timing support
- Maximum Vertical Refresh Rate field extension of Dynamic Video Timing Range Limit Data Block

VESA STANDARDS CHANGE REQUEST FORM

To be filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	Timing Formula Field Clarification in Type IX Timing Descriptor
AFFECTED DOCUMENT:	DisplayID v2.0
REVISION CATEGORY:	Category 1
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Bob Ridenour, Apple Inc.

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
12/12/2017	**Initial Submission of SCR**

(add more rows as needed)

To be filled in by VESA Office:

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SCR ADOPTED, REJECTED, or otherwise DISPOSITIONED for other action	SCR is (adopted) or (rejected) or (Dispositioned for other action) If rejected, explain reason for acceptation or rejection If dispositioned, explain action or plan for action (such as including in future draft specification revision, or re-visiting at future date, or other)
DATE SCR ADOPTED or REJECTED or DISPOSITIONED	02/02/2018 Adopted

Summary of the Proposed Change(s)

This change makes the intended references to the CVT specification in the Type IX Timing Descriptor more explicit (including section numbers), without changing the intent.

IPR (Intellectual Property Rights) declaration, if any

None

Benefits as a Result of the Changes

References to timing formulas in the CVT specification will be clear to implementers.

Assessment of the Impact

No expected impact. This change is intended to be purely editorial to clarify references to the timing formulas in the CVT v1.2 specification.

Analysis of the Device Hardware Implications

No known impact to HW implementations.

Analysis of the Device Software Implications

No known impact to SW implementations, unless the intent of the enumerated timing formula references was misunderstood. Any possible impact would be limited to associating each timing formula with a different enumerated value.

Analysis of the Compliance Test & Interop Implications

None.

New Referenced Documents Resulting from Change

None.

Attachments

None.

Proposed Document Change(s) or Addition(s)

Table 4-21: Type IX Formula-based Timing Descriptor Format

Byte #	Bit #	Description/Format	Flag	Tag
0	**Timing Options**			
	2:0	**Timing Formula/Algorithm** 000b = ~~*CVT Standard v1.2* and higher's standard blanking.~~ CVT Formula - Standard Blanking Timing (*CVT v1.2, section 3.4.1*). 001b = ~~*CVT Standard v1.1* and higher's reduced blanking.~~ CVT Formula - Reduced Blanking Timing Version 1 (*CVT v1.2, section 3.4.2*). 010b = ~~*CVT Standard v1.2* and higher's reduced blanking.~~ CVT Formula - Reduced Blanking Timing Version 2 (*CVT v1.2, section 3.4.3*). All other values are RESERVED.		✔

Background Information

It appears that the version number of the reduced blanking formula referenced in the CVT standard got mixed up with the version number of the CVT standard itself. The previous version of the DisplayID specification referred to all three of these formulas, so implementers should be familiar with them, and this change simply makes the expected references to the CVT v1.2 specification very explicit.

- End of Document -

VESA STANDARDS CHANGE REQUEST FORM

To be filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	Missing Data Block Payload Length in Table B-1
AFFECTED DOCUMENT:	DisplayID v2.0
REVISION CATEGORY:	Category 1
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Bob Ridenour, Apple Inc.

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
04/10/2018	**Initial Submission of SCR**

(add more rows as needed)

To be filled in by VESA Office:

VESA SCR NUMBER:	(To be assigned by VESA office)
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DATE SCR ADOPTED or REJECTED or DISPOSITIONED	05/05/2018 Adopted

Summary of the Proposed Change(s)

This change inserts a missing header byte in the description of the VESA Organization Vendor-specific Data Block in Table B-1 of Appendix B.

IPR (Intellectual Property Rights) declaration, if any

None

Benefits as a Result of the Changes

The definition of the VESA Organization Vendor-specific Data Block in Table B-1 will include the mandatory Data Block header bytes, avoiding implementer confusion.

Assessment of the Impact

No expected impact. This change is intended to be purely editorial as the missing byte is clearly defined in section 4.9 where the required structure of the Vendor-specific Data Block is specified.

Analysis of the Device Hardware Implications

No known impact to HW implementations.

Analysis of the Device Software Implications

No known impact to SW implementations.

Analysis of the Compliance Test & Interop Implications

None.

New Referenced Documents Resulting from Change

None.

Attachments

None.

Proposed Document Change(s) or Addition(s)

Table B-1: VESA Organization Vendor-specific Data Block

Offset	Bit #	Description/Format	Tag
00h	7:0	**Vendor-specific Data Block** Value is 7Eh.	✔
01h	**Block Revision and Other Data**		
	2:0	**Block Revision** Revision values range from 0 through 7. 000b = Revision 0 (default).	
	7:3	**RESERVED** Cleared to all 0s.	
02h	7:0	**Number of Payload Bytes in Block** Number of bytes range from 3 through 248. 05h = Payload length	
03h	7:0	**IEEE OUI First Byte** Values range from 0 through 255. 3Ah = First VESA IEEE OUI byte.	
04h	7:0	**IEEE OUI Second Byte** Values range from 0 through 255. 02h = First VESA IEEE OUI byte.	
05h	7:0	**IEEE OUI Third Byte** Values range from 0 through 255. 92h = First VESA IEEE OUI byte.	
06h	**VESA Data Structure Type**		
	2:0	**Data Structure Type** 000b = Embedded DisplayPort (eDP). 001b = External DisplayPort. All other values are RESERVED for future use.	
	6:3	**RESERVED** Cleared to all 0s.	

	7	**Default Color Space and EOTF Handling** 0 = MISC signaling of "RGB unspecified color space" by a Source device is interpreted by a Sink device as sRGB color space and EOTF. 1 = MISC signaling of "RGB unspecified color space" by a Source device is interpreted by a Sink device as "native" color space and EOTF as specified in the Display Parameters data block.	
07h	3:0	**Number of Pixels in Horizontal Pixel Count Overlapping an Adjacent Panel Segment** Values range from 0 through 8. Value range of 9 through 15 is RESERVED.	
	4	**RESERVED** Cleared to 0.	
	6:5	**Multi-SST Operation** 00b = Not supported (Conventional Single-Stream Transport). 01b = Two streams (number of links shall be two or four). 10b = Four streams (number of links shall be four). 11b = RESERVED for future use.	
	7	**RESERVED** Cleared to 0.	

Background Information

It appears that during the final editing process, the required payload length byte in the Vendor-specific Data Block was inadvertently removed and the bytes at offsets 03h through 06h were moved up. The payload length byte is a required element of the Data Block, so it must be included in order for this VESA Organization Vendor-specific Data Block to be valid.

- End of Document -

VESA STANDARDS CHANGE REQUEST FORM

To be filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	Appendix A Detailed Timing Corrections
AFFECTED DOCUMENT:	DisplayID v2.0
REVISION CATEGORY:	Category 1
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Bob Ridenour, Apple Inc.

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
04/10/2018	**Initial Submission of SCR**

(add more rows as needed)

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VESA SCR NUMBER:	(To be assigned by VESA office)
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SCR ADOPTED, REJECTED, or otherwise DISPOSITIONED for other action	SCR is (adopted) or (rejected) or (Dispositioned for other action) If rejected, explain reason for acceptation or rejection If dispositioned, explain action or plan for action (such as including in future draft specification revision, or re-visiting at future date, or other)
DATE SCR ADOPTED or REJECTED or DISPOSITIONED	06/15/2018 - Adopted

Summary of the Proposed Change(s)

This change corrects some minor errors in the Type VII detailed timing descriptors that are included in the example DisplayID structure in Appendix A. It also adds the previously unspecified section checksum to the example DisplayID structure in Appendix A.

IPR (Intellectual Property Rights) declaration, if any

None

Benefits as a Result of the Changes

The timings defined in the example in Appendix A will be consistent with the definition of Type VII detailed timings in the DisplayID specification, and CVT Reduced Blanking version 2 in the CVT specification.

Assessment of the Impact

No expected impact. This change is intended to be purely editorial as it corrects some values in an example structure only. The normative parts of the DisplayID and CVT specs that are relevant to the example are not affected.

Analysis of the Device Hardware Implications

No known impact to HW implementations.

Analysis of the Device Software Implications

No known impact to SW implementations.

Analysis of the Compliance Test & Interop Implications

None.

New Referenced Documents Resulting from Change

None.

Attachments

None.

Proposed Document Change(s) or Addition(s)

4Bh	0x22	**Data Block Name**	Type VII Detailed Timing Data Block.
4Ch	0x00	**Block Revision and Other Data**	Bits 7:3 = RESERVED = 00000b. Bits 2:0 = Block Revision = 0.
4Dh	0x3C	**Number of Payload Bytes in Block**	Payload Length = 60 bytes.
4Eh 4Fh 50h 51h 52h 53h 54h 55h 56h 57h 58h 59h 5Ah 5Bh 5Ch 5Dh 5Eh 5Fh 60h 61h	0xC~~8~~7 0x7E 0x08 0x88 0xFF 0x0F 0x4F 0x00 0x07 0x80 0x1F 0x00 0x6F 0x08 0x3D 0x00 0x~~00~~2F 0x00 0x07 0x00	**Timing 1**	Pixel Clock = 556.744MP/s. Bit 7 = 1 (Preferred Detailed timing). Bits 6:5 = 00b (Timing always mono – no stereo). Bit 4 = 0 (Progressive scan frame). Bits 3:0 = 1000b (Aspect Ratio calculated from pixel dimensions). Horizontal Active Image Pixels = 4096. Horizontal Blank Pixels = 80. Horizontal Sync Offset (front porch) = 8. Horizontal Sync Polarity = 1 (positive). Horizontal Sync Width = 32. Vertical Active Image Lines = 2160. Vertical Blank Lines = 62. Vertical Sync Offset (front porch) = ~~1~~48. Vertical Sync Polarity = 0 (negative). Vertical Sync Width = 8.

62h 63h 64h 65h 66h 67h 68h 69h 6Ah 6Bh 6Ch 6Dh 6Eh 6Fh 70h 71h 72h 73h 74h 75h	0x5D 0x94 0x03 0x08 0xFF 0x09 0x4F 0x00 0x07 0x80 0x1F 0x00 0x9F 0x05 0x28 0x00 0x~~00~~1A 0x00 0x07 0x00	**Timing 2**	Pixel Clock = 234.590MP/s. Bit 7 = 0 (Not a preferred detailed timing). Bits 6:5 = 00b (Timing always mono – no stereo). Bit 4 = 0 (Progressive scan frame). Bits 3:0 = 1000b (Aspect Ratio calculated from pixel dimensions). Horizontal Active Image Pixels = 2560. Horizontal Blank Pixels = 80. Horizontal Sync Offset (front porch) = 8. Horizontal Sync Polarity = 1 (positive). Horizontal Sync Width = 32. Vertical Active Image Lines = 1440. Vertical Blank Lines = 41. Vertical Sync Offset (front porch) = ~~1~~27. Vertical Sync Polarity = 0 (negative). Vertical Sync Width = 8.
76h 77h 78h 79h 7Ah 7Bh 7Ch 7Dh 7Eh 7Fh 80h 81h 82h 83h 84h 85h 86h 87h 88h 89h	0xC7 0x08 0x02 0x08 0x7F 0x07 0x4F 0x00 0x07 0x80 0x1F 0x00 0x37 0x04 0x1E 0x00 0x~~00~~10 0x00 0x07 0x00	**Timing 3**	Pixel Clock = 133.320MP/s. Bit 7 = 0 (Not a preferred detailed timing) Bits 6:5 = 00b (Timing always mono – no stereo) Bit 4 = 0 (Progressive scan frame) Bits 3:0 = 1000b (Aspect Ratio calculated from pixel dimensions). Horizontal Active Image Pixels = 1920. Horizontal Blank Pixels = 80. Horizontal Sync Offset (front porch) = 8. Horizontal Sync Polarity = 1 (positive). Horizontal Sync Width = 32. Vertical Active Image Lines = 1080. Vertical Blank Lines = 31. Vertical Sync Offset (front porch) = ~~1~~17. Vertical Sync Polarity = 0 (negative). Vertical Sync Width = 8.

8Ah	0x66	**Checksum Section**	

Background Information

The pixel rate specified in the raw data of the first Type VII timing in the example structure is off by one. The description of the pixel rate, however, is correct.

All three of the Type VII timings in the example structure are intended to be compliant with the CVT Reduced Blanking version 2 standard. However, when the example was generated, the Vertical Sync Offset was generated incorrectly. This field needs to be corrected for all three timings in order to match the correct CVT generated timing.

The section checksum was previously not specified. It is now included for the example structure.

- End of Document -

VESA STANDARDS CHANGE REQUEST FORM

To be filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	Appendix A Color Corrections
AFFECTED DOCUMENT:	DisplayID v2.0
REVISION CATEGORY:	Category 1
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Bob Ridenour, Apple Inc.

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
10/09/2018	**Initial Submission of SCR**

(add more rows as needed)

To be filled in by VESA Office:

VESA SCR NUMBER:	(To be assigned by VESA office)
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DATE SCR ADOPTED or REJECTED or DISPOSITIONED	11/09/2018 - Adopted

Summary of the Proposed Change(s)

This change corrects a minor error in the Display Parameters Data Block that is included in the example DisplayID structure in Appendix A. The raw value of the Native Color Chromaticity (Green) field is corrected to accurately reflect the interpretation.

IPR (Intellectual Property Rights) declaration, if any

None

Benefits as a Result of the Changes

The interpretation of the Chromaticity fields in the example in Appendix A will be consistent with the raw values provided in the example.

Assessment of the Impact

No expected impact. This change is purely editorial as it corrects a value in an example structure only.

Analysis of the Device Hardware Implications

No known impact to HW implementations.

Analysis of the Device Software Implications

No known impact to SW implementations.

Analysis of the Compliance Test & Interop Implications

None.

New Referenced Documents Resulting from Change

None.

Attachments

None.

Proposed Document Change(s) or Addition(s)

2Eh 2Fh 30h	0x45 0x~~5~~64 0xA6	**Native Color Chromaticity (Green)**	Green X = 0.267, Y = 0.650.

Background Information

The example DisplayID structure in Appendix A includes a Display Parameters Data Block that includes Native Color Chromaticity values. The native green chromaticity is intended to match the interpretation which is stated in decimal as "Y=0.650". The raw value for this parameter is given in the example as 0xA65. However, the correct raw value converted from 0.650 is 0xA66. This change simply corrects the raw value in the example structure to match the stated interpretation.

- End of Document -

VESA STANDARDS CHANGE REQUEST FORM

To be Filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	Support DisplayID version 2 section as a base EDID extension
AFFECTED DOCUMENT:	DisplayID standard version 2.0
REVISION CATEGORY:	
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Syed Athar Hussain

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
MM/DD/YYYY	**11/26/18 Version 1**
	12/4/2018 Version 2

(add more rows as needed)

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VESA SCR NUMBER:	(To be assigned by VESA office)
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SCR ADOPTED, REJECTED, or otherwise DISPOSITIONED for other action	SCR is (adopted) or (rejected) or (Dispositioned for other action) If rejected, explain reason for acceptation or rejection If dispositioned, explain action or plan for action (such as including in future draft specification revision, or re-visiting at future date, or other)
DATE SCR ADOPTED or REJECTED or DISPOSITIONED	03/17/2019 - Adopted

Summary of the Proposed Change(s)

This SCR adds the necessary framework in the DisplayID version 2.0 specification to enable support of DisplayID version 2 section as a base EDID extension.

IPR (Intellectual Property Rights) declaration, if any

None.

Benefits as a Result of the Changes

DisplayID version 2.0 section can be utilized as base EDID extension.

Assessment of the Impact

SW and/or FW need to be updated to be able to support new information exposed in the Display ID version 2.0 section as EDID based extension.

Analysis of the Device Hardware Implication

No HW impact is expected.

Analysis of the Device Software Implications

Some SW impact is expected to support parsing of the new structure as part of the EDID extension block.

Analysis of the Compliance Test & Interop Implications

Need to be updated to ensure correct DisplayID exposure of the structure by the sink and correct parsing of the source.

New Referenced Documents Resulting from Change

None

Attachments

None

Proposed Document Change(s) or Addition(s)

Table 2-4 shall be updated as described below. Note this change applies to DisplayID extension section and changes described here were editorial in nature.

Table 2-4: DisplayID Extension Section Review

Offset	Bit #	Register
00h	**DisplayID Structure Version 2, Revision 0**	
	3:0	**Revision** 0h = Revision 0.
	7:4	**Version** 0h = RESERVED. 2h = Version 2.
01h	7:0	**Bytes in Section** Section length, excluding the five mandatory bytes. Value is *N* - 5.[a]

02h	3:0	**Display Product Primary Use Case** Value shall be 0h.
	7:4	RESERVED, cleared to all 0s.
03h	7:0	**Extension Count** Value shall be 00h
04h	7:0	**Data Block** See Section 3.
…		**…**
(*N* - 1)h[a]		**Checksum** Value ranges from 00h through FFh.

a. N represents the total number of bytes within the DisplayID section.

A new paragraph will be added in section 2 to describe how to set up DisplayID version 2 section as a base EDID extension. The proposed new paragraph is described below.

- Proposed Text Change(s) –

2.1 DisplayID version 2.0 as a base EDID extension

To facilitate usage of DisplayID version 2.0 section as a base EDID extension, a new framework is defined. A Sink with base EDID and utilizing DisplayID version 2.0 section as extension shall populate the listed fields as described below:

- EDID extension block tag shall be set to 70h denoting existence of a DisplayID section
- Following the block tag byte, a regular DisplayID version 2.0 section structure shall be used with a fixed length fill data byte to map to the EDID extension requirement of 128 bytes per extension.
- DisplayID Structure Version/Revision byte shall be set to 20h corresponding to DisplayID version 2 revision 0.
- First DisplayID version 2.0 section as EDID extension shall populate Display Product Primary Use Case byte with a value from 1h-8h based on the intended primary use case of the sink. If the Primary Use Case is not known Sink shall set the value of 2h. Any subsequent DisplayID version 2.0 section EDID extension shall set the Display Product Primary Use Case byte to 0h.
- Extension Count byte shall be set to 00h
- Bytes in Section = Shall be set to 79h (121)
    - This corresponds to 5 additional bytes for the DisplayID section framework + EDID extension block tag for DisplayID and EDID extension block checksum for total of 128 bytes
- EDID extension block checksum shall be calculated using the DisplayID section checksum and extension block tag byte. Since DisplayID section checksum already ensures that all DisplayID section bytes adds up so that modulo 256 of the sums of all byte is 0h, only block tag byte needs to be considered for EDID extension block checksum. Consequently, EDID extension block checksum shall be set to 90h.

The following diagram shows an example of the DisplayID version 2 section as a base EDID extension.

Example: DisplayID Extension to Base EDID – with fill data for fixed length section							
			Field Name	Offset (Dec)	Offset (Hex)	Value (Hex)	Value (Dec)
EDID Extension Format	Display ID 2 EDID Extension	EDID Extension Block Tag	Tag	0	0	70	112
	Display ID Extension Section	Display ID 2 Extension Section Header	Structure Version/Revision	1	0	20	32
			Bytes in Section	2	1	79	121
			Display Product Primary Use Case	3	2	2	2
			Extension Count Reserved (00)	4	3	00	00
		Section Data Block(s) (Example)	Data Block Tag	5	4	ID	ID
			Data Block Revision	6	5	0	0
			Payload Bytes	7	6	6	6
			Payload Bytes #1	8	7	PB1	PB1
			Payload Bytes #2	9	8	PB2	PB2
			Payload Bytes #3	10	9	PB3	PB3
			Payload Bytes #4	11	0A	PB4	PB4
			Payload Bytes #5	12	0B	PB5	PB5
			Payload Bytes #6	13	0C	PB6	PB6
		Fill Data for Fixed Length (Example)	Fill Data #1	14	0D	0	0
			Fill Data #2	15	0E	0	0
			Fill Data #3 ..125	125	7D	0	0
			Section Checksum	126	7E	CHK_DID	CHK_DID
			EDID Extension Block Checksum	127	7F	90	144

Figure X-X: Example of DisplayID version 2 section as a base EDID extension.

Background Information

Additional background for justifying the SCR can be included here. For example, a presentation prepared for Task Group introduction can be placed in this section.

- End of Document -

VESA STANDARDS CHANGE REQUEST FORM

To be filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	Appendix A Color Signaling Capabilities
AFFECTED DOCUMENT:	DisplayID v2.0
REVISION CATEGORY:	TBD
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Bob Ridenour, Apple Inc.

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
12/18/2018	**Initial Submission of SCR**
03/05/2019	TGR Comments Addressed

(add more rows as needed)

To be filled in by VESA Office:

VESA SCR NUMBER:	(To be assigned by VESA office)
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SCR ADOPTED, REJECTED, or otherwise DISPOSITIONED for other action	SCR is (adopted) or (rejected) or (Dispositioned for other action) If rejected, explain reason for acceptation or rejection If dispositioned, explain action or plan for action (such as including in future draft specification revision, or re-visiting at future date, or other)
DATE SCR ADOPTED or REJECTED or DISPOSITIONED	04/22/2019 Adopted

Summary of the Proposed Change(s)

This change adds a VESA Organization Vendor-specific Data Block to the example DisplayID structure in Appendix A in order to clarify how the color space of received pixel data is interpreted by the Sink that is described by the example structure. Additional guidance regarding implied or declared color space signaling is also added.

IPR (Intellectual Property Rights) declaration, if any

None

Benefits as a Result of the Changes

Clarifies how DisplayPort Sources should interpret the capabilities in the example structure, and encourages use of the VESA Organization Vendor-specific Data Block in DisplayID structures in order to remove ambiguity related to use of some color space signaling in DisplayPort.

Assessment of the Impact

No expected impact. This change is editorial in that it modifies the example structure, but not the normative text.

Analysis of the Device Hardware Implications

No known impact to HW implementations.

Analysis of the Device Software Implications

No known impact to SW implementations.

Analysis of the Compliance Test & Interop Implications

None.

New Referenced Documents Resulting from Change

None.

Attachments

None.

Proposed Document Change(s) or Addition(s)

76h 77h 78h 79h 7Ah 7Bh 7Ch 7Dh 7Eh 7Fh 80h 81h 82h 83h 84h 85h 86h 87h 88h 89h	0xC7 0x08 0x02 0x08 0x7F 0x07 0x4F 0x00 0x07 0x80 0x1F 0x00 0x37 0x04 0x1E 0x00 0x10 0x00 0x07 0x00	**Timing 3**	Pixel Clock = 133.320MP/s. Bit 7 = 0 (Not a preferred detailed timing) Bits 6:5 = 00b (Timing always mono – no stereo) Bit 4 = 0 (Progressive scan frame) Bits 3:0 = 1000b (Aspect Ratio calculated from pixel dimensions). Horizontal Active Image Pixels = 1920. Horizontal Blank Pixels = 80. Horizontal Sync Offset (front porch) = 8. Horizontal Sync Polarity = 1 (positive). Horizontal Sync Width = 32. Vertical Active Image Lines = 1080. Vertical Blank Lines = 31. Vertical Sync Offset (front porch) = 17. Vertical Sync Polarity = 0 (negative). Vertical Sync Width = 8.
8Ah	0x7E	**Data Block Name**	Vendor-specific Data Block
8Bh	0x00	**Block Revision and Other Data**	Bits 7:3 = RESERVED = 00000b. Bits 2:0 = Block Revision 0 = 000b.
8Ch	0x05	**Number of Payload Bytes**	Data block is composed of 5 payload bytes.
8Dh 8Eh 8Fh	0x3A 0x02 0x92	**Manufacturer/Vendor ID**	IEEE OUI = 3A-02-92
90h	0x81	**VESA Data Structure Type**	Bit 7 = Default Color Space and EOTF = 1 (RGB unspecified color space is interpreted by the Sink device as native color space and EOTF as specified in the Display Parameters data block) Bits 6:3 = RESERVED = 000b. Bits 2:0 = Data Structure Type = 001b (External DisplayPort)
91h	0x00	**Multi-SST Operation**	Bit 7 = RESERVED = 0b Bits 6:5 = Multi-SST Operation = 00b (Not supported) Bit 4 = RESERVED = 0b

			Bits 3:0 = Number of Pixels in Horizontal Pixel Count Overlapping an Adjacent Panel Segment = 0000b
92h	0x84	**Checksum Section**	

The Sink represented by this example structure interprets pixel data as being in the sRGB color space and transfer function when receiving a DisplayPort VSC packet indicting sRGB.

The Sink represented by this example structure interprets pixel data as being in the native color space and transfer function indicated in the Display Parameters Data Block when receiving a DisplayPort VSC packet indicting Custom Color RGB, or when receiving a DisplayPort MSA packet indicating RGB Unspecified.

Background Information

The example structure declares native primaries and native EOTF in the Display Parameters Data Block. However, it is not clear what signaling a DisplayPort Source device should use to access this color space and transfer function. This is clarified by adding the VESA Organization Vendor-specific Data Block to indicate that MSA packet MISC signaling of "RGB Unspecified" is interpreted by the Sink as being in the native color space and EOTF. Additional guidance is included regarding use of the newer DisplayPort VSC packet signaling to specify sRGB, and Custom Color RGB (native primaries and EOTF).

- End of Document -

VESA STANDARDS CHANGE REQUEST FORM

To be Filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	Color Depth Mode Support and YCbCr 420 clarification
AFFECTED DOCUMENT:	DisplayID ver 2.0
REVISION CATEGORY:	Refer to VP235H Appendix A; will be subject to Task Group review
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Syed Athar Hussain, AMD

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
04/09/2019	Draft 1
04/22/2019	Draft 2 update based on the task group feedback

(add more rows as needed)

To be Filled in by VESA Office:

VESA SCR NUMBER:	(To be assigned by VESA office)
SCR ENTRY DATE:	04/09/2019

To be Filled in by Task Group or VESA Office

SCR ADOPTED, REJECTED, or otherwise DISPOSITIONED for other action	SCR is (adopted) or (rejected) or (Dispositioned for other action) If rejected, explain reason for acceptation or rejection If dispositioned, explain action or plan for action (such as including in future draft specification revision, or re-visiting at future date, or other)
DATE SCR ADOPTED or REJECTED or DISPOSITIONED	07/05/2019 - Adopted

Summary of the Proposed Change(s)

The SCR clarifies mode support rules for various encoding formats with and without certain CTA blocks that are used to limit the mode support to specific VIC, for example YCbCr420 capability map data block and YCbCr420 video data block.

IPR (Intellectual Property Rights) declaration, if any

None

Benefits as a Result of the Changes

Clarification on mode support behavior.

Assessment of the Impact

Provide details.

Analysis of the Device Hardware Implication

No hardware impact is expected.

Analysis of the Device Software Implications

SW and FW may need to be updated to apply the clarification in this document.

Analysis of the Compliance Test & Interop Implications

Expected impact on compliance specially for case of YCbCr 420 mode support behavior with DisplayID.

New Referenced Documents Resulting from Change

DisplayID Ver 2.0.

Attachments

None

Proposed Document Change(s) or Addition(s)

Background Information

4.5.1 Supported Interface Color Depth-related Fields

The four Supported Interface Color Depth-related fields – one byte each for RGB, YCbCr 4:4:4, YCbCr 4:2:2, and YCbCr 4:2:0 pixel encodings, as listed in Table 4-24 – define the supported color depths for corresponding ~~that particular~~ pixel encoding.

Definition of “Supported” and “No support indicated” is as follows:

• **Supported** – Color depth is supported for all supported ~~DisplayID exposed~~ timings. Supported timing includes all Display-ID exposed timings (that is timing exposed using DisplayID timing types and CTA VICs) unless a CTA block is exposed that restrict the support to a limited set of timing for particular pixel encoding, for example, YCbCr420 capability map data block and/or YCbCr420 video data block. If those CTA blocks are exposed, then the support for that pixel encoding would be limited to the timings exposed in the restricted set only.

•**No support indicated** – Sink device has not explicitly reported a color-depth capability in the Display Interface Features data block; thus, the Source device shall rely on other DisplayID data blocks, –or– an interface-specific rule, to determine color-depth support. Examples of other data blocks that may report color-depth capability include ~~the CTA YCbCr 4:2:0,~~ HDMI vendor-specific, and HDMI Forum Vendor-specific data blocks.

Table 4-24: Supported Interface Color Depth-related Field Formats

Offset	Bit #	Description/Format
03h	**Supported Interface Color Depth for RGB Encoding**	
	0	**6 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	1	**8 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	2	**10 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	3	**12 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	4	**14 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	5	**16 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	7:6	**RESERVED** Cleared to all 0s.

Table 4-24: Supported Interface Color Depth-related Field Formats (Continued)

Offset	Bit #	Description/Format
04h	**Supported Interface Color Depth for YCbCr 4:4:4 Encoding**	
	0	**6 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	1	**8 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	2	**10 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	3	**12 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	4	**14 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	5	**16 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	7:6	**RESERVED** Cleared to all 0s.

Table 4-24: Supported Interface Color Depth-related Field Formats (Continued)

Offset	Bit #	Description/Format
05h	**Supported Interface Color Depth for YCbCr 4:2:2 Encoding**	
	0	**8 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	1	**10 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	2	**12 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	3	**14 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	4	**16 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	7:5	**RESERVED** Cleared to all 0s.
06h	**Supported Interface Color Depth for YCbCr 4:2:0 Encoding**	
	0	**8 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	1	**10 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	2	**12 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	3	**14 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	4	**16 bits per Primary Color** 0 = No support indicated. 1 = Supported.
	7:5	**RESERVED** Cleared to all 0s.

4.5.2 Minimum Pixel Rate at Which YCbCr420 Encoding Is Supported

The Minimum Pixel Rate at Which YCbCr 4:2:0 Encoding Is Supported field indicates the minimum pixel rate at which the Sink device shall support YCbCr 4:2:0 encoding, as indicated in the Supported Interface Color Depth for YCbCr 4:2:0 Encoding field (offset 06h). The Source device shall use YCbCr 4:2:0 encoding only for supported ~~DisplayID-exposed~~ modes that meet or exceed the listed pixel rate. A value of 00h in this field shall indicate that the Sink device can support YCbCr 4:2:0 encoding at all supported ~~DisplayID-exposed~~ modes. Note that if, YCbCr420 capability map data block and YCbCr420 video data block is used to limit the YCbCr 420 timing support then the field shall be set to 00h and support for 420 pixel encoding is limited to the timings exposed in the restricted set exposed in the CTA data block. For further details of supported mode rules please refer to section 4.5.1.

Table 4-25 defines the byte format.

Table 4-25: Minimum Pixel Rate at Which YCbCr 4:2:0 Encoding Is Supported Field Format

Offset	Bit #	Description
07h	7:0	**Minimum Pixel Rate at Which YCbCr 4:2:0 Encoding Is Supported** YCbCr 4:2:0 Minimum Pixel Rate Requirement = 74.25MP/s × field value 00h = Sink device can support YCbCr 4:2:0 encoding at all DisplayID-exposed modes.

- End of Document -

VESA STANDARDS CHANGE REQUEST FORM

To be Filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	DSC pass-through timing support
AFFECTED DOCUMENT:	DisplayID ver 2.0
REVISION CATEGORY:	Refer to VP235H Appendix A; will be subject to Task Group review
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Syed Athar Hussain, AMD

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
07/16/2019	Initial Draft, rev1
07/30/2019	Rev2, Incorporated task group feedback on explicit tie in between passthrough timing and the VESA VSDB fields.

(add more rows as needed)

To be Filled in by VESA Office:

VESA SCR NUMBER:	(To be assigned by VESA office)
SCR ENTRY DATE:	07/16/2019

To be Filled in by Task Group or VESA Office

SCR ADOPTED, REJECTED, or otherwise DISPOSITIONED for other action	SCR is (adopted) or (rejected) or (Dispositioned for other action) If rejected, explain reason for acceptation or rejection If dispositioned, explain action or plan for action (such as including in future draft specification revision, or re-visiting at future date, or other)
DATE SCR ADOPTED or REJECTED or DISPOSITIONED	10/04/2019 - Adopted

Summary of the Proposed Change(s)

The SCR extends exiting data blocks to support DSC pass-through for some exposed timings. A new version of the Type VII timing data block with a flag to indicate pass-through timing support is added along with new bytes in VESA vendor specific data block to expose the DSC integer and fractional target bit depth.

IPR (Intellectual Property Rights) declaration, if any

None

Benefits as a Result of the Changes

DSC pass-through timing support.

Assessment of the Impact

SW/FW update on source and sinks side.

Analysis of the Device Hardware Implication

No hardware impact is expected.

Analysis of the Device Software Implications

SW and FW may need to be updated to support the new field described in the document.

Analysis of the Compliance Test & Interop Implications

Currently no compliance exits, if required a new DSC pass-through compliance support can be verified with this framework.

New Referenced Documents Resulting from Change

DisplayID Ver 2.0.

Attachments

None

Proposed Document Change(s) or Addition(s)

Background Information

4.3.1 Type VII Timing – Detailed Timing Data Block

Table 4-17: Type VII Timing – Detailed Timing Data Block Format

Offset	Bit #	Description/Format/Priority	Tag
00h	7:0	**Type VII Timing – Detailed Timing Data Block** Value is 22h.	✔
01h	**Block Revision and Other Data**		
	2:0	**Block Revision** Revision values range from 0 through 7. 000b = Revision 0 (default). **001b = Revision 1 (redefined (bit 3 of byte 1) as a flag indicating DSC pass-through timing support for all listed timing in the block)**	
	3	**For Block Revision 0** Bit 3 shall be 0. **For Block Revision 1** Value 0 = Same as revision 0 (standard timing support declaration ~~only~~ as original specification) Value 1 = Indicates listed timing descriptors in the data block are supported with DSC pass-through with DSC RGB encoding and specific target DSC bits per pixel only. ~~Pass-through bpp applies as declared in VESA organization vendor-specific data block.~~ For DisplayPort, VESA organization vendor-specific data block shall exists with relevant pass-through integer and fractional DSC bits per pixel declaration if this bit is set; otherwise source shall disregard the timings. ~~DP Tx and Rx shall follow DisplayPort specification rules pertaining to other DSC capability support.~~	
	7:4	**RESERVED** Cleared to all 0s.	
02h	7:0	**Number of Payload Bytes in Block** Number of bytes within the data block range from 20 through 240 ($1 \le N \le 12$). Values are based on $N \times 20$ – 14h, 28h, 3Ch, and so forth, through F0h. All other values are RESERVED.	
03h – 16h	159:0	**First Type VII Detailed Timing Descriptor** 20-byte descriptor. Priority 1.	
17h – 2Ah	159:0	**Second Type VII Detailed Timing Descriptor** 20-byte descriptor, if present. Priority 2.	
…		…	

B VESA Organization Vendor-specific Data Block

Table B-1: VESA Organization Vendor-specific Data Block (Continued)

Offset	Bit #	Description/Format	Tag
07h	5:0	**Pass through timing's integer target DSC bits per pixel** Integer portion of target DSC bits per pixel for pass-through timing descriptors declared in Type VII timing data block with revision 1 and higher and byte 1h and bit 3 set to value 1 of the timing data block. DP Tx and Rx shall follow DisplayPort specification rules pertaining to other DSC capability support. Valid value is 0 and 8 through 16 integer target DSC bits per pixel, all other values are reserved and shall not be used.	
	7:6	**RESERVED** Shall be set to 0.	
08h	3:0	**Pass through timing's fractional target DSC bits per pixel** Fractional portion of target DSC bits per pixel for pass-through timing descriptors declared in Type VII timing data block with revision 1 and higher and byte 1h and bit 3 set to value 1 of the timing data block. DP Tx and Rx shall follow DisplayPort specification rules pertaining to other DSC capability support. Valid value range is 0 through 15 corresponding to fraction DSC bit per pixel of (1/16) * value. Note value of 0 indicates no fractional DSC bits per pixel exists.	
	7:4	**RESERVED** Shall be set to 0.	

- End of Document -

VESA STANDARDS CHANGE REQUEST FORM

To be Filled in by Submitter (Refer to VESA Document VP235H, Section 5)

TITLE:	Maximum Vertical Refresh Rate field extension of Dynamic Video Timing Range Limit Data Block
AFFECTED DOCUMENT:	DisplayID ver 2.0
REVISION CATEGORY:	Refer to VP235H Appendix A; will be subject to Task Group review
SUBMITTED TO:	DisplayID Task Group
SPONSOR:	Syed Athar Hussain, AMD

SCR REVISION HISTORY	
(DATE)	**(CHANGE)**
12/17/2019	Initial Draft, rev1

(add more rows as needed)

To be Filled in by VESA Office:

VESA SCR NUMBER:	(To be assigned by VESA office)
SCR ENTRY DATE:	12/17/2019

To be Filled in by Task Group or VESA Office

SCR ADOPTED, REJECTED, or otherwise DISPOSITIONED for other action	SCR is (adopted) or (rejected) or (Dispositioned for other action) If rejected, explain reason for acceptation or rejection If dispositioned, explain action or plan for action (such as including in future draft specification revision, or re-visiting at future date, or other)
DATE SCR ADOPTED or REJECTED or DISPOSITIONED	03/06/2020 Adopted

Summary of the Proposed Change(s)

The SCR extends the Maximum Vertical Refresh Rate field of the Dynamic Video Timing Range Limit Data Block to support higher the 255Hz refresh rate. The SCR also clarifies some of the range values of other fields to explicitly call out the min and max possible values.

IPR (Intellectual Property Rights) declaration, if any

None

Benefits as a Result of the Changes

With this change Adaptive-Sync displays with 255Hz and more can enumerate their capability in a standard method.

Assessment of the Impact

SW/FW update on source and sinks side.

Analysis of the Device Hardware Implication

No hardware impact is expected if higher refresh rate timings are supported. If not supported, then source shall not expose the higher refresh rate timing and revert to a lower timing mode.

Analysis of the Device Software Implications

SW and FW may need to be updated to support the new field associated with new data block revision described in the document.

Analysis of the Compliance Test & Interop Implications

Adaptive-Sync related compliance test would need to be updated for source and sink testing of beyond 255Hz.

New Referenced Documents Resulting from Change

DisplayID Ver 2.0 + SCR.

Attachments

None

Proposed Document Change(s) or Addition(s)

Background Information

Dynamic Video Timing Range Limits Data Block

The Dynamic Video Timing Range Limits data block shall be used to convey the supported timing range of vertical frequencies. Any Sink device that exposes this data block shall indicate support for a seamless, continuous vertical frequency device that can support the seamless timing change for any timing that lies within the specified minimum and maximum pixel rates. Dynamic Video Timing Range Limits is an **optional** data block in Basesections.

Table 4-22 lists the size and order of each field, with all addresses relative to the beginning of the data block.

Table 4-22: Dynamic Video Timing Range Limits Data Block Fields

Offset	Bit #	Description/Format	Flag	Tag
00h	7:0	**Dynamic Video Timing Range Limits Data Block** Value is 25h.		✓
01h	**Block Revision and Other Data**			
	2:0	**Block Revision** Revision ranges from 0 through 7. ~~000b = Revision 0 (default).~~ 001b = Revision 1		
	7:3	**RESERVED** Cleared to all 0s.		
02h	7:0	**Number of Payload Bytes in Block** 09h = Data block is composed of nine payload bytes. All other values are RESERVED.		
05h– 03h	23:0	**Minimum Pixel Clock (in kHz)** ~~Required.~~ The field is required to be populated and specifies the minimum pixel rate above which dynamic video timing changes shall be supported, as per the reported scheme. Range shall be defined as 0.001 through 16,777.216MP/s, where value of 000000h corresponds to 0.001 MP/s and value of FFFFFFh corresponds to 16,777.216MP/s. ~~Value ranges from 000000h through FFFFFFh.~~		

08h – 06h	23:0	**Maximum Pixel Clock (in kHz)** ~~Required.~~ The field is required to be populated and specifies the maximum pixel rate below which dynamic video timing changes shall be supported, as per the reported scheme. Range shall be defined as 0.001 through 16,777.216MP/s, where value of 000000h corresponds to 0.001 MP/s and value of FFFFFFh corresponds to 16,777.216MP/s. ~~Value ranges from 000000h through FFFFFFh.~~		
09h	7:0	**Minimum Vertical Refresh Rate** ~~Required.~~ The field is required to be populated and specifies the display device's minimum dynamic vertical frequency. Vertical frequency shall be defined as follows: *(pixel_clock/horizontal_total) / vertical_total* Range shall be defined as 0 through 255Hz, where value of 00h corresponds to 0Hz and value of FF corresponds to 255Hz. ~~Value ranges from 00h through FFh.~~		

Table 4-22: Dynamic Video Timing Range Limits Data Block Fields (Continued)

Offset	Bit #	Description/Format	Flag	Tag
0Ah	7:0	**Maximum Vertical Refresh Rate (8 least significant bits)** ~~Required.~~ The field is required to be populated and specifies the display device's maximum dynamic vertical frequency. In version 0 of the data block, the "**Maximum Vertical Refresh Rate"** field was 8 bits wide and the range is defined as 0 through 255Hz, where value of 00h corresponds to 0Hz and value of FF corresponds to 255Hz. In version 1 of the data block, the "**Maximum Vertical Refresh Rate"** field is 10 bits wide and the range is defined as 0 through 1023Hz, where value of 00h corresponds to 0Hz and value of 3FF corresponds to 1023Hz. The 8 least significant bits are defined in offset 0Ah and remaining 2 bits are defined in offset 0Bh bit 0 and 1.		
0Bh	**Dynamic Video Timing Range Related and Support Flags**			
	1:0	**Maximum Vertical Refresh Rate most significant bits 9 and 10** In version 0 of the data block the field is set to zero. In version 1 of the data block the bit 0 correspond to the bit 9 and bit 1 correspond to the bit 10 of the "Maximum Vertical Refresh Rate" to all the range to be extended from a max 255 Hz to 1023 Hz.		
	6:2	**RESERVED** Cleared to all 0s.		
	7	**Seamless Dynamic Video Timing Support** 0 = Seamless Dynamic Video Timing change shall not be supported with a fixed horizontal pixel rate and dynamic vertical blanking. 1= Seamless Dynamic Video Timing change shall be supported with a fixed horizontal pixel rate and dynamic vertical blanking.	✓	

- End of Document -