



VME64x IFC_1211 HW Technical User Guide

IFC1211_HW_UG_A0

Preliminary

TITLE :

IFC_1211 Hardware Technical User's Guide

KEY WORD :

VME64xT2081, HSID, PCI Express resources description,

ACCESS CODE :

IOxOS Confidential

SUMMARY :

This document provides detailed informations for programmer and scientific users of the IFC210 equipment includes static options, external connectors assignment, visual indicators, PCI Express resources mapped in the CONFIGURATION Space, IO Space and MEMORY Space.

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IOxOS Technologies SA
4, Chemin des Fontenailles
CH-1196 Gland
SWITZERLAND

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AUTHOR	[JB] Joël Bovier	20 June 2016
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HW Technical User Guide

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Author References

INITIAL	NAME	COMPANY	COMMENTS
[JB]	Joel BOVIER	IOxOS Technologies SA	
[JFG]	Jean François GILOT	IOxOS Technologies SA	

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1. Introduction

This user guide provides a technical hardware description of the IFC_1211 implementation

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1.1 Product Overview

1.1.1 Main Features

Refer to IFC_1211 commercial data-sheet.

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1.1.2 IFC_1210 Backward Compatibility

The IFC_1211 has been designed to keep as far as possible the investment made on IFC_1210.

For more complete IFC_1210 → IFC_1211 migration refer to § 4.1

1.2 References

1.2.1 IOxOS Documentation Architecture

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The IFC_1211 technical documentation is organized around three(3) main user's guide, summarized in following table :

#	Document	Comments
1	IFC1211_HW_UG	
2	IFC1211_ALTHEA_UG	PCI Express to VME64x Bridge
3	IFC1211_XUSER_UG	

Table 1.1 : IOxOS IFC_1211 Documentation Architecture

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1.2.2 Standard Specification References

Following table sums up the standard specification :

#	Document	Comments
1	ANSI/VITA 1-1994 (R2002) for VME64	VME64 standard
2	ANSI/VITA 1.1-1997 (R2003) for VME64 Extensions	VME64x Extensions (160 Pin DIN/IEC Connector)
3	ANSI/VITA 1.5-2003 (R2009) 2eSST	VME64x 2eSST protocol
4	ANSI/VITA 1.7-2003 (R2009) Increased Current Level for 96 Pin & 160 Pin DIN/IEC Connector	VME64x
5	ANSI/VITA 35-2000 (R2005) for PMC-P4 Pin Out Mapping To VME-P0 and VME64x-P2	XMC mapping/PMC JN14 → VME_P2 User IO
6	ANSI/VITA 42.3-2010 XMC PCI Express Protocol Layer Standard	XMC Mezzanine carrier

7	P1386.1/Draft 2.4 Layers for PCI Mezzanine Cards:PMC	PMC Mezzanine carrier
8	ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard	FMC Mezzanine Carrier

Table 1.2 : IOxOS IFC_1211 Standard Specification

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1.2.3 Third-Party Technical References

Following table sums up the related technical references from third parties supplier used on the IFC_1211. These documentations could be required for user specific software/firmware support. Some of them can be only available under NDA.

#	Document	Supplier	Comments
1	T2080RM Rev. 2, 02/2016	NPX/Freescale	QorIQ T2080/T2081 Reference Manual
2	T2081DS Rev. 1, 03/2016	NPX/Freescale	QorIQ T2080/T2081 Data-sheet
3	T2081 Chip Errata, Rev 0, 02/2015	NPX/Freescale	QorIQ T2080/T2081 Errata list
4	PES32NT24AG2	IDT	PCI Express Switch 24 Ports, IFC_1211 on-board PCI Express infrastructure
5	LMK04803	TI	Dual PLL Clock Synthesiser, very low jitter, VCXO Used for IFC_1211 internal programmable clock generation.
6	ARTIX7 FPGA XC7A75	XILINX	On-board PON_FPGA and IO_FPGA
7	KINTEX7 Ultrascale FPGA XCKU040	XILINX	On-board CENTRAL_FPGA
8	DS125MB203	TI	Low-Power 12.5-Gbps Dual-Lane 2:1/1:2 Mux/Buffer With Equalization and De-Emphasis. Used for CENTRAL_FPGA MGT_225, MGT_226 selection
9	LMK00338	TI	8-Output Differential Clock Buffer/Level Translator.
10	CSD16570Q5B	TI	25-V N-Channel NexFET™ Power MOSFET, very low resistance
11	TPS82085	TI	Low current (<3[A]) DCDC with embedded inductor
12	TPS7A7300RGW	TI	3-A, Fast-Transient, Low-Dropout Voltage Regulator
13	TPS386596L33DGKT	TI	Quad Reset Supervisor With Manual Reset Input
14	TPS51200	TI	Sink and Source DDR Termination Regulator
15	BMR463	ERICSSON	High current (25[A]) DCDC with PMBus interface
16	KSZ9031RNX	MICROCHIP	Gigabit Ethernet Transceiver with RGMII Support
17	MAX5970	MAXIM	0V to 16V, Dual Hot-Swap Controller with 10-Bit Current and Voltage Monitor
18	DS1339U-33+	MAXIM	I ² C Serial Real-Time Clock
19	LTC2803	LINEAR	1.8V to 5.5V RS-232 Dual Transceivers
20	MT29F4G08	MICRON	NAND Flash
21	S25FL129P0xNFI00 S25FL512SAGBHI210	CYPRESS	128 Mb SPI Serial Flash EEPROM 512 Mb SPI Serial Flash EEPROM
22	CCLD-033-50-100	CRYSTEK	Oscillator 100 MHz
23	CVHD-037X-100MHz 20ppm	CRYSTEK	Voltage Controlled Oscillator 100 MHz
23	PEX8112-144PA	AVAGO	PCI Express to PCI bridge. Support for PMC mezzanine

Table 1.3 : IOxOS IFC_1211 Third-Party Technical References

1.2.4 Acronyms and Abbreviation

Following table sums up specific abbreviation and acronyms used in this document.

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Following table sums up specific abbreviation and acronyms used in this document.

ABBREVIATION	MEANING
2eSST	
ADC	Analogue to Digital converter
BFM	Bus Functional Model, HDL behaviour model for Bus interface. The IFC_1211 XUSER FDK
CRCRSR	
DAC	Digital to Analogue converter
DUT	Device Under Test
FDK	FPGA Design Kit..
FPGA	Field Programmable Gate Array
NDA	Non Disclosure Agreement
PCI Express / PCIe	Serial based PCI Interface
PLL	Phase Locked Loop
RMW	Read Modify Write, VME atomic transaction type
SERDES	Serializer /de-serializer interface.
TOSCA IIA	IOxOS Technologies FPGA Design Kit based on NoC technology,optimized for XILINX ARTIX7 family.
TOSCA III	IOxOS Technologies FPGA Design Kit based on NoC technology,optimized for XILINX KINZEX Ultrascale family.
VCXO	Voltage Controlled Crystal Oscillator
VHDL	Hardware description language

Table 1.4 : List of Acronyms and Abbreviation

55

1.2.5 Environmental and Regulations

The IFC_1211 is designed to operate and fulfil following environmental conditions

- Storage Temperature -55 to 105 [°C]
- Commercial operating Temperature 0 to 55[°C] (with 200LFM forced air cooling)
- Industrial operating Temperature -25 to 55[°C] (with 400LFM forced air cooling)
- Safety regulation IEC/EN/UL60950
- EMI/RFI regulations EN50022

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The IFC_1211 maximal operating temperature is also conditioned by the several parameters as FPGA type installed, the FPGA firmware, the MPF section, ... To characterize the maximal operating temperature, several thermal sensors are implemented on the critical sections of the IFC_1210. (FPGA die temperature, high current DCDC, ...)

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To satisfy the safety regulations, all IFC_1211 power sources incorporate short circuit protections and over temperature protections .

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- + 5[V] VME power supply → protected with MAX5970
- + 3.3[V] VME power supply → protected with MAX5970
- + 12[V] / -12[V] VME power supplies → protected with fuses
- Ericsson BMR463 internal DC-DC for 1.0[V], 0.95[V] and VADJ (1.5[-1.95V])

85

The IFC_1211 front panel IO connections are protected against ESD as follow

- Ethernet 10/100/1000 Base-T → embedded in the RJ45 JUMBO BELFUSE 0875-1G2T-E3 (2260 V_{DC})
- RS232 → LTC2803 with ±15kV Human Body Model
- USB 2.0 Host → External TVS diode array (D801) SEMTEC RCLAMP0504P
- microSD Holder → SEMTEC ECLAMP2357N ESD protection to IEC 61000-4-2 (ESD) Level4, ±15kV (air), ±8kV (contact)

1.2.6 Ordering Informations

Reference	CENTRAL_FPGA	T2081	DDR3	VME Front Panel	Environmental
IFC1211-A0	XCKU040-1-FFVA	1.8 GHz	2048M	Dual FMC	0 - 50 [°C]
IFC1211-A1	XCKU040-1-FFVA	1.8 GHz	2048M	One FMC + one XMC	0 - 50 [°C]

Table 1.5 : IFC_1211 Options & Ordering Informations

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Note For others IFC_1211 board configuration, and environmental contact directly IOxOS Technologies

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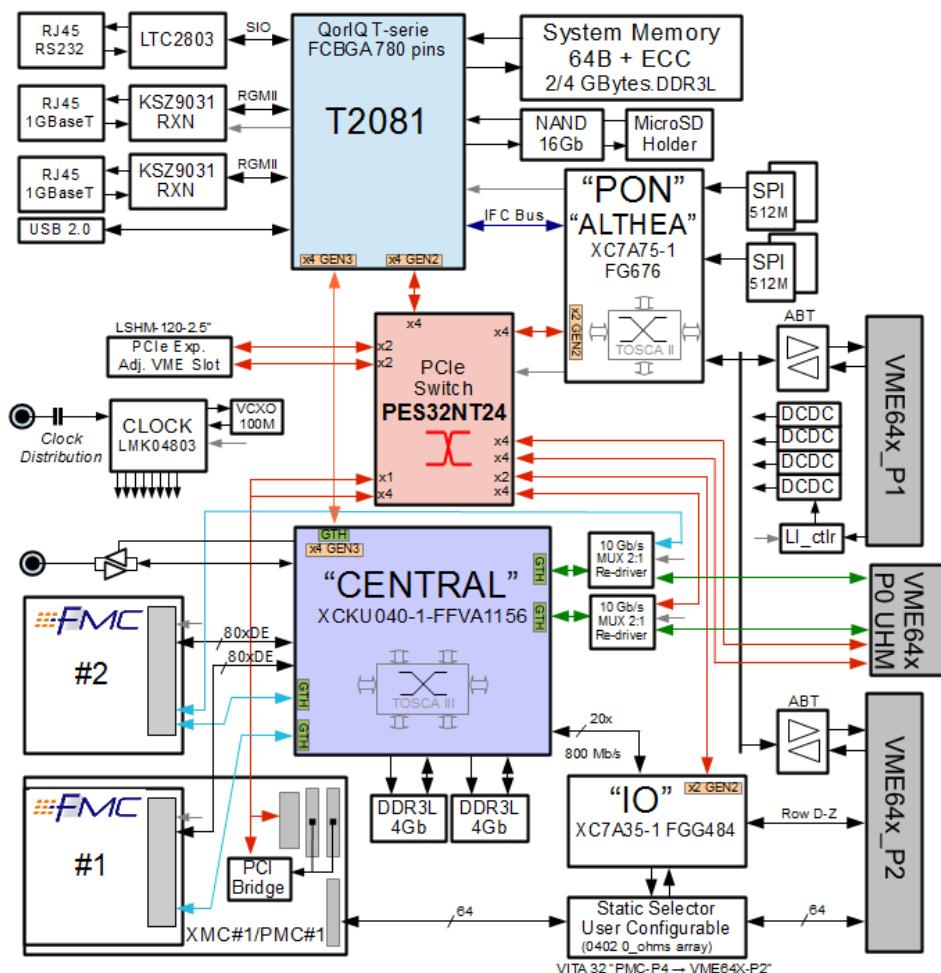
2. IFC_1211 Hardware Description

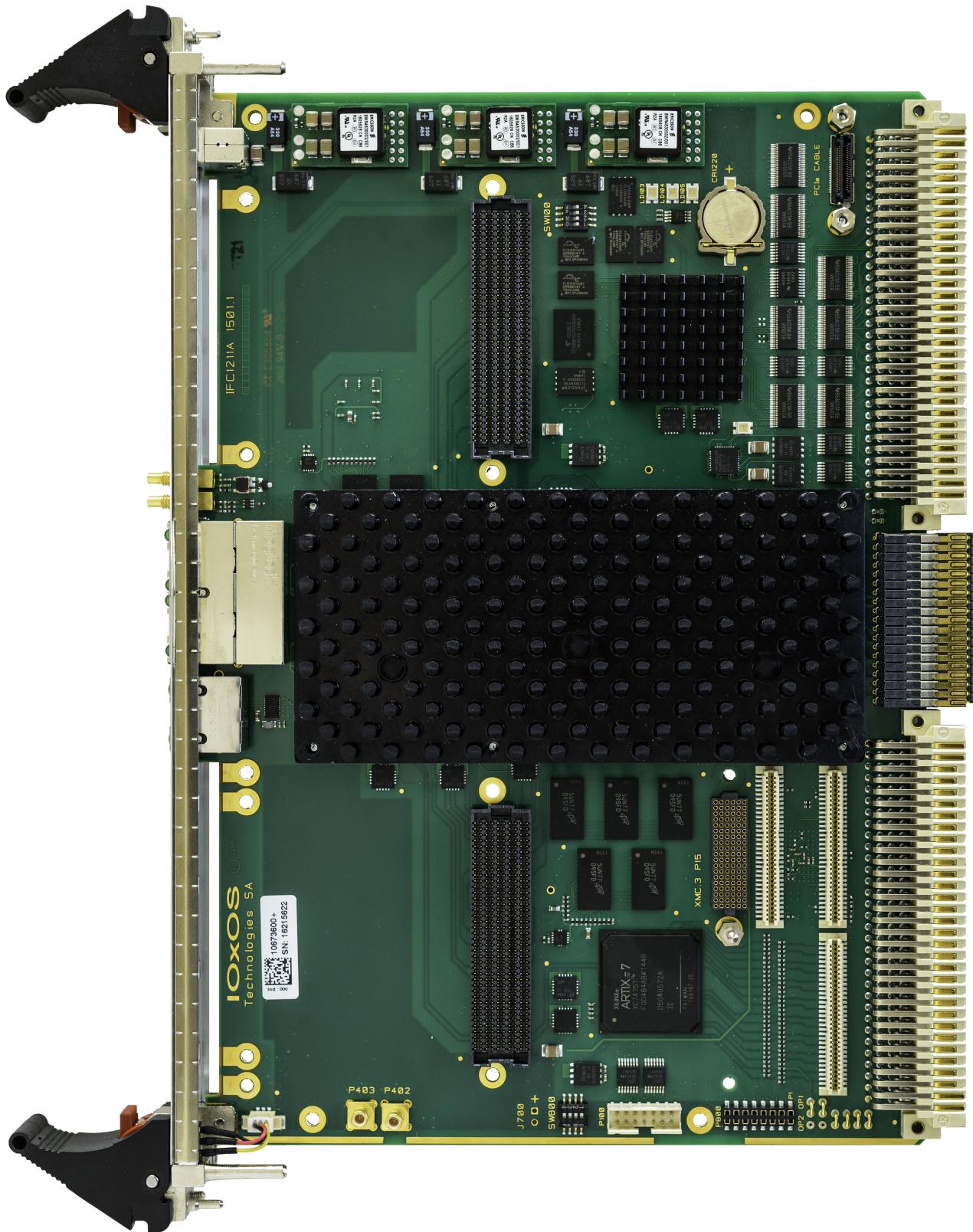
Following section describes the IFC_1211 hardware implementation.

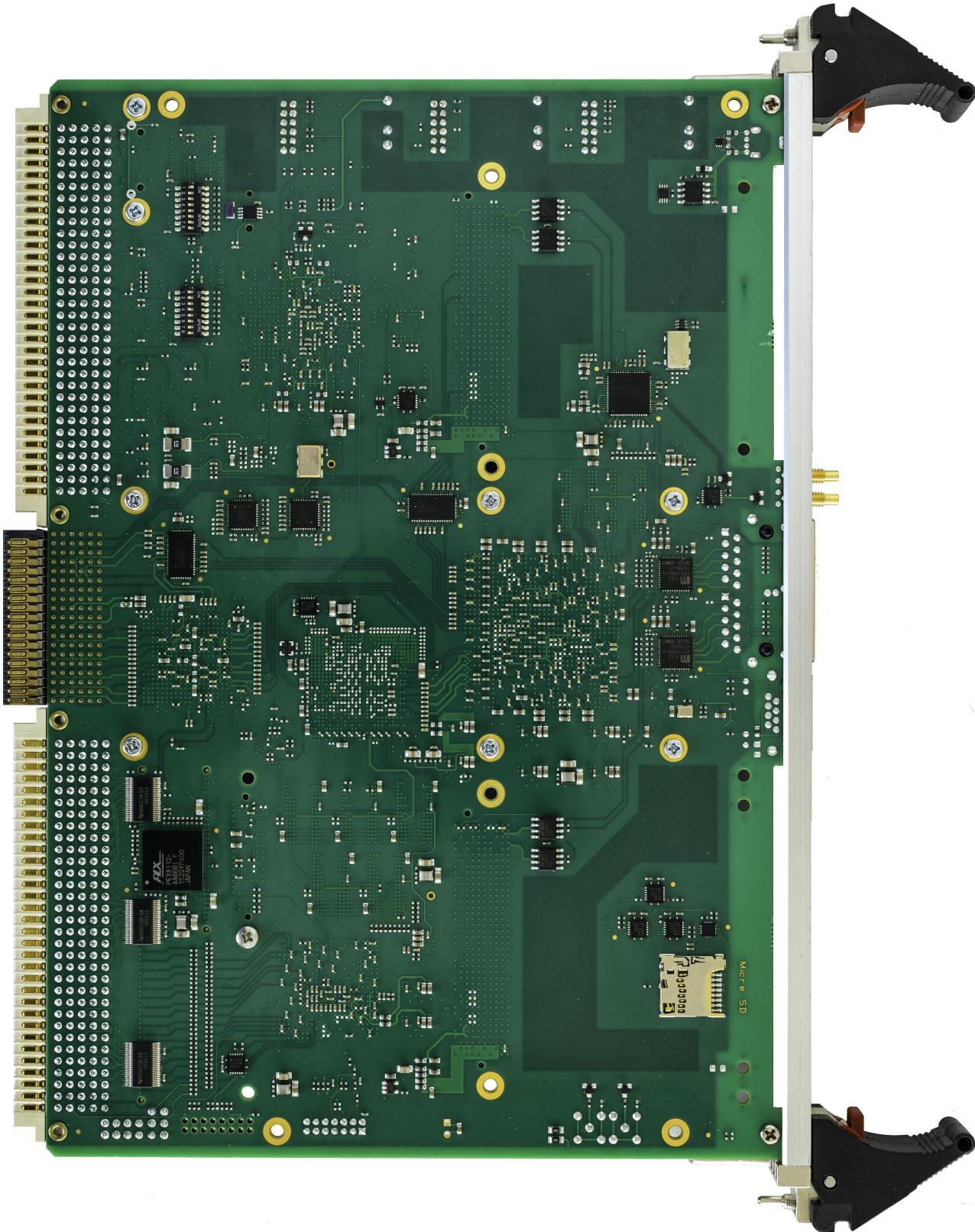
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2.1 Block Diagram

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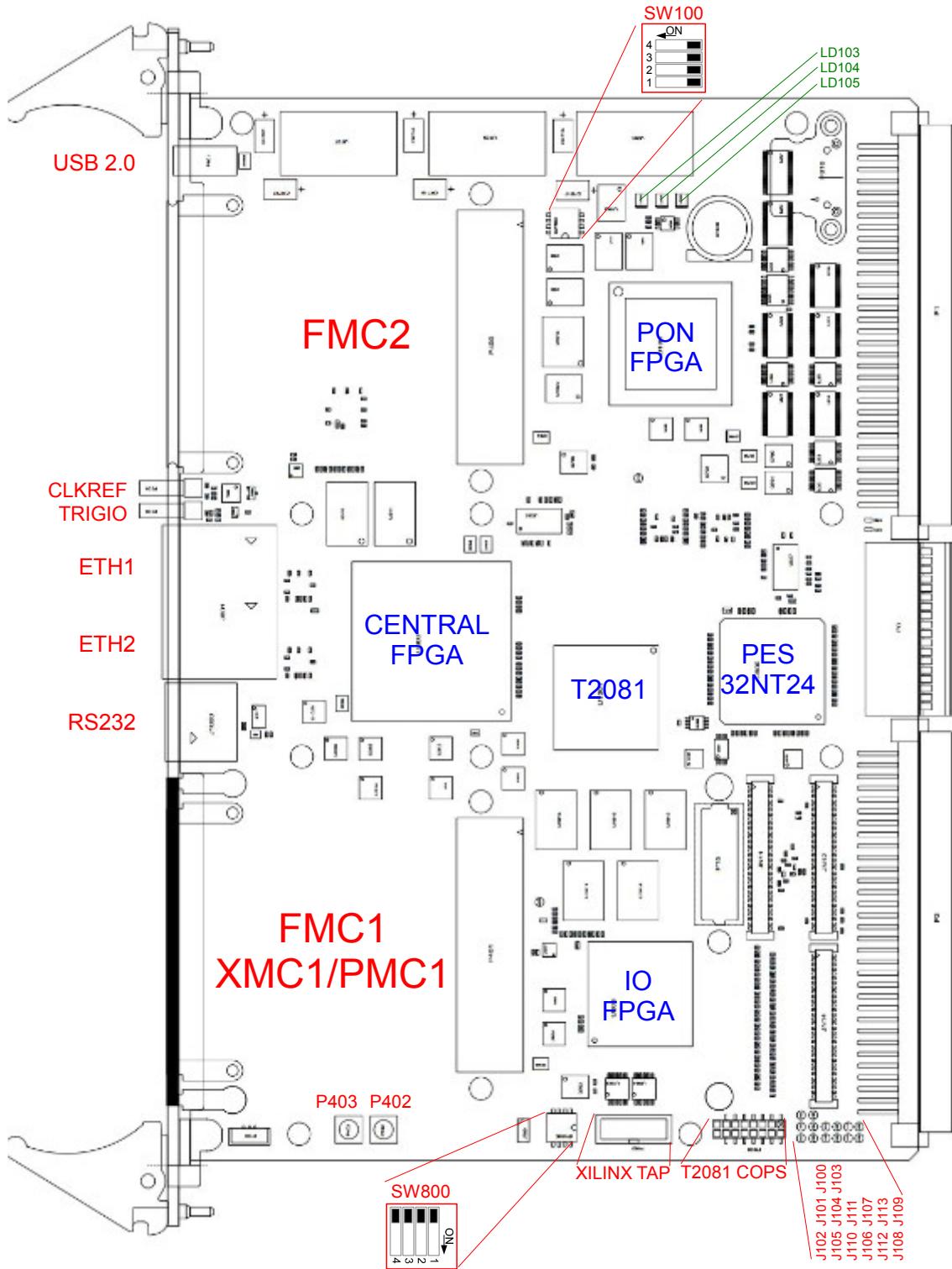


2.1.1 IFC_1211 Bottom PCB side



Illustration 1 : IFC_1211 IFC PCB bottom side equipment

2.1.2 IFC_1211 Top side



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2.2 General Resources

2.2.1 STATIC Options

The IFC_1210 provides following on-board user configurable static options :

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- SW100 Mini-DIP switch 4 pos. Power-up IFC_1211 mode
- SW101 Mini-DIP switch 8 pos. ALTHEA CRCCSR mapping in A24 Address space
- SW102 Mini-DIP switch 8 pos. ALTHEA PCIe-VME64x Bridge general options
- SW800 Mini-DIP switch 4 pos. IO_FPGA user option.
- J100-J113 2.54 jumpers. VME_P2 Rear-IO power supplies

120

2.2.1.1 IFC_1211 Power-up/BOOT Static Option

SW100 Mini-DIP switch 4 positions select the IFC_1211 power-up mode.

SW100	IFC_1211 Option	Functions	Notes / Comments								
SW100-2:1	T2081_BOOTSRC[1:0]	T2081 BOOT Source <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20px; text-align: center;">00</td><td>T2081 Boot from NOR#0 RCW in NOR#0 0x00'0000-0x00'003F</td></tr> <tr> <td style="text-align: center;">01</td><td>T2081 Boot from NOR#1 RCW in NOR#1 0x00'0100-0x00'013F</td></tr> <tr> <td style="text-align: center;">10</td><td>T2081 Boot from attached SPI 29FL129 RCW in NOR#0 0x00'0200-0x00'023F</td></tr> <tr> <td style="text-align: center;">11</td><td>T2081 Boot from SD card RCW in NOR#0 0x00'0300-0x00'033F</td></tr> </table>	00	T2081 Boot from NOR#0 RCW in NOR#0 0x00'0000-0x00'003F	01	T2081 Boot from NOR#1 RCW in NOR#1 0x00'0100-0x00'013F	10	T2081 Boot from attached SPI 29FL129 RCW in NOR#0 0x00'0200-0x00'023F	11	T2081 Boot from SD card RCW in NOR#0 0x00'0300-0x00'033F	
00	T2081 Boot from NOR#0 RCW in NOR#0 0x00'0000-0x00'003F										
01	T2081 Boot from NOR#1 RCW in NOR#1 0x00'0100-0x00'013F										
10	T2081 Boot from attached SPI 29FL129 RCW in NOR#0 0x00'0200-0x00'023F										
11	T2081 Boot from SD card RCW in NOR#0 0x00'0300-0x00'033F										
SW100-3	CENTRAL/IO_CFG	CENTRAL/IO_FPGA configuration mode <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20px; text-align: center;">0</td><td>CENTRAL/IO_FPGAs are configured autonomously at power-up from SPI Flash EPROM device #4/#5</td></tr> <tr> <td style="text-align: center;">1</td><td>CENTRAL/IO_FPGA are configured under control of the T2081 through control registers "IFCBus_FPGA_CFGCTL" + "IFCBus_FPGA_CFGDAT"</td></tr> </table>	0	CENTRAL/IO_FPGAs are configured autonomously at power-up from SPI Flash EPROM device #4/#5	1	CENTRAL/IO_FPGA are configured under control of the T2081 through control registers "IFCBus_FPGA_CFGCTL" + "IFCBus_FPGA_CFGDAT"					
0	CENTRAL/IO_FPGAs are configured autonomously at power-up from SPI Flash EPROM device #4/#5										
1	CENTRAL/IO_FPGA are configured under control of the T2081 through control registers "IFCBus_FPGA_CFGCTL" + "IFCBus_FPGA_CFGDAT"										
SW100-4	T2081_FRST	Force T2081 to stay in RESET state at power-up. Allows T2081 RESET sequence controlled remotely from VME slave VME64x CRCCSR.									

Table 2.1 : IFC_1211 SW100 IFC-1211 Power-up/BOOT options

125

2.2.1.2 ALTHEA VME Bridge Static Option

IFC_1211 integrates in the PON_FPGA the ALTHEA PCIe-VME64x Bridge. This embedded macro function is controlled by static options defined by two Mini-DIP switch 8 positions. For complete description of IFC_1211 ALTHEA implementation, Refer to "IFC1211_ALTHEA_UG".

SW101	ALTHEA Option	Functions	Notes / Comments
SW101-8:1	CRCRSR_A24_MAP[23:16]	CRCRSR_A24 64K window offset mapping. Used while VME64x Mode is not used	

Table 2.2 : IFC_1211 SW101 ALTHEA CRCRSR A24 Mapping options

130

While ALTHEA operates in VME64X Mode, SW101 Mini DIP switch is re-affected to general purpose IFC_1211.

SW101	ALTHEA Option	Functions	Notes / Comments								
SW101-2:1	FPGA_Config[1:0]	These two static options selects the CENTRAL_FPGA and IO_FPGA bit-stream number used by default at power-up. <table border="1" data-bbox="769 797 1198 954"> <tr><td>00</td><td>Back-up bit-stream,</td></tr> <tr><td>01</td><td>1st FPGA bit-stream</td></tr> <tr><td>10</td><td>2nd FPGA bit-stream</td></tr> <tr><td>11</td><td>3rd FPGA bit-stream</td></tr> </table>	00	Back-up bit-stream,	01	1 st FPGA bit-stream	10	2 nd FPGA bit-stream	11	3 rd FPGA bit-stream	If VME64X is not enabled, FPGA_Config[1:0] is fixed to "00".
00	Back-up bit-stream,										
01	1 st FPGA bit-stream										
10	2 nd FPGA bit-stream										
11	3 rd FPGA bit-stream										
SW101-3	PES32NT24_INIT	This static option select the PES32NT24AG2 Initialisation mode. <table border="1" data-bbox="753 1066 1198 1246"> <tr><td>0</td><td>PES32NT24AG2 is initialized from its SMBus Slave Port, controlled from PON_FPGA FSM.</td></tr> <tr><td>1</td><td>PES32NT24AG2 is initialized through its SMBus Master interface from U801 M24256 attached EEPROM.</td></tr> </table>	0	PES32NT24AG2 is initialized from its SMBus Slave Port, controlled from PON_FPGA FSM.	1	PES32NT24AG2 is initialized through its SMBus Master interface from U801 M24256 attached EEPROM.	If VME64X is not enabled, PES32NT24AG2_INIT is fixed to '0'.				
0	PES32NT24AG2 is initialized from its SMBus Slave Port, controlled from PON_FPGA FSM.										
1	PES32NT24AG2 is initialized through its SMBus Master interface from U801 M24256 attached EEPROM.										
SW101-5:4	PES32NT24_IMG	These two static options selects the 32NT24 Port allocation while SW101-3 is positioned to '0'(OFF) → 32NT24 initialized by PON_FPGA FSM <table border="1" data-bbox="769 1403 1198 1583"> <tr><td>00</td><td>Port_2 → RC (T2081) Port_12 → Downstream (VME_P0)</td></tr> <tr><td>01</td><td>Port_2 → NTB(T2081) Port_12 → RC (VME_P0)</td></tr> <tr><td>1x</td><td>Reserved</td></tr> </table>	00	Port_2 → RC (T2081) Port_12 → Downstream (VME_P0)	01	Port_2 → NTB(T2081) Port_12 → RC (VME_P0)	1x	Reserved	Refer to § 2.7.2		
00	Port_2 → RC (T2081) Port_12 → Downstream (VME_P0)										
01	Port_2 → NTB(T2081) Port_12 → RC (VME_P0)										
1x	Reserved										
SW101-8:6	Reserved	Not used									

Table 2.3 : IFC_1211 SW101 Alternate options while VME64X Mode enabled

SW102	ALTHEA Option	Functions	Notes / Comments				
SW102-2:1	VME_SYSCONMOD[1:0]	This 2-bit field defines the VME System Controller activation mode <table border="1" data-bbox="769 1920 1158 2010"> <tr><td>00</td><td>Disabled</td></tr> <tr><td>10</td><td>Enabled</td></tr> </table>	00	Disabled	10	Enabled	
00	Disabled						
10	Enabled						

		<table border="1"> <tr> <td>01</td><td>64X mode. Enabled while GA = "00001" (VME64X Slot-1)</td></tr> <tr> <td>11</td><td>Enabled while BGIN#3 is detected low at power-up. Refer to VME Specification chapter 5.8</td></tr> </table>	01	64X mode. Enabled while GA = "00001" (VME64X Slot-1)	11	Enabled while BGIN#3 is detected low at power-up. Refer to VME Specification chapter 5.8	
01	64X mode. Enabled while GA = "00001" (VME64X Slot-1)						
11	Enabled while BGIN#3 is detected low at power-up. Refer to VME Specification chapter 5.8						
SW102-3	VME64x_SYSRST_ENA	Enable (authorize) VME SYSRESET generation.					
SW102-4	VME64x_AUTOID_ENA	VME Auto Slot Identification logic enable					
SW102-5	PON_FSM_DIS	PON_FSM micro-sequencer Disable					
SW102-6	PERSTVME_ENA	Enable propagation of PCI Express PERSTn assertion to VME SYSRESET#	EP mode				
SW102-7	SPI_WRPROT	SPI Flash EPROM Configuration Write Protect. Also refer to SPI device area definition BP2:BP0 control field.	1K2 to GND pull-done enable the SPI write protection.				
SW102-8	SPI_CFG_ENA	SPI Flash EPROM Configuration area enable.	Warning, must be hardware selected (OPEN / 1K2 to GND)				

Table 2.4 : IFC_1211 SW102 ALTHEA General options

135

Note ALTHEA static options are implemented with pull-down/pull-up polarisation on PON_FPGA internal VME Address/Data Bus. Refer to "IFC1211_ALTHEA_UG" User manual.

140

2.2.1.3 USER Static Option

SW800 Mini-DIP switch 4 positions is reserved for IO_FPGA user specific option.

SW800	Description		Comments
SW800-4:1	user_SWITCH[4:1]	Reserved for user customisation. Supplied to the USER Agent_SW blocks and to the IO_FPGA.	

Table 2.5 : IFC_1211 SW800 USER Static options

2.2.1.4 VME_P2 Rear_IO Power Option

145

J100-J113 2.54 jumpers allows to provide power supplies 3.3[V], +12.0[V], and -12.0[V] on the VME_P2 dedicated pins.

The IFC_1210 implement a collection of 2.54 jumpers to control VME P2 specific usage of User IO. Six of these IO can be used for power supplies and therefore can not be used as generic IO controlled by the "IO" FPGA.

150

Jumpers	Selection	VME_P2	Comments
J100,J101,J102	J100-J101 → IOC31 "IO" FPGA. J102-J101 → VCC12VPOS	C31	User_IO / VCC12VPOS
J103,J104,J105	J103-J105 → IOC31 "IO" FPGA.	A31	User_IO / VCC12VNEG

	J104-J105 → VCC12VNEG		
J107,J10	J107-J106 → VCC3V3	C28	User_IO / VCC3V3
J109,J108	J109-J108 → VCC3V3	C30	User_IO / VCC3V3
J111,J110	J111-J110 → VCC3V3	D28	User_IO / VCC3V3
J113,J110	J113-J112 → VCC3V3	D30	User_IO / VCC3V3

Table 2.6 : IFC_1211 VME_P2 Power supplies 2.54 J100..J113 options

2.2.2 LED Visual Indicators

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The IFC_1211 incorporates eight(8) general purpose Bi-colour LED indicators. Additionnaly the front panel RJ45 connectors (Ethernet + RS232) also provide two LED indicator with each connector. Refer § 2.2.3.1 , 2.2.3.2

160

2.2.2.1 Front Panel LED Visual Indicators

Five(5) Bi-colour LEDs are implemented on the VME front panel directly attached to the PON_FPGA and CENTRAL_FPGA.

LED#	Color	Information	Comments
LED_401 “FMC1”	Green	CENTRAL_FPGA controlled	“CENTRAL” FPGA FMC_1 User function defined.
	Amber	CENTRAL_FPGA controlled	
	Red	CENTRAL_FPGA controlled	
LED_102 “VME”	Green	TOSCA II VME Slave access	Stretched 0.3 [s]
	Amber	TOSCA II VME Master access	Stretched 0.3 [s]
	Red	TOSCA II VME Error detected (BERR)	Stretched 0.3 [s]
LED_101 “S1”	Green	TOSCA II VME Slot_1 Enable	IFC_1211 incorporates a complete VME Slot_1 function.
LED_400 “CENTRAL”	Green	CENTRAL_FPGA OK	CENTRAL_FPGA Operation status
	Amber	CENTRAL_FPGA TBD	
	Red	CENTRAL_FPGA ERROR	
LED_402 “FMC2”	Green	CENTRAL_FPGA controlled	CENTRAL_FPGA FMC_2 User function defined.
	Amber	CENTRAL_FPGA controlled	
	Red	CENTRAL_FPGA controlled	

Table 2.7 : IFC_1211 Front Panel LED

2.2.2.2 On-board LED Visual Indicators

Three(3) Bi-colour LEDs are implemented directly on the IFC_1211 PCB top side, providing general status informations. These LED indicators are not visible from the VME front panel.



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Preliminary

LED#	Color	Information	Comments
LED_103	Green	PON_FPGA controlled LED	USER available LED. Can be controlled directly from the PON_FPGA (pad_loc_LED103Rn, pad_loc_LED103Gn)
	Amber	PON_FPGA controlled LED	
	Red	PON_FPGA controlled LED	
LED_104	Green	"IO" & CENTRAL_FPGA configured OK	OK Configured with selected bit-stream number (#0, #1, #2 or #3)
	Amber	"IO" & CENTRAL_FPGA configured with back-up bit-streams	WARNING, the configured with back-up stream #0
	Red	"IO" & CENTRAL_FPGA configuration FAIL	ERROR, FPGA are not configured
LED_105	Green	PON_FPGA Configured	Light-on while the ARTIX-7 PON_FPGA is auto-configured at power-up from the dedicated SPI Flash EPROM.

Table 2.8 : IFC_1211 On board top PCB side LED

165

2.2.3 Front Panel IO Interface

2.2.3.1 RS232C

The IFC_1211 provides one console port RS232C on front panel RJ45. This RJ45 dedicated to the RS232 interface integrates two LED indicators (Green and Yellow).

170

These two LEDs are controlled by the PON_FPGA and provides RESET_FSM status informations as follow :

LED#		Information	Comments
GREEN	OFF	Power OFF	Provides IFC_1211 RESET FSM status informations.
	Pulsed	Cold_RESET active	
	Toggle FAST	PCIe SWITCH Configured	Allow to track T2081 + FPGA Configuration process. This LED is controlled directly from the „PON“ FPGA (pad_LED_RJ232_Gn)
	Toggle SLOW	T2081 Running	
	ON	READY, In Operation	
YELLOW	OFF	In Operation	Power-up RESET FSM is active
	ON	RESET State	Power-up RESET FSM is in IDLE state

Table 2.9 : IFC_1211 Front Panel RJ45 LED

2.2.3.2 Ethernet 10/100/1000 BaseT RJ45

175

The IFC_1211 provides two standard Ethernet 10/100/1000 BaseT RJ45 with dual combo J801 Belfuse 0875-1G2T-E3. The embedded magnetics are interfaced to two(2) PHY MICREL KSZ9031RNX .

The two(2) Ethernet RJ45 COMBO incorporate two(2) LED providing operation status on the Ethernet 10/100/1000 Base-T port. (Tx / Rx / Linked)

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These four LED indicators are directly controlled by the Ethernet PHY KSZ9031RNX (U1026, U1028)

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2.2.3.3 SSMC “CLREF” Clock INPUT

The IFC_1211 provides one P305 SSMC front panel connector to receive an external clock reference to CLKin_0 of the Dual PLL programmable clock synthesizer LMK04803. Refer to § 2.8.2

This input clock reference is terminated with 50 ohms impedance and is AC coupled through a TC1-1-13MX+ balun, providing single-ended to differential conversion. A dual schottky bridge U300/U301 HSMS-281C provides voltage clamping.

190

Note The SSMC clock INPUT accept analogue SIN signalling

195

2.2.3.4 SSMC “TRIGIO” Trigger IO

The IFC_1211 provides one P304 SSMC front panel connector directly wired to a LVTTL driver/receiver level translator SN74AVC4T245RGYR. The back-end (SSMC_TRIG_IN, SSMC_TRIG_OUT, SSMC_TRIG_OE) is 1.5[V] level and directly interfaced to the CENTRAL_FPGA.

Additional, a 50 ohms termination can be activated from the CENTRAL_FPGA with a dedicated



signal (SSMC_TRIGGER_TERM) .

200

Note *The level translator provides over-voltage protection for the CENTRAL_FPGA IO.*

2.2.4 Front Panel RESET

205

The IFC_1211 uses the "Ergonomic IEEE Hot-swap Injector/Ejector Handle" (ELMA 81-096) with Micro-switch (ELMA 81-088-1) to implement the front panel RESET action. Action on the switch is interpreted as :

- SHORT action (< 1[s]) Activate only the CPU T2081 HRESET
- LONG action (> 1[s]) Complete "Cold_RESET" (Refer to previous chapter)

The micro-switch denouncing logic and the short/long interpretation is implemented in PON_FPGA.

210

2.2.5 On-board IO Interface

2.2.5.1 SMB Debugging Support (P402, P403)

215 The IFC_1211 provides two SMB connectors (vertical mount) dedicated for FPGA user VHDL code debugging. These connectors are located inside the VME board (close to the front panel) and are not directly available on the VME front panel.

- SMB_1 → CENTRAL_FPGA IO_Bank_66 pin E12
- SMB_2 → CENTRAL_FPGA IO_Bank_44 pin AM25

220 Because these connectors are not dedicated to external connection, no ESD protection nor EMI/RFI practice are implemented. The SMB signal are directly connected to the CENTRAL_FPGA IO_Bank.

Note *The SMB signalling can be configured as INPUT or OUTPUT in the CENTRAL_FPGA.*

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2.2.5.2 TAP Debugging Support

The IFC_1211 provides two(2) JTAG TAP connector located on its PCB top side.

230 • XILINX P100 TAP receptacle connector (2x7 14-pin 2[mm]) is dedicated to XILINX VIVADO tool. It allows to configure all IFC_1211 FPGA and also the PON_FPGA attached SPI Flash EPROM 128Mbit U102 S25FL129P0xNFI00 .

The XILINX TAP daisy-chain devices are assigned as :

1st	PON_FPGA XC7A75T-2-FG(G)676
2nd	CENTRAL_FPGA XCKU040-1-FFVA1156
3rd	IO_FPGA XC7A75T-1-FG(G)484

- 235 • T2081 P800 COPS receptacle connector (2x8 16-pin 2[mm]) is dedicated to NPX CodeWARRIOR.

Note *The T2081 COPS interface requires an external adaptor to fit default connector NPX CodeWARRIOR. (16-pin 2.54[mm])*

240

2.3 Thermal Monitoring

The IFC_1211 integrates one (1) U1000 LM95235, on-board temperature monitoring, connected to a dedicated I2C Bus. It is able to issue an interrupt “TERM_CRITn” on software programmable condition. The LM95235 is also connected to the temperature sensing diode (DXP:Anode – DXN:Cathode) of the NPX T2081 die temperature.

245

LM95235 : I2C Bus_1 Address = 0x4C

Note *The CENTRAL_FPGA System Monitor is able to monitor by itself its die temperature.*

250

2.4 Power Supplies

The IFC_1211 is fully powered from the VME64x backplane standard power supplies. To be protected against internal short circuit, the VME +5[V] and +3.3[V] power are isolated with a LI controller and associated Power MOSFET.

255

VME64x Power	CC Protection	Connected to (after protection)	Comments
+5[V]	MAX5970	PMC Carrier JN11 VCC XMC Carrier P15 VPWR 4x DCDC BMR4630002/001 USB2.0 Power Switch MIC2505 U1023 PEX8112 VDD5 U810	
+3.3[V]	MAX5970	PMC Carrier JN11 V33 XMC Carrier P15 3V3 VME I/F SN74VMEH22501A FMC1/FMC2 Carrier P400, P401 VME_P0 (extra USF0603 2A/63V) LDO + Internal IFC1211 logic	
+12[V]	USF0603 2A/63V	PMC Carrier JN11 12VPOS XMC Carrier P15 12VPOS FMC1/FMC2 Carrier P400, P401	Standard fuse protection. In case of internal short circuit, USF0603 2A/63V broken SMD component shall be replaced
-12[V]	USF0603 2A/63V	PMC Carrier JN11 12VNEG XMC Carrier P15 12VNEG	
+5V_STBY	None	Not used	

Table 2.10.: IFC_1211 VME64x Power Supplies

In addition to the MAX5970 and internal DCDC/LDO monitoring circuitry, a TI TPS 386596L3 is monitoring the key (high current) internal power supplies +5[V] +3.3[V], 0.95[V] (T2081 CPU) and 1.0[V] (CENTRAL FPGA KINTEX-7 Ultrascale) to control the IFC-1211 the power-up sequence

260

Warning IFC_1211 requires VME64x 3.3[V] power supply

2.4.1 Input LI Controller MAX5970

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The IFC_1211 is equipped with one MAX5970 (U702) integrated power controller device monitoring continuous the VME power supplies 3.3[V] and 5.0[V]. To limit voltage drop, latest generation CMOS transistor CSD16570Q5B, with extremely low $R_{DS(ON)}$ MOSFET (< 0.49 milli-ohm) are used on +3.3[V] and +5[V].

270

The MAX5970 (U702) incorporates a I2C remote control interface allowing to monitor all key parameters related to the on-board power supplies (V_{CC} Max/Min I_{CC} Max/Min for both VME power inputs. To support the measurements the MAX5970 integrates a 10-bit ADC .

MAX5970 : I2C Bus_2 Address = 0x60

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The MAX5970 provides following IFC_1211 power management facilities :

- Electronic Circuit Breaker with programmable over-current
- Power supplies dV/dt control
- Under-voltage lockout (UVLO)



280

- Power-Good PG and Power-Fault signalling
- Complete remote monitoring of VIN/VOUT and Current

285

2.4.2 High Current DCDC Controllers BMR463-0002/001

The IFC_1211 is equipped with latest generation high efficiency DCDC converter ERICSSON BMR463, able to supply up to 25[A]. This new DCDC generation provides key features as :

290

- High efficiency, typ. 97.1%
- Configuration and Monitoring via PMBus
- Synchronization & Phase spreading
- Current sharing, Voltage Tracking & Voltage margining
- Input under voltage shut-down
- Over temperature protection
- Output short-circuit & Output over voltage protection
- MTBF >20 Mh

Uxxx	VIN	VOUT	Load	Comments
U704	VCC_5V0	1.0[V]	CENTRAL_FPGA	
U705	VCC_5V0	0.95[V]	T2081	CPU _{CORE} shall be adjustable 0.90VCC_5V0 – 1.05[V]
U707	VCC_5V0	1.5[V] – 1.9[V]	FMC_VADJ	Also power to CENTRAL_FPGA related VCC _{IO} banks.

Table 2.11.: IFC_1211 MBR463 High Current

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These new generation of DCDC provide very high efficiency and integrate a I2C Interface (PMBus) allowing to monitor and control them remotely. Through the PMBus, it is also possible to adjust the Voltate Output level (+ 10% / - 10%).

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BMR465_0V95 : I2C Bus_2 Address = 0x24

BMR465_1V0 : I2C Bus_2 Address = 0x53

BMR465_VADJ : I2C Bus_2 Address = 0x63

305

The three(3) BMR463 (U704, U705, U706, U707) can be synchronized together with programmable de-phasing. The phase set-up can be tuned under SW control for optimal noise distribution.

310

The SYNC pins of the three(3) (optionnaly four(4)) BMR463 (U704, U705, U707) are connected together and can be also controller by the „PON“ FPGA. The control register IFCBus_BMRCTL (Refer to § 3.2.7) allows to set-up the SYNC frequency (320 -> 640[KHz]) or inactive.

315

The SYNC pins of the three(3) BMR463 (U704, U705, U706, U707) are connected together and can be also controller by the „PON“ FPGA. The control register IFCBus_BMRCTL (Refer to § 3.2.7) allows to set-up the SYNC frequency (320 -> 640[KHz]) or inactive.

Note The IFC_1211 implements only three BMR463. (IFC_1210 has four). The middle voltage (1.5[V] → 1.8[V] is built with low current DCDC TPS82085.

315

2.4.3 Low Current DCDC Controllers TPS82085

The IFC_1211 middle voltage requirements are implemented with highly integrated Step-down bulk DCDC TI TPS82085, with optimal physical locations, close to the consumer.

Uxxx	VIN	VOUT	I _{max}	
U706	VCC_3V3	1.35[V]	1500[mA]	T2081 G1VDD, T2081 SSTL_REF
U708	VCC_3V3	1.50[V]	1050[mA]	FPGA_DDR3, DDR3, GETH PHY
U710	VCC_3V3	1.50[V]	1300[mA]	SIO_MGT, PLX8112, T2081 S1VDD
U711	VCC_3V3	1.80[V]	1350[mA]	FPGA_VCCAUX, T2081 COP
U712	VCC_3V3	2.50[V]	2000[mA]	T2081 DVDD, LVDD, PCIe Switch, Clock drivers, VME_P0
U713	VCC_3V3	1.50[V]	2400[mA]	CENTRAL FPGA MGT_R, MGT_L
U716	VCC_3V3	1.80[V]	1600[mA]	FPGA All VCCAUX, T2081 COP, ...

Table 2.12.: IFC_1211 TPS82085 3[A] Current

320

2.4.4 General LDO

The IFC_1211 low voltage low current are implemented with LDO devices..

Uxxx	LDO Device	VIN	VOUT	I _{exp}	
U709	TPS7A7300	VCC_3V3	2.50[V]	130[mA]	GETH PHY, LED, OSC 25MHz
U1029	TPS7A7300	VCC_1V5A	1.2[V]	250[mA]	Ethernet PHY Micrel KSZ9031
U1030	TPS7A7300	VCC_1V5B	1.1[V]	600[mA]	T2081 VCC_S1VDD
U1031	TPS7A7300	VCC_1V8A	1.45[V]	300[mA]	T2081 VCC_X1VDD

Table 2.13.: IFC_1211 TPS7A7300 General LDO

2.4.5 XILINX KINTEX-7 Ultrascale MGT Low Noise LDO

325

The FPGA KINTEX-7 Ultrascale and ARTIX-7 MGTs are powered with dedicated low noise LDO. Additionaly, individual LC filters are located close to the FPGA ball.

The two ARTIX-7 (PON and IO) uses only Quad_216 for PCI Express Gen2 interface. The KINTEX-7 Ultrascale can use potentially the five MGT Quad available.

Uxxx	LDO Device	VIN	VOUT	I _{exp}	MGT powered
U105	TPS7A7300	VCC_1V8A	1.0[V]	300[mA]	XC7A75T PON FPGA MGT Quad_216/Quad_213
U106	TPS7A7300	VCC_1V8A	1.2[V]	250[mA]	XC7A75T PON FPGA MGT Quad_216/Quad_213
U804	TPS7A7300	VCC_1V5B	1.0[V]	150[mA]	XC7A75T IO FPGA MGT Quad_216
U805	TPS7A7300	VCC_1V5B	1.2[V]	125[mA]	XC7A75T IO FPGA MGT Quad_216
U312	TPS7A7300	VCC_1V5C	1.0[V]	450[mA]	XCKU040 CENTRAL MGT Quad_225/Quad_226/Quad_224
U313	TPS7A7300	VCC_1V5C	1.0[V]	375[mA]	XCKU040 CENTRAL MGT Quad_225/Quad_226/Quad_224
U315	TPS7A7300	VCC_1V5C	1.0[V]	300[mA]	XCKU040 CENTRAL MGT Quad_225/Quad_226/Quad_224
U314	TPS7A7300	VCC_1V5C	1.0[V]	350[mA]	XCKU040 CENTRAL MGT Quad_225/Quad_226/Quad_224

Table 2.14.: IFC_1211 TPS7A7300 MGT low noise LDO

330

Note The LDO TI TPS7A7300 are protected against short-circuit and over temperature.

2.4.6 PMC/XMC Carrier Power Supplies

The on-board mixed PMC/XMC carrier mezzanine power supplies are directly connected to VME64x internal power supplies, after the on-board protections (MAX5970, USF0603 2A/63V)

335

2.4.7 VITA57.1 FMC Carrier Power Supplies

The two VITA57.1 FMC slots are powered with standard VME64X power supplies (3.3[V] and +12.0[V]) and from on-board high current BMR463 DCDC (U707) for the VADJ power supply.

340

The VADJ power supplies also the CENTRAL_FPGA HP IO_Bank 44, 45, 47, 64, 66, 67 and 68 interfacing the FMC parallel signalling LA, HA and HB. These interfaces shall be able to operate in differential LVDS and single-ended 1.8[V].

345

The FMC VADJ power supply is gated enable/disable from FMC with a very low R_{DSON} MOSFET (CSD16570Q5B). To achieve lowest R_{DSON} a charge pump device (LTC1981ES5) is used to drive the CMOS gate with a $V_{GS} > 4.5[V]$. The control bits "FMC12_VADJ_ENA" and "FMC12_PG_C2M". Both located in Register IFCBus_FMCXMC_CTL, allows to enable/disable globally VADJ power supply to the two FMC slots. Refer to § 3.2.3.4

The 3P3AUX power supply is dedicated to specific FMC I2C Bus interfaced device as Signature Serial EEPROM and temperature measurement.

FMC VITA57	Protection	Voltage	Imax	Comments
3P3V(x4)	MAX5970	+3.3[V]	3A]	Directly supplied by the VME64x backplane power supply through the Hot-Swap Controller MAX5970 (U702) Power monitoring and short circuit protection.
3P3VAUX	MAX5970	+3.3[V]	1[A]	Hard wired with 3V3
12P0V(x2)	USF0603 2A/63V	+12[V]	1[A]	Directly supplied by the VME64x backplane power supply through the fuse USF0603 2A/63V. Max current can be also limited by the VME64x power supply.
VADJ(x4)	BMR463	1.5[V] – 1.95[V]	5[A]	Power supply built with a DCDC U707 BMR463 (Isolation with a FET switch (Q702, Q703) supporting SW ON/OFF. Voltage level is SW programmable in the U707 BMR463

Table 2.15.: IFC_1211 VITA57.1 FMC Power Supplies

350

Note The VITA57.1 FMC standard does not include negative power supplies. While required, they shall be built locally on the FMC mezzanine.

355

Warning Maximum VADJ voltage is limited to 1.95[V] for CENTRAL FPGA KINTEX-7 Ultrascale HP IO_bank. Refer to XILINX technical documentation.

2.4.8 VME_P2 Rear_IO Power Supplies

To fully support VME64x Rear_IO unit, +3.3[V], +12[V] and -12[V] internal power supplies can optionally be connected directly to VME_P2 connector with installation of dedicated 2.54 jumpers.

360

VME64x Power	Protection	Jumper	VME_P2	Comments	
+3.3[V]	MAX5970	J106-J107 J108-J109 J110-J111 J112-J113	C28 C30 D28 D30	Allows to provide 3.3[V] on VME Rear-IO unit. Nota +5V is directly available on VME_P2	
+12[V]	None	J101-J102	C31	Nota There are no short circuit protection inside the IFC1211 for these two power supplies.	
-12[V]	None	J104-J105	A31		

Table 2.16.: IFC_1211 VME_P2 Extra Power Supplies

2.4.9 VME_P0 Power Supplies

The IFC_1211 provides +3.3[V] and 2.5[V] power supplies on VME_P0 UHM connectors. These power supplies are dedicated to high-speed signal conditioner or simple logic level adapter.

365

IFC_1211 Power	Protection	VME_P0	Comments
+3.3[V]	USF0603 2A/63V	C-9	<i>Even there is no limitation on current availability, VME_P0 load on VME_P0 shall not exceed 200[mA]</i>
+2.5[V]	USF0603 2A/63V	C-11	

Table 2.17.: IFC_1211 VME_P0 Power Supplies

2.5 Power_UP/Cold_RESET Sequence

The IFC_1211 supports two basic Cold_RESET options, selected with the static switch SW100-3 "CENTRAL/IO_CFG"

- Mode_0 : Autonomous CENTRAL/IO_FPGA configuration
- Mode_1 : CENTRAL/IO_FPGA configuration under control of T2081

Following diagram shows the IFC_1210 Cold RESET sequence :

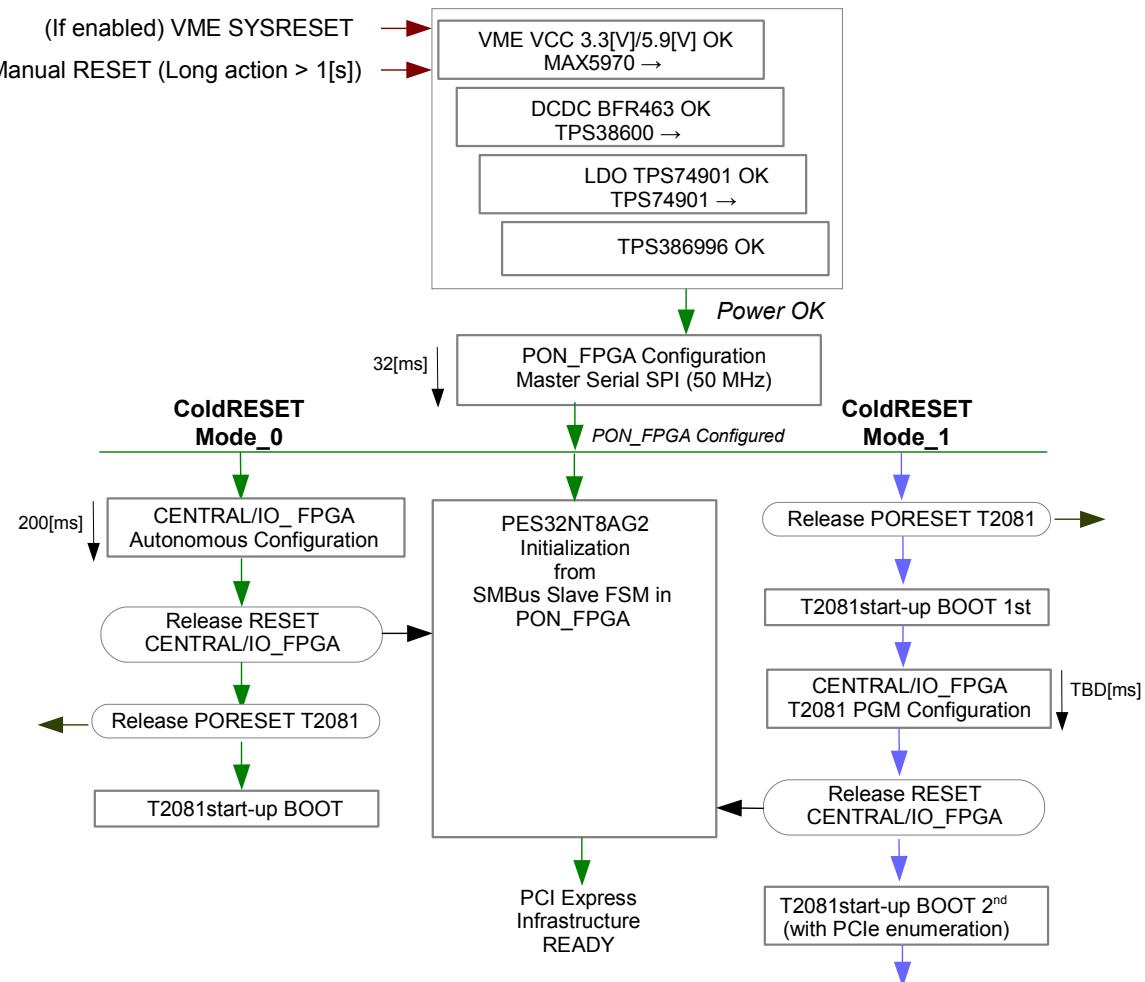


Illustration 3 : IFC_1211 Power_UP/Cold_RESET Sequence

While configured in Mode_0 (SW100-3 = "OFF"), the embedded FSM (located in the PON_FPGA) configures completely the IFC_1210 before releasing the on-board RESET signals.

In Mode_1 (SW100-3 = "ON"), the final on-board hardware configuration is deported to the T2081 microprocessor and shall be integrated in its bootstrap software.

The sequence steps are described below :

- 385 1. Discrete logic monitors on-board power supplies states determining when the IFC_1210 is ready for start-up sequence. Following power sources are monitored through :
- The VME power inputs (+3.3[V] and +5.0[V]) are monitored by the LI Controller MAX5970.
 - The BMR 463 DCDC outputs (1.0[V], 0.95[V] and FMC_VADJ) provides DCDC_power_OK signaling (wired OR open drain)
 - The TPS82085SIL DCDC outputs provides DCDC power_OK signaling (wired OR open drain)
 - The TPS7A7300 LDOs outputs provides LDO power_OK signaling (wired OR open drain)
- 390 2. The "PON_FPGA" is configured autonomously through its Master Serial SPI. The attached SPI Flash EPROM is read-out in Quad-bit mode @ 50 MHz. The PON_FPGA is configured in less than 32[ms]. Refer to § 2.9.4.1
- 395 3. The PCI Express Switch U800 PES32NT24AG2 RESET is released with "SWMODE[3:0]" option hard coded in the PON_FPGA.
- 400 • PES32NT24AG2 Initialization is supplied by the PON_FPGA to its Slave_SMBus interface. Refer to § 2.7.2

At this point the Cold RESET sequence execution can be selected between Mode_0 or Mode_1 with the static option SW100-3.

405 While Mode_0 is enabled (SW100-3 = "OFF") the PON_FPGA embedded logic continues the configuration process as :

- 410 4. The CENTRAL_FPGA and the IO_FPGA are configured under control of two dedicated FSM, extracting the FPGA bit-stream from the SPI Serial Flash EPROM #3 and #4. The two FPGA are configured sequentially
- The IO_FPGA ARTIX XC7A75 is configured in Slave SelectMAP 8-bit Mode @ ~400 Mbit/s. (→ 31[ms]) Refer to § 2.9.4.2
 - The CENTRAL_FPGA KINTEX-7 Ultrascale XCKU040 is configured in Slave SelectMAP 8-bit Mode @ ~400 Mbit/s. (→ 161[ms]) Refer to § 2.9.4.3
- 415 5. The on-board general RESET is released to the IO_FPGA and CENTRAL_FPGA
6. The PORRESET is released to the processor T2081, starting-up its boot code.

420 While Mode_1 is enabled (SW100-3 = "ON") the PORRESET is released to the processor T2081, starting-up its boot code. From this point it is under the responsibility of the T2081 to configure the IO_FPGA and the CENTRAL_FPGA. The programmable configuration resources (control & status) are located in the "IFCBus_FPGA_CFGCTL" and "IFCBus_FPGA_CFGDAT" mapped on the T2081 IFC Bus. Refer to § 3.2.4

- 425 7. The PORESET is released to the processor T2081, starting-up its boot code.
8. The CENTRAL_FPGA and the IO_FPGA are configured under control of the T2081. The CENTRAL/IO_FPGA bit-stream images shall be retrieved from on-board non-volatile memory resources or downloaded from Ethernet/FTP server.
9. The on-board RESET is released to the IO_FPGA and CENTRAL_FPGA
10. The T2081 shall trigger a HRESET to restart its boot sequence. And re-run the PCI Express initial enumeration.

430 **Note** The IFC1211 Power_up/Cold_RESET sequence can also be triggered with the front panel "Ergonomic IEEE Hot-swap Injector/Ejector Handle" (ELMA 81-096) Refer to § 2.2.4



2.5.1 Front Panel RESET

435 The IFC_1211 uses the "Ergonomic IEEE Hot-swap Injector/Ejector Handle" (ELMA 81-096) with Micro-switch (ELMA 81-088-1) to implement the front panel RESET action. Action on the switch is interpreted as :

- SHORT action (< 1[s]) Activate only the CPU T2081 HRESET
- LONG action (> 1[s]) Complete "Cold_RESET" (Refer to previous chapter)

440 The micro-switch denouncing logic and the short/long interpretation is controlled by the PON_FPGA.

2.6 QorIQ T2081 Infrastructure

The IFC_1211 T2081 computing core follows the NPX/Freescale reference design implementation, limiting the SW effort for OS porting. (LINUX and VxWorks)

The T2081 computing core is fully operational without CENTRAL/IO_FPGA configured. This allows to have a fully functional environment under OS, connected on the Ethernet Local Network, with PMC/XMC mezzanine operational. In that case, the CENTRAL/IO_FPGA configuration process can be left under control of the P2020. (.bit/.mcs files downloaded from the Network)

The IFC_1211 central microprocessor QorIQ T2081 is implemented with following configuration options.

- 780 FC-PBGA package, 23 mm x 23 mm, 0.8mm pitch
- 1.8 GHz Low Power version (highest available speed grade)
 - 4 e6500 cores built on Power ArchitectureR technology sharing a 2 MB L2 cache.
 - < 18.4[W] @ T_J 105°, < 12.5[W] @ T_J 65°
- DDR3-3133 operating up to 1066 MHz clock.
- Dual PCI Express Gen2/Gen3 Root Complex (RC) (one support PCIe 2.0 and one support PCIe 3.0)
- IFC Bus 1.8[V] running at 100 MHz, directly connected to PON_FPGA
- Boot Mode selectable with static DIP switch SW100-2:1
 - = "01" → NOR Flash EPROM #0
 - = "01" → NOR Flash EPROM #1
 - = "10" → SPI Flash EPROM S25FL129
 - = "11" → No BOOT (Remote control from VME64x CRCSR)

Note The IFC_1211 is equipped with a large heat-sink covering the T2081, the XCKU040 CENTRAL_FPGA and the PCI Express Switch PES32NT24AG2.

2.6.1 T2081 RESET Management

The T2081 power-up options are controlled under control of the PON_FPGA

- PORESETn, HRESETn controlled by the PON_FPGA
- Reset Configuration Word provided by PON_FPGA
- RCW 64 bytes provided by NOR0 /NOR1

Info Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 4, 5

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2.6.2 COP Debugging Tool

The IFC_1211 provides one P800 2x8 16pins 2[mm] COP compatible with CodeWarrior TAP Kit. The COP signalling is isolated from the T2081 microprocessor with SN74AVC4T245RGYR buffer.

490

Note *To be operational, the PON_FPGA shall be configured to control the T2081 HRESET/TRST*

500

2.6.3 System Memory DDR3

The IFC_1211 T2081 System Memory is built with five(5) DDR3 4Gbit devices organized in 256Mx16 providing 2 GBytes with ECC system memory.

- 2 GBytes with ECC
- 4x DDR3-2133 MT41J256M16HA-093
- 1x DDR3-2133 MT41J256M16HA-093 (only lowest byte used)
- T2081 Highest supported speed grade 1066 MHz

510

Note *Provision made for up coming 8Gbit and 16Gbit DDR3-2133 version.*

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2.6.4 NOR/NAND/ SPI/SD NV Memory Resources

2.6.4.1 NOR Flash EPROM

505

The IFC_1211 provides two emulated asynchronous 64 MBytes NOR Flash EPROM, built from two SPI Flash EPROM S25FL512 devices. A Bridge controller emulates the 16-bit asynchronous Parallel Flash EPROM protocol to full fill the IFC Bus protocol dedicated to the asynchronous NOR device interfacing.

520

The NOR BOOT device (NOR#0 or NOR#1) is selected with SW100-2:1 static option. Refer § 2.2.1.1

The bridge function is integrated in the PON_FPGA, providing VME Slave CRCSR access to the programming register “IFCBus_SPI” of the SPI Flash EPROM devices used for the NOR emulation . Refer § 3.2.5.1

525

Note *Thanks to new high speed SPI Flash EPROM Read protocol, read access time is similar to standard NOR device.*

530

2.6.4.2 NAND Flash EPROM

The IFC_1211 provides one 8-bit wide NAND Flash Memory interfaced on the T2081 Integrated Flash Controller. (IFC Bus)

535

- U1018 4Gbit MT29F4G08 (or equivalent TOSHIBA)
- Upgrade pin compatible path to 8, 16 and 32 Gbit.

Note *The NAND Flash can be (re-)programmed with utilities supplied in U-BOOT.*

Note *The IFC_1211 can be equipped under request with larger NAND Flash device.*



VME64x IFC_1211 HW Technical User Guide

IFC1211_HW_UG_A0

Preliminary

Info Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 13

2.6.4.3 SPI Flash EEPROM

535

The IFC_1211 provides one 128Mb SPI Flash EEPROM U1022 S25FL129P0xNFI00 it attached to the T2081 SPI port. This NV memory can be used as BOOT device while SW100-2:1 = 01.

Note The NAND Flash can be (re-)programmed with utilities supplied in U-BOOT.

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Info Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 15

2.6.4.4 MicroSD Card Holder

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The IFC_1211 provides one J1001 microSD holder (socket), interfaced to the T2081 Enhanced Secured Digital Host Controller (eSDHC) To support 3.3[V] SD/MMC card, 3.3[V]↔1.8[V] level translators SN74AVC4T245RGYR are inserted between the socket and the T2081.

Note This NV memory can not be used as BOOT device.

550

Note With specific PON_FPGA version, dedicated to IFC_1211 bring-up process, an MMC card can be selected for BOOT device.

Info Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 16

2.6.5 USB 2.0 Host Interface

The IFC_1211 implements one Host USB 2.0, directly available from its the front panel.

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- P801 Type A USB 2.0 connector vertical mount (P801)
- U1025 ASDMB-24MHz 50ppm oscillator
- U1023 MIC2505YM USB Power controller

560

Note The T2081 integrates the USB 2.0 PHY.

Info Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 17

2.6.6 10/100/1000 BaseT Ethernet

The IFC_1211 implements two 10/100/1000 Base-T Ethernet available on the front panel.

565

- J801 Belfuse 0875-1G2T-E3 Dual RJ45 with embedded magnetics
- U1026, U1028 MICREL KSZ9031RNX PHY
- U1027 ASE2-25-LC-T 25MHz 50ppm oscillator

ETH Port	MAC Address			Comments
	MAC Address IFC_1211			
	[47:11]	[10:1]	[0]	
ETH0	7C DD 20 01 09	Serial NB	0	IOxOS MAC Address (Front Panel #0)

ETH1	7C DD 20 01 09	Serial NB	1	IOxOS MAC Address (Front Panel #1)
------	----------------	-----------	---	------------------------------------

Table 2.18.: IFC_1211 Ethernet MAC Address assignation

570 **Info** Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 19

2.6.7 RS232 Serial Console

The IFC_1211 implements one RS232C Serial line, available on its front panel

- Electrical IF implemented with U1011 LTC2803 (2.5[V] compatible)
- RS232C available on standard J802 RJ45 (Following PSI pin assignment)

RJ45 pin#	Function
1	Not used (DCD)
2	RTS
3	GNDC
4	TXD
5	RXD
6	GNDC
7	CTS
8	Not used (DTR)

Note The IFC1210 RS232 didnt provides CTS and RTS signalling.

Info Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 18

580

2.6.8 IFC_Bus

The T2081 integrates a general purpose 16-bit parallel bus interface (IFC_Bus) primary dedicated to NAND and NOR non volatile memory boot device. On IFC_1211 the T2081 IFC_Bus is connected to the U800 XC7A75 PON_FPGA and to the NAND Flash U1018 MT29F4G08 (or equivalent).

585

- 1.8V CMOS level interface
- Up to 100 MHz operation
- Selectable protocol for each CS (Chip Select) definition (NOR/NAND/GPCM)

The T2081 can control up to eight(8) IFC_Bus S.. On IFC_1211 only four(4) are used.

590

- CS1 is directly connected to NAND Flash U1018 MT29F4G08
- CS0, CS6 and CS7 connected to PON_FPGA U100 XC7A75

Following table sums up the IFC1211 IFC_Bus assignation with protocol.

CS	Function	Size	IFC_Bus protocol	Description
0	NOR Flash	64 MBytes	Async. 16-bit NOR Flash	The IFC-1211 NOR Flash are bridged to 512Mbit SPI Flash EEPROM with a dedicated FSM embedded in the PON_FPGA emulating the IFC_Bus NOR protocol. The IFC-1211 provides two NOR Flash devices

				selected with SW100-2:1 static option Refer to § 2.6.4.1
1	NAND Flash	TBD	Standard 8-bit NAND	Refer to NPX/Freescale T2081 documentation
6	IFC_CSR	64 KBytes	Normal GPCM with external termination	The IFC_1211 implements specific resources for its operation general control. <ul style="list-style-type: none"> • General Control & Status • 8 Kbytes SRAM Refer to § 3.2
7	VME Direct Path	256 MBytes	Normal GPCM with external termination (Error reported with Bad parity)	The IFC_1211 provides a direct path (low latency) T2081 to VME Master. This direct interconnection provides very fast single beat (low latency) T2081 → VME read access. T2081 → VME write can also be optionally 1-stage posted. The 256 MBytes allocated space is divided in eight(8) 16 MBytes windows with user programmable VME addressing parameters as : <ul style="list-style-type: none"> • High address remapping A[31:24] • VME AM[5:0] Refer to § 2.11.2
Others	Not used		To Be defined	

Table 2.19.: IFC_1211 T2081 IFC_Bus Mapping

595

Info T2081 IFC_Bus is similar to P2020 ELB Bus.

Info Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 13

2.6.8.1 IFC_Bus CS0 NOR Initialization

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The related IFC_Bus CS0 Chip-Select Option register - GPCM (IFC_CSOR0_NOR) fields shall be set as :

- PGRD_EN → '1' : A multi-beat read transaction received from...
- NOR_MODE → "00" : Simple asynchronous NOR (ALE is asserted before CE_B)
- BCTL_D → '0' : BCTL is actively driven by IFC based on direction of access
-

605

2.6.8.2 IFC_Bus CS6 IFC_CSR Initialization

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The related IFC_Bus CS6 Chip-Select Option register - GPCM (IFC_CSOR6_GPCM) fields shall be set as :

- GPMODE → '0' : Normal GPCM operation
- PAR → '0' : Odd Parity
- PAR_EN → '1' : Parity checking enabled over the received data
- GPTO → X"4" : 4096 cycles of IFC module input clocks
- RGETA → '1' : External Read Transfer acknowledge
- WGETA → '1' : External Write Transfer acknowledge
- BURST_LEN → "010" : GPCM burst length = 2 (4 Bytes).

615

Note Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 13.3.7

2.6.8.3 IFC_Bus CS7 VME Direct Path Initialization

The related IFC_Bus CS7 Chip-Select Option register - GPCM (IFC_CSOR_GPCM) fields shall be set as :

- GPMODE → '0' : Normal GPCM operation
- PAR → '0' : Odd Parity
- PAR_EN → '1' : Parity checking enabled over the received data
- GPTO → X"n" : GPCM Timeout Count: For normal GPCM, the timeout occurs only when read data/write data transaction is external transaction acknowledgement based and IFCTA signal has not come. GPTO shall be initialized to cover the VME Master access. (IFC module input clocks = 400 MHz)
- RGETA → '1' : Acknowledgement mode. IFCTA_B acts as acknowledgement / data qualifier signal. GPCM read access is acknowledged by external pin IFCTA_B and only it can complete the read access. If it is not asserted within CSOR[GPTO] time, GPCM_EVTER_STAT[TOER] will be set.
- WGETA → '1' : Acknowledgement mode: GPCM write access is acknowledged/qualified by external pin IFCTA_B assertion. If it is not asserted within CSOR[GPTO] time, GPCM_EVTER_STAT[TOER] will be set
- BURST_LEN → "nnn" : GPCM burst length. It defines the maximum number of beats that will be sent/received in one burst cycle. This is programmed in terms of port-size transfer. For example, if the port size is 2 bytes and burst_length is 2, then the total of 8 bytes will be transferred in one burst cycle (that is, 4 beats of data transfers and each data transfer of 2 bytes).

Note Refer to *QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 13.3.7*

2.6.9 PCI Express Controller

The T2081 integrates up to four(4) PCI Express EP/RC controllers. On IFC_1211 only two of them are used in Root Complex mode. (T2081 SRDS_PRTCL_S1 = 0xAA)

- PCIe4 x4 Gen3 connected to CENTRAL_FPGA XCKU040-1 MGT_227
 - T2081 SerDes EFGH
- PCIe3 x4 Gen2 connected to PCIe Switch PES32NT24AG2 Port_2
 - T2081 SerDes ABCD

Note For specific IFC_1211 application, PCIe3 (connected to the PCIe Switch PES32NT24AG2) could be also configured in EP mode.

Info Refer to *QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 20*

2.6.10 I2C Buses

The T2081 integrates four(4) I2C Module, all connected to the IFC_1211 I2C/SMBus infrastructure. I2C signalling SCL/SDA are connected to 4K7 pull-up at 2.5[V]. Refer § 2.10



Info Refer to QorIQ T2080 Reference Manual, Rev. 2, 02/2016 Chapter 14

665

2.6.11 Real Time Clock

The IFC_1211 implements one Real Time Clock with a local 32.768 Khz crystal. The RTC is interfaced with I2C Bus_1. Refer § 2.10

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- U1008 MAXIM DS1339U-33 +
- Y100 CC7V-T1A 32.768KHz
- BT800 CR1225 battery holder

2.7 PCI Express Gen2 Infrastructure

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The IFC_1211 PCI Express express infrastructure is built around a PCI Express Switch U200 PES32NT24AG2.

The IDT PES32NT24AG2 (U200) is a member of latest PCI Express GEN2 generation, optimized for embedded applications. This new switch generation provides capabilities for real-time and high performance data acquisition system.

PES32NT24AG2 key features

685

- Switching capability of 32 GBytes/s
- Eight Ports PCI Express x4 Gen2/Gen1
- Two adjacent x4 Ports can be merged to form a single PCI Express x8 GEN2/GEN1
- Programmable Tx De-emphasis, Rx Equalization and Tx Drive strength
- Low latency cut-through architecture
- Switch partitioning with dynamic reconfiguration
- Non Transparent Bridge capability available on the eight Ports
- Multicast with up to 64 multicast group
- Dual channel DMA controller with linked list descriptors
- Flexible clocking Mode (CFC Common, CFC Non-common, SSC)
- Hot-Plug on all Downstream Ports

690

The following table sums up the IDT PES32NT24AG2 Ports assignment with its associated capabilities

Port	Link Partner	Size	UP	DWN	NTB	DMA	SSC	Comments
00	PON_FPGA ALTHEA_IFC1211	x4	Y	Y	Y	Y	N	PON_FPGA XC7A075 PCIe-VME64x
02	T2081 PCIe3	x4	N	Y	Y	--	N	The T2081 PCIe3 Gen2 x4 Port shall be defined as RC (Root Complex) or EP (End Point)
04	IO_FPGA	x2	Y	N	N	--	N	IFC_1211 assign one PCI Express interface to the user defined IO_FPGA.
05	PCIe-PCI Bridge PEX8112	x1 (x2)	Y	N	N	--	Y	IFC_1211 legacy PMC PCI 32-bit support. The PEX8112 PCIe to PCI Bridge is assigned to a dedicated PES32NT24 Port
06 07	XMC VITA42.3	x4	Y	Y	Y	--	N	

08	VME P0 UHM Port_A	x4	Y	Y	Y	Y	Y	Standard implementation with Dual PClex4 <ul style="list-style-type: none"> • Can be merged → Single PCIe x8 • Can be splitted → Quad PCIe x2 • Can be splitted → Octal PCIe x1
12	VME P0 UHM Port_B	x4	Y	Y	Y	--	--	
16	PCIe Expansion #1 XMP_1262	x2	Y	N	N	--	--	IFC_1211 provides a PCIe expansion connector SAMTEC LSHM-120-02.5-F-DV-A-S-TR. P810 This connector provides HLCD interfacing to XMP_1262 dual XMC/PMC carrier.
18	PCIe Expansion #2 XMP_1262	x2	Y	N	N	--	--	
20	CENTRAL_FPGA or VME_P0 UHM Port_C	x4	Y	N	Y	--	Y	Standard implementation with Single PClex4 <ul style="list-style-type: none"> • Can be splitted → Quad PCIe x2

Table 2.20 : IFC_1211 PCIe Express Switch PES32NT24AG2 Port Assignment

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2.7.1 PCIe Switch PES32NT24AG2 Clock

The PCI Express Switch U200 PES32NT24AG2 clocking infrastructure is set-up with a modular schema, accommodating several modes of operation :

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- CFC Common clock with link partner
- CFC Non-common clock with link partner
- SSC clock Common with link partner

705

The PES32NT24AG2 clocking operation mode can be selected by Port through following PES32NT24AG2's registers :

- PxxCLKMODE[1:0] {PCLKMODE} = Global or Local Clock Mode
- SCLK {PCIELSTS} = Common/Non-common clock with link partner

Following table sums up the PES32NT24AG2 Port clocking configuration :

PES32NT24AG2	CLK Source	Port	Comments
GCLK0 GCLK1	CLK100REF CLK100REF	PES32NT8AG2	Global Reference clock. 100 MHz +/- 50[ppm]
P00CLK	'0'		Fixed to '0' with Global CLOCK
P02CLK	'0'		
P04CLK	'0'		
P06CLK	XMC1_RxCLK1	XMC#1	Clock source selectable between the on-board CLK100_REF100 MHz +/- 50[ppm] and a clock reference supplied by the XMC1. Selection through P06CLKMODE[1:0]
P08CLK	UHM_RxCLKA	VME P0 UHM Port_B	Clock source selectable between the on-board CLK100_REF100 MHz +/- 50[ppm] and a clock reference supplied by the VME P0 UHM. Selection through P08CLKMODE[1:0] and P12CLKMODE[1:0]
P12CLK	UHM_RxCLKB	VME P0 UHM Port_A	
P16CLK	'0'		Fixed to '0' with Global CLOCK
P20CLK	'0'		Fixed to '0' with Global CLOCK

Table 2.21 : IFC_1211 PCIe Express Switch PES32NT24AG2 Clock Support

710

Note The selection of the external PCI Express clock reference is required while the Link

partner is running with SSC (Spread Spectrum Clocking) mode.

2.7.2 PCIe Switch PES32NT24AG2 Initialization

715

To operate on the IFC_1211 PCI Express defined infrastructure, the PCI Express Switch PES32NT24AG2 requires a specific configuration setting, defined at PERSTn de-assertion. This configuration sequence is defined by :

- Pin strapping (static option)
- SMBus Master port → I2C EEPROM U801 24C256
- SMBus Slave port controlled by a PON_FPGA embedded FSM

720

The PES32NT24AG2 static configuration is based on pin strapping. Value found on these specific pins during PERSTn de-assertion are memorized and used as default options.

725

Several of these initial configured options can also be overridden with the Serial Flash EEPROM (24C256) or from the SMBus Slave port.

Following table sums up the IFC1211 PES32NT24AG2 PIN strapping options.

Signal	Override	IFC_1211 Default Setup	Name & Description						
GCLKFSEL	N	'0'	Global Clock Frequency Select. Fixed to '0' → 100 MHz						
CLKMODE[1:0]	Y	PON_FPGA	Clock Mode Refer to PES32NT24AG2 User's Manual Table 2.4						
RSTHALT	Y	PON_FPGA	Reset Halt Refer to PES32NT24AG2 User's Manual Table 3.2						
SSMBADDR[2:1]	N	"01"	SMBus Slave Address = 0x75						
SWMODE[3:0]	Y	PON_FPGA	Switch Mode Refer to PES32NT24AG2 User's Manual Table 3.8 At Cold_RESET the SWMODE[3:0] is conditioned by SW101-[3] as : <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>SW101-3</th><th>Switch Mode</th></tr> <tr> <td>0</td><td>Single partition with reduced latency</td></tr> <tr> <td>1</td><td>Single partition with Serial EEPROM Initialization with reduced latency</td></tr> </table>	SW101-3	Switch Mode	0	Single partition with reduced latency	1	Single partition with Serial EEPROM Initialization with reduced latency
SW101-3	Switch Mode								
0	Single partition with reduced latency								
1	Single partition with Serial EEPROM Initialization with reduced latency								
STK0CFG[1:0]	Y	"01"	Stack 0 Configuration → Port_0 = PCI Express x4 (PON_FPGA) → Port_2 = PCI Express x4 (T2081)						
STK1CFG[1:0]	Y	"11"	Stack 1 Configuration → Port_4 = PCI Express x2 (IO_FPGA) → Port_5 = PCI Express x2 (PCIe-PCI bridge) → Port_6 = PCI Express x4 (XMC)						
STK2CFG[4:0]	Y	PON_FPGA STK2CFG[4:0] "00001"	Stack 2 Configuration → Port_8 = PCI Express x4 (VME_P0 Port_A) → Port_12 = PCI Express x4 (VME_P0 Port_B) Note Port_8 / Port_12 Alternate configuration set-up can be re-configured to fit application specific.						
STK3CFG[4:0]	Y	PON_FPGA	Stack 3 Configuration (PCIe Expansion + VME_P0 UHM /						

		STK3CFG[3:0] “0110”	CENTRAL_FPGA) → Port_16 = PCI Express x2 (PCIe Expansion #1) → Port_18 = PCI Express x2 (PCIe Expansion #2) → Port_20 = PCI Express x4 (CENTRAL_FPGA) PCI Express x4 (VME_P0 Port_C)	Note Port_20 Alternate configuration set-up can be re-configured to fit application specific.
--	--	------------------------	---	--

Table 2.22 : IFC_1211 PES32NT24AG2 Default Configuration (“Boot Configuration Vector”)

A dedicated FSM, embedded in the PON_FPGA, controls the PCI Express Switch PES32NT24AG2 fundamental cold reset initialization (“Boot Configuration Vector”). This FSM is linked to the T2081 ColdRESET FSM managing the PCI Express RESET generation. Refer to § 2.5

730

- Boot Configuration vector supplied to the PES32NT24AG2 with IFC-1211 default setting
- PCI Express PERSTn management
- Updating internal PES32NT24AG2 option through its SMBus Slave interface.
 - Configure Port_2 (T2081 PCIe3 Gen2) as Downstream port
 - Re-configure Port_8, Port_12 and Port_20 for alternate PCI Express schema.

735

Warning On IFC_1211, The PES32NT24AG2 Port_2, connected to the T2081 PCIe3, SHALL be reconfigured to be the Upstream Port or NT Upstream.

740

Note Refer to PES32NT24AG2 User Manual Chapter 3 for Reset and Initialization process.

The PES32NT24AG2 fundamental cold reset initialization can also be redefined with the use of the U801 M24256-BWDW6TP EEPROM attached to the PES32NT24 SMBus master Interface. This mode of operation is enabled with static option SW101-3 = « ON ». Refer to § 2.2.1

745

While enabled, the EEPROM shall be programmed with adequate initialization sequence as defined in PES32NT24AG2 User Manual Chapter 12 « Master SMBus Interface ».

Note The attached M24256-BWDW6TP EEPROM can be programmed with specific register mapped in the PES32NT24AG2 PCI Express interface.

750

2.7.3 PCIe Switch PES32NT24AG2 Advanced Features

The PCI Express Switch integrates advanced functions for high performance real-time applications.

755

- Embedded DMA controller. Refer to PES32NT24AG2 User Manual Chapter 15
- Non Transparent Bridge. Refer to PES32NT24AG2 User Manual Chapter 14
- Multicast support . Refer to PES32NT24AG2 User Manual Chapter 14

760

The IFC_1211 provides one XMC VITA42.2 Mezzanine carrier slot, directly connected to the on-board PCI Express Switch Port_06 (x2). Only XMC VITA 42.3 P15 connector is provided.

XMC VITA42.3 control and status signalling is provided in IFCBus_XMCFMC register. (XMC15_PRST, XMC15_MVMR0, XMC15_MBIST, XMC15_MBIS). Refer to § 3.2.3.4 .

Warning

While populated, the FMC HPC carrier connectors (Height = 6.5 [mm]) can be in conflict with the XMC Mezzanine mechanical envelope.

765

2.7.5 PMC IEEE1386.1 Mezzanine Slot

The IFC_1211 provides one IEEE1386.1 PMC site (JN11, JN12, JN14) with PCI 32-bit 33/66MHz interface. The PMC site does not supports the VITA32-2003 PrPMC (Processor PMC) signalling.

770

The PMC PCI Interface is built with a PCI Express PCI bridge PLX Technology U810 PEX8112 operating only in FORWARD mode.

775

Warning

While populated, the FMC HPC carrier connectors (Height = 6.5 [mm]) can be in conflict with the PMC Mezzanine mechanical envelope

780

2.7.5.1 PCI Express PCI Bridge PEX8112

The PLX technology PEX8112 is a legacy PCI Express x1 - PCI Bridge following the PCISIG specification. The function is fully transparent for the PCI enumeration.

785

2.7.6 PMC / XMC User's IO JN14

The IEEE1386.1 PMC JN14 provides 64 User IO. These 64 signals are wired to the XILINX ARTIX-7 XC7A75-2-FG484 IO_FPGA and/or VME_P2 rows A and C through a custom configurable twin SMD 0603 0_ohms resistors array allowing to control the interconnect between the PMC/XMC Jn14, the VME_P2 rows A and C and/or the IO_FPGA. An array of 64 dual 0603 footprint is available for custom configuration.

790

Refer to Annexe 4.2 for IFC_1211 physical location of referenced dual footprint.

This XILINX ARTIX-7 XC7A75-2-FG484 IO are LVTTL compatible and tolerant up to 3.6[V]. Refer to § 2.9.2 The IEEE1386.1 PMC JN4 can also be used as User IO for the VITA42.3 XMC#1 Mezzanine.

800

Following drawing shows the PCB foot print layout supporting four(4) equipment option as :

- (a) PMC/XMC Jn14 ↔ VME_P2 rows A and C and FPGA_IO
- (b) PMC/XMC Jn14 ↔ VME_P2 rows A and C only
- (c) PMC/XMC Jn14 ↔ FPGA_IO only
- (d) FPGA_IO ↔ VME_P2 FPGA_IO only

Thu 29 Sep 16 - 11:51 AM

IFC1211_HW_UG_A0

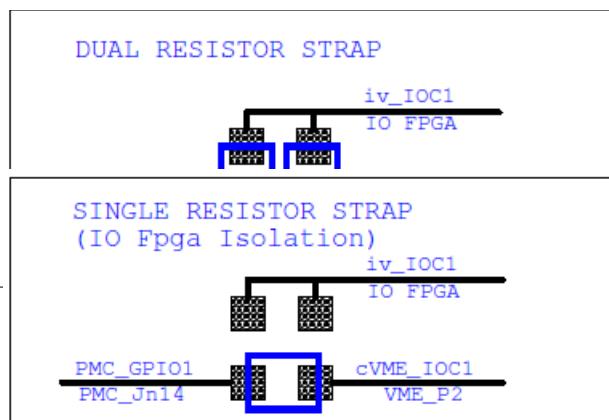


Illustration 4 : IFC_1211 XMC/FMC <-> VME_P2 Customization

The XILINX ARTIX-7 XC7A75-2-FG484 IO_FPGA signalling is LVTTL compatible and tolerant up to 3.6[V]. Refer to § 2.9.2. The IEEE1386.1 PMC JN4 can also be used as User IO for the VITA42.3 XMC#1 Mezzanine.

805 Thanks to direct connection capability (b) between JN14 and VME_P2 rows A and C with IO_FPGA isolated, XMC/PMC Mezzanine with high voltage or analog signal on JN15 can be routed to VME_P2 connectors.

810 **Warning** *The IO_FPGA ARTIX-7 XC7A75T-FG484 signalling is 3.3[V] compatible. So any signal connected across the array shall not exceed V_{INH} level.*

815 **Note** *The 0603 array footprint can also be equipped with capacitors for AC coupling, 50_ohms resistor for serial termination or any resistors value for current limitation.*

Note *By default, IFC_1211 array is equipped with 64x2 0603 0_ohms resistor schema (a).*

2.7.7 VME_P0 UHM PCIe Expansion

820 The VME_P0 UHM connector integrates PCI Express Gen2 interfaces (labelled VME_P0_Port_A, VME_P0_Port_B) connected to the on-board PCI Express Switch PES32NT24AG2.

- PCIe VME_P0_Port_A → PCIe Switch PES32NT24AG2 Port_8
- PCIe VME_P0_Port_B → PCIe Switch PES32NT24AG2 Port_12

These two PCI Express Ports are fully configurable to operate either in Single PCIe_x8, Dual PCIe_x4, Quad PCIe_x2 or Octal PCIe_x1. Refer to § 2.11.4

2.7.8 XMP_1262 PCIe Expansion

830 The IFC_1211 integrates a PCI Express Expansion connector P810 SAMTEC LSHM-120-02.5-F. This high-speed connector provides interconnect to the XMP_1262 through a 15[cm] HLCD mini-coaxial cable, ready up to 10Gb/s.

835 The XMC_1262 is a dual XMC/PMC carrier on a 6U VME64x form factor, with direct dual PCI Express (one in x4 and one in x2) and two SATA II through SAMTEC LSHM-120-02.5-F. Common side-band signalling as PERSTn, WAKEn and SMBus is also embedded in the connection.

- PCIe Expansion #1 → PCIe Switch PES32NT24AG2 Port_16 (x2)
- PCIe Expansion #2 → PCIe Switch PES32NT24AG2 Port_20 (x2)

840 Specific mechanism allows easy VME64X board insertion/de-insertion. (one board at the time)

The P810 SAMTEC LSHM-120-02.5-F connector is assigned as follow :

Signal	Pining	Signal
Thu 29 Sep 16 - 11:51 AM	45/104	IFC1211_HW_UG_A0

PCI Express x2 Gen2 Expansion #1 PES32NT24AG2 Port_16	pcie_exp1_TX0p	1	2	pcie_exp1_RX0p	PCI Express x2 Gen2 Expansion #1 PES32NT24AG2 Port_16
	pcie_exp1_TX0n	3	4	pcie_exp1_RX0n	
	pcie_exp1_TX1p	5	6	pcie_exp1_RX1p	
	pcie_exp1_TX1n	7	8	pcie_exp1_RX1n	
IFC_1211 not used Reserved for PCIe x4	pcie_exp1_TX2p	9	10	pcie_exp1_RX2p	IFC_1211 not used Reserved for PCIe x4
	pcie_exp1_TX2n	11	12	pcie_exp1_RX2n	
	pcie_exp1_TX3p	13	14	pcie_exp1_RX3p	
	pcie_exp1_TX3n	15	16	pcie_exp1_RX3n	
PCI Express x2 Gen2 Expansion #2 PES32NT24AG2 Port_18	pcie_exp2_TX0p	17	18	pcie_exp2_RX0p	PCI Express x2 Gen2 Expansion #2 PES32NT24AG2 Port_18
	pcie_exp2_TX0n	19	20	pcie_exp2_RX0n	
	pcie_exp2_TX1p	21	22	pcie_exp2_RX1p	
	pcie_exp2_TX1n	23	24	pcie_exp2_RX1n	
PCI Express Clock 100MHz Expansion #1-2	exp12_PECLKp	25	26	exp12_PERTSTn	PCI Express RESET
	exp12_PECLKn	27	28	exp12_WAKEn	PCI Express WAKE
SMBus Expansion #1-2 IFC_1211 I2C Bus_4	exp12_SCL	29	30	IOX_Spare0	Reserved Connected to PON_FPGA
	exp12_SDA	31	32	IOX_Spare1	
IFC_1211 not used Reserved for SATA II	exp1_SATA_Tx0p	33	34	exp1_SATA_Rx0p	IFC_1211 not used Reserved for SATA II
	exp1_SATA_Tx0n	35	36	exp1_SATA_Rx0n	
	exp2_SATA_Tx1p	37	38	exp2_SATA_Rx1p	
	exp2_SATA_Tx1n	39	40	exp2_SATA_Rx1n	

Table 2.23 : IFC_1211 PCI Express Expansion SAMTEC LSHM-120-02.5-F.

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Note The IFC_1211 processor T2081 does not provide any SATA II interface.

Note The IFC_1211 PCIe Expansion #1 is PCIe_x2, with provision for PCIe_x4 on further generation.

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2.8 CLOCK Infrastructure

The IFC_1211 clocking infrastructure is based on following main sources :

- Local 100 MHz oscillator, full-filling PCI Express GEN3 jitter specification.
- Programmable clock based on Dual PLL programmable clock synthesizer LMK04803.
- 25 MHz oscillator U1027 ASE2-25-LC-T 25MHz 50ppm dedicated to both Ethernet PHY MICREL KSZ9031RNX.
- 24 MHz oscillator U1025 ASDMB-24MHz 50ppm dedicated to USB 2.0 Host controller.
- 32.768 KHz crystal CC7V-T1A 32.768KHz dedicated to RTC DS1339U-33+.

860

865

2.8.1 PCI Express 100 MHz Clock Distribution

The IFC_1211 100 MHz primary clock reference (labelled REF100A) is built with U320 Crystek CCLD-033-50-100 oscillator with LVDS output. The clock source is buffered with U331 LMK00338 8-output PCIe Gen1/2/3 1 fan out buffer (AC coupled HCSL) to on-board PCIe interfaces :

OUTn	Target Device	Uxxx	Comments
AQ_0	XCKU040	U300	CENTRAL FPGA PCIe Gen3 Quad_GTH MGT 22x
AQ_1	T2081 SD1_CPU	U1001	T2081 SerDes[3:0] PCIe Gen2
AQ_2	T2081 SD2_CPU	U1001	T2081 SerDes[7:4] PCIe Gen3
AQ_3	PCIe Expansion XMP_1262	P810	PCIe Gen2 Expansion connector LSHM-120-02.5-F-DV-A-S-TR
BQ_0	PES32NT24AG2	U800	PCIe Gen2 Switch PCIe 1 st copy
BQ_1	PES32NT24AG2	U800	PCIe Gen2 Switch PCIe 2 nd copy
BQ_2	XC7A75T	U100	PCIe PON_FPGA PCIe Gen2 Quad_GTX MGT 22x
BQ_3	LMK04803	U328	Generic 100 MHz clock input reference for LMK04803
REFCLK	XC7A75T	U100	Single ended 2.5V DC coupled General/EMCCLK source PON_FPGA

Table 2.24.: IFC_1211 PCI Express HSCL/CML AC coupled Clock Distribution

The IFC_1211 100 MHz secondary clock reference (labelled REF100B) is buffered with a 2nd U322 LMK00338 8-output PCIe Gen1/2/3 1 fan out buffer (AC coupled HCSL) with selectable 100 MHz source clock is used to feed following target devices.

Uxxx	Target Device	Uxxx	Comments
AQ_0	XCKU040-MGT225	U300	CENTRAL_FPGA Quad_GTH MGT 22x
AQ_1	XCKU040-MGT226	U300	CENTRAL_FPGA Quad_GTH MGT 22x
AQ_2	VME_P0_A	P0	VME_P0 UHM C12/C13 PCI Express Gen2 Switch 32NT24 connection
AQ_3	VME_P0_B	P0	VME_P0 UHM C12/C13 PCI Express Gen2 Switch 32NT24 connection
BQ_0	XMC P15	P100	XMC VITA42.3 PCIe Gen2
BQ_1	XCKU040	U300	CENTRAL_FPGA general differential 100 MHz
BQ_2	XCA7T75	U803	PCIe IO_FPGA PCIe Gen2 Quad_GTX MGT 22x
BQ_3	PLX8112	U810	PCIe Gen2 → PCI Bridge
REFCLK	XCA75T	U803	Single ended 2.5V DC coupled General source PON_FPGA

Table 2.25.: IFC_1211 PCI Express CML AC coupled Clock Distribution

In normal mode of operation, the clock source shall be selected from U320 Crystek CCLD-033-50-100 oscillator (PGM_CLKSRC = '0'), providing identical clocking reference as the primary clock buffer.

880 Alternatively, the clock source can be selected from a synthesized 100MHz version generated by the LMK04803 (PGM_CLKSRC = '1'). In this case the 100 MHz is built/derived from an external clock reference.

The alternate clock source selection, controlled with "PGM_CLKSRC" control bit located in Register "IFCBus_PGM_RST" Refer § 3.2.6

885 Thanks to on-board PCIe Switch PES32NT24AG2 supporting multi time domain, PCIe devices clocked with the alternate 100 MHz clock are fully supported.

Note If the alternate clock is selected with PGM_CLKSRC = '1', the LMK04803 shall be initialized with CLK_Out7 providing continuous 100 MHz.

890 2.8.2 LMK04803 Programmable Synthesiser

IFC_1211 integrates a programmable Dual PLL programmable clock synthesizer LMK04803. This device can produce low noise, ultra low RMS jitter (< 125[ps]) clock references to on-board IFC_1211 sections. The LMK04803 operates from 1840 to 2030 MHz internal VCO.

The LMK04803 can be programmed to operates from two selected input clock :

- CLKin_0 driven by external AC coupled clock available on the IFC_1211 front panel SSMC connector P304.
- CLKin_1 driven by 100MHz generated with CCLD-033-50-100

900 Thanks to dual PLL implementation, the LMK04803 integrates management of on board VCXO U325 Crystek CVHD-037X-100MHz 20ppm with VCO synchronised to external clock reference provided on "CLOCK_IN" P304 SSMC front panel connector . For optimal noise environment the on-board VCXO can be powered down with control bit "LMK_VCxo_ON". Refer § 3.2.9

905 The LMK04803 is able to generate six(6) dual differential output clock derived from its internal 2000 MHz VCO. Fine tune delay allows adjustement on every output clock.

The LMK04803 owns a uWIRE read/write serial interface controlled through register "IFCBus_LMK04803_CTL" and "IFCBus_LMK04803_DATA". Refer § 3.2.9

910 External LMK04803 direct control and status signalling (LMK_VCxo_ON, LMK_Status_LD, LMK_Status_HOLDVER, LMK_Status_CLKin0, LMK_Status_CLKin1) are available in the "IFCBus_LMK04803_CTL". Refer § 3.2.9

Following table sums up the LMK04803 output clock reference

CLKout	Name	Target Device	Comments
CLKout_0	Not used		
CLKout_1	PGMCLK_MGT226	XCKU040 MGT226 CLK0	VME_P0 Quad GTH
CLKout_2	PGMCLK_MGT228	XCKU040 MGT226 CLK1	FMC1 HS Interface
CLKout_3	Not used		
CLKout_4	PGMCLK_MGT224	XCKU040 MGT226 CLK1	FMC1 HS Interface
CLKout_5	Not used		
CLKout_6	PGM_CLK_CENTRAL	XCKU040	General purpose CENTRAL_FPGA clock reference
CLKout_7	PGM_CLK_REFCLK	LMK00338	Secondary clock reference

CLKout_8	PGMCLK2_FMC1	VITA57.1 FMC Bidirectional CLK2
CLKout_9	PGMCLK2_FMC2	
CLKout_10	PGMCLK3_FMC1	VITA57.1 FMC Bidirectional CLK3
CLKout_11	PGMCLK3_FMC2	

Table 2.26.: IFC_1211 LMK04803 Clock Synthesiser Output

915

Note The LMK04803 in a performance upgrade of the IFC_1210 “Quad frequency Programmable XO” IDT8N4Q001 REV G programmable clock

2.8.3 Others

2.8.3.1 VME SYSCLK

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The 16 MHz VME SYSCLK is generated within the “ALTHEA” section of the PON_FPGA

2.8.3.2 T2081 Clocking set-up

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2.8.3.3 Ethernet PHY clock reference

The two on-board PHY for Ethernet 10/100/1000 BaseT U1026, U1028 KSZ9031RNX are clocked with a dedicated 25 MHz oscillator U1027 ASE2-25-LC-T 25MHz 50ppm.

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2.8.3.4 RTC clock reference

The Real Time Clock Controller U1008 DS1339U-33+ owns a dedicated 32.768 KHz crystal Y001 CC7V-T1A 32.768KHZ.

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2.8.3.5 USB 2.0 Host clock reference

The USB 2.0 Host Controller is clocked with a dedicated 24 MHz oscillator U1025 ASDMB-24MHz 50ppm.

2.9 FPGA Resources

The IFC_1211 is based on three(3) XILINX FPGA devices :

- 940 • PON_FPGA (ARTIX-7 XC7A75T), integrating the power-up sequencer/configurator, the PCIe to VME64x Bridge and T2081 IFC_Bus attached resources attached resources to the T2081.
- 945 • IO_FPGA (ARTIX-7 XC7A75T), integrating user specific VME_P2/PMC J14 interconnect schema.
- CENTRAL_FPGA (KINTEX-7 Ultrascale XCKU040), integrating user specific application controlling the two VITA57.1 FMC.

2.9.1 PON_FPGA

The “ALTHEA-PON” FPGA integrates the PCIe-VME64x Bridge and also IFC1211 dedicated resources directly connected to the T2081 IFC Bus interface. These resources are fully available even while the “CENTRAL” FPGA and the “IO”FPGA are not configured. Moreover they are also available from the VME Slave interface, allowing IFC 1211 be controlled remotely.

This capability allows to leave the IFC_1211 FPGA configuration sequence under control of the T2081. (UBOOT) before loading OS and application.

955 The IFC_1211 PON_FPGA integrates following IOxOS functions as :

- 960 • ALTHEA_IFC1211 T2081 PCIe3 to VME64X Bridge.
- ALTHEA_IFC1211 User_Agent_SW TCSR specific resource. Refer §
- IFC_1211 Power-up/ ColdRESET FSM. Refer § 2.5
- T2081 Power-up sequencer. Refer § 2.6.1
- T2081 Pre-Boot Loader EEPROM emulator. Refer §
- T2081 IFC_Bus Interface Refer § 2.6.8
- T2081 IFC_Bus low latency VME Master direct path. Refer § 2.11.2
- T2081 IFC_Bus local resources as CSR register and SRAM area Refer § 2.6.5
- 965 • IFC_1211 PES32NT24AG2 Initialisation FSM Refer § 2.7.1
- IFC_1211 CENTRAL/IO_FPGA autonomous configuration FSM Refer § 2.9.4.5
- IFC_1211 SPI Flash EPROM controller Refer § 2.9.4.4

970 The PON_FPGA is configured at power-up (only) , directly from its attached SPI Flash EPROM U102 S25FL129P0xNFI00.

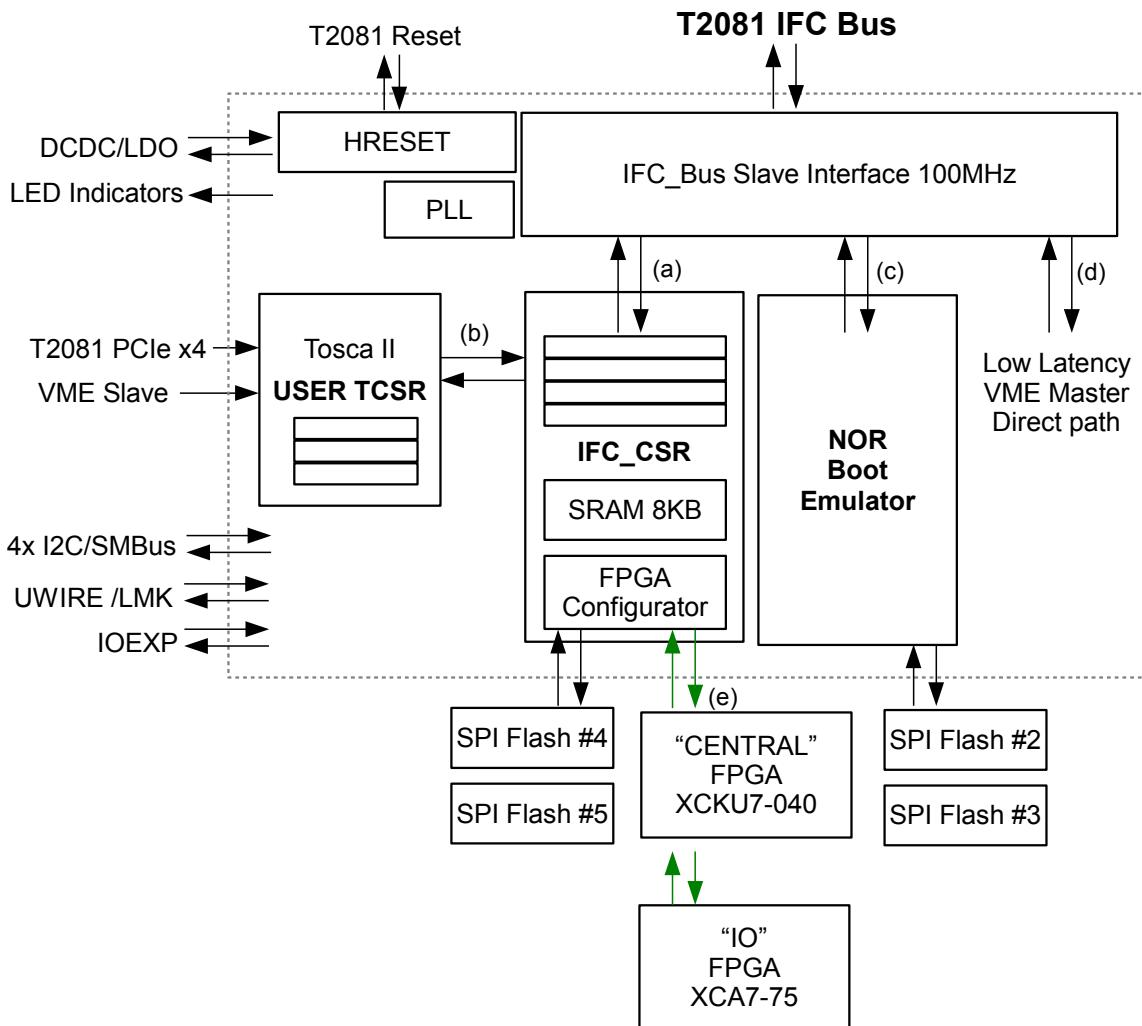


Illustration 5 : IFC_1211 PON_FPGA USER Agent_SW Block Diagram

The T2081 IFC Bus interface operates at maximum allowed speed (100 MHz). Three decoding area are supported as :

- IFC_CSR. This 64 KBytes area map general IFC1211 Control and Status registers, a SRAM general scratch area and the FPGA configuration controller. All are described in following chapters.
- NOR Flash Interface. This 64 MBytes area is directly mapped to either SPI Flash EPROM #2 or #3. The IFC Bus NOR protocol is emulated with a local embedded FSM. Both SPI Flash EPROM can be re-programmed through IFC_SPICTL register.
- VME Master Direct path. This 256 MBytes area is directly connected to the ALTHEA VME Master controller. Thanks to its direct connection, by-passing the PCI Express infrastructure, VME Read is executed with minimal latency.

Note All three areas are supported with GPRM mode.

Note The PON FPGA integrates only IOxOS system core function and is not available for user application.

2.9.1.1 PON_FPGA Quad_MGT Assignation

The IFC_1211 PON_FPGA XILINX XC7A75-2-FG676 owns two(1) Quad_GTP MGT_216/213 operating up to 5.0 Gbit/s. The MGT_216 is dedicated to PCIe IP_core End Point and controlled by a single clock reference CLK0.

MGT	MGT_Clock	Connected to ...	Comments
216	CLK0 → PCIe CLK100	T2081 PCIe3 x4 gen2	
	CLK0 → Not connected		
213	CLK0 → Not connected	Not connected	Reserved for future implementation
	CLK1 → Not connected		

Table 2.27.: IFC_1211 CENTRAL_FPGA MGT Assignation

Note Refer to XILINX 7 Series GTP Transceivers User Guide UG482.

2.9.2 IO_FPGA

The IFC_1211 IO_FPGA U803 ARTIX-7 XC7A75-2-FF484 manages the user IO to/from XMC/PMC JN14 and the VME_P2 rows A, C, D and Z. Refer to § 2.11.4

A bidirectional time multiplexed HSI (High Speed Interface) provides access to/from the user IO to/from the CENTRAL_FPGA. Refer to § 2.9.2.3

Additionally the IO_FPGA is also connected to the IFC_1211 PCI Express infrastructure through the PCI Express Switch PES32NT64AG2 Port_0(PCle x2 Gen2)4 . Refer to § 2.7

The IO_FPGA is fully available for user specific application, and supported with a IOxOS reference design FDK (FPGA Design Kit) including :

- HSI bridging with CENTRAL_FPGA reference design.
- PCI Express EP x2 Gen2 with specific TOSCA II XUSER .

The IO_FPGA can be configured autonomously at power-up from pre-loaded bit-stream stored in SPI Flash EPROM or under control of the T2081 processor. Refer to § 2.9.4.2

Note The IO_FPGA can optionally integrates a full TOSCA IIA infrastructure with SMEM DPRAM controller (without DDR3) and dedicated XUSER Agent_SW handling the VME_P2 and JN14 user IO.

2.9.2.1 IO_FPGA Quad_MGT Assignation

The IFC_1211 IO_FPGA XILINX XC7A75-2-FG484 owns one(1) Quad_GTP MGT_216 operating up to 5.0 Gbit/s. The MGT_216 is dedicated to PCIe IP_core End Point and controlled by a single clock reference CLK0.

MGT	MGT_Clock	Connected to ...	Comments
216	CLK0 → PCIe CLK100	PCIe Switch PES32NT24AG2 Port_04	PCI Express x2 gen2
	CLK1 → Not connected		

Table 2.28.: IFC_1211 IO_FPGA MGT Assignation

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Note Refer to XILINX 7 Series GTP Transceivers User Guide UG482.

2.9.2.2 IO_FPGA IO_Bank Assigntion

The IO_FPGA XILINX U803 ARTIX-7 XC7A75-2-FG488 owns six(6) HR IO_bank assigned as follow :

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IO_Bank	VCC ₀	Signalling	Comments
0	3.3[V]	General ARTIX-7 FPGA support	Configuration control, JTAG, ...
13	3.3[V]	Not used	Not available in XC7A50-2-484
14	3.3[V]	PMC/XMX JN15 - VME_P2 rows A&C IO_FPGA SelectMAP 8-bit Configuration Port	
15	3.3[V]	PMC/XMX JN15 - VME_P2 rows A&C	
16	1.5V	High Speed Interface (HSI) to/from CENTRAL_FPGA	Source synchronous SerDes based @ 800 MHz
34	3.3[V]	PMC/XMX JN15 - VME_P2 rows A&C	
35	3.3[V]	PMC/XMX JN15 - VME_P2 rows A&C Mini DIP switch 4 positions SW800	User option

Table 2.29.: IFC_1211 IO_FPGA IO_Bank Assigntion

2.9.2.3 HSI IO_FPGA ↔ CENTRAL_FPGA Interconnect.

To support direct communication between the CENTRAL_FPGA and VME64x P2 user IO / XMC/PMC JN14, a high-speed interface (HSI) is assigned for this function.

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The HSI interface is defined with following key topics

- 1.5[V] IO_Bank (Support for unipolar and differential signalling)
- Bidirectional Source Synchronous Interface with PLL
- ISERDES2/OSERDES2 on both side (ARTIX-7 and KINTEX-7 Ultrascale)
- IO_FPGA ARTIX-7 XC7A75 IO_Bank_16 without DCI support.
- CENTRAL_FPGA KINTEX-7 Ultrascale IO_BANK_48 with DCI support

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Twenty-two(22) signals are allocated to the HSI interfacem with 1.5[V] single ended anddifferential ended signalling. Both Tx/Rx interface ar built with source synchronous interface built on top of ISERDES2/OSERDES2 macro. Each Rx interface embedds a dedicated PLL to rebuilt local clock alligned to the clock source HSI_V2S_CLK and HSI_S2V_CLK.

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Thanks to time multiplexing logic built on top of ISERDES2/OSERDES2, 64, 128 or 256 bits are forwarded between the two FPGA with update rate at 100, 50 or 25 Mhz within the IFC_1211 100MHz time domain.

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Depending on selected configuration mode with HSI_CFG[1:0] selected, the HSI bridge function transport 64, 128 or 256 bits at every update cycle.

Following table sums up the HSI signal :

Signal Name	CENTRAL_FPGA	IO_FPGA	Function
HSI_CFG[1:0]	OUT	IN	Single ended Remote Configuration selection. This two bit field allows to select the IO_FPGA operating mode.

			<table border="1"> <tr><td>00</td><td>VME_P2 row_A[32:1] + VME_P2 row_C[32:1] Update rate VME_P2 output 50 MHz Update rate VME_P2 input 100 MHz</td></tr> <tr><td>01</td><td>VME_P2 row_A[32:1] + VME_P2 row_C[32:1] + VME_P2 row_D[30:1] + VME_P2 row_Z[16:1] Update rate 25 MHz VME_P2 output 25 MHz Update rate 25 MHz VME_P2 input 50 MHz</td></tr> <tr><td>10</td><td>XMC/PMC JN14[64:1] Update rate JN14 output 50 MHz Update rate JN14 input 100 MHz</td></tr> <tr><td>11</td><td>Reserved for user specific schema.</td></tr> </table>	00	VME_P2 row_A[32:1] + VME_P2 row_C[32:1] Update rate VME_P2 output 50 MHz Update rate VME_P2 input 100 MHz	01	VME_P2 row_A[32:1] + VME_P2 row_C[32:1] + VME_P2 row_D[30:1] + VME_P2 row_Z[16:1] Update rate 25 MHz VME_P2 output 25 MHz Update rate 25 MHz VME_P2 input 50 MHz	10	XMC/PMC JN14[64:1] Update rate JN14 output 50 MHz Update rate JN14 input 100 MHz	11	Reserved for user specific schema.
00	VME_P2 row_A[32:1] + VME_P2 row_C[32:1] Update rate VME_P2 output 50 MHz Update rate VME_P2 input 100 MHz										
01	VME_P2 row_A[32:1] + VME_P2 row_C[32:1] + VME_P2 row_D[30:1] + VME_P2 row_Z[16:1] Update rate 25 MHz VME_P2 output 25 MHz Update rate 25 MHz VME_P2 input 50 MHz										
10	XMC/PMC JN14[64:1] Update rate JN14 output 50 MHz Update rate JN14 input 100 MHz										
11	Reserved for user specific schema.										
HSI_V2S_MODE[1:0]	OUT	IN	Single ended HSI communication synchronisation. <table border="1"> <tr><td>00</td><td>HSI Disable</td></tr> <tr><td>01</td><td>HSI IO_FPGA PLL Enable</td></tr> <tr><td>10</td><td>HSI IO_FPGA + CENTRAL_FPGA PLL Enable</td></tr> <tr><td>11</td><td>HSI Interconnect enable</td></tr> </table>	00	HSI Disable	01	HSI IO_FPGA PLL Enable	10	HSI IO_FPGA + CENTRAL_FPGA PLL Enable	11	HSI Interconnect enable
00	HSI Disable										
01	HSI IO_FPGA PLL Enable										
10	HSI IO_FPGA + CENTRAL_FPGA PLL Enable										
11	HSI Interconnect enable										
HSI_V2S_SPARE1	TBD	TBD	Reserved for user specific application								
HSI_V2S_CLKp HSI_V2S_CLKn	OUT	IN	Differential source synchronous clock CENTRAL_FPGA → IO_FPGA data path.								
HSI_V2S_DAT[7:0]	OUT	IN	Single ended CENTRAL_FPGA → IO_FPGA data path.								
HSI_S2V_CLKp HSI_S2V_CLKn	IN	OUT	Differential source synchronous clock for IO_FPGA → CENTRAL_FPGA data path.								
HSI_S2V_DAT[7:0]	IN	OUT	Single ended IO_FPGA → CENTRAL_FPGA data path.								

Table 2.30 : IFC_1211 IO_FPGA ↔ CENTRAL_FPGA HSI Interface

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Note IFC_1210 was based on bidirectionnal 16-bit data interface. Thanks to higher performance IO interface, the data width has been reduced to 8-bit. IFC_1211 can operates up to 800 MHz

Note Six spare signals “SIO_Spare[5:0]” (3.3[V] signalling) are available for additionnal direct connection between the IO_FPGA and the CENTRAL_FPGA

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Note Default controllers for each FPGA, are supplied in VHDL format, providing full control of the User IO resources on VME64x P2, and PMC/XMC JN14 from the TOSCA III infrastructure located in the CENTRAL_FPGA. These two source files are available in the TOSCA III distribution folder.

- “tosca2_ifc_xuser_P2_IO_ctl_CENTRAL.vhd”
- “tosca2_ifc_xuser_P2_IO_ctl_IO.vhd”

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2.9.3 CENTRAL_FPGA

The IFC_1211 CENTRAL FPGA U300 KINTEX-7 XCKU040-1-FFVA1156 manages primary the two on-board VITA57.1 FMC Mezzanine. Refer to §Error: Reference source not found

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The CENTRAL_FPGA is connected to on-board PCI Express infrastructure with two different (mutually exclusive) schemas :

- T2081 PCIe4 x4 Gen3 (highest performance)
- PES32NT24AG2 x4 Gen2 (legacy compatibility with IFC_1210)

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The CENTRAL_FPGA is fully available for user specific application, and supported with a IOxOS reference design FDK (FPGA Design Kit) based on TOSCA IIA and TOSCA III. The CENTRAL_FPGA FDK includes up to date backward compatible XUSER Example.

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TOSCA IIA is fully compatible with TOSCA II but optimized for XILINX Series 7 FPGA family. It has been used to built ALTHEA PCIe – VME64X Bridge.

TOSCA III is backward compatible with IFC_1210 TOSCA II infrastructure but optimized for new XILINX KINTEX-7 Ultrascale architecture with following improvement :

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- NoC TOSCA III Central Switch 128-bit @ 250 MHz
- Up to three PCI Express EP/RC Agent_SW support.
- Ready for full bandwidth PCI Express Gen3
- SMEM DDR3-2000 controller (4 GBytes/s burst bandwidth)
- SMEM DPRAM controller for internal BRAM area.

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A bidirectional time multiplexed HSI (High Speed Interface) provides access to/from the user IO to/from the CENTRAL_FPGA. Refer to § 2.9.2.3

VME_P0 GPIO are controlled directly from the CENTRAL FPGA with 3.3[V] signalling.

The CENTRAL_FPGA can be configured autonomously at power-up from pre-loaded bit-stream stored in SPI Flash EPROM or under control of the T2081 processor. Refer to § 2.9.4.3

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Note TOSCA III will be used for next generation MicroTCA IFC_1410 unit.

2.9.3.1 CENTRAL_FPGA Quad_MGT Assigntion

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The IFC_1211 CENTRAL_FPGA XILINX XCKU040-1-FFVA1156 owns five(5) Quad_GTH MGT operating up to 11.4 Gbit/s. Each MGT can be controlled by two dedicated clock reference CLK0/CLK1 and/or by clocking schema from adjacent MGT. Refer to XILINX UltraScale Architecture GTH Transceivers User Guide UG576.

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Following table sums-up the IFC_1211 CENTRAL_FPGA XCKU040 Quad_GTH MGT.

MGT	MGT_Clock	Connected to ...	Comments
224	CLK0 → PGMCLK_MGT224 CLK1 → FMC2_GBTCLK0_M2C	VITA57.1 FMC2 Gigabit Interface lane [3:0]	
225	CLK0 → VME_P0_RxCLK CLK1 → FMC2_GBTCLK1_M2C	VME_P0 UHM (C1/C2) or VITA57.1 FMC2 Gigabit Interface lane [7:4]	DS125MB203SQE External 2.1 Mux implemented.
226	CLK0 → PGMCLK_MGT226	VME_P0 UHM (C5/C6)	

	CLK1 → VME_P0_RxCLK	or PCIe Switch PES32NT24AG2 Port_XX	DS125MB203SQE External 2.1 Mux implemented.
227	CLK0 → PCIe CLK100 CLK1 → Not wired	T2081 PCIe4 x4 Gen3	
228	CLK0 → FMC1_GBTCLK0_M2C CLK1 → PGMCLK_MGT228	VITA57.1 FMC1 Gigabit Interface lane [3:0]	

Table 2.31.: IFC_1211 CENTRAL_FPGA MGT Assignation

The XCKU040 embeds three(3) Integrated Block for PCI Express Gen3 with following Quad_GTH MGT physical assignation :

- PCIe Block X0Y0 → MGT224/MGT225
- PCIe Block X0Y1 → MGT226/MGT227
- PCIe Block X0Y2 → MGT228

Note PGMCLK_MGT_xxx clocks are generated with U328 LMK04803. Refer to § 2.8.2

Note All MGT dedicated clock reference CLK0/CLK1 are interfaced with AC coupling.

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2.9.3.2 CENTRAL_FPGA Quad_MGT 2:1 Multiplexer

To extend the MGT_XXX connection flexibility, four(4) DS125MB203SQE PCIe 2-Lane Mux2:1/Repeater 2:1 are used on the MGT_225 and MGT_226. The DS125MB203SQE initialization (equalization, de-emphasis, output level, ...) shall be handled through their respective SMBus Slave interface :

MGT_225 (Lane[1:0] DS125MB203SQE :I2C Bus_2 Address = 0xB0

MGT_225 (Lane[3:2] DS125MB203SQE :I2C Bus_2 Address = 0xB2

MGT_226 (Lane[1:0] DS125MB203SQE :I2C Bus_2 Address = 0xB4

MGT_226 (Lane[3:2] DS125MB203SQE :I2C Bus_2 Address = 0xB6

Following default DS125MB203SQE control signals are fixed by hardware as :

- ENSMB → Fixed to 3.3[V], Enable SMBus Slave interface.
- MODE → Fixed to GND , Normal mode of operation.
- IN_EN → 10K Pull-up (can be overdrive with control bit "mgt22X_MUXSEL")

Programmable DS125MB203SQE control signals (SEL0, PWDN) are controlled through control bit "mgt225_MUXSEL", "mgt225_MUXDWN", "mgt225_MUXSEL", "mgt225_MUXDWN", all located in "IFCBus_DS125MB203". Refer to §Error: Reference source not found

2.9.3.3 CENTRAL_FPGA IO_Bank Assignation

The IO_FPGA XILINX 300 KINTEX-7 Ultrascale XCKU040-1-FFVA1156 owns eight (8) HP IO_bank and two(2) HR IO_Bank assigned as follow :

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IO_Bank	Type	VCC ₀	Signalling	Comments
0	--	3.3[V]	General KINTEX-7 Ultrascale FPGA support	Configuration control, JTAG, ...
44	HP	VADJ	VITA57.1 FMC2_LA,	
45	HP	VADJ	VITA57.1 FMC2_HB + remainder FMC2_LA	
46	HP	1.5[V]	SMEM U310, U311 DDR3 interface	
47	HP	VADJ	VITA57.1 FMC1_HB, FMC2_HB VITA57.1 FMC1_M2CCLK[1:0] VITA57.1 FMC2_M2CCLK[1:0]	
48	HP	1.5V]	SMEM U310, U311 DDR3 interface HSI SerDes Interface to IO_FPGA	
64	HR	VADJ	VITA57.1 FMC2_HA	IO_Bank HR type, some limitation related to DCI unsupported.
65	HR	3.3[V]	General LVDS signalling	SelectMAP 8-bit
66	HP	VADJ	VITA57.1 FMC1_HA	
67	HP	VADJ	VITA57.1 FMC1_LA	
68	HP	VADJ	VITA57.1 FMC1_HB + remainder FMC1_LA	
VADJ is programmable from 1.5[V] to 1.95[V]				

Table 2.32.: IFC_1211 CENTRAL_FPGA IO_Bank Assigntion

Note VITA57.1 FMC LVDS signalling shall be instantiated with SUB_LVDS I/O standard, commonly available on HR and HP IO_Bank.

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Warning CENTRAL_FPGA IO_Bank_64 is HR type, without DCI support.

2.9.4 IFC_1211 FPGA Configuration

The three IFC-1211 on-board FPGA (KINTEX-7 Ultrascale and ARTIX-7) are SRAM based devices requiring configuration at power-up. This configuration process can be handled with :

- Automatically at power-on with bit-stream(s) stored in SPI Flash EPROM
- Under control of XILINX VIVADO tool through the dedicated JTAG TAP
- Under control of the T2081 processor (Only CENTRAL_FPGA and IO_FPGA)

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Through dedicated P100 JTAG TAP connector, the XILINX VIVADO tool can configure (program) all on-board FPGA and also program the SPI#1 Serial Flash EPROM attached to the PON_FPGA (red path) This TAP connection is also used while XILINX VIVADO debugger is used.

The following functional diagram shows the IFC_1211 FPGA configuration sub-system.

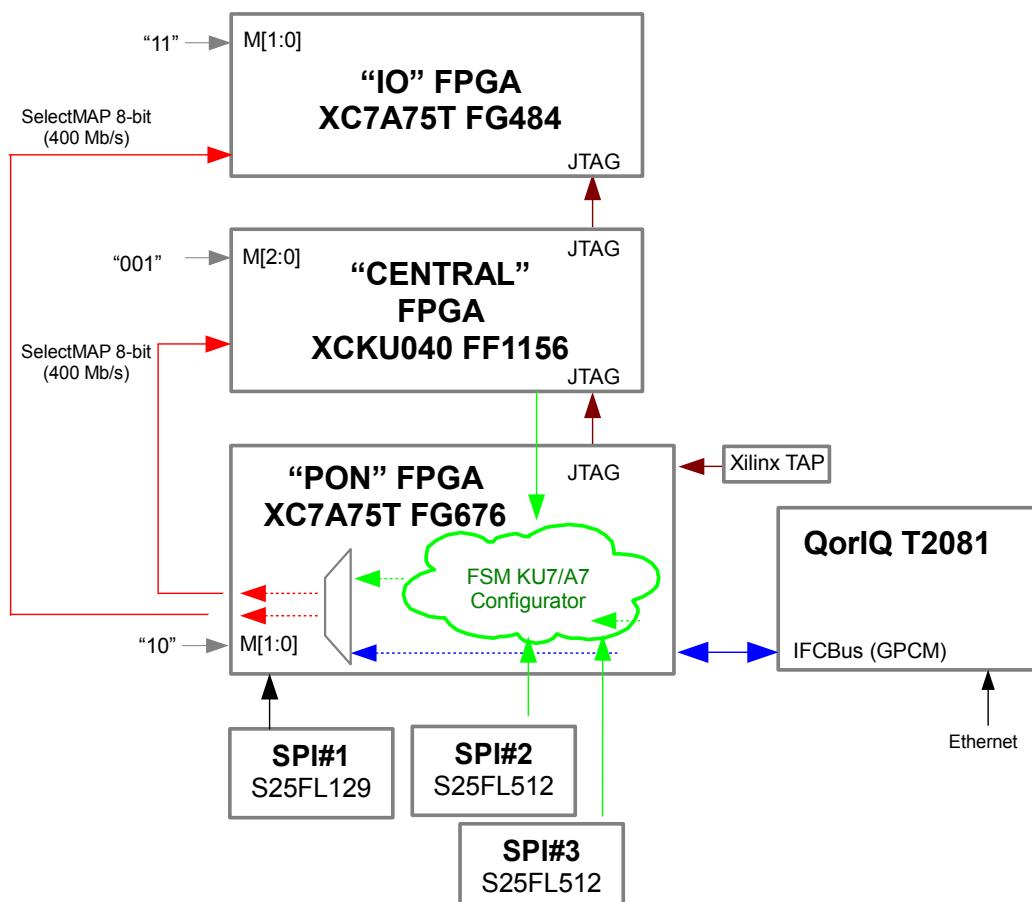


Illustration 6 : IFC_1211 FPGA Configuration Functional Diagram

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The IFC_1211 FPGA Configuration process is conditioned by three(3) static options as

Static	Description		Comments
SW100-3	CENTRAL/IO_CFG	CENTRAL/IO_FPGA configuration mode <input type="checkbox"/> 0 CENTRAL/IO_FPGAs are configured	This static option shall be positioned "ON" while the FPGA are configured with the XILINX VIVADO tool

		<table border="1"> <tr> <td></td><td>autonomously at power-up from SPI FlashEPROM device #4/#5</td></tr> <tr> <td>1</td><td>CENTRAL/IO_FPGAs are configured under control of the T2081 through control registers "IFCBus_FPGA_CFGCTL" + "IFCBus_FPGA_CFGDAT"</td></tr> </table>		autonomously at power-up from SPI FlashEPROM device #4/#5	1	CENTRAL/IO_FPGAs are configured under control of the T2081 through control registers "IFCBus_FPGA_CFGCTL" + "IFCBus_FPGA_CFGDAT"					
	autonomously at power-up from SPI FlashEPROM device #4/#5										
1	CENTRAL/IO_FPGAs are configured under control of the T2081 through control registers "IFCBus_FPGA_CFGCTL" + "IFCBus_FPGA_CFGDAT"										
SW101-2:1	FPGA Config [1:0]	<p>These two static options selects the CENTRAL_FPGA and IO_FPGA bit-stream number used by default at power-up.</p> <table border="1"> <tr> <td>00</td><td>Back-up bit-stream,</td></tr> <tr> <td>01</td><td>1st FPGA bit-stream</td></tr> <tr> <td>10</td><td>2nd FPGA bit-stream</td></tr> <tr> <td>11</td><td>3rd FPGA bit-stream</td></tr> </table>	00	Back-up bit-stream,	01	1 st FPGA bit-stream	10	2 nd FPGA bit-stream	11	3 rd FPGA bit-stream	<p>The bitstream selection is only available when the VME64X mode is enabled with :</p> <p>VME_SYSICONMOD[1:0] = "01" VME_SYSICONMOD[1:0] = "11"</p>
00	Back-up bit-stream,										
01	1 st FPGA bit-stream										
10	2 nd FPGA bit-stream										
11	3 rd FPGA bit-stream										

Table 2.33 : IFC_1211 CENTRAL/IO_FPGA Configuration Static Option

Warning The autonomous FPGA Configuration bit-stream selection is only available while the IFC1211 VME interface CRCSR operates in 64X mode. In this case, SW101 static options are useless and re-affected to additional static option. While VME interface CRCSR does not operate in 64X mode, then FPGA Config [1:0] is fixed to "01".

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Under T2081 control, through its IFCBus, the CENTRAL_FPGA and IO_FPGA can be (re-)configured with two selectable modes :

1. Trigger the "FSM KU7/A7 Configurator" with selectable bit-stream number. In this case the FPGA bit-stream are fetched from the SPI Flash EPROM #4/#5 devices.
2. Load the complete bit-stream images through its IFCBus interface. In this case the bit-streams shall be supplied by the T2081 non-volatile memories (NAND, NOR, microSD) or directly from a FTP server through its Ethernet interface.

The two control registers "IFCBus_FPGA_CFGCTL" and "IFCBus_FPGA_CFGDAT" mapped on the T2081 IFC Bus interface are used to configure the FPGA. Refer to § 3.2.4.1 and § 3.2.4.2

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Note Control registers "IFCBus_FPGA_CFGCTL" and "IFCBus_FPGA_CFGDAT" are also mapped in VME Slave CRCSR Space, providing remote re-programming from VME Bus.

2.9.4.1 PON_FPGA ARTIX-7 Configuration

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The XILINX ARTIX-7 PON_FPGA is an SRAM based FPGA and therefore requires a power-up configuration process. The configuration bit stream is stored in an external 128 Mbit SPI Flash EPROM device :

SPANSION S25FL129P0xNFI00

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This non-volatile device storing the FPGA configuration bit-stream can be programmed through the P100 XILINX tap interface by means of XILINX VIVADO software tool. After initial programming, the SPI Flash EPROM device can also be re-programmed in-situ through a dedicated controller embedded in the ALTHEA_IFC1211.

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The ARTIX-7 FPGA configuration process is operating in "Master SPI x4" mode with external CCLK clock source driven from EECCLK 100 MHz. Multi-Boot operation is fully supported by the SPI Flash EPROM.

The ARTIX-7 FPGA configuration process is triggered by the power monitor circuitry, signalling with low → high on PROGRAMM_B pin. The complete PON_FPGA configuration is handled in less than 150 [ms].

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Refer to ALTHEA_IFC1211_UG chapter 4.2.1 "ALTHEA_IFC1211 ARTIX-7 Configuration

Note *The PON_FPGA is configured only one at power-up. Front panel RESET activation through the "Ergonomic IEEE Hot-swap Injector/Ejector Handle" (ELMA 81-096) do not re-configure the PON_FPGA.*

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2.9.4.2 IO_FPGA ARTIX-7 Configuration

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The IFC_1211 IO_FPGA can be configured either autonomously at power-up or under control of the T2081 processor unit through a SlaveSERIAL serial interface operating at 100 MHz. The IO_FPGA configuration images are stored in SPI#2 and SPI#3 Flash EPROM devices. Refer to § 2.9.4.4

IO_FPGA XC7A75 : bitstream size = 30,606,304 bits Conf_time ~ 310 ms

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Warning *To be correctly interpreted by the embedded FPGA configurator, IO_FPGA bitstream generation with VIVADO tool shall be set-up with option "set_property CONFIG_MODE S_SERIAL [current_design]"*

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2.9.4.3 CENTRAL FPGA KINTEX-7 Ultrascale Configuration

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The IFC_1211 CENTRAL_FPGA can be configured either autonomously at power-up or under control of the T2081 processor unit through a SelectMAP 8-bit parallel interface operating at 100 MHz. The CENTRAL_FPGA configuration images are stored in SPI#2 and SPI#3 Flash EPROM devices. Refer to § 2.9.4.4

CENTRAL_FPGA XCK040 : 128,055,264 bits Conf_time = 161 ms

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Warning *To be correctly interpreted by the embedded FPGA configurator, CENTRAL_FPGA bitstream generation with VIVADO tool shall be set-up with option "set_property CONFIG_MODE S_SELECTMAP [current_design]"*

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2.9.4.4 SPI Flash EEPROM Resources

The IFC_1211 implements five(6) SPI Flash EPROM devices dedicated to T2081 non volatile memory resources and on-board FPGA configuration image storage.

SPI Device	Uxxx	Type	Size	Assignation
SPI#0		S25FL129	128 Mb	SPI Flash directly attached to T2081 SPI interface. This SPI Flash EPROM can be programmed from T2081 SPI interface
SPI#1	U102	S25FL129	128 Mb	PON_FPGA Configuration device. Also used to store signature and other ALTHEA specific non volatile parameter. This SPI Flash EPROM can be programmed through : <ul style="list-style-type: none"> • XILINX TAP port / VIVADO tool • IFC1211_ALTHEA TCSR register "ILOC_SPI" Refer to "IFC1211_ALTHEA_UG" chapter 4.4 and 3.2.5
SPI#2	U108	S25FL512	1024 Mb	These two SPI Flash devices store the CENTRAL_FPGA and IO_FPGA configuration bit-stream for autonomous configuration mode. See next section for bit-stream mapping.
SPI#3	U111	S25FL512		Each device stores a 4-bit nibble forming the Byte for the SelectMAP 8-bit configuration interface

				The two devices can be programmed through "IFCBus_SPI" control register. Refer § 3.2.5.1
SPI#4	U109	S25FL512	512 Mb	This SPI device provides T2081 NOR Flash emulator #0.
SPI#5	U112	S25FL512	512 Mb	This SPI device provides T2081 NOR Flash emulator #1.

Table 2.34 : IFC_1211 SPI Flash EPROM Devices

1240 To operate with optimal CENTRAL/IO_FPGA configuration frequency (100 MHz) , SPI Flash EPROM #2 and #3 are used in parallel, providing each a 4-bit nibble. The FPGA bit-stream image shall be loaded in the two SPI Flash EPROM device.

1245 **Note** Dual SPI Flash EPROM #2/#3 nibble programming is supported by specific IFC_1211 XprsMON command.

Parallel NOR Flash EPROM used for T2081 Boot are emulated with SPI Flash EPROM devices #4 and #5. A specific IFC_Bus bridge function is implemented in the PON_FPGA to convert NOR IFC Bus protocol to SPI Fast Quad Read.

1250 Thanks to specific IFC_1211 architectures, the registers used to program the SPI Flash EPROM #1, #2, #3, #4 and #5 are mapped on the VME64x CRCSR Slave, even if the T2081 is forced in RESET state with SW100-4 T2081_FRST= '1'.

Following table shows the SPI #2/#3 bit-stream mapping allocation :

1255

SPI #2+#3 Byte address	Size	CENTRAL/IO FPGA Bit-stream image
0x000'0000-0x17F'FFFF	192 Mbit	CENTRAL_FPGA Bit-stream #0. (back-up image)
0x180'0000-0x2FF'FFFF	192 Mbit	CENTRAL_FPGA Bit-stream #1.
0x300'0000-0x47F'FFFF	192 Mbit	CENTRAL_FPGA Bit-stream #2.
0x480'0000-0x5FF'FFFF	192 Mbit	CENTRAL_FPGA Bit-stream #3.
0x600'0000-0x6FF'FFFF	128 Mbit	Reserved/Not used
0x700'0000-0x73F'FFFF	16Mbit	IO_FPGA Bit-stream #0. (back-up image)
0x740'0000-0x77F'FFFF	16Mbit	IO_FPGA Bit-stream #1.
0x780'0000-0x7BF'FFFF	16Mbit	IO_FPGA Bit-stream #2.
0x7C0'0000-0x7FF'FFFF	16Mbit	IO_FPGA Bit-stream #3.

1260 **Note** SPI Flash EPROM #2,#5 are provisionned to support CENTRAL_FPGA XCKU060 (192,999,264 bits)

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2.9.4.5 Autonomous FPGA Configurator

The IFC_1211 autonomous FPGA configurator FSM is integrated in the PON_FPGA. If enabled with SW100-2 "CENTRAL/IO_CFG" static option, the CENTRAL_FPGA and IO_FPGA configuration procedure is immediately started with bit-stream number fixed with SW101-2:1 "FPGA Config [1:0]". The bit-stream stored in SPI Flash EPROM #2/#3 are pushed to the FPGA at maximal speed to the SelectMAP 8-bit parallel interface.

In case of configuration error detected with :

1270

- FPGA INITn signal → '1'
- FPGA DONE signal is not → '1' after expected calculated time

the CENTRAL_FPGA and IO_FPGA configuration procedure is restarted with bitstream #0.



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Warning

To be correctly interpreted by the embedded autonomous FPGA configurator, bitstream generation with VIVADO tool shall be set-up with following options

- *IO_FPGA → “set_property CONFIG_MODE S_SERIAL [current_design]”*
- *CENTRAL_FPGA → “set_property CONFIG_MODE S_SELECTMAP [current_design]”*

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2.9.5 FMC VITA57.1 FMC

The IFC_1211 provides two ANSI/VITA57.1-2008(R2010) FMC sites. The FMC IO signals are mainly wired to the CENTRAL_FPGA U300 KINTEX-7 Ultrascale XCKU040-1-FFVA1156 and some side-band signalling to the PON_FPGA U100 ARTIX-7 XC7A75-2-FG676.

The Mezzanine sites (P400, P401) are dedicated for high-speed analog interface (ADC, TDC, DAC). To reduce noise induced by the carrier board, following precaution have been implemented.

- Ferrite serial isolation on power supplies
- Ground plane bellow the two FMC sites.

Moreover, The IFC_1211 FMC carrier, provides a full height (10[mm]) envelope for the installed FMC mezzanines (No components are located on the carrier board bellow the FMC mezzanine). This provides enough available height to equip critical components on the FMC mezzanine with adequate heat-sink.

2.9.5.1 FMC VITA57.1 Power and Side Band Signalling

The IFC_1211 VITA57.1 power supplies are described in related chapter § 2.4.7 .

The IFC_1211 VITA57.1 power side-band signalling are suns-up in following table :

VITA57.1 Signals	Level	Comments
VIO_B_M2C(x2)	User defined	Not used by the IFC_1210 Carrier. The CENTRAL_FPGA related IO_Bank are powered with VADJ.
VREF_A_M2C	User defined	Not used by the IFC_1210 Carrier. The CENTRAL_FPGA related IO_Bank nave fixed single ended VREF.
VREF_B_M2C	User defined	Not used by the IFC_1210 Carrier. The CENTRAL_FPGA related IO_Bank nave fixed single ended VREF.
PG_C2M	LVTTL	Carrier Power Good . Control bit available in the register "IFCBus_FMCXMC_CTL". Refer § 3.2.3.4
PG_M2C	LVTTL	Mezzanine Power Good . Available in U300 CENTRAL_FPGA XCKU040 HR IO_Bank_65.

Table 2.35.: IFC_1211 VITA57.1 FMC Power side-band signalling

The ANSI/VITA57.1 FMC implements a number of side band signaling, controlled/monitored by the IFC_1211 Carrier through the PON_FPGA

The FMC Geographic addressing signals "GA1" & "GA0" are hardwired on the IFC_1211 Carrier as :

- GA1, GA0 = "10" for FMC#2 (P400 Top)
- GA1, GA0 = "01" for FMC#1 (P401 Bottom)

The FMC status informations as "FMC1_PRSTN" and "FMC2_PRSTN" are connected to the PON_FPGA and made available in control register "IFCBus_FMCXMC_CTL". Refer to § 3.2.3.4

2.9.5.2 FMC VITA57.1 CENTRAL FPGA Interfacing

The IFC_1211 VITA57.1 FMC interfacing with CENTRAL_FPGA KINTEX-7 Ultrascale XCKU040 has been optimized for optimal PCB layout.

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Following table sums-up the VITA57.1 FMC to CENTRAL_FPGA KINTEX-7 Ultrascale XCKU040 signalling

FMC signals	CENTRAL_FPGA IO_Bank	IO_Bank Type	Comments
fmc1_LA[23:0] fmc1_LA[33:24]	IO_Bank_67 IO_Bank_68	HP HP	fmc1_LA[0], fmc1_LA[1], fmc1_LA[17], fmc1_LA[18] are wired to XCKU040 GCC inputs.
fmc1_HA[23:0]	IO_Bank_66	HP	fmc1_HA[0], fmc1_HA[1], fmc1_HA[17] are wired to XCKU040 GCC inputs.
fmc1_HB[21:0]	IO_Bank_68 IO_Bank_47	HP	fmc1_HB[0] , fmc1_HB[6], fmc1_HB[17] are wired to XCKU040 GCC inputs. fmc1 HB signalling is distributed over the two IO_Bank_68 and IO_Bank_47.
fmc1_CLK0_M2C	IO_Bank_47	HP	Direct control to XCKU040 MMMCs and PLLs
fmc1_CLK1_M2C	IO_Bank_47	HP	Direct control to XCKU040 MMMCs and PLLs
fmc1_CLK2_M2C	--	--	Source from on-board CLK100 or PGMCLK from LMK04803.
fmc1_CLK3_M2C	--	--	Source from on-board CLK100 or PGMCLK from LMK04803.
fmc1_DBG_SMB	IO_Bank_66	HP	Support for XUSER FMC#2 debugging
<hr/>			
fmc2_LA[23:0] fmc2_LA[33:24]	IO_Bank_44 IO_Bank_45	HP	fmc2_LA[0], fmc2_LA[1], fmc2_LA[17], fmc2_LA[18] are wired to XCKU040 GCC inputs.
fmc2_HA[23:0]	IO_Bank_64	HR	fmc2_HA[0], fmc2_HA[1], fmc2_HA[17] are wired to XCKU040 GCC inputs.
fmc2_HB[21:0]	IO_Bank_45 IO_Bank_47	HP	fmc2_HB[0] , fmc2_HB[6], fmc2_HB[17] are wired to XCKU040 GCC inputs. fmc2 HB signalling is distributed over the two IO_Bank_45 and IO_Bank_47.
fmc2_CLK0_M2C	IO_Bank_47	HP	Direct control to XCKU040 MMMCs and PLLs
fmc2_CLK1_M2C	IO_Bank_47	HP	Direct control to XCKU040 MMMCs and PLLs
fmc2_CLK2_M2C	--	--	Source from on-board CLK100 or PGMCLK from LMK04803.
fmc2_CLK3_M2C	--	--	Source from on-board CLK100 or PGMCLK from LMK04803.
fmc2_DBG_SMB	IO_Bank_44	HP	Support for XUSER FMC#1 debugging

Table 2.36.: IFC_1211 VITA57.1 FMC HPC Signalling

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Note KINTEX-7 Ultrascale family instantiates a new clock distribution architecture with enhanced distribution facilities. Refer to XILINX UG 572 "UltraScale Architecture Clocking Resources"

Note On IFC_1211, the FMC LA, HA and HB signalling are routed without any polarity inversion between the FPM carrier connector and the CENTRAL_FPGA.

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2.9.5.3 FMC VITA57.1 Gigabit Interface

The two ANSI/VITA57.1 FMC Gigabit Interface are both connected to the CENTRAL_FPGA KINTEX-7 Ultrascale XCKU040 Quad_MGT blocks :

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- P400 VITA57.1 FMC#2 site → Quad MGT_224 (+ optional MGT_225)
- P401 VITA57.1 FMC#1 site → Quad MGT_228

The VITA57.1 Gigabit interface allows to implements SerDes based communication as XILINX "Aurora", PCI Express x4, Serial RapidIO, and user defined protocol.

1340 The P400 VITA57.1 FMC#2 site can optionally be connected to an additional MGT_225 providing eight(8) Gigabit Interface lanes. Refer to § 2.9.3.2 and § 2.9.3.1

Warning

As defined by the VITA57.1 specification, all AC coupling capacitors shall be located on the FMC Mezzanine, so no AC coupling capacitors are implemented on the IFC1211 carrier board .

Note *Thanks to multi PCI Express IPcore (up to three) available in CENTRAL_FPGA KINTEX7 Ultrascale XCKU040, additional PCI Express interfaces (EP or RC) can also be integrated on the FMC . (External PCI Express cable, DSP engines, ...)*

1350 **2.9.5.4 FMC VITA57.1 Clocking Infrastructure**

The IFC_1211 implements following clocking support to/from the ANSI/VITA57.1-R2010 FMC sites. Implementation is conditionned by the XILINX KINTEX-7 Ultrascale architecture.

For both FMC sites (P400, P401) the C2M clocks are assigned as follow :

- “CLK3_BIDIR” is driven by on-board 100 MHz reference clock while CLK_DIR = High, otherwise high impedance (not used)
- “CLK2_BIDIR” is driven by a programmable clock supplied by LMK04803 Programmable Synthesiser Refer to § 2.8.2 ,while CLK_DIR = High, otherwise high impedance (not used)

The “CLK3_BIDIR” and “CLK2_BIDIR” clock signal are controlled with external LVDS buffer with high impedance capability U316, U317, U318, U319 DS90LV001. The high impedance is controlled directly with the “CLK_DIR” signal supplied by the FMC mezzanine.

1365 The M2C clock signals are connected individually to the CENTRAL_FPGA KINTEX-7 Ultrascale XCKU040 Global Clock inputs located in the IO_Bank_47.

- FMC#2 CLK0_M2C → IO_Bank_47_GC (Global Clock)
- FMC#2 CLK1_M2C → IO_Bank_47_GC (Global Clock)
- FMC#1 CLK0_M2C → IO_Bank_47_GC (Global Clock)
- FMC#1 CLK1_M2C → IO_Bank_47_GC (Global Clock)

Note *The CENTRAL_FPGA MRCC IO pins allows to control directly the IO_cell clocking and provide optimized routing to the KINTEX-7 Ultrascale CMT/MMCM. (PLL/DLL functions)*

1375 **Note** *Any CENTRAL_FPGA IO connected to LA, HA or HB Interface is able to supply clock reference to the FMC Mezzanine.*

2.9.5.5 FMC VITA57.1 I2C Interfacing

The VITA57.1 FMC I2C/SMBus are both connected to IFC_1211 I2C/SMBus Bus 3. Refer to § 2.10

- FMC#1 : I2C Bus_3 Address = 0xXX (Refer VITA57.1 Specification)**
FMC#2 : I2C Bus_3 Address = 0xXX (Refer VITA57.1 Specification)

1385 2.9.5.6 FMC VITA57.1 Derogations and Limitations

Due to IFC_1211 implementation based on KINTEX-7 Ultrascale, following exceptions shall be considered for the FMC Mezzanine utilization :

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- The power signal **VIO_B_M2C** supplied by the mezzanine used to fill the CENTRAL_FPGA corresponding VCC_IO. (limitation on the FPGA pin count) All FPGA IO Bank interfacing the FMC are powered with **VADJ** (programmable from 1.5[V] → 2.5[V]).
 - The FMC JTAG port are not implemented
 - The FMC signals VREF_A_M2C and VREF_A_M2C are not used. The CENTRAL_FPGA inputs do not support IO standard requiring external voltage reference. The KINTEX-7 Ultrascale XCKU040 device is capable to built internally a VREF derived from the IO_Bank VCC_IO. (= VCC_IO / 2)
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1400 2.9.5.7 FMC VITA57.1 VHDL Examples

A basic VITA57.1 FMC controller interface is supplied in example. This example is instantiated twice (FMC#1, FMC#2) and allows to control individually each FMC signals.

To Be Updated

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2.10 I2C Infrastructure

The IFC_1211 I2C/SMBus infrastructure can be controlled from two Master controllers.

1. T2081 embedded I2C Module (Master/Slave)
2. PON_FPGA I2C Master Controller backward compatible with IFC_1210

The T2081 I2C Module can operate in Master or Slave mode. Refer to NPX QorIQ T2080 Reference Manual, Rev. 2, 02/2016 for complete description.

The legacy IFC_1210 I2C Master Controllers are integrated in the PON_FPGA and controlled through a register set compatible with the T2081 embedded I2C Module. Refer to § 3.2.11

Following table sums-up the IFC_1211 I2C/SMBus/PMBus Slave devices

Bus #	Slave Device		Address	Comments
Bus_1	U1000	LM92535CIMM	0x4C	Temperature sensor local + T2081 die diode
	U1008	DS1339U-33+	0x68	RTC
	U100	XC7A75-1	0x50 0x57	PON_FPGA emulating Pre-Boot loader PON_FPGA emulating System_ID
Bus_2	U702	MAX5970	0x30	VME power supplies LI Controller
	U704	BMR463	0x53	High current DCDC VCC_1V0 (CENTRAL_FPGA, ...)
	U705	BMR463	0x24	High current DCDC VCC_1V0 (T2081 core)
	U707	BMR463	0x63	High current DCDC VADJ (VITA57.1 FMC1/FMC2e)
	U800	PES32NT24AG2	0x75	PCI Express Switch SMBus Slave port
	U329	DS125MB203SQE	0x58	High speed 2:1 MUX CENTRAL_FPGA MGT225 lane[3:2]
	U330	DS125MB203SQE	0x59	High speed 2:1 MUX CENTRAL_FPGA MGT225 lane[1:0]
	U327	DS125MB203SQE	0x5A	High speed 2:1 MUX CENTRAL_FPGA MGT226 lane[3:2]
Bus_3	U331	DS125MB203SQE	0x5B	High speed 2:1 MUX CENTRAL_FPGA MGT226 lane[1:0]
	P400	FMC specific	0x--	VITA57.1 FMC SMBus
	P401	FMC specific	0x--	VITA57.1 FMC SMBus
	P15	XMC specific	0x--	VITA57.1 FMC SMBus
Bus_4	P810	PCIe_Expansion	0x--	PCI Express Expansion to XMP_1262 adjacent PMC/XMC carrier
Bus_5	P0	VME_P0	0x--	Bridged to VME_P0 through CENTRAL_FPGA. SMBus over P0 is defined on GPIO_3/SCL - GPIO_5 /SDA

Table 2.37 : IFC_1211 I2C/SMBus Infrastructure

Note I2C/SMBus Bus_5 is only available through legacy I2C Master Controller

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2.11 IFC_1211 VME64x Interface

The IFC_1211 PCI Express to VME64x Bridge is implemented in PON_FPGA with IOxOS ALTHEA IPcore function.

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- Transparent PCI Express - VME64x Master / Slave Bridge with embedded chained DMA and local shared memory
- TOSCA IIA Network on Chip (NoC) based architecture optimized for ARTIX-7 FPGA family
- True PCI Express End Point x4 Gen2 (v 2.1)
- Higher performance compared to legacy ASIC solutions
- Low Read latency (PCI Express-VME64x)
- Little / Big endian conversion by hardware
- High performance DMA (>1'600 MBytes/s with PCI Express Gen2)
- IO Space for CSR mapping
- Programmable Memory Space window size (Prefetchable and Non-Prefetchable)
- INgress MMU based IO scatter-gather on PCI Express and VME Slave ports
- VME Address CFG, A16, A24, A32, ADO, and ADOH
- VME Data D08, D16, D32, BLT32, MBLT64, 2eVME, 2eSST, and 2eSST Broadcast to access multiple VME slaves
- System Controller PRI, RRS, BTO, 2eBTO
- Drivers for Linux and VxWorks

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The complete function description is supplied in ALTHEA_IFC1211_UG document.

Note IOxOS ALTHEA “PCI Express to VME64x Bridge” has been already integrated in IOxOS COTS product as PEV_7912, VDV_7913 and also in other major VME actors as ACROMAG, XES, Curtiss Wright, ...

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2.11.1 ALTHEA_IFC1211 Implementation Specific

The ALTHEA “PCI Express to VME64x Bridge” function is implemented in IFC_1211 with some specific set-up.

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- ALTHEA_IFC1211 PCI Express x4 Gen2 EP is connected to PES32NT24AG2 Port_00
- The VME64X electrical interface is built with 74VMEH22501A transceivers.
- The VME64x interface uses 5 -rows P1/P2 connectors
- The SMEM DDR3 is not implemented, only internal 1 MBytes SMEM built with FPGA BRAM resource is available.
- The PCI Express BAR window size are hard-wired to pre-defined size.
 - PCIe_EP_MEM_PF_A64 = '0' → A64 Prefetchable window enabled
 - PCIe_EP_MEM_PF_SIZ = "101" → 1024 MBytes
 - PCIe_EP_MEM_NoPF_SIZ = "110" → 128 MBytes
 - PCIe_EP_IO_4K = '1' → 4 KBytes IO Space

Note The default PCI Express BAR window size option can be redefined with dynamic option

selection stored in the SPI Flash EPROM. Refer to IFC1211_ALTHEA_UG Chapter 4.4.3

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2.11.2 IFC1211 T2081 IFC_Bus → VME Direct Path

Due to inherent PCI Express architecture, a consequent delay latency is added for each transaction beat. This initial latency can be masked in case of burst transaction but remain relatively important for single beat transaction, especially in case of transparent VME Read.

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The latency delay of PCI Express to VME Master Write transaction can be easily hidden with Write Posting support, but the latency delay on PCI Express to VME Master Read transaction introduce a consequent dead time.

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In application using large amount of processor single beat VME Read, the use of PCI Express to VME64x bridge has inherent poor performance. Moreover the PON_FPGA integrating the ALTHEA "PCI Express to VME64x Bridge" function is connected through the PCI Express Switch PES32NT24AG2, adding a latency of 2x 160[ns].

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To solve this issue the IFC_1211 integrates an independent VME direct path from T2081 IFC_Bus to the ALTHEA VME Master controller, optimized to have minimal latency dead time on T2081 ← VME Master Read single beat transaction.. (IFC CS7, 256 MBytes window, GPCM with external termination) Refer to § 2.6.8.3

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The T2081 IFC_Bus → VME Master Write transaction can be handled with or without a 1-stage write posting selected with "ifc_VMEDIRO_WPOST" located in IFC_VMEDIRP_CTL register. Refer to § 3.2.12 . VME Master Write with BERR# acknowledge signalling is reported to the T2081 through ifc_PERRn signal.

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The T2081 IFC_Bus ← VME Master Read with BERR# acknowledge is reported to the T2081 through a Parity Error.

The VME RETRY# acknowledge is handled by the hardware FSM, with mode of operation selected with "ifc_VMEDIRP_RTY[1:0]" located in IFC_VMEDIRP_CTL register. Refer to § 3.2.12

This independent path is implemented with an IFC_INgress MMU scatter-gather of 64 pages of 4 MBytes, similar to the PCI INgress MMU. Refer to ALTHEA_IFC1211_UG Chapter 2.1.6

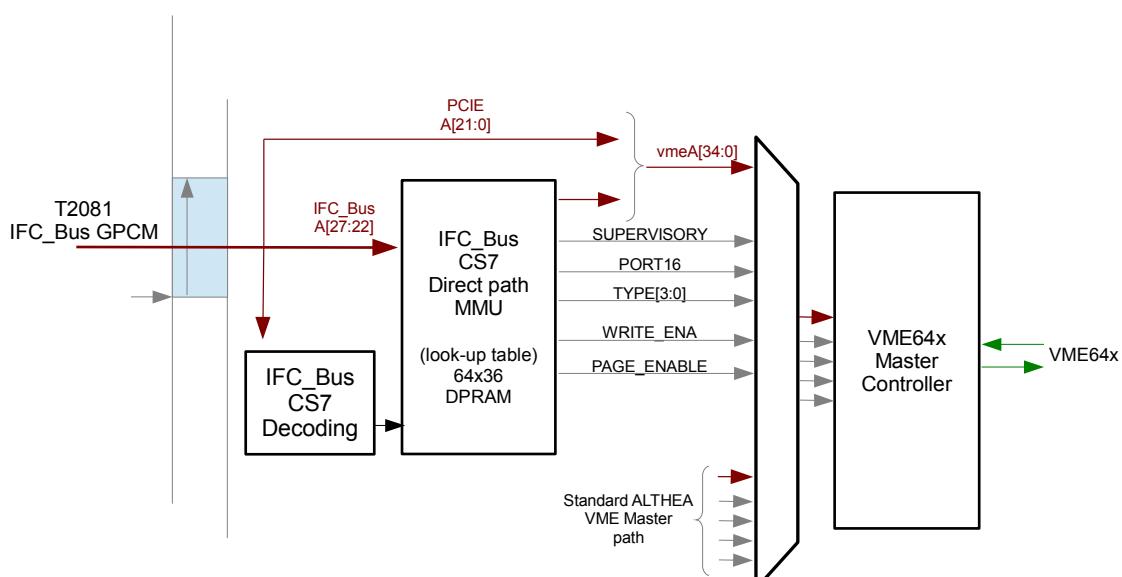


Illustration 7 : IFC_1211 IFC Bus Direct Path -> VME64x Master

The IFC_INgress MMU look-up table is implemented within a 64x36 DPRAM initialized/loaded

through two control registers “IFCBus_VMEDIRP_MMUADD”, “IFCBus_VMEDIRP_MMUDAT”. Refer to § 3.2.12

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For each page entry (4 MBytes), an associated 36-bit Page_Descriptor provides following parameters :

Bit[]	Field	Description	Comments				
<i>Low WORD Page_Descriptor (IFC_INgress_MMU_ADD0 = '0')</i>							
[0]	Page_Enable	Enable the Page entry. If not set, the incoming transaction is rejected					
[1]	Write_Enable	Enable Write access across this page entry. If not set, the Write is rejected.	Allows to support write-protect area per page entry				
[2]	Reserved	Not used					
[3]	VME_Port_D16	Select 16-bit data port interface. While set, 32-bit operand are executed with dual 16-bit operand. <table border="1" data-bbox="610 819 1142 954"> <tr> <td>0</td><td>Standard VME 32-bit interface</td></tr> <tr> <td>1</td><td>Legacy VME 16-bit interface (Only P1 connector installed or VME Slave supporting only D16 transactions)</td></tr> </table>	0	Standard VME 32-bit interface	1	Legacy VME 16-bit interface (Only P1 connector installed or VME Slave supporting only D16 transactions)	
0	Standard VME 32-bit interface						
1	Legacy VME 16-bit interface (Only P1 connector installed or VME Slave supporting only D16 transactions)						
[4]	VME_Program	Select Data/Program level. Only applicable while targeting VME64x Master interface. <table border="1" data-bbox="610 1066 1142 1156"> <tr> <td>0</td><td>VME Data AM</td></tr> <tr> <td>1</td><td>VME Program AM</td></tr> </table>	0	VME Data AM	1	VME Program AM	Refer to VME64x Specification.
0	VME Data AM						
1	VME Program AM						
[5]	VME_Supervisory	Select User/Supervisory level. Only applicable while targeting VME64x Master interface. <table border="1" data-bbox="610 1268 1142 1358"> <tr> <td>0</td><td>VME User AM</td></tr> <tr> <td>1</td><td>VME Supervisory AM</td></tr> </table>	0	VME User AM	1	VME Supervisory AM	Refer to VME64x Specification.
0	VME User AM						
1	VME Supervisory AM						
[7:6]	Byte Swapping Policy	BYTE Swapping Policy. This 2-bit field specifies the Byte Swapping policy (Little – Big Endian conversion) <table border="1" data-bbox="610 1448 1142 1538"> <tr> <td>00</td><td>No Swapping</td></tr> <tr> <td>Others</td><td>Not supported</td></tr> </table>	00	No Swapping	Others	Not supported	There is no Byte swapping requirement because T2081 and VME64x are big endian
00	No Swapping						
Others	Not supported						
[11:8]	Space_TYPE[3:0]	This 4-bit field encodes the Address Space targeted in VME64x (Refer to)	Encoded to				
[15:12]	Reserved	Not used in IFC_INgress MMU					
[17:16]	Reserved	Not used in IFC_INgress MMU					
<i>High WORD Page_Descriptor (IFC_INgress_MMU_ADD0 = '0')</i>							
[19:18]	Reserved	Not used in IFC_INgress MMU					
[31:20]	int_ADD[31:20]	Internal VME64x High Address remapping.					
[35:32]	int_ADD[35:32]	4-bit field is also used for : <ul style="list-style-type: none"> USER AM code selection. Refer to ALTHEA_IFC1211_UG Chapter X.X.X 					

Table 2.38.: IFC_1211 IFC_INgress MMU Page_Descriptor

Space_TYPE[3:0]	VME64x Master Addressing Space
0x0	Configuration Space
0x1	A16 : D08-D16-D32
0x2	A24 : D08-D16-D32
0x3	A32: D08-D16-D32
0x4	A32: BLT
0x5 - 0xE	Not supported for IFC_Bus VME Direct Path
0xF	IACK Cycle

Table 2.39.: IFC_1211 IFC_INgress VME64x Address Space Type Encoding

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Note For easiest software support, the IFC_INgress Page Descriptor format and the Space_TYPE[3:0] encoding is similar to ALTEA PCI INgress.

2.11.3 IFC1211 VME_P0

The IFC_1211 provides a VME P0 connector based on 3M UHM technology.

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The 3M Ultra Hard Metric UHM connector technology makes possible to use the VME64x P0 legacy connector with high-speed SERDES protocols (PCI Express GEN1/GEN2, Serial RapidIO, USB 3.0 or Custom point to point protocols as AURORA).

The following tables shows how the pin-out organization :

Row	Group Allocation					Comments
	a	b	c	d	e	
1						FPGA KINTEX-7 Ultrascale XCKU MGT_225 <ul style="list-style-type: none"> • 1 group of 4 GTH • TxCLK / RxCLK
2						
3						
4						
5						FPGA KINTEX-7 Ultrascale XCKU MGT_226
6						or PCIe Switch PES32NT24AG2 → Port_20
7						<ul style="list-style-type: none"> • 1 group of 4 GTH • TxCLK / RxCLK
8						
9	■	■	■	■	■	
10	■	■	■	■	■	CENTRAL_FPGA 12x GPIO + 3.3[V]/2.5[V] Power supplies
11	■	■	■	■	■	
12	■	■	■	■	■	
13	■	■	■	■	■	PCIe Switch PES32NT24AG2 → Port_12 <ul style="list-style-type: none"> • PCI Express GEN2 x4/x2/x1 • TxCLK / RxCLK
14	■	■	■	■	■	
15	■	■	■	■	■	
16	■	■	■	■	■	
17	■	■	■	■	■	PCIe Switch PES32NT24AG2 → Port_16 <ul style="list-style-type: none"> • PCI Express GEN2 x4/x2/x1 • TxCLK / RxCLK
18	■	■	■	■	■	
19	■	■	■	■	■	

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- ■ Ten(10) Differential pairs to/from the PCIe Switch PES32NT24AG2
- ■ Ten(10) Differential pairs to/from the PCIe Switch PES32NT24AG2
- ■ Twenty(20) Differential pairs dedicated to the FPGA GTH Transceivers or FMC2 or PCIe Switch PES32NT24AG2
- ■ Twelve(12) single ended from CENTRAL_FPGA KINTEX-7 Ultrascale XCKU040
- ■ Three(3) power supplies as 3.3[V], 2.5[V] and GND

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#	Row_A	Row_B	Row_C	Row_D	Row_E
1	MGT_225_Rx_0P	MGT_225_Rx_1P	MGT_225_RxCLK_P	MGT_225_Tx_0P	MGT_225_Tx_1P
2	MGT_225_Rx_0N	MGT_225_Rx_1N	MGT_225_RxCLK_N	MGT_225_Tx_0N	MGT_225_Tx_1N
3	MGT_225_Rx_2P	MGT_225_Rx_3P	MGT_225_TxCLK_P	MGT_225_Tx_2P	MGT_225_Tx_3P
4	MGT_225_Rx_2N	MGT_225_Rx_3N	MGT_225_TxCLK_N	MGT_225_Tx_2N	MGT_225_Tx_3N
5	MGT_226_Rx_0P	MGT_226_Rx_1P	MGT_226_RxCLK_P	MGT_226_Tx_0P	MGT_226_Tx_1P
6	MGT_226_Rx_0N	MGT_226_Rx_1N	MGT_226_RxCLK_N	MGT_226_Tx_0N	MGT_226_Tx_1N
7	MGT_226_Rx_2P	MGT_226_Rx_3P	MGT_226_TxCLK_P	MGT_226_Tx_2P	MGT_226_Tx_3P
8	MGT_226_Rx_2N	MGT_226_Rx_3N	MGT_226_TxCLK_N	MGT_226_Tx_2N	MGT_226_Tx_3N
9	GPIO_6	GPIO_9	VCC2V5	GPIO_3	GPIO_0
10	GPIO_7	GPIO_10	GND	GPIO_4	GPIO_1
11	GPIO_8	GPIO_11	VCC3V3	GPIO_5	GPIO_2
12	P0_A_Rx_2P	P0_A_Rx_3P	P0_A_TxCLK_P	P0_A_Tx_2P	P0_A_Tx3P
13	P0_A_Rx_2N	P0_A_Rx_3N	P0_A_TxCLK_N	P0_A_Tx_2N	P0_A_Tx_3N
14	P0_A_Rx_0P	P0_A_Rx_1P	P0_A_RxCLK_P	P0_A_Tx_0P	P0_A_Tx_1P
15	P0_A_Rx_0N	P0_A_Rx_1N	P0_A_RxCLK_N	P0_A_Tx_0N	P0_A_Tx_1N
16	P0_B_Rx_2P	P0_B_Rx_3P	P0_B_TxCLK_P	P0_B_Tx_2P	P0_B_Tx_3P
17	P0_B_Rx_2N	P0_B_Rx_3N	P0_B_TxCLK_N	P0_B_Tx_2N	P0_B_Tx_3N
18	P0_B_Rx_0P	P0_B_Rx_1P	P0_B_RxCLK_P	P0_B_Tx_0P	P0_B_Tx_1P
19	P0_B_Rx_0N	P0_B_Rx_1N	P0_B_RxCLK_N	P0_B_Tx_0N	P0_B_Tx_1N
	 P0_Input  P0_Output				

Table 2.40 : IFC_1210 VME UHM P0 VME64x UHM P0 pin assignment.

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The CENTRAL_FPGA MGT_225 can be connected either to the VME_P0 or to the FMC#2 high speed lane{7.4} with dual high-speed 2:1 multiplexer U329, U330 DS125MB203SQE. Refer to § 2.9.3.2 Thanks to multiple PCIe IPcore embedded in the CENTRAL_FPGA, The MGT_225 can be configured as PCI Express EP(End Point) or RC (Root Complex), providing a 2nd PCI Express connection to the CENTRAL_FPGA.

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The CENTRAL_FPGA MGT_226 can also be connected either to the VME_P0 or to the PCIe Switch PES32NT24AG2 P20 (PCI Express x4 gen2) with dual high-speed 2:1 multiplexer U327, U331 DS125MB203SQE. Refer to § 2.9.3.2

The high-speed differential allocated to the CENTRAL_FPGA KINTEX-7 Ultrascale XCKU040 MGT group MGT_225 and MGT_226 are AC coupled on the IFC_1211.

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The VME_P0 2.5[V] power supply is protected on FC1211 with a fuse F400 USF0603 2A/63V.

GPIO[11:0] signalling is controlled to/from the CENTRAL_FPGA with HR IO_Bank_65 (3.3[V] VCC_{IO}) For backward compatibility with IFC_1210, GPIO_[3:0] are reserved for dedicated purpose.

GPIO_0	OUT	IFC1211 System RESET (active low)
GPIO_1	OUT	IFC1211 PCI Express RESET (active low)
GPIO_[9:2]	IO	Available for User specific application
GPIO_10	IO	I2C/SMBus Port_4 SCL (Open drain, require pull-up on the rear IO)
GPIO_11	IO	I2C/SMBus Port_4 SDA (Open drain, require pull-up on the rear IO)

Note The VME_P0 I2C/SMBus interface is available only through the internal I2C/SMBus/PMBus Master Controller 3.2.11 .

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2.11.4 IFC1211 VME_P2 User IO

The VME_P2 User IO rows D and Z are connected to directly to the IO_FPGA U803 ARTIX-7 XC7A75-2-FG484.

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The VME_P2 User IO rows A and C are connected to the IO_FPGA U803 ARTIX-7 XC7A75 through a custom configurable twin SMD 0603 0_ohms resistors array allowing to control the interconnect between the PMC/XMC Jn14, the VME_P2 rows A and C and/or the IO_FPGA. An array of 64 dual 0603 footprint is available for custom configuration. Refer to § 2.7.6

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To support VME_P2 User_IO control from embedded user application in the CENTRAL_FPGA U300 KINTEX-7 Ultrascale XCKU040, a high-speed time multiplexed interface (HSI) is supplied with IOxOS IPcore support. Refer to § 2.9.2.3

For backward compatibility with previous generation IFC_1210, VME_P2 missing power supplies 3.3[V], +12[V] and -12[V] can be optionally forwarded to VME_P2 rows C with jumpers J101-J113. Refer to § 2.4.8

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2.12 VME USER Agent_SW TCSR Resources

The IFC_1211PON_FPGA ALTHEA sub-section, integrating the PCIe-VME64X Bridge function provides through its VME CRCSR Slave port following direct mapping of :

- Local TCSR USER_IFC1211 Signature, RWT and T2081 Remote RESET control registers
- IFC_1211 IFCBus Register Bridge. Refer § 3.2.1

Offset	IO_BUS	Size	Register_Name	Description	Comments
0xC00 - 0xC03		0x4	IFC1211_PON_VENDDEV_ID	IFC1211 PON_FPGA Read only Vendor/Device identifier.	2.12.1
0xC04 - 0xC07		0x4	IFC1211_PON_SIGN_ID	IFC1211 PON_FPGA Read only Signature	2.12.2
0xC08 - 0xC0B		0x4	IFC1211_RWT	Simple 32-bit Write/Read register	2.12.3
0xC0C - 0xC7F		0x4	IFC1211_T2081_REMCTL	T2081 Remote control RESET	2.12.4
0xC80-0xC8F		0x10	USER_ITC	USER ITC Interrupt Pending	Refer to IFC1211_ALTHEA_UG
0xC90 - 0xCFF			Reserved	Not implemented	
0xD00- 0xDFF		0x100	IFCBus_CSR Bridge	Bridging to IFC_1211 IFCBus mapped resources. Refer to IFC-1211_UG Chapter 3 "IFC_1211_HSID"	\$ 3.2.1
0xE00- 0xF7F			Reserved	Not used	
0xF80 - 0xFFFF		0x80	Signature_ROM	Defined ROM area for software signature	Refer to IFC1211_ALTHEA_UG

Table 2.41. : USER_IFC1211 TCSR Resources mapping

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CME CRC SR Bridge

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2.12.1 IFC1211_VendDev Register

This read only register provides related PCI Express Vendor_ID + Device_ID information.

VENDEDEV_ID IO_Bus : 0xC00 - 0xC03		PON_FPGA Vendor/Device ID				
Bit[]	Function	R/W	Reset	Description	Comments	
[31:0]	PON_VendDev_ID[31:0]	R	Value	Fixed Value = 0x7357_1211		

2.12.2 IFC1211_Signature Register

This read only register provides Signature_ID (Day, Month, Year and version)

SIGN_ID IO_Bus : 0xC04 - 0xC07		PON_FPGA Signature ID				
Bit[]	Function	R/W	Reset	Description	Comments	
[31:0]	PON_Signature_ID[31:0]	R	Value	Signature = DDMMYYYY		

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2.12.3 IFC1211_RWT Register

This simple 32-bit Read-Write Registers allows to implement SW markers.

RWT IO_Bus : 0xC08 - 0xC0B		Read_Write_Test Register				
Bit[]	Function	R/W	Reset	Description	Comments	
[31:0]	TEST1[31:0]	RW	0x12345678	Basic 32-bit RW register.		

2.12.4 IFC1211_T2081_Remote Control Register

This simple 32-bit Registers provides IFC_1211 T2081 RESET remote control.

RWT IO_Bus : 0xC08 - 0xC0B		Read_Write_Test Register				
Bit[]	Function	R/W	Reset	Description	Comments	
[29:0]	Reserved	R	0x00000000	Not used		
[30]	cpu_HRST	RW	'0'	While '1', the T2081 HRSTn is activated if SW100-3 is "ON".		
[31]	cpu_PONRST	RW	'0'	While '1', the T2081 PONRSTn is activated if SW100-3 is "ON".		



2.13 Miscellaneous

The ...

2.13.1 Miscellaneous #1

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This

3. IFC_1211 HSID

1595 Following chapters provides the IFC_1211's Hardware-Software Interface Data (HSID).

3.1 QorIQ T2081 Mapping

The T2081 resource mapping is assigned during the primary bootstrap by U-BOOT utility. Following table sum up the default mapping.

T2081 Address Range	Ressources	Comments
0x0000'0000-0x3FFF'FFFF	System Memory	1st GBytes
0x4000'0000-0x7FFF'FFFF	System Memory Extension	2nd GBytes
0x8000'0000-0xBFFF'FFFF	PCIe3 x4 Gen2	PCI MEM space (1 GBytes window) PES32NT24AG2
0xC000'0000-0xCFFF'FFFF	PCIe4 x4 GEN3	PCI MEM space (256 MBytes Window) CENTRAL FPGA Kintey7 Ultrascale
0xD000'0000-0xDFFF'FFFF	VME Master Direct path	Low latency VME direct path
0xF802'0000-0xF802'FFFF	PCIe3 x4 Gen2	PCI IO space (64Kbytes window)
0xF803'0000-0xF803'FFFF	PCIe4 x4 Gen3	PCI IO space (64Kbytes window)
0xFFD0'0000-0xFFD0'FFFF	IFC CSR Resources	Mirrored with User AgentSW IO_Bus Slave
0xFFC0'0000-0xFFFF'FFFF	NOR Flash Memory	Emulated with SPI Flash EPROM

Table 3.1 : T2081 Default Resources Mapping

For internal T2081 resource, refer to NPX/Freescale documentation "QorIQ T2081 Integrated Processor Reference Manual"

Note Above address reference are valid for U-BOOT set-up. Because the T2081 provides dynamic resource mapping capability, the OS mapping can be different

3.1.1 IOxOS UBOOT Add-on

Following UBOOT commands have been added to access IFC specific hardware resources

3.1.1.1 UBOOT for the IFC1211

After reset or power on the IFC1211 enter u-boot. Refer to the u-boot documentation for a list and syntax of supported commands.

```
U-Boot 2015.01+SDKv1.9+geb3d4fc (Sep 28 2016 - 10:41:30)

CPU0: T2081, Version: 1.1, (0x85310011)
Core: e6500, Version: 2.0, (0x80400120)
Clock Configuration:
    CPU0:1199.880 MHz, CPU1:1199.880 MHz, CPU2:1199.880 MHz, CPU3:1199.880 MHz,
    CCB:533.280 MHz,
    DDR:666.650 MHz (1333.300 MT/s data rate) (Asynchronous), IFC:133.320 MHz
    FMAN1: 533.280 MHz
    QMAN: 266.640 MHz
    PME: 533.280 MHz
```



```
L1: D-cache 32 KiB enabled
    I-cache 32 KiB enabled
Reset Configuration Word (RCW):
    00000000: 10050012 15000000 00000000 00000000
    00000010: aa020002 00004000 ec027000 a1000000
    00000020: 00000000 00000000 00000000 000307fc
    00000030: 00000000 00000000 00000000 00000004
Board: T2081RDB, Board rev: 0xff CPLD ver: 0xff, boot from NAND
SERDES Reference Clocks:
SD1_CLK1=100.00MHZ, SD1_CLK2=100.00MHZ
SD2_CLK1=100.00MHZ, SD2_CLK2=100.00MHZ
I2C: ready
SPI: ready
DRAM: Initializing....using SPD
    SPD emulation..Detected UDIMM
    Performing Hardware DDR test
    Test mode 0... -> Done OK
    2 GiB (DDR3, 64-bit, CL=11, ECC on)
VID: Core voltage is currently at 1048 mV
VID: set voltage to BMR at 1025 mV
VID: Core voltage after adjustment is at 1048 mV
Flash: PON Emulation 64 MiB
L2: 2 MiB enabled
Corenet Platform Cache: 512 KiB enabled
Using SERDES1 Protocol: 170 (0xaa)
Using SERDES2 Protocol: 2 (0x2)
NAND: 512 MiB
MMC: FSL_SDHC: 0
EEPROM: Read failed.
1655    PCIE3: Root Complex, x4 gen2, regs @ 0xfe260000
        01:00.0      - 111d:808c - Bridge device
        02:00.0      - 111d:808c - Bridge device
        03:00.0      - 7357:1211 - Bridge device
        02:04.0      - 111d:808c - Bridge device
        04:00.0      - 7357:1000 - Bridge device
        02:05.0      - 111d:808c - Bridge device
        05:00.0      - 10b5:8112 - Bridge device
        02:06.0      - 111d:808c - Bridge device
        02:08.0      - 111d:808c - Bridge device
        02:0c.0      - 111d:808c - Bridge device
        02:10.0      - 111d:808c - Bridge device
        02:12.0      - 111d:808c - Bridge device
        02:14.0      - 111d:808c - Bridge device
        0c:00.0      - 7357:1002 - Bridge device
1660    PCIE3: Bus 00 - 0c
PCIE4: Root Complex, x4 gen2, regs @ 0xfe270000
    0e:00.0      - 7357:1001 - Bridge device
PCIE4: Bus 0d - 0e
In: serial
Out: serial
Err: serial
Net: SerDes1 protocol 0xaa is not supported on T208xRDB
Fman1: Uploading microcode version 106.4.17
FM1@DTSEC3 [PRIME], FM1@DTSEC4
1675    =>
1680
```

3.1.1.2 Board configuration

The **conf** command allows to display the IFC1211 current configuration:

```
1685    => conf show
Board local temperature: 32
T2081 die temperature : 32
BMR463_1 [central FPGA]:
    VIN : 4.960 [ca7b]
    VOUT : 0.948 [1e5e]
    IOUT : 5.335 [caab]
1690
```



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3.1.1.3 PROM access

The ***prom*** command allows to read/program the emulated PROMs controlled by the PON FPGA PROM#2 and PROM#3 contain bit stream for IO and CENTRAL FPGAs. PROM#4 contains boot objects (RCW,u-boot,...) for the t2080.

Syntax:

prom.<x> <operation> [<para0> <para1>...]

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where $\langle x \rangle$ is the PROM index (from 2 to 5)

allowed operations are:

1755

```
prom.<x> rdid
prom.<x> wrsr <sr>
prom.<x> read <addr> <offset> <size>
prom.<x> write <addr> <offset> <size>
prom load <fpga>:<idx>
```

1760

The **rdid** operation displays the 3 bytes PROM identifier

The **wrsr** operation allows to overwrite the PROM 16 bit status register.

The **read** operation read <size> bytes from PROM <offset> and copies them in system memory at address <addr>.

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The **write** operation read <size> bytes from system memory address <addr> and copies them at PROM <offset>.

The **write** operation can be used to update u-boot in PROM 4 at offset 0x3f4000

=> tftp 1000000 u-boot.bin

1770

=> prom.4 write 1000000 3f40000 \$filesize

```
=> tftp 1000000 u-boot-t2080_new.bin
Using FM1@DTSEC3 device
1775   TFTP from server 192.168.1.112; our IP address is 192.168.1.102
Filename 'u-boot-t2080_new.bin'.
Load address: 0x1000000
Loading: #####
9.7 MiB/s
1780   done
Bytes transferred = 786432 (c0000 hex)
=> prom.4 write 1000000 3f40000 $filesize
erase sector 3f40000
program sector 3f40000
040000
erase sector 3f80000
program sector 3f80000
040000
erase sector 3fc0000
program sector 3fc0000
040000
=>
```

1795

The **load** operation shall be used to load FPGA bit streams in PROM the <fpga> identifier can be **io** or **central** and the <index> shall be from 0 to 3.

=> tftp 1000000 IFC1211_CENTRAL_a0.bit
=> prom load 1000000 central:1 \$filesize

1800

3.1.1.4 FPGA loading

The **fpga load** command allows for a dynamic loading of a FPGA bitstream from system memory <addr>

1805

fpga load io <addr>
fpga load central <addr>

3.2 IFC_Bus PON_FPGA Resources

Refer to § 2.9.1 for PON_FPGA description.

1810

3.2.1 IFCBus CSR Resource Mapping

The IFC_1211 IFC_Bus CSR resources are mapped through IFC_Bus CS6

Refer to § 2.6.8.2

1815

Following CSR resources are mapped over the T2081 IFC Bus CS6 space

IFCBus Offset	Register	Comments
+ 0x0000	IFCBus_VendDev_ID	Vendor_ID + Device_ID = 0x7357_1211
+ 0x0004	IFCBus_Static_SW	Status of the IFC_1211 static options. (Switches & Hex_ROT)
+ 0x0008	IFCBus_VME_CTL	VME64x related
+ 0x000C	IFCBus_FMCXMC_CTL	Mezzanine card control FMC, XMC, PMC
+ 0x0010	IFCBus_PON_imer	Power up timer
+ 0x0014	IFCBus_PCIESW	PCI Express Switch PES32NT24AG2 Static option
+ 0x0018	IFCBus_RWTST1	32-bit RW Register (Cleared while Short RESET)
+ 0x001C	IFCBus_HDLSIGN	32-bit signature word. Defined in the VHDL source code
+ 0x0020	IFCBus_FPGA_CFGCTL	FPGA Configuration control
+ 0x0024	IFCBus_FPGA_CFGDAT	FPGA Configuration data port (32-bit)
+ 0x0028	IFCBus_SPICTL	SPI Master Controller
+ 0x002C	IFCBus_PGM_RST_CTL	T2081 + FPGA PGM RST Sequencing
+ 0x0030 ...	Reserved	Not used in IFC_1211
+ 0x003C		
+ 0x0040	IFCBus_BMRCTL	BMR463 SYNC Control
+ 0x0048	IFCBus_LMK04806	Dual PLL Clock Synthesise Control Register
+ 0x004C	IFCBus_LMK04806	Dual PLL Clock Synthesise Data Register
+ 0x0050	IFCBus_DS125MB203	DS125MB203 2:1 PCIe Multiplexer P0 direct control <ul style="list-style-type: none"> • VME_P0 → PCIe Switch 32NT24 • VME_P0 → PCIe Switch MGT226/MGT225
+ 0x0054	IFCBus_VMEDIRP_CTL	IFC_Bus → VME64x Direct path control
+ 0x0058	IFCBus_VMEDIRP_MMUADD	IFC_Bus → VME64x IFC_INgoing MMU Address Pointer
+ 0x005C	IFCBus_VMEDIRP_MMUDAT	IFC_Bus → VME64x IFC_INgoing MMU Data
+ 0x0060 ...	Not Implemented	Reserved for further user defined resources
+ 0x006F		
+ 0x0070	T2081_IRQ_IMSK	Interrupt Mask register
+ 0x0074	T2081_IRQ_IP	Interrupt Pending register
+ 0x0078	T2081_IRQ_ICLR	IP Clear Command register
+ 0x007C	T2081_STATIC_OPT	T2081 Static Options
+ 0x0080...0x008F	IFCBus_NEW_I2C_CTL_0 IFCBus_NEW_2C_CMD_0	NEW Individual I2C Controller #0

	IFCBus_NEW_I2C_DATW_0 IFCBus_NEW_I2C_DATR_0	
+ 0x0090 0x009F	IFCBus_NEW_I2C_XXX_1	NEW Individual I2C Controller #1
+ 0x00A0...0x00AF	IFCBus_NEW_I2C_XXX_2	NEW Individual I2C Controller #2
+ 0x00B0...0x00BF	IFCBus_NEW_I2C_XXX_3	NEW Individual I2C Controller #3
+ 0x00C0...0x00CF	IFCBus_NEW_I2C_XXX_4	NEW Individual I2C Controller #4
+ 0x00D0...0x00FF	Reserved	
+ 0x0100...0xFFFF	Not Implemented	Reserved for further user defined resources
+ 0xE000...0xFFFF	IFCBus_SRAM	8 KBytes SRAM scratcharea

Table 3.2 : T2081 IFC Bus “PON” Resources Mapping

Note Above resources are also mapped through the VME64X CRCSR space.

3.2.2 SRAM

A 8 KBytes SRAM area is instantiated at the top of the decoded area. This SRAM area can be used for temporary data storage, independent from Cold_RESET sequence.

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Note The IFC_Bus mapped SRAM is reset to its default contents (All '0') only at power-up PON_FPGA configuration.

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Note The IFC_Bus mapped SRAM can not be mapped through the VME64x/CRCRS space.

3.2.3 General Control & Status

3.2.3.1 IFCBus_VendDev_ID

Following IFC_Bus Register provides HDL related Vendor_ID + Device_ID information.

IFCBus_VendDev_ID		“PON” Vendor_ID + Device_ID Signature				
IFCBus	: 0x0000 - 0x0003	R/W	Reset	Description	Comments	
[31:0]	VendDev_ID[31:0]	R	Value	Fixed Value = 0x7357_1211		

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3.2.3.2 IFCBus_Static_SW

Following IFC_Bus Register provides status information of the IFC_1211 static options

IFCBus_Static_SW		“PON” Static Switch Status				
IFCBus	: 0x0004 - 0x0007	R/W	Reset	Description	Comments	
[7:0]	Reserved	R	0b00	Not used		
[15:8]	Switch_101[8:1]	R		Mini DIP Switch SW102	Refer to 2.2.1.2	
[17:16]	FPGA_Config[1:0]	R		Mini DIP Switch SW101-2:1	While VME64X CRCSR is enabled, additional static options are defined Refer to § 2.2.1.2	
[18]	PES32NT24_INIT	R		Mini DIP Switch SW101-3		
[23:19]	Reserved			Mini DIP Switch SW101-8:4		

IFCBus_Static_SW IFCBus : 0x0004 - 0x0007		“PON” Static Switch Status				
[23:16]	CRCSR_A24	R		ALTHEA CRCSR mapping default in A24 Mini DIP Switch SW101:8:1	While VME64X CRCSR is not enabled Refer to § 2.2.1.2	
[24]	CFG_Default	R		ALTHEA static configuration Default		
[25]	CFG_Done	R		ALTHEA static configuration Done		
[27:26]	Reserved	R	0b00	Not used		
[31:28]	CPUOPT[3:0]	R		CPU Boot option Mini DIP Switch SW100	Refer to § 2.2.1.1	

3.2.3.3 IFCBus_VME_CTL

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Following IFC_Bus Register provides direct status of VME64x Bus key signals.

IFC_VME_CTL IFCBus : 0x0008 - 0x000B		VME Direct Control and Status				
Bit[]	Function	R/W	Reset	Description	Comments	
[4:0]	Rx_GA	R		VME Geographic addressing		
[5]	Rx_GAP	R		VME Geographic addressing		
[6]	Rx_SLOT1	R		VME Slot-1 function enabled		
[7]	Rx_BBSY#	R		VME BBSY direct signal	! Active Low	
[8]	Rx_ACFAIL#	R		VME direct ACFAIL signal	! Active Low	
[15:9]	Rx_IRQ[7:1]#	R		VME direct INTERRUPT signal	! Active Low	
[27:16]	Reserved			Not used		
[28]	Rx_SYSRESET#	R		VME direct SYSRESET signal	! Active Low	
[29]	Rx_SYSFAIL#	R		VME direct SYSFAIL signal	! Active Low	
[30]	Reserved			Not used		
[31]	Reserved			Not used		

3.2.3.4 IFCBus_FMCXMC_CTL

Following IFC_Bus Register provides direct Mezzanine (PMC, XMC, FMC) related control and status. Refer to 2.4.6

IFC_FMCXMC_CTL IFCBus : 0x000C - 0x000F		Mezzanine Direct Control and Status				
Bit[]	Function	R/W	Res	Description	Comments	
[0]	XMC1_PRST	R		XMC Mezzanine present status = '1' : FMC installed = '0' : FMC installed not installed		
[1]	PMC1_PRST	R		PMC Mezzanine present status = '1' : FMC installed		

IFC_FMCXMC_CTL IFCBus : 0x000C - 0x000F		Mezzanine Direct Control and Status				
				= '0' : FMC installed not installed		
[2]	XMC1_MVMR0	RW	'0'	XMC Mezzanine control		
[3]	XMC1_MBIST	R		XMC Mezzanine status		
[4]	XMC1_ROOT	RW	'0'	XMC Mezzanine control		
[5]	XMC1_TRST	RW	'0'	XMC Mezzanine control		
[12:6]	Reserved			Not used		
[13]	8112_GPIO_0	R		PES8112 PCIe-PCI Bridge direct GPIO status		
[21:14]	Reserved	R		Not used		
[22]	FMC1_PRSTN	R		FMC#1 direct status present = '1' : FMC installed = '0' : FMC installed not installed		
[23]	FMC2_PRSTN	R		FMC#2 direct status present = '1' : FMC installed = '0' : FMC installed not installed		
[29:24]	Reserved	R		Not used		
[30]	FMC12_PG_C2M	RW	'0'	FMC#12 Power Good		
[31]	FMC12_VADJ_ENA	RW	'0'	FMC#12 Enable VADJ power supply		

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3.2.3.5 IFCBus_GENERAL_CTL

The PON_Timer provides a boot time information with [ms] granularity. The PON_Timer is reset (forced to 0x0000) on detection of a "Cold_RESET".

IFC_GENERAL_CTL IFCBus : 0x0010- 0x0013		Power Supplies Direct Control and Status				
Bit[]	Function	R/W	Reset	Description	Comments	
[15:0]	Reserved	R		Not used		
[31:16]	PON_Timer[15:0]	R	0x0000	16-bit counter-timer 1KHz. This counter timer is reset at power-up or under action of Cold_RESET detection		

1845

"Cold_RESET" is activated at power-up or while the "Ergonomic IEEE Hot-swap Injector/Ejector Handle" is opened for more than 1 second.

3.2.3.6 IFCBus_PCIESW_CTL

This control register provides information to configure the PCI Express Switch PES32NT24AG2 while a programmable command RESET is generated with PGM_RSTCMD[1:0] = 01" or "11". Refer to § 2.7.2

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IFC_PCIESW IFCBus : 0x0014 - 0x0017		PCI Express Switch Control and Status																		
Bit[]	Function	R/W	Reset	Description		Comments														
[1:0]	PCIESW_STK1CFC[1:0]	RW	HDL	PCI Express Switch PES32NT24AG2 Stack_1 Static Configuration.																
				<table border="1"> <thead> <tr> <th>CFC[1:0]</th><th>PCI Express Lane assignation</th></tr> </thead> <tbody> <tr> <td>00</td><td>x8</td></tr> <tr> <td>01</td><td>x4 – x4 (<i>RESET default</i>)</td></tr> <tr> <td>10</td><td>x2 – x2 -x4</td></tr> <tr> <td>11</td><td>x2 – x2 - x2 - x2</td></tr> </tbody> </table>		CFC[1:0]	PCI Express Lane assignation	00	x8	01	x4 – x4 (<i>RESET default</i>)	10	x2 – x2 -x4	11	x2 – x2 - x2 - x2					
CFC[1:0]	PCI Express Lane assignation																			
00	x8																			
01	x4 – x4 (<i>RESET default</i>)																			
10	x2 – x2 -x4																			
11	x2 – x2 - x2 - x2																			
[7:2]	Reserved	R		Not used																
[12:8]	PCIESW_STK2CFC[4:0]	RW	HDL	PCI Express Switch PES32NT24AG2 Stack_2 Static Configuration. (VME_P0)																
				<table border="1"> <thead> <tr> <th>CFC[4:0]</th><th>PCI Express Lane assignation</th></tr> </thead> <tbody> <tr> <td>0_0000</td><td>x8</td></tr> <tr> <td>0_0001</td><td>x4 - x4 (<i>RESET default</i>)</td></tr> <tr> <td>0_0010</td><td>x2 – x2 -x4</td></tr> <tr> <td>0_0011</td><td>x2 – x2 - x2 - x2</td></tr> <tr> <td>1_1011</td><td>x1 - x1 - x1 - x1 - x1 - x1 - x1</td></tr> <tr> <td>Others</td><td>Refer to IDT PES32NT24AG user' Manual Table 3.6</td></tr> </tbody> </table>		CFC[4:0]	PCI Express Lane assignation	0_0000	x8	0_0001	x4 - x4 (<i>RESET default</i>)	0_0010	x2 – x2 -x4	0_0011	x2 – x2 - x2 - x2	1_1011	x1 - x1 - x1 - x1 - x1 - x1 - x1	Others	Refer to IDT PES32NT24AG user' Manual Table 3.6	
CFC[4:0]	PCI Express Lane assignation																			
0_0000	x8																			
0_0001	x4 - x4 (<i>RESET default</i>)																			
0_0010	x2 – x2 -x4																			
0_0011	x2 – x2 - x2 - x2																			
1_1011	x1 - x1 - x1 - x1 - x1 - x1 - x1																			
Others	Refer to IDT PES32NT24AG user' Manual Table 3.6																			
[15:13]	Reserved	R		Not used																
[19:16]	PCIESW_STK3CFC[3:0]	RW	HDL	PCI Express Switch PES32NT24AG2 Stack_3 Static Configuration.																
				<table border="1"> <thead> <tr> <th>CFC[3:0]</th><th>PCI Express Lane assignation</th></tr> </thead> <tbody> <tr> <td>0000</td><td>x8</td></tr> <tr> <td>0001</td><td>x4 - x4 (<i>RESET default</i>)</td></tr> <tr> <td>0010</td><td>x2 – x2 -x4</td></tr> <tr> <td>0011</td><td>x2 – x2 - x2 - x2</td></tr> </tbody> </table>		CFC[3:0]	PCI Express Lane assignation	0000	x8	0001	x4 - x4 (<i>RESET default</i>)	0010	x2 – x2 -x4	0011	x2 – x2 - x2 - x2					
CFC[3:0]	PCI Express Lane assignation																			
0000	x8																			
0001	x4 - x4 (<i>RESET default</i>)																			
0010	x2 – x2 -x4																			
0011	x2 – x2 - x2 - x2																			
[23:18]	Reserved	R		Not used																
[28:24]	PCIESW_SWMODE[0:0]	RW	HDL	PCI Express Switch PES32NT24AG2 Static Configuration.																
				<table border="1"> <thead> <tr> <th>SWMOD [3:0]</th><th>Switch Mode of operation</th></tr> </thead> <tbody> <tr> <td>0000</td><td>Single Partition</td></tr> <tr> <td>0001</td><td>Single Partition with reduced latency</td></tr> <tr> <td>0010</td><td>Single Partition with EEPROM initialization</td></tr> <tr> <td>0011</td><td>Single Partition with reduced latency</td></tr> </tbody> </table>		SWMOD [3:0]	Switch Mode of operation	0000	Single Partition	0001	Single Partition with reduced latency	0010	Single Partition with EEPROM initialization	0011	Single Partition with reduced latency					
SWMOD [3:0]	Switch Mode of operation																			
0000	Single Partition																			
0001	Single Partition with reduced latency																			
0010	Single Partition with EEPROM initialization																			
0011	Single Partition with reduced latency																			

IFC_PCIESW IFCBus : 0x0014 - 0x0017		PCI Express Switch Control and Status				
					latency and EEPROM initialization	
				Others	Refer to IDT PES32NT24AG2 user' Manual Table 3.8	
[29:28]	PCIESW_CLKMODE[1:0]	RW	HDL	PCI Express Switch PES32NT24AG2 Static Configuration.		
				CLKMODE	PES32NT24AG2 Clock Mode	
				00	Global Clock Mode	
				01	Local Clock Mode	
				1X	Reserved	
[30]	PCIESW_RSTHALT	RW	'0'	PCI Express Switch PES32NT24AG2 Static Configuration.		
[31]	Reserved	R		Not used		

3.2.3.7 IFCBus_TEST_REG

1855

This simple 32-bit Read-Write register allows to implement SW markers during boot sequencing.

The IFCBus_RWTST register is cleared on assertion of FPSW_DET_SHORT. ("Ergonomic IEEE Hot-swap Injector/Ejector Handle" open for less than 1 second)

IFC_RWTST IFCBus : 0x0018 - 0x001B		Simple RW Test Register				
Bit[]	Function	R/W	Reset	Description	Comments	
[31:0]	TEST1[31:0]	RW	0x00000000	Basic 32-bit RW register. Cleared on detection of FPSW_DET_SHORT.		

3.2.3.8 IFCBus_HDL Signature

1860

This control register provides HDL related signature information.

IFC_HDLSIGN IFCBus : 0x001C - 0x001F		PON_FPGA Signature				
Bit[]	Function	R/W	Reset	Description	Comments	
[31:0]	HDL_Signature[31:0]	R	Value	This status field provides signature information specified in the PON_FPGA VHDL.		

1865

3.2.4 IFCBus FPGA Configuration

Following control and status registers provide facility to configure the CENTRAL_FPGA and IO_FPGA directly from the T2081 processor. The IFC_1211 computing core can be fully operational while the CENTRAL_FPGA and IO_FPGA are not configured.

1870

In this mode of operation is enabled, (SWB-4 = "ON" "**ColdRESET_Mode**") the IFC_1211 FPGA CENTRAL_FPGA and IO_FPGA shall be configured under the control of the T2081 processor.

Note *CENTRAL_FPGA and IO_FPGA can also be configured through the VME64x/CRCRSR space.*

3.2.4.1 IFCBus_FPGA_CFGCTL

This control & status register supports the CENTRAL_FPGA and IO_FPGA configuration logic.

IFCBus_FPGA_CFGCTL IFCBus : 0x0020 - 0x0023		PON_FPGA Configuration Control											
Bit[]	Function	R/W	Reset	Description	Comments								
[0]	fpga_central_INIT	R		FPGA "CENTRAL" KINTEX_7 Ultrascale INIT pin.									
[1]	fpga_central_DONE	R		FPGA "CENTRAL" KINTEX_7 Ultrascale DONE pin.									
[2]	fpga_central_PROG	RW	'0'	FPGA "CENTRAL" KINTEX_7 Ultrascale PROGRAM pin									
[4:3]	Reserved	R		Not used									
[5]	fpga_central_RDWR	RW	'0'	FPGA "CENTRAL" KINTEX_7 Ultrascale RDWR pin.									
[6]	fpga_central_CSI	RW	'0'	FPGA "CENTRAL" KINTEX_7 Ultrascale CSI pin.									
[7]	fpga_central_ENA	RW	'0'	FPGA "CENTRAL" KINTEX_7 Ultrascale Enable Configuration									
[8]	fpga_io_INIT	R		FPGA "IO" ARTIX-7 INIT pin.									
[9]	fpga_io_DONE	R		FPGA "IO" ARTIX-7 DONE pin.									
[10]	fpga_io_PROG	RW	'0'	FPGA "IO" ARTIX-7 PROGRAM pin.									
[13:11]	Reserved	R		Not used									
[14]	fpga_io_CSI	RW	'0'	FPGA "IO" ARTIX-7 CSI pin.									
[15]	fpga_io_ENA	RW	'0'	FPGA "IO" ARTIX-7 Enable Configuration									
[19:16]	fpga_INIT_MEM[5:0]	R	'0'	Read-Write field dedicated to T2081 FPGA load control									
[21:20]	fpga_INIT_PGMLED	RW	"00"	Programmable front panel RS232 yellow LED, dedicated to FPGA configuration support.									
				<table border="1"> <tr> <td>00</td><td>Yellow LED OFF</td></tr> <tr> <td>01</td><td>Yellow LED toggling SLOW</td></tr> <tr> <td>10</td><td>Yellow LED toggling FAST</td></tr> <tr> <td>11</td><td>Yellow LED ON</td></tr> </table>	00	Yellow LED OFF	01	Yellow LED toggling SLOW	10	Yellow LED toggling FAST	11	Yellow LED ON	
00	Yellow LED OFF												
01	Yellow LED toggling SLOW												
10	Yellow LED toggling FAST												
11	Yellow LED ON												

IFCBus_FPGA_CFGCTL IFCBus : 0x0020 - 0x0023		PON_FPGA Configuration Control												
[22]	Seq_T2081_LRESET	W	'0'	While set, IFC-1210 Cold_RESET is activated. Equivalent to FPSW_DET_LONG.										
[23]	iloc_cfg_a7k7_BUSY	R	'0'	Status FPGA configuration DATA push in progress. While reset, new FPGA CFGDAT 32-bit word can be loaded.										
[25:24]	fpga_CONF_BSTR[1:0]	R	"00"	FPGA Harware Configurator status FPGA bit-stream number										
[27:26]	fpga_CONF_STATUS[1:0]	R	"00"	FPGA Harware Configurator status	<table border="1"> <tr><td>00</td><td>Not Configured</td></tr> <tr><td>01</td><td>Error</td></tr> <tr><td>10</td><td>Configured OK</td></tr> <tr><td>11</td><td>Configured BACKUP</td></tr> </table>	00	Not Configured	01	Error	10	Configured OK	11	Configured BACKUP	
00	Not Configured													
01	Error													
10	Configured OK													
11	Configured BACKUP													
[29:28]	Seq_BSTR[1:0]	RW	"00"	FPGA Bit-stream Number associated with command Seq_CONF_CMD										
[30]	Seq_CONF_CMD	RW	'0'	Force FPGA Configuration HW process with Seq_BSTR[1:0]										
[31]	Seq_RUN_CMD	RW	'0' or '1'	Force FPGA RESET release and issue a programmable RESET . This control bit shall be forced to '1' after „CENTRAL“ FPGA and „IO“ FPGA have been configured by the T2081.										
				Note If SW100-3 CENTRAL / IO_CFG is „ON“ -> Seq_RUN_CMD control bit is forced to '1' at power-up.										

1875

Note CENTRAL_FPGA and IO_FPGA configuration signalling is (xxx_INIT, xxx_PROG, xxx_CSI, xxx_RDWR is defined in their logical state. (i.e fpga_central_PROG = '1' → FPGA PROGn is forced in low level)

1880

3.2.4.2 IFCBus_FPGA_CFGDAT

This data register allows to load 32-bit at the time in the configuration logic

- KINTEX_7 Ultrascale CENTRAL_FPGA → 4 Bytes @ 100 MHz.
- ARTIX-7 IO_FPGA → 32-bit @ 100 MHz.

1885

IFC_FPGA_CFGDAT IFCBus : 0x0024 - 0x0027		PON_FPGA Configuration Data				
Bit[]	Function	R/W	Reset	Description	Comments	
[31:0]	FPGA Bit-stream[31:0]	W	0x0000	FPGA bit-stream low half-word common		

IFC_FPGA_CFGDAT IFCBus : 0x0024 - 0x0027	PON_FPGA Configuration Data		
	for CENTRAL_ and IO_FPGA.		

It provides the FPGA configuration streaming support.

When fpga_central_ENA = '1' Every-time the IFCBus_FPGA_CFGDAT is written, the 32-bit is demultiplexed in 4 time 8-bit with 4 clock edges. This sequence is executed in 80[ns].

1890

When fpga_io_ENA = '1' Every-time the IFCBus_FPGA_CFGDAT is written, the 32-bit is demultiplexed in 4 time 8-bit with 4 clock edges. This sequence is executed in 80[ns].

3.2.5 SPI Master Interface

1895

The two SPI Flash EPROM dedicated for the CENTRAL/IO_FPGA bit-stream non volatile storage can be accessed through the T2081 IFCBus port.

- Read access for FPGA signature verification
- Write access for Flash EPROM programming (non volatile storage of FPGA bit-streams and PONFSM microcode)

1900

The SPI Master controller is implemented identical as in the TOSCA II infrastructure, providing backward software compatibility.

1905

3.2.5.1 IFCBus_SPI Register

This register provides control&status information to support on-board SPI Flash EPROM device #2, #3, #4 and #5 programming.

The SPI interface protocol shall be completely controlled under software.

IFCBus_SPI IO_Bus : 0x028 - 0x02B		SPI Flash EPROM programming													
Bit[]	Function	R/W	Res	Description		Comments									
[0]	pgm_SPICLK	W	'0'	SPI Clock calibrated pulse. While set a calibrated 32 [ns] pulse is automatically generated, with controlled set-up /hold time related to "pgm_SPIDO"		Need time accurate sequencing.									
[1]	pgm_SPIDO	RW	'0'	SPI Data OUT direct pin control											
[2]	pgm_SPIDI	R	'0'	SPI Data IN direct pin status											
[3]	pgm_SPICS	RW	'0'	SPI Chip Select direct pin control. '1' for CS active.											
[6:4]	pgm_SPISEL[2:0]	RW	"00"	IFC_1211 SPI Flash EPROM device selection.											
				<table border="1"> <thead> <tr> <th>pgm_SPISEL[2:0]</th> <th>SPI Flash EPROM #n</th> </tr> </thead> <tbody> <tr> <td>Others</td> <td>No selection</td> </tr> <tr> <td>010</td> <td>SPI Device#2</td> </tr> <tr> <td>011</td> <td>SPI Device#3</td> </tr> <tr> <td>100</td> <td>SPI Device#4</td> </tr> </tbody> </table>		pgm_SPISEL[2:0]	SPI Flash EPROM #n	Others	No selection	010	SPI Device#2	011	SPI Device#3	100	SPI Device#4
pgm_SPISEL[2:0]	SPI Flash EPROM #n														
Others	No selection														
010	SPI Device#2														
011	SPI Device#3														
100	SPI Device#4														

IFCBus_SPI IO_Bus : 0x028 - 0x02B		SPI Flash EPROM programming										
				101	SPI Device#5							
					<ul style="list-style-type: none"> SPI Device#2/3 → CENTRAL/IO_FPGA bitstream storage (Low/High nibble) SPI Device#4 → T2081 NOR#0 Flash SPI Device#5 → T2081 NOR#1 Flash 							
[7]	pgm_SPI_BYTEW	W	--	Selection for BYTE (8* BIT) Mode								
					<table border="1"> <thead> <tr> <th></th><th>FPGA bit-stream Nb</th></tr> </thead> <tbody> <tr> <td>0</td><td>Single bit push on SPI MOSI with single SPI CLK</td></tr> <tr> <td>1</td><td>Eight(8) bits push on SPI MOSI with eight(8) SPI CLK. pgm_SPI_BDAT[7] pushed 1st.</td></tr> </tbody> </table>		FPGA bit-stream Nb	0	Single bit push on SPI MOSI with single SPI CLK	1	Eight(8) bits push on SPI MOSI with eight(8) SPI CLK. pgm_SPI_BDAT[7] pushed 1 st .	
	FPGA bit-stream Nb											
0	Single bit push on SPI MOSI with single SPI CLK											
1	Eight(8) bits push on SPI MOSI with eight(8) SPI CLK. pgm_SPI_BDAT[7] pushed 1 st .											
[23:8]	Reserved	R	--	Not implemented								
[31:24]	pgm_SPI_BDAT[7:0]	RW	--	SPI BYTE Data OUT used while BYTE mode used (pgm_SPI_BYTEW = '1')								

1910

3.2.6 Pgm RESET Control

This control register allows to issue an IFC_1211 RESET sequence under control of the T2081.

Following sequence shall be used while the T2081 control is taking control of the IFC_1211 FPGA configuration process.

1915

- Download IO_FPGA configuration bit-stream (from TFTP or local NV memory)
 - Configure the IO_FPGA with the registers “IFCBus_FPGA_CFGCTL” & “IFCBus_FPGA_CFGDAT”
- Download CENTRAL_FPGA configuration bit-stream (from TFTP or local NV memory)
 - Configure the CENTRAL_FPGA with the registers “IFCBus_FPGA_CFGCTL” & “IFCBus_FPGA_CFGDAT”
- Set the control “Seq_CONF_CMD” located in the register “IFCBus_FPGA_CFGCTL”
- Select the PCIe Switch PES32NT24AG2 options in register “IFCBus_PCIE_SW_CTL”
- Generate a Programmed RESET with control bit “Seq_RUN_CMD” located in the register “IFCBus_FPGA_CFGCTL”

1920

1925

This control register can also be used to issue a programmable IFC_1211 RESET without configuring the CEANTRAL_FPGA and IO_FPGA with the field “PGM_RSTCMD[1:0]”

IFCBus_PGMRST IFCBus : 0x002C - 0x002F		IFCBus Programmable RESET				
Bit[]	Function	R/W	Reset	Description	Comments	
[1:0]	T2081_BMOD[1:0]	RW	00	Programmable RESET T2081 Boot Mode. Used only with “PGM_RSTCMD”.		

IFCBus_PGMRST		IFCBus Programmable RESET														
IFCBus : 0x002C - 0x002F																
					<table border="1"> <thead> <tr> <th>T2081_BMOD</th><th>Boot Mode</th></tr> </thead> <tbody> <tr> <td>00</td><td>NOR1 Flash 512Mb (64 MBytes)</td></tr> <tr> <td>01</td><td>NOR2 Flash 128Mb (64 MBytes)</td></tr> <tr> <td>10</td><td>SPI Flash 128Mb (16 MBytes)</td></tr> <tr> <td>11</td><td>Micro SD card</td></tr> </tbody> </table>	T2081_BMOD	Boot Mode	00	NOR1 Flash 512Mb (64 MBytes)	01	NOR2 Flash 128Mb (64 MBytes)	10	SPI Flash 128Mb (16 MBytes)	11	Micro SD card	
T2081_BMOD	Boot Mode															
00	NOR1 Flash 512Mb (64 MBytes)															
01	NOR2 Flash 128Mb (64 MBytes)															
10	SPI Flash 128Mb (16 MBytes)															
11	Micro SD card															
[7:2]	Reserved	R	--	Not implemented												
[8]	PGM_CLKSRC	RW	0	Secondary 100MHz clock fan out buffer LMK00338 input clock selection												
				<table border="1"> <tr> <td>0</td><td>Oscillator CCLD-033-50-100</td></tr> <tr> <td>1</td><td>LMK04803 clock synthesizer CLKout_7</td></tr> </table>	0	Oscillator CCLD-033-50-100	1	LMK04803 clock synthesizer CLKout_7								
0	Oscillator CCLD-033-50-100															
1	LMK04803 clock synthesizer CLKout_7															
[15:9]	Reserved	R	--	Not implemented												
[23:16]	HRESET_CNT[7:0]	R	--	This 8 bit counter tracks the number of T2081 HRESET sequence triggered with : <ul style="list-style-type: none"> T2081_RSTREQ assertion (i.e UBOOT "reset" command). Short_RESET issued with short front-panel handle activation. The counter is RESET at power-up RESET												
[28:24]	Reserved	R	--	Not implemented												
[29]	PGM_ColdRESET	RW	--	IFC_1211 Forced COLDRESET												
				<table border="1"> <tr> <td>0</td><td></td></tr> <tr> <td>1</td><td></td></tr> </table>	0		1									
0																
1																
[31:30]	PGM_RSTCMD[1:0]	W	00	Programmable RESET Command. This 2-bit field define the triggered process. Only applicable when PGM_ColdRESET = '1'.												
				<table border="1"> <thead> <tr> <th>RSTCMD[1:0]</th><th>RESET action</th></tr> </thead> <tbody> <tr> <td>00</td><td>No action</td></tr> <tr> <td>01</td><td>No action, + Enable PES32NT24AG2 RESET</td></tr> <tr> <td>10</td><td>T2081 RESET only</td></tr> <tr> <td>11</td><td>T2081 + PES32NT24AG2 RESET</td></tr> </tbody> </table>	RSTCMD[1:0]	RESET action	00	No action	01	No action, + Enable PES32NT24AG2 RESET	10	T2081 RESET only	11	T2081 + PES32NT24AG2 RESET		
RSTCMD[1:0]	RESET action															
00	No action															
01	No action, + Enable PES32NT24AG2 RESET															
10	T2081 RESET only															
11	T2081 + PES32NT24AG2 RESET															

3.2.7 IFCBus_BMRCTL Register

1930

This Control register allows to supply a programmable synchronisation signal (SYNC) to the three(3) on-board BMR463. Refer to § 2.4.2

- Programmable SYNC (195 – 769 [KHz]) with 20[ns] step resolution.

IFC_BMRCTL		BMR463 Control Register												
Bit[]	Function	R/W	Reset	Description		Comments								
[7:0]	BMR_SYNC_CNT[7:0]	RW	0x00	This eight bit field define the SYNC frequency supplied d to the BMR463		Refer to BMR563 technical doc for valid limit.								
				<table border="1"> <thead> <tr> <th>Value</th> <th>BMR463 SYNC</th> </tr> </thead> <tbody> <tr> <td>X"00"</td> <td>Fixed to '0'</td> </tr> <tr> <td>< X"40"</td> <td>High Impedance</td> </tr> <tr> <td>= X"40"</td> <td>Period = 2*Value*10[ns])</td> </tr> </tbody> </table>		Value	BMR463 SYNC	X"00"	Fixed to '0'	< X"40"	High Impedance	= X"40"	Period = 2*Value*10[ns])	
Value	BMR463 SYNC													
X"00"	Fixed to '0'													
< X"40"	High Impedance													
= X"40"	Period = 2*Value*10[ns])													
[8]	BMR_SYNC_RUN	R		This status is positioned to '1' only if BMR_SYNC_CNT[7:0] >= 0x40										
[31:9]	Reserved	R	0x00	Not used										

1935

3.2.8 IFCBus_I2CDEF Register

This control & status register allows to configure the on-board I2C Master controller infrastructure.

IFC_I2CDEF		I2C Internal Assigmentation										
Bit[]	Function	R/W	Reset	Description		Comments						
[0]	I2C_MAS_MODE[0]	R	b'1'	IFC_1211 on-board I2C/SMBus/PMBus Buses can be controlled from								
				<table border="1"> <thead> <tr> <th>Value</th> <th></th> </tr> </thead> <tbody> <tr> <td>'0'</td> <td>Not valid on IFC1211</td> </tr> <tr> <td>'1'</td> <td>On-board I2C controlled by NEW IFCBus_I2C_#[7:0]</td> </tr> </tbody> </table>		Value		'0'	Not valid on IFC1211	'1'	On-board I2C controlled by NEW IFCBus_I2C_#[7:0]	
Value												
'0'	Not valid on IFC1211											
'1'	On-board I2C controlled by NEW IFCBus_I2C_#[7:0]											
[1]	I2C_MAS_MODE[1]	RW	b'1'	IFC_1211 I2C_P0 Control selection. The PSI Rear_IO I2C/SMBus can be controlled either by the I2C Master controller instantiated in the XUSER_Agent_SW or directly by the individual IFCBus_I2C_#4 Master Controller .								
				<table border="1"> <thead> <tr> <th>Value</th> <th></th> </tr> </thead> <tbody> <tr> <td>'0'</td> <td>P0_I2C controlled by XUSER_Agent_SW</td> </tr> <tr> <td>'1'</td> <td>P0_I2C controlled by IFCBus_I2C_0</td> </tr> </tbody> </table>		Value		'0'	P0_I2C controlled by XUSER_Agent_SW	'1'	P0_I2C controlled by IFCBus_I2C_0	
Value												
'0'	P0_I2C controlled by XUSER_Agent_SW											
'1'	P0_I2C controlled by IFCBus_I2C_0											
[3:2]	Reserved	R	b'0'	Not used								
[4]	T2081_IRQ4_ENA	RW	b'0'	Enable Interrupt generation on T2081 IRQ4								
[5]	T2081_IRQ5_ENA	RW	b'0'	Enable Interrupt generation on T2081 IRQ5								
[31:6]	Reserved	R	b'0'	Not used								

1940

3.2.9 IFCBus_LMK04803_CTL/DAT Registers

This control & status register provides uWIRE access control to the Dual PLL programmable clock synthesizer LMK04803 . Refer to § 2.8.2

IFC_LMKCTL IFCBus : 0x0048 - 0x004B		LMK04803 Control Register														
Bit[]	Function	R/W	Reset	Description		Comments										
[4:0]	SER_ADD[4:0]	RW	0x00	This five bit field defines the LMK04803 device address resource.		Refer to LMK04803 data-sheet.										
[11:5]	Reserved	R	0	Not used												
[12]	LMK_Control_CLKin0_OE	RW	0	LMK04903 programmable status pin												
[13]	LMK_Control_CLKin0	RW	0	LMK04903 programmable status pin												
[14]	LMK_Control_CLKin1_OE	RW	0	LMK04903 programmable status pin												
[15]	LMK_Control_CLKin0	RW	0	LMK04903 programmable status pin												
[18:16]	Reserved	R	0	Not used												
[19]	LMK_VCxo_ON	RW	0b0	Power on VCxo oscillator												
[20]	LMK_Status_LD	R	0b0	LMK04903 programmable status pin												
[21]	LMK_Status_HOLDOVER	R	0b0	LMK04903 programmable status pin												
[22]	LMK_Status_CLKin0	R	0b0	LMK04903 programmable status pin												
[23]	LMK_Status_CLKin1	R	0b0	LMK04903 programmable status pin												
[25:24]	Reserved	R	0b10	Fixed to "10"												
[27:26]	LMK_2CLK_LE[1:0]	RW	0b00	LMK04906 uWIRE Special protocol												
				<table border="1"> <tr> <td>Value</td><td>Device Selection</td></tr> <tr> <td>"0x"</td><td>Standard uWIRE</td></tr> <tr> <td>"10"</td><td>3 extra uWIRE clock with LE = '0'</td></tr> <tr> <td>"11"</td><td>3 extra uWIRE clock with LE = '1'</td></tr> </table>		Value	Device Selection	"0x"	Standard uWIRE	"10"	3 extra uWIRE clock with LE = '0'	"11"	3 extra uWIRE clock with LE = '1'			
Value	Device Selection															
"0x"	Standard uWIRE															
"10"	3 extra uWIRE clock with LE = '0'															
"11"	3 extra uWIRE clock with LE = '1'															
[29:28]	Reserved	R	0b00	Not used												
[31:30]	CMD[1:0]	RW	0	This two bit field allows to trigger the Serial Bus transaction.												
				<table border="1"> <tr> <td>Value</td><td>Command Operation</td></tr> <tr> <td>"00"</td><td>No operation or previous command completed</td></tr> <tr> <td>"01"</td><td></td></tr> <tr> <td>"10"</td><td>READ Operation</td></tr> <tr> <td>"11"</td><td>WRITE Operation</td></tr> </table>		Value	Command Operation	"00"	No operation or previous command completed	"01"		"10"	READ Operation	"11"	WRITE Operation	
Value	Command Operation															
"00"	No operation or previous command completed															
"01"																
"10"	READ Operation															
"11"	WRITE Operation															

1945

IFC_LMKDAT IFCBus : 0x004C - 0x004F		LMK04803 Data Register				
Bit[]	Function	R/W	Reset	Description		Comments
[4:0]	Reserved	R	0	Not used		
[31:5]	uWIRE_DATR[26:0]	RW	0	27-bit uWIRE LMK04906 Read-back		

3.2.10 IFCBus_DS125MB203 Register

This control % status register allows to select/enable the CENTRAL_FPGA MGT225/MGT226 routing conditioned by the 2.1 high speed multiplexer DS125MB203. Refer to § 2.9.3.2

IFC_DS125MB203		DS125MB203 Control Register										
Bit[]	Function	R/W	Reset	Description		Comments						
[0]	mgt225_MUXSEL	RW	0	CENTRAL FPGA MGT225 External 2:1 multiplexer control		DS125MB203 U329, U330						
				<table border="1"> <thead> <tr> <th>Value</th><th></th></tr> </thead> <tbody> <tr> <td>'0'</td><td>MGT226 → VME_P0 A</td></tr> <tr> <td>'1'</td><td>MGT226 → FMC#2 DP[7:4]</td></tr> </tbody> </table>			Value		'0'	MGT226 → VME_P0 A	'1'	MGT226 → FMC#2 DP[7:4]
Value												
'0'	MGT226 → VME_P0 A											
'1'	MGT226 → FMC#2 DP[7:4]											
[1]	mgt225_MUXDWN	RW	1	RESET/Enable DS125MB203 U329, U330		DS125MB203 U329, U330						
				<table border="1"> <thead> <tr> <th>Value</th><th></th></tr> </thead> <tbody> <tr> <td>'0'</td><td>Enables</td></tr> <tr> <td>'1'</td><td>RESET/Power down</td></tr> </tbody> </table>			Value		'0'	Enables	'1'	RESET/Power down
Value												
'0'	Enables											
'1'	RESET/Power down											
[3:2]	Reserved	R	00	Not used								
[4]	mgt226_MUXSEL	RW	1	CENTRAL FPGA MGT226 External 2:1 multiplexer control		DS125MB203 U327, U331						
				<table border="1"> <thead> <tr> <th>Value</th><th></th></tr> </thead> <tbody> <tr> <td>'0'</td><td>MGT226 → VME_P0 A</td></tr> <tr> <td>'1'</td><td>MGT226 → PCIe Switch 32NT24 Port_20</td></tr> </tbody> </table>			Value		'0'	MGT226 → VME_P0 A	'1'	MGT226 → PCIe Switch 32NT24 Port_20
Value												
'0'	MGT226 → VME_P0 A											
'1'	MGT226 → PCIe Switch 32NT24 Port_20											
[5]	mgt226_MUXDWN	RW	1	RESET/Enable DS125MB203 U327, U331		DS125MB203 U327, U331						
				<table border="1"> <thead> <tr> <th>Value</th><th></th></tr> </thead> <tbody> <tr> <td>'0'</td><td>Enables</td></tr> <tr> <td>'1'</td><td>RESET/Power down</td></tr> </tbody> </table>			Value		'0'	Enables	'1'	RESET/Power down
Value												
'0'	Enables											
'1'	RESET/Power down											
[7:6]	Reserved	R	00	Not used								
[31:8]	Reserved	R	0x00	Not used								

3.2.11 NEW I2C/SMBus/PMBus Master Controller

A dedicated I2C master controller is instantiated for each I2C bus. Each I2C master controller provides an interrupt output, and all the interrupts are routed directly to T2081 IRQ4#.

The new I2C master controller core logic managing the I2C/SMBus protocol is compatible with the I2C module integrated into a wide range of NPX/FreeScale PowerPC processors.

Following table sums up the new Individual IFCBus I2C/SMBus/PMBus Master Controller assignation

I2C_MAS Port#	IFCBusReg.	Bus #	Devices connected
#0	0x0080-0x008F	Bus_0	VME_P0
#1	0x0090-0x009F	Bus_1	Emulated BOOT Sequencer, Emulated System_ID, LM95235, RTC
#2	0x00A0-0x00AF	Bus_2	MAX5970, BMR463s, PES32NT24AG2, DS125MB203s
#3	0x00B0-0x00BF	Bus_3	FMC1, FMC2, XMC
#4	0x00C0-0x00CF	Bus_4	PCIe Expansion XMP_1262

Table 3.3.: IFC_1211 New IFCBus_I2C implemented I2C/SMBus/PMBus Devices

1960

Note The I2C_Bus[4.1] can also be controlled by the T2081 embedded I2C modules. Refer to § 2.10

1965

3.2.11.1 MPC Compatible Register Mapping

All NPX/Freescale MPC-compatible registers are 8-bit wide. They are packed into four(4) 32-bit IFCBus registers as follows :

IFCBus_Reg. Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x00	CR	DFSRR (not supported)	FDR	ADR (not supported)
0x04	Reserved	Reserved	Reserved	SR
0x08	Reserved	Reserved	Reserved	DR
0x0C	I2C controller revision (Day/Month/Year/Index)			

1970

The functionality of the MPC registers is described in NPX/FreeScale Reference Manuals, chapter "I2C Module". Please refer to those manuals for more information on how to use the I2C controller from the software side.

1975

3.2.11.2 Unsupported Features

Some of the NPX/Freescale I2C module features are currently not supported:

1980

- Slave mode: the controller supports only the master mode of operation. There is no other I2C bus master on the IFC_1211, supporting the slave mode of operation has no purpose;
- Digital filter sampling: the current implementation of the I2C controller performs a single data capture on the rising edge of the clock signal. Future implementations may support over-sampling.

1985

3.2.12 T2081 IFC_Bus → VME64x Master Direct Path

The T2081 IFC Bus to VME Direct Path is managed through three control & status registers. Refer to § 2.11.2

IFC_VMEDIRP_CTL IFCBus : 0x0054 - 0x0057		IFCBus VME Direct Control & Status				
Bit[]	Function	R/W	Reset	Description		Comments
[0]	ifc_VMEDIRP_RERR_FF	RWc	0	VME Read with BERR# detected flag. Flag reset by writing '1' over it.		
[1]	ifc_VMEDIRP_WERR_FF	RWc	0	VME Write with BERR# detected flag. Flag reset by writing '1' over it.		
[27:2]	Reserved	R	0	Not used		
[28]	ifc_VMEDIRO_WPOST	RW	0	VME 1 stage Write Posting		
				0	Write posting disabled	
				1	Write posting enabled	
[30:29]	ifc_VMEDIRP_RTY[1:0]	RW	0	VME RETRY policy.		
				00	Abort the transaction with Error	
				01	Retry the transaction 256x	
				10	Retry indefinite	
				11	To Be defined	
[31]	ifc_VMEDIRP_ENA	RW	1	Enable Read path		

Following two IFCBus registers are defined for IFC_INgress MMU initialization.

IFC_VMEDIRP_MMUADD IFCBus : 0x0058 - 0x005B		IFCBus VME Direct MMU Address Pointer				
Bit[]	Function	R/W	Reset	Description		Comments
[0]	IFC_INgress_MMU_ADD0	RW	0	Selection of Low/High word of IFC_INgress Page Descriptor.		
[6:1]	IFC_INgress_MMU_ADD[6:1]	RW	0	IFC_INgress MMU DPRAM Address Pointer.		
[31:7]	Reserved	R	0	Not used		

1990

IFC_VMEDIRP_MMUDAT IFCBus : 0x005C - 0x005F		IFCBus VME Direct MMU Data				
Bit[]	Function	R/W	Reset	Description		Comments
[17:0]	IFC_INgress_MMU_DAT[17:0]	RW	0	IFC_INgress MMU Data		
[31:18]	Reserved	R	0	Not used		



VME64x IFC_1211 HW Technical User Guide

IFC1211_HW_UG_A0

Preliminary

1995

3.2.13 T2081 Direct INT0# Generator

The PON_FPGA is able to control directly the the T2081 IRQ4 and IRQ5 inputs. To provide most efficient real-time capabilities of the NEW individual I2C Master Controller, a Simple dedicated Interrupt Management has been added for this purpose.

- Eight(8) I2C_Master Controller INTOK
- Eight(8) I2C_Master Controller INTERR
- CRITn signal from LM95235 Thermometer
- ALERTn signal from the BMR463 DCDC and MAX5970
- VME64x Direct Path exception. (To Be Defined)

These three control & status registers supports the T2081 IRQ4/5 interrupt handling.

3.2.13.1 IFCBus_T2081 IRQ4/5 Mask Register

This register provides individual Interrupt masking.

T2081_IRQ4_IMSK IFCBus : 0x0070 - 0x0073		IRQ4/5 Interrupt Mask				
Bit[]	Function	R/W	Reset	Description	Comments	
[0]	I2C_MC_0_MSK_INTOK	RW	'1'	INT Mask. While set, current IT does not activate T2081 IRQ4/IRQ5.	Edge Interrupt	
[1]	I2C_MC_0_MSK_INTERR	RW	'1'	INT Mask. While set, current IT does not activate T2081 IRQ4/IRQ5..	Edge Interrupt	
[2]	I2C_MC_1_MSK_INTOK	RW	'1'		Edge Interrupt	
[3]	I2C_MC_1_MSK_INTERR	RW	'1'		Edge Interrupt	
[4]	I2C_MC_2_MSK_INTOK	RW	'1'		Edge Interrupt	
[5]	I2C_MC_2_MSK_INTERR	RW	'1'		Edge Interrupt	
[6]	I2C_MC_3_MSK_INTOK	RW	'1'		Edge Interrupt	
[7]	I2C_MC_3_MSK_INTERR	RW	'1'		Edge Interrupt	
[8]	I2C_MC_4_MSK_INTOK	RW	'1'		Edge Interrupt	
[9]	I2C_MC_4_MSK_INTERR	RW	'1'		Edge Interrupt	
[10]	I2C_MC_5_MSK_INTOK	RW	'1'		Edge Interrupt	
[15:11]	Reserved	RW	'1'		Edge Interrupt	
[16]	CRIT_MSK_INTERR	RW	'1'		Level Interrupt	
[17]	ALERT_MSK_INTERR	RW	'1'		Level Interrupt	
[31:18]	Reserved	R	'0'	Not used		

3.2.13.2 IFCBus_T2081 IRQ4/5 Pending Register

This register provides individual Interrupt Pending.

T2081_IRQ4_IP IFCBus : 0x0070 - 0x0074		IRQ4 Interrupt Pending				
Bit[]	Function	R/W	Reset	Description	Comments	
[0]	I2C_MC_0_IP_INTOK	R	-	Interrupt Pending status		

T2081_IRQ4_IP		IRQ4 Interrupt Pending				
IFCBus : 0x0070 - 0x0074						
[1]	I2C_MC_0_IP_INTERR	R	-	Interrupt Pending status		
[2]	I2C_MC_1_IP_INTOK	R	-			
[3]	I2C_MC_1_IP_INTERR	R	-			
[4]	I2C_MC_2_IP_INTOK	R	-			
[5]	I2C_MC_2_IP_INTERR	R	-			
[6]	I2C_MC_3_IP_INTOK	R	-			
[7]	I2C_MC_3_IP_INTERR	R	-			
[8]	I2C_MC_4_IP_INTOK	R	-			
[9]	I2C_MC_4_IP_INTERR	R	-			
[15:10]	Reserved	R	-			
[16]	CRIT_IP_INTERR	R	-			
[17]	ALERT_IP_INTERR	R	-			
[31:18]	Reserved	R	-			

2015

3.2.13.3 IFCBus_T2081 IRQ4/5 Clear Command INT Register

This register provides individual Interrupt Clear command. The I2C Master Controller issue pulsed interrupt, latched by the interrupt pending FF. This latch/FF shall be cleared individually

T2081_IRQ4_ICLR		IRQ4 Interrupt Clear Command				
IFCBus : 0x0078 - 0x007B						
Bit[]	Function	R/W	Reset	Description	Comments	
[0]	I2C_MC_0_ICLR_INTOK	Wo	-	While '1', clear the IP FF, '0' does not clear it.		
[1]	I2C_MC_0_ICLR_INTERR	Wo	-	While '1', clear the IP FF, '0' does not clear it.		
[2]	I2C_MC_1_ICLR_INTOK	Wo	-			
[3]	I2C_MC_1_ICLR_INTERR	Wo	-			
[4]	I2C_MC_2_ICLR_INTOK	Wo	-			
[5]	I2C_MC_2_ICLR_INTERR	Wo	-			
[6]	I2C_MC_3_ICLR_INTOK	Wo	-			
[7]	I2C_MC_3_ICLR_INTERR	Wo	-			
[8]	I2C_MC_4_ICLR_INTOK	Wo	-			
[9]	I2C_MC_4_ICLR_INTERR	Wo	-			
[15:10]	Reserved	R	-	Nit used		
[16]	Reserved	R	'0'	Not used, CRITn is level interrupt.		
[17]	Reserved	R	'0'	Not used, ALERTn is level interrupt.		
[31:18]	Reserved	R	'0'	Not used		

2020

4. Annexes

4.1 IFC_1210 → IFC1211 Migration

The IFC_1211 has been designed with target to be as close as possible to the IFC_1210 but with a number of key improvements identified in following sub-sections.

2025

4.1.1 Key IFC_1210 / IFC_1211 Improvements

Following sub-sections sums up IFC_1211 key improvements compared to 1st generation IFC_1210.

2030

4.1.1.1 NPX/Freescale T2081

The IFC_1211 is based on NPX/Freescale T2081 CPU, providing major computing performance improvement compared to the IFC_1210 P2020.

2035

- QorIQ T2081 operating at 1.8 GHz (QorIQ P2020 at 1.2 GHz)
- Quad core E6500 with true hardware based FPU
- ALTIVEC vectorial unit
- Dual independent PCIe_x4 Gen3/Gen2 RC Interfaces
- System Memory 2 GBytes 64-bit+ ECC DDR3-2133 (DDR3-1200)

2040

4.1.1.2 XILINX ARTIX-7 Family

The IFC_1211 implements XILINX ARTIX-7 family for PON_FPGA and IO_FPGA.

2045

- Higher performance FPGA family (level similar to VIRTEX-6 level)
- Embedded PCIe Gen2 IPcore

4.1.1.3 XILINX KINTEX-7 Ultrascale Family

The IFC_1211 implements XILINX KINTEX-7 family for PON_FPGA and IO_FPGA.

2050

- Higher performance higher-density FPGA
- Three PCIe IPcore Gen3 support

2055

4.1.1.4 TOSCA IIA Infrastructure

The TOSCA IIA infrastructure is optimized for XILINX ARTIX-7 family. It is used on IFC_1211 PON_FPGA and optionally in IO_FPGA. Both are based on XILINX ARTIX-7 XC7A75.

2060

- Dual full mesh non-blocking switch 64-bit @ 200-250 MHz
- Switch infrastructure for up to four(4) TOSCA II Agent_SW
 - 1x Agent_SW PCI Express EP x4 Gen2
 - 1x Agent_SW VME64x Master/Slave. (only in PON_FPGA)
 - 1x Agent_SW SMEM DPRAM with dual channel IDMA

- 1x Agent_SW USER
- PON_FPGA Agent_SW USER integrates IOxOS generic control and T2081 IFC_Bus mapped resources. Refer to § 2.9.1
- IO_FPGA Agent_SW USER integrates user application specific based on XUSER framework, with direct access to VME_P2 and JN14 user IO. Refer to § 2.9.2

4.1.1.5 TOSCA III Infrastructure

The TOSCA III infrastructure is optimized for KINTEX-7 family. It is used on IFC_1211 CENTRAL_FPGA based on XILINX KINTEX-7 Ultrascale XCKU040.

- Dual full mesh non-blocking switch 128/64-bit @ 250-3000 MHz
- Switch infrastructure for up to eight(8) TOSCA II Agent_SW
 - 1x-3x Agent_SW PCI Express EP x4 Gen3
 - 1x Agent_SW SMEM DDR3 with dual channel IDMA
 - 1x-2x Agent_SW SMEM DPRAM with dual channel IDMA
 - 2x Agent_SW USER
- CENTRAL_FPGA Agent_SW USER integrates user application specific based on XUSER/SUSER framework, with direct access to VITA57.1 FsMC. Refer to § 2.9.3

2080

4.1.1.6 PCIe_x4 Gen3 Interface to CENTRAL_FPGA

IFC_1211 CENTRAL_FPGA XILINX KINTEX-7 Ultrascale XCKU040 is connected to the T2081 with a private PCI Express x4 Gen3. (T2081 PCIe4) Refer to § 2.9.3

2085

- Lower latency for single beat T2081 Read/Write CENTRAL_FPGA
- Up to 4 GBytes/s sustained bandwidth under DMA control
- Optional connection through the PCI Express Switch PES32NT24AG2

4.1.1.7 PCIe_x2 Gen2 Interface to IO_FPGA

2090

IFC_1211 IO_FPGA XILINX ARTIX-7 XC7A75, handling VME_P2 and XMC/PMC JN14 user IO, is also connected to the T2081 through the PCI Express Switch PES32NT24AG2 Port_04. Refer to § 2.9.2

IFC_1211 IO_FPGA is also connected to the CENTRAL_FPGA with HSI Interface. Refer to § 2.9.2.3

- New generation FPGA supporting VME_P2 and XMC/PMC JN14 user IO
- 800 MHz HSI 8-bit bidirectional interface with CENTRAL FPGA
- PCI Express x2 Gen2 interface to on chip TOSCA IIA infrastructure
- SUSER/XUSER supports for Application specific

2100

4.1.1.8 LMK04803 for on-board CLOCK Synthesiser

The IFC_1211 integrates a Dual PLL programmable clock synthesizer LMK04803. Refer to § 2.8.2

- Low noise VCO 2000 MHz
- Very low jitter (<125[fs])
- Six(2) group of programmable clock up to 1000MHz

- Programmable digital delay (250[ps]/step) + Analog delay (25[ps]/step)
- On-board 100 MHz VCXO
- External clock reference available on front-panel SSMC

2110

4.1.1.9 ALTHEA based PCIe-VME64x Bridge

The IFC_1211 VME64x is built on top of IOxOS “ALTHEA PCI Express to VME64x Bridge”. This latest declination of PCIe-VME64x Bridge is also used by several others VME manufacturer in replacement of the TSI148 device. ALTHEA bridge function has been improved with following capabilities

2115

- VME Master with AM code for Program/Data, User/Supervisor mode
- VME Master controlling D32 → 2x D16 access
- VME Master/Slave 2eSST Broadcast

2120

- VME Slave windows A24, A16 with INgress MMU scatter-gather
- Control bits VTON/VTOFF for TSI148 compatibility
- Optional SMEM built with embedded FPGA DPRAM
- IDMA Pipeline_2 for direct PCIe ↔ VME64x without intermediate copy in SMEM
- Eight(8) Message passing FIFO + eight(8) Semaphores

2125

4.1.1.10 T2081 → VME Master Direct Path

The IFC_1211 provides a low latency direct path from the T2081 to VME64x Master interface. This additional path is running in parallel of standard “ALTHEA PCI Express to VME64x Bridge” and then by-pass the inherent latency of the on-board PCI Express infrastructure.

- Direct path T2081 IFC_Bus GPCM → VME64x Master controller.
- Single beat D08, D16, D32 Read/Write access
- Low latency T2081 ← VME Read transaction (< 500[ns])

2135

4.1.1.11 XMP_1262 Expansion

The IFC_1211 provides the support for a dual XMC/FMC expansion. (XMP-1262). This expansion capability is provided on a standard VME64x board with high speed PCI Express interconnect. Refer to § 2.7.8

2140

4.1.1.12 I2C/SMBus Infrastructure

The IFC_1211 on-board I2C/SMBus is composed of five(5) independent SMBus. Four of them can be controller either by T2081 I2C controller or by I2C controller embedded in the PON_FPGA (backward compatible with IFC_1210). Refer to 4.1.1.12

2145

4.1.1.13 Others

- ...

2150

4.1.2 Major IFC_1210 / IFC_1211 Differences

4.1.2.1 Single XMC/PMC Slot

2155

The IFC_1211 provides a single XMX/PMC mezzanine slot (IFC1210 provides two(2)

For application requiring more than one XMC/FMC, the IFC_1211 can be attached to a XMP_1262 unit , providing three(3) XMC/PMC slots in a dual 6U VME slots. Refer to § 2.7.8

4.1.2.2 Front Panel SSMC

2160

The IFC_1211 provides two front panel SSMC connectors.

- SSMC#1 → AC coupled (balloon) clock reference for Dual PLL programmable clock synthesizer LMK04803. Refer to 2.8.2
- SSMC#2 → GPIO isolated LVTTL to/from CENTRAL_FPGA

2165

4.1.2.3 IO_FPGA ↔ CENTRAL_FPGA HSI 8-bit

The HSI interface allowing to control remotely the VME_P2 and XMC/PMC JN14 from the CENTRAL_FPGA has been re-dimensioned due to XILINX XCKU040 IO pins limitation. The HSI data bus width has been reduced from 16-bit to 8-bit.

2170

For user application built on top of IOxOS HSI Bridge with ISERDES/OSERDES the migration is fully transparent because the IFC_1211 HSI bridge operates at 800 MHz.

For user application built with custom re-definition of HSI signalling following work-around can be used.

2175

- (a) Seven interconnect are available (not used) between CENTRAL_FPGA and IO_FPGA. Those signals can be allocated to custom re-definition
- (b) Thanks to higher bandwidth HSI CENTRAL_FPGA ↔ IO_FPGA point to point signalling, HSI Data Bus can be interfaced with ODDR and IDDR IO cell, virtually providing HSI 16.bit data interface. IOxOS will supply such implementation example.
- (c) IFC_1211 IO_FPGA can be configured with a TOSCA IIA infrastructure, with PCI Express EP Gen2 interface. Complete XUSER AP specific with direct access to VME_P2 and JN14 user IO can be fitted in the IO_FPGA.

2185

2190



4.2 JN15 - IO_FPGA – VME_P2 Array

Add PCB layout image of 64x dual 0603 footprint for user customisation.

Add differential signalling allocation.

2195

2200

[EOF] 29/09/16 08:53:57