Microcontroller, CPLD, USB, Power

File: mcu.kicad_sch

Clock

File: clock.kicad_sch

Baseband

File: baseband.kicad_sch

Front End

File: frontend.kicad_sch

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Sheet: /
File: hackrf-one.kicad_sch

Title: HackRF One

Size: USLedger	Date: 2022-10-30	**Rev: r9**
KiCad E.D.A. kicad 6.0.10-86aedd382b~118~ubuntu22.04.1		Id: 1/5

Cortex Debug Connector (10 pin 50 mil)

pin straps for hardware version detection

Do not raise VBUSCTRL unless VIN is supplied.

See also I2S0 pins on P20.

U23 starts up on this 12 MHz crystal. This makes it possible to use USB0 DFU boot mode. It should be possible to switch to GP_CLKIN provided by the clock generator IC (MCU_CLK) if desired.

Default boot configuration is SPIFI. Press SW1 during reset to switch to USB0 (DFU mode).

Boot selection:

	P2_9	P2_8	P1_2	P1_1
USART0	GND	GND	GND	GND
SPIFI	GND	GND	GND	VCC
USB0	GND	VCC	GND	VCC
SSP0	GND	VCC	VCC	VCC
USART3	VCC	GND	GND	GND

Series resistors are here because of a possible overshoot/undershoot problem. They may be able to be removed safely. Anyway, they probably will minimize damage in the event of SGPIO/CPLD misconfiguration.

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Sheet: /Microcontroller, CPLD, USB, Power/
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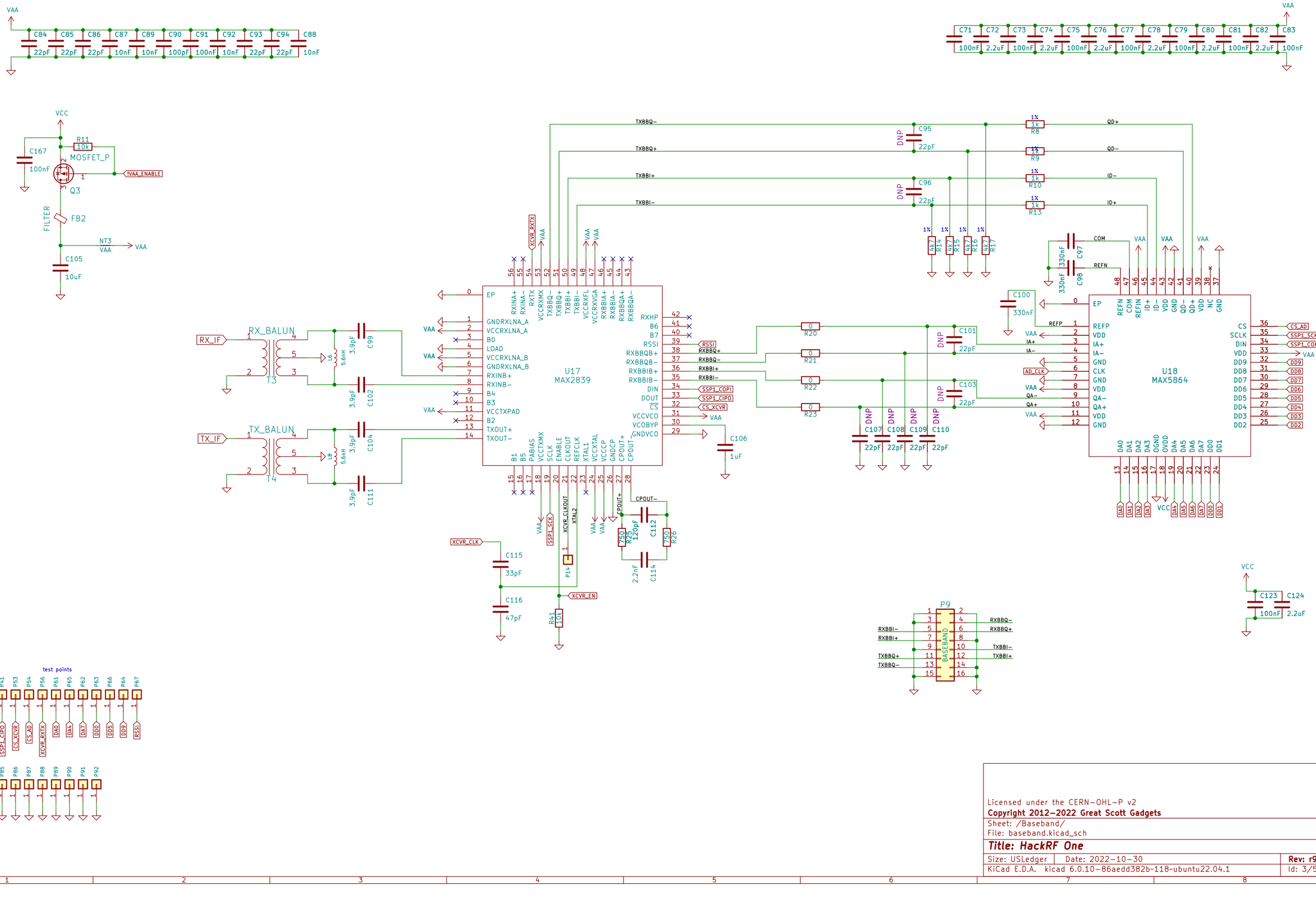
Size: USLedger	Date: 2022-10-30	Rev: r9
KiCad E.D.A. kicad 6.0.10-86aedd382b-118-ubuntu22.04.1		Id: 2/5



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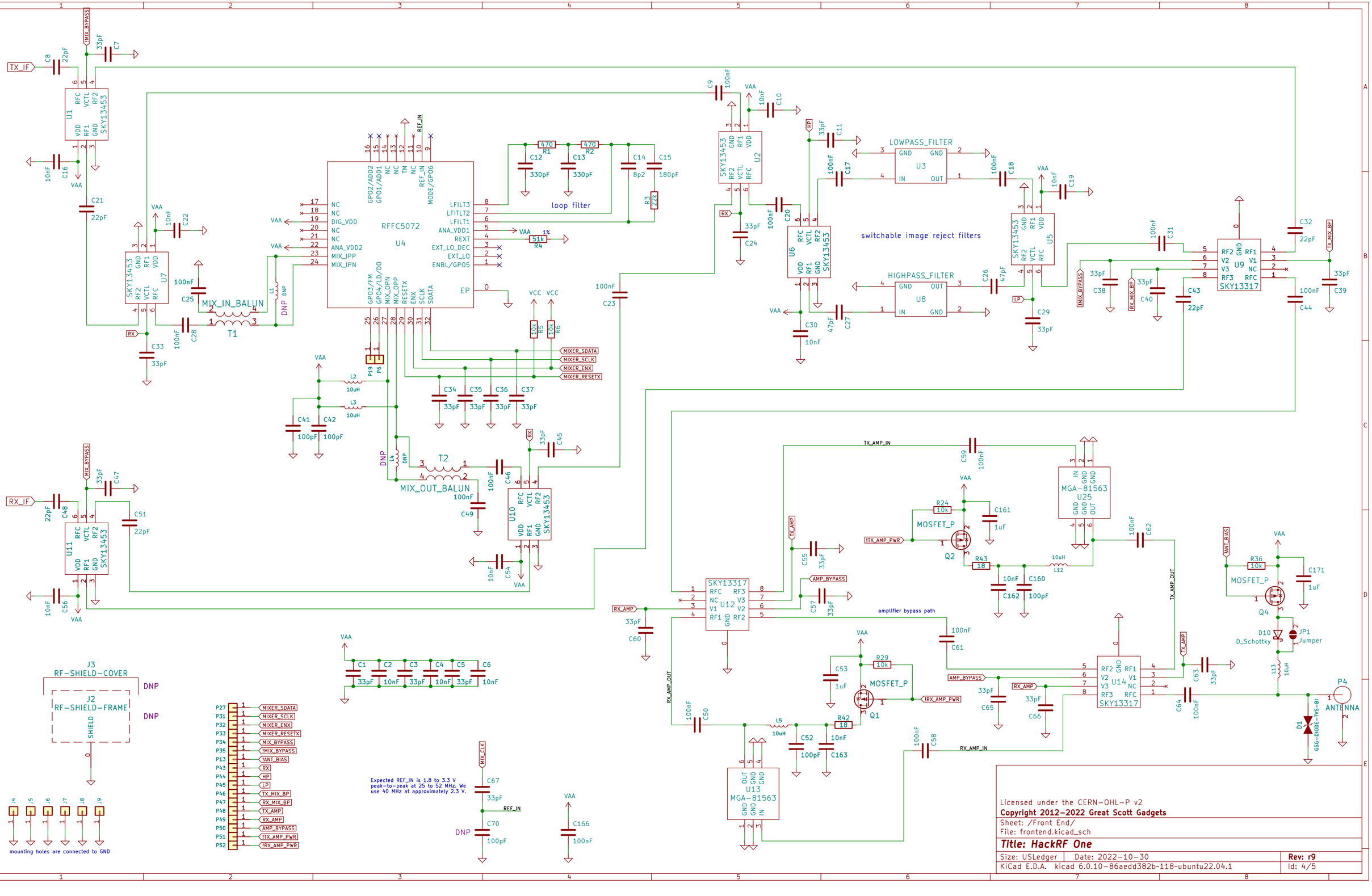
Sheet: /Baseband/
File: baseband.kicad_sch

Title: HackRF One

Size: USLedger	Date: 2022−10−30	**Rev: r9**
KiCad E.D.A. kicad 6.0.10−86aedd382b~118~ubuntu22.04.1		Id: 3/5


TX_IF
MIX_BYPASS
U1
SKY13453
RFC
VCTL
RF2
VDD
RF1
GND
VAA
RFFC5072
U4
MIX_IN_BALUN
T1
DNP
loop filter
switchable image reject filters
LOWPASS_FILTER
HIGHPASS_FILTER
U3
U8
U5
U6
U7
U2
U9
SKY13317
MIXER_SDATA
MIXER_SCLK
MIXER_ENX
MIXER_RESETX
MIX_OUT_BALUN
T2
U10
U11
RX_IF
J3
RF-SHIELD-COVER
J2
RF-SHIELD-FRAME
SHIELD
mounting holes are connected to GND
Expected REF_IN is 1.8 to 3.3 V peak-to-peak at 25 to 52 MHz. We use 40 MHz at approximately 2.3 V.
TX_AMP_IN
RX_AMP_OUT
RX_AMP_IN
amplifier bypass path
TX_AMP_OUT
U12
U13
U14
MGA-81563
Q1
Q2
Q4
MOSFET_P
D10
D_Schottky
JP1
Jumper
D1
GSG-DIODE-TWS-BI
ANTENNA
P4
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Sheet: /Front End/
File: frontend.kicad_sch
Title: HackRF One
Size: USLedger
Date: 2022-10-30
Rev: r9
KiCad E.D.A. kicad 6.0.10-86aedd382b-118-ubuntu22.04.1
Id: 4/5

3.3 V CMOS clock input at 10 MHz
(or 10 MHz to 40 MHz with firmware modification)

P16
CLKIN

D3
GSG-DIODE-TVS-BI

C159
100nF

R61
10k

R85
10k

C165
DNP
33pF

U26
74AUP2G58GU

CLKIN_EN

R39
39

R40
DNP

C117
33pF

C156
100pF

CLKIN_DETECT
R38
39

R105
10k

U16
74LVC1G3157

X1
MAIN_XTAL

1.8pF
DNP
C169

1.8pF
DNP
C170

P37
P38
R27
1k8
R28
1k8

SCL
SDA

U19
SI5351A-B-GT

R44
39

R45
0

R50
39
R53
39

MIX_CLK
XCVR_CLK

FSX2_CLK

R71
DNP

C172
22pF

R83
0
R84
0
DNP

U27
74AUP2G58GU

R92
0
R95
0
DNP
R97
0
DNP
R101
0
DNP
R102
0
DNP
R103
0
DNP
R104
0
DNP
R106
0

XCVR_RXTX
inverted
GCK2

U29
74AUP2G58GU
DNP

R107
39
DNP
R94
39

SGPIO_CLK

R60
100
/2
AD_CLK
R31
100
/2
GCK1

U22
74LVC1G80

sample rate clocks:
AD_CLK, GCK1

2x sample rate clocks:
CLK1, FSX2_CLK, GCK2, SGPIO_CLK

P72

MCU_CLK_EN
R34
39
MCU_CLK

U28
74AUP2G58GU

3.3 V CMOS clock output at 10 MHz
(or other frequency with firmware modification)

CLKOUT_EN
R33
39

CLKOUT

D9
GSG-DIODE-TVS-BI

P2
CLKOUT

P21
P57
P1
P59
P60
P8

MIX_CLK
XCVR_CLK
GCK1
GCK2
SGPIO_CLK
FSX2_CLK

C168
C68
C69
C113
C119
C120
C121
C122
100nF

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Sheet: /Clock/
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