Result of using Yosys to convert to NANDs for various softcores

core name	options	NANDs	
darkriscv		50424	
glacial		2063	
serv		3595	
picorv32		34463	
vexriscv	MinDebugCache	49214	
Hazard3	1 port	42042	
Hazard3	2 ports	41790	

non RISC-V:

core name	options	NANDs	
femto8		1730	
femto16		6827	
zpu_avalanche		7997	
j0 (gameduino)		20998	
j0	no mult (16 stk)	10616	
ukp (nestang)		3961	includes code ROM
MCPU		425	
6502 (nestang)		4891	
cray1		303823	Includes 9 hard_v_reg, 65 latches
MiniCPU_SerPCU		1105	
MiniCPU_SerALU		1269	
	PCU+ALU	2374	

Baby 8 blocks

logic function	98
ALU	280
datapath	3024
test	178
decode	29
cmux	52
fsm2control	167

Result of synth_ice40 in Yosys for various softcores

core name	options	total cells	flip-flops	LUT4	CARRY	TBUF	RAM40_4K	
darkriscv		7777	2262	5176	339	0	0	
glacial		355	84	224	47	0	0	
serv		450	201	241	8	0	0	
picorv32		2683	596	1678	405	0	4	
vexriscv	MinDebugCache	2627	991	1534	96	0	6	
Hazard3	1 port	4187	507	3330	346		4	
Hazard3	2 ports	4170	506	3314	346		4	

non RISC-V:

core name	options	total cells	flip-flops	LUT4	CARRY	TBUF	RAM40_4K	
femto8		364	55	257	52	0	0	
femto16		1398	194	1038	166	0	0	
zpu_avalanche		1651	272	1307	72	0	0	
j0 (gameduino)		942	67	782	91	0	2	
j0	no mult (16 stk)	590	65	445	78	0	2	
ukp (nestang)		494	151	272	68	2	1	
MCPU		79	24	35	12	8	0	
6502 (nestang)		936	123	754	59	0	0	
cray1		37355	8510	25769	3057	0	19	9 hard_v_reg
MiniCPU_SerPCU		157	51	106	0	0	0	
MiniCPU_SerALU		176	49	127	0	0	0	
	PCU+ALU	333	100					

Baby 8 blocks		total cells	flip-flops	LUT4	CARRY	TBUF	RAM40_4K

logic function	8		8	
ALU	36		28	8
datapath	391	136	247	8
test	21	8	13	
decode	9		9	
cmux	14		14	
fsm2control	40		40	

Result of synth_efinix in Yosys for various softcores

core name	options	total cells	flip-flops	LUT4	ADD	MISC	RAM_5K	
darkriscv		7543	2262	4905	375	1	0	
glacial		331	84	186	60	1	0	
serv		401	164	225	11	1	0	
picorv32		2321	565	1308	443	1	4	
vexriscv	MinDebugCache	2549	991	1440	111	1	6	
Hazard3	1 port	3985	538	3058	383	2	4	
Hazard3	2 ports	3951	537	3025	383	2	4	

non RISC-V:

core name	options	total cells	flip-flops	LUT4	ADD	MISC	RAM_5K	
femto8		329	55	204	69	1	0	
femto16		1272	194	884	193	1	0	
zpu_avalanche		1558	272	1203	82	1	0	
j0 (gameduino)		834	33	671	127	1	2	
j0	no mult (16 stk)	527	31	388	105	1	2	
ukp (nestang)		452	151	196	101	3	1	
MCPU		77	24	27	17	9	0	
6502 (nestang)		873	123	674	75	1	0	
cray1		35440	8511	23348	3562	1	18	9 hard_v_reg
MiniCPU_SerPCU		155	51	103	0	1	0	
MiniCPU_SerALU		174	49	124	0	1	0	
	PCU+ALU	329	100					

Baby 8 blocks		total cells	flip-flops	LUT4	ADD	MISC	RAM_5K

logic function	8		8		
ALU	30		20	10	
datapath	391	136	244	10	1
test	22	8	13		1
decode	9		9		
cmux	13		13		
fsm2control	40		40		

Result of synth_gowin in Yosys for various softcores

core name	options	total cells	flip-flops	MISC	ALU	LUT	MuxLUT	RAM16S4
darkriscv		9032	142	176	355	5198	3105	56
glacial		753	84	41	55	351	222	0
serv		1083	201	207	12	452	211	0
picorv32		4039	567	411	424	2009	596	32
vexriscv	MinDebugCache	3692	1038	363	105	1762	377	47
Hazard3	1 port	12196	602	343	366	7045	3808	32
Hazard3	2 ports	11220	601	463	336	6483	3305	32

non RISC-V:

core name	options	total cells	flip-flops	MISC	ALU	LUT	MuxLUT	RAM16S4
femto8		1514	55	29	62	771	597	0
femto16		3240	194	55	182	1780	1029	0
zpu_avalanche		3930	272	104	78	2053	1423	0
j0 (gameduino)		2064	35	78	112	1245	578	16
j0	no mult (16 stk)	4250	31	78	91	2163	1879	8
ukp (nestang)		986	151	29	89	477	240	0
MCPU		187	24	20	15	90	38	0
6502 (nestang)		1833	123	41	68	1100	501	0
cray1		0 D latches not supported						
MiniCPU_SerPCU		167	51	19	0	84	13	0
MiniCPU_SerALU		407	49	14	0	217	127	0
	PCU+ALU	574	100					

Baby 8 blocks		total cells	flip-flops	MISC	ALU	LUT	MuxLUT	RAM16S4

					gowin		
logic function	34		26		8		
ALU	106		35	9	40	22	
datapath	193	8	87	9	57	28	4
test	126	8	13		57	48	
decode	45		26		14	5	
cmux	100		23		41	36	
fsm2control	314		62		137	115	

Result of synth_intel_alm -family cyclonev in Yosys for various softcores

core name	options	total cells	flip-flops	MISC	ALU	LUT	M18x18	M27x27	memories	mem type
darkriscv		1891	162	178	365	1057	1	0	128	mlab
glacial		328	84	42	58	144	0	0	0	
serv		641	204	209	27	201	0	0	0	
picorv32		2322	608	413	431	868	0	0	2	m10k
vexriscv	MinDebugCache	2405	944	191	84	1158	0	0	28	mlab+ 3 m10k
Hazard3	1 port	3705	540	375	413	2375	0	0	2	m10k
Hazard3	2 ports	3948	539	495	413	2499	0	0	2	m10k

non RISC-V:

core name	options	total cells	flip-flops	MISC	ALU	LUT	M18x18	M27x27	memories	mem type
femto8		331	55	28	46	202	0	0	0	
femto16		1028	194	56	169	609	0	0	0	
zpu_avalanche		1331	272	109	79	871	0	0	0	
j0 (gameduino)		558	67	77	100	311	1	0	2	m10k
j0	no mult (16 stk)	540	39	77	95	297	0	0	32	mlab
ukp (nestang)		561	155	31	100	275	0	0	0	
MCPU		93	24	28	15	26	0	0	0	
6502 (nestang)		704	123	41	68	472	0	0	0	
cray1		0 D latches not supported								
MiniCPU_SerPCU		139	51	22	0	66	0	0	0	
MiniCPU_SerALU		167	49	14	0	104	0	0	0	
	PCU+ALU	306	100							

Baby 8 blocks		total cells	flip-flops	MISC	ALU	LUT	M18x18	M27x27	memories	mem type

			cyclonev			
logic function	34		26		8	
ALU	63		33	10	20	
datapath	149	8	86	10	29	16 mlab
test	33	8	13		12	
decode	34		25		9	
cmux	31		22		9	
fsm2control	90		61		29	

Result of synth_xilinx -flatten in Yosys for various softcores (default family is xc7)

core name	options	total cells	flip-flops	MISC	CARRY4	LUT	MuxLUT	DSP48	memories	mem type
darkriscv		2506	150	281	68	1428	498	1	80	RAM32x1D+RAM32M(16)
glacial		298	84	44	15	139	16	0	0	
serv		650	201	207	4	212	26	0	0	
picorv32		2447	572	657	97	1038	67	0	16	RAM32M
vexriscv	MinDebugCache	2758	914	453	28	1260	100	0	3	RAMB18E1+RAM36E1(1)
Hazard3	1 port	5006	612	1001	93	2799	485	0	16	RAM32M
Hazard3	2 ports	5431	611	1118	93	2967	626	0	16	RAM32M

non RISC-V:

core name	options	total cells	flip-flops	MISC	CARRY4	LUT	MuxLUT	DSP48	memories	mem type
femto8		267	55	52	20	133	7	0	0	
femto16		1071	194	118	50	635	74	0	0	
zpu_avalanche		1307	272	105	21	754	155	0	0	
j0 (gameduino)		797	43	110	24	397	190	1	32	RAM32x1D
j0	no mult (16 stk)	683	39	107	19	315	171	0	32	RAM32x1D
ukp (nestang)		527	159	71	25	213	58	0	1	RAMB18E1
MCPU		101	24	35	5	36	1	0	0	
6502 (nestang)		780	123	43	14	520	80	0	0	
cray1		25005	6803	1056	811	15406	661	11	257	RAM32x1D+RAMB18E1(1)
MiniCPU_SerPCU		137	51	19	0	65	2	0	0	
MiniCPU_SerALU		171	49	14	0	97	11	0	0	
	PCU+ALU	308	100							

Baby 8 blocks		total cells	flip-flops	MISC	CARRY4	LUT	MuxLUT	DSP48	memories	mem type

					xilinx		
logic function	34		26		8		
ALU	59		33	3	19	4	
datapath	131	8	86	3	30		4 RAM32M
test	34	8	13		10	3	
decode	34		25		9		
cmux	39		22		11	6	
fsm2control	107		61		28	18	