### NAND

# Result of using Yosys to convert to NANDs for various softcores

core name	options	NANDs
darkriscv glacial		50424 2063
riscv simple	RV32I UNI	2003
riscv_simple	RV32I MULTI	
riscv_simple	RV32I PIPE	
riscv_simple	<b>RV32IM UNI</b>	
riscv_simple	<b>RV32IM MULTI</b>	
riscv_simple	<b>RV32IM PIPE</b>	
serv		3595
picorv32		34463

### non RISC-V:

core name	options	NANDs	
zpu_avalanche		7900	
MiniCPU_SerPCU	J	1105	
MiniCPU_SerALU	J	1269	
	PCU+ALU	2374	
MCPU		425	
6502 (nestang)		4881	
cray1		303711	Includes 9 hard_v_reg, 65 latches
j0 (gameduino)		20998	
j0	no mult (16 stk)	10616	
ukp (nestang)		3961	includes code ROM

## NAND

# Baby 8 blocks

logic function	26
ALU	32
datapath	445

ice40

# Result of synth\_ice40 in Yosys for various softcores

core name	options	total cells fli	p-flops	LUT4	CARRY	TBUF	RAM40_4K
darkriscv		7777	2262	5176	339	0	0
glacial		355	84	224	47	0	0
riscv_simple	RV32I UNI	8273	1743	5801	441	32	256
riscv_simple	<b>RV32I MULTI</b>	8362	1978	5682	446	0	256
riscv_simple	RV32I PIPE	10272	2587	6910	487	32	256
riscv_simple	<b>RV32IM UNI</b>	18611	1743	12698	3882	32	256
riscv_simple	<b>RV32IM MULTI</b>	18740	1984	12608	3891	1	256
riscv_simple	<b>RV32IM PIPE</b>	20445	2595	13629	3933	32	256
serv		450	201	241	. 8	0	0
picorv32		2683	596	1678	405	0	4

## non RISC-V:

core name	options	total cells fli	p-flops	LUT4 C	CARRY T	BUF	RAM40_4K
zpu_avalanche		1651	272	1307	72	0	0
MiniCPU_SerPo	CU	157	51	106	0	0	0
MiniCPU_SerAl	LU	176	49	127	0	0	0
_	PCU+ALU	333	100				
MCPU		79	24	35	12	8	0
6502 (nestang)		936	123	754	59	0	0
cray1		37355	8510	25769	3057	0	19 9 hard_v_reg
j0 (gameduino)		942	67	782	91	0	2
j0	no mult (16 stk)	590	65	445	78	0	2
ukp (nestang)		494	151	272	68	2	1

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ice40

Baby 8 blocks	total cells flip-flo	ops LUT4 CA	RRY TBUF	RAM40_4K
logic function	8	8		
ALU	36	28	8	
datapath	391	136 247	8	

gowin

# Result of synth\_gowin in Yosys for various softcores

core name	options	total cells	flip-flops	MISC	ALU	LUT	MuxLUT	RAM16S4
darkriscv		9032	142	176	355	5198	3105	56
glacial		753	84	41	55	351	222	0
riscv_simple	RV32I UNI	32136	1729	547	422	16926	12512	0
riscv_simple	<b>RV32I MULTI</b>	17631	1964	515	461	9709	4982	0
riscv_simple	<b>RV32I PIPE</b>	23066	2573	515	470	12540	6968	0
riscv_simple	<b>RV32IM UNI</b>	94934	1729	547	6156	50099	36403	0
riscv_simple	<b>RV32IM MULTI</b>	85103	1964	515	6131	45825	30668	0
riscv_simple	<b>RV32IM PIPE</b>	85506	2581	547	6209	45840	30329	0
serv		1083	201	207	12	452	211	0
picorv32		4039	567	411	424	2009	596	32

# non RISC-V:

core name	options	total cells	flip-flops I	MISC ,	ALU	LUT	MuxLUT	RAM16S4
zpu_avalanche		3930	272	104	78	2053	1423	0
MiniCPU_SerPC	CU	167	51	19	0	84	13	0
MiniCPU_SerAL	_U	407	49	14	0	217	127	0
	PCU+ALU	574	100					
MCPU		187	24	20	15	90	38	0
6502 (nestang)		1833	123	41	68	1100	501	0
cray1		0	D latches	not suppo	rted			
j0 (gameduino)		2064	35	78	112	1245	578	16
j0	no mult (16 stk)	4250	31	78	91	2163	1879	8
ukp (nestang)		986	151	29	89	477	240	0

### gowin

Baby 8 blocks	total cells flip-fl	total cells flip-flops MISC ALL			Mu	MuxLUT RAM16S4		
logic function	34		26		8			
ALU	106		35	9	40	22		
datapath	193	8	87	9	57	28	4	

cyclonev

Result of synth\_intel\_alm -family cyclonev in Yosys for various softcores

core name	options	total cells	flip-flops	MISC	ALU	LUT	M18x18	M27x27	memories mem type
darkriscv		1891	162	178	365	5 1057	1	. 0	128 mlab
glacial		328	84	42	58	3 144	C	) (	0
riscv_simple	RV32I UNI	6795	1731	483	507	3946	C	) (	128 m10k
riscv_simple	<b>RV32I MULTI</b>	7157	1966	456	581	4026	C	) (	128 m10k
riscv_simple	<b>RV32I PIPE</b>	8428	2627	487	573	3 4613	C	) (	128 m10k
riscv_simple	<b>RV32IM UNI</b>	10419	1731	485	701	7370	2	2 2	2 128 m10k
riscv_simple	<b>RV32IM MULTI</b>	10620	1966	457	709	7356	2	2 2	2 128 m10k
riscv_simple	<b>RV32IM PIPE</b>	12127	2635	488	739	8133	2	2 2	128 m10k
serv		641	204	209	27	7 201	C	) (	0
picorv32		2322	608	413	431	868	C	) (	2 m10k

non RISC-V:

core name	options	total cells flip	o-flops N	MISC AL	U LI	JT N	M18x18 M2	7x27 memories	mem type
zpu_avalanche		1331	272	109	79	871	0	0	0
MiniCPU_SerPC	CU	139	51	22	0	66	0	0	0
MiniCPU_SerAL	U	167	49	14	0	104	0	0	0
	PCU+ALU	306	100						
MCPU		93	24	28	15	26	0	0	0
6502 (nestang)		704	123	41	68	472	0	0	0
cray1		0 D	latches r	not supporte	ed				
j0 (gameduino)		558	67	77	100	311	1	0	2 m10k
j0	no mult (16 stk)	540	39	77	95	297	0	0	32 mlab
ukp (nestang)		561	155	31	100	275	0	0	0

# cyclonev

Baby 8 blocks	total cells flip-flops MI	SC ALU	LUT	M18x18	M27x27	memories	mem type
logic function	34	26		8			
ALU	63	33	10	20			
datapath	149 8	86	10	29			16 mlab

xilinx

Result of synth\_xilinx -flatten in Yosys for various softcores (default family is xc7)

core name	options	total cells fli	p-flops M	IISC C	CARRY4 L	UT	MuxLUT D	SP48 me	mories mem type
darkriscv		2506	150	281	68	1428	498	1	80 RAM32x1D+RAM32M(16)
glacial		298	84	44	15	139	16	0	0
riscv_simple	RV32I UNI	6581	1728	528	88	3469	736	0	32 RAMB36E1
riscv_simple	<b>RV32I MULTI</b>	7371	1963	509	74	3969	824	0	32 RAMB36E1
riscv_simple	<b>RV32I PIPE</b>	8534	2572	542	92	4508	788	0	32 RAMB36E1
riscv_simple	<b>RV32IM UNI</b>	35014	1728	2514	2736	18378	9618	8	32 RAMB36E1
riscv_simple	<b>RV32IM MULTI</b>	35780	1963	2497	2722	18758	9800	8	32 RAMB36E1
riscv_simple	<b>RV32IM PIPE</b>	35660	2580	2534	2742	18685	9079	8	32 RAMB36E1
serv		650	201	207	4	212	26	0	0
picorv32		2447	572	657	97	1038	67	0	16 RAM32M

non RISC-V:

core name	options	total cells fli	ip-flops M	ISC	CARRY4 L	UT M	luxLUT D	SP48 mer	nories mem type
zpu_avalanche		1307	272	105	21	754	155	0	0
MiniCPU_SerPCU		137	51	19	0	65	2	0	0
MiniCPU_SerALU		171	49	14	0	97	11	0	0
	PCU+ALU	308	100						
MCPU		101	24	35	5	36	1	0	0
6502 (nestang)		780	123	43	14	520	80	0	0
cray1		25005	6803	1056	811	15406	661	11	257 RAM32x1D+RAMB18E1(1)
j0 (gameduino)		797	43	110	24	397	190	1	32 RAM32x1D
j0	no mult (16 stk)	683	39	107	19	315	171	0	32 RAM32x1D
ukp (nestang)		527	159	71	25	213	58	0	1 RAMB18E1

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# xilinx

Baby 8 blocks	total cells flip-flo	ps MISC	CARR	Y4 LUT	MuxLl	JT DSP48	memories	mem type
logic function	34		26		8			
ALU	59		33	3	19	4		
datapath	131	8	86	3	30			4 RAM32M