ICCAD 2018 CAD Contest

Timing-Aware Fill Insertion

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Synopsys Inc.

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Introduction

It is a mandatory step in modern semiconductor manufacturing process to fill the empty conductor layers with metal fills, and it is commonly performed after the physical design stage. These fills can reduce the dielectric thickness variation, increase planarity, and provide better pattern density, all of which are important to mitigate the process variability thereby achieving better yield.

Problem Description

When a fill is inserted, it improves the metal density and increases planarity. But on the other hand it inevitably couples to the signal tracks (Figure 1). If the coupling capacitance to a critical net is significant, the original timing-closure may not be achieved anymore. Therefore it is important to reduce the capacitance impact during metal fill insertion.

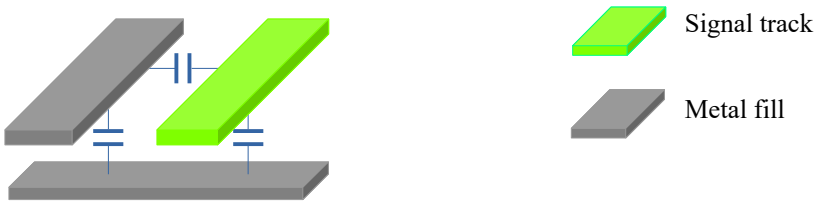


Figure 1: Signal track-metal fill coupling

The current mainstream solution is to set up a keepout region (space around a metal track to its nearest fill, Figure 2) for metal fill around critical signal tracks so that the coupling capacitance introduced by the metal fills can be safely ignored. However, achieving optimum metal fill insertion with this method is a challenge. A large keepout distance could result in sub-optimal metal density and uneven fill patterns that negatively impact yield. Conversely, a small keepout distance could significantly increase capacitance and break timing. Furthermore, the impact on timing is not known without running a parasitic extraction tool. Hence an efficient algorithm to insert optimum metal fill is required.

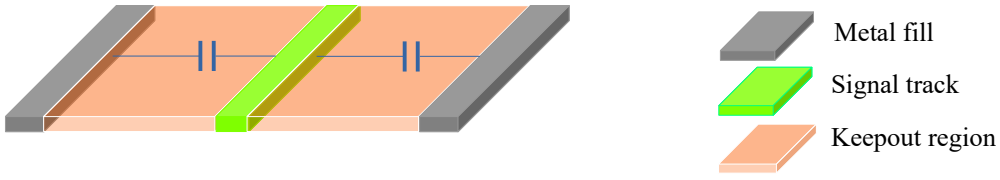


Figure 2: Keepout regions

Capacitance Calculation

The metal fill insertion algorithm needs to account for the impact of capacitance on the signal nets. There are three main types of capacitances that need to be considered when evaluating the impact of metal fill. They are as follows:

1) Area Capacitance

Two conductor pieces will form an area capacitance when a) they are on different metal layers, b) their projections on the ground plane overlap, and c) no other intermediate-layer metal appears between the two conductors in the overlapped region (Figure 3).

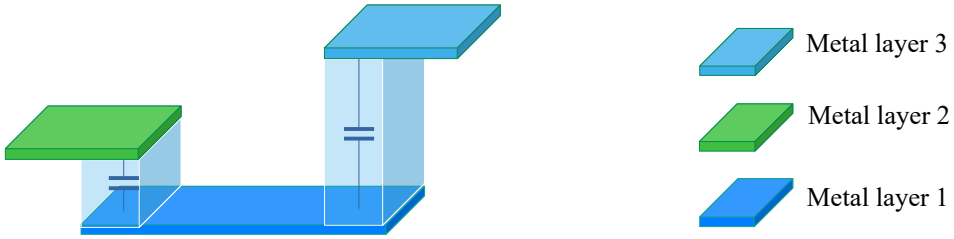


Figure 3: Area Capacitance

For an overlapped area s formed by conductors on layers l_1 and l_2, the area capacitance C_a is calculated by $C_a = P_{l_1,l_2}(s) \times s$, where $P_{l_1,l_2}(s)$ is the area capacitance per unit area and it is a function of overlapped area s.

2) Lateral Capacitance

The lateral capacitance is formed by the conductors on the same layer. Any two conductors that horizontally overlap will form lateral capacitance as shown in Figure 4. The capacitance is calculated by $C_l = P_l(d) \times l$, where l is the length of the parallel edges of the conductors and $P_l(d)$ is the lateral capacitance per unit length, which is a function of distance of the parallel edges d.

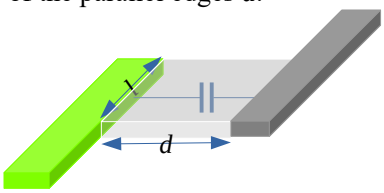


Figure 4: Lateral Capacitance

3) Fringe Capacitance

The fringe capacitance is formed by two conductors on different layers and its calculation is based on the following formula, where these two conductors don't overlap with each other.

$$C_f = \begin{cases} p_{l_1,l_2}(d) \times l + p_{l_2,l_1}(d) \times l, & d \geq 0 \\ 0, & d < 0 \end{cases}$$

where l is the length of parallel edges and d is the horizontal distance of two conductors (Figure 5). d will be negative if the conductors overlap (i.e., $C_a > 0$). $P_{l_1,l_2}(d)$ and $P_{l_2,l_1}(d)$ are the fringe capacitance per unit length.

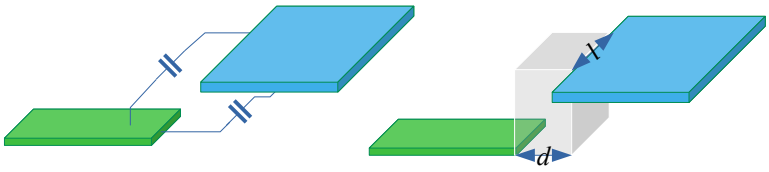


Figure 5: Fringe Capacitance

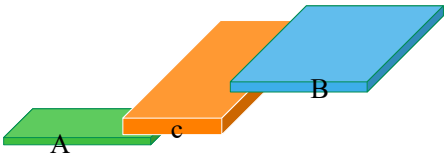


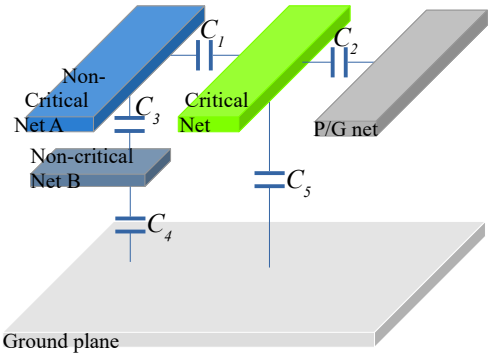
Figure 6: Shielding effect

3.1) Shielding Effect

If two conductors A, B are on the different layers l_1 and l_2, respectively, the fringe coupling between A and B is shielded and the capacitance goes to zero when there is a horizontal conductor on the intermediate layer between A and B. Note that the coupling capacitance to the shielding conductor C still needs to be calculated (Figure 6). In Figure 6, the fringe capacitance between A and B is shielded by C, but the coupling capacitance (either fringe capacitance or area capacitance) between (A,C) and (B,C) need to be calculated.

Total Capacitance Calculation

After metal fill insertion, the total capacitance of a critical net needs to be calculated as the equivalent capacitance to ground. Note that resistance is ignored. All non-critical nets, except for the power/ground nets, are treated as floating. Coupling to the power/ground nets is calculated as direct-coupling to ground (Figure 7).



$$C_{total} = C_2 + C_5 + \frac{C_1 \times C_3 \times C_4}{C_1 \times C_3 + C_3 \times C_4 + C_1 \times C_4}$$

Figure 7: Total capacitance calculation

Metal Density

The layout with metal fill must meet the density criteria. The density is calculated in a window based manner (Figure 8):

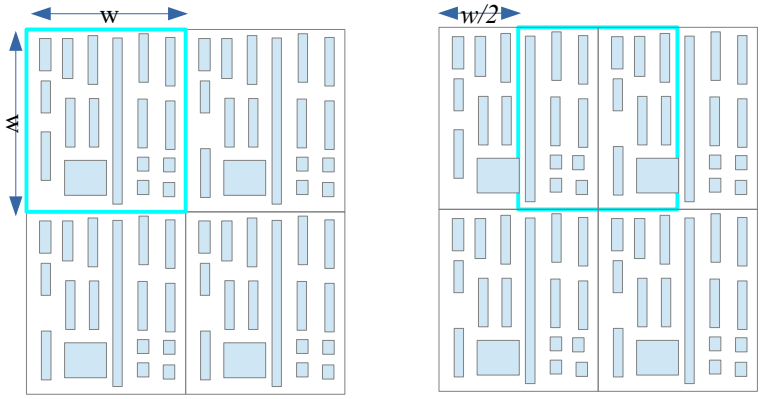


Figure 8: Density Calculation Window

w is the window size for density calculation, and the step length is set to $w/2$. The density in a window W_i is calculated as

$$D_{l,W_i} = \sum_{S \in W_i} S/w^2,$$

where l is the metal layer, and S is the metal area that is enclosed inside W_i. The density in each window must be larger than the given metal density for that layer.

Algorithm Evaluation

The optimization algorithm should insert metal fills subject to the density criteria and design rules, while minimizing the total capacitance of a given critical net. Metal fills must not introduce any design rule violation. Results with design rule violation will not be accepted for further evaluation. Results need to pass the window-based density check. Results with density violation will be rejected as well.

The accepted result with smaller total capacitance will get higher quality score with the highest of 15 points. For instance, the best result (smallest total cap) gets 15 points and the second place gets 14 points. The accepted result with shorter run time gets higher performance score with the highest of 5 points. For instance, the result with shortest run time gets 5 points and the second place gets 4 points. Results beyond the the fifth place in run time do not get any performance points.

Teams will be ranked by the sum of quality points and performance points.

Benchmark suites

Five benchmark cases will be provided along with one rule file and one process file which describe design rules and process-related information. The benchmark cases are all text files with different number of polygons (rectangular). Lines starting with a semicolon (;) are comments.

Layout File Format:

```
; The first non-comment line of layout file is the chip boundary:
;   bottom_left_x bottom_left_y top_right_x top_right_y
Chip_boundary_BL_x Chip_boundary_BL_y Chip_boundary_TR_x Chip_boundary_TR_y

; Polygon_id is a positive integer. The polygon type will be one of the four types:
; Drv_Pin that marks this polygon is a drive pin of the net,
; Normal marks this polygon is a normal conductor,
; Load_Pin indicates the polygon is a load pin, and
; Fill indicates this is a fill polygon.

; For a fill polygon, its net id can be set to any integer.
Polygon_id bl_pt tr_pt net_id layer_id <polygon type: Drv_Pin|Normal|Load_Pin|Fill>
```

Rule file:

```
Layer_id <conductor|via> min_width min_space max_fill_width min_density max_density
```

Please note that the density criteria does not apply to via layer, so if the second field of the rule file is `via`, `min_density` will be set to `0` and max_density will be `1`.

Process file:

```
; Window size for density calculation (unit: nanometers)
window: 5000

; Unit Capacitance
; when a table does not exist, it’s marked by ‘*’
; lateral_table_* can be thought of as a special case of fringe_table_*
; layer id (layer id 0 is ground plane)
```

	1	2	...	n
0	(area_table_1_0,*)	(area_table_2_0, *)		(area_table_n_0, *)
1	(*, lateral_table_1)	(area_table_1_2, fringe_table_1_2)	...	(area_table_1_n, fringe_table_1_n)
2	(area_table_2_1, fringe_table_2_1)	(*, lateral_table_1)	...	(area_table_2_n, *)
...	...	...	...	...
n	(area_table_n_1, fringe_table_n_1)	(area_table_n_2, fringe_table_n_2)	...	(*, lateral_table_n)

```
TableName: area_table_1_0
; p(s)= a*s + b
; the unit cap is a piece-wise linear function of s
;  s1=<s <s2, s2=<s<= s3 …
s1,  s2, s3, ...
(a1, b1), (a2, b2), (a3, b3) ….

TableName: area_table_1_2
; p(s)= a*s + b
; the unit cap is a piece-wise linear function of s
;  s1=<s <s2, s2=<s< s3 …
s1,  s2, s3, ...
(a1, b1), (a2, b2), (a3, b3) ….

TableName: area_table_1_3
; p(s)= a*s + b
;
s1, s2, s3, ...
(a1, b1), (a2, b2), (a3, b3) ….
...
...
; lateral cap table
TableName: lateral_table _1
; p(d) = a*d + b
d1, d2, d3, …
(a1, b1), (a2, b2), (a3, b3)…
...
; fringe cap table
TableName: fringe_table_1_0
; p(d) = a*d +b
d1, d2, d3, …
(a1, b1), (a2, b2), (a3, b3)…
```

The contest program should read in an config file, for example, input.conf, to parse all necessary files and parameters:

```
; Test1
design: <benchmark_file_name>
output: <output file>
rule_file: <design rule file>
process_file: <process file>
critical_net: net_id1, net_id2,...
power_nets: power_net1, power_net2, …
ground_nets: ground_net1, ground_net2, …
```

The program should output a design with metal-fills. The output file format should be same as input benchmark file.

Cap Extraction Example

Example1.conf:

```
design: example1.layout
output: example1.fill
rule_file: rule.dat
process_file: process.dat
critical_net: 1
power_nets: 2
ground_nets: 0
```

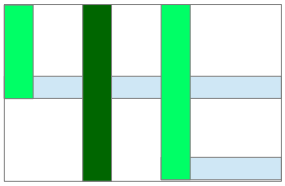


Figure 9: Example layout with one metal-fill (dark green rectangle)

Example1.layout:

```
0 0 100 80 ; chip boundary
1 60 0 100 10 2 1 Normal; A normal polygon on layer 1 (net 2: power)
2 0 40 100 50 1 1 Normal; A normal polygon on layer 1 (net 1: critical net)
3 0 40 10 80 1 2 Normal; A normal polygon on layer 2 (net 1: critical net)
4 60 0 70 80 2 2 Normal; A normal polygon on layer 2 (net 2: power)
```

rule.dat:

```
;Layer_id <conductor|via> min_width min_space max_fill_width min_density max_density
1 conductor 10 10 30 0.3 1
2 conductor 10 10 30 0.3 1
```

process.dat:

```
;table matrix, layer id 0 means ground plane
        1                           2
0 (area_1_0, *)          (area_2_0, *)
1 (*, lateral_1)         (area_2_1, fringe_2_1)
2 (area_2_1, fringe_1_2) (*, lateral_2)
; process tables
TableName: area_1_0
  100                 200            300   400
  (0.01, 0.017) (0.0102, -0.02) (0.0101, 0.015)

TableName: lateral_1
  10                 50         100       200
  (0.01, 0.017) (0.0102, 0.001) (0.0101, 0.015)

TableName: fringe_1_2
  0                  50          100       150
  (0.007, 0.012) (0.0102, 0.001) (0.0101, 0.015)


TableName: area_2_0
  100                 150         200       300
  (0.01, 0.017) (0.0102, -0.01) (0.0101, 0.015)

TableName: area_2_1
  100                 300         400      500
  (0.01, 0.017) (0.0102, -0.02) (0.00101, 0.015)

TableName: lateral_2
  10                 50          100    200
  (0.01, 0.011) (0.0102, 0.001) (0.0101, 0.015)

TableName: fringe_2_1
  10                 50         100       150
  (0.011, 0.01) (0.0102, 0.001) (0.0101, 0.015
```

Now assuming the metal-fill output file example1.fill:

```
1 30 0 40 80 0 2 Fill; A metal-fill on layer 2
```

The coupling capacitance between the critical net (net id 1) and the metal-fill consists of 1) area-capacitance between polygon 2 and the fill polygon, and 2) lateral-capacitance between polygon 3 and the fill.

For the area capacitance, the overlapped area is 100 nm^2 between layers 1 and 2. Hence the area cap table should be `area_2_1`. Since the area is between index 100 and 300, the coefficients 0.01 and 0.017 are selected to calculate the unit area capacitance:

C_{unit} =0.01x overlapped area + 0.017 = 1.017 ff/nm^2 ,

and the area-capacitance is

C_{unit} x overlapped area = 101.7ff.

Please note that if the overlapped area is larger than the largest area sampling point of the area cap table, then the largest sampling point is used to calculate an initial capacitance and then scaled by a factor of overlapped-area /

largest area-sampling point. For instance, assuming an overlapped area of 800 nm^2 formed by two polygons on layers 1 and 2, and since the largest sampling point in the table `area_2_1` is 400nm^2, we use 400 to calculate an initial cap:

C_{init} = (0.0101 x 400 + 0.015)x400 = 1622 fF

The final area capacitance is calculated by

$C_{area} = C_{init}$ x (800/400) = 1622 x 2 = 3244 fF

A similar procedure can be applied when the overlapped area is smaller than the smallest area sampling point:

$C_{area} = C_{init} * S_{overlap}/S_{min\_sampling\_area}$,

where C_{init} is the initial capacitance calculated with the smallest area sampling point, $S_{overlap}$ is the overlapped area and $S_{min\_sampling\_area}$ is the smallest sampling point in the table.

For the lateral-capacitance between polygon 3 and the fill polygon, the distance of the two polygons is 20nm, and the table `lateral_2` is used. Since 20nm is between 10nm and 50nm, we choose the first coefficient pair: (0.01, 0.011). Then the unit capacitance will be:

C_l = 0.01 * 20 + 0.011 = 0.211 ff/nm.

Since the parallel edges between the polygons are 40nm long, the lateral-capacitance will be

C_l x 40nm = 8.44 ff

Similar, we can calculate the coupling cap between the fill polygon and net 2 (power net). Note that there is a fringe cap between polygon 1 and the fill polygon. The distance between polygon 1 and the fill is 20nm. Two tables need to considered: `fringe_2_1` and `fringe_1_2` (because metal layers have different thicknesses, the two tables may not be the same). We can get two unit capacitance:

C_{f12} = 0.007 X 20 + 0.012 = 0.152/nm

C_{f21} = 0.011 X 20 + 0.01 = 0.23/nm

The parallel edge length is 10nm, so the fringe capacitance between the file and polygon 1 will be

C_{f12} * 10nm + C_{f12}*10nm = 3.82 ff.

Note that for any lateral-capacitance or fringe-capacitance due polygons with horizontal distance larger than the largest sampling point in the corresponding unit-cap table, the capacitance can be assumed to be zero because the value is small.

Reference

[1] https://www.eetimes.com/document.asp?doc_id=1302632

[2] Y. Chen, P. Gupta and A. B. Kahng, "Performance-Impact Limited Area Fill Synthesis", Proc. ACM/IEEE Design Automation Conf., June 2003, pp. 22-27.

[3] P. Gupta, A. B. Kahng, O.S. Nakagawa and K. Samadi, "Closing the Loop in Interconnect Analyses and Optimization: CMP Fill, Lithography and Timing", Proc. 22nd Intl. VLSI/ULSI Multilevel Interconnection (VMIC) Conf., October 2005, pp. 352-363.

[4] A. B. Kahng, K. Samadi and P. Sharma, "Study of Floating Fill Impact on Interconnect Capacitance", Proc. International Symposium on Quality Electronic Design, April 2006, pp. 691-696.

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[7] VS Shilimkar, SG Gaskill, A Weisshaar, “Impact of metal fill on on-chip interconnect performance”, 2009 The 42nd International Symposium on Microelectronics, 983-990

[8] Vikas S Shilimkar, Andreas Weisshaar, “Modeling of Metal-Fill Parasitic Capacitance and Application to On-Chip Slow-Wave Structures,” IEEE Transactions on Microwave Theory and Techniques 65 (5), 1456-1464

IV. FAQ

Q1. I can't find any info about window size in the file format of benchmark suite, so how can we read in window size info?
A1. new parameter (window) is added into the process file:
window: window size

Q2. In Figure 7, should there have fringe capacitance between critical net and non-critical net B?
A2. This is just an example to explain how to calculate the total capacitance by assuming the couplings are extracted as shown in the figure.

Q3. In III. Algorithm Evaluation, is quality score is measured by the sum of total capacitances of all critical nets in all benchmark cases?
A3. Yes.

Q4. The object is only minimize capacitance effect and runtime described in the Problem Description when doing fill insertion? or other objects like density, etc.
A4. Yes, the object is only to minimize capacitance effect and run-time. The density requirements can be considered as constraints that after filling, density in each window must meet the requirement within given range.

Q5. From Q1, If we need to minimize density, how can we get lower bound and upper bound constraint?
A5. Inside the rule file, each layer has min/max constraints.

Q6. The shape of Insertion Filler is only rectangle? or others like diamond, etc.
A6. Yes, ONLY rectangle are accepted.

Q7. When will you release testcase?
A7. Two cases will be released by 4/23/2018. Other three will be released in May.

Q8. How to calculate parallel capacitance?
A8. Please see II. 2) Lateral Capacitance and the example.

Q9. Can we connect dummy fill to power or ground poly?

A9. No, you cannot as it will pose difficulty for design rule checking. I.e., Fills are not allowed to touch any signals.

Q10. When will you release testcase?
A10.Two cases will be released by 4/23/2018. Other three will be released in May.

Q11. Which density criteria should we satisfy? In "Metal Density" section, the description says "The density is calculated in a window based manner", in other words, we need to satisfy window density constraint. But in "Rule file" section, the description of density constraint is behind layer id. Is this min_density and max_density is the window constraint for every window in this layer? or these constraints are layer constraints (We just need to calculate density for a layer and satisfy these constraints)
A11. The density constraint applies to each layer. In other words, for each layer, we will perform a window-based check.

Q12. What is the table naming rule?

In row layer 0 and column layer 1, the name is area_table_1_0 ->first number is column number and second number is row number. But in row layer n column layer 1, the name is area_table_n_1->first number is row number and second number is column number. Which one is the correct rule?

	1	2	...	n
0	(area_table_1_0,*)	(area_table_2_0, *)		(area_table_n_0, *)
1	(*, lateral_table_1)	(area_table_1_2, fringe_table_1_2)	...	(area_table_1_n, fringe_table_1_n)
2	(area_table_2_1, fringe_table_2_1)	(*, lateral_table_1)	...	(area_table_2_n, *)
...	...	...	...	...
n	(area_table_n_1, fringe_table_n_1)	(area_table_n_2, fringe_table_n_2)	...	(*, lateral_table_n)

A12. There is no rule in naming a table. One should check the name matrix to get the right table name.

Q13. Filler type is 0 in example1.fill, but type 0 is ground nets. Is the type always ground nets when we inserting fill?

```
1 30 0 40 80 0 2 Fill; A metal-fill on layer 2
```

A13. The net id is not used in the fill file, just to main format consistency. All fills are treated as floating (meaning they should not touch any signals).

Q14. Could we insert dummy fill in via layer?
A14. No, only metal fills are allowed.

Q15. The answer of "Could we insert dummy fill in via layer" is yes. No, only metal fills are allowed. We think you may have a misunderstanding. The question we wanted to ask is **Can we insert dummy fill in "VIA Layer"**? (Because we don't need to consider area criteria in this layer, we want to know that inserting in via layer is legal or not?)
A15. To further clear the problem, I've removed all via layers from the rule file and test data. So the answer is still no. But in the real design, via FILL is allowed and the designer is encouraged to fill as many vias as possible to the top via layer, in order to improve yield.
"

Q16. The questions is about testcase file
In "rule.dat", you provide layer 1 to layer 19's constraint
In "Circuit1.cut", there are lots of poly in layer 10-19
But in "process.dat", it only provides us layer 0-9's capacitance table.
How to calculate capacitance when poly in layer 10-19?
A16. All via layers have been removed.

Q17. In "circuit1.cut" line 367, "net id" is 70144. But we can't find net id 70144 in circuit1.conf. Is this a wrong Id? or How to do when we get a non-defined Id?
A17. The nets whose ids are specified in the config file are "critical nets", meaning we should minimize the timing impact to them when inserting metal fills.

Q18. What's the difference if a polygon is Drv_pin or Load_pin compare with Normal or Fill when calculating capacitance?
A18. You can ignore the pin types. Ideally, we should calculate the delay from drv_pin to load_pin in order to more accurately evaluate the timing impact from the metal fills. But this will pose great difficulty. So please ignore them.

Q19. Can we insert FILL into via layer? Do we need to consider the connection between the vias and their upper and lower conductor layer? If so, which via layer

connects which pair of conductor layers? If we insert Fill in via layer, do we need to avoid the Fill in via layer touching the conductors in upper or lower layer?
A19. No via FILL. The test cases have been updated and all via layers have been removed.

Q20. In the testcases, there are via layers from layer 11~layer 19, but we don't have the corresponding capacitance table in process file. Is via involved in the capacitance calculation?
A20. Via layers have been removed.

Q21. In the testcases ,net 0 is set to both power net and ground net. Do we consider net 0 as ground net?
A21. Yes, this is made on purpose. All nets with ID 0 are ground nets.

Q22. We can't find the window size in process file.
A22. Please re-download the cases. It has been added into the process file.

Q23. Is there any hard limit on run time?
A23. Yes, 24 hours.

Q24. The question is about testcase file.
In “process.dat”, the amounts of unit capacitance at the first line of table are one more than second line of table.
For example, there are 12 range numbers at line 23, but 11 parameters of function. In cap extraction example, you give both of them a same amount. Therefore, if I got three values which was defined as “area_table_1_0”,
1600, 2400, 320000. And which parameters of function will be chosen, respectively?
A24. Yes, the examples in the problem description missed one sampling point. Thanks for pointing that out. Assuming a parameter x, and a series of sampling point x_1 x_2 x_3 .. x_n. If x_k =< x <x_k+1, you should choose the kth function coefficient. If x is out of the sample region, i.e., x < x_1 or x >= x_n, please see the problem description on how to scale or discard the values.

Q25. May I know in the contest question C, for the total capacitance, what is the exact way to calculate the total capacitance? in the example, there is only mention the capacitance between the critical and non-critical net, or should we just sum up all the capacitance in the final evaluation?
A25. To calculated the total cap:

1. "the total capacitance of a critical net will be calculated as the equivalent capacitance to ground"
2. Total cap = sum of the total capacitance of each critical net.
For step 1, it's a basic pure capacitor-network analysis that calculates the equivalent capacitance of a two-port cap-network.
If you don't know how to do this, please refer to
https://en.wikipedia.org/wiki/Series_and_parallel_circuits
https://en.wikipedia.org/wiki/Capacitor#Networks
slides 10-11
of http://www.ece.ubc.ca/~shahriar/eece251_notes/eece251_set4_2up.pdf
for the basic rules of capacitance calculation.

Q26. How do we read file path ? Is use absolute path or other path?
A26. Please use the path that is relative to the config file.

Q27.

Q1: As shown in Fig. 1, suppose nets A and B in layer 1 and layer 3, respectively. Meanwhile, their projections on the ground plane overlap. If a small net C in layer 2 cross the overlapping region of projection between nets A and B, is the area capacitance between nets A and B completely shielded by net C (i.e., $C_3^a = 0$)? If not, how to calculate C_3^a?

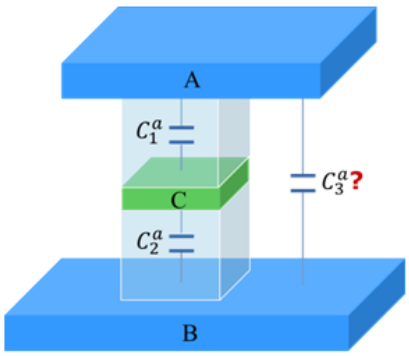

Fig. 1 Area capacitance

A27. No, C{^a}_{3} is not zero. The area cap is formed by the overlapped area in which two conductors that form this area can directly "see" each other.
In your case, A/C formed an area. Inside the area, A and C can directly "see" each other and its area cap would be calculated as C1. C/B formed an area
inside which B/C can see each other and its area cap would be calculated as C2. The other overlapped area, i.e., the area that A/B can directly "see"
each other would be calculated as C3.

Q28.

Q2: As shown in Fig. 2, suppose nets A, B and C belong to the same layer and net B is between nets A and C (Note: there are lateral capacitance between any two nets). In Fig. 2 (a), is the lateral capacitance between nets A and C shielded by net B? If there can be shield, then in Fig. (b), is the lateral capacitance between nets A and C completely shielded by net B (i.e., $C_3^l = 0$)? If $C_3^l \neq 0$, does the calculation of the lateral capacitance between nets A and C be affected by net B? If it does, what is the detailed calculation formula for the lateral capacitance C_3^l between nets A and C?

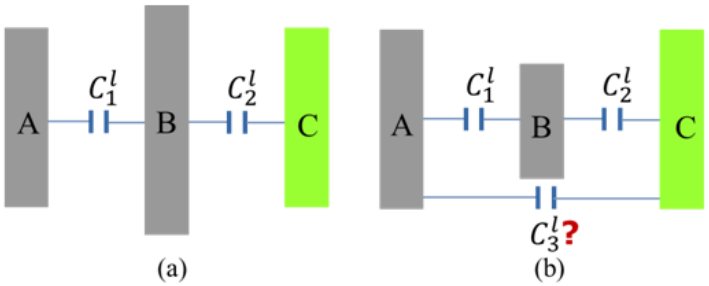

Fig.2 Lateral capacitance shielding. (a) Example 1. (b) Example 2.

A28. This is similar to Q1. If any part of A/C cannot see each other (horizontally), C3 is 0 (case a). If any part of A/C can "see" each other, that part should have lateral coupling cap.

The calculation is similar as the calculation of c1l or c2l. i.e., with the parallel edge of A/C and distance between A/C. Please note the parallel edge only contains the part in which A/C can directly see each other.

Here is how to calculate caps in b:

Assuming A&B's parallel edge is l_ab (which is actually B's length as B is within a's horizontal projection), and the distance between A&B is d_ab,

C1l = P(l_ab)*d_ab

Similar, we can cat C2l = P(l_bc)*d_bc.

Assuming A&C's parallel edge is l_ac, and the distance is d_ac, since part of A&C's parallel edge is blocked by B, then the effective parallel edge length should be

l_eff_ac = l_ac - l_ab (or l_ac - l_bc, since l_ab == l_bc),

C3l = P(l_eff_ac) * d_ac.

Q29.

Q3: Suppose a structure with nets A, B, C in layer 1 and nets D, E in layer 2 (Notes: there is not fringe capacitance between nets C and D). The details are shown in following Fig. 3.

Case 1: Is the capacitance between net D and ground plane shielded by net B?

Case 2: There is a lateral capacitance between nets A and C, is it shielded by net B?

Case 3: If there is a fringe capacitance between nets A and E, is it shielded by nets B or D? If there can be shield, is also the fringe capacitance between nets B and E shielded by nets C or D?

Case 4: For the specific example shown in following Fig. 3, can you show me a whole formula for calculating the total capacitance of critical net A?

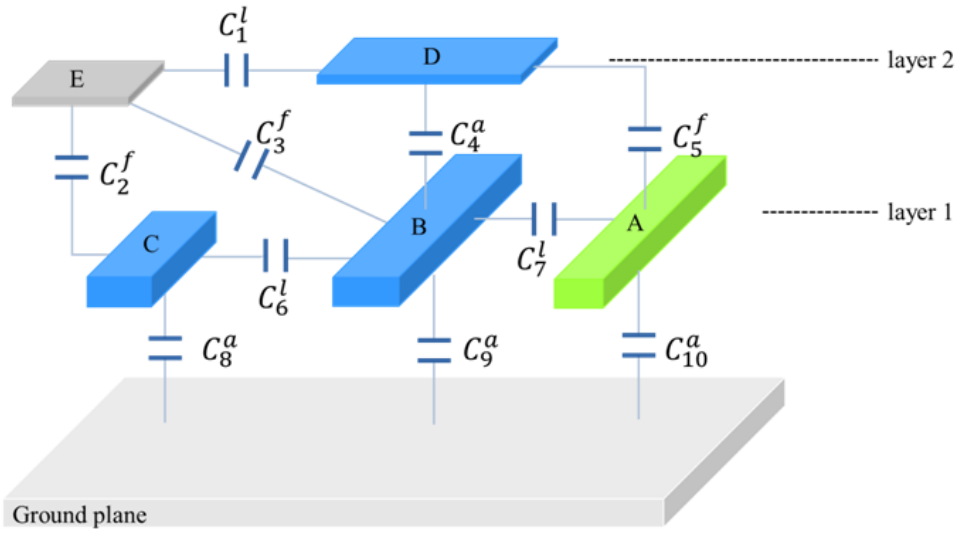

Fig.3 The total capacitance

A29.

Case 1: partly. Part of D may see the ground plane, so that part should have area cap to the ground. Please see A1 for more details.

Case2: It depends if A/C can directly see each other. Please see A2 for more information.

Case3: Fringe cap between A/E is shield by B/D/C. Fringe cap between B/E is also shielded (by D/C).

Case4: The case is too complicated to do a hand calculation. The standard method would be

doing a Y-delta transformation or using a matrix-based method (similar to conductance matrix based network analysis):

	A	B	C	D	E
A	(c5+c7+c10)	-c7	0	-c5	0

B -c7 (c3+c4+c6+c7+c9) -c6 -c4 -c3

C 0 -c6 .....

D -c5 -c4 .....

E 0 -c3 .....

Assuming the matrix is partitioned as follows:

C11 | C12

C21| C22

(C11 == (c5+c7+c10))
Then the total cap of A would be C11 - C12 * (1/C22)*C21