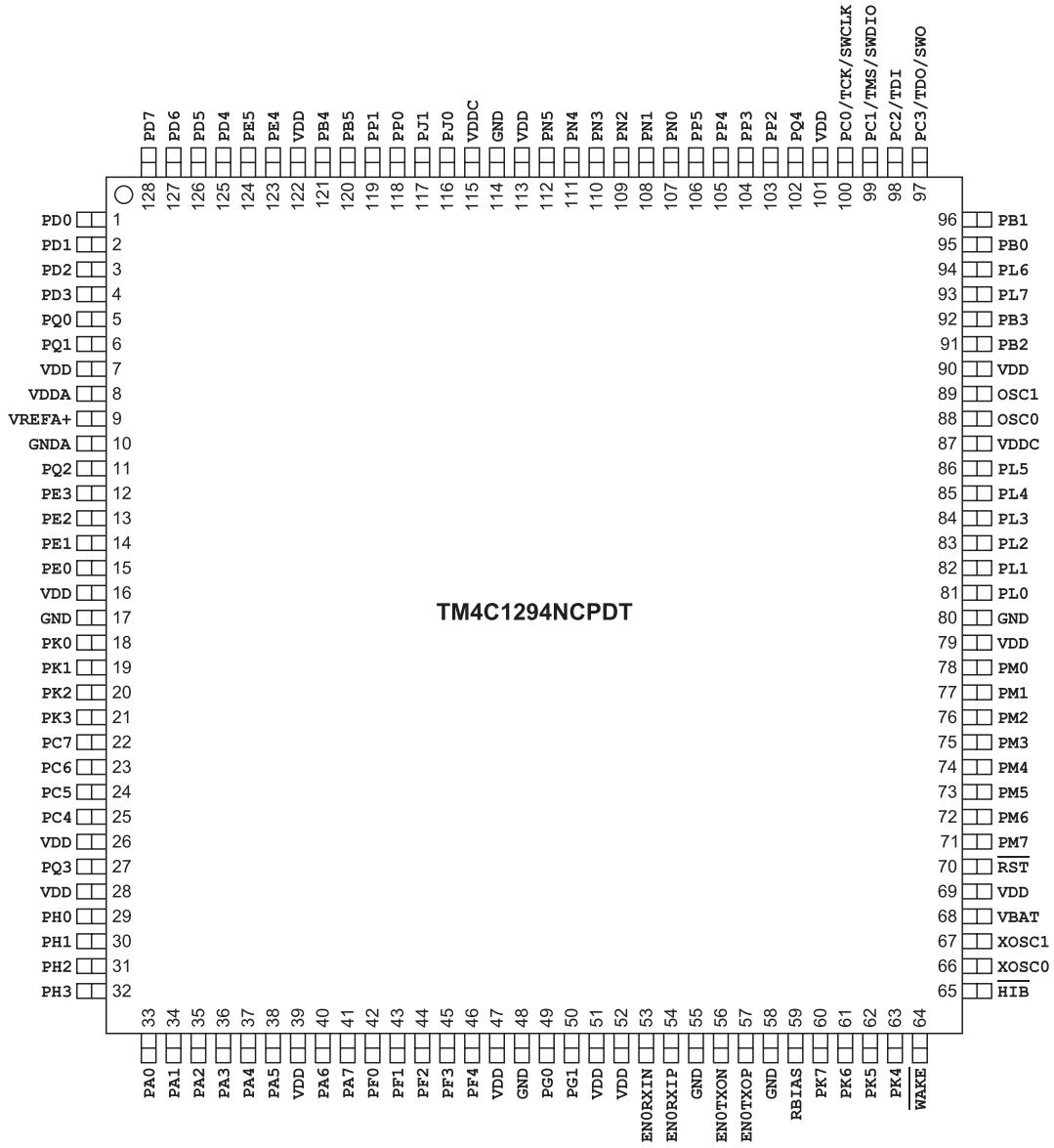
25 Pin Diagram

The TM4C1294NCPDT microcontroller pin diagram is shown below.

Each GPIO signal is identified by its GPIO port unless it defaults to an alternate function on reset. In this case, the GPIO port name is followed by the default alternate function. To see a complete list of possible functions for each pin, see Table 26-5 on page 1808.

Figure 25-1. 128-Pin TQFP Package Pin Diagram



26 Signal Tables

The following tables list the signals available for each pin. Signals are configured as GPIOs on reset, except for those noted below. Use the **GPIOAMSEL** register (see page 786) to select analog mode. For a GPIO pin to be used for an alternate digital function, the corresponding bit in the **GPIOAFSEL** register (see page 770) must be set. Further pin muxing options are provided through the PMCx bit field in the **GPIOPCTL** register (see page 787), which selects one of several available peripheral functions for that GPIO.

Important: Table 10-1 on page 743 shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL**=0, **GPIODEN**=0, **GPIOPDR**=0, **GPIOPUR**=0, and **GPIOPCTL**=0). Special consideration pins may be programed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset ($\overline{\text{POR}}$) returns these GPIO to their original special consideration state.

Table 26-1. GPIO Pins With Special Considerations

GPIO Pins	Default Reset State	GPIOAFSEL	GPIODEN	GPIOPDR	GPIOPUR	GPIOPCTL	GPIOCR
PC[3:0]	JTAG/SWD	1	1	0	1	0x1	0
PD[7]	GPIO[a]	0	0	0	0	0x0	0
PE[7]	GPIO[a]	0	0	0	0	0x0	0

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the **GPIOLOCK** register and uncommitting it by setting the **GPIOCR** register.

Table 26-2 on page 1773 shows the pin-to-signal-name mapping, including functional characteristics of the signals. Each possible alternate analog and digital function is listed for each pin.

Table 26-3 on page 1785 lists the signals in alphabetical order by signal name. If it is possible for a signal to be on multiple pins, each possible pin assignment is listed. The "Pin Mux" column indicates the GPIO and the encoding needed in the PMCx bit field in the **GPIOPCTL** register.

Table 26-4 on page 1797 groups the signals by functionality, except for GPIOs. If it is possible for a signal to be on multiple pins, each possible pin assignment is listed.

Table 26-5 on page 1808 lists the GPIO pins and their analog and digital alternate functions. The AINx analog signals go through an isolation circuit before reaching their circuitry. These signals are configured by clearing the corresponding DEN bit in the **GPIO Digital Enable (GPIODEN)** register and setting the corresponding AMSEL bit in the **GPIO Analog Mode Select (GPIOAMSEL)** register. Other analog signals are 3.3-V tolerant and are connected directly to their circuitry (C0-, C0+, C1-, C1+, C2-, C2+, USB0VBUS, USB0ID). These signals are configured by clearing the DEN bit in the **GPIO Digital Enable (GPIODEN)** register. The digital signals are enabled by setting the appropriate bit in the **GPIO Alternate Function Select (GPIOAFSEL)** and **GPIODEN** registers and configuring the PMCx bit field in the **GPIO Port Control (GPIOPCTL)** register to the numeric enoding shown in the table below. Table entries that are shaded gray are the default values for the corresponding GPIO pin.

Table 26-6 on page 1811 lists the signals based on number of possible pin assignments. This table can be used to plan how to configure the pins for a particular functionality. Application Note AN01274 Configuring Tiva™ C Series Microcontrollers with Pin Multiplexing provides an overview of the pin muxing implementation, an explanation of how a system designer defines a pin configuration, and examples of the pin configuration process.

Note: All digital inputs are Schmitt triggered.

26.1 Signals by Pin Number

Table 26-2. Signals by Pin Number

Pin Number	Pin Name	Pin Type	Buffer Type	Description
1	PD0	I/O	TTL	GPIO port D bit 0.
	AIN15	I	Analog	Analog-to-digital converter input 15.
	C0o	O	TTL	Analog comparator 0 output.
	I2C7SCL	I/O	OD	I^2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI2XDAT1	I/O	TTL	SSI Module 2 Bi-directional Data Pin 1 (SSI2RX in Legacy SSI Mode).
	T0CCP0	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
2	PD1	I/O	TTL	GPIO port D bit 1.
	AIN14	I	Analog	Analog-to-digital converter input 14.
	C1o	O	TTL	Analog comparator 1 output.
	I2C7SDA	I/O	OD	I^2C module 7 data.
	SSI2XDAT0	I/O	TTL	SSI Module 2 Bi-directional Data Pin 0 (SSI2TX in Legacy SSI Mode).
	T0CCP1	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
3	PD2	I/O	TTL	GPIO port D bit 2.
	AIN13	I	Analog	Analog-to-digital converter input 13.
	C2o	O	TTL	Analog comparator 2 output.
	I2C8SCL	I/O	OD	I^2C module 8 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI2Fss	I/O	TTL	SSI module 2 frame signal.
	T1CCP0	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
4	PD3	I/O	TTL	GPIO port D bit 3.
	AIN12	I	Analog	Analog-to-digital converter input 12.
	I2C8SDA	I/O	OD	I^2C module 8 data.
	SSI2Clk	I/O	TTL	SSI module 2 clock.
	T1CCP1	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
5	PQ0	I/O	TTL	GPIO port Q bit 0.
	EPI0S20	I/O	TTL	EPI module 0 signal 20.
	SSI3Clk	I/O	TTL	SSI module 3 clock.
6	PQ1	I/O	TTL	GPIO port Q bit 1.
	EPI0S21	I/O	TTL	EPI module 0 signal 21.
	SSI3Fss	I/O	TTL	SSI module 3 frame signal.
7	VDD	-	Power	Positive supply for I/O and some logic.
8	VDDA	-	Power	The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in , regardless of system implementation.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
9	VREFA+	-	Analog	A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with GNDA. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in Table 27-44 on page 1861.
10	GNDA	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
11	PQ2	I/O	TTL	GPIO port Q bit 2.
	EPI0S22	I/O	TTL	EPI module 0 signal 22.
	SSI3XDAT0	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
12	PE3	I/O	TTL	GPIO port E bit 3.
	AIN0	I	Analog	Analog-to-digital converter input 0.
	U1DTR	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
13	PE2	I/O	TTL	GPIO port E bit 2.
	AIN1	I	Analog	Analog-to-digital converter input 1.
	U1DCD	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
14	PE1	I/O	TTL	GPIO port E bit 1.
	AIN2	I	Analog	Analog-to-digital converter input 2.
	U1DSR	I	TTL	UART module 1 Data Set Ready modem output control line.
15	PE0	I/O	TTL	GPIO port E bit 0.
	AIN3	I	Analog	Analog-to-digital converter input 3.
	U1RTS	O	TTL	UART module 1 Request to Send modem flow control output line.
16	VDD	-	Power	Positive supply for I/O and some logic.
17	GND	-	Power	Ground reference for logic and I/O pins.
18	PK0	I/O	TTL	GPIO port K bit 0.
	AIN16	I	Analog	Analog-to-digital converter input 16.
	EPI0S0	I/O	TTL	EPI module 0 signal 0.
	U4Rx	I	TTL	UART module 4 receive.
19	PK1	I/O	TTL	GPIO port K bit 1.
	AIN17	I	Analog	Analog-to-digital converter input 17.
	EPI0S1	I/O	TTL	EPI module 0 signal 1.
	U4Tx	O	TTL	UART module 4 transmit.
20	PK2	I/O	TTL	GPIO port K bit 2.
	AIN18	I	Analog	Analog-to-digital converter input 18.
	EPI0S2	I/O	TTL	EPI module 0 signal 2.
	U4RTS	O	TTL	UART module 4 Request to Send modem flow control output line.
21	PK3	I/O	TTL	GPIO port K bit 3.
	AIN19	I	Analog	Analog-to-digital converter input 19.
	EPI0S3	I/O	TTL	EPI module 0 signal 3.
	U4CTS	I	TTL	UART module 4 Clear To Send modem flow control input signal.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
22	PC7	I/O	TTL	GPIO port C bit 7.
	C0-	I	Analog	Analog comparator 0 negative input.
	EPI0S4	I/O	TTL	EPI module 0 signal 4.
	U5Tx	O	TTL	UART module 5 transmit.
23	PC6	I/O	TTL	GPIO port C bit 6.
	C0+	I	Analog	Analog comparator 0 positive input.
	EPI0S5	I/O	TTL	EPI module 0 signal 5.
	U5Rx	I	TTL	UART module 5 receive.
24	PC5	I/O	TTL	GPIO port C bit 5.
	C1+	I	Analog	Analog comparator 1 positive input.
	EPI0S6	I/O	TTL	EPI module 0 signal 6.
	RTCCLK	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
	U7Tx	O	TTL	UART module 7 transmit.
25	PC4	I/O	TTL	GPIO port C bit 4.
	C1-	I	Analog	Analog comparator 1 negative input.
	EPI0S7	I/O	TTL	EPI module 0 signal 7.
	U7Rx	I	TTL	UART module 7 receive.
26	VDD	-	Power	Positive supply for I/O and some logic.
27	PQ3	I/O	TTL	GPIO port Q bit 3.
	EPI0S23	I/O	TTL	EPI module 0 signal 23.
	SSI3XDAT1	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
28	VDD	-	Power	Positive supply for I/O and some logic.
29	PH0	I/O	TTL	GPIO port H bit 0.
	EPI0S0	I/O	TTL	EPI module 0 signal 0.
	U0RTS	O	TTL	UART module 0 Request to Send modem flow control output signal.
30	PH1	I/O	TTL	GPIO port H bit 1.
	EPI0S1	I/O	TTL	EPI module 0 signal 1.
	U0CTS	I	TTL	UART module 0 Clear To Send modem flow control input signal.
31	PH2	I/O	TTL	GPIO port H bit 2.
	EPI0S2	I/O	TTL	EPI module 0 signal 2.
	U0DCD	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
32	PH3	I/O	TTL	GPIO port H bit 3.
	EPI0S3	I/O	TTL	EPI module 0 signal 3.
	U0DSR	I	TTL	UART module 0 Data Set Ready modem output control line.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
33	PA0	I/O	TTL	GPIO port A bit 0.
	CAN0Rx	I	TTL	CAN module 0 receive.
	I2C9SCL	I/O	OD	I^2C module 9 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	T0CCP0	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
	U0Rx	I	TTL	UART module 0 receive.
34	PA1	I/O	TTL	GPIO port A bit 1.
	CAN0Tx	O	TTL	CAN module 0 transmit.
	I2C9SDA	I/O	OD	I^2C module 9 data.
	T0CCP1	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
	U0Tx	O	TTL	UART module 0 transmit.
35	PA2	I/O	TTL	GPIO port A bit 2.
	I2C8SCL	I/O	OD	I^2C module 8 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI0Clk	I/O	TTL	SSI module 0 clock
	T1CCP0	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
	U4Rx	I	TTL	UART module 4 receive.
36	PA3	I/O	TTL	GPIO port A bit 3.
	I2C8SDA	I/O	OD	I^2C module 8 data.
	SSI0Fss	I/O	TTL	SSI module 0 frame signal
	T1CCP1	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
	U4Tx	O	TTL	UART module 4 transmit.
37	PA4	I/O	TTL	GPIO port A bit 4.
	I2C7SCL	I/O	OD	I^2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI0XDAT0	I/O	TTL	SSI Module 0 Bi-directional Data Pin 0 (SSI0TX in Legacy SSI Mode).
	T2CCP0	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
	U3Rx	I	TTL	UART module 3 receive.
38	PA5	I/O	TTL	GPIO port A bit 5.
	I2C7SDA	I/O	OD	I^2C module 7 data.
	SSI0XDAT1	I/O	TTL	SSI Module 0 Bi-directional Data Pin 1 (SSI0RX in Legacy SSI Mode).
	T2CCP1	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.
	U3Tx	O	TTL	UART module 3 transmit.
39	VDD	-	Power	Positive supply for I/O and some logic.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
40	PA6	I/O	TTL	GPIO port A bit 6.
	EPI0S8	I/O	TTL	EPI module 0 signal 8.
	I2C6SCL	I/O	OD	I^2C module 6 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI0XDAT2	I/O	TTL	SSI Module 0 Bi-directional Data Pin 2.
	T3CCP0	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
	U2Rx	I	TTL	UART module 2 receive.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
41	PA7	I/O	TTL	GPIO port A bit 7.
	EPI0S9	I/O	TTL	EPI module 0 signal 9.
	I2C6SDA	I/O	OD	I^2C module 6 data.
	SSI0XDAT3	I/O	TTL	SSI Module 0 Bi-directional Data Pin 3.
	T3CCP1	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
	U2Tx	O	TTL	UART module 2 transmit.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
	USB0PFLT	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.
42	PF0	I/O	TTL	GPIO port F bit 0.
	EN0LED0	O	TTL	Ethernet 0 LED 0.
	M0PWM0	O	TTL	Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.
	SSI3XDAT1	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
	TRD2	O	TTL	Trace data 2.
43	PF1	I/O	TTL	GPIO port F bit 1.
	EN0LED2	O	TTL	Ethernet 0 LED 2.
	M0PWM1	O	TTL	Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.
	SSI3XDAT0	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
	TRD1	O	TTL	Trace data 1.
44	PF2	I/O	TTL	GPIO port F bit 2.
	M0PWM2	O	TTL	Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.
	SSI3Fss	I/O	TTL	SSI module 3 frame signal.
	TRD0	O	TTL	Trace data 0.
45	PF3	I/O	TTL	GPIO port F bit 3.
	M0PWM3	O	TTL	Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.
	SSI3Clk	I/O	TTL	SSI module 3 clock.
	TRCLK	O	TTL	Trace clock.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
46	PF4	I/O	TTL	GPIO port F bit 4.
	EN0LED1	O	TTL	Ethernet 0 LED 1.
	M0FAULT0	I	TTL	Motion Control Module 0 PWM Fault 0.
	SSI3XDAT2	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
	TRD3	O	TTL	Trace data 3.
47	VDD	-	Power	Positive supply for I/O and some logic.
48	GND	-	Power	Ground reference for logic and I/O pins.
49	PG0	I/O	TTL	GPIO port G bit 0.
	EN0PPS	O	TTL	Ethernet 0 Pulse-Per-Second (PPS) Output.
	EPI0S11	I/O	TTL	EPI module 0 signal 11.
	I2C1SCL	I/O	OD	I^2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M0PWM4	O	TTL	Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.
50	PG1	I/O	TTL	GPIO port G bit 1.
	EPI0S10	I/O	TTL	EPI module 0 signal 10.
	I2C1SDA	I/O	OD	I^2C module 1 data.
	M0PWM5	O	TTL	Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.
51	VDD	-	Power	Positive supply for I/O and some logic.
52	VDD	-	Power	Positive supply for I/O and some logic.
53	EN0RXIN	I/O	TTL	Ethernet PHY negative receive differential input.
54	EN0RXIP	I/O	TTL	Ethernet PHY positive receive differential input.
55	GND	-	Power	Ground reference for logic and I/O pins.
56	EN0TXON	I/O	TTL	Ethernet PHY negative transmit differential output.
57	EN0TXOP	I/O	TTL	Ethernet PHY positive transmit differential output.
58	GND	-	Power	Ground reference for logic and I/O pins.
59	RBIAS	O	Analog	4.87-kΩ resistor (1% precision) for Ethernet PHY.
60	PK7	I/O	TTL	GPIO port K bit 7.
	EPI0S24	I/O	TTL	EPI module 0 signal 24.
	I2C4SDA	I/O	OD	I^2C module 4 data.
	M0FAULT2	I	TTL	Motion Control Module 0 PWM Fault 2.
	RTCCLK	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
	U0RI	I	TTL	UART module 0 Ring Indicator modem status input signal.
61	PK6	I/O	TTL	GPIO port K bit 6.
	EN0LED1	O	TTL	Ethernet 0 LED 1.
	EPI0S25	I/O	TTL	EPI module 0 signal 25.
	I2C4SCL	I/O	OD	I^2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M0FAULT1	I	TTL	Motion Control Module 0 PWM Fault 1.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
62	PK5	I/O	TTL	GPIO port K bit 5.
	EN0LED2	O	TTL	Ethernet 0 LED 2.
	EPI0S31	I/O	TTL	EPI module 0 signal 31.
	I2C3SDA	I/O	OD	I^2C module 3 data.
	M0PWM7	O	TTL	Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.
63	PK4	I/O	TTL	GPIO port K bit 4.
	EN0LED0	O	TTL	Ethernet 0 LED 0.
	EPI0S32	I/O	TTL	EPI module 0 signal 32.
	I2C3SCL	I/O	OD	I^2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	M0PWM6	O	TTL	Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.
64	$\overline{\text{WAKE}}$	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
65	$\overline{\text{HIB}}$	O	TTL	An output that indicates the processor is in Hibernate mode.
66	XOSC0	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a crystal or a 32.768-kHz oscillator for the Hibernation module RTC.
67	XOSC1	O	Analog	Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.
68	VBAT	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
69	VDD	-	Power	Positive supply for I/O and some logic.
70	$\overline{\text{RST}}$	I	TTL	System reset input.
71	PM7	I/O	TTL	GPIO port M bit 7.
	T5CCP1	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.
	TMPR0	I/O	TTL	Tamper signal 0.
	U0RI	I	TTL	UART module 0 Ring Indicator modem status input signal.
72	PM6	I/O	TTL	GPIO port M bit 6.
	T5CCP0	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
	TMPR1	I/O	TTL	Tamper signal 1.
	U0DSR	I	TTL	UART module 0 Data Set Ready modem output control line.
73	PM5	I/O	TTL	GPIO port M bit 5.
	T4CCP1	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	TMPR2	I/O	TTL	Tamper signal 2.
	U0DCD	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
74	PM4	I/O	TTL	GPIO port M bit 4.
	T4CCP0	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	TMPR3	I/O	TTL	Tamper signal 3.
	U0CTS	I	TTL	UART module 0 Clear To Send modem flow control input signal.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
75	PM3	I/O	TTL	GPIO port M bit 3.
	EPI0S12	I/O	TTL	EPI module 0 signal 12.
	T3CCP1	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
76	PM2	I/O	TTL	GPIO port M bit 2.
	EPI0S13	I/O	TTL	EPI module 0 signal 13.
	T3CCP0	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
77	PM1	I/O	TTL	GPIO port M bit 1.
	EPI0S14	I/O	TTL	EPI module 0 signal 14.
	T2CCP1	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.
78	PM0	I/O	TTL	GPIO port M bit 0.
	EPI0S15	I/O	TTL	EPI module 0 signal 15.
	T2CCP0	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
79	VDD	-	Power	Positive supply for I/O and some logic.
80	GND	-	Power	Ground reference for logic and I/O pins.
81	PL0	I/O	TTL	GPIO port L bit 0.
	EPI0S16	I/O	TTL	EPI module 0 signal 16.
	I2C2SDA	I/O	OD	I^2C module 2 data.
	M0FAULT3	I	TTL	Motion Control Module 0 PWM Fault 3.
	USB0D0	I/O	TTL	USB data 0.
82	PL1	I/O	TTL	GPIO port L bit 1.
	EPI0S17	I/O	TTL	EPI module 0 signal 17.
	I2C2SCL	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	PhA0	I	TTL	QEI module 0 phase A.
	USB0D1	I/O	TTL	USB data 1.
83	PL2	I/O	TTL	GPIO port L bit 2.
	C0o	O	TTL	Analog comparator 0 output.
	EPI0S18	I/O	TTL	EPI module 0 signal 18.
	PhB0	I	TTL	QEI module 0 phase B.
	USB0D2	I/O	TTL	USB data 2.
84	PL3	I/O	TTL	GPIO port L bit 3.
	C1o	O	TTL	Analog comparator 1 output.
	EPI0S19	I/O	TTL	EPI module 0 signal 19.
	IDX0	I	TTL	QEI module 0 index.
	USB0D3	I/O	TTL	USB data 3.
85	PL4	I/O	TTL	GPIO port L bit 4.
	EPI0S26	I/O	TTL	EPI module 0 signal 26.
	T0CCP0	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
	USB0D4	I/O	TTL	USB data 4.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
86	PL5	I/O	TTL	GPIO port L bit 5.
	EPI0S33	I/O	TTL	EPI module 0 signal 33.
	T0CCP1	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
	USB0D5	I/O	TTL	USB data 5.
87	VDDC	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 27-15 on page 1834 .
88	OSC0	I	Analog	Main oscillator crystal input or an external clock reference input.
89	OSC1	O	Analog	Main oscillator crystal output. Leave unconnected when using a single-ended clock source.
90	VDD	-	Power	Positive supply for I/O and some logic.
91	PB2	I/O	TTL	GPIO port B bit 2.
	EPI0S27	I/O	TTL	EPI module 0 signal 27.
	I2C0SCL	I/O	OD	I^2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	T5CCP0	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
	USB0STP	O	TTL	Asserted by the USB controller to signal the end of a USB transmit packet or register write operation.
92	PB3	I/O	TTL	GPIO port B bit 3.
	EPI0S28	I/O	TTL	EPI module 0 signal 28.
	I2C0SDA	I/O	OD	I^2C module 0 data.
	T5CCP1	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.
	USB0CLK	O	TTL	60-MHz clock to the external PHY.
93	PL7	I/O	TTL	GPIO port L bit 7.
	T1CCP1	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
	USB0DM	I/O	Analog	Bidirectional differential data pin (D- per USB specification) for USB0.
94	PL6	I/O	TTL	GPIO port L bit 6.
	T1CCP0	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
	USB0DP	I/O	Analog	Bidirectional differential data pin (D+ per USB specification) for USB0.
95	PB0	I/O	TTL	GPIO port B bit 0.
	CAN1Rx	I	TTL	CAN module 1 receive.
	I2C5SCL	I/O	OD	I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	T4CCP0	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	U1Rx	I	TTL	UART module 1 receive.
	USB0ID	I	Analog	This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
96	PB1	I/O	TTL	GPIO port B bit 1.
	CAN1Tx	O	TTL	CAN module 1 transmit.
	I2C5SDA	I/O	OD	I^2C module 5 data.
	T4CCP1	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	U1Tx	O	TTL	UART module 1 transmit.
	USB0VBUS	I/O	Analog	This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.
97	PC3	I/O	TTL	GPIO port C bit 3.
	SWO	O	TTL	JTAG TDO and SWO.
	TDO	O	TTL	JTAG TDO and SWO.
98	PC2	I/O	TTL	GPIO port C bit 2.
	TDI	I	TTL	JTAG TDI.
99	PC1	I/O	TTL	GPIO port C bit 1.
	SWDIO	I/O	TTL	JTAG TMS and SWDIO.
	TMS	I	TTL	JTAG TMS and SWDIO.
100	PC0	I/O	TTL	GPIO port C bit 0.
	SWCLK	I	TTL	JTAG/SWD CLK.
	TCK	I	TTL	JTAG/SWD CLK.
101	VDD	-	Power	Positive supply for I/O and some logic.
102	PQ4	I/O	TTL	GPIO port Q bit 4.
	DIVSCLK	O	TTL	An optionally divided reference clock output based on a selected clock source. Note that this signal is not synchronized to the System Clock.
	U1Rx	I	TTL	UART module 1 receive.
103	PP2	I/O	TTL	GPIO port P bit 2.
	EPI0S29	I/O	TTL	EPI module 0 signal 29.
	U0DTR	O	TTL	UART module 0 Data Terminal Ready modem status input signal.
	USB0NXT	O	TTL	Asserted by the external PHY to throttle all data types.
104	PP3	I/O	TTL	GPIO port P bit 3.
	EPI0S30	I/O	TTL	EPI module 0 signal 30.
	RTCCLK	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
	U0DCD	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
	U1CTS	I	TTL	UART module 1 Clear To Send modem flow control input signal.
	USB0DIR	O	TTL	Indicates that the external PHY is able to accept data from the USB controller.
105	PP4	I/O	TTL	GPIO port P bit 4.
	U0DSR	I	TTL	UART module 0 Data Set Ready modem output control line.
	U3RTS	O	TTL	UART module 3 Request to Send modem flow control output line.
	USB0D7	I/O	TTL	USB data 7.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
106	PP5	I/O	TTL	GPIO port P bit 5.
	I2C2SCL	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	U3CTS	I	TTL	UART module 3 Clear To Send modem flow control input signal.
	USB0D6	I/O	TTL	USB data 6.
107	PN0	I/O	TTL	GPIO port N bit 0.
	U1RTS	O	TTL	UART module 1 Request to Send modem flow control output line.
108	PN1	I/O	TTL	GPIO port N bit 1.
	U1CTS	I	TTL	UART module 1 Clear To Send modem flow control input signal.
109	PN2	I/O	TTL	GPIO port N bit 2.
	EPI0S29	I/O	TTL	EPI module 0 signal 29.
	U1DCD	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
	U2RTS	O	TTL	UART module 2 Request to Send modem flow control output line.
110	PN3	I/O	TTL	GPIO port N bit 3.
	EPI0S30	I/O	TTL	EPI module 0 signal 30.
	U1DSR	I	TTL	UART module 1 Data Set Ready modem output control line.
	U2CTS	I	TTL	UART module 2 Clear To Send modem flow control input signal.
111	PN4	I/O	TTL	GPIO port N bit 4.
	EPI0S34	I/O	TTL	EPI module 0 signal 34.
	I2C2SDA	I/O	OD	I^2C module 2 data.
	U1DTR	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
	U3RTS	O	TTL	UART module 3 Request to Send modem flow control output line.
112	PN5	I/O	TTL	GPIO port N bit 5.
	EPI0S35	I/O	TTL	EPI module 0 signal 35.
	I2C2SCL	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	U1RI	I	TTL	UART module 1 Ring Indicator modem status input signal.
	U3CTS	I	TTL	UART module 3 Clear To Send modem flow control input signal.
113	VDD	-	Power	Positive supply for I/O and some logic.
114	GND	-	Power	Ground reference for logic and I/O pins.
115	VDDC	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 27-15 on page 1834 .
116	PJ0	I/O	TTL	GPIO port J bit 0.
	EN0PPS	O	TTL	Ethernet 0 Pulse-Per-Second (PPS) Output.
	U3Rx	I	TTL	UART module 3 receive.
117	PJ1	I/O	TTL	GPIO port J bit 1.
	U3Tx	O	TTL	UART module 3 transmit.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
118	PP0	I/O	TTL	GPIO port P bit 0.
	C2+	I	Analog	Analog comparator 2 positive input.
	SSI3XDAT2	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
	U6Rx	I	TTL	UART module 6 receive.
119	PP1	I/O	TTL	GPIO port P bit 1.
	C2-	I	Analog	Analog comparator 2 negative input.
	SSI3XDAT3	I/O	TTL	SSI Module 3 Bi-directional Data Pin 3.
	U6Tx	O	TTL	UART module 6 transmit.
120	PB5	I/O	TTL	GPIO port B bit 5.
	AIN11	I	Analog	Analog-to-digital converter input 11.
	I2C5SDA	I/O	OD	I^2C module 5 data.
	SSI1Clk	I/O	TTL	SSI module 1 clock.
	U0RTS	O	TTL	UART module 0 Request to Send modem flow control output signal.
121	PB4	I/O	TTL	GPIO port B bit 4.
	AIN10	I	Analog	Analog-to-digital converter input 10.
	I2C5SCL	I/O	OD	I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	SSI1Fss	I/O	TTL	SSI module 1 frame signal.
	U0CTS	I	TTL	UART module 0 Clear To Send modem flow control input signal.
122	VDD	-	Power	Positive supply for I/O and some logic.
123	PE4	I/O	TTL	GPIO port E bit 4.
	AIN9	I	Analog	Analog-to-digital converter input 9.
	SSI1XDAT0	I/O	TTL	SSI Module 1 Bi-directional Data Pin 0 (SSI1TX in Legacy SSI Mode).
	U1RI	I	TTL	UART module 1 Ring Indicator modem status input signal.
124	PE5	I/O	TTL	GPIO port E bit 5.
	AIN8	I	Analog	Analog-to-digital converter input 8.
	SSI1XDAT1	I/O	TTL	SSI Module 1 Bi-directional Data Pin 1 (SSI1RX in Legacy SSI Mode).
125	PD4	I/O	TTL	GPIO port D bit 4.
	AIN7	I	Analog	Analog-to-digital converter input 7.
	SSI1XDAT2	I/O	TTL	SSI Module 1 Bi-directional Data Pin 2.
	T3CCP0	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
	U2Rx	I	TTL	UART module 2 receive.
126	PD5	I/O	TTL	GPIO port D bit 5.
	AIN6	I	Analog	Analog-to-digital converter input 6.
	SSI1XDAT3	I/O	TTL	SSI Module 1 Bi-directional Data Pin 3.
	T3CCP1	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
	U2Tx	O	TTL	UART module 2 transmit.

Table 26-2. Signals by Pin Number *(continued)*

Pin Number	Pin Name	Pin Type	Buffer Type	Description
127	PD6	I/O	TTL	GPIO port D bit 6.
	AIN5	I	Analog	Analog-to-digital converter input 5.
	SSI2XDAT3	I/O	TTL	SSI Module 2 Bi-directional Data Pin 3.
	T4CCP0	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	U2RTS	O	TTL	UART module 2 Request to Send modem flow control output line.
	USB0EPEN	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
128	PD7	I/O	TTL	GPIO port D bit 7.
	AIN4	I	Analog	Analog-to-digital converter input 4.
	NMI	I	TTL	Non-maskable interrupt.
	SSI2XDAT2	I/O	TTL	SSI Module 2 Bi-directional Data Pin 2.
	T4CCP1	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	U2CTS	I	TTL	UART module 2 Clear To Send modem flow control input signal.
	USB0PFLT	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.

26.2 Signals by Signal Name

Table 26-3. Signals by Signal Name

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
AIN0	12	PE3	I	Analog	Analog-to-digital converter input 0.
AIN1	13	PE2	I	Analog	Analog-to-digital converter input 1.
AIN2	14	PE1	I	Analog	Analog-to-digital converter input 2.
AIN3	15	PE0	I	Analog	Analog-to-digital converter input 3.
AIN4	128	PD7	I	Analog	Analog-to-digital converter input 4.
AIN5	127	PD6	I	Analog	Analog-to-digital converter input 5.
AIN6	126	PD5	I	Analog	Analog-to-digital converter input 6.
AIN7	125	PD4	I	Analog	Analog-to-digital converter input 7.
AIN8	124	PE5	I	Analog	Analog-to-digital converter input 8.
AIN9	123	PE4	I	Analog	Analog-to-digital converter input 9.
AIN10	121	PB4	I	Analog	Analog-to-digital converter input 10.
AIN11	120	PB5	I	Analog	Analog-to-digital converter input 11.
AIN12	4	PD3	I	Analog	Analog-to-digital converter input 12.
AIN13	3	PD2	I	Analog	Analog-to-digital converter input 13.
AIN14	2	PD1	I	Analog	Analog-to-digital converter input 14.
AIN15	1	PD0	I	Analog	Analog-to-digital converter input 15.
AIN16	18	PK0	I	Analog	Analog-to-digital converter input 16.
AIN17	19	PK1	I	Analog	Analog-to-digital converter input 17.
AIN18	20	PK2	I	Analog	Analog-to-digital converter input 18.
AIN19	21	PK3	I	Analog	Analog-to-digital converter input 19.
C0+	23	PC6	I	Analog	Analog comparator 0 positive input.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
C0-	22	PC7	I	Analog	Analog comparator 0 negative input.
C0o	1 83	PD0 (5) PL2 (5)	O	TTL	Analog comparator 0 output.
C1+	24	PC5	I	Analog	Analog comparator 1 positive input.
C1-	25	PC4	I	Analog	Analog comparator 1 negative input.
C1o	2 84	PD1 (5) PL3 (5)	O	TTL	Analog comparator 1 output.
C2+	118	PP0	I	Analog	Analog comparator 2 positive input.
C2-	119	PP1	I	Analog	Analog comparator 2 negative input.
C2o	3	PD2 (5)	O	TTL	Analog comparator 2 output.
CAN0Rx	33	PA0 (7)	I	TTL	CAN module 0 receive.
CAN0Tx	34	PA1 (7)	O	TTL	CAN module 0 transmit.
CAN1Rx	95	PB0 (7)	I	TTL	CAN module 1 receive.
CAN1Tx	96	PB1 (7)	O	TTL	CAN module 1 transmit.
DIVSCLK	102	PQ4 (7)	O	TTL	An optionally divided reference clock output based on a selected clock source. Note that this signal is not synchronized to the System Clock.
EN0LED0	42 63	PF0 (5) PK4 (5)	O	TTL	Ethernet 0 LED 0.
EN0LED1	46 61	PF4 (5) PK6 (5)	O	TTL	Ethernet 0 LED 1.
EN0LED2	43 62	PF1 (5) PK5 (5)	O	TTL	Ethernet 0 LED 2.
EN0PPS	49 116	PG0 (5) PJ0 (5)	O	TTL	Ethernet 0 Pulse-Per-Second (PPS) Output.
EN0RXIN	53	fixed	I/O	TTL	Ethernet PHY negative receive differential input.
EN0RXIP	54	fixed	I/O	TTL	Ethernet PHY positive receive differential input.
EN0TXON	56	fixed	I/O	TTL	Ethernet PHY negative transmit differential output.
EN0TXOP	57	fixed	I/O	TTL	Ethernet PHY positive transmit differential output.
EPI0S0	18 29	PK0 (15) PH0 (15)	I/O	TTL	EPI module 0 signal 0.
EPI0S1	19 30	PK1 (15) PH1 (15)	I/O	TTL	EPI module 0 signal 1.
EPI0S2	20 31	PK2 (15) PH2 (15)	I/O	TTL	EPI module 0 signal 2.
EPI0S3	21 32	PK3 (15) PH3 (15)	I/O	TTL	EPI module 0 signal 3.
EPI0S4	22	PC7 (15)	I/O	TTL	EPI module 0 signal 4.
EPI0S5	23	PC6 (15)	I/O	TTL	EPI module 0 signal 5.
EPI0S6	24	PC5 (15)	I/O	TTL	EPI module 0 signal 6.
EPI0S7	25	PC4 (15)	I/O	TTL	EPI module 0 signal 7.
EPI0S8	40	PA6 (15)	I/O	TTL	EPI module 0 signal 8.
EPI0S9	41	PA7 (15)	I/O	TTL	EPI module 0 signal 9.
EPI0S10	50	PG1 (15)	I/O	TTL	EPI module 0 signal 10.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
EPI0S11	49	PG0 (15)	I/O	TTL	EPI module 0 signal 11.
EPI0S12	75	PM3 (15)	I/O	TTL	EPI module 0 signal 12.
EPI0S13	76	PM2 (15)	I/O	TTL	EPI module 0 signal 13.
EPI0S14	77	PM1 (15)	I/O	TTL	EPI module 0 signal 14.
EPI0S15	78	PM0 (15)	I/O	TTL	EPI module 0 signal 15.
EPI0S16	81	PL0 (15)	I/O	TTL	EPI module 0 signal 16.
EPI0S17	82	PL1 (15)	I/O	TTL	EPI module 0 signal 17.
EPI0S18	83	PL2 (15)	I/O	TTL	EPI module 0 signal 18.
EPI0S19	84	PL3 (15)	I/O	TTL	EPI module 0 signal 19.
EPI0S20	5	PQ0 (15)	I/O	TTL	EPI module 0 signal 20.
EPI0S21	6	PQ1 (15)	I/O	TTL	EPI module 0 signal 21.
EPI0S22	11	PQ2 (15)	I/O	TTL	EPI module 0 signal 22.
EPI0S23	27	PQ3 (15)	I/O	TTL	EPI module 0 signal 23.
EPI0S24	60	PK7 (15)	I/O	TTL	EPI module 0 signal 24.
EPI0S25	61	PK6 (15)	I/O	TTL	EPI module 0 signal 25.
EPI0S26	85	PL4 (15)	I/O	TTL	EPI module 0 signal 26.
EPI0S27	91	PB2 (15)	I/O	TTL	EPI module 0 signal 27.
EPI0S28	92	PB3 (15)	I/O	TTL	EPI module 0 signal 28.
EPI0S29	103 109	PP2 (15) PN2 (15)	I/O	TTL	EPI module 0 signal 29.
EPI0S30	104 110	PP3 (15) PN3 (15)	I/O	TTL	EPI module 0 signal 30.
EPI0S31	62	PK5 (15)	I/O	TTL	EPI module 0 signal 31.
EPI0S32	63	PK4 (15)	I/O	TTL	EPI module 0 signal 32.
EPI0S33	86	PL5 (15)	I/O	TTL	EPI module 0 signal 33.
EPI0S34	111	PN4 (15)	I/O	TTL	EPI module 0 signal 34.
EPI0S35	112	PN5 (15)	I/O	TTL	EPI module 0 signal 35.
GND	17 48 55 58 80 114	fixed	-	Power	Ground reference for logic and I/O pins.
GNDA	10	fixed	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
$\overline{\text{HIB}}$	65	fixed	O	TTL	An output that indicates the processor is in Hibernate mode.
I2C0SCL	91	PB2 (2)	I/O	OD	I^2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C0SDA	92	PB3 (2)	I/O	OD	I^2C module 0 data.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
I2C1SCL	49	PG0 (2)	I/O	OD	I^2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C1SDA	50	PG1 (2)	I/O	OD	I^2C module 1 data.
I2C2SCL	82 106 112	PL1 (2) PP5 (2) PN5 (3)	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C2SDA	81 111	PL0 (2) PN4 (3)	I/O	OD	I^2C module 2 data.
I2C3SCL	63	PK4 (2)	I/O	OD	I^2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C3SDA	62	PK5 (2)	I/O	OD	I^2C module 3 data.
I2C4SCL	61	PK6 (2)	I/O	OD	I^2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C4SDA	60	PK7 (2)	I/O	OD	I^2C module 4 data.
I2C5SCL	95 121	PB0 (2) PB4 (2)	I/O	OD	I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C5SDA	96 120	PB1 (2) PB5 (2)	I/O	OD	I^2C module 5 data.
I2C6SCL	40	PA6 (2)	I/O	OD	I^2C module 6 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C6SDA	41	PA7 (2)	I/O	OD	I^2C module 6 data.
I2C7SCL	1 37	PD0 (2) PA4 (2)	I/O	OD	I^2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C7SDA	2 38	PD1 (2) PA5 (2)	I/O	OD	I^2C module 7 data.
I2C8SCL	3 35	PD2 (2) PA2 (2)	I/O	OD	I^2C module 8 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C8SDA	4 36	PD3 (2) PA3 (2)	I/O	OD	I^2C module 8 data.
I2C9SCL	33	PA0 (2)	I/O	OD	I^2C module 9 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
I2C9SDA	34	PA1 (2)	I/O	OD	I^2C module 9 data.
IDX0	84	PL3 (6)	I	TTL	QEI module 0 index.
M0FAULT0	46	PF4 (6)	I	TTL	Motion Control Module 0 PWM Fault 0.
M0FAULT1	61	PK6 (6)	I	TTL	Motion Control Module 0 PWM Fault 1.
M0FAULT2	60	PK7 (6)	I	TTL	Motion Control Module 0 PWM Fault 2.
M0FAULT3	81	PL0 (6)	I	TTL	Motion Control Module 0 PWM Fault 3.
M0PWM0	42	PF0 (6)	O	TTL	Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
M0PWM1	43	PF1 (6)	O	TTL	Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.
M0PWM2	44	PF2 (6)	O	TTL	Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.
M0PWM3	45	PF3 (6)	O	TTL	Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.
M0PWM4	49	PG0 (6)	O	TTL	Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.
M0PWM5	50	PG1 (6)	O	TTL	Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.
M0PWM6	63	PK4 (6)	O	TTL	Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.
M0PWM7	62	PK5 (6)	O	TTL	Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.
NMI	128	PD7 (8)	I	TTL	Non-maskable interrupt.
OSC0	88	fixed	I	Analog	Main oscillator crystal input or an external clock reference input.
OSC1	89	fixed	O	Analog	Main oscillator crystal output. Leave unconnected when using a single-ended clock source.
PA0	33	-	I/O	TTL	GPIO port A bit 0.
PA1	34	-	I/O	TTL	GPIO port A bit 1.
PA2	35	-	I/O	TTL	GPIO port A bit 2.
PA3	36	-	I/O	TTL	GPIO port A bit 3.
PA4	37	-	I/O	TTL	GPIO port A bit 4.
PA5	38	-	I/O	TTL	GPIO port A bit 5.
PA6	40	-	I/O	TTL	GPIO port A bit 6.
PA7	41	-	I/O	TTL	GPIO port A bit 7.
PB0	95	-	I/O	TTL	GPIO port B bit 0.
PB1	96	-	I/O	TTL	GPIO port B bit 1.
PB2	91	-	I/O	TTL	GPIO port B bit 2.
PB3	92	-	I/O	TTL	GPIO port B bit 3.
PB4	121	-	I/O	TTL	GPIO port B bit 4.
PB5	120	-	I/O	TTL	GPIO port B bit 5.
PC0	100	-	I/O	TTL	GPIO port C bit 0.
PC1	99	-	I/O	TTL	GPIO port C bit 1.
PC2	98	-	I/O	TTL	GPIO port C bit 2.
PC3	97	-	I/O	TTL	GPIO port C bit 3.
PC4	25	-	I/O	TTL	GPIO port C bit 4.
PC5	24	-	I/O	TTL	GPIO port C bit 5.
PC6	23	-	I/O	TTL	GPIO port C bit 6.
PC7	22	-	I/O	TTL	GPIO port C bit 7.
PD0	1	-	I/O	TTL	GPIO port D bit 0.
PD1	2	-	I/O	TTL	GPIO port D bit 1.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
PD2	3	-	I/O	TTL	GPIO port D bit 2.
PD3	4	-	I/O	TTL	GPIO port D bit 3.
PD4	125	-	I/O	TTL	GPIO port D bit 4.
PD5	126	-	I/O	TTL	GPIO port D bit 5.
PD6	127	-	I/O	TTL	GPIO port D bit 6.
PD7	128	-	I/O	TTL	GPIO port D bit 7.
PE0	15	-	I/O	TTL	GPIO port E bit 0.
PE1	14	-	I/O	TTL	GPIO port E bit 1.
PE2	13	-	I/O	TTL	GPIO port E bit 2.
PE3	12	-	I/O	TTL	GPIO port E bit 3.
PE4	123	-	I/O	TTL	GPIO port E bit 4.
PE5	124	-	I/O	TTL	GPIO port E bit 5.
PF0	42	-	I/O	TTL	GPIO port F bit 0.
PF1	43	-	I/O	TTL	GPIO port F bit 1.
PF2	44	-	I/O	TTL	GPIO port F bit 2.
PF3	45	-	I/O	TTL	GPIO port F bit 3.
PF4	46	-	I/O	TTL	GPIO port F bit 4.
PG0	49	-	I/O	TTL	GPIO port G bit 0.
PG1	50	-	I/O	TTL	GPIO port G bit 1.
PH0	29	-	I/O	TTL	GPIO port H bit 0.
PH1	30	-	I/O	TTL	GPIO port H bit 1.
PH2	31	-	I/O	TTL	GPIO port H bit 2.
PH3	32	-	I/O	TTL	GPIO port H bit 3.
PhA0	82	PL1 (6)	I	TTL	QEI module 0 phase A.
PhB0	83	PL2 (6)	I	TTL	QEI module 0 phase B.
PJ0	116	-	I/O	TTL	GPIO port J bit 0.
PJ1	117	-	I/O	TTL	GPIO port J bit 1.
PK0	18	-	I/O	TTL	GPIO port K bit 0.
PK1	19	-	I/O	TTL	GPIO port K bit 1.
PK2	20	-	I/O	TTL	GPIO port K bit 2.
PK3	21	-	I/O	TTL	GPIO port K bit 3.
PK4	63	-	I/O	TTL	GPIO port K bit 4.
PK5	62	-	I/O	TTL	GPIO port K bit 5.
PK6	61	-	I/O	TTL	GPIO port K bit 6.
PK7	60	-	I/O	TTL	GPIO port K bit 7.
PL0	81	-	I/O	TTL	GPIO port L bit 0.
PL1	82	-	I/O	TTL	GPIO port L bit 1.
PL2	83	-	I/O	TTL	GPIO port L bit 2.
PL3	84	-	I/O	TTL	GPIO port L bit 3.
PL4	85	-	I/O	TTL	GPIO port L bit 4.
PL5	86	-	I/O	TTL	GPIO port L bit 5.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
PL6	94	-	I/O	TTL	GPIO port L bit 6.
PL7	93	-	I/O	TTL	GPIO port L bit 7.
PM0	78	-	I/O	TTL	GPIO port M bit 0.
PM1	77	-	I/O	TTL	GPIO port M bit 1.
PM2	76	-	I/O	TTL	GPIO port M bit 2.
PM3	75	-	I/O	TTL	GPIO port M bit 3.
PM4	74	-	I/O	TTL	GPIO port M bit 4.
PM5	73	-	I/O	TTL	GPIO port M bit 5.
PM6	72	-	I/O	TTL	GPIO port M bit 6.
PM7	71	-	I/O	TTL	GPIO port M bit 7.
PN0	107	-	I/O	TTL	GPIO port N bit 0.
PN1	108	-	I/O	TTL	GPIO port N bit 1.
PN2	109	-	I/O	TTL	GPIO port N bit 2.
PN3	110	-	I/O	TTL	GPIO port N bit 3.
PN4	111	-	I/O	TTL	GPIO port N bit 4.
PN5	112	-	I/O	TTL	GPIO port N bit 5.
PP0	118	-	I/O	TTL	GPIO port P bit 0.
PP1	119	-	I/O	TTL	GPIO port P bit 1.
PP2	103	-	I/O	TTL	GPIO port P bit 2.
PP3	104	-	I/O	TTL	GPIO port P bit 3.
PP4	105	-	I/O	TTL	GPIO port P bit 4.
PP5	106	-	I/O	TTL	GPIO port P bit 5.
PQ0	5	-	I/O	TTL	GPIO port Q bit 0.
PQ1	6	-	I/O	TTL	GPIO port Q bit 1.
PQ2	11	-	I/O	TTL	GPIO port Q bit 2.
PQ3	27	-	I/O	TTL	GPIO port Q bit 3.
PQ4	102	-	I/O	TTL	GPIO port Q bit 4.
RBIAS	59	fixed	O	Analog	4.87-kΩ resistor (1% precision) for Ethernet PHY.
$\overline{\text{RST}}$	70	fixed	I	TTL	System reset input.
RTCCLK	24 60 104	PC5 (7) PK7 (5) PP3 (7)	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
SSI0Clk	35	PA2 (15)	I/O	TTL	SSI module 0 clock
SSI0Fss	36	PA3 (15)	I/O	TTL	SSI module 0 frame signal
SSI0XDAT0	37	PA4 (15)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 0 (SSI0TX in Legacy SSI Mode).
SSI0XDAT1	38	PA5 (15)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 1 (SSI0RX in Legacy SSI Mode).
SSI0XDAT2	40	PA6 (13)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 2.
SSI0XDAT3	41	PA7 (13)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 3.
SSI1Clk	120	PB5 (15)	I/O	TTL	SSI module 1 clock.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
SSI1Fss	121	PB4 (15)	I/O	TTL	SSI module 1 frame signal.
SSI1XDAT0	123	PE4 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 0 (SSI1TX in Legacy SSI Mode).
SSI1XDAT1	124	PE5 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 1 (SSI1RX in Legacy SSI Mode).
SSI1XDAT2	125	PD4 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 2.
SSI1XDAT3	126	PD5 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 3.
SSI2Clk	4	PD3 (15)	I/O	TTL	SSI module 2 clock.
SSI2Fss	3	PD2 (15)	I/O	TTL	SSI module 2 frame signal.
SSI2XDAT0	2	PD1 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 0 (SSI2TX in Legacy SSI Mode).
SSI2XDAT1	1	PD0 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 1 (SSI2RX in Legacy SSI Mode).
SSI2XDAT2	128	PD7 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 2.
SSI2XDAT3	127	PD6 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 3.
SSI3Clk	5 45	PQ0 (14) PF3 (14)	I/O	TTL	SSI module 3 clock.
SSI3Fss	6 44	PQ1 (14) PF2 (14)	I/O	TTL	SSI module 3 frame signal.
SSI3XDAT0	11 43	PQ2 (14) PF1 (14)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
SSI3XDAT1	27 42	PQ3 (14) PF0 (14)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
SSI3XDAT2	46 118	PF4 (14) PP0 (15)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
SSI3XDAT3	119	PP1 (15)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 3.
SWCLK	100	PC0 (1)	I	TTL	JTAG/SWD CLK.
SWDIO	99	PC1 (1)	I/O	TTL	JTAG TMS and SWDIO.
SWO	97	PC3 (1)	O	TTL	JTAG TDO and SWO.
T0CCP0	1 33 85	PD0 (3) PA0 (3) PL4 (3)	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
T0CCP1	2 34 86	PD1 (3) PA1 (3) PL5 (3)	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
T1CCP0	3 35 94	PD2 (3) PA2 (3) PL6 (3)	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
T1CCP1	4 36 93	PD3 (3) PA3 (3) PL7 (3)	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
T2CCP0	37 78	PA4 (3) PM0 (3)	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
T2CCP1	38 77	PA5 (3) PM1 (3)	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
T3CCP0	40 76 125	PA6 (3) PM2 (3) PD4 (3)	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
T3CCP1	41 75 126	PA7 (3) PM3 (3) PD5 (3)	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
T4CCP0	74 95 127	PM4 (3) PB0 (3) PD6 (3)	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
T4CCP1	73 96 128	PM5 (3) PB1 (3) PD7 (3)	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
T5CCP0	72 91	PM6 (3) PB2 (3)	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
T5CCP1	71 92	PM7 (3) PB3 (3)	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.
TCK	100	PC0 (1)	I	TTL	JTAG/SWD CLK.
TDI	98	PC2 (1)	I	TTL	JTAG TDI.
TDO	97	PC3 (1)	O	TTL	JTAG TDO and SWO.
TMPR0	71	PM7	I/O	TTL	Tamper signal 0.
TMPR1	72	PM6	I/O	TTL	Tamper signal 1.
TMPR2	73	PM5	I/O	TTL	Tamper signal 2.
TMPR3	74	PM4	I/O	TTL	Tamper signal 3.
TMS	99	PC1 (1)	I	TTL	JTAG TMS and SWDIO.
TRCLK	45	PF3 (15)	O	TTL	Trace clock.
TRD0	44	PF2 (15)	O	TTL	Trace data 0.
TRD1	43	PF1 (15)	O	TTL	Trace data 1.
TRD2	42	PF0 (15)	O	TTL	Trace data 2.
TRD3	46	PF4 (15)	O	TTL	Trace data 3.
U0CTS	30 74 121	PH1 (1) PM4 (1) PB4 (1)	I	TTL	UART module 0 Clear To Send modem flow control input signal.
U0DCD	31 73 104	PH2 (1) PM5 (1) PP3 (2)	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
U0DSR	32 72 105	PH3 (1) PM6 (1) PP4 (2)	I	TTL	UART module 0 Data Set Ready modem output control line.
U0DTR	103	PP2 (1)	O	TTL	UART module 0 Data Terminal Ready modem status input signal.
U0RI	60 71	PK7 (1) PM7 (1)	I	TTL	UART module 0 Ring Indicator modem status input signal.
U0RTS	29 120	PH0 (1) PB5 (1)	O	TTL	UART module 0 Request to Send modem flow control output signal.
U0Rx	33	PA0 (1)	I	TTL	UART module 0 receive.
U0Tx	34	PA1 (1)	O	TTL	UART module 0 transmit.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
U1CTS	104 108	PP3 (1) PN1 (1)	I	TTL	UART module 1 Clear To Send modem flow control input signal.
U1DCD	13 109	PE2 (1) PN2 (1)	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
U1DSR	14 110	PE1 (1) PN3 (1)	I	TTL	UART module 1 Data Set Ready modem output control line.
U1DTR	12 111	PE3 (1) PN4 (1)	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
U1RI	112 123	PN5 (1) PE4 (1)	I	TTL	UART module 1 Ring Indicator modem status input signal.
U1RTS	15 107	PE0 (1) PN0 (1)	O	TTL	UART module 1 Request to Send modem flow control output line.
U1Rx	95 102	PB0 (1) PQ4 (1)	I	TTL	UART module 1 receive.
U1Tx	96	PB1 (1)	O	TTL	UART module 1 transmit.
U2CTS	110 128	PN3 (2) PD7 (1)	I	TTL	UART module 2 Clear To Send modem flow control input signal.
U2RTS	109 127	PN2 (2) PD6 (1)	O	TTL	UART module 2 Request to Send modem flow control output line.
U2Rx	40 125	PA6 (1) PD4 (1)	I	TTL	UART module 2 receive.
U2Tx	41 126	PA7 (1) PD5 (1)	O	TTL	UART module 2 transmit.
U3CTS	106 112	PP5 (1) PN5 (2)	I	TTL	UART module 3 Clear To Send modem flow control input signal.
U3RTS	105 111	PP4 (1) PN4 (2)	O	TTL	UART module 3 Request to Send modem flow control output line.
U3Rx	37 116	PA4 (1) PJ0 (1)	I	TTL	UART module 3 receive.
U3Tx	38 117	PA5 (1) PJ1 (1)	O	TTL	UART module 3 transmit.
U4CTS	21	PK3 (1)	I	TTL	UART module 4 Clear To Send modem flow control input signal.
U4RTS	20	PK2 (1)	O	TTL	UART module 4 Request to Send modem flow control output line.
U4Rx	18 35	PK0 (1) PA2 (1)	I	TTL	UART module 4 receive.
U4Tx	19 36	PK1 (1) PA3 (1)	O	TTL	UART module 4 transmit.
U5Rx	23	PC6 (1)	I	TTL	UART module 5 receive.
U5Tx	22	PC7 (1)	O	TTL	UART module 5 transmit.
U6Rx	118	PP0 (1)	I	TTL	UART module 6 receive.
U6Tx	119	PP1 (1)	O	TTL	UART module 6 transmit.
U7Rx	25	PC4 (1)	I	TTL	UART module 7 receive.
U7Tx	24	PC5 (1)	O	TTL	UART module 7 transmit.
USB0CLK	92	PB3 (14)	O	TTL	60-MHz clock to the external PHY.
USB0D0	81	PL0 (14)	I/O	TTL	USB data 0.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
USB0D1	82	PL1 (14)	I/O	TTL	USB data 1.
USB0D2	83	PL2 (14)	I/O	TTL	USB data 2.
USB0D3	84	PL3 (14)	I/O	TTL	USB data 3.
USB0D4	85	PL4 (14)	I/O	TTL	USB data 4.
USB0D5	86	PL5 (14)	I/O	TTL	USB data 5.
USB0D6	106	PP5 (14)	I/O	TTL	USB data 6.
USB0D7	105	PP4 (14)	I/O	TTL	USB data 7.
USB0DIR	104	PP3 (14)	O	TTL	Indicates that the external PHY is able to accept data from the USB controller.
USB0DM	93	PL7	I/O	Analog	Bidirectional differential data pin (D- per USB specification) for USB0.
USB0DP	94	PL6	I/O	Analog	Bidirectional differential data pin (D+ per USB specification) for USB0.
USB0EPEN	40 41 127	PA6 (5) PA7 (11) PD6 (5)	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
USB0ID	95	PB0	I	Analog	This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).
USB0NXT	103	PP2 (14)	O	TTL	Asserted by the external PHY to throttle all data types.
USB0PFLT	41 128	PA7 (5) PD7 (5)	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.
USB0STP	91	PB2 (14)	O	TTL	Asserted by the USB controller to signal the end of a USB transmit packet or register write operation.
USB0VBUS	96	PB1	I/O	Analog	This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.
VBAT	68	fixed	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
VDD	7 16 26 28 39 47 51 52 69 79 90 101 113 122	fixed	-	Power	Positive supply for I/O and some logic.

Table 26-3. Signals by Signal Name *(continued)*

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
VDDA	8	fixed	-	Power	The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in , regardless of system implementation.
VDDC	87 115	fixed	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 27-15 on page 1834 .
VREFA+	9	fixed	-	Analog	A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with GNDA. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in Table 27-44 on page 1861.
$\overline{\text{WAKE}}$	64	fixed	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
XOSC0	66	fixed	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a crystal or a 32.768-kHz oscillator for the Hibernation module RTC.
XOSC1	67	fixed	O	Analog	Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.

26.3 Signals by Function, Except for GPIO

Table 26-4. Signals by Function, Except for GPIO

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
ADC	AIN0	12	I	Analog	Analog-to-digital converter input 0.
	AIN1	13	I	Analog	Analog-to-digital converter input 1.
	AIN2	14	I	Analog	Analog-to-digital converter input 2.
	AIN3	15	I	Analog	Analog-to-digital converter input 3.
	AIN4	128	I	Analog	Analog-to-digital converter input 4.
	AIN5	127	I	Analog	Analog-to-digital converter input 5.
	AIN6	126	I	Analog	Analog-to-digital converter input 6.
	AIN7	125	I	Analog	Analog-to-digital converter input 7.
	AIN8	124	I	Analog	Analog-to-digital converter input 8.
	AIN9	123	I	Analog	Analog-to-digital converter input 9.
	AIN10	121	I	Analog	Analog-to-digital converter input 10.
	AIN11	120	I	Analog	Analog-to-digital converter input 11.
	AIN12	4	I	Analog	Analog-to-digital converter input 12.
	AIN13	3	I	Analog	Analog-to-digital converter input 13.
	AIN14	2	I	Analog	Analog-to-digital converter input 14.
	AIN15	1	I	Analog	Analog-to-digital converter input 15.
	AIN16	18	I	Analog	Analog-to-digital converter input 16.
	AIN17	19	I	Analog	Analog-to-digital converter input 17.
	AIN18	20	I	Analog	Analog-to-digital converter input 18.
	AIN19	21	I	Analog	Analog-to-digital converter input 19.
	VREFA+	9	-	Analog	A reference voltage used to specify the voltage at which the ADC converts to a maximum value. This pin is used in conjunction with GNDA. The voltage that is applied to VREFA+ is the voltage with which an AINn signal is converted to 4095. The VREFA+ voltage is limited to the range specified in Table 27-44 on page 1861.
Analog Comparators	C0+	23	I	Analog	Analog comparator 0 positive input.
	C0-	22	I	Analog	Analog comparator 0 negative input.
	C0o	1 83	O	TTL	Analog comparator 0 output.
	C1+	24	I	Analog	Analog comparator 1 positive input.
	C1-	25	I	Analog	Analog comparator 1 negative input.
	C1o	2 84	O	TTL	Analog comparator 1 output.
	C2+	118	I	Analog	Analog comparator 2 positive input.
	C2-	119	I	Analog	Analog comparator 2 negative input.
	C2o	3	O	TTL	Analog comparator 2 output.
Controller Area Network	CAN0Rx	33	I	TTL	CAN module 0 receive.
	CAN0Tx	34	O	TTL	CAN module 0 transmit.
	CAN1Rx	95	I	TTL	CAN module 1 receive.
	CAN1Tx	96	O	TTL	CAN module 1 transmit.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
Core	TRCLK	45	O	TTL	Trace clock.
	TRD0	44	O	TTL	Trace data 0.
	TRD1	43	O	TTL	Trace data 1.
	TRD2	42	O	TTL	Trace data 2.
	TRD3	46	O	TTL	Trace data 3.
Ethernet	EN0LED0	42 63	O	TTL	Ethernet 0 LED 0.
	EN0LED1	46 61	O	TTL	Ethernet 0 LED 1.
	EN0LED2	43 62	O	TTL	Ethernet 0 LED 2.
	EN0PPS	49 116	O	TTL	Ethernet 0 Pulse-Per-Second (PPS) Output.
	EN0RXIN	53	I/O	TTL	Ethernet PHY negative receive differential input.
	EN0RXIP	54	I/O	TTL	Ethernet PHY positive receive differential input.
	EN0TXON	56	I/O	TTL	Ethernet PHY negative transmit differential output.
	EN0TXOP	57	I/O	TTL	Ethernet PHY positive transmit differential output.
	RBIAS	59	O	Analog	4.87-kΩ resistor (1% precision) for Ethernet PHY.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
External Peripheral Interface	EPI0S0	18 29	I/O	TTL	EPI module 0 signal 0.
	EPI0S1	19 30	I/O	TTL	EPI module 0 signal 1.
	EPI0S2	20 31	I/O	TTL	EPI module 0 signal 2.
	EPI0S3	21 32	I/O	TTL	EPI module 0 signal 3.
	EPI0S4	22	I/O	TTL	EPI module 0 signal 4.
	EPI0S5	23	I/O	TTL	EPI module 0 signal 5.
	EPI0S6	24	I/O	TTL	EPI module 0 signal 6.
	EPI0S7	25	I/O	TTL	EPI module 0 signal 7.
	EPI0S8	40	I/O	TTL	EPI module 0 signal 8.
	EPI0S9	41	I/O	TTL	EPI module 0 signal 9.
	EPI0S10	50	I/O	TTL	EPI module 0 signal 10.
	EPI0S11	49	I/O	TTL	EPI module 0 signal 11.
	EPI0S12	75	I/O	TTL	EPI module 0 signal 12.
	EPI0S13	76	I/O	TTL	EPI module 0 signal 13.
	EPI0S14	77	I/O	TTL	EPI module 0 signal 14.
	EPI0S15	78	I/O	TTL	EPI module 0 signal 15.
	EPI0S16	81	I/O	TTL	EPI module 0 signal 16.
	EPI0S17	82	I/O	TTL	EPI module 0 signal 17.
	EPI0S18	83	I/O	TTL	EPI module 0 signal 18.
	EPI0S19	84	I/O	TTL	EPI module 0 signal 19.
	EPI0S20	5	I/O	TTL	EPI module 0 signal 20.
	EPI0S21	6	I/O	TTL	EPI module 0 signal 21.
	EPI0S22	11	I/O	TTL	EPI module 0 signal 22.
	EPI0S23	27	I/O	TTL	EPI module 0 signal 23.
	EPI0S24	60	I/O	TTL	EPI module 0 signal 24.
	EPI0S25	61	I/O	TTL	EPI module 0 signal 25.
	EPI0S26	85	I/O	TTL	EPI module 0 signal 26.
	EPI0S27	91	I/O	TTL	EPI module 0 signal 27.
	EPI0S28	92	I/O	TTL	EPI module 0 signal 28.
	EPI0S29	103 109	I/O	TTL	EPI module 0 signal 29.
	EPI0S30	104 110	I/O	TTL	EPI module 0 signal 30.
	EPI0S31	62	I/O	TTL	EPI module 0 signal 31.
	EPI0S32	63	I/O	TTL	EPI module 0 signal 32.
	EPI0S33	86	I/O	TTL	EPI module 0 signal 33.
	EPI0S34	111	I/O	TTL	EPI module 0 signal 34.
	EPI0S35	112	I/O	TTL	EPI module 0 signal 35.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
General-Purpose Timers	T0CCP0	1 33 85	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 0.
	T0CCP1	2 34 86	I/O	TTL	16/32-Bit Timer 0 Capture/Compare/PWM 1.
	T1CCP0	3 35 94	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 0.
	T1CCP1	4 36 93	I/O	TTL	16/32-Bit Timer 1 Capture/Compare/PWM 1.
	T2CCP0	37 78	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 0.
	T2CCP1	38 77	I/O	TTL	16/32-Bit Timer 2 Capture/Compare/PWM 1.
	T3CCP0	40 76 125	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 0.
	T3CCP1	41 75 126	I/O	TTL	16/32-Bit Timer 3 Capture/Compare/PWM 1.
	T4CCP0	74 95 127	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 0.
	T4CCP1	73 96 128	I/O	TTL	16/32-Bit Timer 4 Capture/Compare/PWM 1.
	T5CCP0	72 91	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 0.
	T5CCP1	71 92	I/O	TTL	16/32-Bit Timer 5 Capture/Compare/PWM 1.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
Hibernate	HIB	65	O	TTL	An output that indicates the processor is in Hibernate mode.
	RTCCLK	24 60 104	O	TTL	Buffered version of the Hibernation module's 32.768-kHz clock. This signal is not output when the part is in Hibernate mode and before being configured after power-on reset.
	TMPR0	71	I/O	TTL	Tamper signal 0.
	TMPR1	72	I/O	TTL	Tamper signal 1.
	TMPR2	73	I/O	TTL	Tamper signal 2.
	TMPR3	74	I/O	TTL	Tamper signal 3.
	VBAT	68	-	Power	Power source for the Hibernation module. It is normally connected to the positive terminal of a battery and serves as the battery backup/Hibernation module power-source supply.
	WAKE	64	I	TTL	An external input that brings the processor out of Hibernate mode when asserted.
	XOSC0	66	I	Analog	Hibernation module oscillator crystal input or an external clock reference input. Note that this is either a crystal or a 32.768-kHz oscillator for the Hibernation module RTC.
	XOSC1	67	O	Analog	Hibernation module oscillator crystal output. Leave unconnected when using a single-ended clock source.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
I2C	I2C0SCL	91	I/O	OD	I^2C module 0 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C0SDA	92	I/O	OD	I^2C module 0 data.
	I2C1SCL	49	I/O	OD	I^2C module 1 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C1SDA	50	I/O	OD	I^2C module 1 data.
	I2C2SCL	82 106 112	I/O	OD	I^2C module 2 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C2SDA	81 111	I/O	OD	I^2C module 2 data.
	I2C3SCL	63	I/O	OD	I^2C module 3 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C3SDA	62	I/O	OD	I^2C module 3 data.
	I2C4SCL	61	I/O	OD	I^2C module 4 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C4SDA	60	I/O	OD	I^2C module 4 data.
	I2C5SCL	95 121	I/O	OD	I^2C module 5 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C5SDA	96 120	I/O	OD	I^2C module 5 data.
	I2C6SCL	40	I/O	OD	I^2C module 6 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C6SDA	41	I/O	OD	I^2C module 6 data.
	I2C7SCL	1 37	I/O	OD	I^2C module 7 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C7SDA	2 38	I/O	OD	I^2C module 7 data.
	I2C8SCL	3 35	I/O	OD	I^2C module 8 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C8SDA	4 36	I/O	OD	I^2C module 8 data.
	I2C9SCL	33	I/O	OD	I^2C module 9 clock. Note that this signal has an active pull-up. The corresponding port pin should not be configured as open drain.
	I2C9SDA	34	I/O	OD	I^2C module 9 data.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
JTAG/SWD/SWO	SWCLK	100	I	TTL	JTAG/SWD CLK.
	SWDIO	99	I/O	TTL	JTAG TMS and SWDIO.
	SWO	97	O	TTL	JTAG TDO and SWO.
	TCK	100	I	TTL	JTAG/SWD CLK.
	TDI	98	I	TTL	JTAG TDI.
	TDO	97	O	TTL	JTAG TDO and SWO.
	TMS	99	I	TTL	JTAG TMS and SWDIO.
PWM	M0FAULT0	46	I	TTL	Motion Control Module 0 PWM Fault 0.
	M0FAULT1	61	I	TTL	Motion Control Module 0 PWM Fault 1.
	M0FAULT2	60	I	TTL	Motion Control Module 0 PWM Fault 2.
	M0FAULT3	81	I	TTL	Motion Control Module 0 PWM Fault 3.
	M0PWM0	42	O	TTL	Motion Control Module 0 PWM 0. This signal is controlled by Module 0 PWM Generator 0.
	M0PWM1	43	O	TTL	Motion Control Module 0 PWM 1. This signal is controlled by Module 0 PWM Generator 0.
	M0PWM2	44	O	TTL	Motion Control Module 0 PWM 2. This signal is controlled by Module 0 PWM Generator 1.
	M0PWM3	45	O	TTL	Motion Control Module 0 PWM 3. This signal is controlled by Module 0 PWM Generator 1.
	M0PWM4	49	O	TTL	Motion Control Module 0 PWM 4. This signal is controlled by Module 0 PWM Generator 2.
	M0PWM5	50	O	TTL	Motion Control Module 0 PWM 5. This signal is controlled by Module 0 PWM Generator 2.
	M0PWM6	63	O	TTL	Motion Control Module 0 PWM 6. This signal is controlled by Module 0 PWM Generator 3.
	M0PWM7	62	O	TTL	Motion Control Module 0 PWM 7. This signal is controlled by Module 0 PWM Generator 3.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
Power	GND	17 48 55 58 80 114	-	Power	Ground reference for logic and I/O pins.
	GNDA	10	-	Power	The ground reference for the analog circuits (ADC, Analog Comparators, etc.). These are separated from GND to minimize the electrical noise contained on VDD from affecting the analog functions.
	VDD	7 16 26 28 39 47 51 52 69 79 90 101 113 122	-	Power	Positive supply for I/O and some logic.
	VDDA	8	-	Power	The positive supply for the analog circuits (ADC, Analog Comparators, etc.). These are separated from VDD to minimize the electrical noise contained on VDD from affecting the analog functions. VDDA pins must be supplied with a voltage that meets the specification in , regardless of system implementation.
	VDDC	87 115	-	Power	Positive supply for most of the logic function, including the processor core and most peripherals. The voltage on this pin is 1.2 V and is supplied by the on-chip LDO. The VDDC pins should only be connected to each other and an external capacitor as specified in Table 27-15 on page 1834 .
QEI	IDX0	84	I	TTL	QEI module 0 index.
	PhA0	82	I	TTL	QEI module 0 phase A.
	PhB0	83	I	TTL	QEI module 0 phase B.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
SSI	SSI0Clk	35	I/O	TTL	SSI module 0 clock
	SSI0Fss	36	I/O	TTL	SSI module 0 frame signal
	SSI0XDAT0	37	I/O	TTL	SSI Module 0 Bi-directional Data Pin 0 (SSI0TX in Legacy SSI Mode).
	SSI0XDAT1	38	I/O	TTL	SSI Module 0 Bi-directional Data Pin 1 (SSI0RX in Legacy SSI Mode).
	SSI0XDAT2	40	I/O	TTL	SSI Module 0 Bi-directional Data Pin 2.
	SSI0XDAT3	41	I/O	TTL	SSI Module 0 Bi-directional Data Pin 3.
	SSI1Clk	120	I/O	TTL	SSI module 1 clock.
	SSI1Fss	121	I/O	TTL	SSI module 1 frame signal.
	SSI1XDAT0	123	I/O	TTL	SSI Module 1 Bi-directional Data Pin 0 (SSI1TX in Legacy SSI Mode).
	SSI1XDAT1	124	I/O	TTL	SSI Module 1 Bi-directional Data Pin 1 (SSI1RX in Legacy SSI Mode).
	SSI1XDAT2	125	I/O	TTL	SSI Module 1 Bi-directional Data Pin 2.
	SSI1XDAT3	126	I/O	TTL	SSI Module 1 Bi-directional Data Pin 3.
	SSI2Clk	4	I/O	TTL	SSI module 2 clock.
	SSI2Fss	3	I/O	TTL	SSI module 2 frame signal.
	SSI2XDAT0	2	I/O	TTL	SSI Module 2 Bi-directional Data Pin 0 (SSI2TX in Legacy SSI Mode).
	SSI2XDAT1	1	I/O	TTL	SSI Module 2 Bi-directional Data Pin 1 (SSI2RX in Legacy SSI Mode).
	SSI2XDAT2	128	I/O	TTL	SSI Module 2 Bi-directional Data Pin 2.
	SSI2XDAT3	127	I/O	TTL	SSI Module 2 Bi-directional Data Pin 3.
	SSI3Clk	5 45	I/O	TTL	SSI module 3 clock.
	SSI3Fss	6 44	I/O	TTL	SSI module 3 frame signal.
	SSI3XDAT0	11 43	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
	SSI3XDAT1	27 42	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
	SSI3XDAT2	46 118	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
	SSI3XDAT3	119	I/O	TTL	SSI Module 3 Bi-directional Data Pin 3.
System Control & Clocks	DIVSCLK	102	O	TTL	An optionally divided reference clock output based on a selected clock source. Note that this signal is not synchronized to the System Clock.
	NMI	128	I	TTL	Non-maskable interrupt.
	OSC0	88	I	Analog	Main oscillator crystal input or an external clock reference input.
	OSC1	89	O	Analog	Main oscillator crystal output. Leave unconnected when using a single-ended clock source.
	$\overline{\text{RST}}$	70	I	TTL	System reset input.

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
UART	U0CTS	30 74 121	I	TTL	UART module 0 Clear To Send modem flow control input signal.
	U0DCD	31 73 104	I	TTL	UART module 0 Data Carrier Detect modem status input signal.
	U0DSR	32 72 105	I	TTL	UART module 0 Data Set Ready modem output control line.
	U0DTR	103	O	TTL	UART module 0 Data Terminal Ready modem status input signal.
	U0RI	60 71	I	TTL	UART module 0 Ring Indicator modem status input signal.
	U0RTS	29 120	O	TTL	UART module 0 Request to Send modem flow control output signal.
	U0Rx	33	I	TTL	UART module 0 receive.
	U0Tx	34	O	TTL	UART module 0 transmit.
	U1CTS	104 108	I	TTL	UART module 1 Clear To Send modem flow control input signal.
	U1DCD	13 109	I	TTL	UART module 1 Data Carrier Detect modem status input signal.
	U1DSR	14 110	I	TTL	UART module 1 Data Set Ready modem output control line.
	U1DTR	12 111	O	TTL	UART module 1 Data Terminal Ready modem status input signal.
	U1RI	112 123	I	TTL	UART module 1 Ring Indicator modem status input signal.
	U1RTS	15 107	O	TTL	UART module 1 Request to Send modem flow control output line.
	U1Rx	95 102	I	TTL	UART module 1 receive.
	U1Tx	96	O	TTL	UART module 1 transmit.
	U2CTS	110 128	I	TTL	UART module 2 Clear To Send modem flow control input signal.
	U2RTS	109 127	O	TTL	UART module 2 Request to Send modem flow control output line.
	U2Rx	40 125	I	TTL	UART module 2 receive.
	U2Tx	41 126	O	TTL	UART module 2 transmit.
	U3CTS	106 112	I	TTL	UART module 3 Clear To Send modem flow control input signal.
	U3RTS	105 111	O	TTL	UART module 3 Request to Send modem flow control output line.
	U3Rx	37 116	I	TTL	UART module 3 receive.
	U3Tx	38 117	O	TTL	UART module 3 transmit.
	U4CTS	21	I	TTL	

Table 26-4. Signals by Function, Except for GPIO *(continued)*

Function	Pin Name	Pin Number	Pin Type	Buffer Type	Description
					UART module 4 Clear To Send modem flow control input signal.
	U4RTS	20	O	TTL	UART module 4 Request to Send modem flow control output line.
	U4Rx	18 35	I	TTL	UART module 4 receive.
	U4Tx	19 36	O	TTL	UART module 4 transmit.
	U5Rx	23	I	TTL	UART module 5 receive.
	U5Tx	22	O	TTL	UART module 5 transmit.
	U6Rx	118	I	TTL	UART module 6 receive.
	U6Tx	119	O	TTL	UART module 6 transmit.
	U7Rx	25	I	TTL	UART module 7 receive.
	U7Tx	24	O	TTL	UART module 7 transmit.
USB	USB0CLK	92	O	TTL	60-MHz clock to the external PHY.
	USB0D0	81	I/O	TTL	USB data 0.
	USB0D1	82	I/O	TTL	USB data 1.
	USB0D2	83	I/O	TTL	USB data 2.
	USB0D3	84	I/O	TTL	USB data 3.
	USB0D4	85	I/O	TTL	USB data 4.
	USB0D5	86	I/O	TTL	USB data 5.
	USB0D6	106	I/O	TTL	USB data 6.
	USB0D7	105	I/O	TTL	USB data 7.
	USB0DIR	104	O	TTL	Indicates that the external PHY is able to accept data from the USB controller.
	USB0DM	93	I/O	Analog	Bidirectional differential data pin (D- per USB specification) for USB0.
	USB0DP	94	I/O	Analog	Bidirectional differential data pin (D+ per USB specification) for USB0.
	USB0EPEN	40 41 127	O	TTL	Optionally used in Host mode to control an external power source to supply power to the USB bus.
	USB0ID	95	I	Analog	This signal senses the state of the USB ID signal. The USB PHY enables an integrated pull-up, and an external element (USB connector) indicates the initial state of the USB controller (pulled down is the A side of the cable and pulled up is the B side).
	USB0NXT	103	O	TTL	Asserted by the external PHY to throttle all data types.
	USB0PFLT	41 128	I	TTL	Optionally used in Host mode by an external power source to indicate an error state by that power source.
	USB0STP	91	O	TTL	Asserted by the USB controller to signal the end of a USB transmit packet or register write operation.
	USB0VBUS	96	I/O	Analog	This signal is used during the session request protocol. This signal allows the USB PHY to both sense the voltage level of VBUS, and pull up VBUS momentarily during VBUS pulsing.

26.4 GPIO Pins and Alternate Functions

Table 26-5. GPIO Pins and Alternate Functions

IO	Pin	Analog or Special Function[a]	Digital Function (GPIOPCTL PMCx Bit Field Encoding)[b]											
			1	2	3	4	5	6	7	8	11	13	14	15
PA0	33	-	U0Rx	I2C9SCL	T0CCP0	-	-	-	CAN0Rx	-	-	-	-	-
PA1	34	-	U0Tx	I2C9SDA	T0CCP1	-	-	-	CAN0Tx	-	-	-	-	-
PA2	35	-	U4Rx	I2C8SCL	T1CCP0	-	-	-	-	-	-	-	-	SSI0Clk
PA3	36	-	U4Tx	I2C8SDA	T1CCP1	-	-	-	-	-	-	-	-	SSI0Fss
PA4	37	-	U3Rx	I2C7SCL	T2CCP0	-	-	-	-	-	-	-	-	SSI0XDAT0
PA5	38	-	U3Tx	I2C7SDA	T2CCP1	-	-	-	-	-	-	-	-	SSI0XDAT1
PA6	40	-	U2Rx	I2C6SCL	T3CCP0	-	USB0EPEN	-	-	-	-	SSI0XDAT2	-	EPI0S8
PA7	41	-	U2Tx	I2C6SDA	T3CCP1	-	USB0PFLT	-	-	-	USB0EPEN	SSI0XDAT3	-	EPI0S9
PB0	95	USB0ID	U1Rx	I2C5SCL	T4CCP0	-	-	-	CAN1Rx	-	-	-	-	-
PB1	96	USB0VBUS	U1Tx	I2C5SDA	T4CCP1	-	-	-	CAN1Tx	-	-	-	-	-
PB2	91	-	-	I2C0SCL	T5CCP0	-	-	-	-	-	-	-	USB0STP	EPI0S27
PB3	92	-	-	I2C0SDA	T5CCP1	-	-	-	-	-	-	-	USB0CLK	EPI0S28
PB4	121	AIN10	U0CTS	I2C5SCL	-	-	-	-	-	-	-	-	-	SSI1Fss
PB5	120	AIN11	U0RTS	I2C5SDA	-	-	-	-	-	-	-	-	-	SSI1Clk
PC0	100	-	TCK SWCLK	-	-	-	-	-	-	-	-	-	-	-
PC1	99	-	TMS SWDIO	-	-	-	-	-	-	-	-	-	-	-
PC2	98	-	TDI	-	-	-	-	-	-	-	-	-	-	-
PC3	97	-	TDO SWO	-	-	-	-	-	-	-	-	-	-	-
PC4	25	C1-	U7Rx	-	-	-	-	-	-	-	-	-	-	EPI0S7
PC5	24	C1+	U7Tx	-	-	-	-	-	RTCCLK	-	-	-	-	EPI0S6
PC6	23	C0+	U5Rx	-	-	-	-	-	-	-	-	-	-	EPI0S5
PC7	22	C0-	U5Tx	-	-	-	-	-	-	-	-	-	-	EPI0S4
PD0	1	AIN15	-	I2C7SCL	T0CCP0	-	C0o	-	-	-	-	-	-	SSI2XDAT1
PD1	2	AIN14	-	I2C7SDA	T0CCP1	-	C1o	-	-	-	-	-	-	SSI2XDAT0
PD2	3	AIN13	-	I2C8SCL	T1CCP0	-	C2o	-	-	-	-	-	-	SSI2Fss
PD3	4	AIN12	-	I2C8SDA	T1CCP1	-	-	-	-	-	-	-	-	SSI2Clk
PD4	125	AIN7	U2Rx	-	T3CCP0	-	-	-	-	-	-	-	-	SSI1XDAT2
PD5	126	AIN6	U2Tx	-	T3CCP1	-	-	-	-	-	-	-	-	SSI1XDAT3
PD6	127	AIN5	U2RTS	-	T4CCP0	-	USB0EPEN	-	-	-	-	-	-	SSI2XDAT3
PD7	128	AIN4	U2CTS	-	T4CCP1	-	USB0PFLT	-	-	NMI	-	-	-	SSI2XDAT2
PE0	15	AIN3	U1RTS	-	-	-	-	-	-	-	-	-	-	-
PE1	14	AIN2	U1DSR	-	-	-	-	-	-	-	-	-	-	-
PE2	13	AIN1	U1DCD	-	-	-	-	-	-	-	-	-	-	-
PE3	12	AIN0	U1DTR	-	-	-	-	-	-	-	-	-	-	-
PE4	123	AIN9	U1RI	-	-	-	-	-	-	-	-	-	-	SSI1XDAT0

Table 26-5. GPIO Pins and Alternate Functions *(continued)*

IO	Pin	Analog or Special Function[a]	Digital Function (GPIOPCTL PMCx Bit Field Encoding)[b]											
			1	2	3	4	5	6	7	8	11	13	14	15
PE5	124	AIN8	-	-	-	-	-	-	-	-	-	-	-	SSI1XDAT1
PF0	42	-	-	-	-	-	EN0LED0	M0PWM0	-	-	-	-	SSI3XDAT1	TRD2
PF1	43	-	-	-	-	-	EN0LED2	M0PWM1	-	-	-	-	SSI3XDAT0	TRD1
PF2	44	-	-	-	-	-	-	M0PWM2	-	-	-	-	SSI3Fss	TRD0
PF3	45	-	-	-	-	-	-	M0PWM3	-	-	-	-	SSI3Clk	TRCLK
PF4	46	-	-	-	-	-	EN0LED1	M0FAULT0	-	-	-	-	SSI3XDAT2	TRD3
PG0	49	-	-	I2C1SCL	-	-	EN0PPS	M0PWM4	-	-	-	-	-	EPI0S11
PG1	50	-	-	I2C1SDA	-	-	-	M0PWM5	-	-	-	-	-	EPI0S10
PH0	29	-	U0RTS	-	-	-	-	-	-	-	-	-	-	EPI0S0
PH1	30	-	U0CTS	-	-	-	-	-	-	-	-	-	-	EPI0S1
PH2	31	-	U0DCD	-	-	-	-	-	-	-	-	-	-	EPI0S2
PH3	32	-	U0DSR	-	-	-	-	-	-	-	-	-	-	EPI0S3
PJ0	116	-	U3Rx	-	-	-	EN0PPS	-	-	-	-	-	-	-
PJ1	117	-	U3Tx	-	-	-	-	-	-	-	-	-	-	-
PK0	18	AIN16	U4Rx	-	-	-	-	-	-	-	-	-	-	EPI0S0
PK1	19	AIN17	U4Tx	-	-	-	-	-	-	-	-	-	-	EPI0S1
PK2	20	AIN18	U4RTS	-	-	-	-	-	-	-	-	-	-	EPI0S2
PK3	21	AIN19	U4CTS	-	-	-	-	-	-	-	-	-	-	EPI0S3
PK4	63	-	-	I2C3SCL	-	-	EN0LED0	M0PWM6	-	-	-	-	-	EPI0S32
PK5	62	-	-	I2C3SDA	-	-	EN0LED2	M0PWM7	-	-	-	-	-	EPI0S31
PK6	61	-	-	I2C4SCL	-	-	EN0LED1	M0FAULT1	-	-	-	-	-	EPI0S25
PK7	60	-	U0RI	I2C4SDA	-	-	RTCCLK	M0FAULT2	-	-	-	-	-	EPI0S24
PL0	81	-	-	I2C2SDA	-	-	-	M0FAULT3	-	-	-	-	USB0D0	EPI0S16
PL1	82	-	-	I2C2SCL	-	-	-	PhA0	-	-	-	-	USB0D1	EPI0S17
PL2	83	-	-	-	-	-	C0o	PhB0	-	-	-	-	USB0D2	EPI0S18
PL3	84	-	-	-	-	-	C1o	IDX0	-	-	-	-	USB0D3	EPI0S19
PL4	85	-	-	-	T0CCP0	-	-	-	-	-	-	-	USB0D4	EPI0S26
PL5	86	-	-	-	T0CCP1	-	-	-	-	-	-	-	USB0D5	EPI0S33
PL6	94	USB0DP	-	-	T1CCP0	-	-	-	-	-	-	-	-	-
PL7	93	USB0DM	-	-	T1CCP1	-	-	-	-	-	-	-	-	-
PM0	78	-	-	-	T2CCP0	-	-	-	-	-	-	-	-	EPI0S15
PM1	77	-	-	-	T2CCP1	-	-	-	-	-	-	-	-	EPI0S14
PM2	76	-	-	-	T3CCP0	-	-	-	-	-	-	-	-	EPI0S13
PM3	75	-	-	-	T3CCP1	-	-	-	-	-	-	-	-	EPI0S12
PM4	74	TMPR3	U0CTS	-	T4CCP0	-	-	-	-	-	-	-	-	-
PM5	73	TMPR2	U0DCD	-	T4CCP1	-	-	-	-	-	-	-	-	-
PM6	72	TMPR1	U0DSR	-	T5CCP0	-	-	-	-	-	-	-	-	-
PM7	71	TMPR0	U0RI	-	T5CCP1	-	-	-	-	-	-	-	-	-
PN0	107	-	U1RTS	-	-	-	-	-	-	-	-	-	-	-

Table 26-5. GPIO Pins and Alternate Functions *(continued)*

IO	Pin	Analog or Special Function[a]	Digital Function (GPIOPCTL PMCx Bit Field Encoding)[b]											
			1	2	3	4	5	6	7	8	11	13	14	15
PN1	108	-	U1CTS	-	-	-	-	-	-	-	-	-	-	-
PN2	109	-	U1DCD	U2RTS	-	-	-	-	-	-	-	-	-	EPI0S29
PN3	110	-	U1DSR	U2CTS	-	-	-	-	-	-	-	-	-	EPI0S30
PN4	111	-	U1DTR	U3RTS	I2C2SDA	-	-	-	-	-	-	-	-	EPI0S34
PN5	112	-	U1RI	U3CTS	I2C2SCL	-	-	-	-	-	-	-	-	EPI0S35
PP0	118	C2+	U6Rx	-	-	-	-	-	-	-	-	-	-	SSI3XDAT2
PP1	119	C2-	U6Tx	-	-	-	-	-	-	-	-	-	-	SSI3XDAT3
PP2	103	-	U0DTR	-	-	-	-	-	-	-	-	-	USB0NXT	EPI0S29
PP3	104	-	U1CTS	U0DCD	-	-	-	-	RTCCLK	-	-	-	USB0DIR	EPI0S30
PP4	105	-	U3RTS	U0DSR	-	-	-	-	-	-	-	-	USB0D7	-
PP5	106	-	U3CTS	I2C2SCL	-	-	-	-	-	-	-	-	USB0D6	-
PQ0	5	-	-	-	-	-	-	-	-	-	-	-	SSI3Clk	EPI0S20
PQ1	6	-	-	-	-	-	-	-	-	-	-	-	SSI3Fss	EPI0S21
PQ2	11	-	-	-	-	-	-	-	-	-	-	-	SSI3XDAT0	EPI0S22
PQ3	27	-	-	-	-	-	-	-	-	-	-	-	SSI3XDAT1	EPI0S23
PQ4	102	-	U1Rx	-	-	-	-	-	DIVSCLK	-	-	-	-	-

a. The TMPRn signals are digital signals enabled and configured by the Hibernation module. All other signals listed in this column are analog signals.

b. The digital signals that are shaded gray are the power-on default values for the corresponding GPIO pin. Encodings 9, 10, and 12 are not used on this device.

26.5 Possible Pin Assignments for Alternate Functions

Table 26-6. Possible Pin Assignments for Alternate Functions

# of Possible Assignments	Alternate Function	GPIO Function
one	AIN0	PE3
	AIN1	PE2
	AIN10	PB4
	AIN11	PB5
	AIN12	PD3
	AIN13	PD2
	AIN14	PD1
	AIN15	PD0
	AIN16	PK0
	AIN17	PK1
	AIN18	PK2
	AIN19	PK3
	AIN2	PE1
	AIN3	PE0
	AIN4	PD7
	AIN5	PD6
	AIN6	PD5
	AIN7	PD4
	AIN8	PE5
	AIN9	PE4
	C0+	PC6
	C0-	PC7
	C1+	PC5
	C1-	PC4
	C2+	PP0
	C2-	PP1
	C2o	PD2
	CAN0Rx	PA0
	CAN0Tx	PA1
	CAN1Rx	PB0
	CAN1Tx	PB1
	DIVSCLK	PQ4
	EPI0S10	PG1
	EPI0S11	PG0
	EPI0S12	PM3
	EPI0S13	PM2
	EPI0S14	PM1
	EPI0S15	PM0
	EPI0S16	PL0

Table 26-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
	EPI0S17	PL1
	EPI0S18	PL2
	EPI0S19	PL3
	EPI0S20	PQ0
	EPI0S21	PQ1
	EPI0S22	PQ2
	EPI0S23	PQ3
	EPI0S24	PK7
	EPI0S25	PK6
	EPI0S26	PL4
	EPI0S27	PB2
	EPI0S28	PB3
	EPI0S31	PK5
	EPI0S32	PK4
	EPI0S33	PL5
	EPI0S34	PN4
	EPI0S35	PN5
	EPI0S4	PC7
	EPI0S5	PC6
	EPI0S6	PC5
	EPI0S7	PC4
	EPI0S8	PA6
	EPI0S9	PA7
	I2C0SCL	PB2
	I2C0SDA	PB3
	I2C1SCL	PG0
	I2C1SDA	PG1
	I2C3SCL	PK4
	I2C3SDA	PK5
	I2C4SCL	PK6
	I2C4SDA	PK7
	I2C6SCL	PA6
	I2C6SDA	PA7
	I2C9SCL	PA0
	I2C9SDA	PA1
	IDX0	PL3
	M0FAULT0	PF4
	M0FAULT1	PK6
	M0FAULT2	PK7
	M0FAULT3	PL0
	M0PWM0	PF0

Table 26-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
	M0PWM1	PF1
	M0PWM2	PF2
	M0PWM3	PF3
	M0PWM4	PG0
	M0PWM5	PG1
	M0PWM6	PK4
	M0PWM7	PK5
	NMI	PD7
	PhA0	PL1
	PhB0	PL2
	SSI0Clk	PA2
	SSI0Fss	PA3
	SSI0XDAT0	PA4
	SSI0XDAT1	PA5
	SSI0XDAT2	PA6
	SSI0XDAT3	PA7
	SSI1Clk	PB5
	SSI1Fss	PB4
	SSI1XDAT0	PE4
	SSI1XDAT1	PE5
	SSI1XDAT2	PD4
	SSI1XDAT3	PD5
	SSI2Clk	PD3
	SSI2Fss	PD2
	SSI2XDAT0	PD1
	SSI2XDAT1	PD0
	SSI2XDAT2	PD7
	SSI2XDAT3	PD6
	SSI3XDAT3	PP1
	SWCLK	PC0
	SWDIO	PC1
	SWO	PC3
	TCK	PC0
	TDI	PC2
	TDO	PC3
	TMPR0	PM7
	TMPR1	PM6
	TMPR2	PM5
	TMPR3	PM4
	TMS	PC1
	TRCLK	PF3

Table 26-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
	TRD0	PF2
	TRD1	PF1
	TRD2	PF0
	TRD3	PF4
	U0DTR	PP2
	U0Rx	PA0
	U0Tx	PA1
	U1Tx	PB1
	U4CTS	PK3
	U4RTS	PK2
	U5Rx	PC6
	U5Tx	PC7
	U6Rx	PP0
	U6Tx	PP1
	U7Rx	PC4
	U7Tx	PC5
	USB0CLK	PB3
	USB0D0	PL0
	USB0D1	PL1
	USB0D2	PL2
	USB0D3	PL3
	USB0D4	PL4
	USB0D5	PL5
	USB0D6	PP5
	USB0D7	PP4
	USB0DIR	PP3
	USB0DM	PL7
	USB0DP	PL6
	USB0ID	PB0
	USB0NXT	PP2
	USB0STP	PB2
	USB0VBUS	PB1

Table 26-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
two	C0o	PD0 PL2
	C1o	PD1 PL3
	EN0LED0	PF0 PK4
	EN0LED1	PF4 PK6
	EN0LED2	PF1 PK5
	EN0PPS	PG0 PJ0
	EPI0S0	PH0 PK0
	EPI0S1	PH1 PK1
	EPI0S2	PH2 PK2
	EPI0S29	PN2 PP2
	EPI0S3	PH3 PK3
	EPI0S30	PN3 PP3
	I2C2SDA	PL0 PN4
	I2C5SCL	PB0 PB4
	I2C5SDA	PB1 PB5
	I2C7SCL	PA4 PD0
	I2C7SDA	PA5 PD1
	I2C8SCL	PA2 PD2
	I2C8SDA	PA3 PD3
	SSI3Clk	PF3 PQ0
	SSI3Fss	PF2 PQ1
	SSI3XDAT0	PF1 PQ2
	SSI3XDAT1	PF0 PQ3
	SSI3XDAT2	PF4 PP0
	T2CCP0	PA4 PM0
	T2CCP1	PA5 PM1
	T5CCP0	PB2 PM6
	T5CCP1	PB3 PM7
	U0RI	PK7 PM7
	U0RTS	PB5 PH0
	U1CTS	PN1 PP3
	U1DCD	PE2 PN2
	U1DSR	PE1 PN3
	U1DTR	PE3 PN4
	U1RI	PE4 PN5
	U1RTS	PE0 PN0
	U1Rx	PB0 PQ4
	U2CTS	PD7 PN3
	U2RTS	PD6 PN2
	U2Rx	PA6 PD4
	U2Tx	PA7 PD5

Table 26-6. Possible Pin Assignments for Alternate Functions *(continued)*

# of Possible Assignments	Alternate Function	GPIO Function
	U3CTS	PN5 PP5
	U3RTS	PN4 PP4
	U3Rx	PA4 PJ0
	U3Tx	PA5 PJ1
	U4Rx	PA2 PK0
	U4Tx	PA3 PK1
	USB0PFLT	PA7 PD7
three	I2C2SCL	PL1 PN5 PP5
	RTCCLK	PC5 PK7 PP3
	T0CCP0	PA0 PD0 PL4
	T0CCP1	PA1 PD1 PL5
	T1CCP0	PA2 PD2 PL6
	T1CCP1	PA3 PD3 PL7
	T3CCP0	PA6 PD4 PM2
	T3CCP1	PA7 PD5 PM3
	T4CCP0	PB0 PD6 PM4
	T4CCP1	PB1 PD7 PM5
	U0CTS	PB4 PH1 PM4
	U0DCD	PH2 PM5 PP3
	U0DSR	PH3 PM6 PP4
	USB0EPEN	PA6 PA7 PD6

26.6 Connections for Unused Signals

Table 26-7 on page 1816 shows how to handle signals for functions that are not used in a particular system implementation for devices that are in a 128-pin TQFP package. Two options are shown in the table: an acceptable practice and a preferred practice for reduced power consumption and improved EMC characteristics. If a module is not used in a system, and its inputs are grounded, it is important that the clock to the module is never enabled by setting the corresponding bit in the **RCGCx** register.

Table 26-7. Connections for Unused Signals (128-Pin TQFP)

Function	Signal Name	Pin Number	Acceptable Practice	Preferred Practice
ADC	VREFA+	9	VDDA	VDDA
Ethernet	EN0RXIN	53	NC	NC
	EN0RXIP	54	NC	NC
	EN0TXON	56	NC	NC
	EN0TXOP	57	NC	NC
	RBIAS	59	Connect to ground through 4.87K resistor	NC[a]
GPIO	PA1(U0TX)	34	NC	GND[b]
	PA4 (SSI0XDAT0)	37	NC	GND[c]
	All unused GPIOs	-	NC	GND