parentheses is the encoding that must be programmed into the PMCn field in the **GPIO Port Control (GPIOPCTL)** register (page 787) to assign the QSSI signal to the specified GPIO port pin. For more information on configuring GPIOs, see "General-Purpose Input/Outputs (GPIOs)" on page 742. Note that for the QSSI module, when operating in Legacy Mode, SSInXDAT0 functions as SSInTX and SSInXDAT1 functions as SSInRX.

Table 17-1. SSI Signals (128TQFP)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type	Description
SSI0Clk	35	PA2 (15)	I/O	TTL	SSI module 0 clock
SSI0Fss	36	PA3 (15)	I/O	TTL	SSI module 0 frame signal
SSI0XDAT0	37	PA4 (15)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 0 (SSI0TX in Legacy SSI Mode).
SSI0XDAT1	38	PA5 (15)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 1 (SSI0RX in Legacy SSI Mode).
SSI0XDAT2	40	PA6 (13)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 2.
SSI0XDAT3	41	PA7 (13)	I/O	TTL	SSI Module 0 Bi-directional Data Pin 3.
SSI1Clk	120	PB5 (15)	I/O	TTL	SSI module 1 clock.
SSI1Fss	121	PB4 (15)	I/O	TTL	SSI module 1 frame signal.
SSI1XDAT0	123	PE4 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 0 (SSI1TX in Legacy SSI Mode).
SSI1XDAT1	124	PE5 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 1 (SSI1RX in Legacy SSI Mode).
SSI1XDAT2	125	PD4 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 2.
SSI1XDAT3	126	PD5 (15)	I/O	TTL	SSI Module 1 Bi-directional Data Pin 3.
SSI2Clk	4	PD3 (15)	I/O	TTL	SSI module 2 clock.
SSI2Fss	3	PD2 (15)	I/O	TTL	SSI module 2 frame signal.
SSI2XDAT0	2	PD1 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 0 (SSI2TX in Legacy SSI Mode).
SSI2XDAT1	1	PD0 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 1 (SSI2RX in Legacy SSI Mode).
SSI2XDAT2	128	PD7 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 2.
SSI2XDAT3	127	PD6 (15)	I/O	TTL	SSI Module 2 Bi-directional Data Pin 3.
SSI3Clk	5 45	PQ0 (14) PF3 (14)	I/O	TTL	SSI module 3 clock.
SSI3Fss	6 44	PQ1 (14) PF2 (14)	I/O	TTL	SSI module 3 frame signal.
SSI3XDAT0	11 43	PQ2 (14) PF1 (14)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 0 (SSI3TX in Legacy SSI Mode).
SSI3XDAT1	27 42	PQ3 (14) PF0 (14)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 1 (SSI3RX in Legacy SSI Mode).
SSI3XDAT2	46 118	PF4 (14) PP0 (15)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 2.
SSI3XDAT3	119	PP1 (15)	I/O	TTL	SSI Module 3 Bi-directional Data Pin 3.

17.3 Functional Description

The QSSI performs serial-to-parallel conversion on data received from a peripheral device. The CPU accesses data, control, and status information. The transmit and receive paths are buffered