Joseph Colosimo

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Summary

Passionate about architecting and delivering advanced digital solutions that provide meaningful benefit to human beings. Experienced in creating optimal embedded sensor stacks—especially for atypically-constrained systems—by leveraging a multi-disciplinary background designing firmware, digital hardware, and platform specifications.

Overview of Technical Skills

Embedded System Architecture: translation of feature requirements into system design, full-stack modeling, protocol design, custom silicon specification, silicon development-cycle support

Firmware (C, ASM; ARM (Cortex-A & M), Picoblaze, AVR…): core system infrastructure, sensor interface architecture, signal processing, power optimization, high-speed communication

Software (C, Python, Bash, Make…): build-system architecture, simulation framework infrastructure, interprocessor communications, hardware abstraction

FPGA Gateware (VHDL, Verilog; Lattice, Altera & Xilinx parts): high-speed/high-bandwidth hardware interfaces, real-time signal processing, intelligent clock routing, soft-processors

Selected Professional Experience

Apple — July 2013–Present

Responsible for architecture design, functional specification, behavioral modeling, and spearheading team delivery of new embedded sensing stack solutions. Deliverables include scalable firmware infrastructure design and implementation, custom silicon specification, and system architecture definition.

Lincoln Lab VI-A Fellowship — June–August 2011, January 2012–June 2013

Designed and built a high-speed channel emulator for airborne communication networks to complete an M.Eng. fellowship degree in June, 2013. Created a digital architecture which interfaced FPGAs with fast, high-bandwidth analog hardware in order to apply complex algorithms to a signal stream in real-time. Architected a full-stack framework for emulating environmental effects on wireless signals and modeled Doppler shifting.

MITRE Corp. Internship Program — June–August 2010

Prototyped hardware encryption concept device and demonstrated it to funding authorities. Wrote and live-tested debug software for an aerial communications module. Built FPGA test framework for a GPS hardware interface.

BAE Systems Internship Program — June–August 2009

Designed and implemented FPGA algorithms for sensor defect image correction and data corruption detection in military night vision goggle. Modeled and simulated to prove correctness and tested implementation on physical hardware.

MIT Course Staff — 2009–2012

Lab staff for MIT courses 6.01, 6.004, 6.091, and 6.111.

Education

Massachusetts Institute of Technology (Cambridge, MA)
2012: B.S. VI-2 (EE & CS) **2013**: M.Eng. VI-A (High-Speed Channel Emulation)

Patents

Dynamic adjustment of a sampling rate for an optical encoder, U.S. Patent US9651405 (2017)

Methods and apparatus for rapid switching of hardware configurations with a speed limited bus, U.S. Patent Pending US20160232124