Joseph Colosimo

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Summary

Passionate about architecting and delivering advanced sensing solutions that provide meaningful benefit to human beings. Experienced in constructing optimized embedded sensing stacks—especially for atypically-constrained systems—by leveraging a multi-disciplinary background designing and executing firmware, digital hardware, and platform specifications.

Principle Technical Skills

Embedded System Architecture: translation of feature requirements into system design, SoC & sensor silicon architecture specification, full-stack modeling, end-to-end optimization, interface protocol design

Firmware (C & ASM, ARM systems): core system infrastructure, sensor interface architecture, signal processing, power optimization, high-speed communications, hardware abstraction, silicon bringup

Software (C, Python, Make…): build-system architecture for multi-target low-level code-bases, simulation framework infrastructure, interprocessor communications

Digital Design for FPGAs (VHDL, Verilog): high-bandwidth hardware interfaces, real-time signal processing, CPU (Picoblaze, NIOS II) integration & firmware bringup

Selected Professional Experience

Apple — July 2013–Present

Responsible for architecture design, functional specification, behavioral modeling, and spearheading team delivery of new embedded sensing stack solutions. Deliverables include scalable firmware infrastructure design and implementation, custom silicon specification, and system architecture definition.

Lincoln Lab VI-A Fellowship — June–August 2011, January 2012–June 2013

Designed and built a high-speed channel emulator for airborne communication networks to complete an M.Eng. fellowship degree in June, 2013. Architected a full-stack solution that interfaced FPGAs with high-bandwidth analog hardware and applied real-time algorithms to emulate Doppler shifting.

MITRE Corp. Internship Program — June–August 2010

Prototyped hardware encryption concept and demonstrated it to funding authorities. Built test infrastructure for an aerial communications module. Built FPGA test framework for a GPS hardware device.

BAE Systems Internship Program — June–August 2009

Designed, implemented, and validated FPGA algorithms for sensor defect image correction and data corruption detection in military night vision goggle.

MIT Course Staff — 2009–2012

Lab staff for MIT courses 6.01, 6.004, 6.091, and 6.111.

Education

Massachusetts Institute of Technology (Cambridge, MA)
2012: B.S. Course VI-2 (Electrical Engineering & Computer Science)
2013: M.Eng. EE&CS *Channel Emulation* (J. Francis Reintjes Excellence in 6-A Industrial Practice Award)

Patents

Wireless charging systems with multiple power receiving devices,
U.S. Patents 10,110,030 (2018), 10,277,046 (2019), 10,396,578 (2019), & 10,491,017 (2019)

Methods and apparatus for rapid switching of hardware configurations with a speed limited bus, U.S. Patent 101,021,76 (2018)

Dynamic adjustment of a sampling rate for an optical encoder,
U.S. Patents 9,651,405 (2017) & 10,302,465 (2019)