SMSC™
SUCCESS BY DESIGN

LAN91C111

Frequently Asked Questions

10/100 Non-PCI Ethernet Single Chip MAC and PHY

IMPLEMENTATION

Q: What is the minimum cycle time for each read and write access (synchronous, asynchronous, burst, non-burst)? When do I need wait state?

A: *The minimum cycle time is 80ns for Half Duplex, and 100ns for Full Duplex mode. If cycle time implemented is less than 80ns for Half Duplex or 100ns for Full Duplex, the LAN91C111 will generate wait states to extend cycles.*

Q: What is the maximum frequency for Bus Clock?

A: *The maximum bus clock frequency is 50MHz.*

Q: Does the LAN91C111 calculate the length of each received frame stored in the internal buffer?

A: *Yes, the BYTE COUNT bits and the ODD bit define the total number of words stored in the SRAM. The BYTE COUNT bits always appears as even; the ODD bit indicates that an odd/even number of bytes.*

Q: How do I access the LAN91C111 using 32-bit?

A: *There are two ways to access the LAN91C111, address decode and chip select. We suggest that customers use two chip selects for the LAN91C111 for easy implementation. One chip select signal (for example, CS1) connects to nDATACS for data access; another chip select signal (for example CS2) connects to AEN for register access. When accessing the data register, asserting CS1/nDATACS for a 32-bit read or write, the LAN91C111 will ignore the address and byte enable signals, and data will directly access to the data register. LCLK must be pulled high or clocked for proper operation of 32-bit direct data access. For register access, use address and byte enables for register offset location. Thus, access is possible to each register by 8-bit, 16-bit or 32-bit by asserting appropriate byte enable signals.*

Q: How does the LAN91C111 determine between asynchronous and synchronous mode?

A: *The LAN91C111 can mix asynchronous or synchronous cycles as long as they are not done simultaneously. In order to enter synchronous mode, nRD and nWR must be pulled high; these two pins are for asynchronous bus interfaces. LCLK must be connected to the system bus clock for synchronous bus interface transactions; the control and bus signals are sampled/driven on the rising edge of the bus clock cycle. In synchronous mode, W/nR is used to define the direction of the transfer.*

To switch to an asynchronous mode, assert either nRD or nWR, depending on the type of transfer, pull up LCLK (Local Bus clock is no longer required for asynchronous transfer), pull up W/nR and nRDYRTN (used only for synchronous bus). Note that the nVLBUS pin is not the pin to determine between synchronous or asynchronous modes. It is used to determine between internal and external address qualification burst modes.

Q: How do I enhance system performance and improve throughput?

A:
a. *Minimize each read or write cycle time to 100ns. Thus, a 32-bit system can support up to 320Mbps-bus bandwidth. (The term cycle time means the time from a read/write strobe asserted to the next read/write strobe asserted.)*
b. *Turn on AUTO_RELEASE, the LAN91C111 will automatically release a frame after successfully transmitted.*
c. *Release the receive frame immediately after it is read by the host to free up more memory.*
d. *Use Early Receive by setting ERCV THRESHOLD in the EARLY RCV Register. The host can start to read a receive frame when the number of bytes written in memory for the presently received packet exceeds the ERCV THRESHOLD, it does not need to read a frame until the whole frame to be received.*
e. *Reduce system latency. Please refer to the related descriptions of AN9.6 for detail.*
f. *Optimize the Interrupt Service Routine by reducing assembly instructions.*

Q: How do I set the chip to Full Duplex mode?

A: *Set both the SWFDUP bit in the Transmit Control Register and the DPLX bit in the Receive/PHY Control Register.*

Q: How do I set the chip to 100Mbps mode manually with auto-negotiation mode off?

A: *Set the SPEED bit in the Receive/PHY Control Register.*

Q: Which bits control Auto-Negotiation mode?

A: *The ANEG bit in the Receive/PHY Control Register and the ANEG_EN bit in the MI PHY Control Register control the Auto-Negotiation mode. To turn on Auto-Negotiation, both bits have to be set, but clearing either these two bits can disable Auto-Negotiation.*

Q: Is the serial EEPROM always required?

A: *No. The serial EEPROM provides a convenient way for storing non-volatile default information like the node's unique IEEE address, configuration register, and base address*

If the host CPU is capable of supplying the above information during initialization the serial EEPROM can be eliminated by grounding the ENEEP. The LAN91C111 will not attempt to read the EEPROM and will use hardware default information, as described in the device's Data sheets.

If the IEEE address is the only parameter to be stored in the serial EEPROM, ENEEP as well as IOS0-2 should be left open. The 91C111 will use hardware defaults for all parameters except the IEEE address.

If ENEEP is left open, and any IOS0-2 is grounded, the 91C111 will read all of its configuration information from the serial EEPROM.

Q: How do I program the IO BASE address, Configuration Register and MAC address if EEPROM is not present?

A: *Please refer to section 4.4 of the Technical Reference Manual AN96 for details, as well as the related descriptions of the latest LAN91C111 Data Sheet.*

Q: How do I write a MAC address to the LAN91C111?

A: *A MAC address should be written to the Individual Address Register of the LAN91C111. Bit 0 of Individual Address 0 Register corresponds to the first bit of the MAC address on the cable. For example, if the MAC*

address is 0123 4567 89AB, the corresponding 6 bytes of individual address should be written as 2301 6745 AB89. Individual address byte 1 and byte 0 should be written as 2301, and Individual address byte 3 and byte 2 should be written as 6745 and so on.

Q: How do I handle Endian problem if I have a big Endian processor?

A: *For big-Endian environments the 91C111 data bus bytes should be swapped. For a 16-bit bus, for example, connect the 91C111 D0-7 to the bus D8-15 and vice versa. By doing this all register's appear swapped to the CPU, and the CPU can move data to and from the DATA REGISTER without having to swap the bytes in software.*

For a 32-bit bus connect D0-7 to D24-31 and so on.
The SMC91C111 is a slave and does not manage any data structures in the system memory, therefore the bus swapping has no adverse side-effects. For more information, call your local SMSC rep for an application note.

Q: How do I Mask or Enable the Interrupts of the MAC and the PHY?

A: *For the internal MAC, interrupt status bits (Bank 2, Offset C- Interrupt Status Registers) are enabled when the appropriate interrupt mask bits (Bank2, Offset D – Interrupt Mask Registers) are 1. In other words, if the interrupt mask bit is 0, the appropriate interrupt status bit remains 0, even its status is changed. Thus no interrupt will be generated.*

For the internal PHY, register 19 – Mask Registers are used to control register 18 Status Output Registers. If the Mask Register bit is set to 1, it will disable the appropriate status interrupt bit. If the Mask Register bit is clear, it will enable the appropriate status interrupt bit.

Q: How does the internal DMA work?

A: *The DMA block of the Ethernet controller is an internal Direct Memory Access block. It is responsible to move received data into the internal SRAM and send transmitted data from the internal SRAM to the transmitter. When data is received from the PHY, the internal EPH block converts the data from a 4-bit data stream to a 16-bit data stream to the DMA block; data is then converted to a 32-bit format and temporarily stored in a small-receive FIFO. The DMA block generates a receive DMA request to the internal Arbiter to determine whether it has the right to access the internal SRAM. Since the internal arbiter handles the arbitration between the BIU (Bus Interface Unit) and DMA to read or write from/to the internal SRAM, if the arbiter granted the access to the BIU to access the SRAM before the receive DMA request is generated, the arbiter will hold the access from the DMA block to the SRAM until the BIU completes its process to the SRAM. If the internal SRAM is free to be access, the arbiter will grant the DMA block to access the internal SRAM immediately.*

Q: What operating systems drivers are currently for the LAN91C111 Ethernet controllers?

A: *At this time, the following operating system environments are available:*

Windows 98/ME/NT/2000	-	*Standard Desktop Hardware*
Win CE.NET	-	*x86 Platform*
Windows CE 3.0	-	*x86 Platform*
VxWorks	-	*x86 Platform*
Linux	-	*x86 Platform*
DOS ODI Driver	-	*x86 Platform (Novell 4.1x & 16bit clients)*
Packet Driver	-	*x86 Platform*

Q: How do I find these drivers?

A: *Most of the driver binaries are available on the SMSC web site (http://www.smsc.com). For source code please contact your SMSC sales representatives.*

Q: When do I need to modify the LAN91C111 drivers, and how can I get access to the software driver source code?

A: The LAN91C111 drivers were written for the PC environment, and they work well for all major operating systems and in Programmed Input/Output (non-bus master) mode with ISA, PC/104, VL and PCMCIA bus interfaces. As long as you follow the design instructions in the SMSC chip specification (such as using the correct IRQ lines...) you should be able to use LAN91C111 drivers for your product.

The following are some reasons why one would need to modify the LAN91C111 drivers:

Need to interface to a bus not supported by the LAN91C111 drivers: In most cases, such as with the Microchannel and EISA bus in non-bus master mode, the modification to the drivers need only be made in the initialization, and are relatively minor.

Need to interface to a non-PC compatible computer.

Need to interface with an operating system not yet supported by the LAN91C111 drivers: If you need support for a new operating system, please contact your local SMSC rep., who will see what SMSC can do to help you in this effort.

Please contact your local SMSC rep. if you need LAN91C111 source code.

Q: Is there a design and layout check guideline info?

A: It's recommended to download and always refer to the latest updated LAN91C111 Data Sheet, the SMSC reference design schematics, and other useful referring information which has all been posted on SMSC web site;

Please refer to SMSC web site ---Ethernet Products---LAN Check Services, download the related update guidelines of design and layout checking information for your general checking guidelines:

1. Schematics Checking List
2. Layout Component Placement Check List
3. Routing Check List
4. Test Procedures
5. EMI/ FCC Reduction Doc

TROUBLESHOOTING

1. The chip drops the first 3 frames it receives after it powers up.

   Check the TX and RX pair polarity of the connections to the magnetics.

2. I am unable to read all the registers including the MAC and the internal PHY.

   Check if the RBIAS resistor value is 11K Ohm.

3. The Ethernet controller could not establish link to either 10BASE-T or 100BASE-TX Hub or Switch.

   Please check the following settings: a) RBIAS value is 11Kohm, b) MII_DIS bit in the PHY Control Register is cleared, c) Input Oscillator clock or Crystal meets the requirement listed in Application note AN9.6.

4. How to debug the chip if it has some abnormal responses?

   The LAN91C111 consists with these three big blocks: MAC, PHY and SRAM.

   To debug a chip, you need to find out where exactly the problem is. For the LAN91C111, you may perform some functional tests to diagnostic the LAN91C111. These tests will exercise the major blocks. Please refer to the related descriptions of application note 9.6 for detail.

5. The Ethernet controller is unable to Auto-Negotiate with a remote hub or switch.

   Please refer to section 4.7 Auto negotiation of Application Note 9.6 for detail procedures.

6. The host is not able to receive any interrupt from the LAN91C111.

   Please check if the appropriate bits in the interrupt mask register is set to cause a hardware interrupt.

7. I am unable to access the PHY, or I always read 0000 in the PHY register.

   a. *To access the internal PHY, please check the following procedures:*
   b. *EXT PHY bit in the Configuration Register is clear.*
   c. *EPH_Power_EN bit in the Configuration Register is set.*
   d. *PDN bit in the PHY Control Register is clear.*
   e. *MII_DIS bit in the PHY Control Register is clear.*
   f. *11K Ohm resistor connected between RBIAS pin and ground.*
   g. *Reading or writing to the PHY using address of 00000.*
   h. *Please refer to related descriptions of application note 9.6 for detail.*

8. Allocation for Transmit fails.

   Check if the internal buffer is full or not. If it is full, release the transmitted frames and the received frames that have been read by host to free up more memory. Then perform allocation command again; poll Allocation Interrupt to see if allocation is completed.

9. The LAN91C111 could not receive any packets.

    a. Check the following conditions:
    b. RXEN bit is set
    c. Internal buffer has free memory available
    d. RBIAS resistor value is 11Kohm
    e. RXINT Mask bit is set, so that it can generate an interrupt after the LAN91C111 completely receive one frame

10. Overrun occurs during heavy traffic or received packet drops frequently.

    Please see Implementation section to tune up system performance.

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