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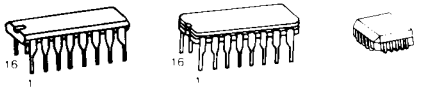
PRODUCT PREVIEW

3 TO 8 LINE DECODER LATCH

DESCRIPTION

The M54/74HC237 is a high speed CMOS 3 TO 8 LINE DECODER LATCH fabricated in silicon gate C²MOS technology.
It has the same high speed performance of LSTTL combined with true CMOS low power consumption. When LE goes from low to high, the address present at the select inputs (A0, A1, A2) is stored in the latches. As long as LE remains high no address changes will be recognized. Output enable controls, CS1 and CS2 control the state of the outputs independantly of the select or latch-enable inputs. All of the outputs are low unless CS1 is high and CS2 is low. The 'HC237 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



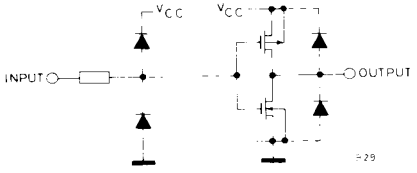
B1 Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

ORDERING NUMBERS: M54HC237 F1
M74HC237 B1
M74HC237 F1
M74HC237 C1

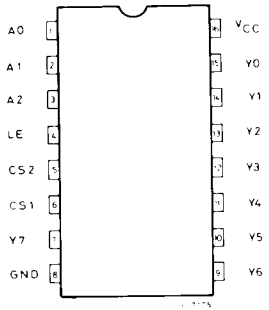
FEATURES

- Low Power Dissipation
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible with 54/74LS237

INPUT AND OUTPUT EQUIVALENT CIRCUIT

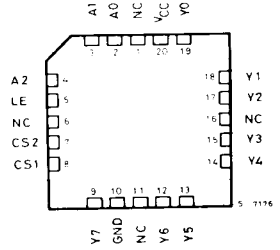


PIN CONNECTIONS
(top view)



Dual in line

CHIP CARRIER



NC = No Internal Connection

TRUTH TABLE

INPUTS						OUTPUTS							
LE	CS_1	CS_2	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	*	*	*	*	*	*	*	*

X = Don't care

* = Depends upon the select data previously, applied while LE was at a logic low.